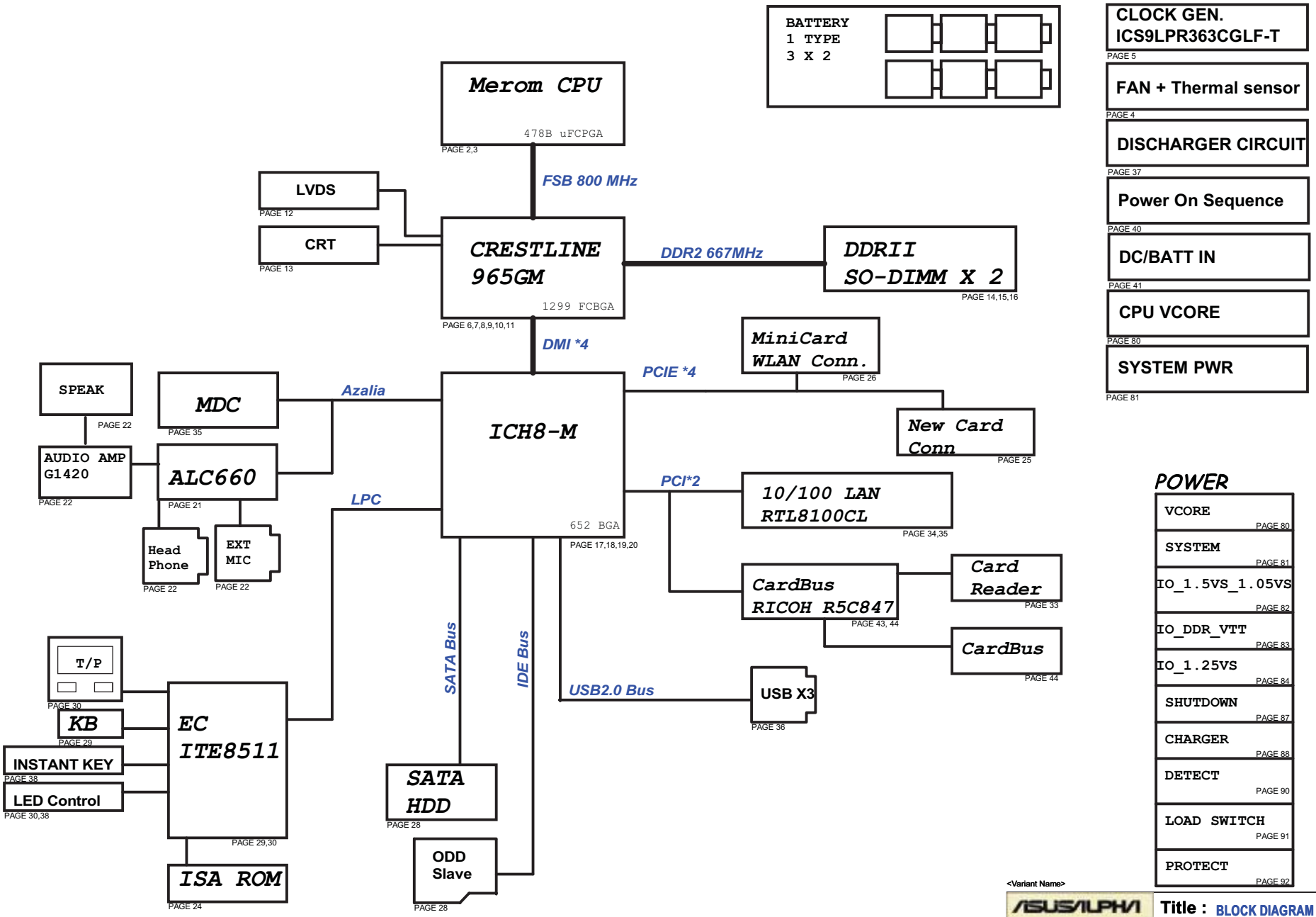
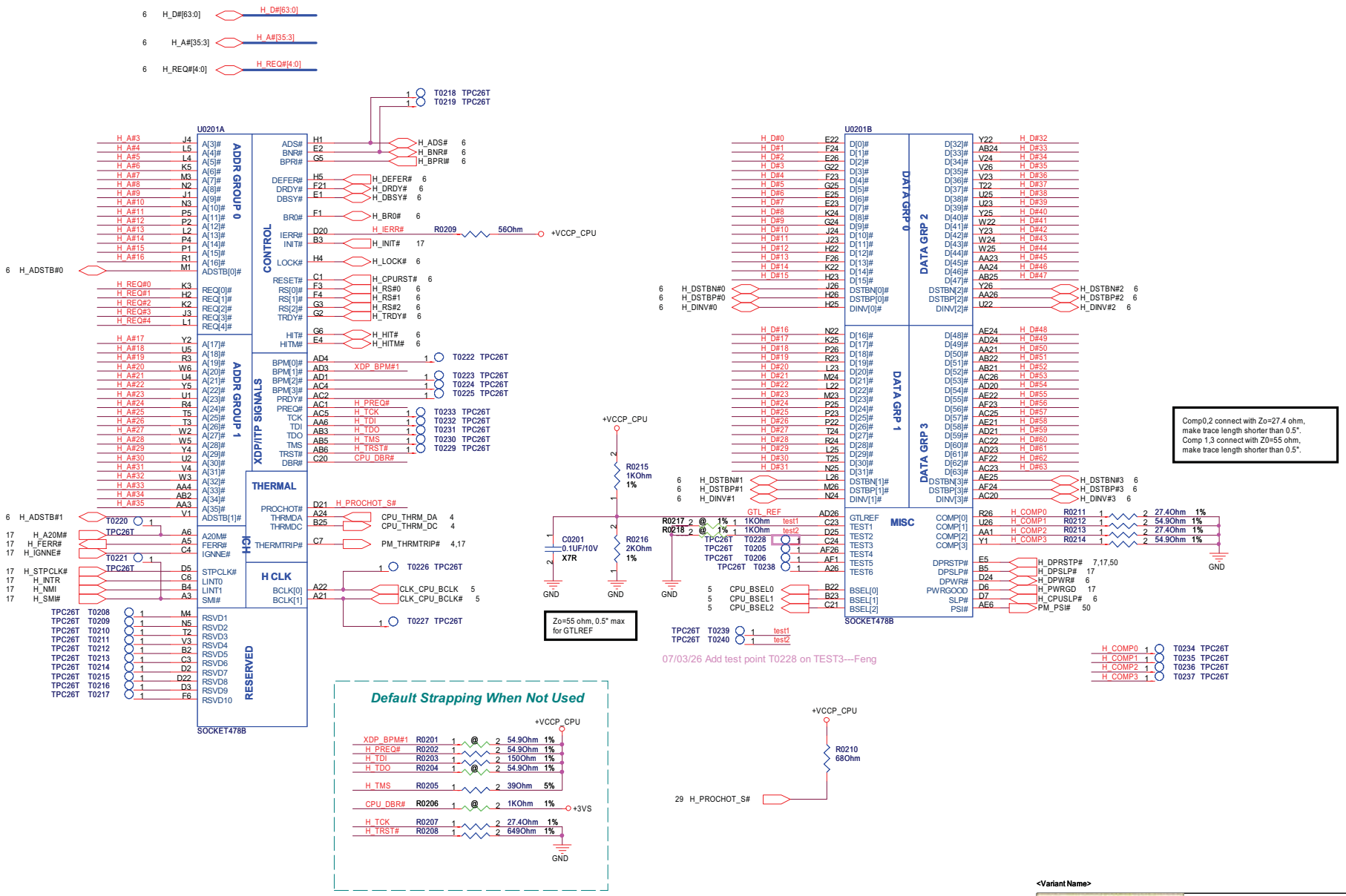
TERESA20 Main BD. R2.0 BLOCK DIAGRAM



<Variant Name>

ASUSALPHA	Title : BLOCK DIAGRAM	
ASUSALPHATeK COMPUTER INC.	Engineer: Julian Kuo	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 1 of 66	



<Variant Name>

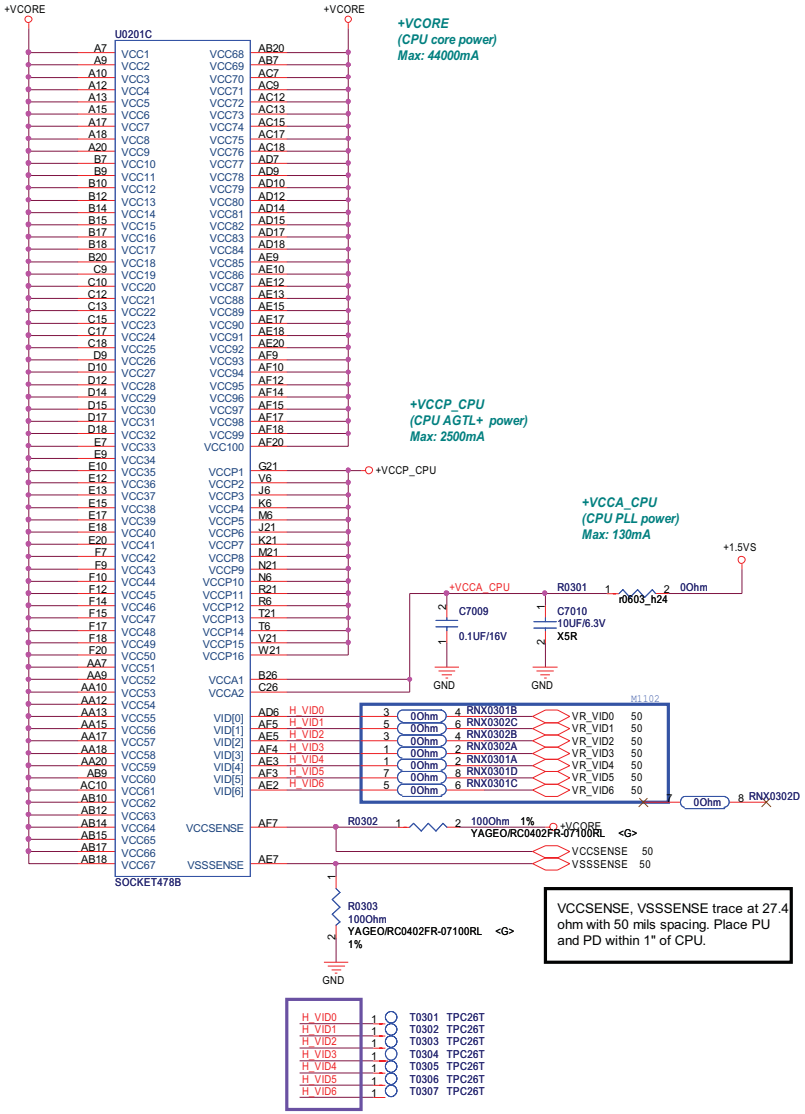
ASUSALPHATeK COMPUTER INC.	Title : MEROM CPU (1)
	Engineer: Julian Kuo
Size: Custom	Project Name: TERESA20
Rev: 2.0	
Date: Thursday, July 05, 2007	Sheet 2 of 66

Decoupling guide from INTEL Schematic Design Checklist Rev 1.6

VCORE 22uF/10V * 32pcs
330uF/2V * 6pcs

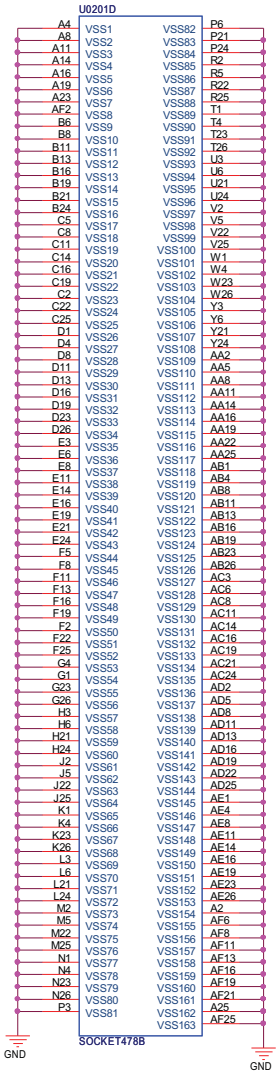
Decoupling guide from INTEL Layout Checklist Rev 2.0

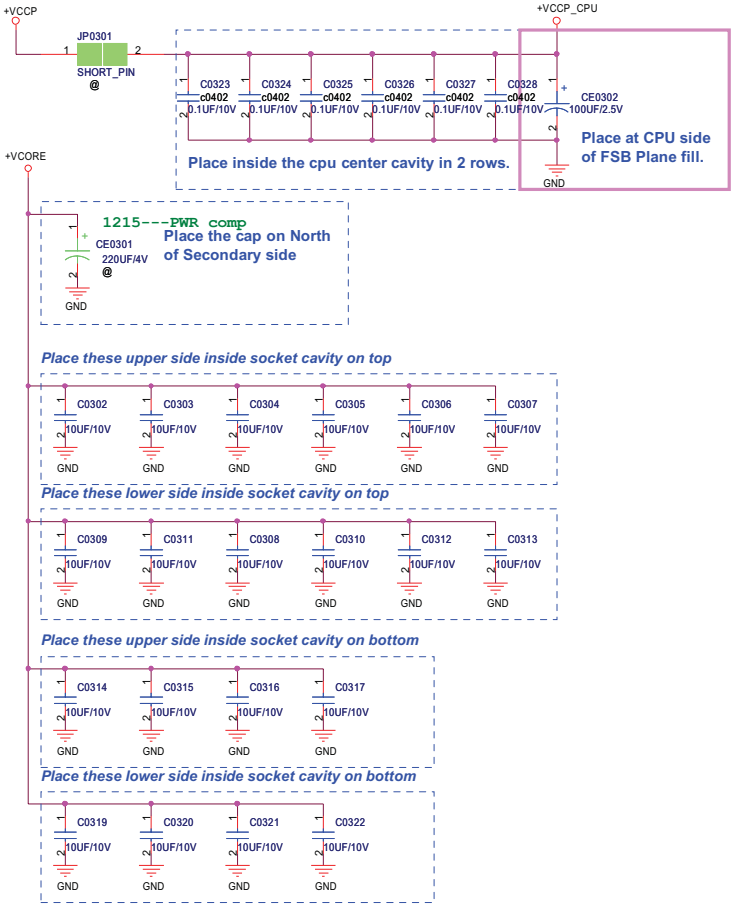
VCCP 0.1uF * 6pcs
220uF * 1pcs



VCCSENSE, VSSSENSE trace at 27.4 ohm with 50 mils spacing. Place PU and PD within 1" of CPU.

07/05/04 To add test point on VID[0:6] signals. --- iverson

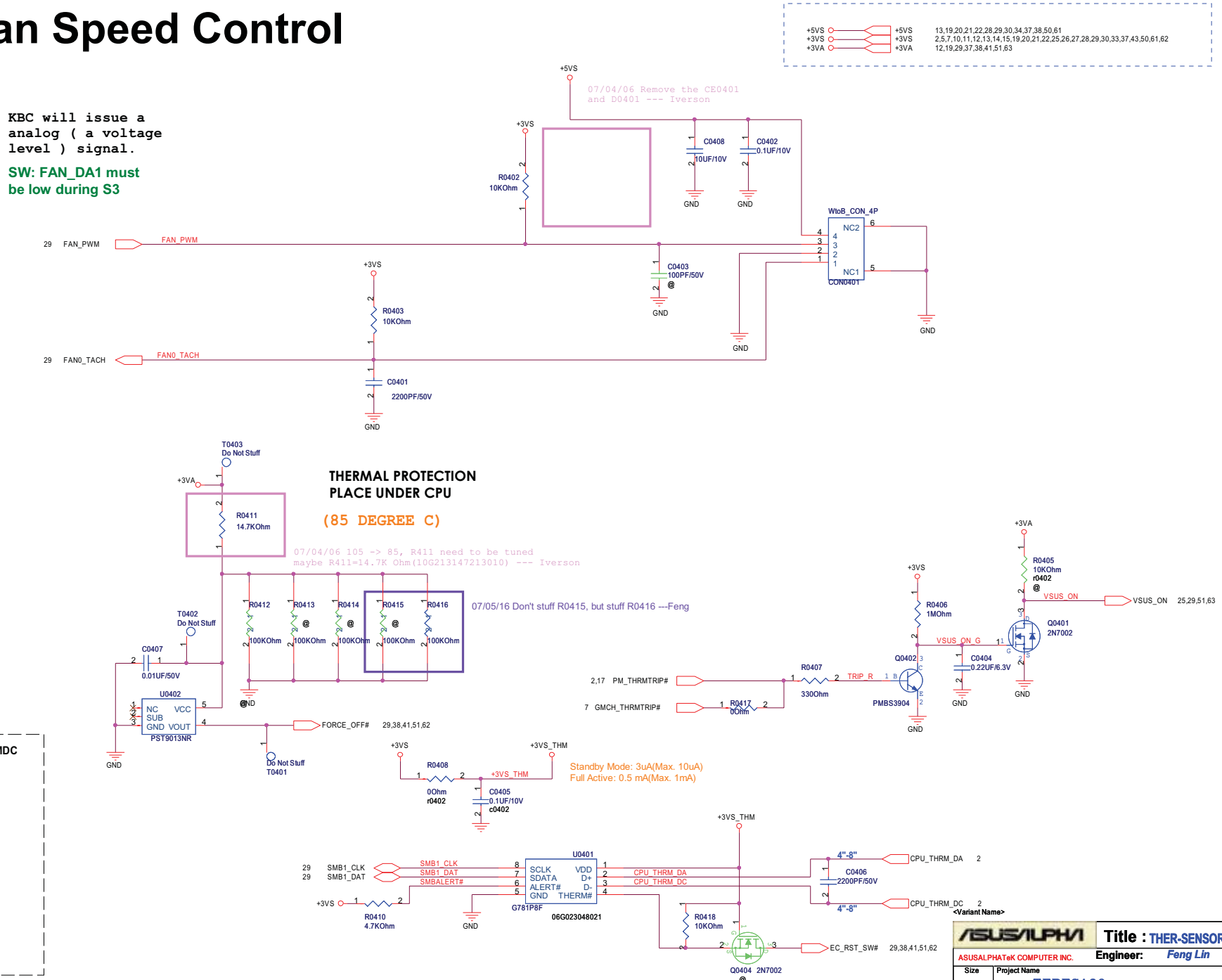


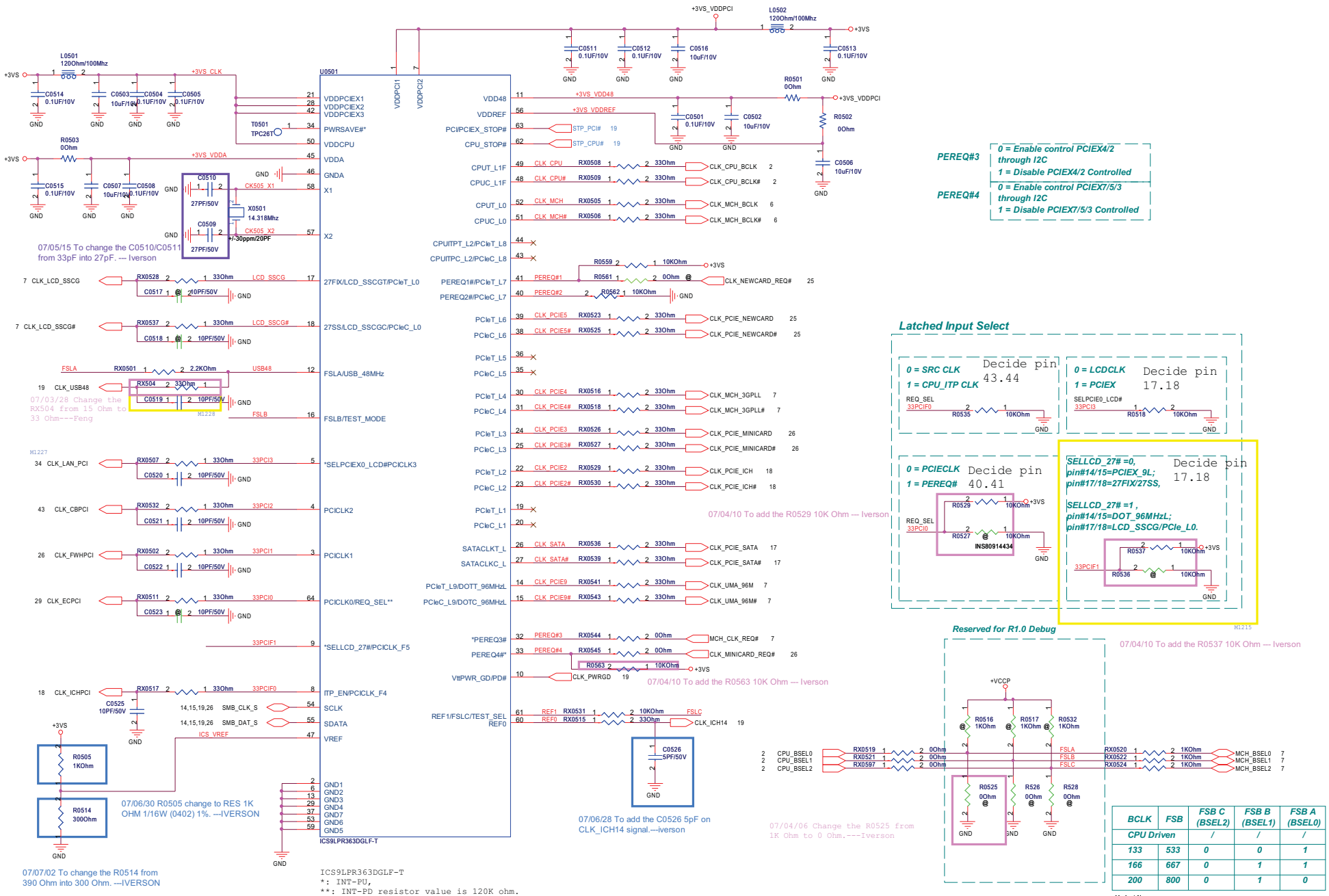


<Variant Name>

ASUSALPHA	Title : MEROM CPU (2)	
ASUSALPHATeK COMPUTER INC.	Engineer: Julian Kuo	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 3 of 66	

Fan Speed Control





BCLK	FSB	FSB C (BSEL2)	FSB B (BSEL1)	FSB A (BSEL0)
CPU Driven		/	/	/
133	533	0	0	1
166	667	0	1	1
200	800	0	1	0

<Variant Name>

ASUSALPHA

Title : CLK GEN

ASUSALPHATeK COMPUTER INC.

Engineer: Julian Kuo

Size: Custom | Project Name: TERESA20 | Rev: 2.0

Date: Thursday, July 05, 2007 | Sheet 5 of 66

RCOMP

For Calibrating the FSB I/O Buffer

H_RCOMP

T 10mils/S 20mils

R0601 24.9Ohm 1%

GND

SCOMP

For Slew Rate Compenssation on the FSB

+VCCP — R0602 54.9Ohm 1% — H_SCOMP

+VCCP — R0603 54.9Ohm 1% — H_SCOMP#

Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP circuits

+VCCP — R0604 221Ohm 1% — H_SWING

R0605 100Ohm 1% — GND

C0601 0.1UF/10V X7R — GND

+VCCP — R0606 1KOhm 1% — H_AVREF

T 10mils/L 500mils/S 25mils

R0608 0Ohm — H_DVREF

R0607 2KOhm 1% — GND

C0602 0.1UF/10V X7R — GND

U0601A

HOST

2 H_D#[63:0]

H_D#0	E2	H_D#_0	
H_D#1	G2	H_D#_1	
H_D#2	G7	H_D#_2	
H_D#3	M6	H_D#_3	
H_D#4	H7	H_D#_4	
H_D#5	H3	H_D#_5	
H_D#6	G4	H_D#_6	
H_D#7	F3	H_D#_7	
H_D#8	N8	H_D#_8	
H_D#9	H2	H_D#_9	
H_D#10	M10	H_D#_10	
H_D#11	N12	H_D#_11	
H_D#12	N9	H_D#_12	
H_D#13	H5	H_D#_13	
H_D#14	P13	H_D#_14	
H_D#15	K9	H_D#_15	
H_D#16	M2	H_D#_16	
H_D#17	W10	H_D#_17	
H_D#18	Y8	H_D#_18	
H_D#19	V4	H_D#_19	
H_D#20	M3	H_D#_20	
H_D#21	J1	H_D#_21	
H_D#22	N5	H_D#_22	
H_D#23	N3	H_D#_23	
H_D#24	W6	H_D#_24	
H_D#25	W9	H_D#_25	
H_D#26	N2	H_D#_26	
H_D#27	Y7	H_D#_27	
H_D#28	Y9	H_D#_28	
H_D#29	P4	H_D#_29	
H_D#30	W3	H_D#_30	
H_D#31	N1	H_D#_31	
H_D#32	AD12	H_D#_32	
H_D#33	AE3	H_D#_33	
H_D#34	AD9	H_D#_34	
H_D#35	AC9	H_D#_35	
H_D#36	AC7	H_D#_36	
H_D#37	AC14	H_D#_37	
H_D#38	AD11	H_D#_38	
H_D#39	AC11	H_D#_39	
H_D#40	AB2	H_D#_40	
H_D#41	AD7	H_D#_41	
H_D#42	AB1	H_D#_42	
H_D#43	Y3	H_D#_43	
H_D#44	AC6	H_D#_44	
H_D#45	AE2	H_D#_45	
H_D#46	AC5	H_D#_46	
H_D#47	AG3	H_D#_47	
H_D#48	AJ9	H_D#_48	
H_D#49	AH8	H_D#_49	
H_D#50	AJ14	H_D#_50	
H_D#51	AE9	H_D#_51	
H_D#52	AE11	H_D#_52	
H_D#53	AH12	H_D#_53	
H_D#54	AJ5	H_D#_54	
H_D#55	AH5	H_D#_55	
H_D#56	AJ6	H_D#_56	
H_D#57	AE7	H_D#_57	
H_D#58	AJ7	H_D#_58	
H_D#59	AJ2	H_D#_59	
H_D#60	AE5	H_D#_60	
H_D#61	AJ3	H_D#_61	
H_D#62	AH2	H_D#_62	
H_D#63	AH13	H_D#_63	

H_SWING	B3	H_SWING	
H_RCOMP	C2	H_RCOMP	
H_SCOMP	W1	H_SCOMP	
H_SCOMP#	W2	H_SCOMP#	
2 H_CPURST#	B6	H_CPURST#	
2 H_CPUSLP#	E5	H_CPUSLP#	
H_AVREF	B9	H_AVREF	
H_DVREF	A9	H_DVREF	

H_A#_3	J13	H_A#3	H_A#[35:3] 2
H_A#_4	B11	H_A#4	
H_A#_5	C11	H_A#5	
H_A#_6	M11	H_A#6	
H_A#_7	C15	H_A#7	
H_A#_8	F16	H_A#8	
H_A#_9	L13	H_A#9	
H_A#_10	G17	H_A#10	
H_A#_11	C14	H_A#11	
H_A#_12	K16	H_A#12	
H_A#_13	B13	H_A#13	
H_A#_14	L16	H_A#14	
H_A#_15	J17	H_A#15	
H_A#_16	B14	H_A#16	
H_A#_17	K19	H_A#17	
H_A#_18	P15	H_A#18	
H_A#_19	R17	H_A#19	
H_A#_20	B16	H_A#20	
H_A#_21	H20	H_A#21	
H_A#_22	L19	H_A#22	
H_A#_23	D17	H_A#23	
H_A#_24	M17	H_A#24	
H_A#_25	N16	H_A#25	
H_A#_26	J19	H_A#26	
H_A#_27	B18	H_A#27	
H_A#_28	E19	H_A#28	
H_A#_29	B17	H_A#29	
H_A#_30	B15	H_A#30	
H_A#_31	E17	H_A#31	
H_A#_32	C18	H_A#32	
H_A#_33	A19	H_A#33	
H_A#_34	B19	H_A#34	
H_A#_35	N19	H_A#35	

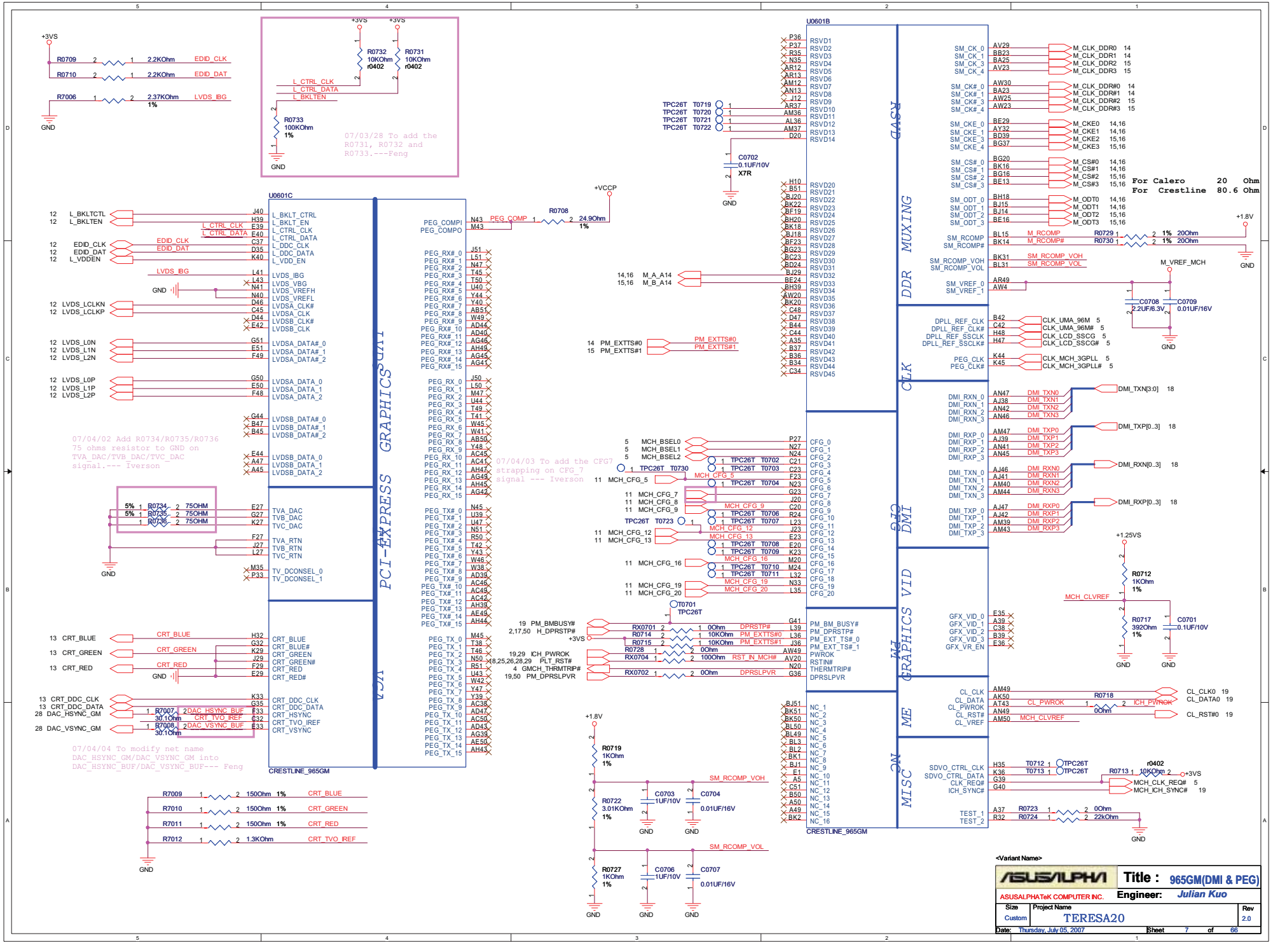
H_ADS#	G12	H_ADS# 2
H_ADSTB#_0	H17	H_ADSTB#0 2
H_ADSTB#_1	G20	H_ADSTB#1 2
H_BNR#	C8	H_BNR# 2
H_BPRI#	E8	H_BPRI# 2
H_BREQ#	F12	H_BR0# 2
H_DEFER#	D6	H_DEFER# 2
H_DBSY#	C10	H_DBSY# 2
HPLL_CLK	AM5	CLK_MCH_BCLK 5
HPLL_CLK#	AM7	CLK_MCH_BCLK# 5
H_DPWR#	H8	H_DPWR# 2
H_DRDY#	K7	H_DRDY# 2
H_HIT#	E4	H_HIT# 2
H_HITM#	C6	H_HITM# 2
H_LOCK#	G10	H_LOCK# 2
H_TRDY#	B7	H_TRDY# 2

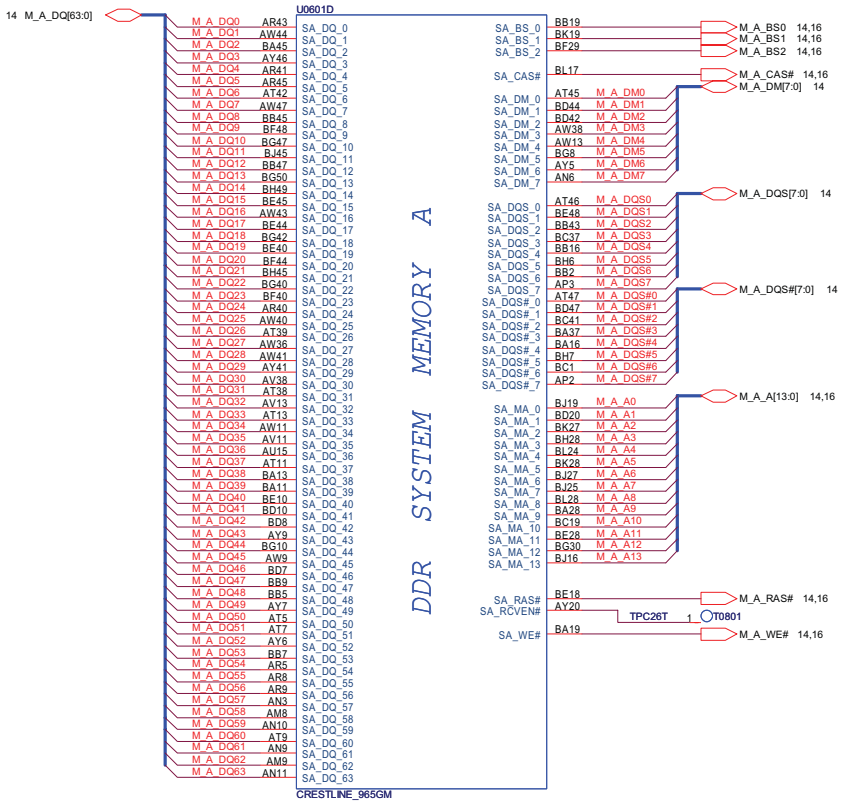
H_DINV#_0	K5	H_DINV#0 2
H_DINV#_1	L2	H_DINV#1 2
H_DINV#_2	AD13	H_DINV#2 2
H_DINV#_3	AE13	H_DINV#3 2
H_DSTBN#_0	M7	H_DSTBN#0 2
H_DSTBN#_1	K3	H_DSTBN#1 2
H_DSTBN#_2	AD2	H_DSTBN#2 2
H_DSTBN#_3	AH11	H_DSTBN#3 2
H_DSTBP#_0	L7	H_DSTBP#0 2
H_DSTBP#_1	K2	H_DSTBP#1 2
H_DSTBP#_2	AC2	H_DSTBP#2 2
H_DSTBP#_3	AJ10	H_DSTBP#3 2
		H_REQ#[4:0] 2
H_REQ#_0	M14	H_REQ#0
H_REQ#_1	E13	H_REQ#1
H_REQ#_2	A11	H_REQ#2
H_REQ#_3	H13	H_REQ#3
H_REQ#_4	B12	H_REQ#4
H_RS#_0	E12	H_RS#0 2
H_RS#_1	D7	H_RS#1 2
H_RS#_2	D8	H_RS#2 2

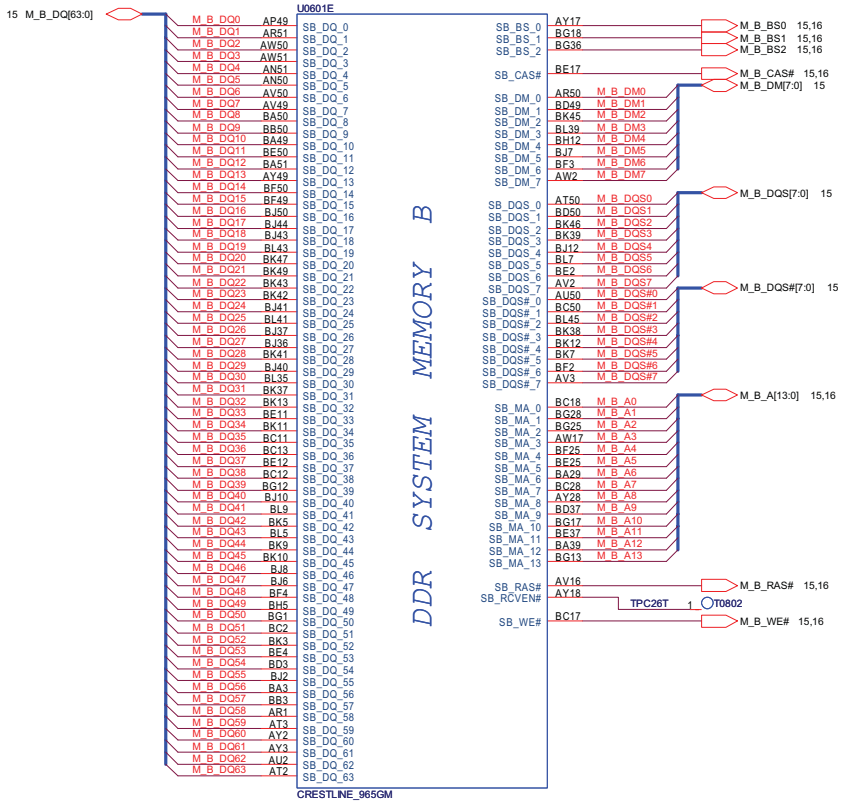
CRESTLINE_965GM

<Variant Name>

ASUSALPHA	Title :	NB-965GM (HOST)	
ASUSALPHATeK COMPUTER INC.	Engineer:	Julian Kuo	
Size: Custom	Project Name: TERESA20		Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 6 of 66		

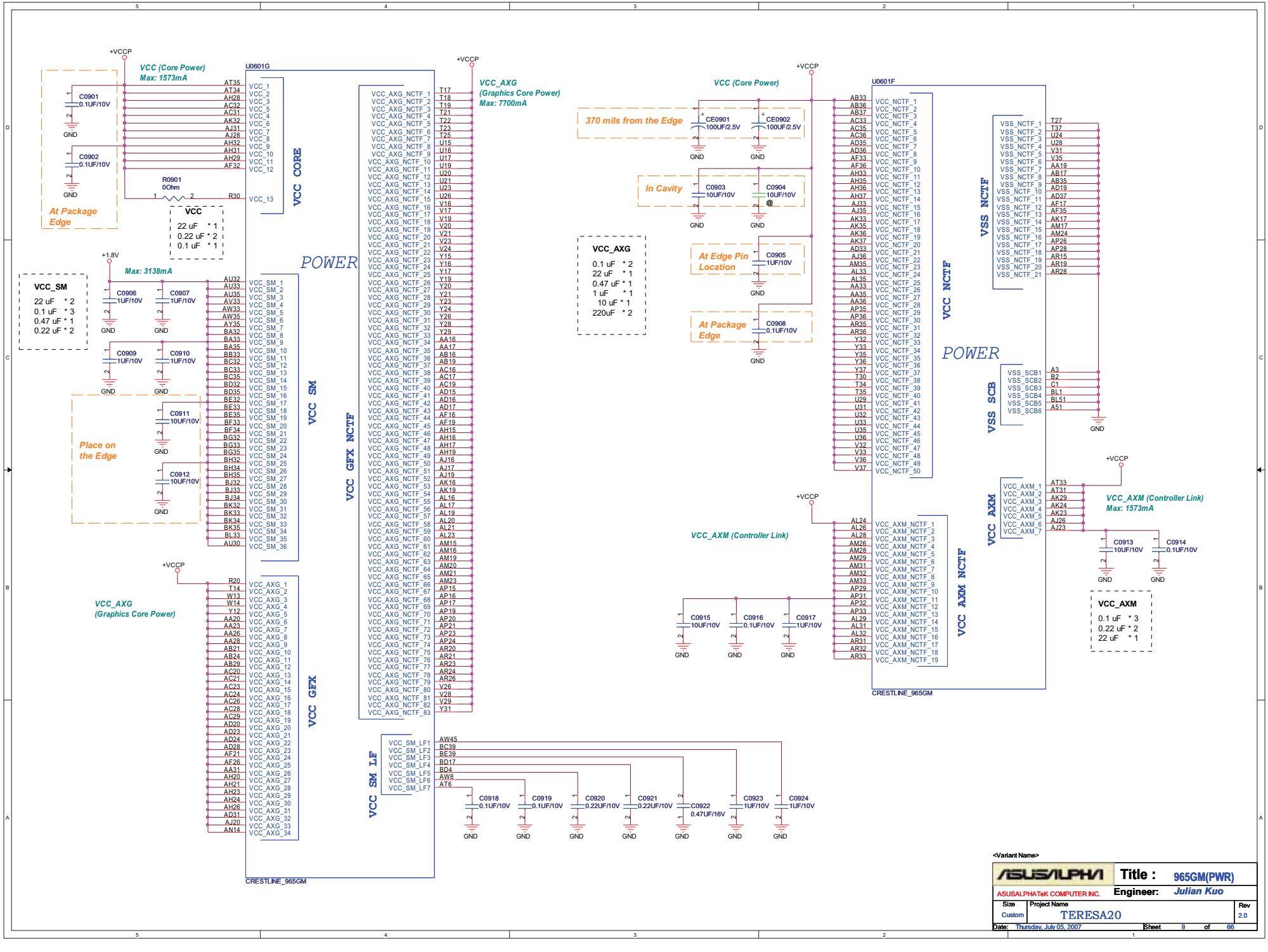

U0601B
U0601C
CRESTLINE_965GM
PCI-EXPRESS GRAPHICS
DDR MUXING
CLK
DMI
CFG
GRAPHICS VID
ME
MISC
For Calero 20 Ohm
For Crestline 80.6 Ohm
07/03/28 To add the R0731, R0732 and R0733.---Feng
07/04/02 Add R0734/R0735/R0736 75 ohms resistor to GND on TVA_DAC/TVB_DAC/TVC_DAC signal.--- Iverson
07/04/03 To add the CFG7 strapping on CFG_7 signal --- Iverson
07/04/04 To modify net name DAC_HSYNC_GM/DAC_VSYNC_GM into DAC_HSYNC_BUF/DAC_VSYNC_BUF--- Feng
Title : 965GM(DMI & PEG)
ASUSALPHATeK COMPUTER INC.
Engineer: Julian Kuo
Size Custom
Project Name TERESA20
Rev 2.0
Date: Thursday, July 05, 2007
Sheet 7 of 66

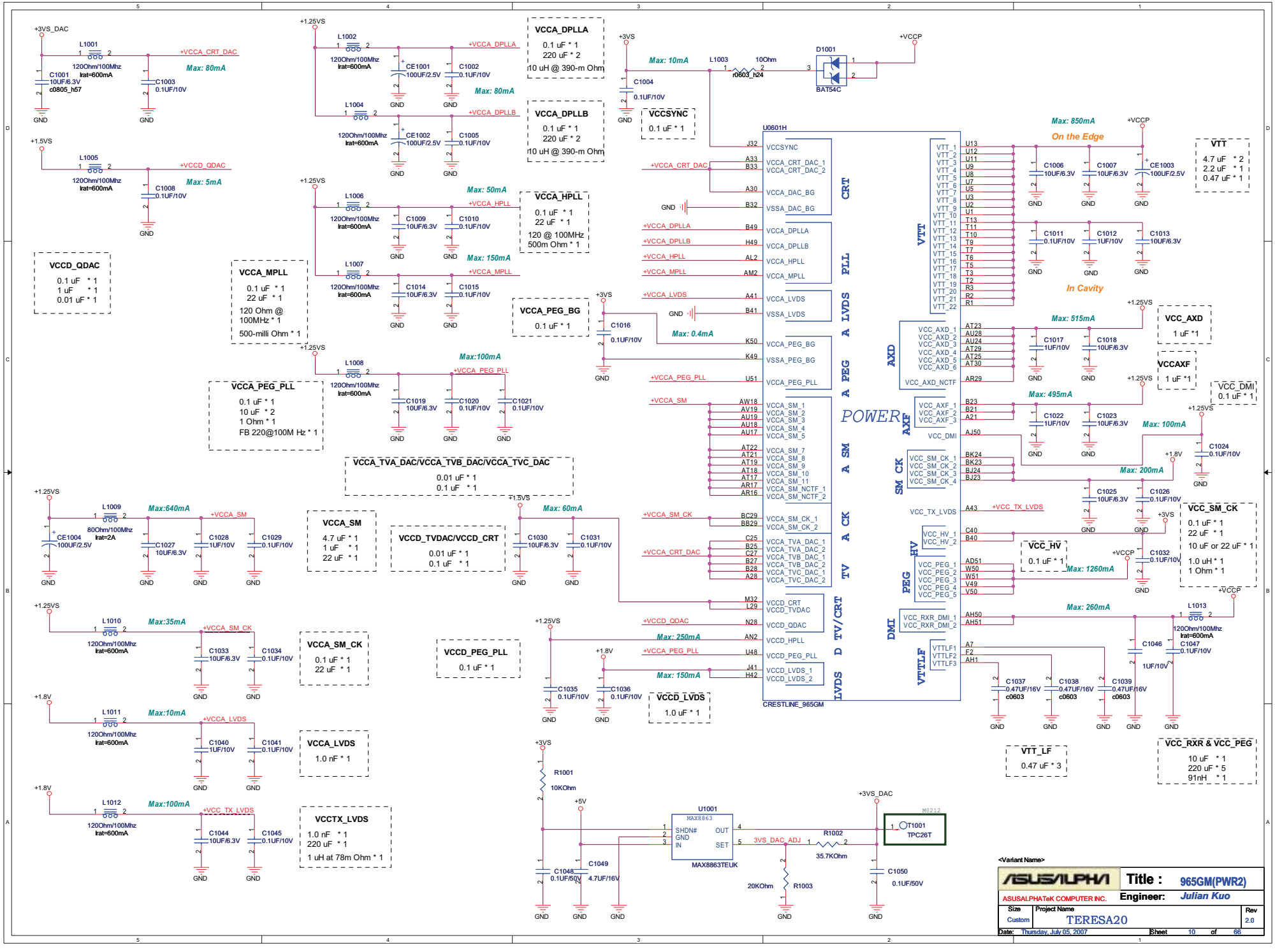


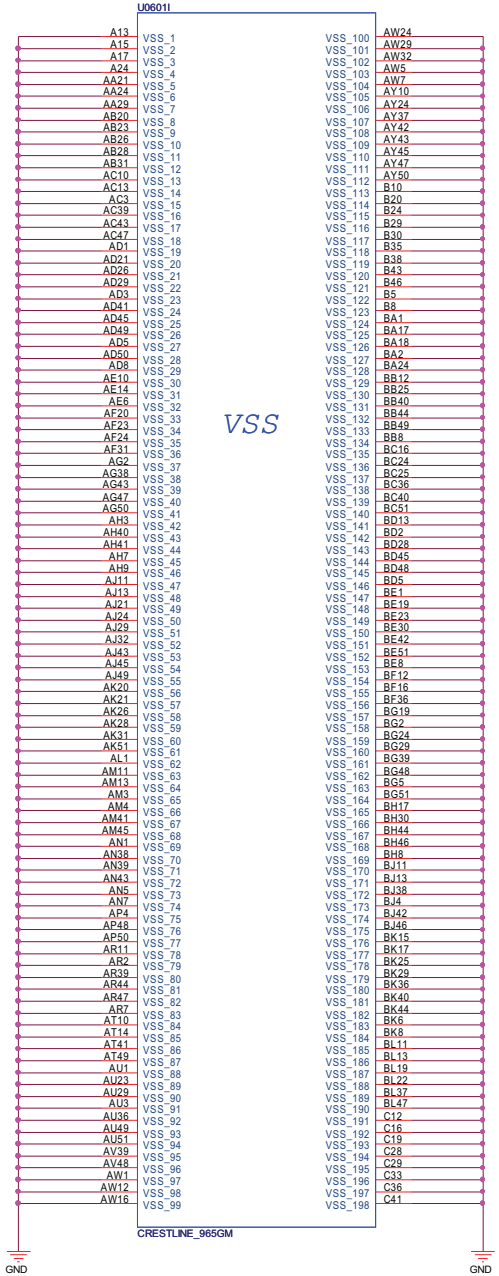


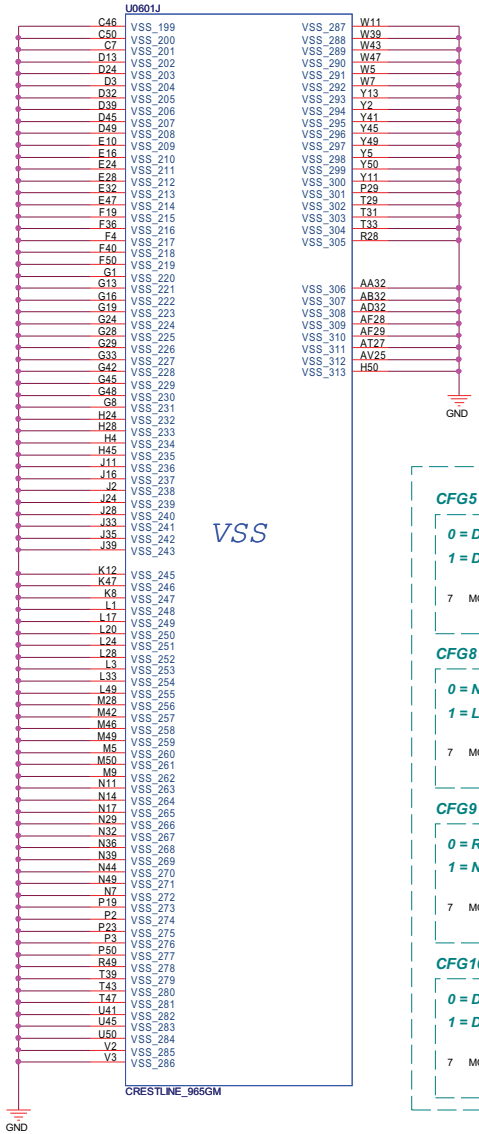
<Variant Name>

ASUSALPHA	Title : 965GM(DDR2)		
ASUSALPHATeK COMPUTER INC.	Engineer: Julian Kuo		
Size: Custom	Project Name: TERESA20		Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 8 of 66		


U0601G
U0601F
POWER
VCC CORE
VCC SM
VCC GFX NCTF
VCC GFX
VCC SM LF
VCC NCTF
VSS NCTF
VSS SCB
VCC AXM
VCC AXM NCTF
VCC (Core Power)
Max: 1573mA
VCC_AXG
(Graphics Core Power)
Max: 7700mA
Max: 3138mA
VCC_AXM (Controller Link)
Max: 1573mA
370 mils from the Edge
In Cavity
At Edge Pin Location
At Package Edge
Place on the Edge
VCC
22 uF * 1
0.22 uF * 2
0.1 uF * 1
VCC_SM
22 uF * 2
0.1 uF * 3
0.47 uF * 1
0.22 uF * 2
VCC_AXG
0.1 uF * 2
22 uF * 1
0.47 uF * 1
1 uF * 1
10 uF * 1
220uF * 2
VCC_AXM
0.1 uF * 3
0.22 uF * 2
22 uF * 1
CRESTLINE_965GM
+VCCP
+1.8V
GND
R0901
0Ohm
C0901 0.1UF/10V
C0902 0.1UF/10V
CE0901 100UF/2.5V
CE0902 100UF/2.5V
C0903 10UF/10V
C0904 10UF/10V
C0905 1UF/10V
C0906 1UF/10V
C0907 1UF/10V
C0908 0.1UF/10V
C0909 1UF/10V
C0910 1UF/10V
C0911 10UF/10V
C0912 10UF/10V
C0913 10UF/10V
C0914 0.1UF/10V
C0915 10UF/10V
C0916 0.1UF/10V
C0917 1UF/10V
C0918 0.1UF/10V
C0919 0.1UF/10V
C0920 0.22UF/10V
C0921 0.22UF/10V
C0922 0.47UF/16V
C0923 1UF/10V
C0924 1UF/10V
ASUSALPHA
Title : 965GM(PWR)
ASUSALPHATeK COMPUTER INC.
Engineer: Julian Kuo
Size Custom
Project Name TERESA20
Rev 2.0
Date: Thursday, July 05, 2007
Sheet 9 of 66


+3VS_DAC
L1001
120Ohm/100Mhz
Irat=600mA
C1001
10UF/6.3V
c0805_h57
+VCCA_CRT_DAC
Max: 80mA
C1003
0.1UF/10V
GND
+1.25VS
L1002
+VCCA_DPLLA
CE1001
100UF/2.5V
C1002
0.1UF/10V
Max: 80mA
L1004
+VCCA_DPLLB
CE1002
100UF/2.5V
C1005
0.1UF/10V
VCCA_DPLLA
0.1 uF * 1
220 uF * 2
10 uH @ 390-m Ohm
VCCA_DPLLB
0.1 uF * 1
220 uF * 2
10 uH @ 390-m Ohm
+1.5VS
L1005
+VCCD_QDAC
C1008
0.1UF/10V
Max: 5mA
VCCD_QDAC
0.1 uF * 1
1 uF * 1
0.01 uF * 1
L1006
+VCCA_HPLL
Max: 50mA
C1009
10UF/6.3V
C1010
0.1UF/10V
VCCA_HPLL
0.1 uF * 1
22 uF * 1
120 @ 100MHz
500 Ohm * 1
L1007
+VCCA_MPLL
Max: 150mA
C1014
10UF/6.3V
C1015
0.1UF/10V
VCCA_MPLL
0.1 uF * 1
22 uF * 1
120 Ohm @
100MHz * 1
500-milli Ohm * 1
VCCA_PEG_BG
0.1 uF * 1
L1008
+VCCA_PEG_PLL
Max:100mA
C1019
10UF/6.3V
C1020
0.1UF/10V
C1021
0.1UF/10V
VCCA_PEG_PLL
0.1 uF * 1
10 uF * 2
1 Ohm * 1
FB 220@100M Hz * 1
VCCA_TVA_DAC/VCCA_TVB_DAC/VCCA_TVC_DAC
0.01 uF * 1
0.1 uF * 1
+3VS
Max: 10mA
L1003
10Ohm
r0603_h24
D1001
BAT54C
+VCCP
C1004
0.1UF/10V
VCCSYNC
0.1 uF * 1
U0601H
CRESTLINE_965GM
CRT
PLL
LVDS
PEG
SM
TV
DAC
TV/CRT
LVDS
POWER
VTT
AXD
AXF
SM CK
HV
PEG
DMI
VTTLF
Max: 850mA
On the Edge
In Cavity
C1006
10UF/6.3V
C1007
10UF/6.3V
CE1003
100UF/2.5V
C1011
0.1UF/10V
C1012
1UF/10V
C1013
10UF/6.3V
VTT
4.7 uF * 2
2.2 uF * 1
0.47 uF * 1
Max: 515mA
C1017
1UF/10V
C1018
10UF/6.3V
VCC_AXD
1 uF *1
VCCAXF
1 uF *1
Max: 495mA
C1022
1UF/10V
C1023
10UF/6.3V
VCC_DMI
0.1 uF * 1
Max: 100mA
C1024
0.1UF/10V
Max: 200mA
C1025
10UF/6.3V
C1026
0.1UF/10V
VCC_SM_CK
0.1 uF * 1
22 uF * 1
10 uF or 22 uF * 1
1.0 uH * 1
1 Ohm * 1
VCC_HV
0.1 uF * 1
Max: 1260mA
C1032
0.1UF/10V
Max: 260mA
L1013
120Ohm/100Mhz
Irat=600mA
C1046
1UF/10V
C1047
0.1UF/10V
C1037
0.47UF/16V
c0603
C1038
0.47UF/16V
c0603
C1039
0.47UF/16V
c0603
VTT_LF
0.47 uF * 3
VCC_RXR & VCC_PEG
10 uF * 1
220 uF * 5
91nH * 1
+1.25VS
L1009
Max:640mA
+VCCA_SM
CE1004
100UF/2.5V
80Ohm/100Mhz
Irat=2A
C1027
10UF/6.3V
C1028
1UF/10V
C1029
0.1UF/10V
VCCA_SM
4.7 uF * 1
1 uF * 1
22 uF * 1
VCCD_TVDAC/VCCD_CRT
0.01 uF * 1
0.1 uF * 1
Max: 60mA
C1030
10UF/6.3V
C1031
0.1UF/10V
L1010
Max:35mA
+VCCA_SM_CK
C1033
10UF/6.3V
C1034
0.1UF/10V
VCCA_SM_CK
0.1 uF * 1
22 uF * 1
VCCD_PEG_PLL
0.1 uF * 1
Max: 250mA
C1035
0.1UF/10V
C1036
0.1UF/10V
VCCD_LVDS
1.0 uF * 1
Max: 150mA
+1.8V
L1011
Max:10mA
+VCCA_LVDS
C1040
1UF/10V
C1041
0.1UF/10V
VCCA_LVDS
1.0 nF * 1
L1012
Max:100mA
+VCC_TX_LVDS
C1044
10UF/6.3V
C1045
0.1UF/10V
VCCTX_LVDS
1.0 nF * 1
220 uF * 1
1 uH at 78m Ohm * 1
R1001
10KOhm
+5V
U1001
MAX8863
SHDN#
GND
IN
OUT
SET
MAX8863TEUK
3VS_DAC_ADJ
R1002
35.7KOhm
R1003
20KOhm
C1048
0.1UF/50V
C1049
4.7UF/16V
C1050
0.1UF/50V
T1001
TPC26T
M0212
<Variant Name>
ASUSALPHA
Title : 965GM(PWR2)
ASUSALPHATeK COMPUTER INC.
Engineer: Julian Kuo
Size Custom
Project Name TERESA20
Rev 2.0
Date: Thursday, July 05, 2007
Sheet 10 of 66





07/04/03 To change name from Partial CLK Gating Disable into Reserved --- Iverson

GMCH Strapping

CFG5 : DMI Strap

0 = DMI x2

1 = DMI x4 (D)

7 MCH_CFG_5 — R1120 4.02KOHM @ — GND

CFG19 : DMI Lane Reversal

0 = Normal Operation (D)

1 = Lanes Reversed

7 MCH_CFG_19 — R1126 4.02KOHM @ — +3VS

CFG[13:12] : GMCH Test Mode

00= Reserved

01 = XOR Mode Enable

10 = All Z Mode Enable

11 = Normal Operation (D)

7 MCH_CFG_12 — R1108 4.02KOHM @

7 MCH_CFG_13 — R1110 4.02KOHM @ — GND

CFG8 : Low Power PCI-E

0 = Normal mode

1 = Low Power Mode (D)

7 MCH_CFG_8 — R1125 4.02KOHM @ — GND

CFG20 : Concurrent SDVO / PCIe

0 = Only one is operational (D)

1 = operate simultaneous

7 MCH_CFG_20 — R1116 4.02KOHM @ — +3VS

CFG9 : PCIE Graphic Lane

0 = Reverse Lane PCI-E (SDVO)

1 = Normal Operation (D)

7 MCH_CFG_9 — R1109 4.02KOHM @ — GND

CFG16 : FSB Dynamic ODT

0 = Dynamic ODT Disable

1 = Dynamic ODT Enable (D)

7 MCH_CFG_16 — R1121 4.02KOHM @ — GND

0 = IntelR Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality

1= Intel Management Engine Crypto TLS Cipher Suite with confidentiality (D)

7 MCH_CFG_7 — R1127 4.02KOHM @ — GND

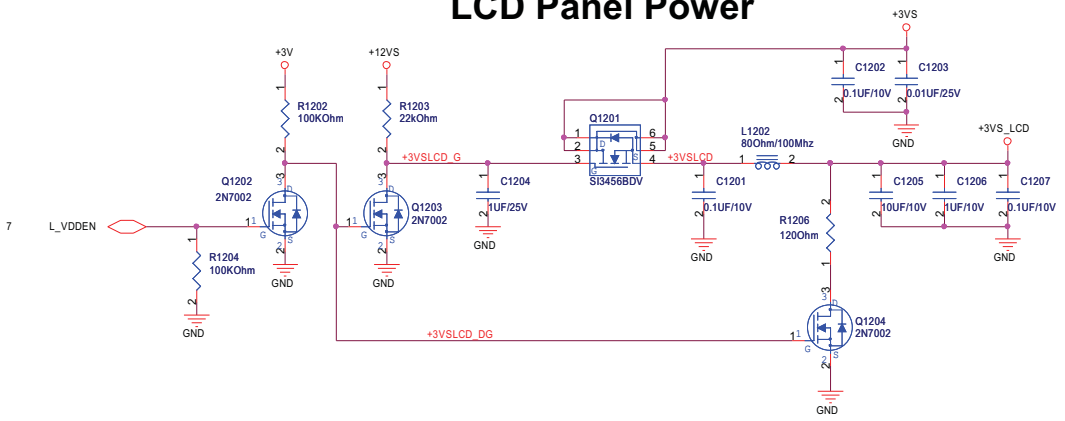
07/04/03 To add the R1127 to pull down on CFG_7 Signal.--- Iverson

<Variant Name>

ASUSALPHA	Title : 965GM(GND)		
ASUSALPHATeK COMPUTER INC.	Engineer: Julian Kuo		
Size: Custom	Project Name: TERESA20		Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 11 of 66		

LCD Panel Power

3~3.6V
Full Active: 410 mA(Max. 500 mA)
3~3.6V
S0-S1 M: 410 mA(Max. 500 mA)



LCD Backlight Control

BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn On/Off backlight

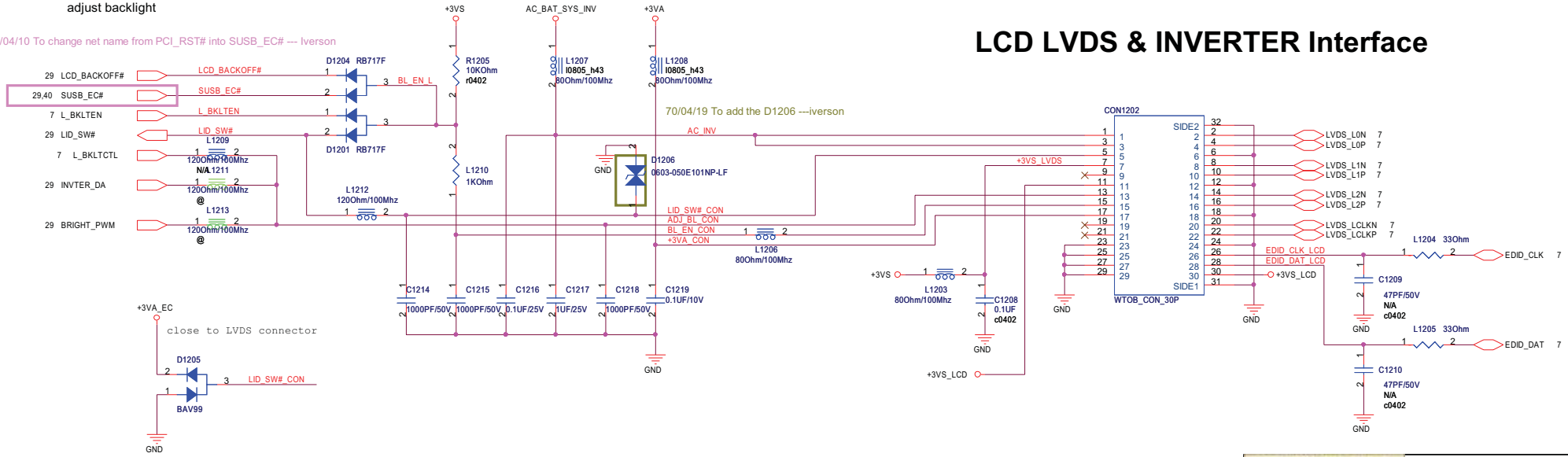
EC
INVTER_DA:
EC output D/A signal (adjust voltage level) to adjust backlight

Inverter Board built in 15.4W LCD Panel

LCD LVDS & INVERTER Interface

07/04/10 To change net name from PCI_RST# into SUSB_EC# --- Iverson

70/04/19 To add the D1206 ---iverson

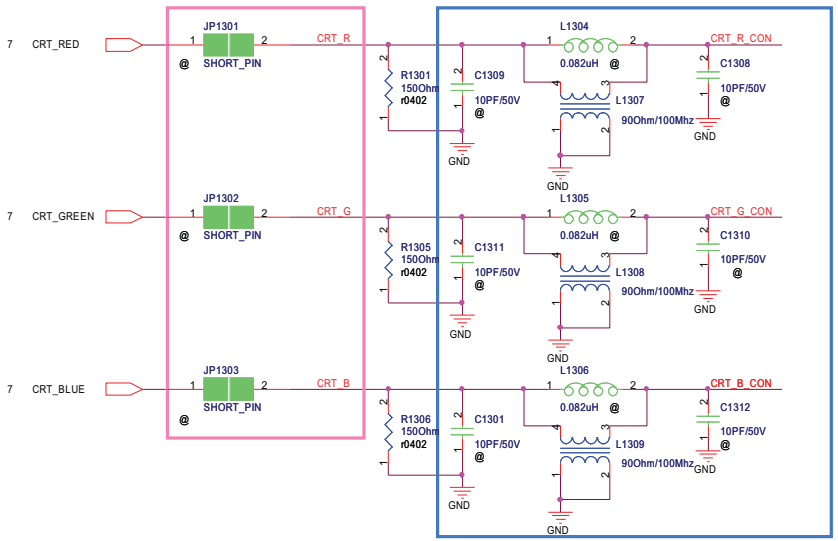


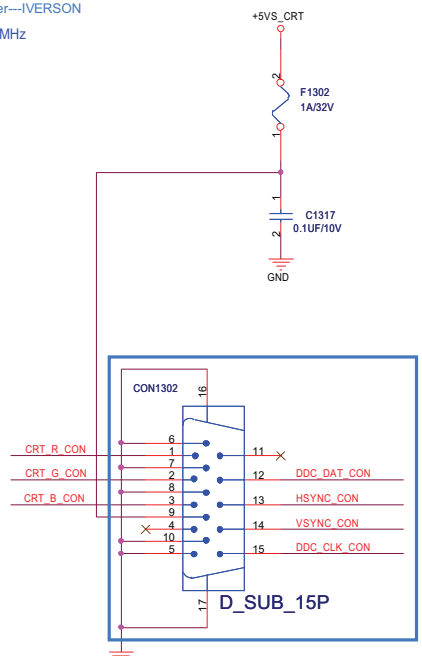
ASUSALPHA	Title : LVDS & INVERTER	
ASUSALPHAtek COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 12 of 66	

CRT OUT

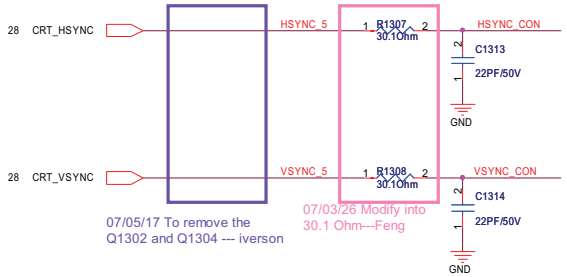
07/07/02 To add the L1307 L1308 L1309. Remove the Pi-type filter---IVERSON
checklist suggests 47ohm/100MHz

07/03/26 Modify Jump type---Feng





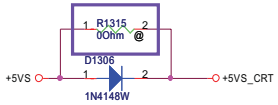
07/06/26 To change the CON1302 P/N from 12G10111015M into 12G10111215TTB --- iverson



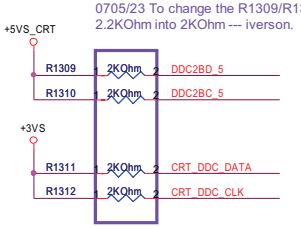
07/05/17 To remove the Q1302 and Q1304 --- iverson

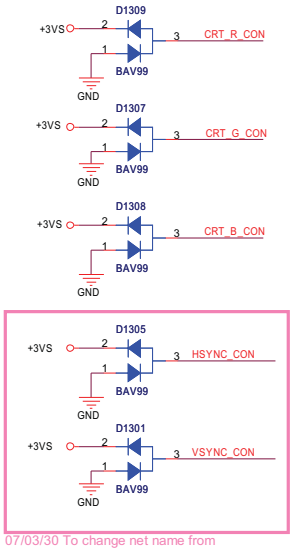
07/03/26 Modify into 30.1 Ohm---Feng

070507 To add the R1315 0Ohm --- iverson.

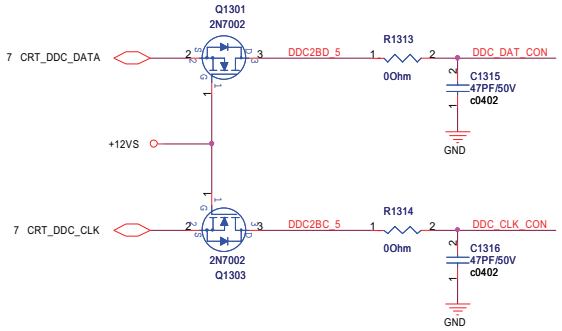


0705/23 To change the R1309/R1310/R1311/R1312 from 2.2KOhm into 2KOhm --- iverson.

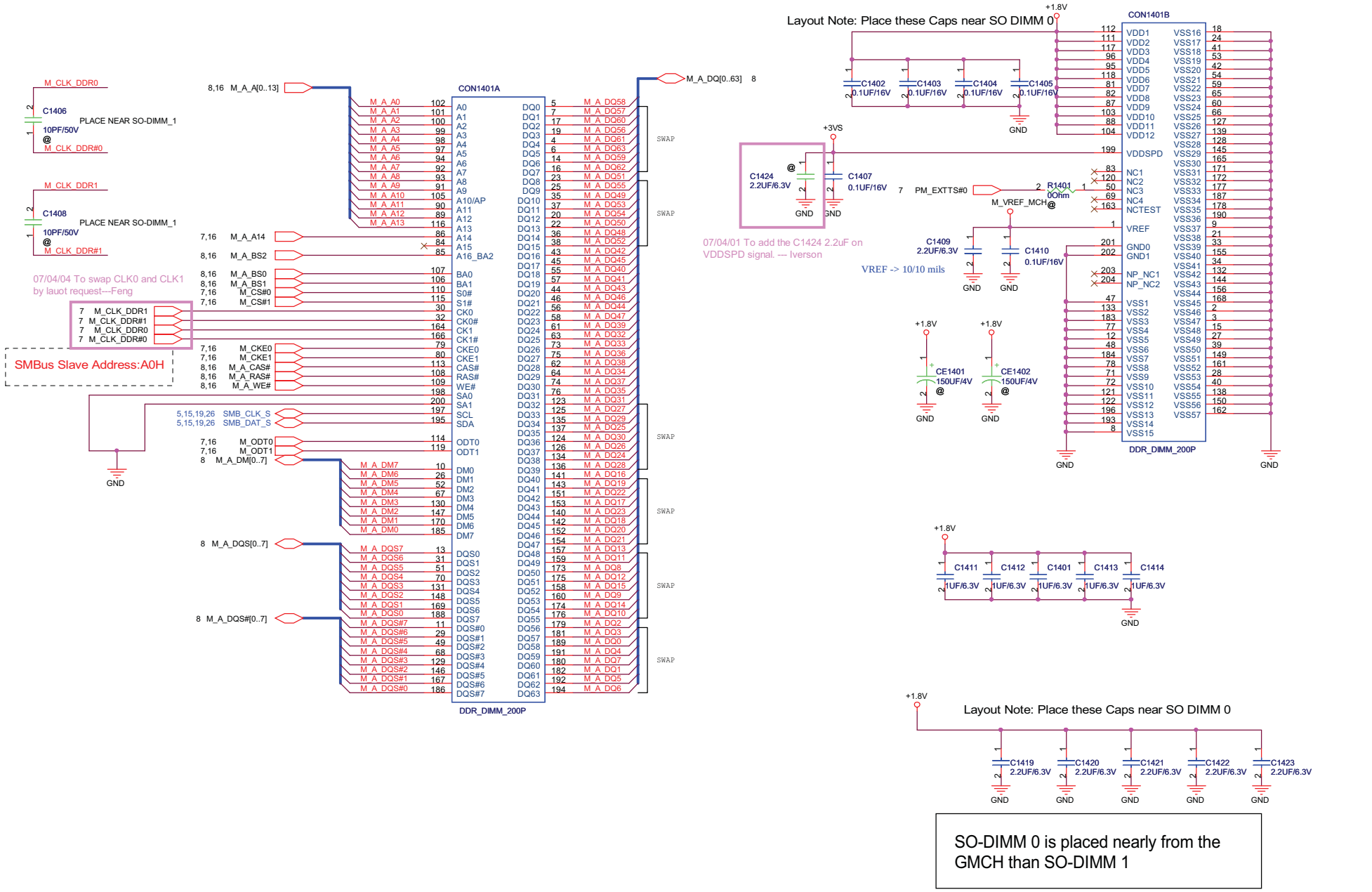




07/03/30 To change net name from VSYNC_5/HSYNC_5 into VSYNC_CON/HSYNC_CON---Feng



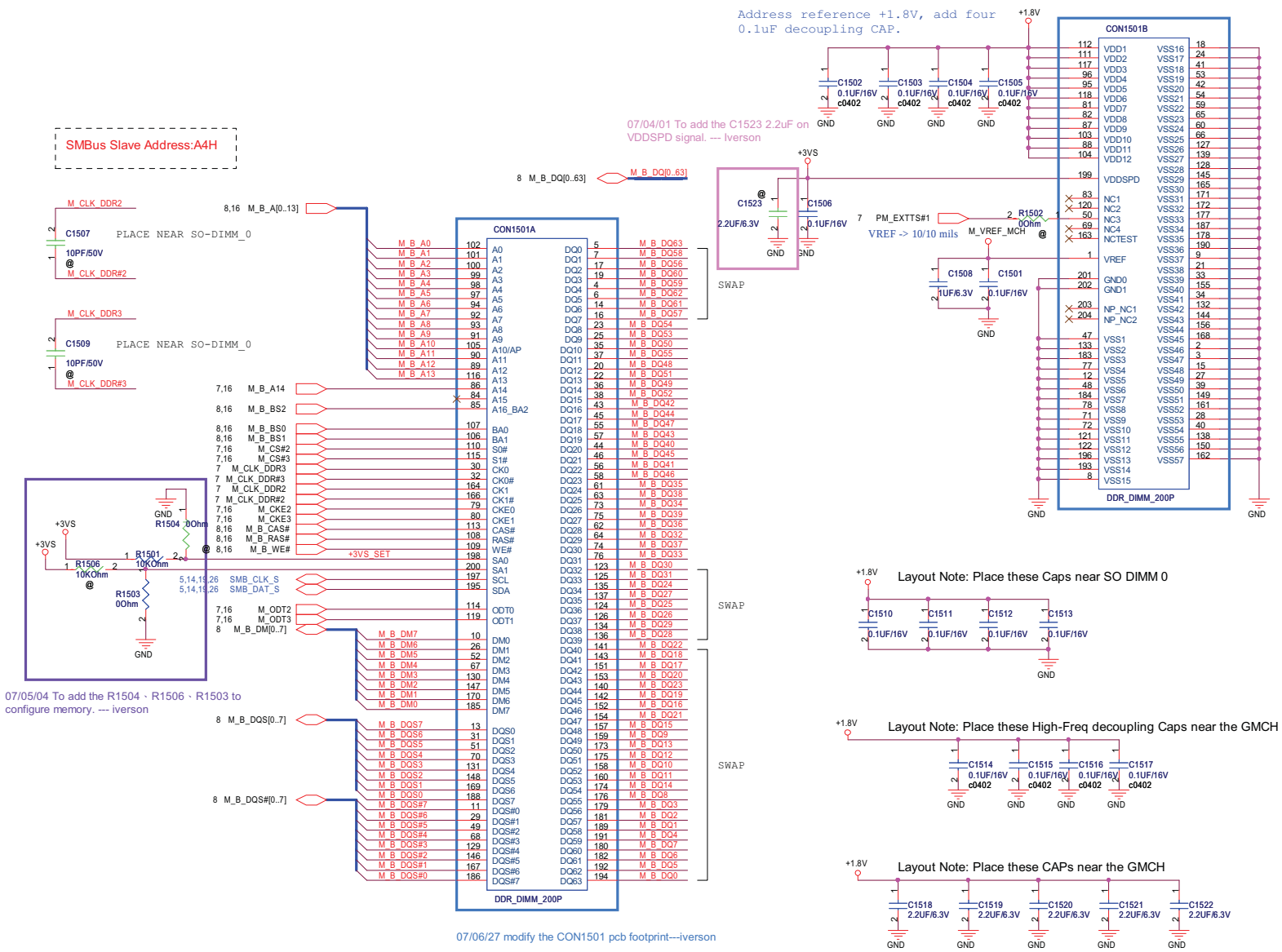
ASUSALPHA	Title : CRT		
ASUSALPHATeK COMPUTER INC.	Engineer: Feng Lin		
Size: Custom	Project Name: TERESA20		Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 13 of 66		



SO-DIMM 0 is placed nearly from the GMCH than SO-DIMM 1

<Variant Name>

ASUSALPHA	Title : DDR2 SO-DIMM0	
ASUSALPHATeK COMPUTER INC.	Engineer: Feng Lin	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 14 of 66	



<Variant Name>

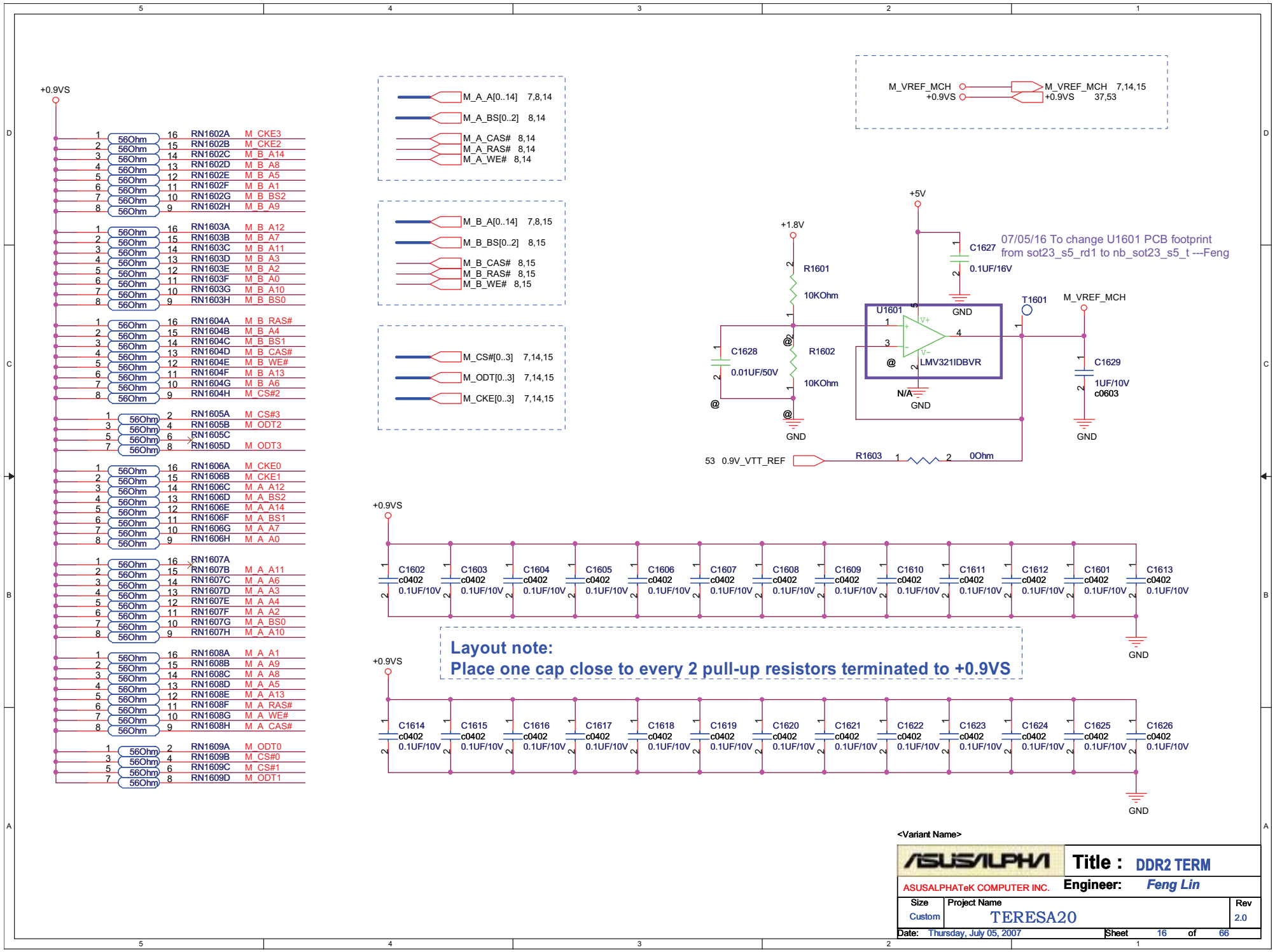
ASUSALPHATeK COMPUTER INC.

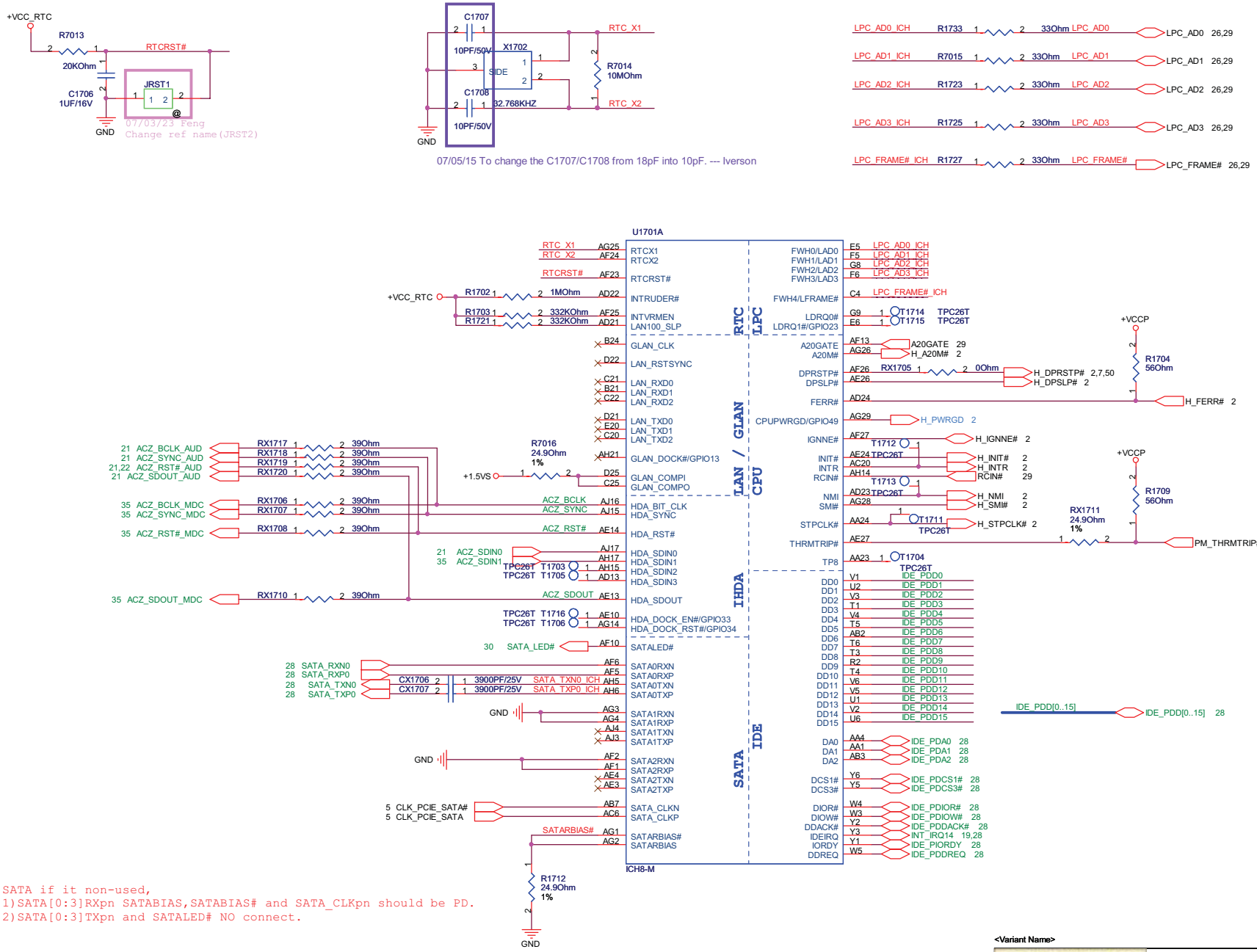
Title : DDR2 SO-DIMM1

Engineer: Feng Lin

Size	Project Name	Rev
Custom	TERESA20	2.0

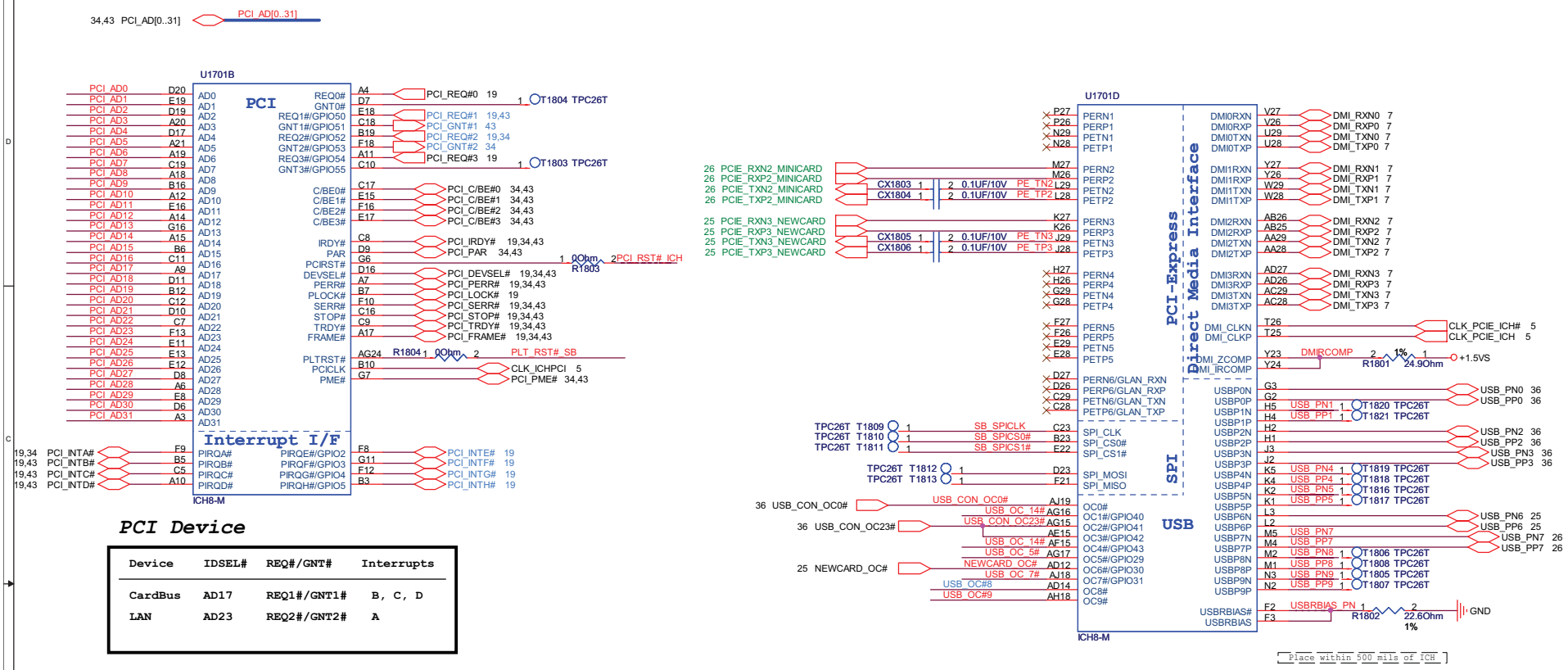
Date: Thursday, July 05, 2007 Sheet 15 of 66


+0.9VS
RN1602A M_CKE3
RN1602B M_CKE2
RN1602C M_B_A14
RN1602D M_B_A8
RN1602E M_B_A5
RN1602F M_B_A1
RN1602G M_B_BS2
RN1602H M_B_A9
RN1603A M_B_A12
RN1603B M_B_A7
RN1603C M_B_A11
RN1603D M_B_A3
RN1603E M_B_A2
RN1603F M_B_A0
RN1603G M_B_A10
RN1603H M_B_BS0
RN1604A M_B_RAS#
RN1604B M_B_A4
RN1604C M_B_BS1
RN1604D M_B_CAS#
RN1604E M_B_WE#
RN1604F M_B_A13
RN1604G M_B_A6
RN1604H M_CS#2
RN1605A M_CS#3
RN1605B M_ODT2
RN1605C
RN1605D M_ODT3
RN1606A M_CKE0
RN1606B M_CKE1
RN1606C M_A_A12
RN1606D M_A_BS2
RN1606E M_A_A14
RN1606F M_A_BS1
RN1606G M_A_A7
RN1606H M_A_A0
RN1607A
RN1607B M_A_A11
RN1607C M_A_A6
RN1607D M_A_A3
RN1607E M_A_A4
RN1607F M_A_A2
RN1607G M_A_BS0
RN1607H M_A_A10
RN1608A M_A_A1
RN1608B M_A_A9
RN1608C M_A_A8
RN1608D M_A_A5
RN1608E M_A_A13
RN1608F M_A_RAS#
RN1608G M_A_WE#
RN1608H M_A_CAS#
RN1609A M_ODT0
RN1609B M_CS#0
RN1609C M_CS#1
RN1609D M_ODT1
56Ohm
M_A_A[0..14] 7,8,14
M_A_BS[0..2] 8,14
M_A_CAS# 8,14
M_A_RAS# 8,14
M_A_WE# 8,14
M_B_A[0..14] 7,8,15
M_B_BS[0..2] 8,15
M_B_CAS# 8,15
M_B_RAS# 8,15
M_B_WE# 8,15
M_CS#[0..3] 7,14,15
M_ODT[0..3] 7,14,15
M_CKE[0..3] 7,14,15
M_VREF_MCH
+0.9VS
M_VREF_MCH 7,14,15
+0.9VS 37,53
+5V
+1.8V
R1601
10KOhm
R1602
10KOhm
C1628
0.01UF/50V
C1627
0.1UF/16V
07/05/16 To change U1601 PCB footprint
from sot23_s5_rd1 to nb_sot23_s5_t ---Feng
U1601
LMV321IDBVR
GND
N/A
T1601
M_VREF_MCH
C1629
1UF/10V
c0603
53 0.9V_VTT_REF
R1603
0Ohm
C1602 c0402 0.1UF/10V
C1603 c0402 0.1UF/10V
C1604 c0402 0.1UF/10V
C1605 c0402 0.1UF/10V
C1606 c0402 0.1UF/10V
C1607 c0402 0.1UF/10V
C1608 c0402 0.1UF/10V
C1609 c0402 0.1UF/10V
C1610 c0402 0.1UF/10V
C1611 c0402 0.1UF/10V
C1612 c0402 0.1UF/10V
C1601 c0402 0.1UF/10V
C1613 c0402 0.1UF/10V
Layout note:
Place one cap close to every 2 pull-up resistors terminated to +0.9VS
C1614 c0402 0.1UF/10V
C1615 c0402 0.1UF/10V
C1616 c0402 0.1UF/10V
C1617 c0402 0.1UF/10V
C1618 c0402 0.1UF/10V
C1619 c0402 0.1UF/10V
C1620 c0402 0.1UF/10V
C1621 c0402 0.1UF/10V
C1622 c0402 0.1UF/10V
C1623 c0402 0.1UF/10V
C1624 c0402 0.1UF/10V
C1625 c0402 0.1UF/10V
C1626 c0402 0.1UF/10V
<Variant Name>
ASUSALPHA
Title : DDR2 TERM
ASUSALPHATeK COMPUTER INC.
Engineer: Feng Lin
Size Custom
Project Name TERESA20
Rev 2.0
Date: Thursday, July 05, 2007
Sheet 16 of 66



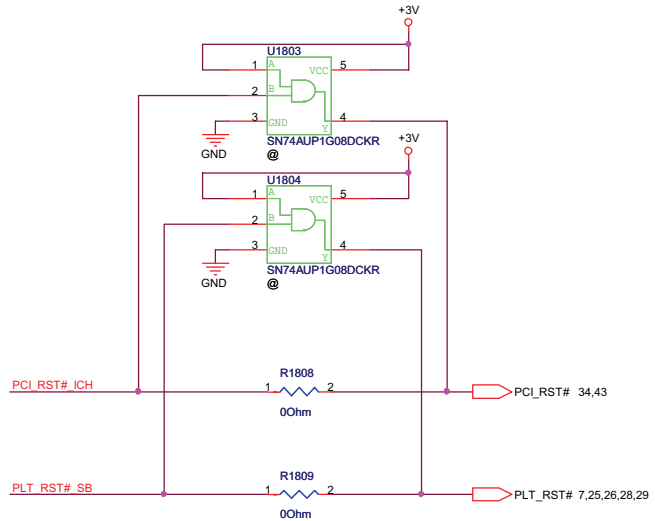
<Variant Name>

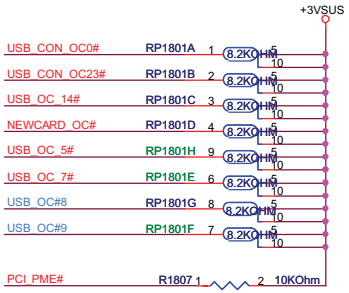
ASUSALPHA	Title :	ICH8-M(1)
ASUSALPHATeK COMPUTER INC.	Engineer:	Julian Kuo
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 17 of 66	



PCI Device

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD17	REQ1#/GNT1#	B, C, D
LAN	AD23	REQ2#/GNT2#	A





ICH8 Boot BIOS select

		GNT#0	CS#1
LPC	11	1	1
PCI	10	1	0
SPI	01	0	1

(default)

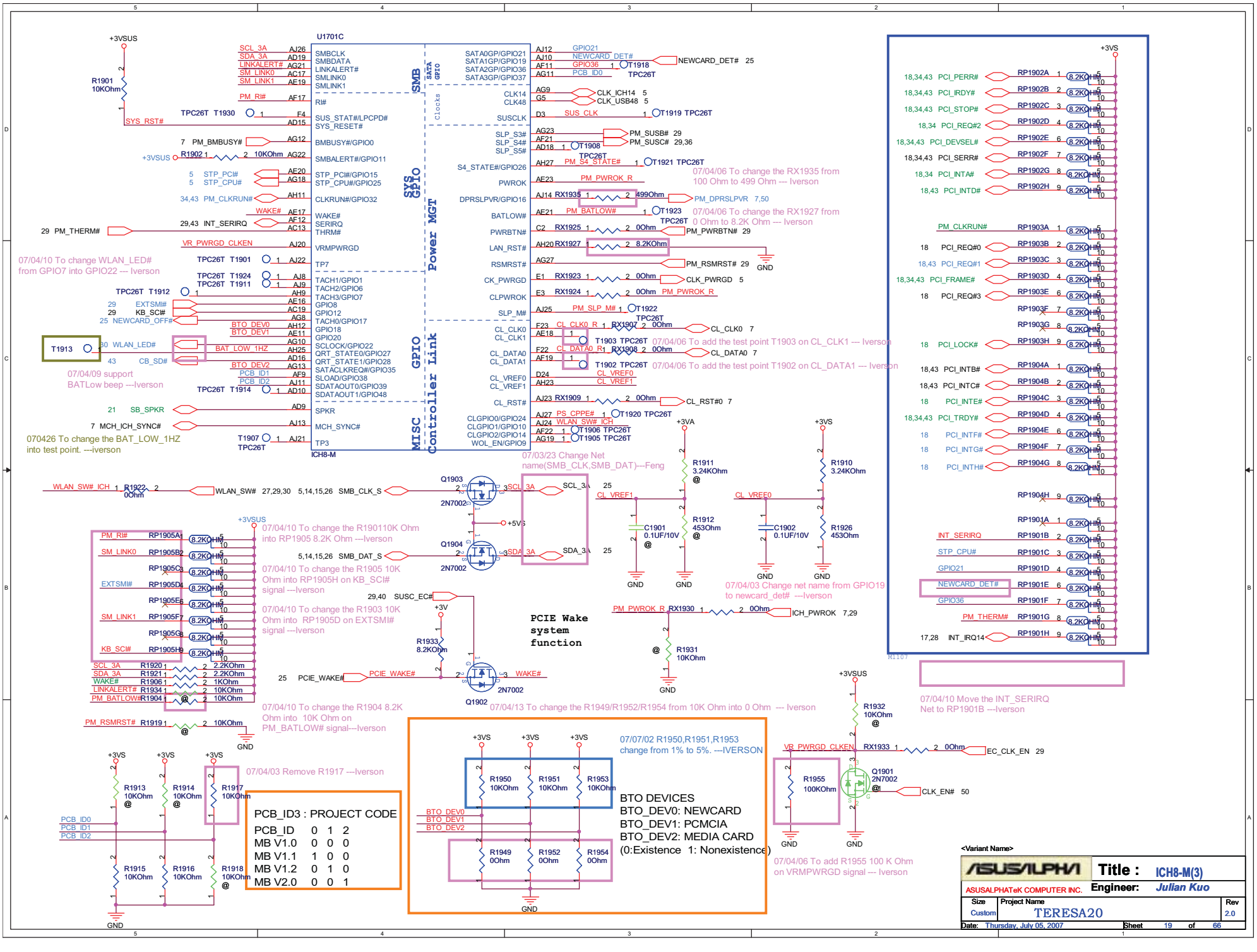
USB Devices

Port 0	CON3602
Port 1	Unused
Port 2	CON3601
Port 3	CON3601
Port 4	Unused
Port 5	Unused
Port 6	NewCard
Port 7	MINICard
Port 8	Unused
Port 9	Unused

07/04/03 To change name from UNUSED into MINI Card --- Iverson

<Variant Name>

ASUSALPHA	Title :	ICH8-M(2)
ASUSALPHATeK COMPUTER INC.	Engineer:	Julian Kuo
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 18 of 66	


U1701C
ICH8-M
SMB
SYS GPIO
Power MGT
GPIO Controller Link
MISC
07/04/10 To change WLAN_LED# from GPIO7 into GPIO22 --- Iverson
07/04/09 support BATLow beep ---Iverson
070426 To change the BAT_LOW_1HZ into test point. ---iverson
07/04/06 To change the RX1935 from 100 Ohm to 499 Ohm --- Iverson
07/04/06 To change the RX1927 from 0 Ohm to 8.2K Ohm --- Iverson
07/04/06 To add the test point T1903 on CL_CLK1 --- Iverson
07/04/06 To add the test point T1902 on CL_DATA1 --- Iverson
07/03/23 Change Net name(SMB_CLK,SMB_DAT)---Feng
07/04/10 To change the R190110K Ohm into RP1905 8.2K Ohm ---Iverson
07/04/10 To change the R1905 10K Ohm into RP1905H on KB_SCI# signal ---Iverson
07/04/10 To change the R1903 10K Ohm into RP1905D on EXTSMI# signal ---Iverson
07/04/10 To change the R1904 8.2K Ohm into 10K Ohm on PM_BATLOW# signal---Iverson
07/04/03 Change net name from GPIO19 to newcard_det# ---Iverson
PCIE Wake system function
07/04/13 To change the R1949/R1952/R1954 from 10K Ohm into 0 Ohm --- Iverson
07/04/10 Move the INT_SERIRQ Net to RP1901B ---Iverson
07/04/03 Remove R1917 ---Iverson
07/07/02 R1950,R1951,R1953 change from 1% to 5%. ---IVERSON
BTO DEVICES
BTO_DEV0: NEWCARD
BTO_DEV1: PCMCIA
BTO_DEV2: MEDIA CARD
(0:Existence 1: Nonexistence)
07/04/06 To add R1955 100 K Ohm on VRMPWRGD signal --- Iverson
PCB_ID3 : PROJECT CODE
PCB_ID 0 1 2
MB V1.0 0 0 0
MB V1.1 1 0 0
MB V1.2 0 1 0
MB V2.0 0 0 1
<Variant Name>
Title : ICH8-M(3)
ASUSALPHATeK COMPUTER INC.
Engineer: Julian Kuo
Size Custom
Project Name TERESA20
Rev 2.0
Date: Thursday, July 05, 2007
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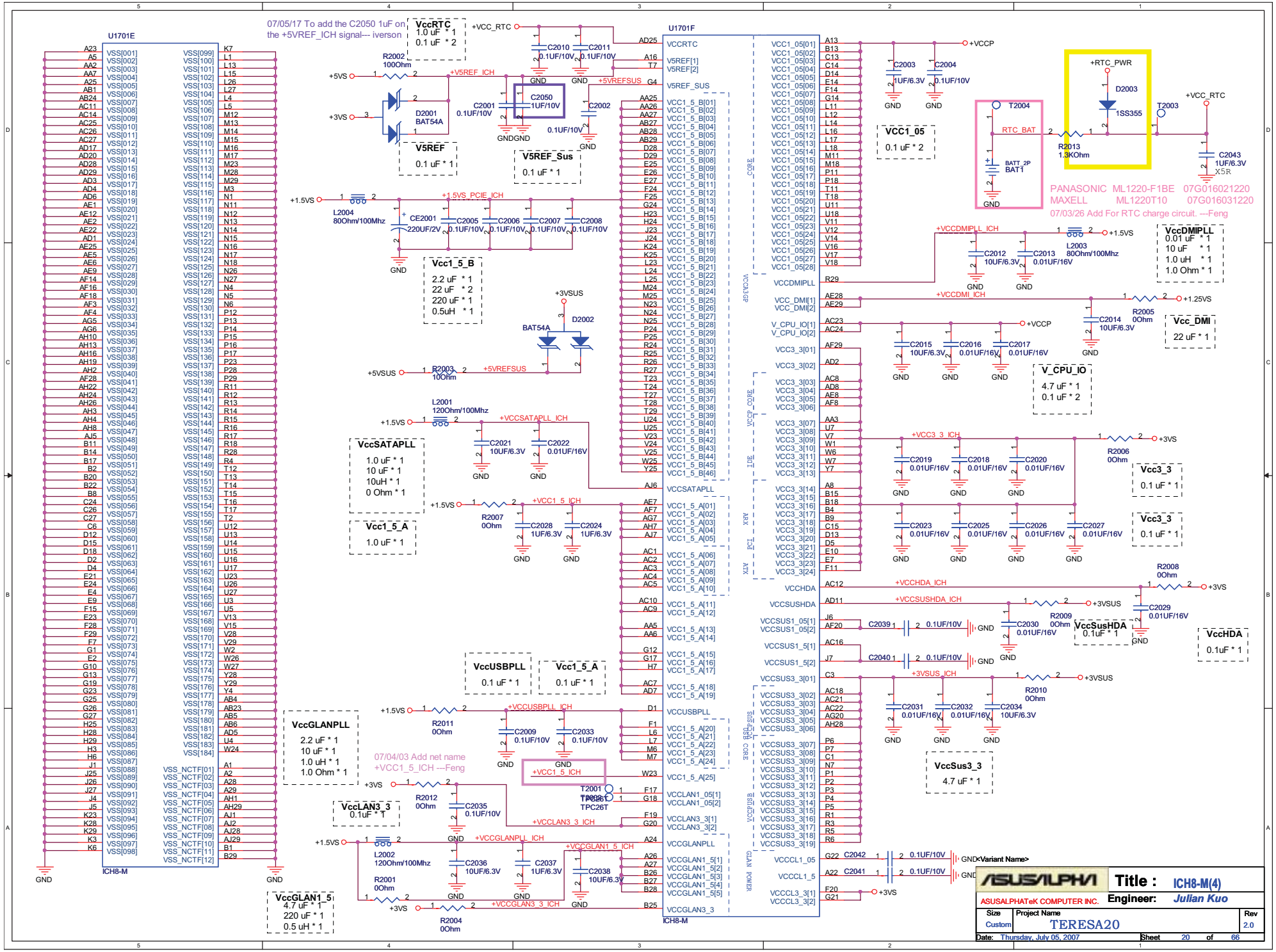
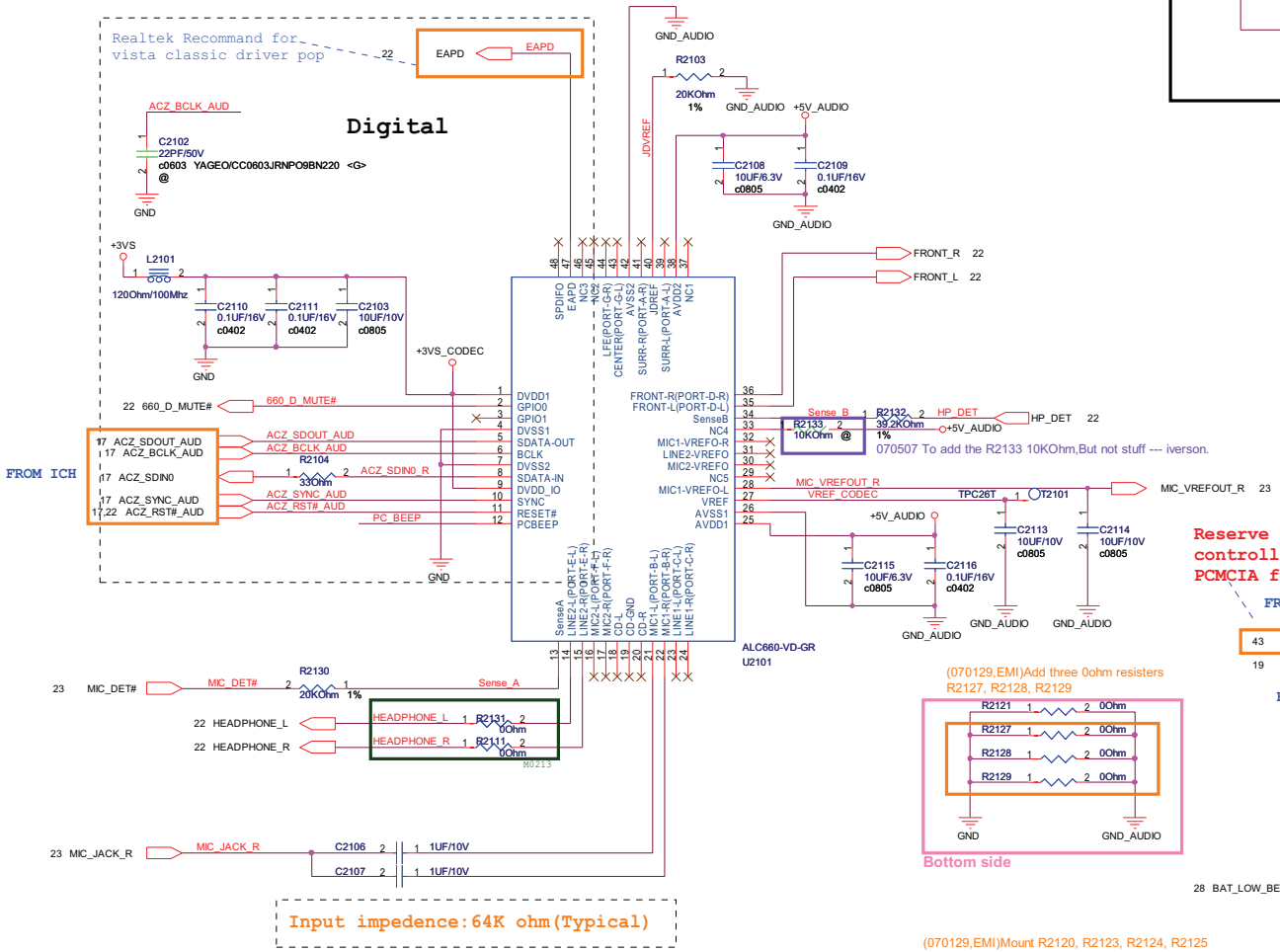
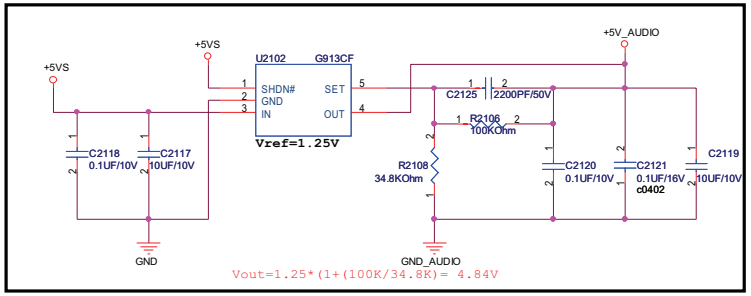

07/05/17 To add the C2050 1uF on the +5VREF_ICH signal--- iverson
U1701E
ICH8-M
U1701F
ICH8-M
VccRTC
1.0 uF * 1
0.1 uF * 2
+VCC_RTC
R2002
100Ohm
+5VS
+3VS
D2001
BAT54A
V5REF
0.1 uF * 1
+5VREF_ICH
C2001
0.1UF/10V
C2050
1UF/10V
C2002
0.1UF/10V
V5REF_Sus
0.1 uF * 1
+5VREFSUS
C2010
0.1UF/10V
C2011
0.1UF/10V
+1.5VS
L2004
80Ohm/100Mhz
+1.5VS_PCIE_ICH
CE2001
220UF/2V
C2005
0.1UF/10V
C2006
0.1UF/10V
C2007
0.1UF/10V
C2008
0.1UF/10V
Vcc1_5_B
2.2 uF * 1
22 uF * 2
220 uF * 1
0.5uH * 1
+3VSUS
D2002
BAT54A
+5VSUS
R2003
10Ohm
+5VREFSUS
L2001
120Ohm/100Mhz
+VCCSATAPLL_ICH
C2021
10UF/6.3V
C2022
0.01UF/16V
VccSATAPLL
1.0 uF * 1
10 uF * 1
10uH * 1
0 Ohm * 1
+VCC1_5_ICH
R2007
0Ohm
C2028
1UF/6.3V
C2024
1UF/6.3V
Vcc1_5_A
1.0 uF * 1
VccUSBPLL
0.1 uF * 1
Vcc1_5_A
0.1 uF * 1
+VCCUSBPLL_ICH
R2011
0Ohm
C2009
0.1UF/10V
C2033
0.1UF/10V
VccGLANPLL
2.2 uF * 1
10 uF * 1
1.0 uH * 1
1.0 Ohm * 1
07/04/03 Add net name
+VCC1_5_ICH ---Feng
+VCC1_5_ICH
T2001
TPC26T
+3VS
R2012
0Ohm
C2035
0.1UF/10V
VccLAN3_3
0.1uF * 1
+VCCLAN3_3_ICH
+VCCGLANPLL_ICH
L2002
120Ohm/100Mhz
C2036
10UF/6.3V
C2037
1UF/6.3V
+VCCGLAN1_5_ICH
C2038
10UF/6.3V
R2001
0Ohm
+VCCGLAN3_3_ICH
R2004
0Ohm
VccGLAN1_5
4.7 uF * 1
220 uF * 1
0.5 uH * 1
+VCCP
C2003
1UF/6.3V
C2004
0.1UF/10V
VCC1_05
0.1 uF * 2
T2004
BAT1
RTC_BAT
R2013
1.3KOhm
+RTC_PWR
D2003
1SS355
T2003
+VCC_RTC
C2043
1UF/6.3V
X5R
PANASONIC ML1220-F1BE 07G016021220
MAXELL ML1220T10 07G016031220
07/03/26 Add For RTC charge circuit. ---Feng
+VCCDMIPLL_ICH
C2012
10UF/6.3V
C2013
0.01UF/16V
L2003
80Ohm/100Mhz
+1.5VS
VccDMIPLL
0.01 uF * 1
10 uF * 1
1.0 uH * 1
1.0 Ohm * 1
+VCCDMI_ICH
R2005
0Ohm
+1.25VS
Vcc_DMI
22 uF * 1
C2014
10UF/6.3V
C2015
10UF/6.3V
C2016
0.01UF/16V
C2017
0.01UF/16V
V_CPU_IO
4.7 uF * 1
0.1 uF * 2
+VCC3_3_ICH
R2006
0Ohm
+3VS
C2019
0.01UF/16V
C2018
0.01UF/16V
C2020
0.01UF/16V
Vcc3_3
0.1 uF * 1
C2023
0.01UF/16V
C2025
0.01UF/16V
C2026
0.01UF/16V
C2027
0.01UF/16V
Vcc3_3
0.1 uF * 1
R2008
0Ohm
+VCCHDA_ICH
+3VS
C2029
0.01UF/16V
+VCCSUSHDA_ICH
+3VSUS
R2009
0Ohm
C2030
0.01UF/16V
VccSusHDA
0.1uF * 1
VccHDA
0.1uF * 1
C2039
0.1UF/10V
C2040
0.1UF/10V
+3VSUS_ICH
R2010
0Ohm
+3VSUS
C2031
0.01UF/16V
C2032
0.01UF/16V
C2034
10UF/6.3V
VccSus3_3
4.7 uF * 1
C2042
0.1UF/10V
C2041
0.1UF/10V
+3VS
GND
ASUSALPHA
Title : ICH8-M(4)
ASUSALPHATeK COMPUTER INC.
Engineer: Julian Kuo
Size Custom
Project Name TERESA20
Rev 2.0
Date: Thursday, July 05, 2007
Sheet 20 of 66

CODEC ALC660 REV:D

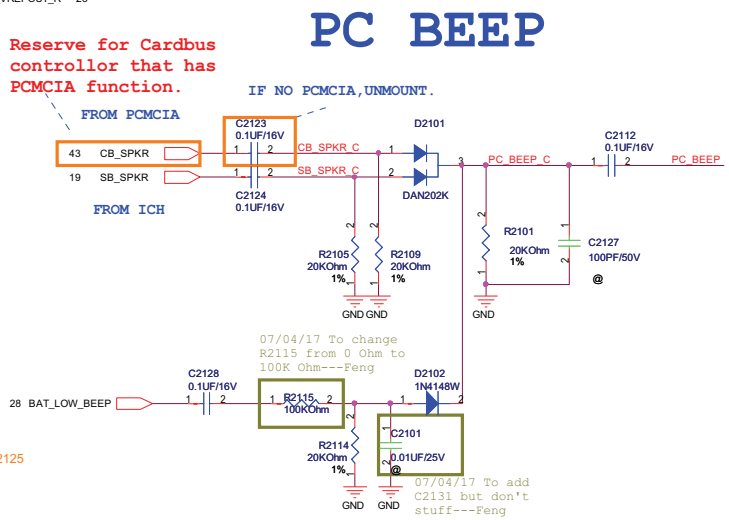


AUDIO POWER



M0207

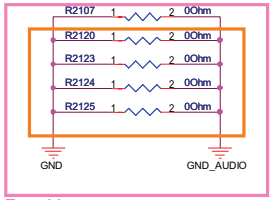
PC BEEP



(070129,EMI)Add three 0ohm resisters R2127, R2128, R2129

Bottom side

(070129,EMI)Mount R2120, R2123, R2124, R2125

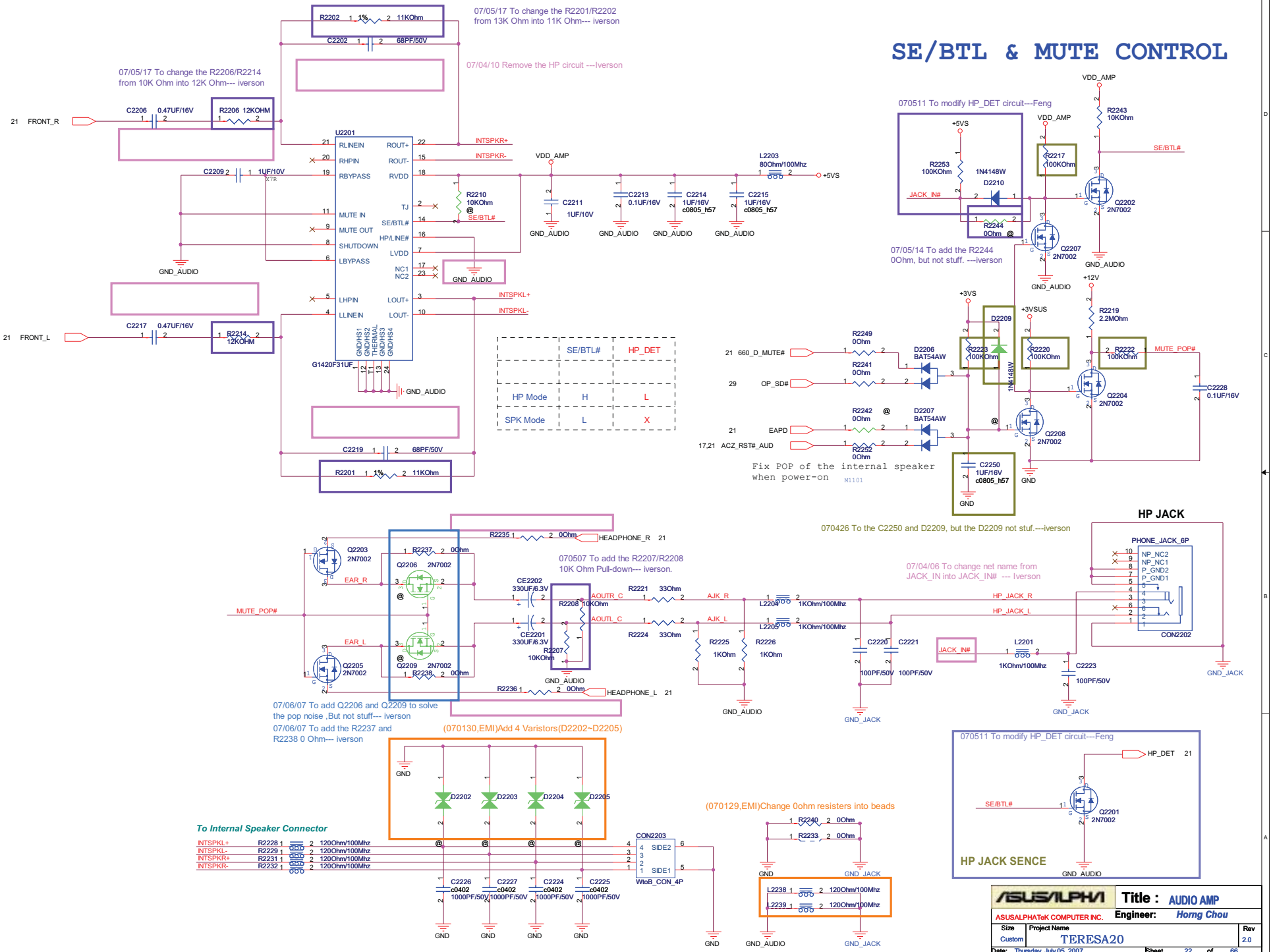


Top side

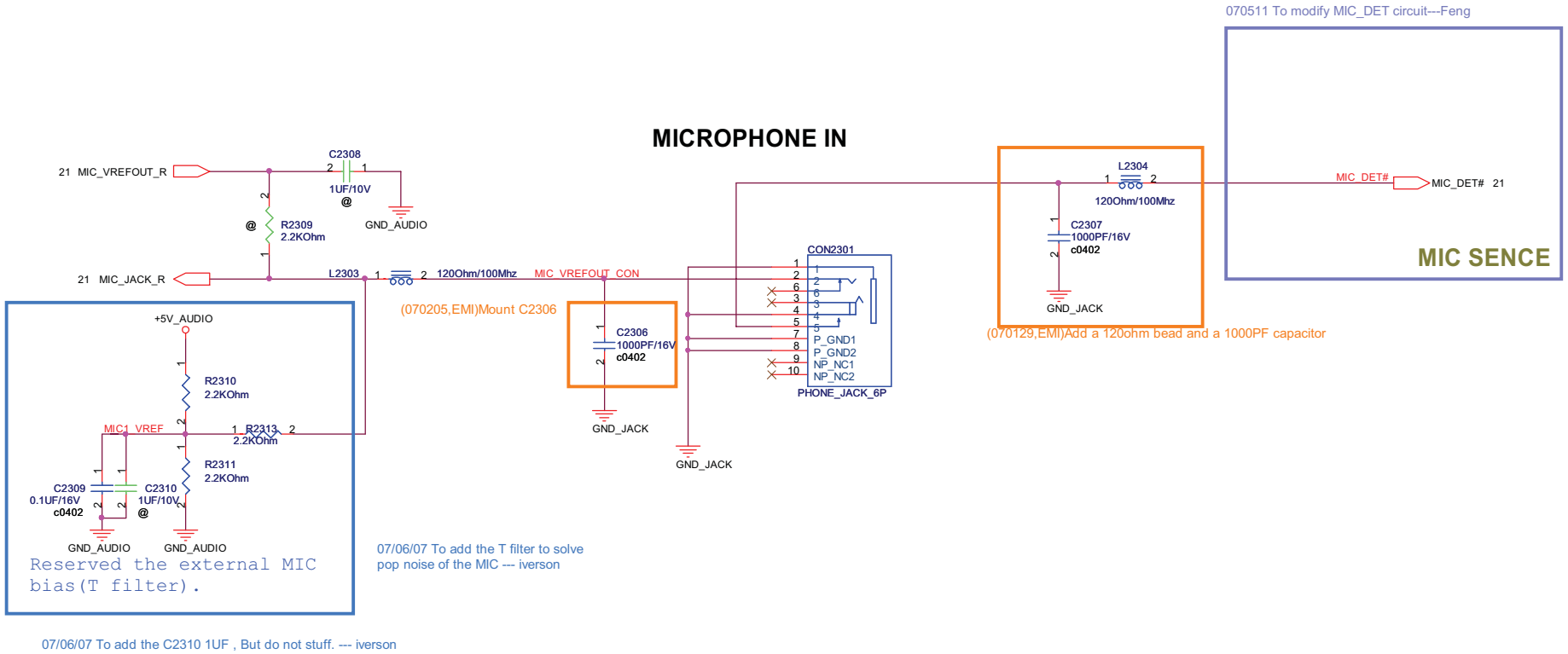
<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : CODEC ALC660(D)		
Size: Custom	Project Name: TERESA20		Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 21 of 66	Engineer: Feng	

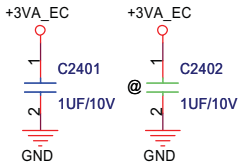
SE/BTL & MUTE CONTROL



MICROPHONE IN



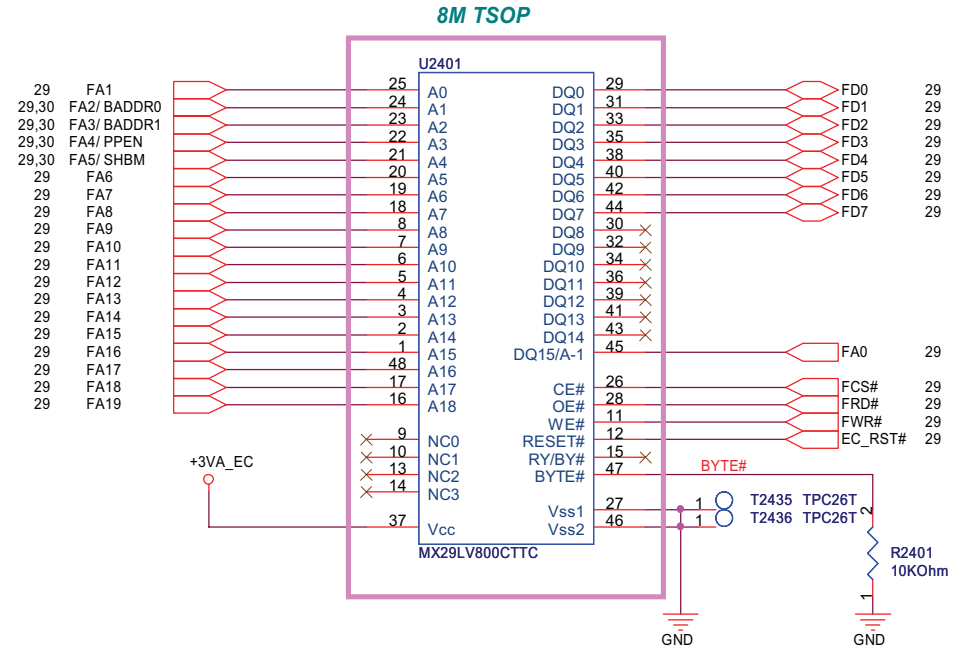
ASUSALPHA	Title : MIC JACK	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 23 of 66	



Note:

If you use 8M bits ROM, you need to connect FA19 to EC side.

For 8M bits ISA ROM



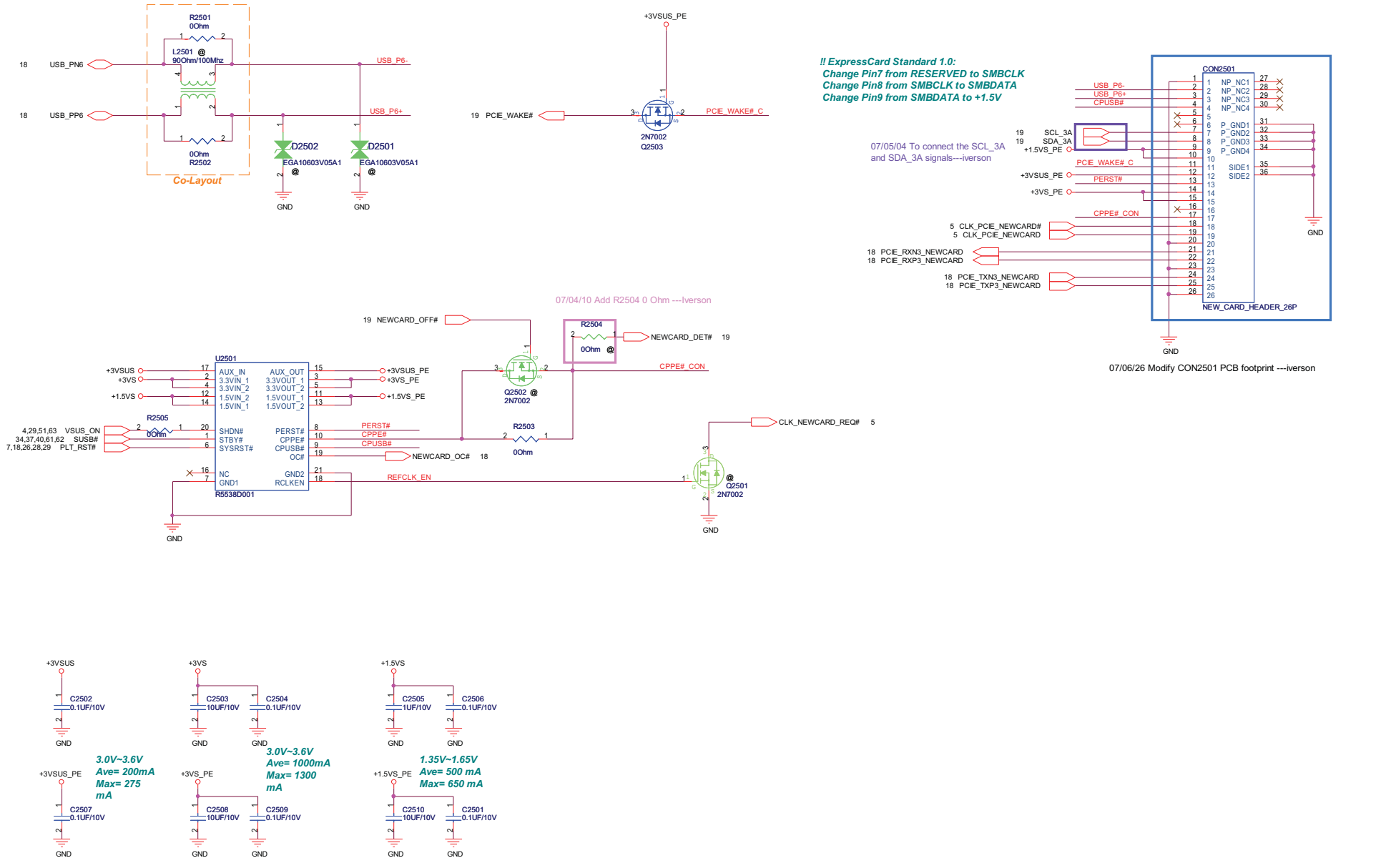
FD0	1	T2401	TPC26T
FD1	1	T2402	TPC26T
FD2	1	T2403	TPC26T
FD3	1	T2404	TPC26T
FD4	1	T2405	TPC26T
FD5	1	T2406	TPC26T
FD6	1	T2407	TPC26T
FD7	1	T2408	TPC26T
FA0	1	T2409	TPC26T
FA1	1	T2410	TPC26T
FA2/ BADDR0	1	T2411	TPC26T
FA3/ BADDR1	1	T2412	TPC26T
FA4/ PPEN	1	T2413	TPC26T
FA5/ SHBM	1	T2414	TPC26T
FA6	1	T2415	TPC26T
FA7	1	T2416	TPC26T
FA8	1	T2417	TPC26T
FA9	1	T2418	TPC26T
FA10	1	T2419	TPC26T
FA11	1	T2420	TPC26T
FA12	1	T2421	TPC26T
FA13	1	T2422	TPC26T
FA14	1	T2423	TPC26T
FA15	1	T2424	TPC26T
FA16	1	T2425	TPC26T
FA17	1	T2426	TPC26T
FA18	1	T2427	TPC26T
FA19	1	T2428	TPC26T
FCS#	1	T2429	TPC26T
FRD#	1	T2430	TPC26T
FWR#	1	T2431	TPC26T
EC_RST#	1	T2432	TPC26T
BYTE#	1	T2433	TPC26T
+3VA_EC	1	T2434	TPC26T

070507 To add test point on the ISA ROM --- iverson.

07/04/13 To change the U2401 from pn:05G001014110 into 05G001204043 --- Iverson

ASUSALPHA	Title : ISA ROM	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 24 of 66	

NewCard Header

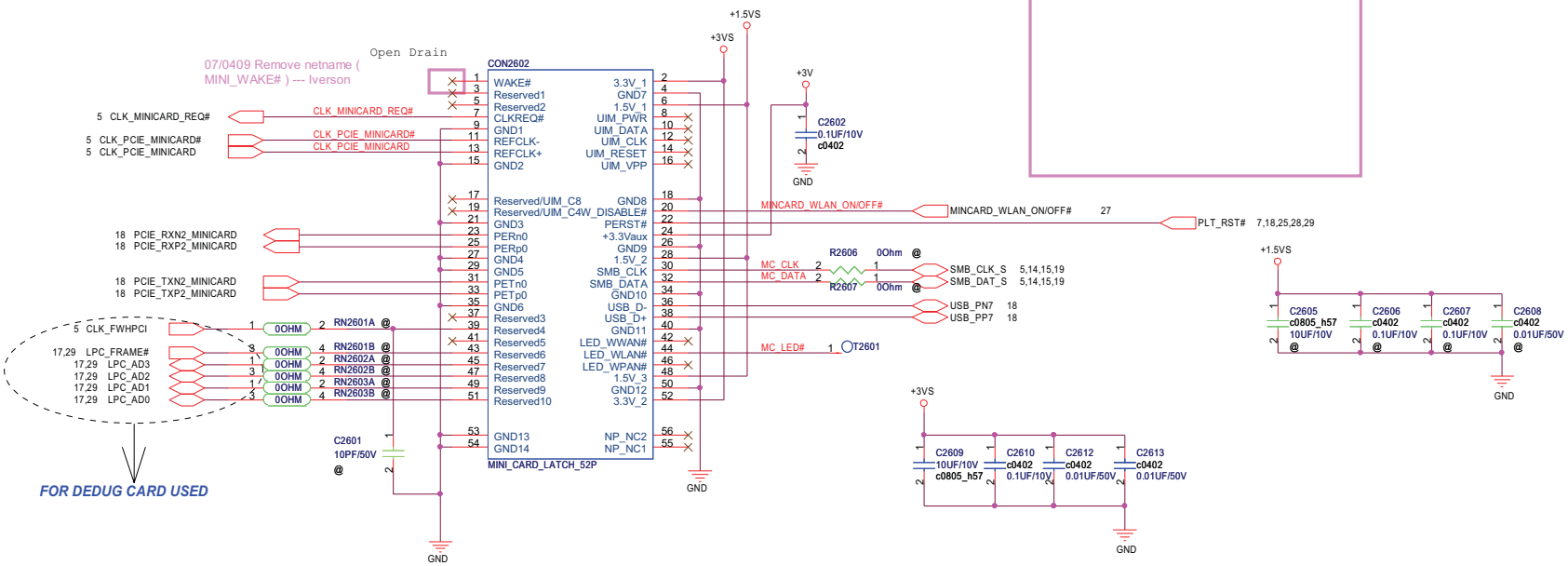


<Variant Name>

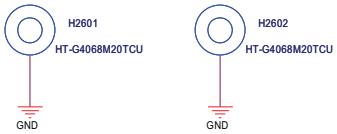
ASUSALPHA	Title : NEWCARD	
ASUSALPHATeK COMPUTER INC.	Engineer: Feng Lin	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 25 of 66	

MINI CARD CONNECTOR

07/04/09 Remove the PCIE Wake system function ---Iverson



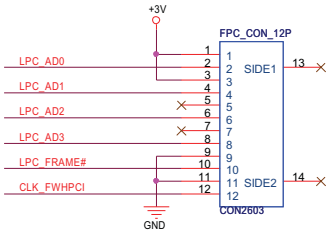
Instead of Mini-PCIE latch connecter.For cost down.



Power consumption of WLAN SPEC:

Vendor		ASKEY	ASKEY	ASKEY	Realtek
Chip Name		XB61	XB62	XB63	RTL8187
		WLL3140	WLL4080	WLL3141	WN6301L
Transmit Mode	11.a		550mA		
	11.b	525mA	560mA	2330mW	445mA
	11.g	560mA	550mA	2155mW	450mA
	11.n				
Receive Mode	11.a		280mA		
	11.b	430mA	270mA	1089mW	310mA
	11.g	460mA	280mA	1122mW	330mA
	11.n				
Sleep Mode Current		220mA	20mA		325mA
Supplied Voltage(VCC)	MIN	3.0V	3.0V	3.0V	3.3V-5%
	TYP	3.3V	3.3V	3.3V	3.3V
	MAX	3.6V	3.6V	3.6V	3.3V+5%

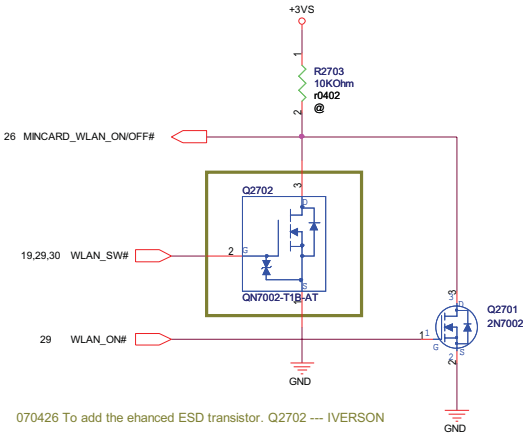
Debug Card CON



ASUSALPHA	Title : MINI PCIEX/DEBUG CON		
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou		
Size: Custom	Project Name: TERESA20		Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 26 of 66		

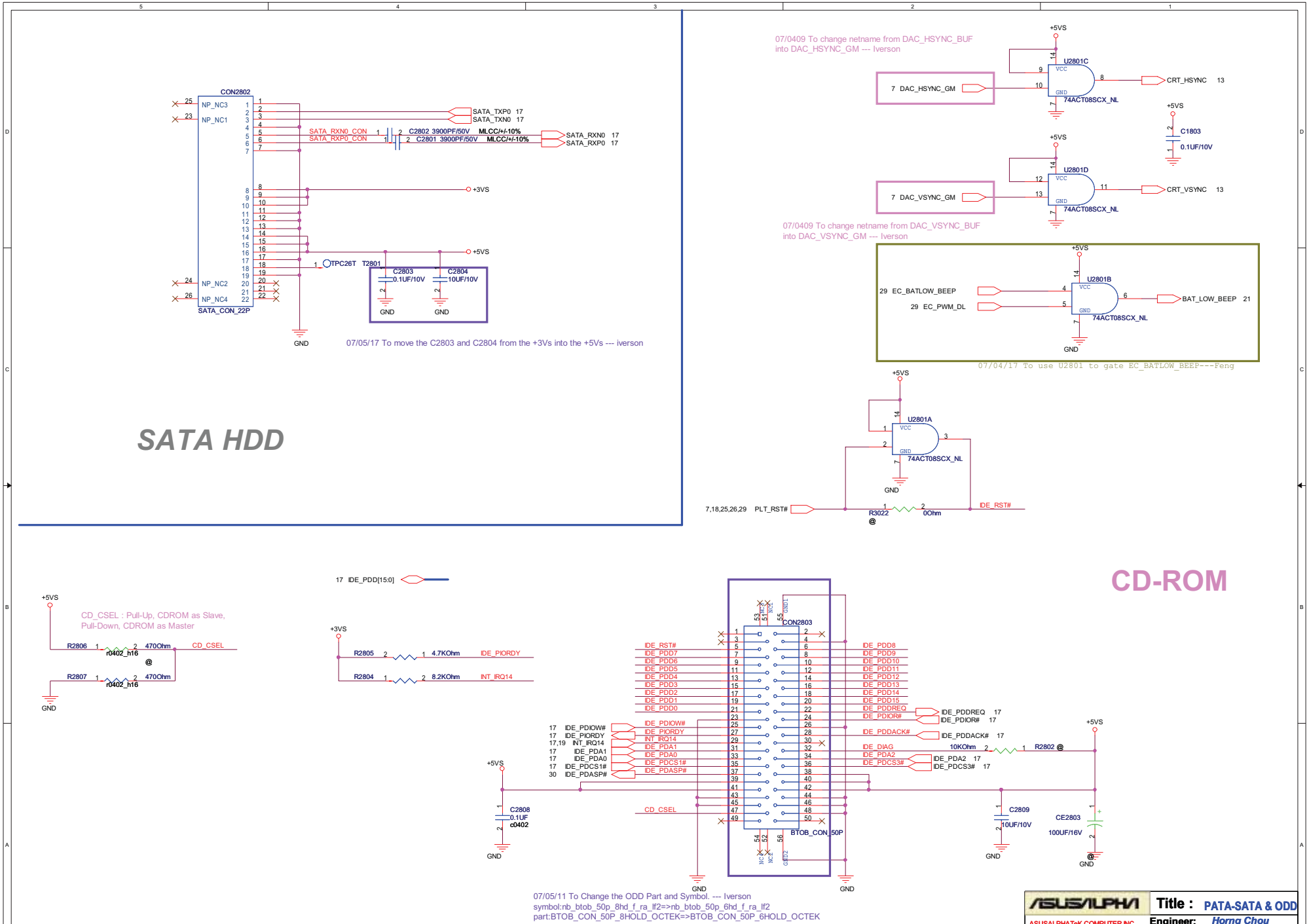
For Side SW

WLAN ON/OFF Control



070426 To add the ehanced ESD transistor. Q2702 --- IVERSON

ASUSALPHA	Title : WLAN CONTROL	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 27 of 66	


SATA HDD
CON2802
SATA_CON_22P
NP_NC3
NP_NC1
NP_NC2
NP_NC4
SATA_TXP0 17
SATA_TXN0 17
SATA_RXN0_CON
SATA_RXP0_CON
C2802 3900PF/50V MLCC/+/-10%
C2801 3900PF/50V MLCC/+/-10%
SATA_RXN0 17
SATA_RXP0 17
+3VS
+5VS
TPC26T T2801
C2803 0.1UF/10V
C2804 10UF/10V
GND
07/05/17 To move the C2803 and C2804 from the +3Vs into the +5Vs --- iverson
07/0409 To change netname from DAC_HSYNC_BUF into DAC_HSYNC_GM --- Iverson
7 DAC_HSYNC_GM
U2801C
74ACT08SCX_NL
CRT_HSYNC 13
C1803
0.1UF/10V
7 DAC_VSYNC_GM
U2801D
CRT_VSYNC 13
07/0409 To change netname from DAC_VSYNC_BUF into DAC_VSYNC_GM --- Iverson
29 EC_BATLOW_BEEP
29 EC_PWM_DL
U2801B
BAT_LOW_BEEP 21
07/04/17 To use U2801 to gate EC_BATLOW_BEEP---Peng
U2801A
7,18,25,26,29 PLT_RST#
R3022 0Ohm
IDE_RST#
CD-ROM
17 IDE_PDD[15:0]
CD_CSEL : Pull-Up, CDROM as Slave, Pull-Down, CDROM as Master
R2806 470Ohm
R2807 470Ohm
CD_CSEL
R2805 4.7KOhm
IDE_PIORDY
R2804 8.2KOhm
INT_IRQ14
CON2803
BTOB_CON_50P
IDE_PDDREQ 17
IDE_PDIOR# 17
IDE_PDDACK# 17
IDE_PDA2 17
IDE_PDCS3# 17
10KOhm
R2802 @
C2808 0.1UF c0402
C2809 10UF/10V
CE2803 100UF/16V
07/05/11 To Change the ODD Part and Symbol. --- Iverson
symbol:nb_btob_50p_8hd_f_ra_lf2=>nb_btob_50p_6hd_f_ra_lf2
part:BTOB_CON_50P_8HOLD_OCTEK=>BTOB_CON_50P_6HOLD_OCTEK
ASUSALPHA
Title : PATA-SATA & ODD
ASUSALPHATeK COMPUTER INC.
Engineer: Horng Chou
Size Custom
Project Name TERESA20
Rev 2.0
Date: Thursday, July 05, 2007
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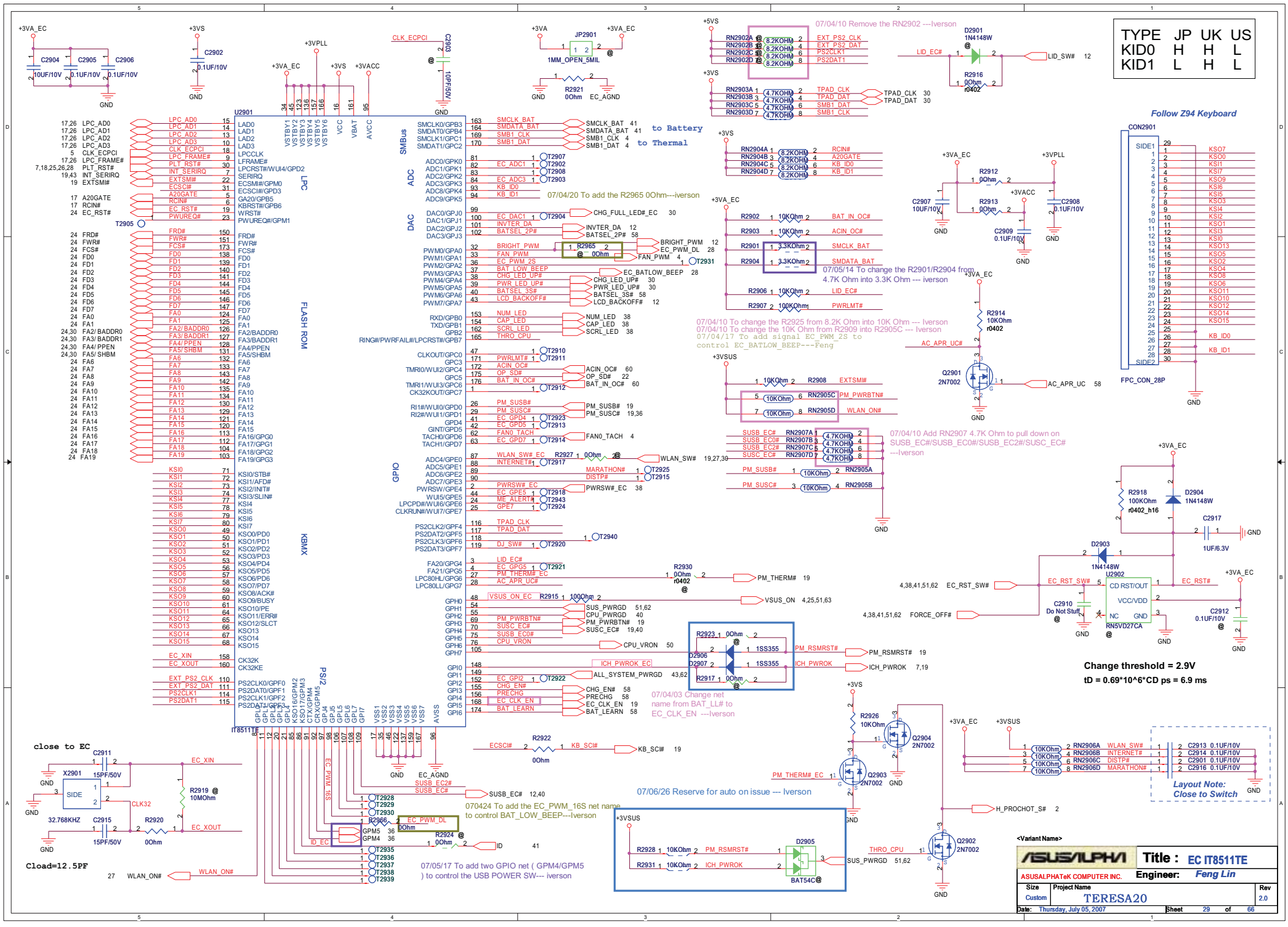
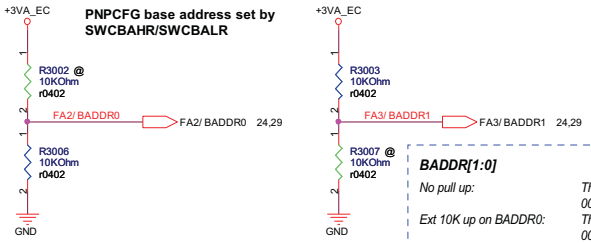

TYPE JP UK US
KID0 H H L
KID1 L H L
U2901
IT8511TE
LPC
FLASH ROM
KBMX
PS/2
SMBus
ADC
DAC
GPIO
to Battery
to Thermal
07/04/10 Remove the RN2902 ---Iverson
07/04/20 To add the R2965 0Ohm---iverson
07/05/14 To change the R2901/R2904 from 4.7K Ohm into 3.3K Ohm --- iverson
07/04/10 To change the R2925 from 8.2K Ohm into 10K Ohm --- Iverson
07/04/10 To change the 10K Ohm from R2909 into R2905C --- Iverson
07/04/17 To add signal EC_PWM_2S to control EC_BATLOW_BEEP---Feng
07/04/10 Add RN2907 4.7K Ohm to pull down on SUSB_EC#/SUSB_EC0#/SUSB_EC2#/SUSC_EC# ---Iverson
07/04/03 Change net name from BAT_LL# to EC_CLK_EN ---Iverson
Follow Z94 Keyboard
CON2901
FPC_CON_28P
Change threshold = 2.9V
tD = 0.69*10^6*CD ps = 6.9 ms
close to EC
Cload=12.5PF
X2901
SIDE
32.768KHZ
070424 To add the EC_PWM_16S net name to control BAT_LOW_BEEP---Iverson
07/05/17 To add two GPIO net (GPM4/GPM5) to control the USB POWER SW--- iverson
07/06/26 Reserve for auto on issue --- Iverson
Layout Note: Close to Switch
<Variant Name>
Title : EC IT8511TE
ASUSALPHATeK COMPUTER INC.
Engineer: Feng Lin
Size Custom
Project Name TERESA20
Rev 2.0
Date: Thursday, July 05, 2007
Sheet 29 of 66

EC Hardware Strap

Strap value sampled after VSTBY power up reset

PNPCFG base address set by SWCBAHR/SWCBALR



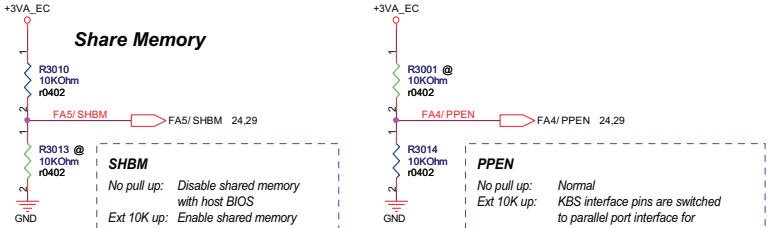
BADDR[1:0]

No pull up:	*The register pair to access PNPCFG is 002Eh and 002Fh.*
Ext 10K up on BADDR0:	*The register pair to access PNPCFG is 004Eh and 004Fh.*
Ext 10K up on BADDR1:	*The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.*

07/04/10 Remove the Adaptor --- Iverson

07/04/10 Remove the Adaptor --- Iverson

Share Memory



SHBM

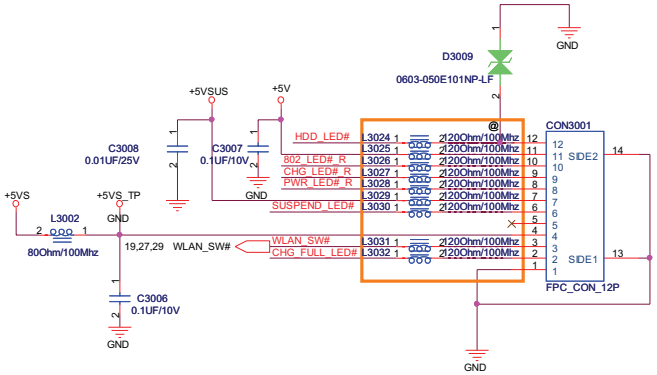
No pull up:	*Disable shared memory with host BIOS*
Ext 10K up:	*Enable shared memory with host BIOS*

PPEN

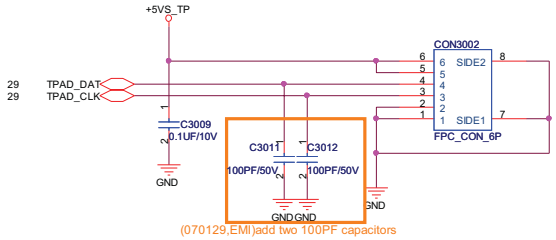
No pull up:	*Normal*
Ext 10K up:	*KBS interface pins are switched to parallel port interface for in-system programming.*

LED Board Interface

(070131,EMI)New addition for EMI
(070205)mount

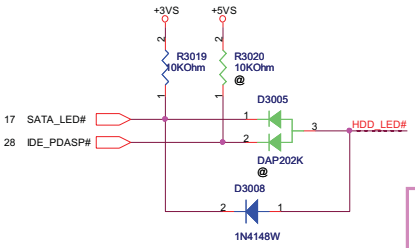


Touchpad Board Interface

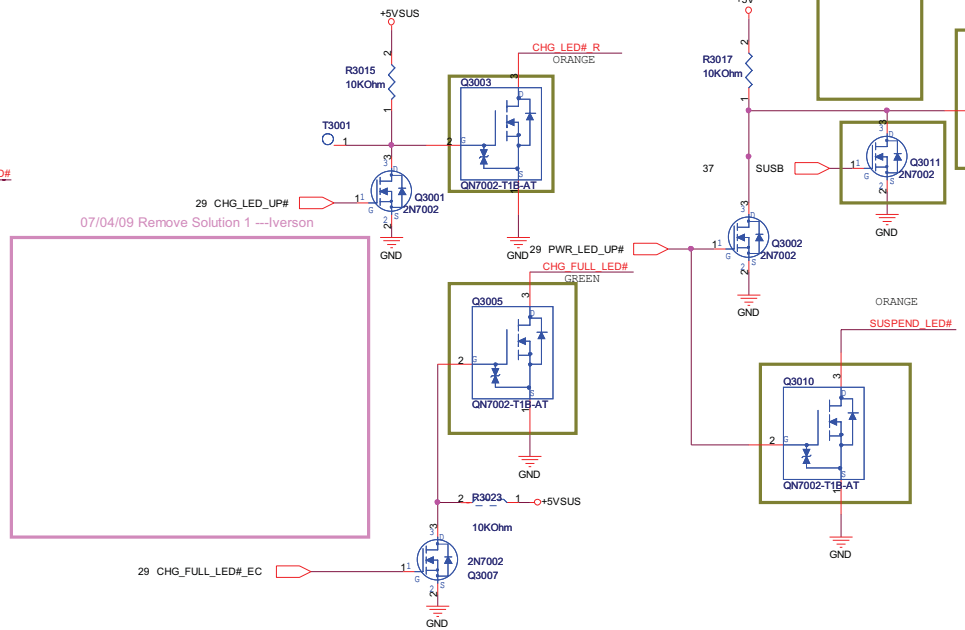


(070129,EMI)add two 100PF capacitors

HDD LED



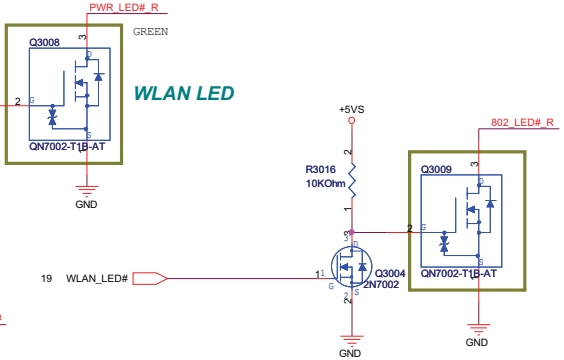
CHARGE LED



POWER LED

070426 To remove the D3006, and To add the Q3011. --- IVERSON

WLAN LED

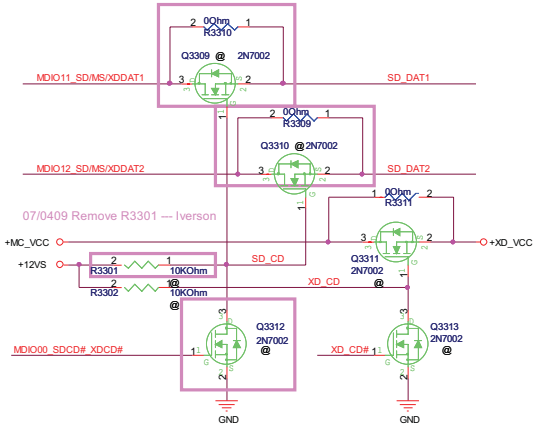


070426 To add the ehanced ESD transistor.
Q3003.Q3005.Q3008.Q3009.Q3010 --- IVERSON

ASUSALPHA	Title : EC IT8511/LED&TP CON.	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 30 of 66	

Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Thursday, July 05, 2007
Sheet	31 of 66

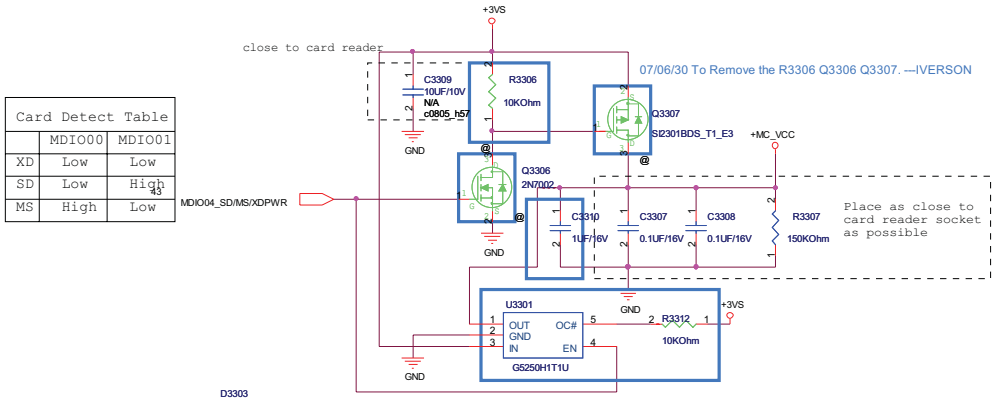
Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date: Thursday, July 05, 2007	Sheet 32 of 66

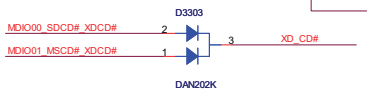


07/04/06 Add R3310 0 Ohm between MDIO11_SD/MS/XDDAT1 and SD_DAT1.
Add R3311 0 Ohm between MDIO12_SD/MS/XDDAT2 and SD_DAT2.
Remove Q3309 Q3310 Q3312 --- Iverson

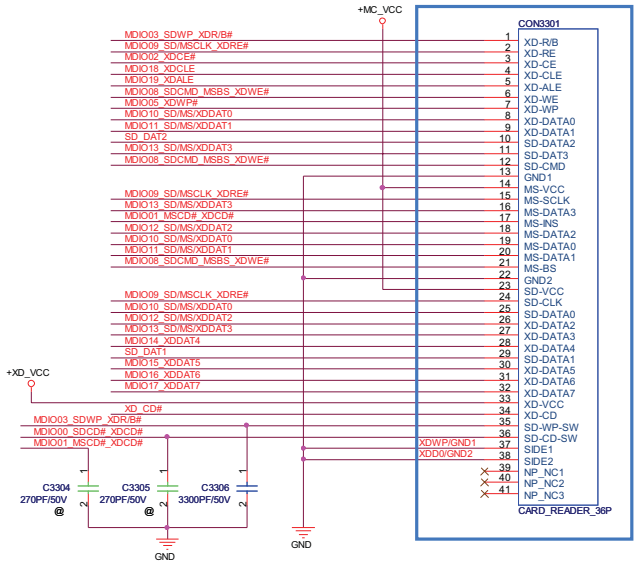
Name	Drive	Name	Drive
MDIO00	I - PU	MDIO10	I/O - PU
MDIO01	I - PU	MDIO11	I/O - PU
MDIO02	O - PU	MDIO12	I/O - PU
MDIO03	I - PU	MDIO13	I/O - PU
MDIO04	O - 3V	MDIO14	I/O - PU
MDIO05	O - 3V	MDIO15	I/O - PU
MDIO06	O - 3V	MDIO16	I/O - PU
MDIO07	I - 3V	MDIO17	I/O - PU
MDIO08	I/O - PU	MDIO18	I/O - PU
MDIO09	I/O - PU	MDIO19	I/O - PU

Card Detect Table		
	MDIO00	MDIO01
XD	Low	Low
SD	Low	High
MS	High	Low

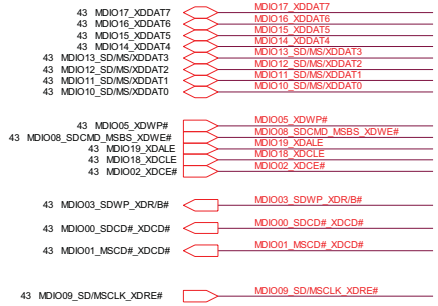


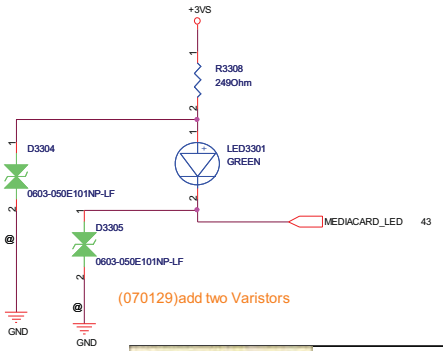


MEDIA CARD SLOT



07/06/26 Modify CON3301 PCB footprint ---iverson





(070129)add two Varistors

ASUSALPHATeK COMPUTER INC.

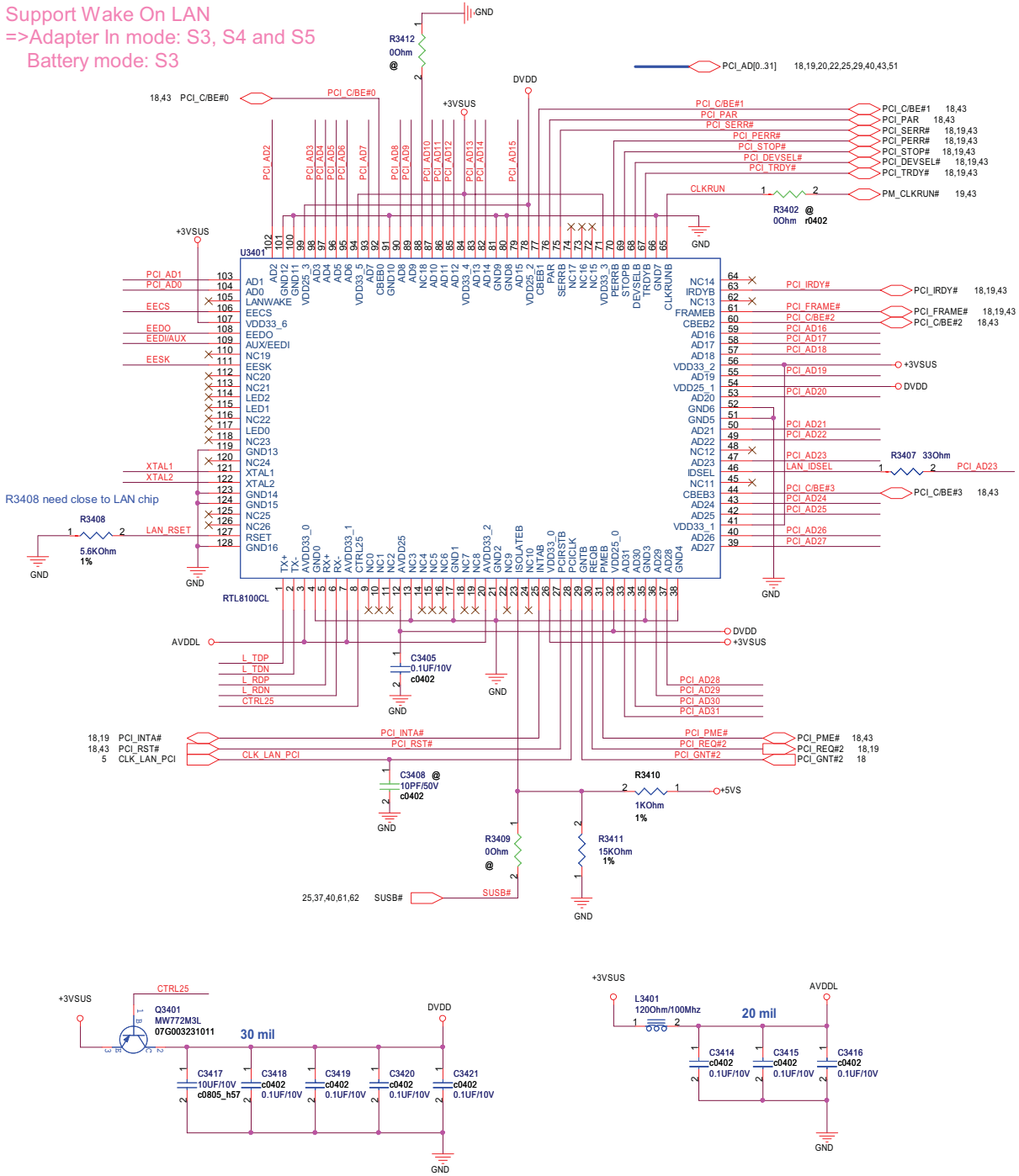
Title : MEDIA CARD SLOT

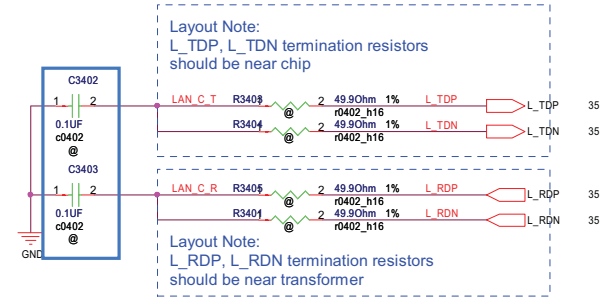
Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA20	2.0

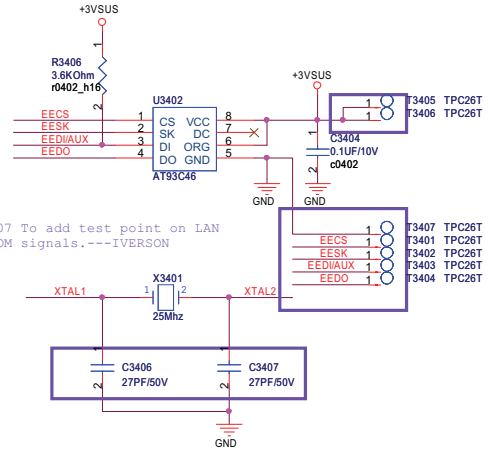
Date: Thursday, July 05, 2007 Sheet 33 of 66

Support Wake On LAN
=>Adapter In mode: S3, S4 and S5
Battery mode: S3



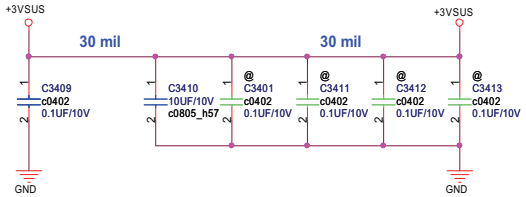


07/06/29 To change the C3402/C3403 from 0.01uF into 0.1uF.---iverson



070507 To add test point on LAN EEPROM signals.---IVERSON

07/05/16 To change the C3407/C3406 from 30pF into 27pF. --- Iverson

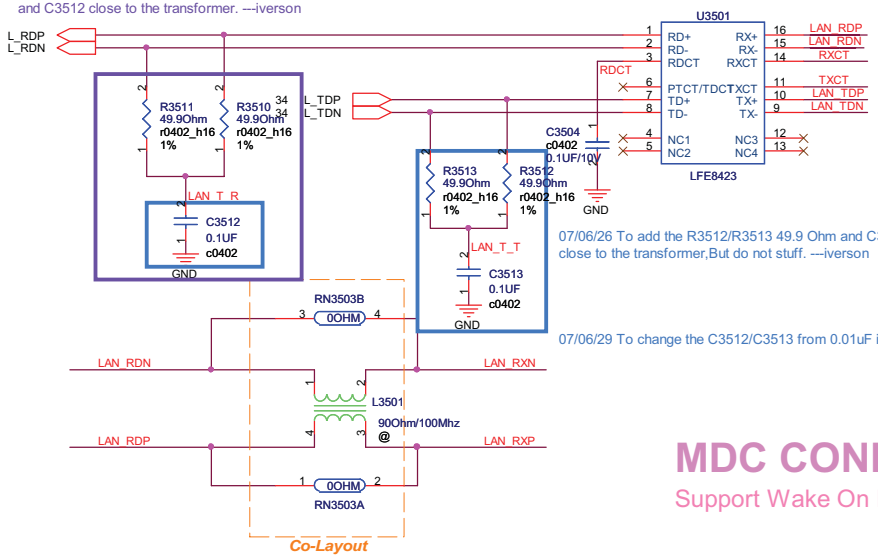


ASUSALPHA	Title : LAN_RTL8100CL	
ASUSALPHAtek COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 34 of 66	

LAN PORT

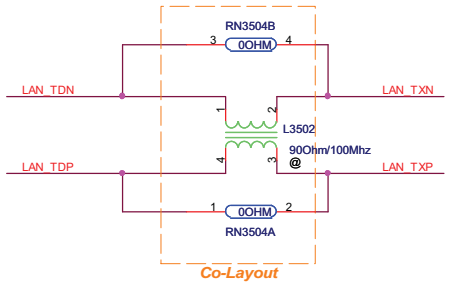
TRANSFORMER 10/100MB

07/05/14 To add the R3510/R3511 49.9 Ohm and C3512 close to the transformer. ---iverson

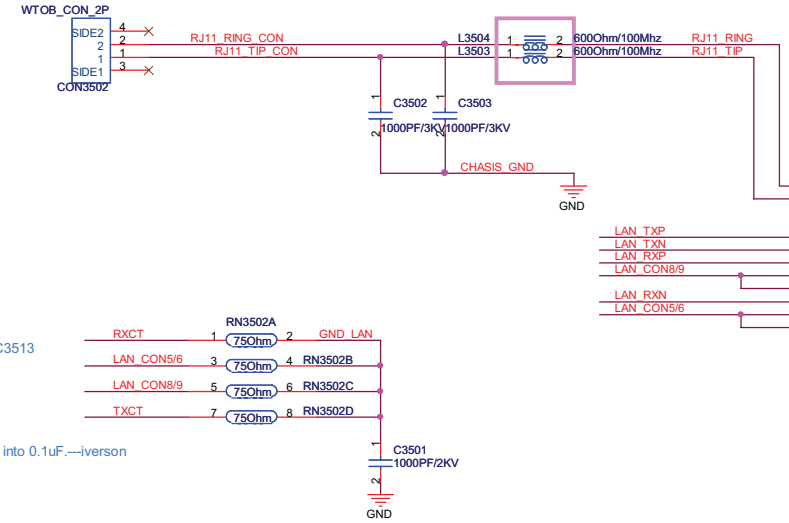


07/06/26 To add the R3512/R3513 49.9 Ohm and C3513 close to the transformer,But do not stuff. ---iverson

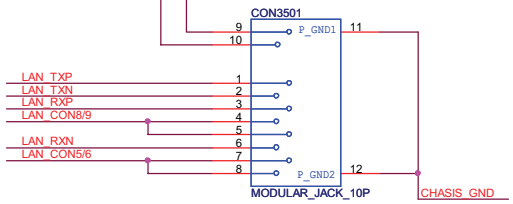
07/06/29 To change the C3512/C3513 from 0.01uF into 0.1uF.---iverson



07/04/10 To change the L3504/L3503 from 1K Ohm/100M Hz into 600 Ohm/100M Hz by EMI request. --- Iverson



RJ11&RJ45

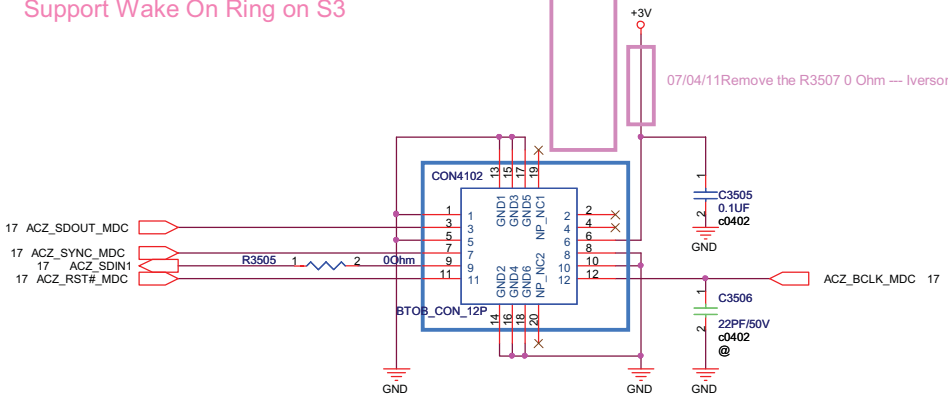


MDC CONNECTOR

Support Wake On Ring on S3

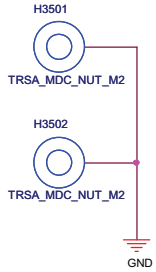
07/04/06 Remove R3506 0 ohm--- Iverson

07/04/11Remove the R3507 0 Ohm --- Iverson

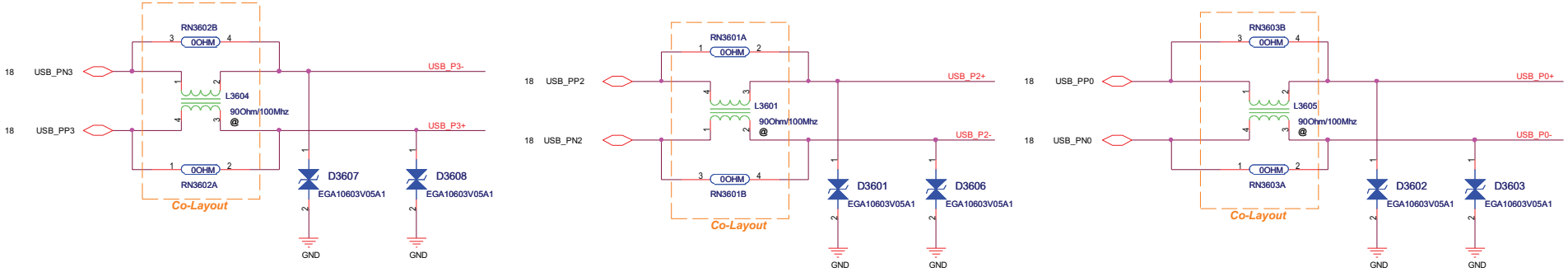


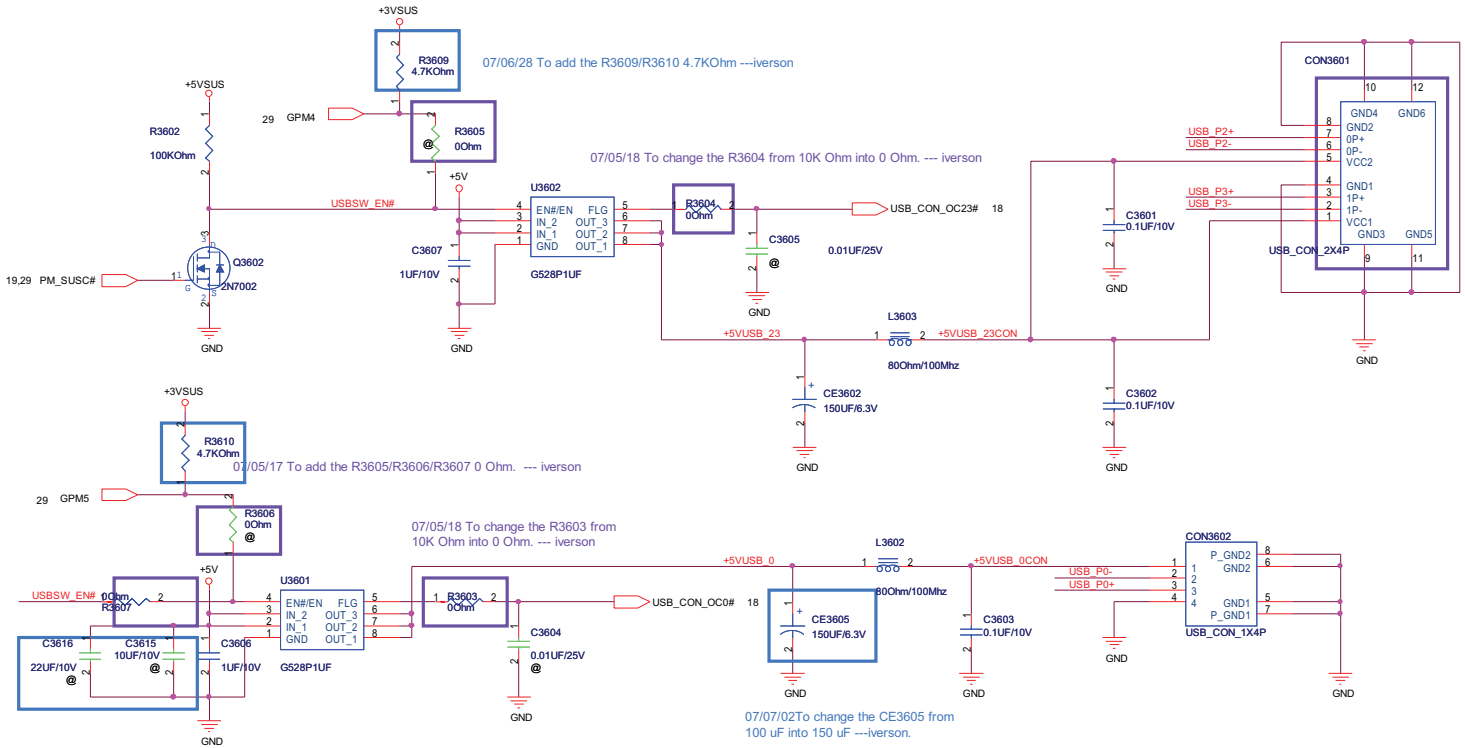
07/06/26 Modify the CON4102 PCB footprint --- iverson

B:MDC NUT

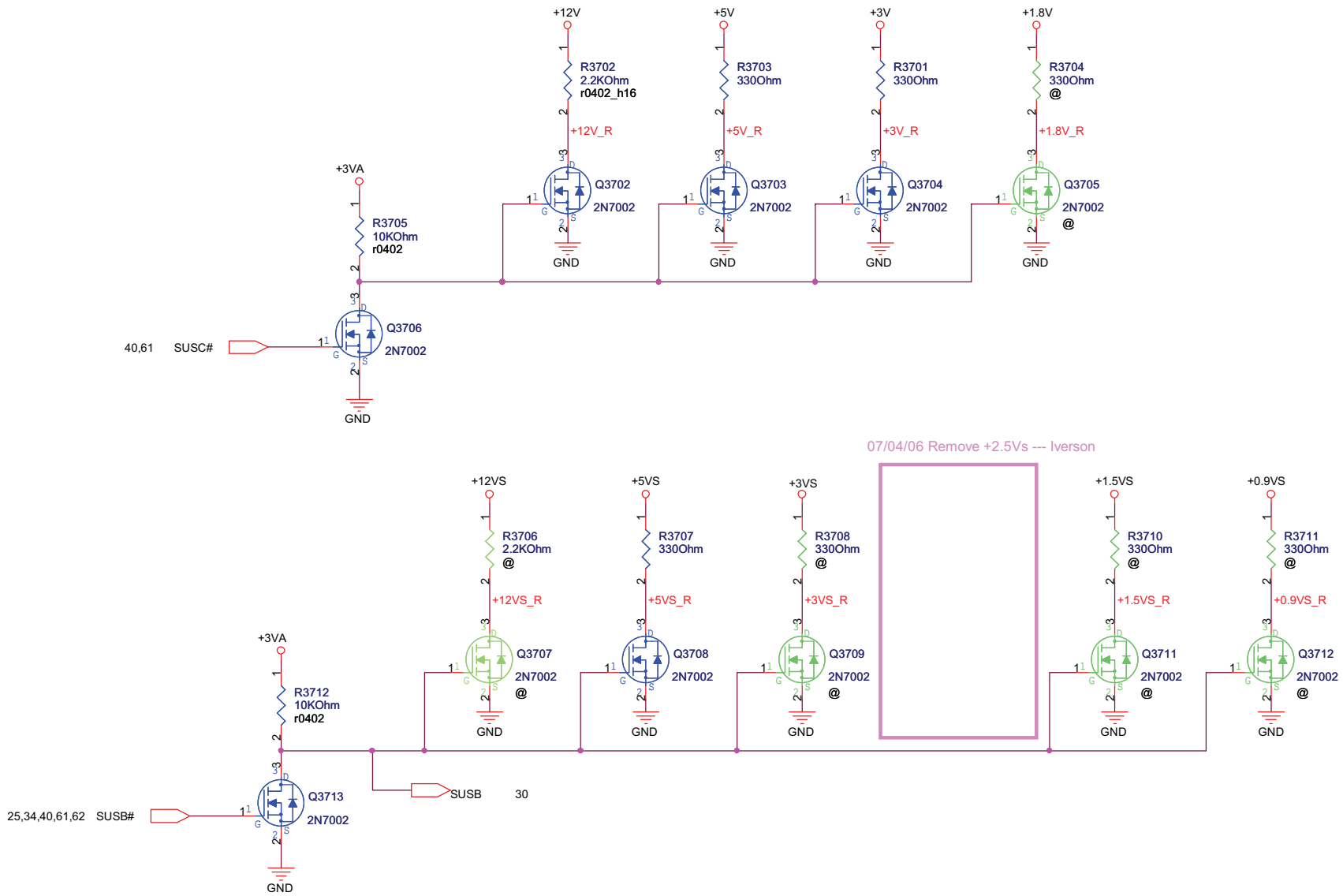


ASUSALPHAteK COMPUTER INC.	Title : RJ45/RJ11/MDC	
	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 35 of 66	



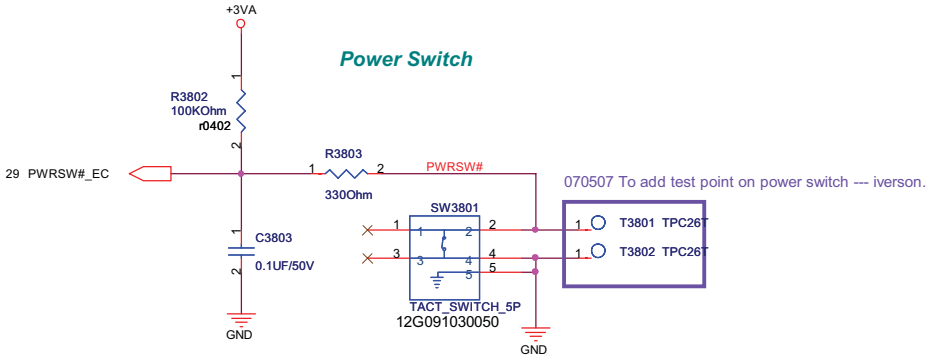


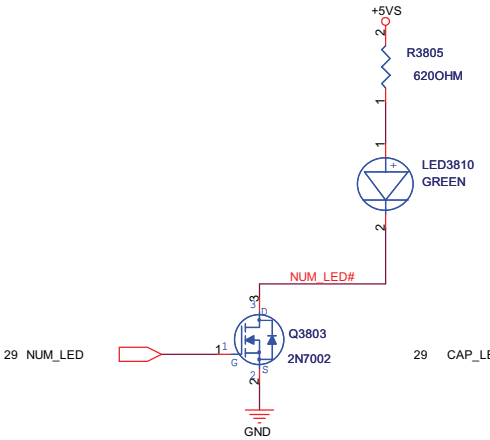
ASUSALPHA	Title : USB CONN x3	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 36 of 66	

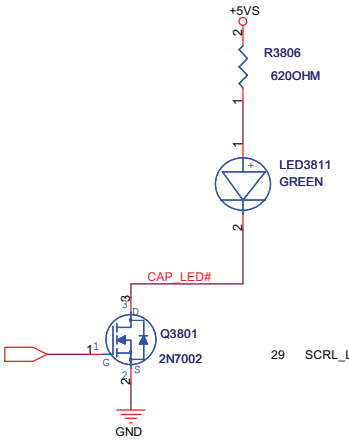


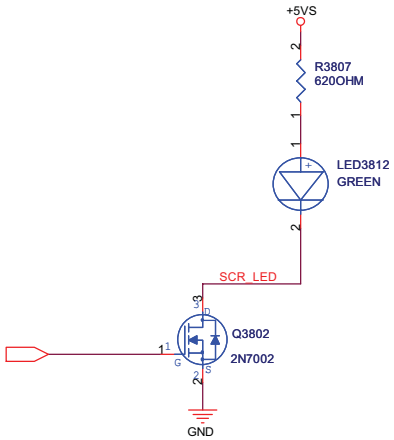
ASUSALPHA	Title : Discharge Circuit	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 37 of 66	

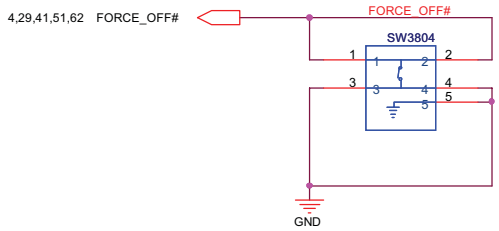
Main Board SW & LED





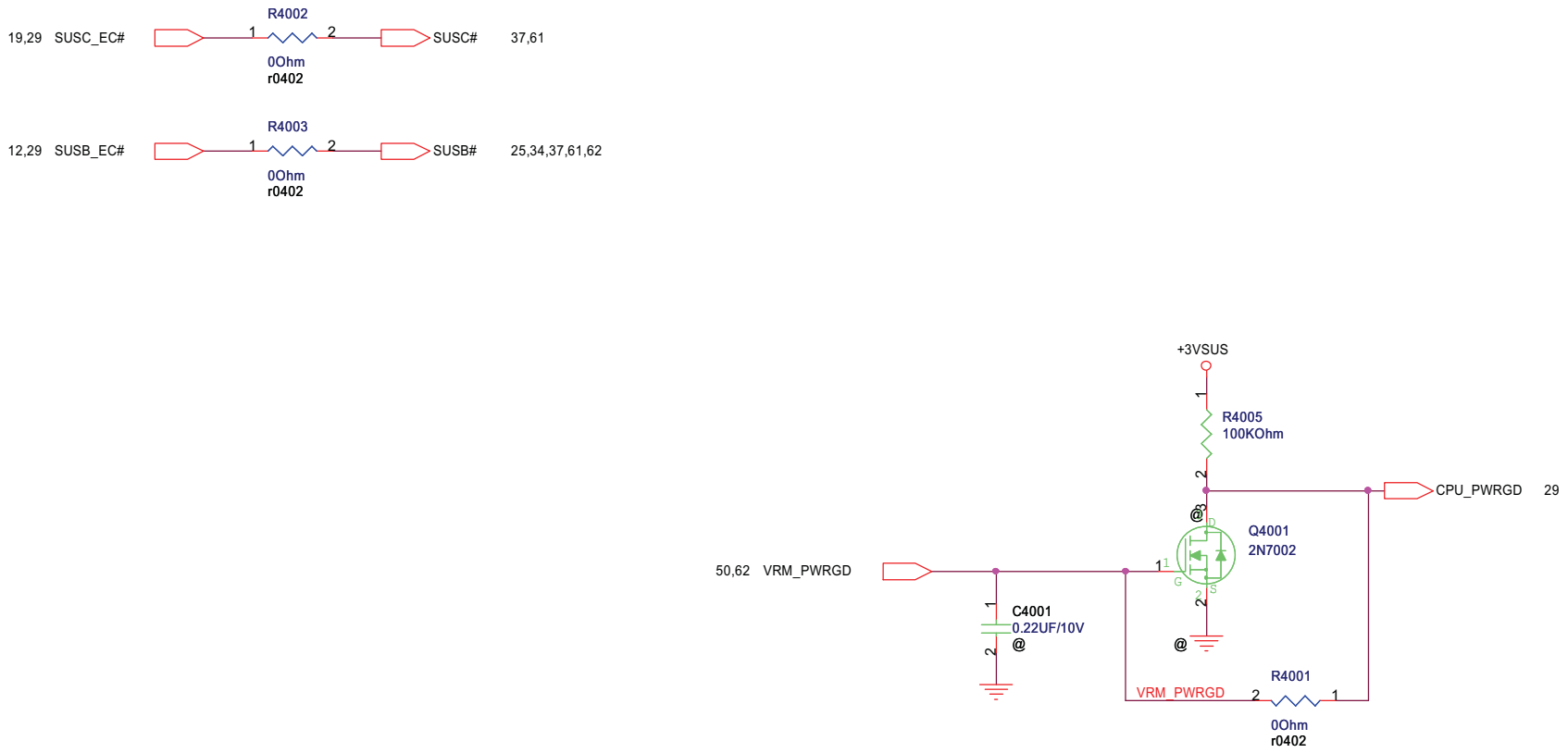






ASUSALPHA	Title : SW/LED	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 38 of 66	

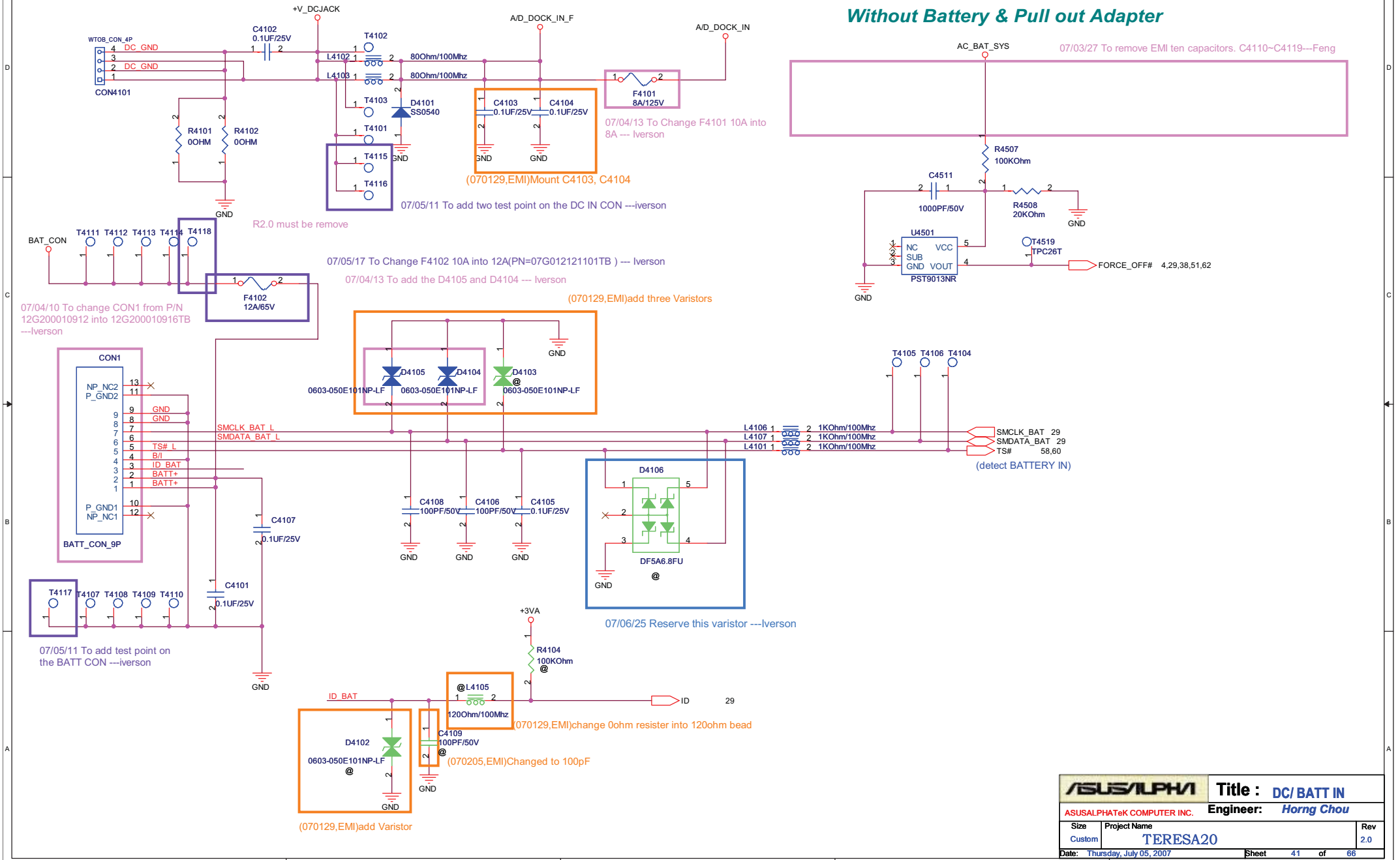
Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date: Thursday, July 05, 2007	Sheet 39 of 66



<Variant Name>

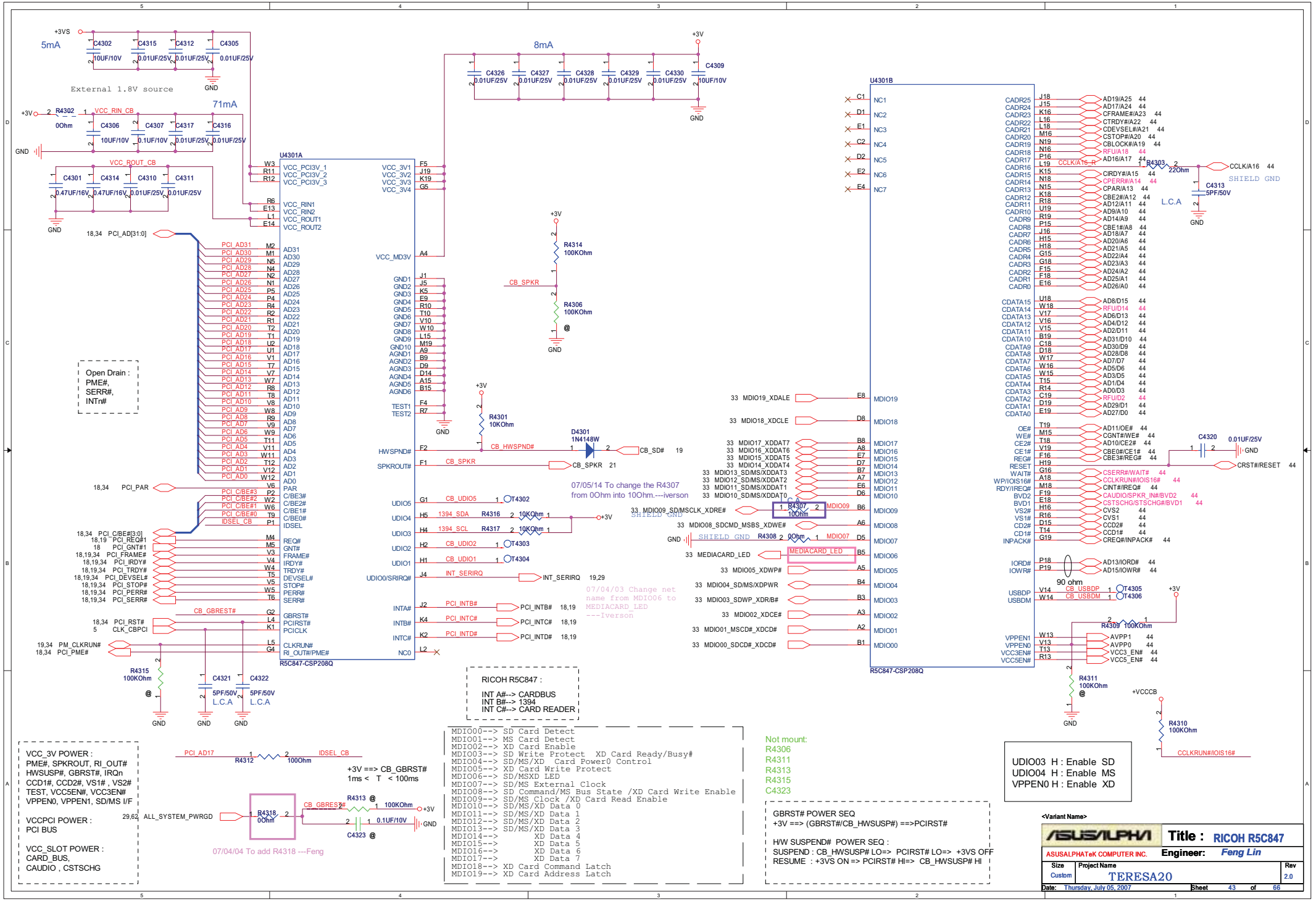
ASUSALPHA	Title : POWER-ON SEQ.	
ASUSALPHATeK COMPUTER INC.	Engineer: Feng Lin	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 40 of 66	

DC Power Jack



ASUSALPHA	Title : DC/ BATT IN	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 41 of 66	

Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date: Thursday, July 05, 2007	Sheet 42 of 66


5mA
8mA
71mA
External 1.8V source
U4301A
R5C847-CSP208Q
U4301B
R5C847-CSP208Q
Open Drain : PME#, SERR#, INTn#
07/05/14 To change the R4307 from 0Ohm into 10Ohm.---iverson
07/04/03 Change net name from MDI006 to MEDIACARD_LED ---Iverson
07/04/04 To add R4318 ---Feng
RICOH R5C847 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
VCC_3V POWER :
PME#, SPKROUT, RI_OUT#
HWSUSP#, GBRST#, IRQn
CCD1#, CCD2#, VS1# , VS2#
TEST, VCC5EN#, VCC3EN#
VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER :
PCI BUS
VCC_SLOT POWER :
CARD_BUS,
CAUDIO , CSTSCHG
+3V ==> CB_GBRST#
1ms < T < 100ms
MDI00--> SD Card Detect
MDI01--> MS Card Detect
MDI02--> XD Card Enable
MDI03--> SD Write Protect XD Card Ready/Busy#
MDI04--> SD/MS/XD Card Power0 Control
MDI05--> XD Card Write Protect
MDI06--> SD/MSXD LED
MDI07--> SD/MS External Clock
MDI08--> SD Command/MS Bus State /XD Card Write Enable
MDI09--> SD/MS Clock /XD Card Read Enable
MDI10--> SD/MS/XD Data 0
MDI11--> SD/MS/XD Data 1
MDI12--> SD/MS/XD Data 2
MDI13--> SD/MS/XD Data 3
MDI14--> XD Data 4
MDI15--> XD Data 5
MDI16--> XD Data 6
MDI17--> XD Data 7
MDI18--> XD Card Command Latch
MDI19--> XD Card Address Latch
Not mount:
R4306
R4311
R4313
R4315
C4323
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
Title : RICOH R5C847
ASUSALPHATeK COMPUTER INC.
Engineer: Feng Lin
Size Custom
Project Name TERESA20
Rev 2.0
Date: Thursday, July 05, 2007
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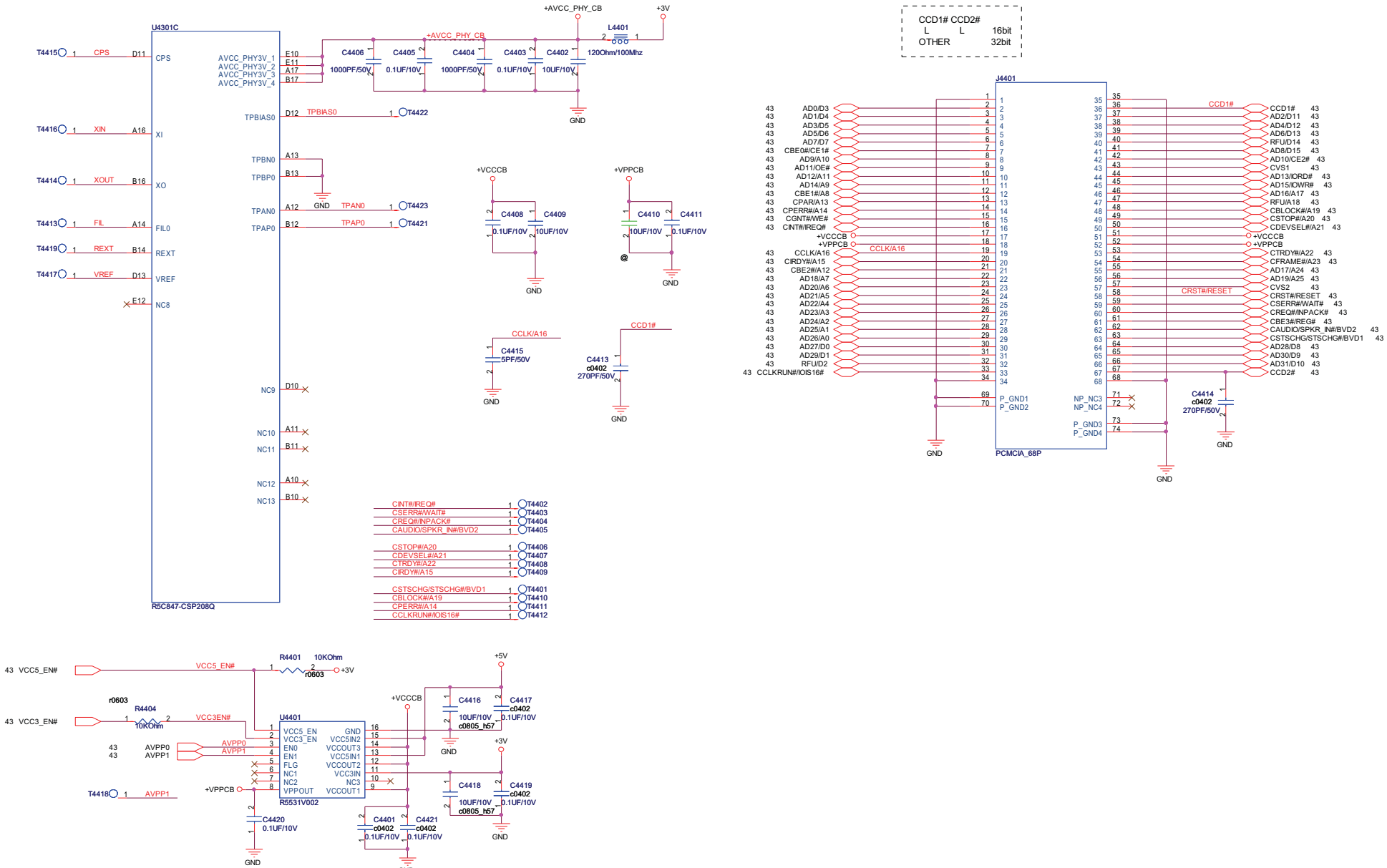
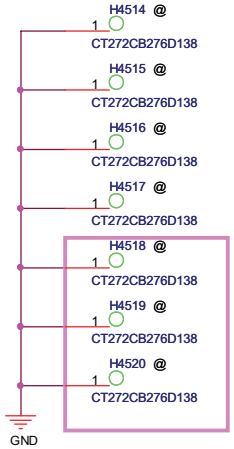
PCMCIA SOCKET



Title :	CARDBUS SOCKET	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 44 of 66	

A:CPU BKT

PN:s01756



B:MDC NUT

MDC NUT put on page35 (H3501, H3502)

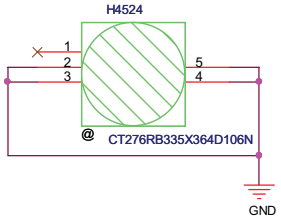
F:MINI CARD NUT

MINI CARD NUT put on page26(H2601, H2602)

07/04/03 Add CPU BKT. H4518 ~ H4520 ---Iverson

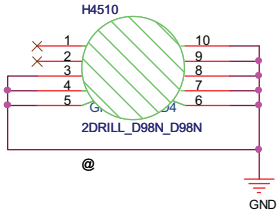
C:TOP TO BTM

PN:S01912



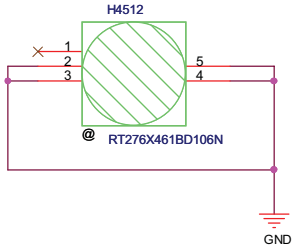
D:FIX MB

PN:s01769



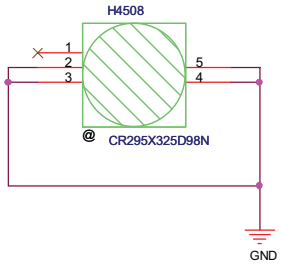
E:TOP TO BTM

PN:S01911



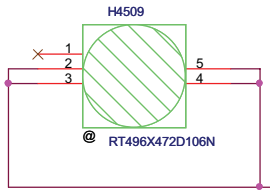
G:FIX MB

PN:s01783



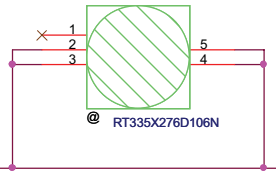
H:SYS BOSS

PN:S01914



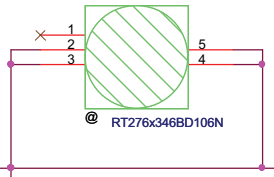
I:MB TO IO BKT

PN:S01913



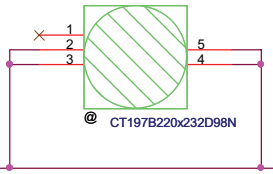
J:SYS BOSS

PN:S01915



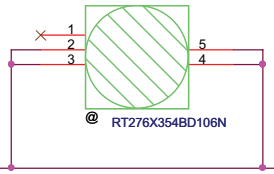
K:MB TO IO BKT

PN:S01705



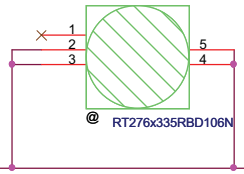
L:TOP TO BTM

PN:S01916



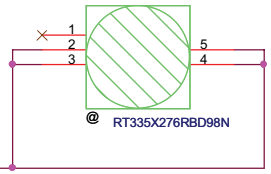
M:SYS BOSS

PN:s01917



N:TOP TO BTM

PN:S01851

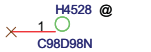


GND

07/04/04 To add 2 pcs U4508/U4509 EMI spring---Feng

O:ALIGNMENT HOLE

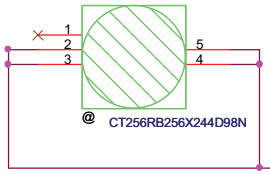
PN:temp_5262_gh15



07/04/03 Remove the T:NB SINK NUT --- Iverson

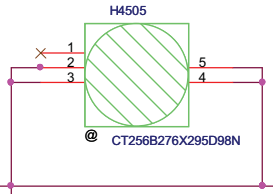
U:TOP TO BTM

PN:S01854



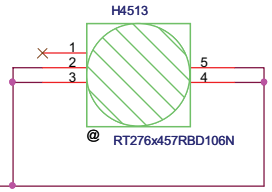
V:TOP TO BTM

PN:S01857



W:TOP TO BTM

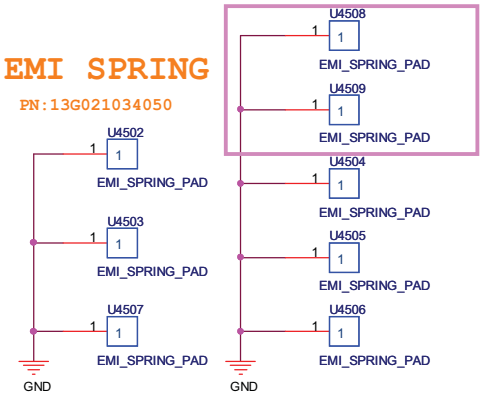
PN:S01918



GND

EMI SPRING

PN:13G021034050



P:ALIGNMENT HOLE

PN:s01724

EMI NUT

for LVDS cable

PN:13G021029050

ASUSALPHA	Title : SCREW HOLE	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 45 of 66	

R1.0 to R1.1

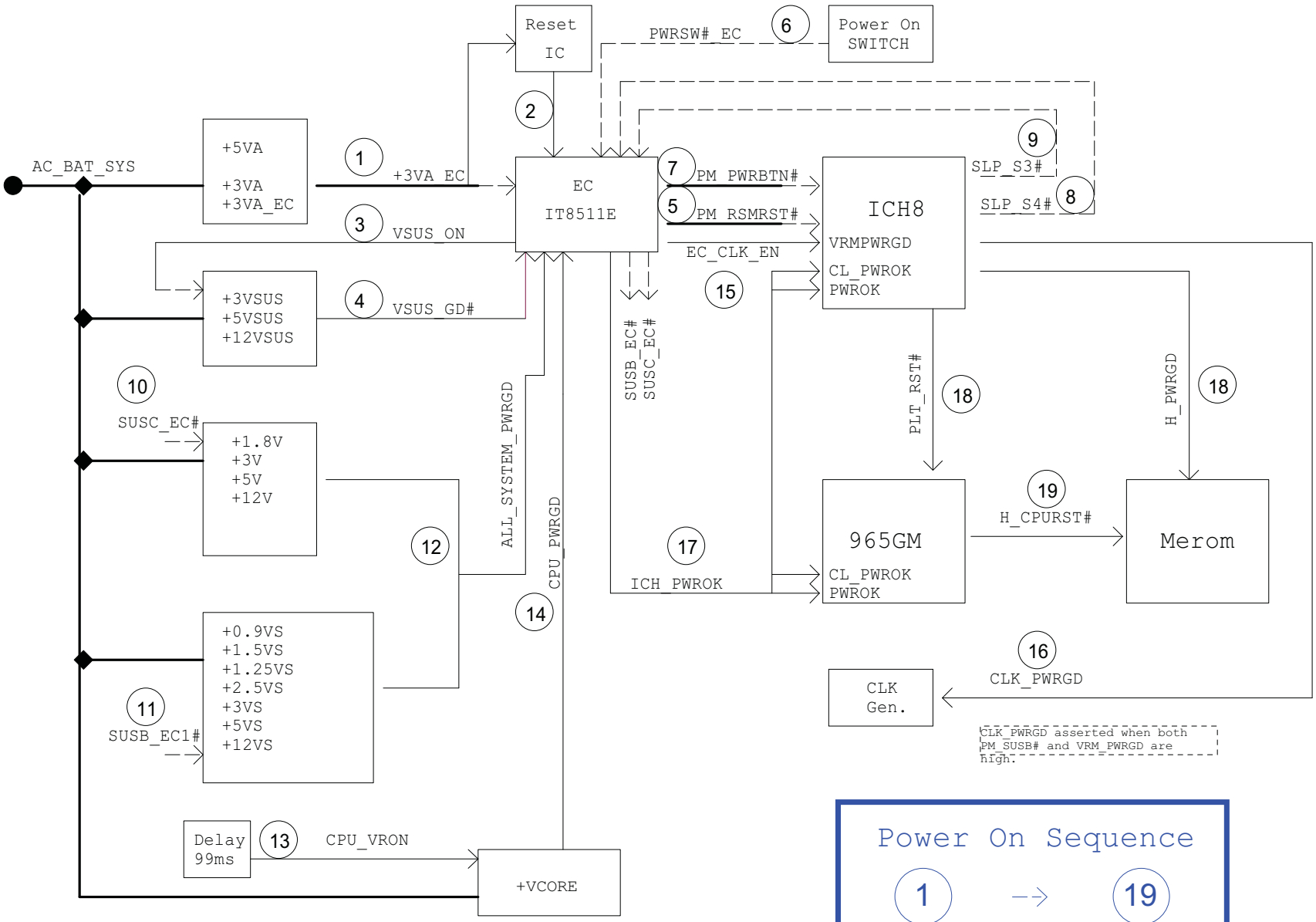
Page	Action
43	To add the varistor, but do not stuff. D4302~D4308
27	To add the ehanced ESD transistor.Q2702
30	To add the ehanced ESD transistor.Q3003.Q3005.Q3008.Q3009.Q3010
19	To change the BAT_LOW_1HZ into test point
12	To add the D1206
30	To remove the D3006, and To add the Q3011.
22	To add the C2250 and D2209, but the D2209 do not stuff
28	To Change the ODD Part andSymbol.
29	To add the EC_PWM_16S net name to control BAT_LOW_BEEP
28	To use U2801 to gate EC_BATLOW_BEEP
29	To add the R2965 0Ohm
21	To change codec from ADI1986 to ALC660.
22	To modify codec depop circuit.
23	To modify codec MIC peripheral circuit.
98	To add the ESD diode(D4302~D4308).

R1.2 to R2.0

Page	Action	Reason
22	To add Q2206 and Q2209 to solve the pop noise ,But do not stuff.	To solve pop noise of the codec
23	To add the T filter to solve pop noise of the MIC	To solve pop noise of the MIC
13	To change the CON1302 P/N from 12G10111015M into 12G10111215TTB	
29	Reserve for auto on issue	
35	To add the R3512/R3513 49.9 Ohm and C3513 close to the transformer,But do not stuff.	For RD verify
35	Modify the CON4102 PCB footprint	Slove SMT issue
25	Modify CON2501 PCB footprint	
33	Modify CON3301 PCB footprint	
15	Modify the CON1501 pcb footprint.	
05	To add the C0526 5pF on CLK_ICH14 signal.	
33	To add the C3310 1UF and the U3301 and R3312 10KOhm	
34	To change the C3402/C3403 from 0.01uF into 0.1uF	
35	To change the C3512/C3513 from 0.01uF into 0.1uF	
36	To add the C3616 22 uF and C3615 10uF.	
33	To Remove the R3306 Q3306 Q3307.	
19	R1950,R1951,R1953 change from 1% to 5%.	
05	R0505 change to RES 1K OHM 1/16W (0402) 1%.	
05	To change the R0514 from 390 Ohm into 300 Ohm.	
36	To change the CE3605 from 100 uF into 150 uF	
13	To add the L1307 L1308 L1309. Remove the Pi-type filter.	

R1.1 to R1.2

Page	Action
25	To connect the SCL_3A and SDA_3A signals.
36	To change the USB CON P/N from 12G13111108F into 12G13111108STB
3	To add test point on VID[0:6] signals.
15	To add the R1504、R1506、R1503 to configure memory
34	To add test point on LAN EEPROM signals.
21	To add the R2133 10KOhm,But do not stuff
22	To add the R2207/R2208 0Ohm Pull-down
13	To add the R1315 0Ohm
13	To change the R1309/R1310/R1311/R1312 from 2.2KOhm into 2KOhm
38	To add test point on power switch
24	To add test point on the ISA ROM
22	To modify HP_DET circuit
23	To modify MIC_DET circuit
41	To add two test point on the DC IN CON
41	To add test point on the BATT CON
22	To add the R2244 0Ohm, but do not stuff.
43	To change the R4307 from 0Ohm into 10 Ohm.
29	To change the R2901/R2904 from 4.7K Ohm into 3.3K Ohm
35	To add the R3510/R3511 49.9 Ohm and C3512 close to transformer.
36	To change the R3603/R3604 from 10K Ohm into 0 Ohm.
36	To add the R3605/R3606/R3607 0 Ohm
13	To remove the Q1302 and Q1304
20	To add the C2050 1uF on the +5VREF_ICH signal
22	To change the R2201/R2202 from 13K Ohm into 11K Ohm
22	To change the R2206/R2214 from 10K Ohm into 12K Ohm
29	To add two GPIO net (GPM4/GPM5) to control the USB POWER SW
28	To move the C2803 and C2804 from the +3Vs into the +5Vs
41	To Change F4102 10A into 12A(PN=07G012121101TB)
34	To change the C3407/C3406 from 30pF into 27pF
5	To change the C0510/C0511 from 33pF into 27pF.
17	To change the C1707/C1708 from 18pF into 10pF
4	Don't stuff R0415, but stuff R0416
16	To change U1601 PCB footprint from sot23_s5_rd1 to nb_sot23_s5_t



<Variant Name>

ASUSALPHA	Title : PowerOn sequence	
ASUSALPHATeK COMPUTER INC.	Engineer: Julian Kuo	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 47 of 66	

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BRIGHT_PWM	O	48	GPH0	VSUS_ON_EC	O
33	PWM1/GPA1	FAN_PWM	O	54	GPH1	SUS_PWRGD	I
36	PWM2/GPA2	/	O	55	GPH2	CPU_PWRGD	I
37	PWM3/GPA3	BAT_LOW_BEEP	O	69	GPH3	PM_PWRBTN#	O
38	PWM4/GPA4	CHG_LED_UP#	O	70	GPH4	SUSC_EC#	O
39	PWM5/GPA5	PWR_LED_UP#	O	75	GPH5	SUSB_EC0#	O
40	PWM6/GPA6	BATSEL_3S#	O	76	GPH6	CPU_VRON	O
43	PWM7/GPA7	LCD_BACKOFF#	O	105	GPH7	PM_RSMRST#	O
153	RXD/GPB0	NUM_LED	O	148	GPI0	ICH_PWROK_EC	O
154	TXD/GPB1	CAP_LED	O	149	GPI1	ALL_SYSTEM_PWRGD	O
162	GPB2	SCRL_LED	O	152	GPI2	/	
163	SMCLK0/GPB3	SMCLK_BAT	I/0	155	GPI3	CHG_EN#	O
164	SMDAT0GPB4	SMDATA_BAT	I/0	156	GPI4	PRECHG	O
5	GA20/GPB5	A20GATE	O	168	GPI5	EC_CLK_EN	O
6	KBRST#/GPB6	RCIN#	O	174	GPI6	BAT_LEARN	O
165	GPB7	THRO_CPU	O	109	GPI7	SUSB_EC2#	
47	CLKOUT/GPC0	/	O	99	DAC0/GPJ0	CHG_FULL_LED#_EC	O
169	SMCLK1/GPC1	SMB1_CLK	I/0	100	DAC1/GPJ1	/	
170	SMDAT1/GPC2	SMB1_DAT	I/0	101	DAC2/GPJ2	INVTER_DA	O
171	GPC3	/	I	102	DAC3/GPJ3	BATSEL_2P#	O
172	TMRI0/WUI2/GPC4	ACIN_OC#	I	97	GPJ4	EC_PWM_16S	
175	GPC5	OP_SD#	O	98	GPJ5	/	
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I				
1	CK32KOUT/GPC7	/	O				
26	RI1#/WUI0/GPD0	PM_SUSB#	I	81	ADC0/GPK0	/	I
29	RI2#/WUI1/GPD1	PM_SUSC#	I	82	ADC1/GPK1	/	
30	LPCRST#/WUI4//GPD2	PLT_RST#	I	83	ADC2/GPK2	/	I
31	ECSCI#/GPD3	ECSCI#	O	84	ADC3/GPK3	/	
41	GPD4	/		93	ADC8/GPK4	KB_ID0	I
42	GINT/GPD5	/		94	ADC9/GPK5	KB_ID1	I
62	TACH0/GPD6	FAN0_TACH	I				
63	TACH1/GPD7	/	O				
87	ADC4/GPE0	WLAN_SW#_EC(Reserved)	I	8	GPL0	WLAN_ON#	O
88	ADC5/GPE1	/	I	11	GPL1	/	O
89	ADC6/GPE2	/	I	12	GPL2	/	I
90	ADC7/GPE3	/	I	20	GPL3	/	O
2	PWRSW/GPE4	PWRSW#_EC	I	21	GPL4	/	
44	WUI5/GPE5	/		106	GPL5	/	
24	LPCPD#/WUI6/GPE6	/	I	107	GPL6	/	
25	CLKRUN#/WUI7/GPE7	/	O	108	GPL7	SUSB_EC#	
110	PS2CLK0/GPF0	/		22	ECSMI#/GPM0	EXTSMI#	O
111	PS2DAT0/GPF1	/		23	PWUREQ#/GPM1	/	
114	PS2CLK1/GPF2	/	I/0	85	KSO16/GPM2	/	
115	PS2DAT1/GPF3	/	I/0	86	KSO17/GPM3	ID_EC (Reserved)	I
116	PS2CLK2/GPF4	TPAD_CLK		91	CTX/GPM4	GPM4	
117	PS2DAT2/GPF5	TPAD_DAT		92	CRX/GPM5	GPM5	
118	PS2CLK3/GPF6	/					
119	PS2DAT3/GPF7	/	I				
113	FA16/GPG0	FA16					
112	FA17/GPG1	FA17					
104	FA18/GPG2	FA18					
103	FA19/GPG3	FA19					
3	FA20/GPG4	LID_EC#	I				
4	FA21/GPG5	/					
27	LPC80HL/GPG6	PM_THERM#_EC(Reserved)	O				
28	LPC80LL/GPG7	AC_APR_UC#	I				

ICH8-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AG12	GPIO00/BM_BUSY#	PM_BMBUSY#	I
AJ8	GPIO01/TACH1	/	I
F8	GPIO02/PIRQE#	PCI_INTE#	I
G11	GPIO03/PIRQF#	PCI_INTF#	I
F12	GPIO04/PIRQG#	PCI_INTG#	I
B3	GPIO05/PIRQH#	PCI_INTH#	I
AC21	GPIO06	/	I/O
AH9	GPIO07	/	I
AE16	GPIO08	EXTSMI#	I
AG19	GPIO09	/	I
AJ24	GPIO10	WLAN_SW#_ICH	I
AG22	SMBALERT#/GPIO11	/	I
AC19	GPIO12	KBC_SC#	I
AH21	GPIO13	/	I
AF22	GPIO14	/	I
AE20	GPIO15	STP_PCI#	O
AJ14	GPIO16	PM_DPRSLPVR	O
AG8	GPIO17	NEWCARD_OFF#	O
AH12	GPIO18	BTO_DEV0	O
AJ10	GPIO19/SATA1GP	NEWCARD_DET#	I
AE11	GPIO20	BTO_DEV1	O
AJ12	GPIO21/SATA0GP	/	I
AG10	REQ4#/GPIO22	WLAN_LED#	I
E6	LDRQ1#/GPIO23	/	
AJ27	GPIO24	/	
AG18	GPIO25	STP_CPU#	O
AH27	GPIO26	/	
AH25	GPIO27	BAT_LOW_1HZ	I
AD16	GPIO28	CB_SD#	O
AG17	GPIO29/OC#5	USB_OC_5#	I
AD12	GPIO30/OC#6	NEWCARD_OC#	I
AJ18	GPIO31/OC#7	USB_OC_7#	I
AH11	GPIO32/CLKRUN#	PM_CLKRUN#	I/O
AE10	GPIO33/AZ_DOCK_EN#	/	I
AG14	GPIO34/AZ_DOCK_RST#	/	I
AG13	GPIO35	BTO_DEV2	O
AF11	GPIO36/SATA2GP	/	
AG11	GPIO37/SATA3GP	PCB_ID0	I
AF9	GPIO38	PCB_ID1	I
AJ11	GPIO39	PCB_ID2	I
AD10	GNT4#/GPIO48	/	O
AG29	GPIO49/CPUPWRGD	H_PWRGD	O

Indigo: the same as T12EG
Pink: different from T12EG

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD23	2	A
CARDBUS	AD17	1	B
1394	AD17	1	C
CARD READER	AD17	1	D

PCIE Device	Bus		
MINI_CARD	PE(T/R)(p/n)2		
NEWCARD	PE(T/R)(p/n)3		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

<Variant Name>

ASUSALPHA

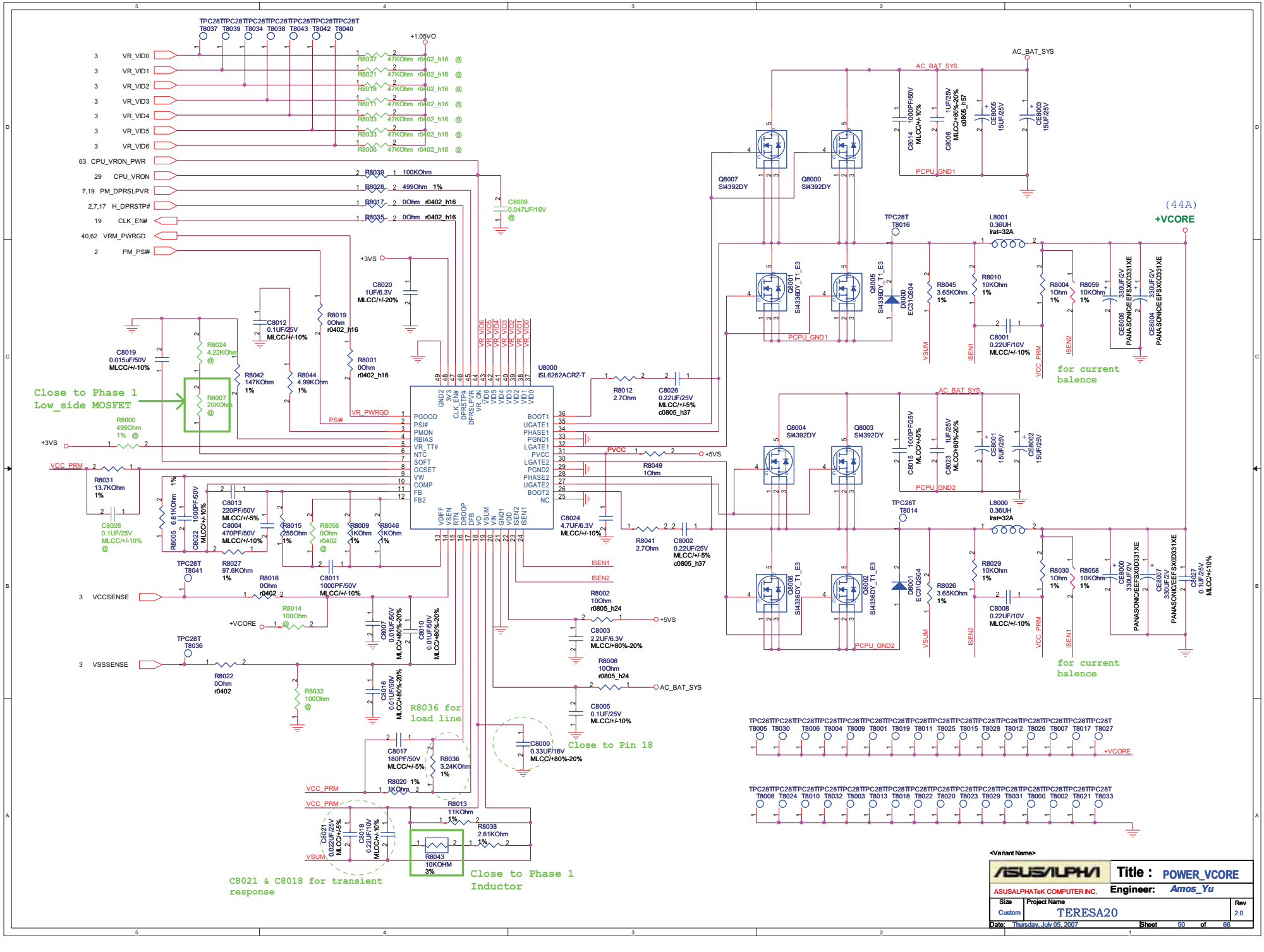
Title : GPIO Setting

ASUSALPHATeK COMPUTER INC. Engineer: Iverson Qiu

Size	Project Name	Rev
Custom	TERESA20	2.0

Date: Thursday, July 05, 2007 Sheet 48 of 66

Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date: Thursday, July 05, 2007	Sheet 49 of 66


U8000
ISL6262ACRZ-T
Q8007 SI4392DY
Q8000 SI4392DY
Q8001 SI4336DY_T1_E3
Q8005 SI4336DY_T1_E3
Q8004 SI4392DY
Q8003 SI4392DY
Q8006 SI4336DY_T1_E3
Q8002 SI4336DY_T1_E3
D8000 EC31QS04
D8001 EC31QS04
L8001 0.36UH Irat=32A
L8000 0.36UH Irat=32A
+VCORE
(44A)
AC_BAT_SYS
PCPU_GND1
PCPU_GND2
VCC_PRM
VSUM
ISEN1
ISEN2
PS#
VR_PWRGD
PVCC
+5VS
+3VS
+1.05VO
VCCSENSE
VSSSENSE
Close to Phase 1 Low_side MOSFET
for current balence
R8036 for load line
Close to Pin 18
C8021 & C8018 for transient response
Close to Phase 1 Inductor
Variant Name
ASUSALPHA
Title : POWER_VCORE
ASUSALPHATeK COMPUTER INC.
Engineer: Amos_Yu
Size Custom
Project Name TERESA20
Rev 2.0
Date: Thursday, July 05, 2007
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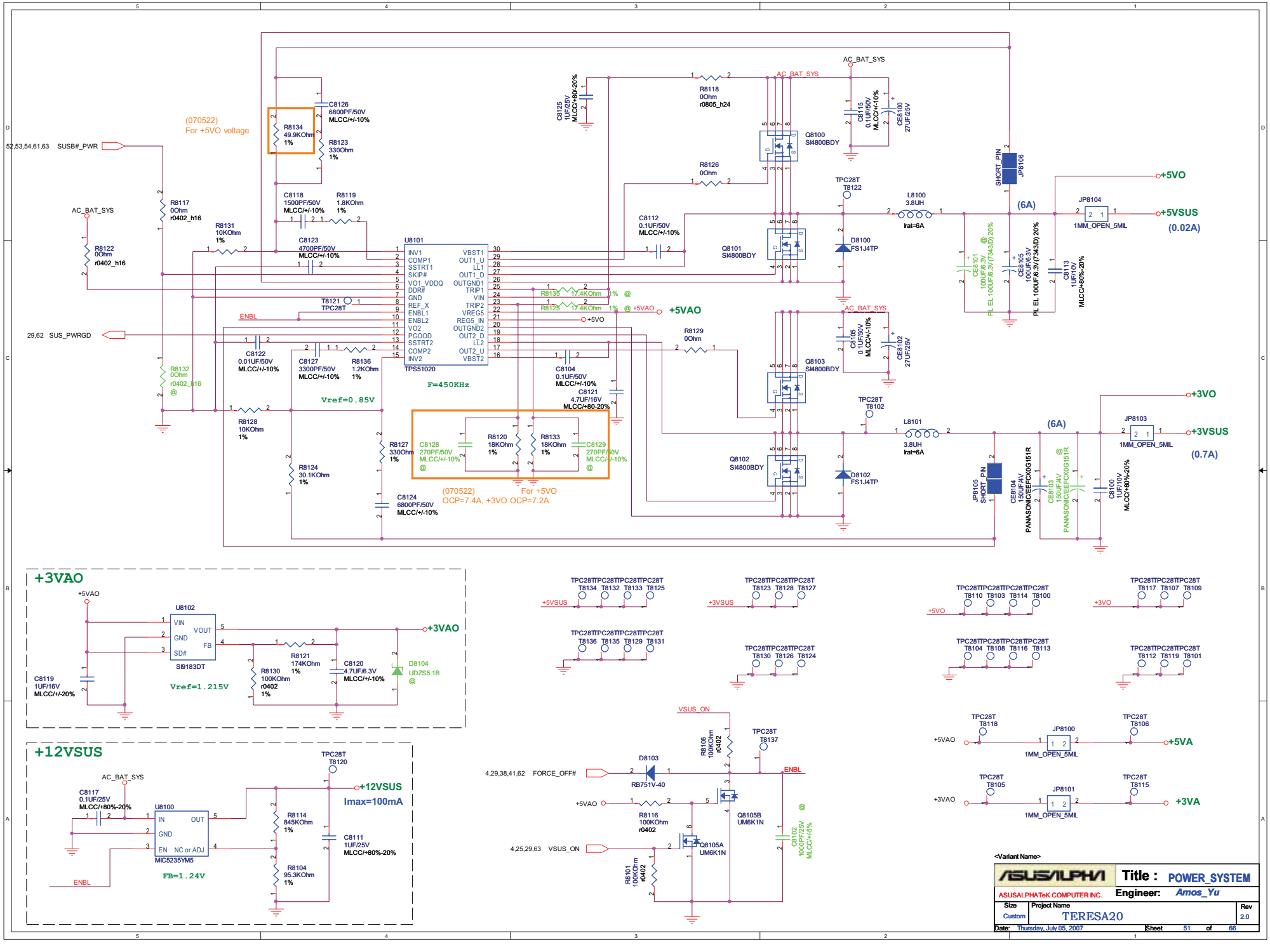
(070522)
For +5VO voltage
52,53,54,61,63 SUSB#_PWR
AC_BAT_SYS
R8117 0Ohm r0402_h16
R8122 0Ohm r0402_h16
R8131 10KOhm 1%
R8134 49.9KOhm 1%
R8123 330Ohm 1%
C8126 6800PF/50V MLCC/+/-10%
C8118 1500PF/50V MLCC/+/-10%
R8119 1.8KOhm 1%
C8123 4700PF/50V MLCC/+/-10%
U8101
INV1
COMP1
SSTRT1
SKIP#
VO1_VDDQ
DDR#
GND
REF_X
ENBL1
ENBL2
VO2
PGOOD
SSTRT2
COMP2
INV2
VBST1
OUT1_U
LL1
OUT1_D
OUTGND1
TRIP1
VIN
TRIP2
VREG5
REG5_IN
OUTGND2
OUT2_D
LL2
OUT2_U
VBST2
TPS51020
F=450KHz
Vref=0.85V
ENBL
T8121 TPC28T
29,62 SUS_PWRGD
R8132 0Ohm r0402_h16 @
C8122 0.01UF/50V MLCC/+/-10%
C8127 3300PF/50V MLCC/+/-10%
R8136 1.2KOhm 1%
R8128 10KOhm 1%
R8124 30.1KOhm 1%
R8127 330Ohm 1%
C8124 6800PF/50V MLCC/+/-10%
C8125 1UF/25V MLCC/+80/-20%
R8118 0Ohm r0805_h24
R8126 0Ohm
C8112 0.1UF/50V MLCC/+/-10%
R8135 17.4KOhm 1% @
R8125 17.4KOhm 1% @ +5VAO
+5VO
+5VAO
C8104 0.1UF/50V MLCC/+/-10%
C8121 4.7UF/16V MLCC/+80-20%
C8128 270PF/50V MLCC/+/-10% @
R8120 18KOhm 1%
R8133 18KOhm 1%
C8129 270PF/50V MLCC/+/-10% @
(070522)
OCP=7.4A, +3VO OCP=7.2A
For +5VO
Q8100 SI4800BDY
Q8101 SI4800BDY
Q8103 SI4800BDY
Q8102 SI4800BDY
C8115 0.1UF/50V MLCC/+/-10%
CE8100 27UF/25V
TPC28T T8122
L8100 3.8UH Irat=6A
D8100 FS1J4TP
SHORT_PIN JP8106
(6A)
JP8104 1MM_OPEN_5MIL
+5VO
+5VSUS
(0.02A)
CE8101 100UF/6.3V(7343D) 20% @ PL EL 100UF/6.3V(7343D) 20%
CE8105 100UF/6.3V(7343D) 20% PL EL 100UF/6.3V(7343D) 20%
C8113 1UF/10V MLCC/+80%-20%
R8129 0Ohm
C8105 0.1UF/50V MLCC/+/-10%
CE8102 27UF/25V
TPC28T T8102
L8101 3.8UH Irat=6A
D8102 FS1J4TP
JP8105 SHORT_PIN
CE8104 150UF/4V PANASONIC/EEFCX0G151R
CE8103 150UF/4V PANASONIC/EEFCX0G151R @
C8100 1UF/10V MLCC/+80%-20%
JP8103 1MM_OPEN_5MIL
+3VO
+3VSUS
(0.7A)
+3VAO
U8102
VIN
GND
SD#
VOUT
FB
SI9183DT
C8119 1UF/16V MLCC/+/-20%
Vref=1.215V
R8130 100KOhm r0402 1%
R8121 174KOhm 1%
C8120 4.7UF/6.3V MLCC/+/-10%
D8104 UDZS5.1B @
+12VSUS
Imax=100mA
TPC28T T8120
AC_BAT_SYS
C8117 0.1UF/25V MLCC/+80%-20%
U8100
IN
GND
EN
OUT
NC or ADJ
MIC5235YM5
ENBL
FB=1.24V
R8114 845KOhm 1%
R8104 95.3KOhm 1%
C8111 1UF/25V MLCC/+80%-20%
TPC28TTPC28TTPC28TTPC28T T8134 T8132 T8133 T8125 +5VSUS
TPC28TTPC28TTPC28T T8123 T8128 T8127 +3VSUS
TPC28TTPC28TTPC28TTPC28T T8110 T8103 T8114 T8100 +5VO
TPC28TTPC28TTPC28T T8117 T8107 T8109 +3VO
TPC28TTPC28TTPC28TTPC28T T8136 T8135 T8129 T8131
TPC28TTPC28TTPC28T T8130 T8126 T8124
TPC28TTPC28TTPC28TTPC28T T8104 T8108 T8116 T8113
TPC28TTPC28TTPC28T T8112 T8119 T8101
VSUS_ON
R8108 100KOhm r0402
TPC28T T8137
D8103 RB751V-40
4,29,38,41,62 FORCE_OFF#
ENBL
+5VAO
R8116 100KOhm r0402
Q8105B UM6K1N
Q8105A UM6K1N
4,25,29,63 VSUS_ON
R8101 100KOhm r0402
C8102 1000PF/25V MLCC/+/-5% @
TPC28T T8118 +5VAO JP8100 1MM_OPEN_5MIL TPC28T T8106 +5VA
TPC28T T8105 +3VAO JP8101 1MM_OPEN_5MIL TPC28T T8115 +3VA
<Variant Name>
ASUSALPHA
Title : POWER_SYSTEM
ASUSALPHATeK COMPUTER INC.
Engineer: Amos_Yu
Size Custom
Project Name TERESA20
Rev 2.0
Date: Thursday, July 05, 2007
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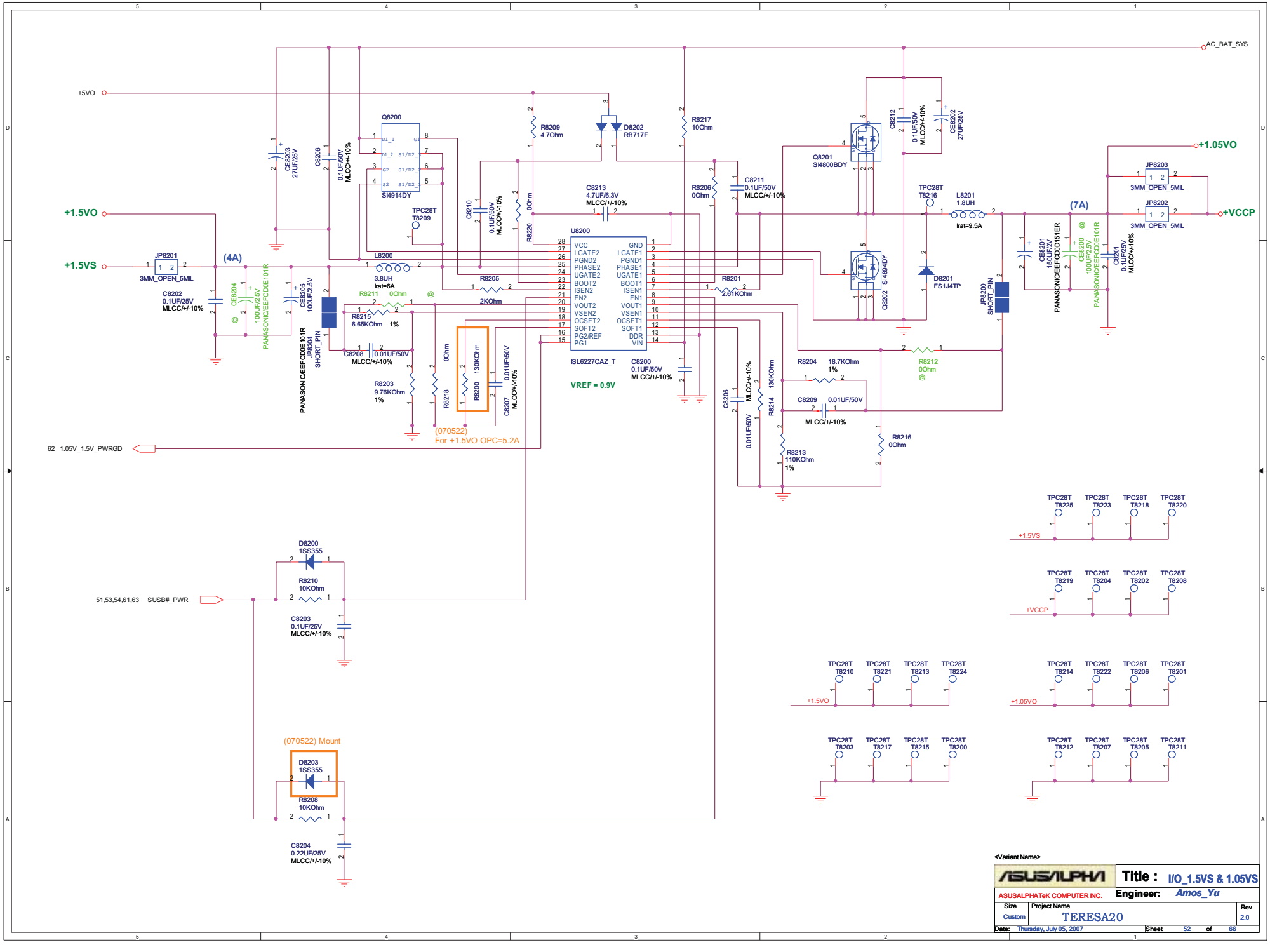
AC_BAT_SYS
+5VO
+1.5VO
+1.5VS
+1.05VO
+VCCP
Q8200
SI4914DY
TPC28T
T8209
CE8203
27UF/25V
C8206
0.1UF/50V
MLCC/+/-10%
R8209
4.7Ohm
D8202
RB717F
R8217
10Ohm
C8212
0.1UF/50V
MLCC/+/-10%
CE8202
27UF/25V
Q8201
SI4800BDY
C8210
0.1UF/50V
MLCC/+/-10%
R8220
0Ohm
C8213
4.7UF/6.3V
MLCC/+/-10%
R8206
0Ohm
C8211
0.1UF/50V
MLCC/+/-10%
TPC28T
T8216
L8201
1.8UH
Irat=9.5A
(7A)
JP8203
3MM_OPEN_5MIL
JP8202
3MM_OPEN_5MIL
JP8201
3MM_OPEN_5MIL
(4A)
C8202
0.1UF/25V
MLCC/+/-10%
CE8204
100UF/2.5V
PANASONICEEFCD0E101R
CE8205
100UF/2.5V
JP8204
SHORT_PIN
L8200
3.8UH
Irat=6A
R8211
0Ohm
R8205
2KOhm
U8200
VCC
LGATE2
PGND2
PHASE2
UGATE2
BOOT2
ISEN2
EN2
VOUT2
VSEN2
OCSET2
SOFT2
PG2/REF
PG1
GND
LGATE1
PGND1
PHASE1
UGATE1
BOOT1
ISEN1
EN1
VOUT1
VSEN1
OCSET1
SOFT1
DDR
VIN
ISL6227CAZ_T
VREF = 0.9V
R8201
2.61KOhm
Q8202
SI4884DY
D8201
FS1J4TP
JP8200
SHORT_PIN
CE8201
150UF/20V
PANASONICEEFCD0D151ER
CE8200
100UF/2.5V
PANASONICEEFCD0E101R
C8201
0.1UF/25V
MLCC/+/-10%
R8215
6.65KOhm
1%
C8208
0.01UF/50V
MLCC/+/-10%
R8203
9.76KOhm
1%
R8218
0Ohm
R8200
130KOhm
C8207
0.01UF/50V
MLCC/+/-10%
(070522)
For +1.5VO OPC=5.2A
C8200
0.1UF/50V
MLCC/+/-10%
C8205
0.01UF/50V
MLCC/+/-10%
R8214
130KOhm
R8204
18.7KOhm
1%
C8209
0.01UF/50V
MLCC/+/-10%
R8213
110KOhm
1%
R8212
0Ohm
R8216
0Ohm
62 1.05V_1.5V_PWRGD
D8200
1SS355
R8210
10KOhm
51,53,54,61,63 SUSB#_PWR
C8203
0.1UF/25V
MLCC/+/-10%
(070522) Mount
D8203
1SS355
R8208
10KOhm
C8204
0.22UF/25V
MLCC/+/-10%
TPC28T
T8225
T8223
T8218
T8220
+1.5VS
TPC28T
T8219
T8204
T8202
T8208
+VCCP
TPC28T
T8210
T8221
T8213
T8224
+1.5VO
TPC28T
T8214
T8222
T8206
T8201
+1.05VO
TPC28T
T8203
T8217
T8215
T8200
TPC28T
T8212
T8207
T8205
T8211
<Variant Name>
ASUSALPHA
Title : I/O_1.5VS & 1.05VS
ASUSALPHATeK COMPUTER INC.
Engineer: Amos_Yu
Size
Custom
Project Name
TERESA20
Rev
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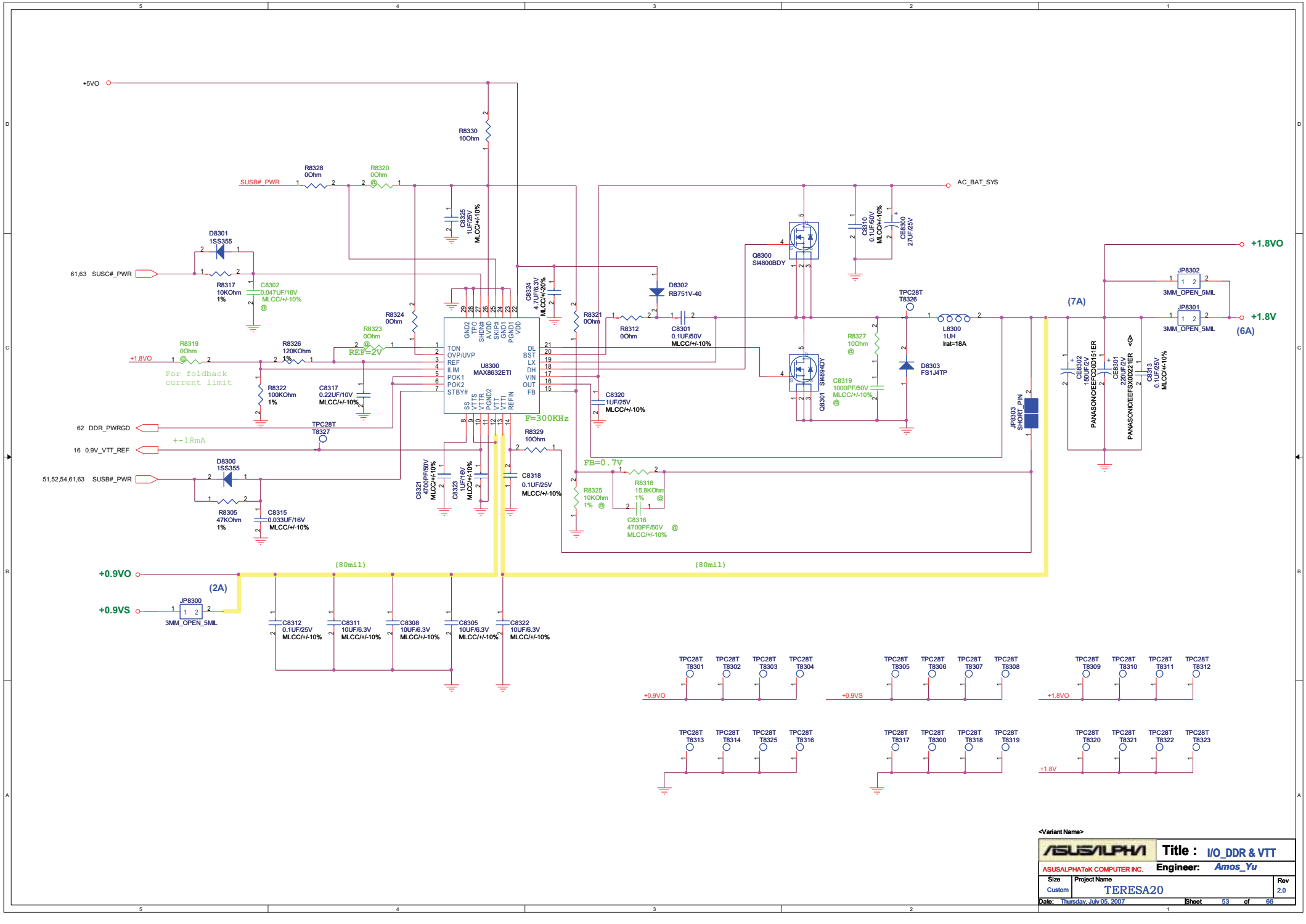
+5VO
R8330 10Ohm
R8328 0Ohm
R8320 0Ohm
SUSB# PWR
C8325 1UF/25V MLCC/+/-10%
AC_BAT_SYS
D8301 1SS355
61,63 SUSC#_PWR
R8317 10KOhm 1%
C8302 0.047UF/16V MLCC/+/-10%
C8324 4.7UF/6.3V MLCC/+/-20%
D8302 RB751V-40
Q8300 SI4800BDY
C8310 0.1UF/50V MLCC/+/-10%
CE8300 27UF/25V
+1.8VO
JP8302 3MM_OPEN_5MIL
JP8301 3MM_OPEN_5MIL
+1.8V
(6A)
(7A)
TPC28T T8326
L8300 1UH Iral=18A
R8324 0Ohm
R8323 0Ohm
REF=2V
R8321 0Ohm
R8312 0Ohm
C8301 0.1UF/50V MLCC/+/-10%
R8327 10Ohm
D8303 FS1J4TP
R8319 0Ohm
R8326 120KOhm 1%
+1.8VO
For foldback current limit
U8300 MAX8632ETI
GND2 TPO SHDN# AVDD SKIP# GND1 PGND1 VDD
TON OVP/UVP REF ILIM POK1 POK2 STBY#
DL BST LX DH VIN OUT FB
SS VSTS VTTR PGND2 VTT VTTI REFIN
R8322 100KOhm 1%
C8317 0.22UF/10V MLCC/+/-10%
Q8301 SI4894DY
C8319 1000PF/50V MLCC/+/-10% @
C8320 1UF/25V MLCC/+/-10%
JP8303 SHORT_PIN
CE8302 150UF/20V PANASONIC/EEFCD0D151ER
CE8301 220UF/2V PANASONIC/EEFSX0D221ER
C8313 0.1UF/25V MLCC/+/-10%
62 DDR_PWRGD
TPC28T T8327
F=300KHz
R8329 10Ohm
16 0.9V_VTT_REF
+-18mA
D8300 1SS355
51,52,54,61,63 SUSB#_PWR
C8321 4700PF/50V MLCC/+/-10%
C8323 1UF/16V MLCC/+/-10%
C8318 0.1UF/25V MLCC/+/-10%
FB=0.7V
R8325 10KOhm 1% @
R8318 15.8KOhm 1% @
C8316 4700PF/50V MLCC/+/-10% @
R8305 47KOhm 1%
C8315 0.033UF/16V MLCC/+/-10%
(80mil)
(80mil)
+0.9VO
(2A)
+0.9VS
JP8300 3MM_OPEN_5MIL
C8312 0.1UF/25V MLCC/+/-10%
C8311 10UF/6.3V MLCC/+/-10%
C8308 10UF/6.3V MLCC/+/-10%
C8305 10UF/6.3V MLCC/+/-10%
C8322 10UF/6.3V MLCC/+/-10%
TPC28T T8301 T8302 T8303 T8304
+0.9VO
TPC28T T8305 T8306 T8307 T8308
+0.9VS
TPC28T T8309 T8310 T8311 T8312
+1.8VO
TPC28T T8313 T8314 T8325 T8316
TPC28T T8317 T8300 T8318 T8319
TPC28T T8320 T8321 T8322 T8323
+1.8V
<Variant Name>
ASUSALPHA
Title : I/O_DDR & VTT
ASUSALPHATeK COMPUTER INC.
Engineer: Amos_Yu
Size Custom
Project Name TERESA20
Rev 2.0
Date: Thursday, July 05, 2007
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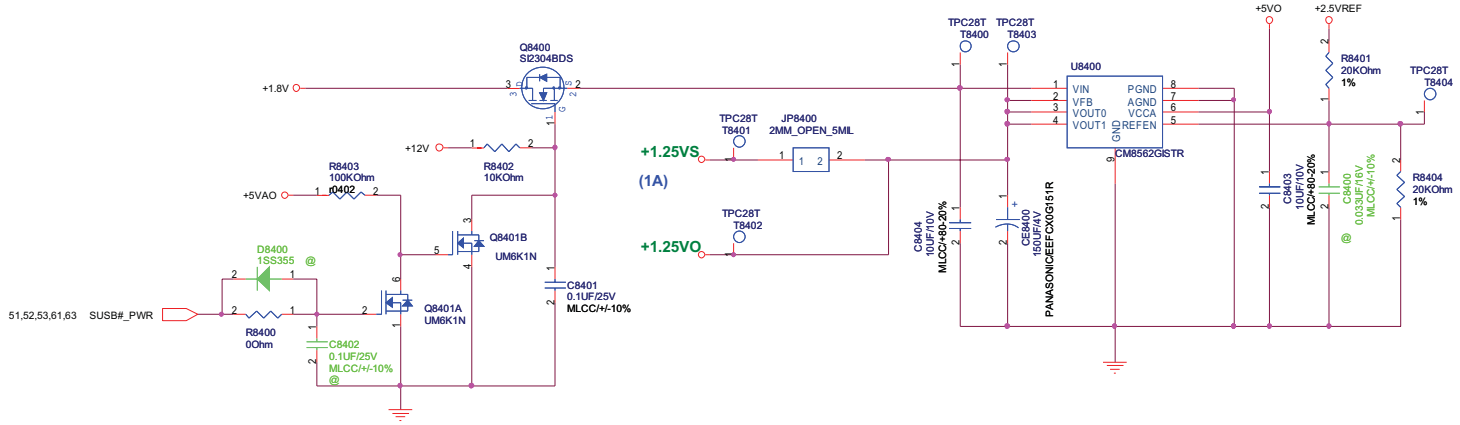
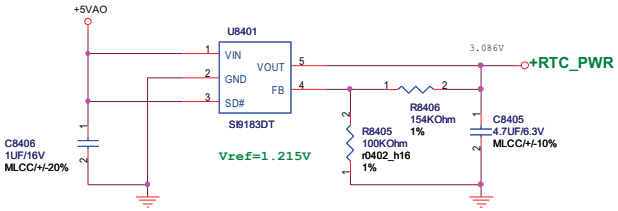
+1.25VS



+RTC_PWR



<Variant Name>

ASUSALPHA	Title :	POWER_I/O_1.25VS & RTC_PWR
ASUSALPHATeK COMPUTER INC.	Engineer:	Amos_Yu
Size: Custom	Project Name: TERESA20	Rev: 2.0
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<Variant Name>

ASUSALPHA	Title : POWER_Empty	
ASUSALPHATeK COMPUTER INC.	Engineer: Amos_Yu	
Size: C	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 55 of 66	

<Variant Name>

ASUSALPHA	Title : POWER_Empty
ASUSALPHATeK COMPUTER INC.	Engineer: Amos_Yu

Size	Project Name	Rev
B	TERESA20	2.0

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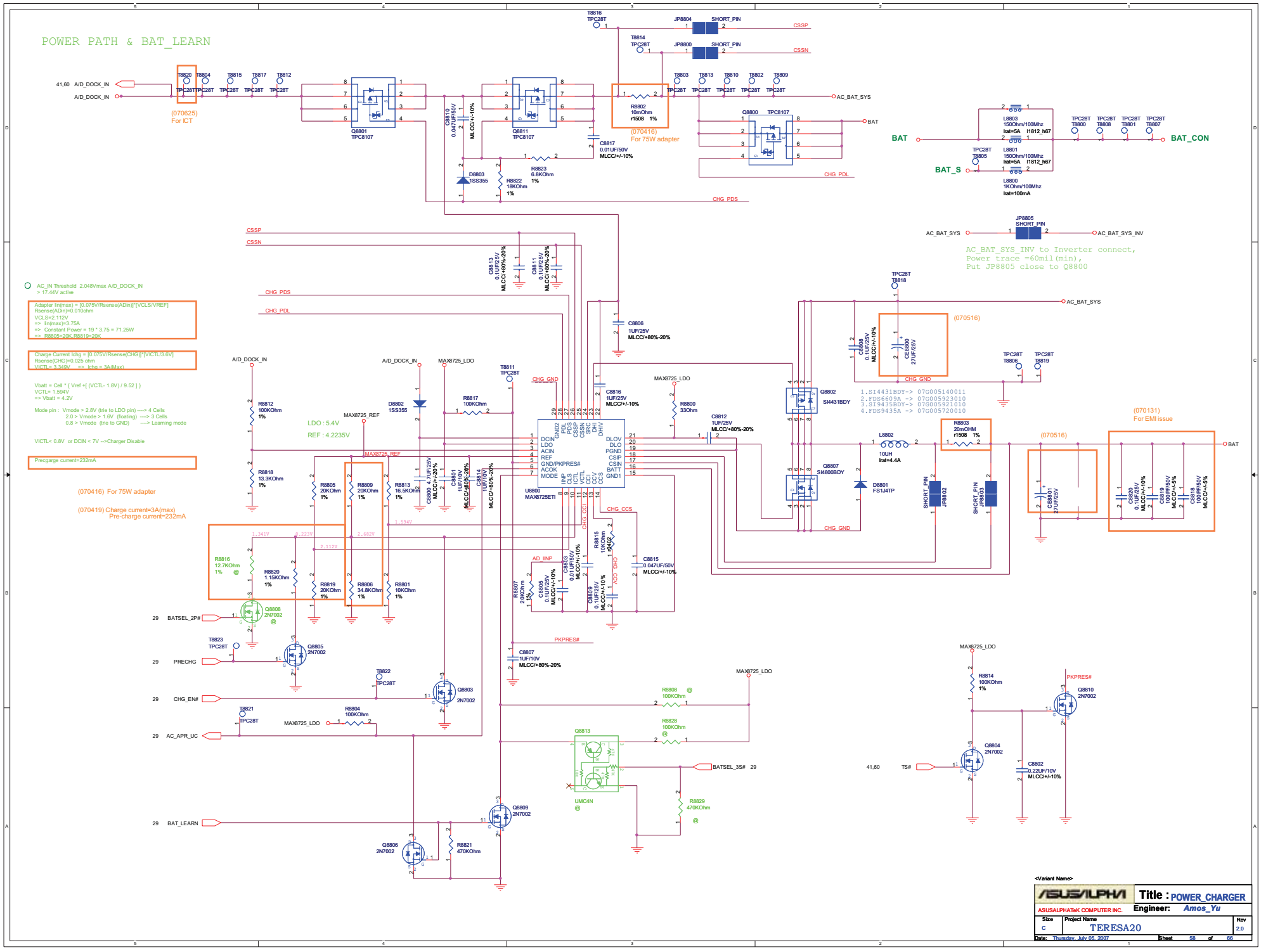
R1.1 to R1.2

Page	Action
81	To modify +5VO output voltage, modify R8134 to 49.9K Ohm,
81	To modify +5VO and +3VO OCP, un-mount C8128, C8129 and modify R8120, R8133 to 18K Ohm
82	To modify +1.5VO OCP, modify R8200 to 130K Ohm
82	To modify +1.05VO Disable timing, mount D8203
88	Modify component, CE8800, CE8801
91	To modify +3VS timing, modify R9108 to 20K Ohm

<Variant Name>

ASUSALPHA	Title : POWER_Empty	
ASUSALPHATeK COMPUTER INC.	Engineer: Amos_Yu	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 57 of 66	


POWER PATH & BAT_LEARN
41,60 A/D_DOCK_IN
A/D_DOCK_IN
(070625)
For ICT
Q8801
TPC8107
Q8811
TPC8107
R8802
10mOhm
r1508 1%
(070416)
For 75W adapter
AC_BAT_SYS
BAT
Q8800 TPC8107
CHG_PDL
CHG_PDS
D8803
1SS355
R8822
18KOhm
1%
R8823
6.8KOhm
1%
C8817
0.01UF/50V
MLCC/+/-10%
CSSP
CSSN
C8813
0.1UF/25V
MLCC/+80%-20%
C8811
0.1UF/25V
MLCC/+80%-20%
C8806
1UF/25V
MLCC/+80%-20%
AC_IN Threshold 2.048Vmax A/D_DOCK_IN
> 17.44V active
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.010ohm
VCLS=2.112V
=> Iin(max)=3.75A
=> Constant Power = 19 * 3.75 = 71.25W
=> R8805=20K,R8819=20K
Charge Current Ichg = [0.075V/Rsense(CHG)]*[VCTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3.348V => Ichg = 3A(Max)
Vbatt = Cell * { Vref +[(VCTL- 1.8V) / 9.52] }
VCTL= 1.594V
=> Vbatt = 4.2V
Mode pin : Vmode > 2.8V (trie to LDO pin) ---> 4 Cells
2.0 > Vmode > 1.6V (floating) ---> 3 Cells
0.8 > Vmode (trie to GND) ---> Learning mode
VICTL< 0.8V or DCIN < 7V -->Charger Disable
Precgarge current=232mA
(070416) For 75W adapter
(070419) Charge current=3A(max)
Pre-charge current=232mA
A/D_DOCK_IN
MAX8725_LDO
MAX8725_REF
LDO : 5.4V
REF : 4.2235V
R8812
100KOhm
1%
R8818
13.3KOhm
1%
D8802
1SS355
R8817
100KOhm
R8800
33Ohm
C8812
1UF/25V
MLCC/+80%-20%
C8816
1UF/25V
MLCC/+/-10%
U8800
MAX8725ETI
DCIN
LDO
ACIN
REF
GND/PKPRES#
ACOK
MODE
DLOV
DLO
PGND
CSIP
CSIN
BATT
GND1
R8805
20KOhm
1%
R8809
20KOhm
1%
R8813
16.5KOhm
1%
C8800 4.7UF/25V
MLCC/+/-20%
C8801
1UF/10V
MLCC/+80%-20%
C8814
1UF/10V
MLCC/+80%-20%
R8816
12.7KOhm
1% @
R8820
1.15KOhm
1%
R8819
20KOhm
1%
R8806
34.8KOhm
1%
R8801
10KOhm
1%
CHG_CCS
R8815
100KOhm
1%
C8815
0.047UF/50V
MLCC/+/-10%
AD_IINP
C8805
0.1UF/25V
MLCC/+/-10%
C8803
0.01UF/50V
MLCC/+/-10%
C8809
0.1UF/25V
MLCC/+/-10%
R8807
20KOhm
1%
PKPRES#
C8807
1UF/10V
MLCC/+80%-20%
29 BATSEL_2P#
Q8808
2N7002
@
T8823
TPC28T
Q8805
2N7002
29 PRECHG
T8822
TPC28T
Q8803
2N7002
29 CHG_EN#
T8821
TPC28T
R8804
100KOhm
29 AC_APR_UC
Q8806
2N7002
R8821
470KOhm
Q8809
2N7002
29 BAT_LEARN
R8808
100KOhm
@
R8828
100KOhm
@
Q8813
UMC4N
@
BATSEL_3S# 29
R8829
470KOhm
@
JP8805
SHORT_PIN
AC_BAT_SYS_INV
AC_BAT_SYS_INV to Inverter connect,
Power trace =60mil(min),
Put JP8805 close to Q8800
(070516)
C8808
0.1UF/25V
MLCC/+/-10%
CE8800
270UF/25V
Q8802
SI4431BDY
Q8807
SI4800BDY
1.SI4431BDY-> 07G005140011
2.FDS6609A -> 07G005923010
3.SI9435BDY-> 07G005921010
4.FDS9435A -> 07G005720010
L8802
10UH
Irat=4.4A
R8803
20mOHM
r1508 1%
D8801
FS1J4TP
SHORT_PIN
JP8802
SHORT_PIN
JP8803
(070131)
For EMI issue
C8820
0.1UF/25V
MLCC/+/-10%
C8819
100PF/50V
MLCC/+/-5%
C8818
100PF/50V
MLCC/+/-5%
C8801
270UF/25V
R8814
100KOhm
1%
Q8810
2N7002
41,60 TS#
Q8804
2N7002
C8802
0.22UF/10V
MLCC/+/-10%
BAT
BAT_S
BAT_CON
L8803
150Ohm/100Mhz
Irat=5A I1812_h67
L8801
150Ohm/100Mhz
Irat=5A I1812_h67
L8800
1KOhm/100Mhz
Irat=100mA
T8816
TPC28T
JP8804
SHORT_PIN
T8814
TPC28T
JP8800
SHORT_PIN
T8820
T8804
T8815
T8817
T8812
T8803
T8813
T8810
T8802
T8809
T8811
TPC28T
T8818
TPC28T
T8806
T8819
T8800
T8808
T8801
T8807
T8805
<Variant Name>
ASUSALPHATeK COMPUTER INC.
Title : POWER_CHARGER
Engineer: Amos_Yu
Size C
Project Name TERESA20
Rev 2.0
Date: Thursday, July 05, 2007
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<Variant Name>

ASUSALPHA	Title : POWER_Empty	
ASUSALPHATeK COMPUTER INC.	Engineer: Amos_Yu	
Size: Custom	Project Name: TERESA20	Rev: 2.0
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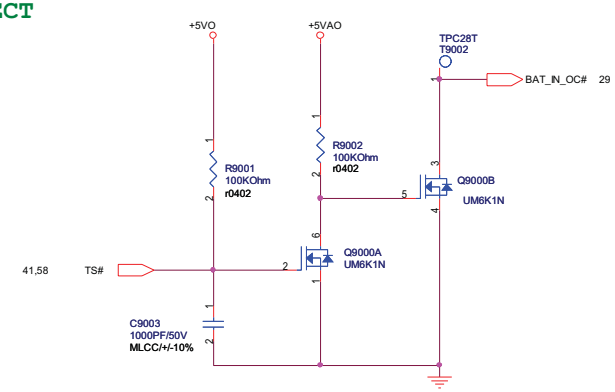
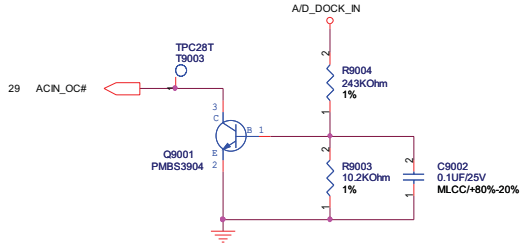
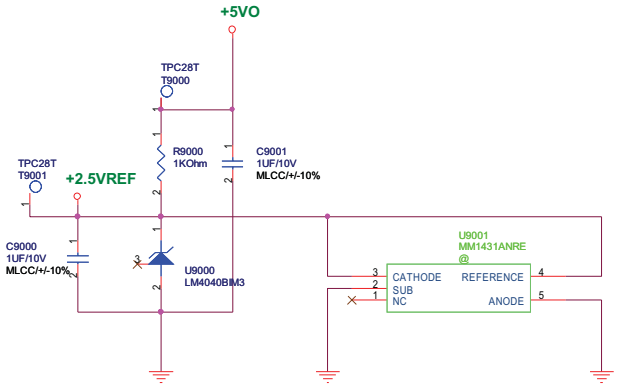
BATTERY IN DETECT



ADAPTER IN DETECT



+2.5VREF



U9000 & U9001 colay

<Variant Name>

ASUSALPHA	Title : POWER_DETECT	
ASUSALPHATeK COMPUTER INC.	Engineer: Amos_Yu	
Size: Custom	Project Name: TERESA20	Rev: 2.0
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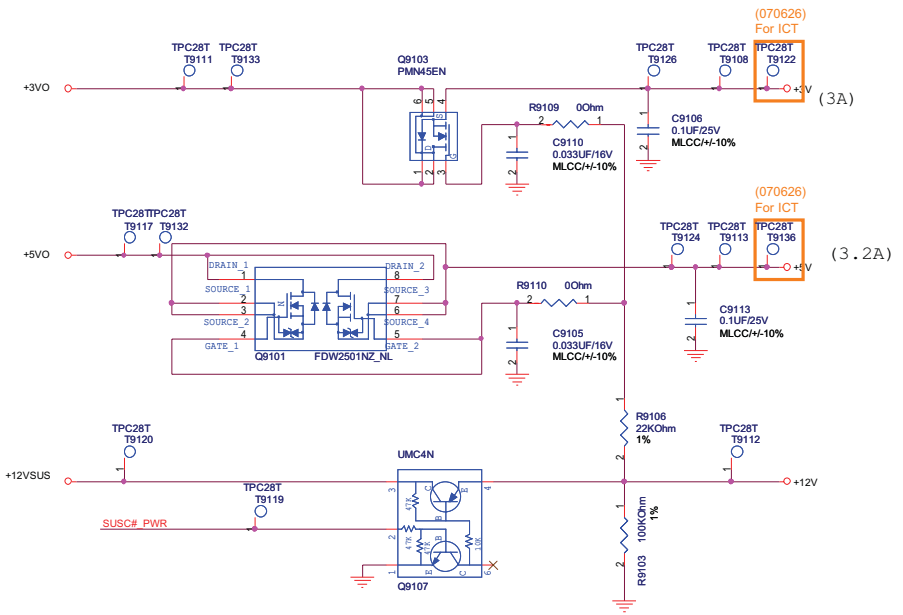
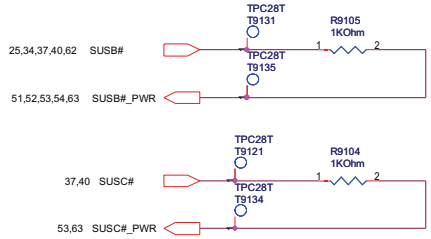
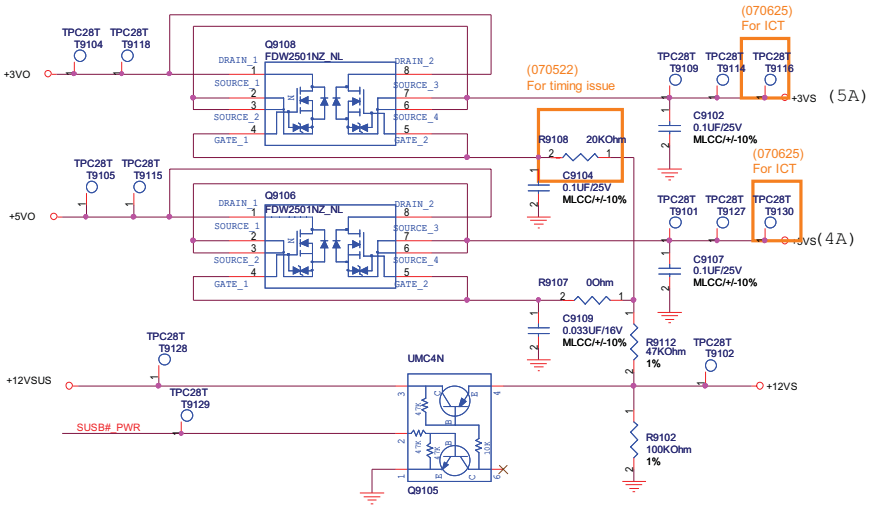
SUSC#_PWR POWER





SUSB#_PWR POWER



<Variant Name>

ASUSALPHA	Title : LOAD SWITCH	
ASUSALPHATeK COMPUTER INC.	Engineer: Amos_Yu	
Size: Custom	Project Name: TERESA20	Rev: 2.0
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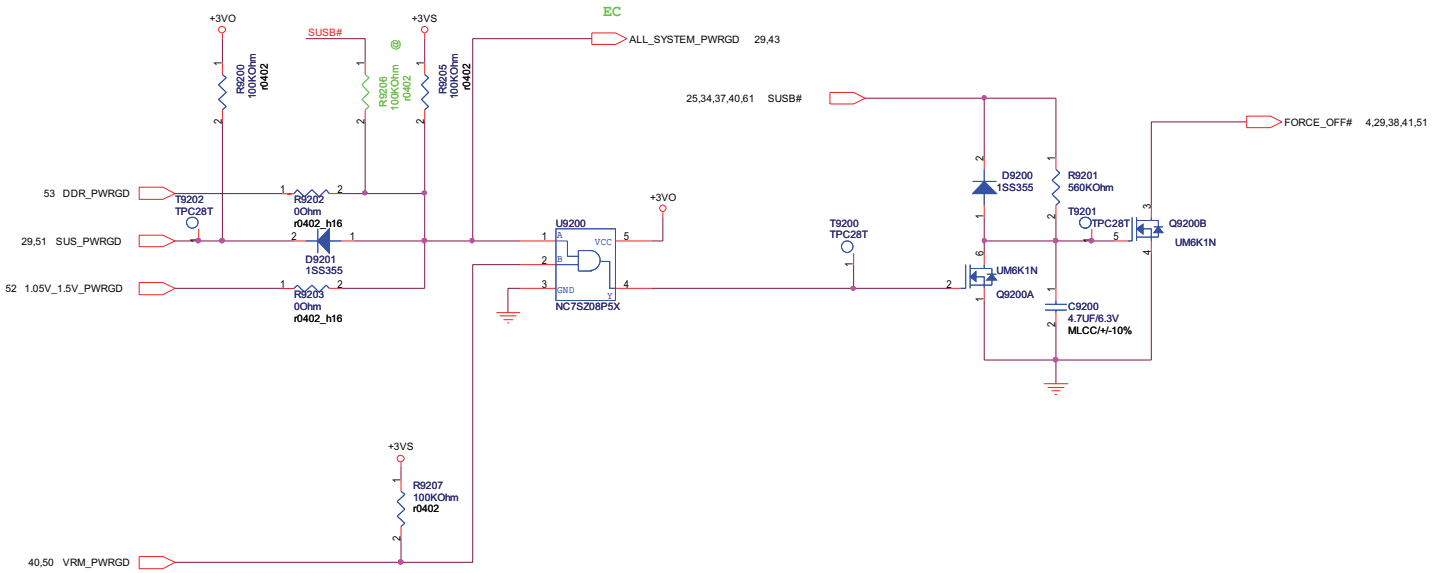
POWER GOOD DETECTER



<Variant Name>

ASUSALPHA	Title : POWER_PROTECT	
ASUSALPHATeK COMPUTER INC.	Engineer: Amos_Yu	
Size: Custom	Project Name: TERESA20	Rev: 2.0
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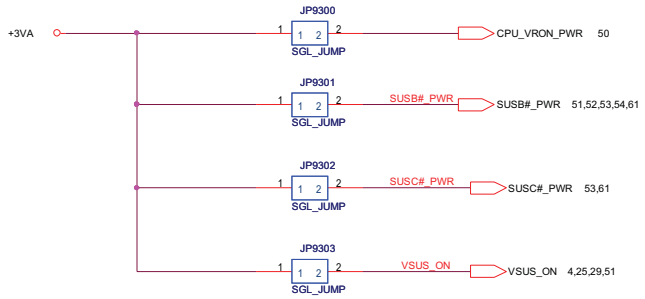
AC_BAT_SYS	AC_BAT_SYS	41,50,51,52,53,58
BAT	BAT	58
BAT_CON	BAT_CON	41,58
+2.5VREF	+2.5VREF	54,60
+3VA	+3VA	4,12,19,29,37,38,41,51
+5VAO	+5VAO	51,54,60
+5VO	+5VO	51,52,53,54,60,61
+5VSUS	+5VSUS	20,30,36,51
+5V	+5V	10,16,30,36,37,44,61
+5VS	+5VS	4,13,19,20,21,22,28,29,30,34,37,38,50,61
+3VO	+3VO	51,61,62
+3VSUS	+3VSUS	18,19,20,22,25,29,34,40,51
+3V	+3V	12,18,19,26,35,37,43,44,61
+3VS	+3VS	2,4,5,7,10,11,12,13,14,15,19,20,21,22,25,26,27,28,29,30,33,37,43,50,61,62
+12VSUS	+12VSUS	51,61
+12V	+12V	22,37,54,61
+12VS	+12VS	12,13,33,37,61
+1.8VO	+1.8VO	53
+1.8V	+1.8V	7,9,10,14,15,16,37,53,54
+0.9VS	+0.9VS	16,37,53
+0.9VO	+0.9VO	53
+1.05VO	+1.05VO	50,52
+VCCP	+VCCP	3,5,6,7,9,10,17,20,52
+1.5VO	+1.5VO	52
+1.5VS	+1.5VS	3,10,17,18,20,25,26,37,52
+VCORE	+VCORE	3,50
+1.25VS	+1.25VS	7,10,20,54

FOR POWER TEST



<Variant Name>

ASUSALPHA	Title : POWER_SIGNAL	
ASUSALPHATeK COMPUTER INC.	Engineer: Amos_Yu	
Size: Custom	Project Name: TERESA20	Rev: 2.0
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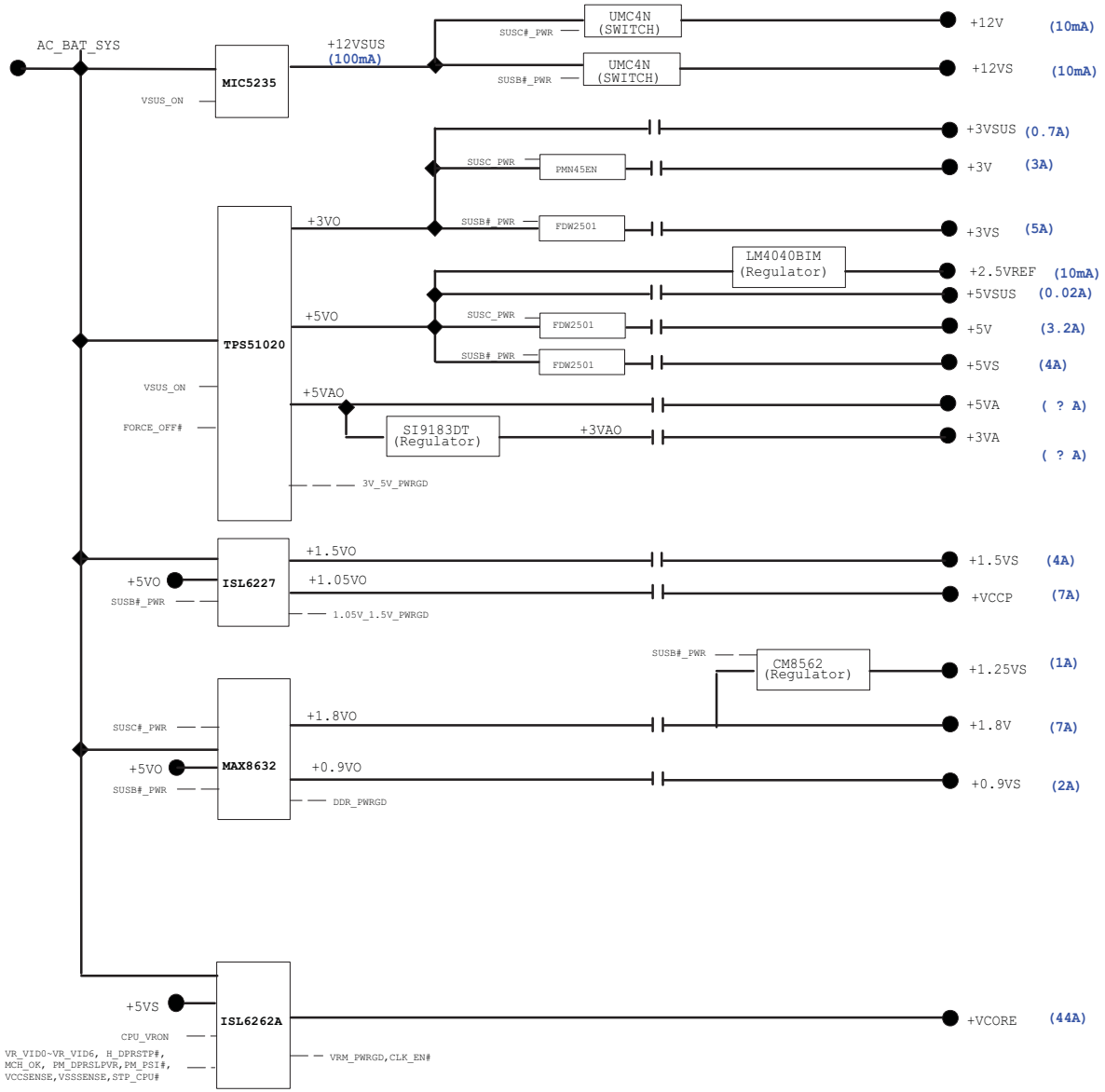

<Variant Name>

ASUSALPHATeK COMPUTER INC.

Title : POWER_FLOW

Engineer: Amos_Yu

Size	Project Name	Rev
Custom	TERESA20	2.0

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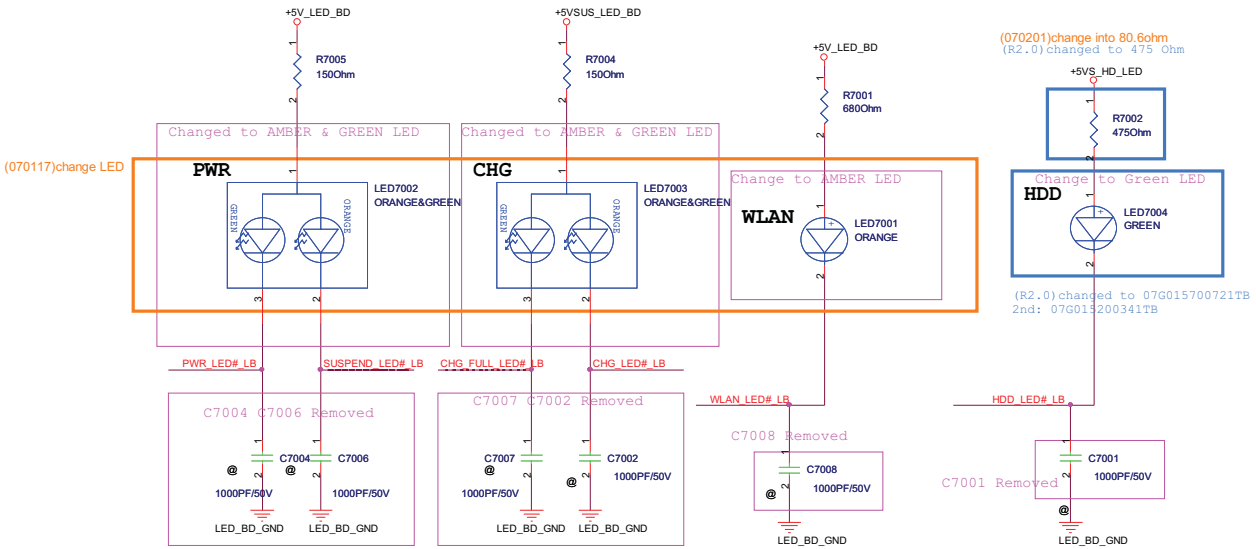
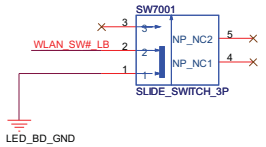
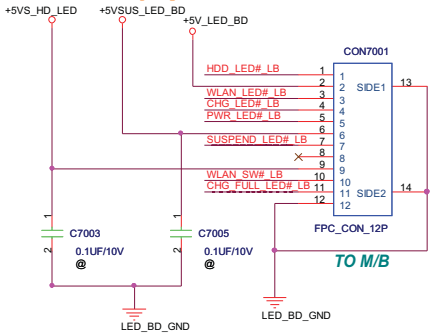
LEFT & RIGHT Button remove to TP BOARD



New added SW for Teresa

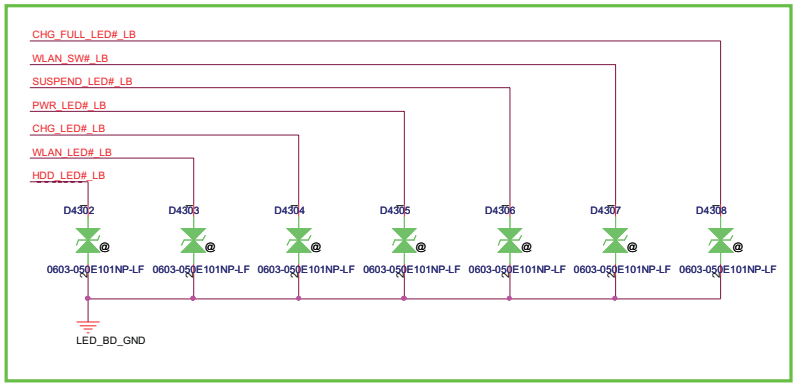


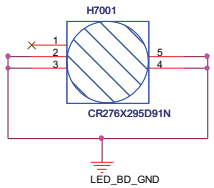
070115 Change pin define



CON to T/P remove to TP BOARD

IR receive module removed





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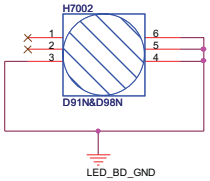

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ASUSALPHA	Title : LED Board	
ASUSALPHATeK COMPUTER INC.	Engineer: Potter_Huang	
Size: Custom	Project Name: TERESA20	Rev: 2.0
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TERESA20 SCHEMATIC V2.0

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DAUGHTER BOARD

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NC

ASUSALPHA	Title : Content & History	
ASUSALPHATeK COMPUTER INC.	Engineer: IVERSON QIU	
Size: Custom	Project Name: TERESA20	Rev: 2.0
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