LCFC Confidential

DY512 M/B Schematics Document

Intel Kabylake H-Processor with DDR4 + NV N17P-G0/G1 GPU

MB NM-B191

2016-11-25

REV:1.0

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: Cover Page		
Size: Custom	Document Number: DY512	Rev: 1.0
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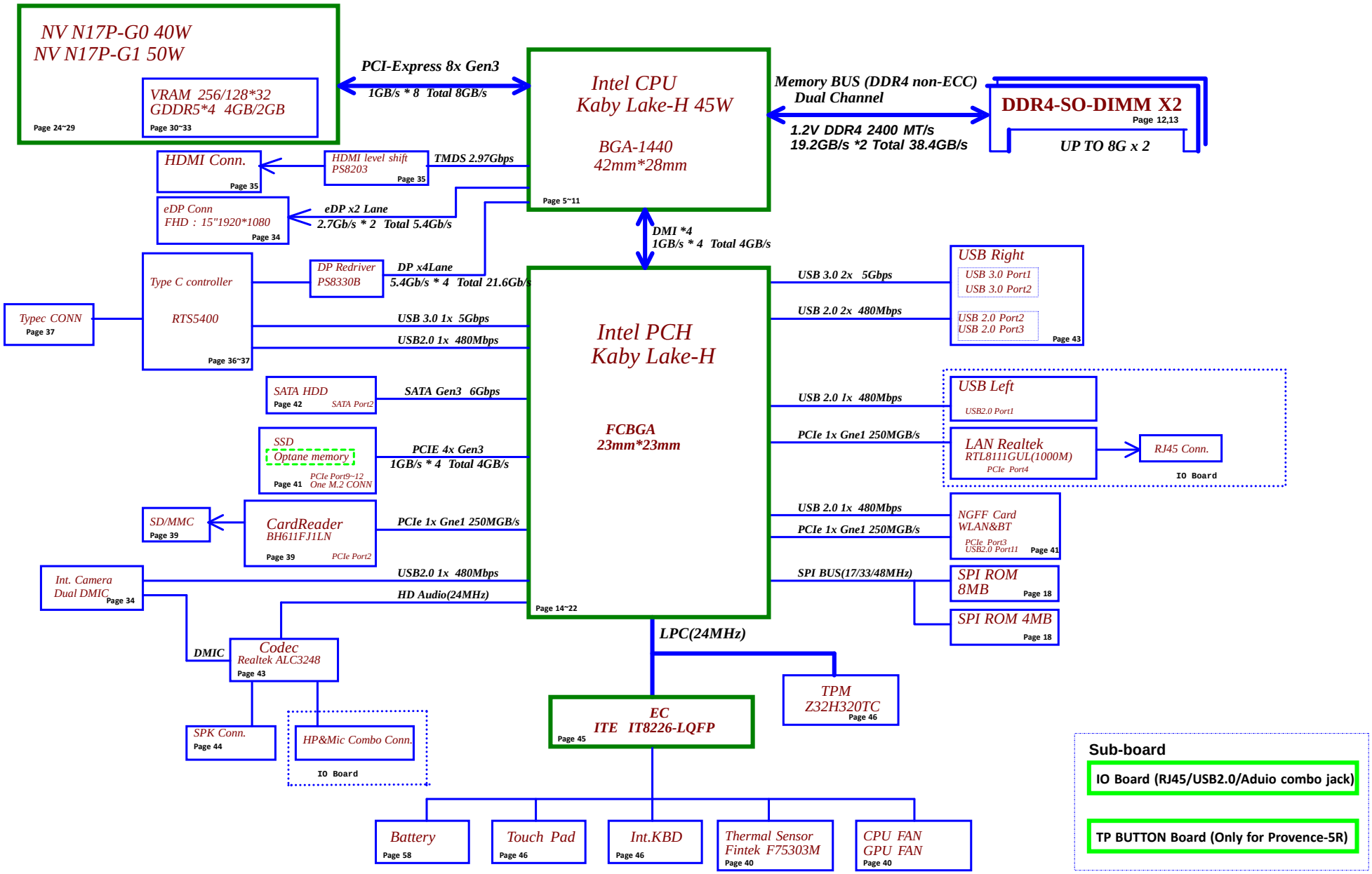

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Title	Block Diagram		
Size C	Document Number DY512		Rev 1.0
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW +1.0VALW	+3VALW_PCH	+2.5V +1.2V VCCST	+5VS +3VS VCCIO VCCSTG +0.6VS CPU_CORE GFX_VCCSA +1.8V_AON +1.8V_MAIN NVVDD NVVDDS +0.95VGS +1.35VGS
S0	0	0	0	0	0
S3	0	0	0	0	X
S3 Battery only	0	0	0	0	X
S5 S4/AC Only	0	0	0	X	X
S5 S4 Battery only	0	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB2.0 Port table

Port	Function
1	Right USB2
2	Left USB3
3	Left USB3
4	TypeC USB2
5	
6	Camera
7	
8	
9	
10	
11	BT
12	
13	
14	

HSIO port Table

Port	Description	Function
1	USB3#1	Left USB3
2	USB3#2	Left USB3
3	USB3#3	TypeC USB3
4	USB3#4	
5	USB3#5	
6	USB3#6	
7	USB3#7 / PCIE#1	
8	USB3#8 / PCIE#2	CarderReader(PCIE)
9	USB3#9 / PCIE#3	WLAN(PCIE)
10	USB3#10 / PCIE#4	LAN(PCIE)
11	PCIE#5	
12	PCIE#6	
13	PCIE#7	
14	PCIE#8	
15	PCIE#9 / SATA#0	PCIe x4 SSD
16	PCIE#10 / SATA#1	
17	PCIE#11	
18	PCIE#12	
19	PCIE#13 / SATA#0	
20	PCIE#14 / SATA#1	
21	PCIE#15 / SATA#2	HDD(SATA3.0)
22	PCIE#16 / SATA#3	HDD cable(SATA3.0) Reserved
23	PCIE#17 / SATA#4	
24	PCIE#18 / SATA#5	
25	PCIE#19 / SATA#6	
26	PCIE#20 / SATA#6	

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
ME@	ME part(connector, hole)
TPM@	For support TPM sku part
CD@	Cost down part
EMC@	EMC part stuff
EMC_NS@	EMC part Not stuff
RF@	RF part stuff
RF_NS@	RF part Not stuff
OPT@	For GPU part
N16@	For N16 GPU part
N17@	For N17 GPU part

Title: **Notes List**

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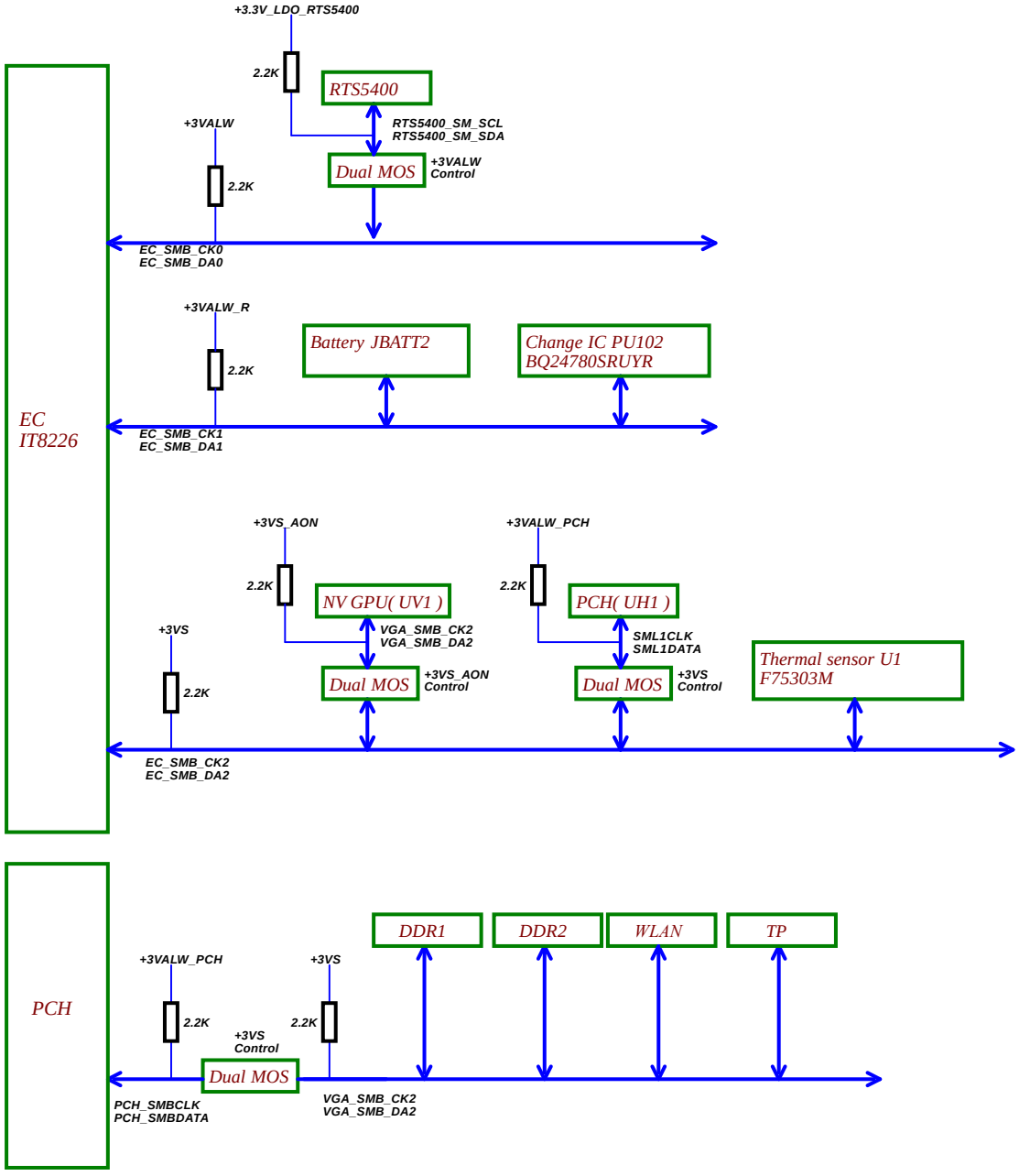

SMBUS Control Table

	SOURCE	VGA	BATT	IT8586E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1 EC_SMB_DA1	IT8226 +3VALW	X	V	V +3VALW	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	IT8226 +3VS	V +3VGS	X	V +3VS	X	X	V +3VS	V +3VALW_PCH	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X

EC SM Bus1 address

Device	
Smart Battery	0X16
Charger	0001 0010 b

EC SM Bus2 address

Device	Address
Thermal Sensor F75303M	1001_100xb
VGA	0x41(default)
PCH	need to update
RTS5400	0xD4

PCH SM Bus address

Device	Address
DDR DIMMA	1010 000Xb
DDR DIMMB	1010 010Xb
WLAN	Rsvd

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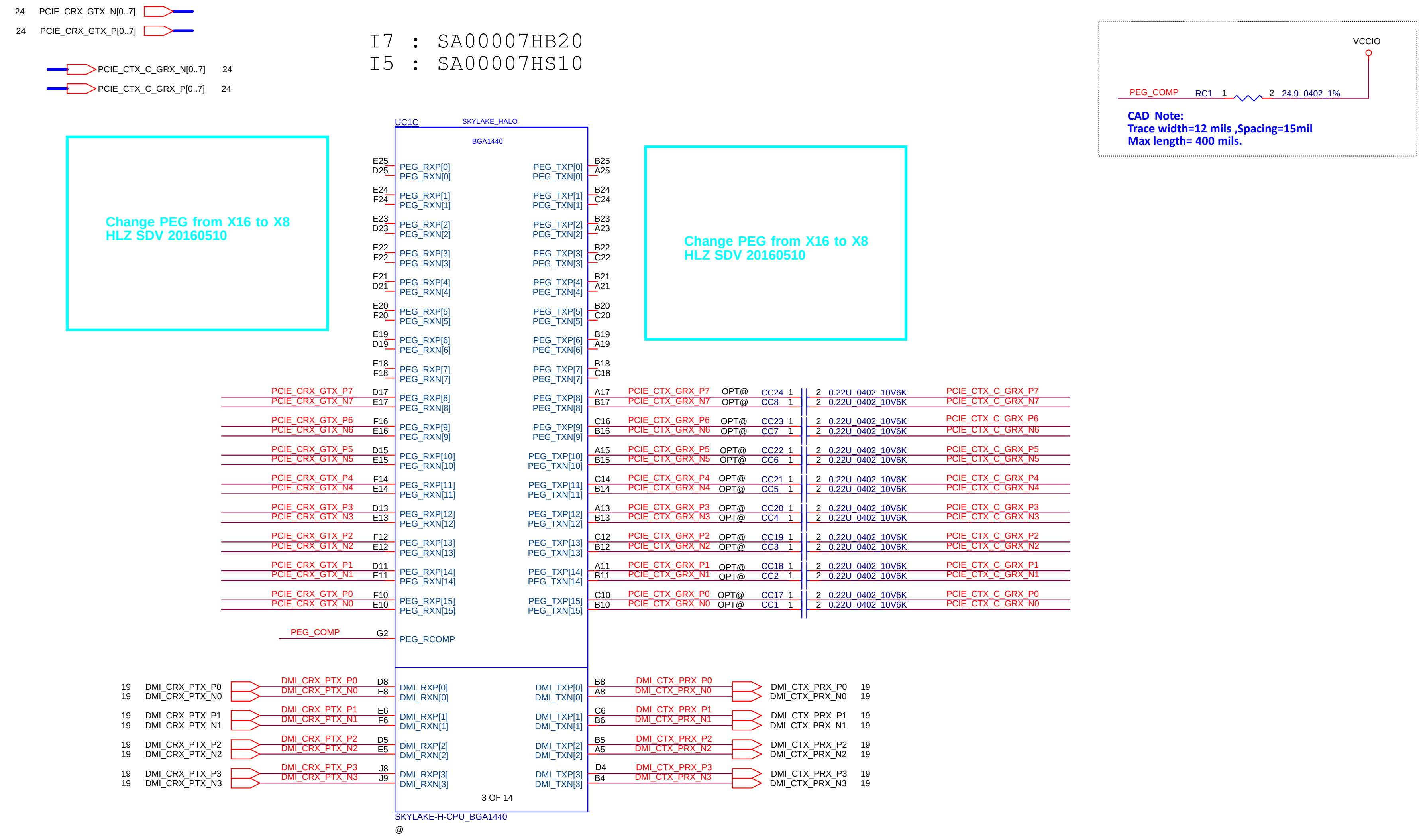
24 PCIE_CRX_GTX_N[0..7]
24 PCIE_CRX_GTX_P[0..7]
PCIE_CTX_C_GRX_N[0..7] 24
PCIE_CTX_C_GRX_P[0..7] 24
I7 : SA00007HB20
I5 : SA00007HS10
Change PEG from X16 to X8
HLZ SDV 20160510
Change PEG from X16 to X8
HLZ SDV 20160510
VCCIO
PEG_COMP RC1 1 2 24.9_0402_1%
CAD Note:
Trace width=12 mils ,Spacing=15mil
Max length= 400 mils.
UC1C SKYLAKE_HALO
BGA1440
E25 PEG_RXP[0] PEG_TXP[0] B25
D25 PEG_RXN[0] PEG_TXN[0] A25
E24 PEG_RXP[1] PEG_TXP[1] B24
F24 PEG_RXN[1] PEG_TXN[1] C24
E23 PEG_RXP[2] PEG_TXP[2] B23
D23 PEG_RXN[2] PEG_TXN[2] A23
E22 PEG_RXP[3] PEG_TXP[3] B22
F22 PEG_RXN[3] PEG_TXN[3] C22
E21 PEG_RXP[4] PEG_TXP[4] B21
D21 PEG_RXN[4] PEG_TXN[4] A21
E20 PEG_RXP[5] PEG_TXP[5] B20
F20 PEG_RXN[5] PEG_TXN[5] C20
E19 PEG_RXP[6] PEG_TXP[6] B19
D19 PEG_RXN[6] PEG_TXN[6] A19
E18 PEG_RXP[7] PEG_TXP[7] B18
F18 PEG_RXN[7] PEG_TXN[7] C18
PCIE_CRX_GTX_P7 D17 PEG_RXP[8] PEG_TXP[8] A17 PCIE_CTX_GRX_P7 OPT@ CC24 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_P7
PCIE_CRX_GTX_N7 E17 PEG_RXN[8] PEG_TXN[8] B17 PCIE_CTX_GRX_N7 OPT@ CC8 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_N7
PCIE_CRX_GTX_P6 F16 PEG_RXP[9] PEG_TXP[9] C16 PCIE_CTX_GRX_P6 OPT@ CC23 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_P6
PCIE_CRX_GTX_N6 E16 PEG_RXN[9] PEG_TXN[9] B16 PCIE_CTX_GRX_N6 OPT@ CC7 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_N6
PCIE_CRX_GTX_P5 D15 PEG_RXP[10] PEG_TXP[10] A15 PCIE_CTX_GRX_P5 OPT@ CC22 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_P5
PCIE_CRX_GTX_N5 E15 PEG_RXN[10] PEG_TXN[10] B15 PCIE_CTX_GRX_N5 OPT@ CC6 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_N5
PCIE_CRX_GTX_P4 F14 PEG_RXP[11] PEG_TXP[11] C14 PCIE_CTX_GRX_P4 OPT@ CC21 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_P4
PCIE_CRX_GTX_N4 E14 PEG_RXN[11] PEG_TXN[11] B14 PCIE_CTX_GRX_N4 OPT@ CC5 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_N4
PCIE_CRX_GTX_P3 D13 PEG_RXP[12] PEG_TXP[12] A13 PCIE_CTX_GRX_P3 OPT@ CC20 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_P3
PCIE_CRX_GTX_N3 E13 PEG_RXN[12] PEG_TXN[12] B13 PCIE_CTX_GRX_N3 OPT@ CC4 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_N3
PCIE_CRX_GTX_P2 F12 PEG_RXP[13] PEG_TXP[13] C12 PCIE_CTX_GRX_P2 OPT@ CC19 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_P2
PCIE_CRX_GTX_N2 E12 PEG_RXN[13] PEG_TXN[13] B12 PCIE_CTX_GRX_N2 OPT@ CC3 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_N2
PCIE_CRX_GTX_P1 D11 PEG_RXP[14] PEG_TXP[14] A11 PCIE_CTX_GRX_P1 OPT@ CC18 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_P1
PCIE_CRX_GTX_N1 E11 PEG_RXN[14] PEG_TXN[14] B11 PCIE_CTX_GRX_N1 OPT@ CC2 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_N1
PCIE_CRX_GTX_P0 F10 PEG_RXP[15] PEG_TXP[15] C10 PCIE_CTX_GRX_P0 OPT@ CC17 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_P0
PCIE_CRX_GTX_N0 E10 PEG_RXN[15] PEG_TXN[15] B10 PCIE_CTX_GRX_N0 OPT@ CC1 1 2 0.22U_0402_10V6K PCIE_CTX_C_GRX_N0
PEG_COMP G2 PEG_RCOMP
19 DMI_CRX_PTX_P0 DMI_CRX_PTX_P0 D8 DMI_RXP[0] DMI_TXP[0] B8 DMI_CTX_PRX_P0 DMI_CTX_PRX_P0 19
19 DMI_CRX_PTX_N0 DMI_CRX_PTX_N0 E8 DMI_RXN[0] DMI_TXN[0] A8 DMI_CTX_PRX_N0 DMI_CTX_PRX_N0 19
19 DMI_CRX_PTX_P1 DMI_CRX_PTX_P1 E6 DMI_RXP[1] DMI_TXP[1] C6 DMI_CTX_PRX_P1 DMI_CTX_PRX_P1 19
19 DMI_CRX_PTX_N1 DMI_CRX_PTX_N1 F6 DMI_RXN[1] DMI_TXN[1] B6 DMI_CTX_PRX_N1 DMI_CTX_PRX_N1 19
19 DMI_CRX_PTX_P2 DMI_CRX_PTX_P2 D5 DMI_RXP[2] DMI_TXP[2] B5 DMI_CTX_PRX_P2 DMI_CTX_PRX_P2 19
19 DMI_CRX_PTX_N2 DMI_CRX_PTX_N2 E5 DMI_RXN[2] DMI_TXN[2] A5 DMI_CTX_PRX_N2 DMI_CTX_PRX_N2 19
19 DMI_CRX_PTX_P3 DMI_CRX_PTX_P3 J8 DMI_RXP[3] DMI_TXP[3] D4 DMI_CTX_PRX_P3 DMI_CTX_PRX_P3 19
19 DMI_CRX_PTX_N3 DMI_CRX_PTX_N3 J9 DMI_RXN[3] DMI_TXN[3] B4 DMI_CTX_PRX_N3 DMI_CTX_PRX_N3 19
3 OF 14
SKYLAKE-H-CPU_BGA1440
@

Security Classification	LC Future Center Secret Data			Title
Issued Date	2015/02/26	Deciphered Date	2016/02/26	CPU (1/7) DMI,PEG

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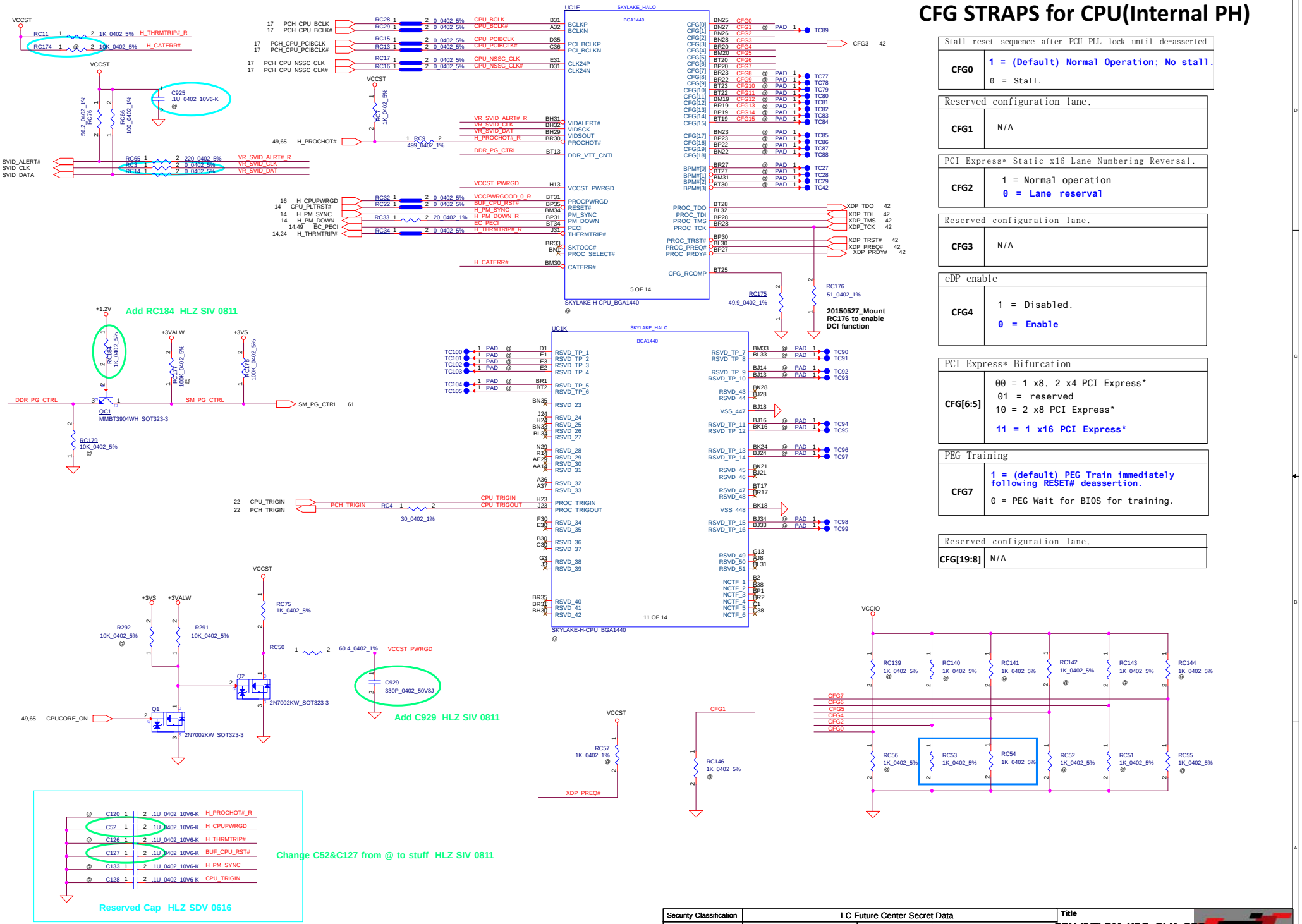
Date: Friday, November 25, 2016



CFG STRAPS for CPU(Internal PH)

Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	**1 = (Default) Normal Operation; No stall.** 0 = Stall.

Reserved configuration lane.	
CFG1	N/A

PCI Express* Static x16 Lane Numbering Reversal.	
CFG2	1 = Normal operation **0 = Lane reserval**

Reserved configuration lane.	
CFG3	N/A

eDP enable	
CFG4	1 = Disabled. **0 = Enable**

PCI Express* Bifurcation	
CFG[6:5]	00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* **11 = 1 x16 PCI Express***

PEG Training	
CFG7	**1 = (default) PEG Train immediately following RESET# deassertion.** 0 = PEG Wait for BIOS for training.

Reserved configuration lane.	
CFG[19:8]	N/A

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Title: CPU (2/7) PM, XDP, CLK, CFG

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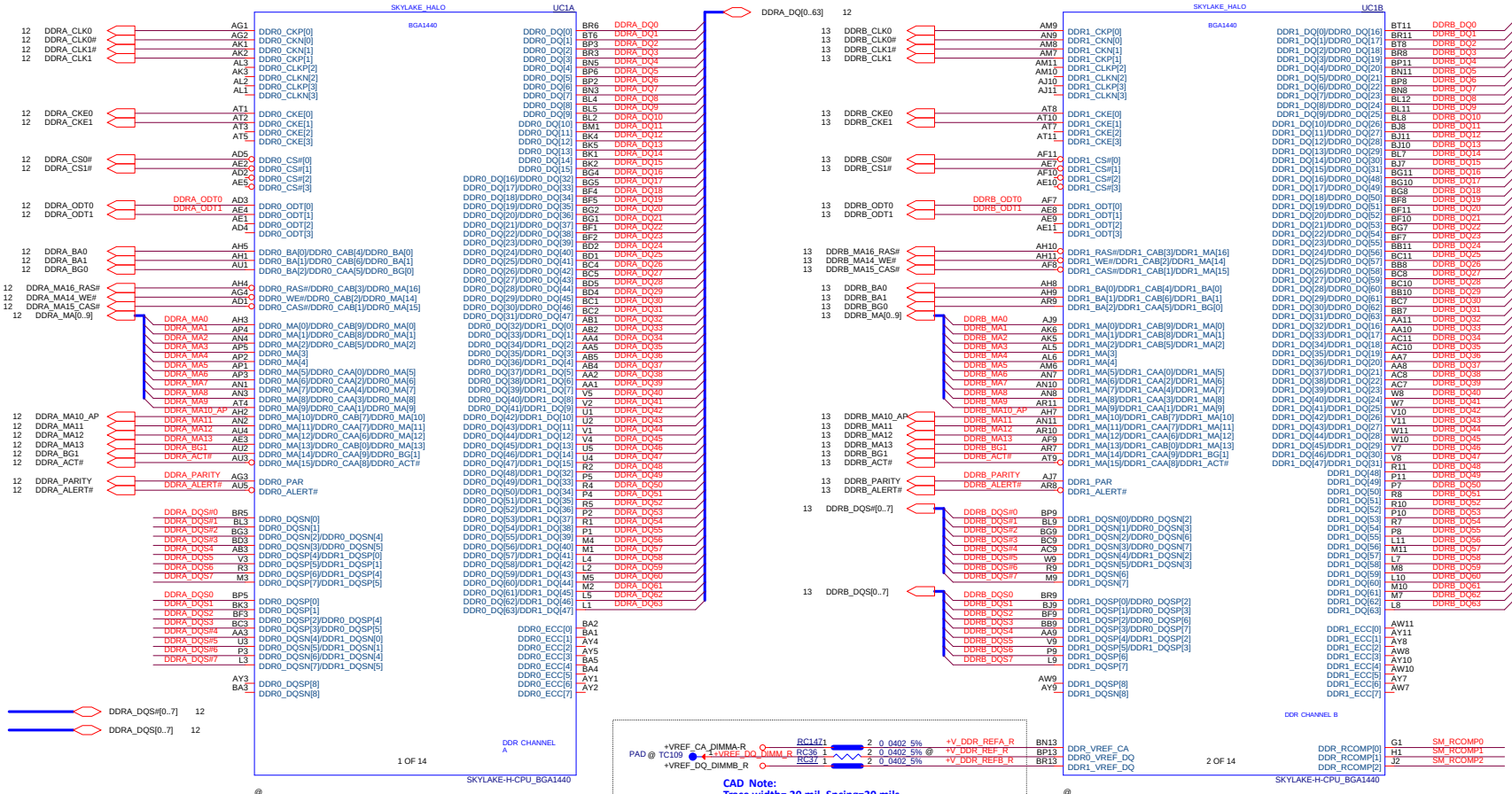

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Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: CPU (3/7) DDRVI

Size	Document Number	Rev
C	DY512	1.0

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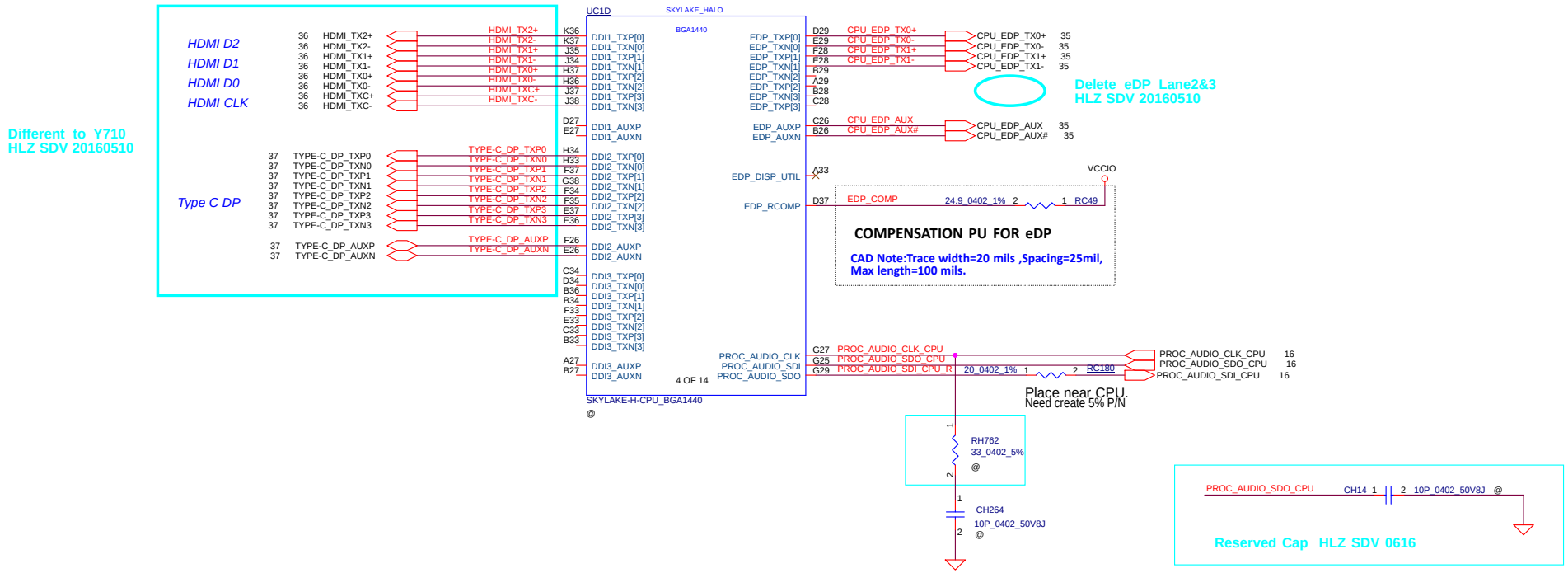

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Title: CPU (4/7) eDP, DDI

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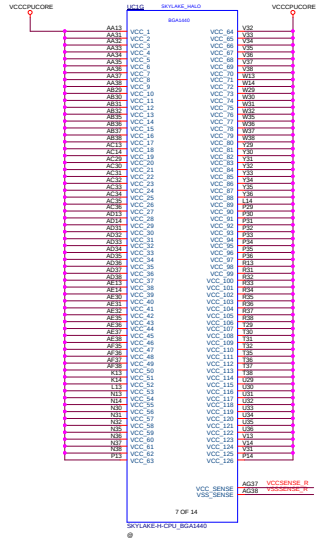
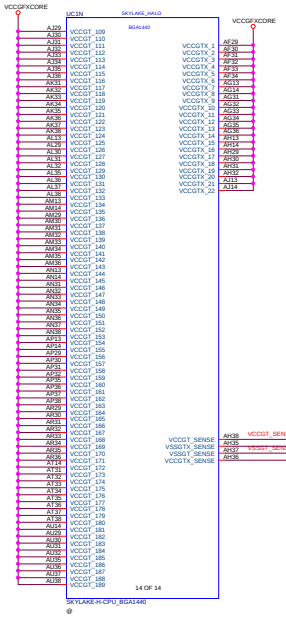
MAX 68A





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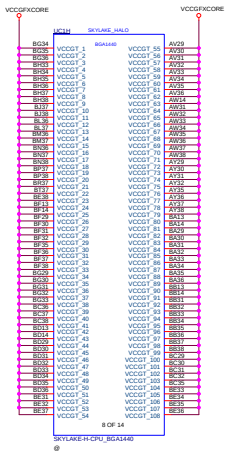

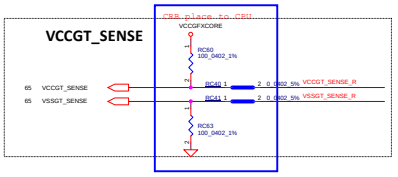

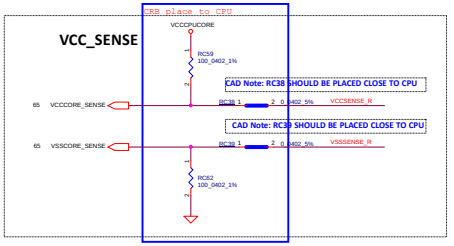

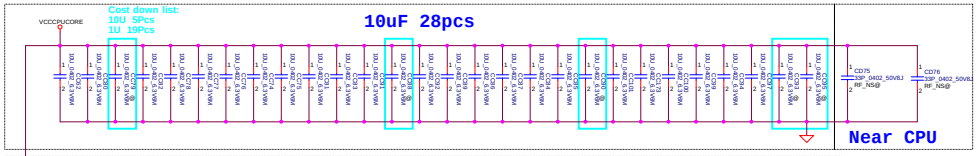

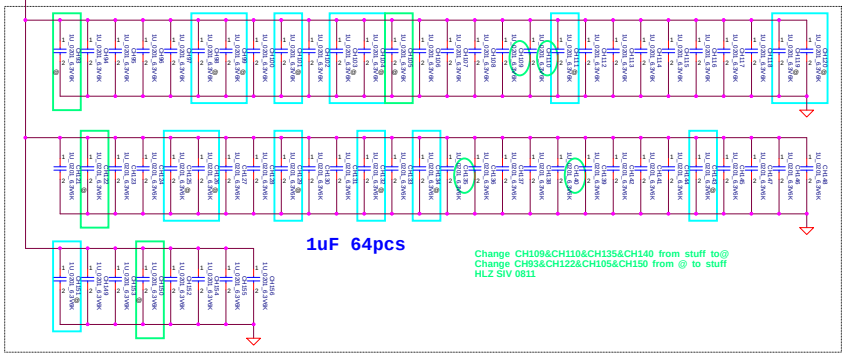

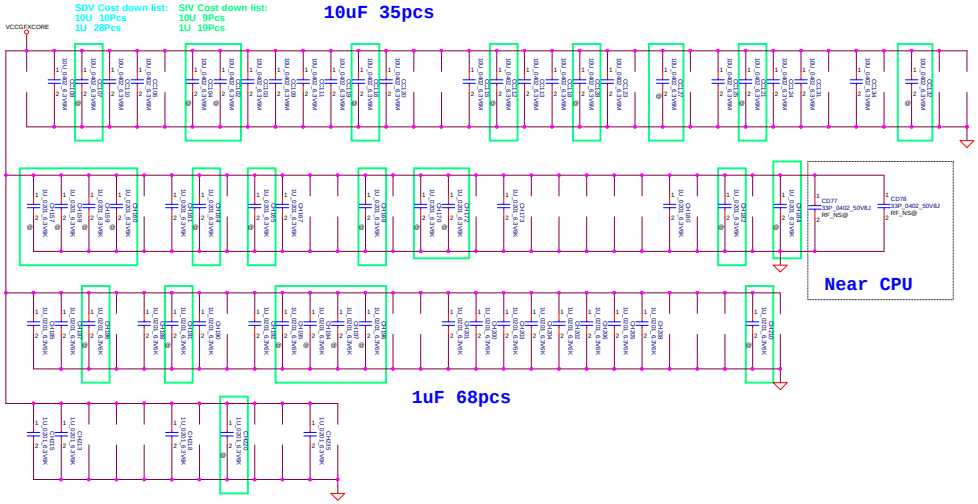

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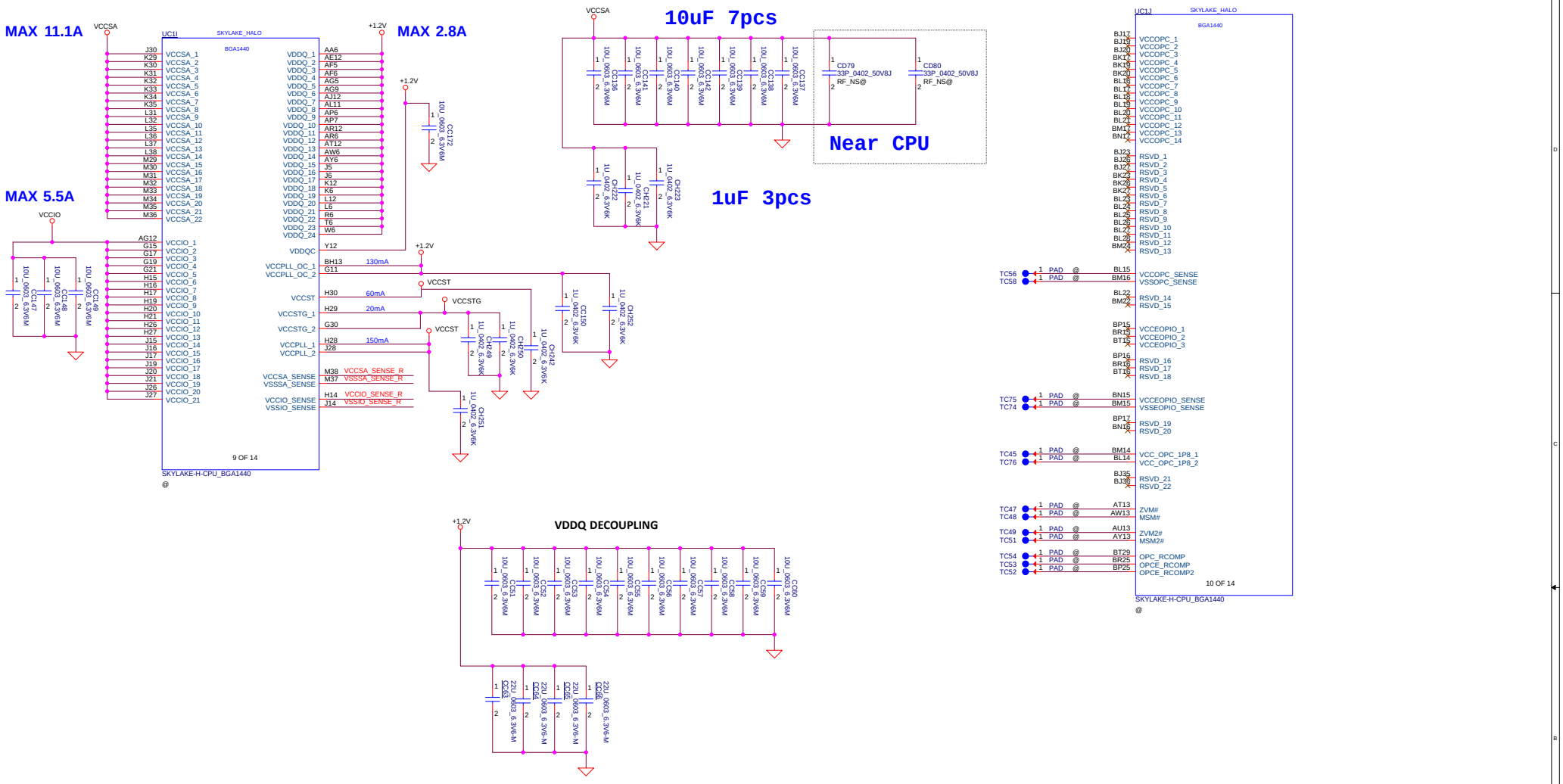

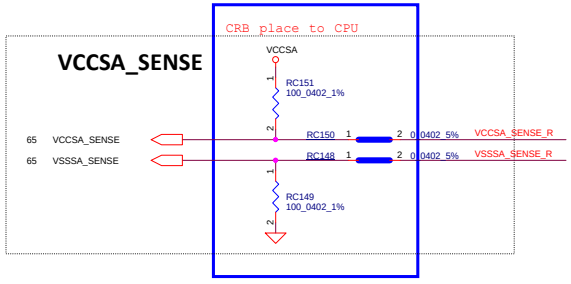

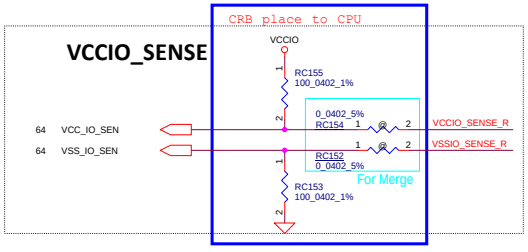

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Title: CPU (6/7) PWR, BYPASS

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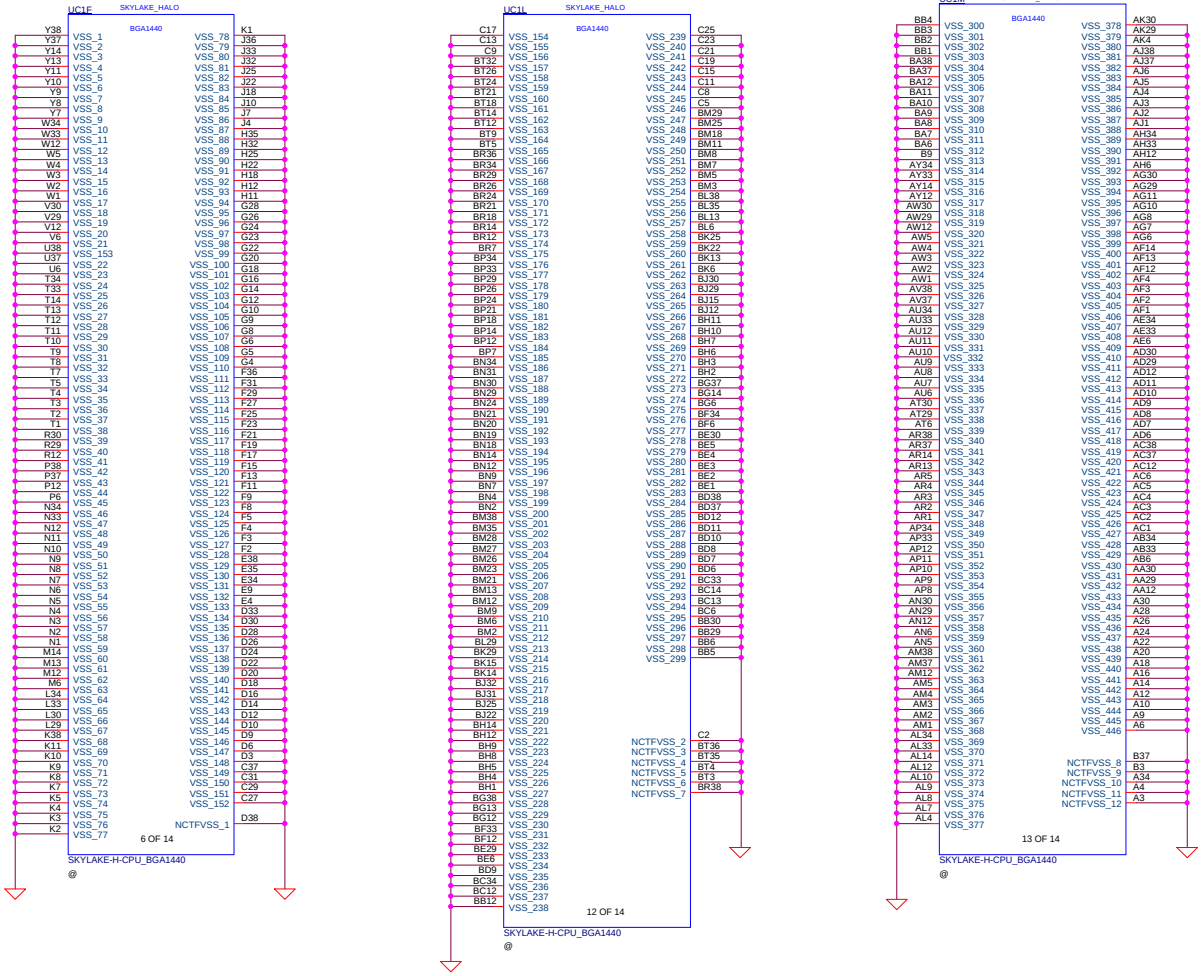

Security Classification	LC Future Center Secret Data		
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Title: *CPU (6/7) PWR, VSS*

Size	Document Number	Rev
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DDR4 SO-DIMM A

Change JDDRL1 from Foxconn to ARGOSY
HLZ SDV 20160510

JDDRL1A — RVS — ARGOSY_D4AR0-26001-1P52 — ME@

JDDRL1B — RVS — ARGOSY_D4AR0-26001-1P52 — ME@

RD5 240_0402_5% — DDRA_EVENT#

RD18 0_0402_5% — SMB_CLK_S3 — DDRA_VDDSPD — 13,16,45,50

RD20 0_0402_5% — +2.5V

CD27 2.2U_0603_6.3V6K — CD28 1U_0402_10V6-K — +3VS

CD69 0.1U_0402_10V7K @ — PCH_DRAMRST# — DDRA_CKE1

RD22 0_0402_5% @ — DDRA_SA0 — RD23 0_0402_5%

RD24 0_0402_5% @ — DDRA_SA1 — RD25 0_0402_5%

RD26 0_0402_5% @ — DDRA_SA2 — RD27 0_0402_5%

SPD Address = 0H

Layout Note:
Place near DIMM

MAX 0.5A — +0.6VS — CD23 10U_0402_6.3V6M — CD24 10U_0402_6.3V6M — CD25 10U_0402_6.3V6M

Layout Note:
Place near DIMM

MAX 0.5A — +2.5V — CD57 10U_0402_6.3V6M — CD58 10U_0402_6.3V6M — CD59 1U_0402_6.3V6K — CD60 1U_0402_6.3V6K

+VREF_CA_DIMMA_R — RD1 1K_0402_1% — RD2 2_0402_5% — +VREF_CA_DIMMA — RD3 1K_0402_1% — CD21 1U_0402_10V6-K — CD1 0.022U_0402_16V7-K — RD4 24.9_0402_1% — For EMC

Change RD2 to 0ohm jump

Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes
Place near DIMM scoket

MAX 3A — +1.2V — CD98 4.7U_0603_6.3V6K EMC_NS@ — CD97 4.7U_0603_6.3V6K EMC_NS@ — CD96 4.7U_0603_6.3V6K EMC_NS@ — CD95 0.1U_0402_10V7K EMC_NS@ — CD7 10U_0603_6.3V6M — CD8 10U_0603_6.3V6M — CD9 10U_0603_6.3V6M — CD10 10U_0603_6.3V6M — CD11 10U_0603_6.3V6M — CD12 10U_0603_6.3V6M — CD13 10U_0603_6.3V6M — CD14 10U_0603_6.3V6M

Change DDR4 220u to B2
HLZ SVD 0527

CD15 1U_0402_6.3V6K — CD16 1U_0402_6.3V6K — CD17 1U_0402_6.3V6K — CD18 1U_0402_6.3V6K — CD65 1U_0402_6.3V6K — CD66 1U_0402_6.3V6K — CD67 1U_0402_6.3V6K — CD68 1U_0402_6.3V6K

CD19 220U_B2_6.3VM_R25M @

CD81 33P_0402_50V8J RF@ — CD82 33P_0402_50V8J RF@

Near JDDRL1

Change CD81 & CD82 from @ to stuff based on RF requirement
HLZ SIT 0924

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

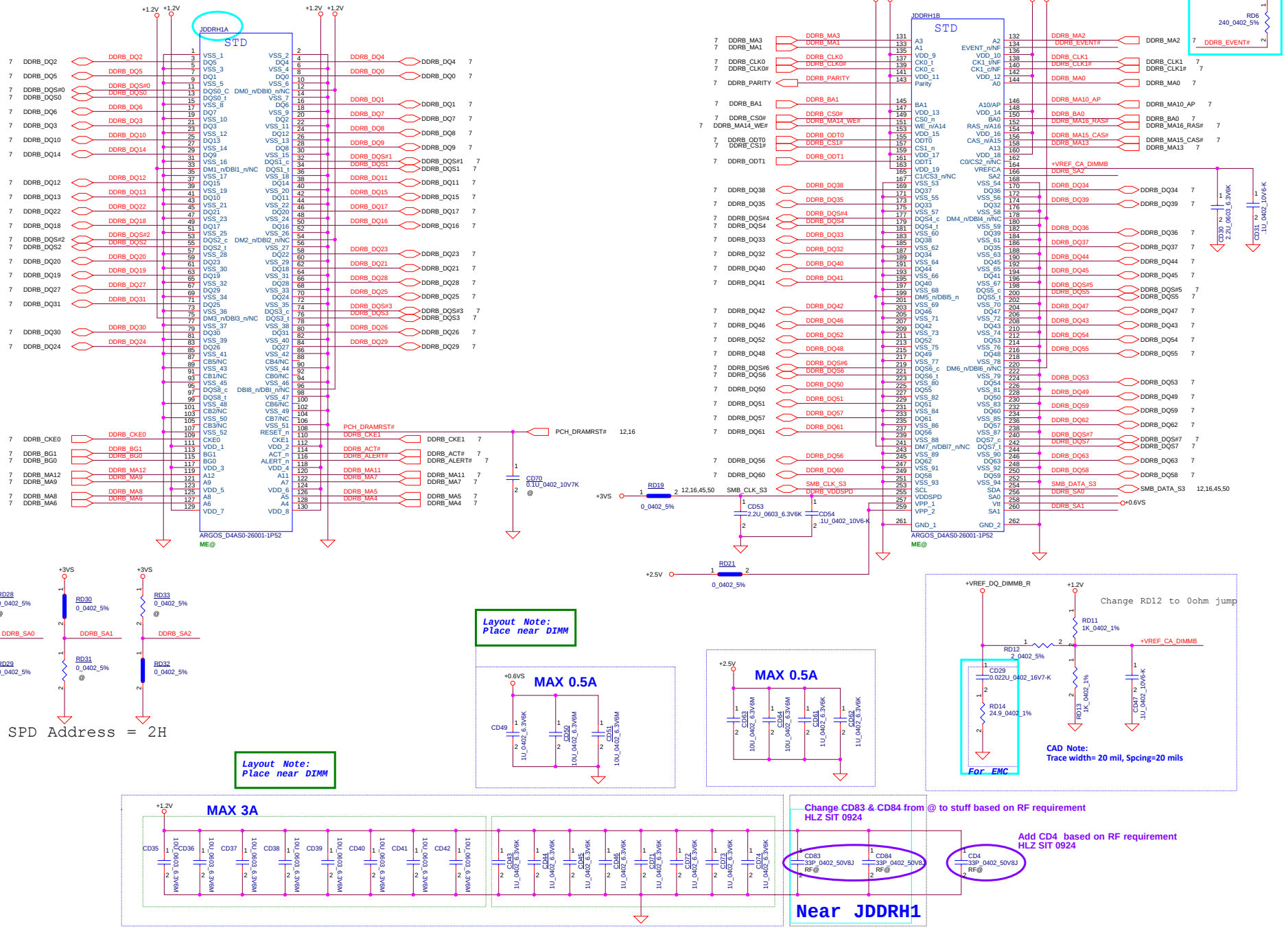
Title: DDRVI SO-DIMM A

Size: C | Document Number: DY512 | Rev: 1.0

Date: Friday, November 25, 2016 | Sheet 12 of 75

DDR4 SO-DIMM B

Change JDDRH1 from Foxconn to ARGOSY and RVS to STD
HLZ SDV 20160510



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: **DDRVI SO-DIMM B**

Size	Document Number	Rev
C	DY512	1.0

Date: Friday, November 25, 2016 Sheet 13 of 75

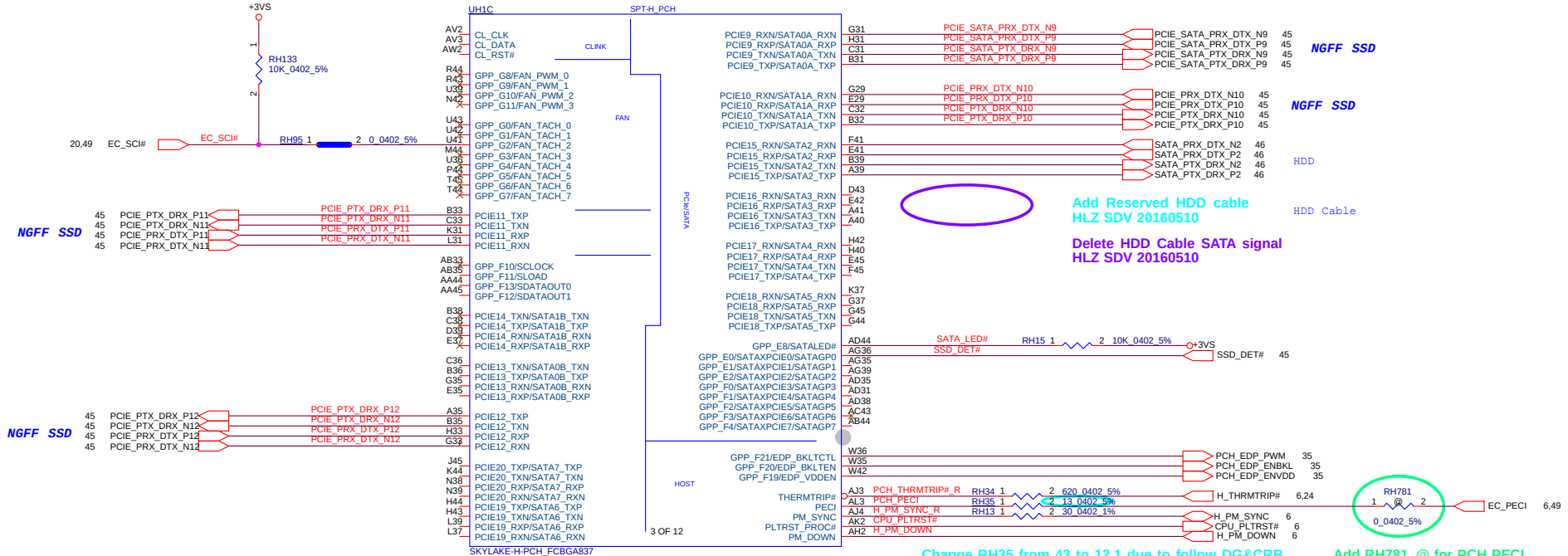


Table 1-2. PCH-H SKUs

Features	H110	H170	HM170	QM170	Z170	B150	Q150	Q170
Intel® Rapid Storage Technology	AHCI Only	Full Features	Full Features	Full Features	Full Features	AHCI Only	AHCI Only	Full Features
Total USB 3.0 Ports	4	8	8	8	10	6	8	10
Total USB 2.0 Ports	10[1]	14[3]	12[2]	12[2]	14[3]	12[2]	14[3]	14[3]
Total SATA 3.0 Ports (Max 6 Gb/s)	4	6	4	4	6	6	6	6
Total PCI Express* Lanes (Gen)	6 (2.0)	16 (3.0)	16 (3.0)	16 (3.0)	20 (3.0)	8 (3.0)	10 (3.0)	20 (3.0)
Total SATA Express Capable Ports (x2)	0	2	2	2	3	1	1	3
Total Intel® RST for PCIe Storage Devices (M.2 or SATA Express)	0	2	2	2	3	0	0	3
SKL Processor dgfx bifurcation support	No	No	Yes[4]	Yes[4]	Yes[4]	No	No	Yes[4]

Notes:
1. USB 2.0 port numbers: 1-10
2. USB 2.0 port numbers: 1-12
3. USB 2.0 port numbers: 1-14
4. PCIe configuration 1x16, or 2x8 or 2x4 or 1x8 are supported.

Title: **PCH (1/9) PCIe/SATA/GPPFG**

Size	Document Number	Rev
Custom	DY512	1.0

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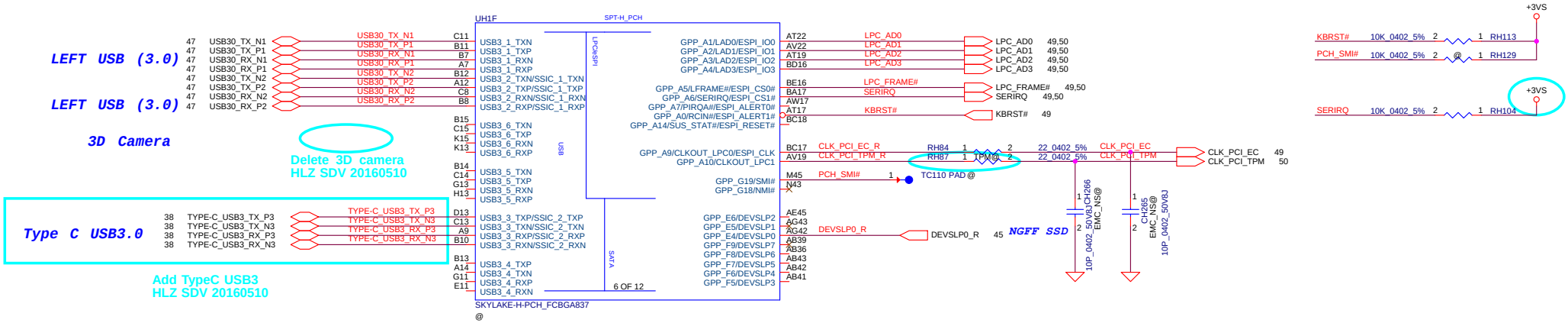

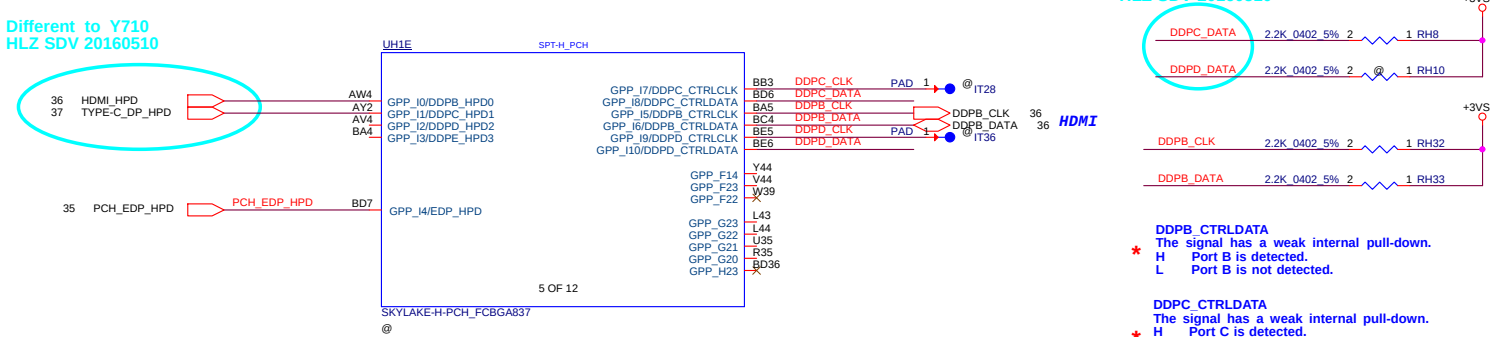

DDPB_CTRLDATA
The signal has a weak internal pull-down.
H Port B is detected.
L Port B is not detected.

DDPC_CTRLDATA
The signal has a weak internal pull-down.
H Port C is detected.
L Port C is not detected. (Default)

DDPD_CTRLDATA
The signal has a weak internal pull-down.
H Port D is detected.
L Port D is not detected. (Default)

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: PCH (2/9) USB3/GPPAEFGHI

Size	Document Number	Rev
Custom	DY512	1.0

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ADD PM_CLKRUN# for Nuvoton TPM
HLZ SIT 0920

Change RH56 from stuff to @
HLZ SIV 0811

Change PM_PWRBTN#_R PWR
HLZ SDV 0606

CMOS

Total Length 8000 mils

Add Testpad for Box RTC discharge Hai SVT 1118

Place JUMPER under RAM door

PLACE NEAR PCH

CRB Reserve

Strap

SMBALERT# / GPP_C2
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

SML0ALERT# / GPP_C5
0 = LPC Is selected for EC. (Default)
1 = eSPI Is selected for EC.

SML1ALERT# / PCHHOT#/GPP_B23
This signal has an internal pull-down

SPKR / GPP_B14
The signal has a weak internal pull-down.
0 = Disable " Top Swap" mode. (Default)
1 = Enable " Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (bendyd through FITC).

AS EMC request

HDA_SDO This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.

PCH is Master

DIMM1, DIMM2, Mini CARD, TP

PCH is salve

GPU, EC, Thermal Sensor

Reserved Cap HLZ SDV 0616

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Title: PCH (3/9) HDA,RTC,SMBUS,PM

Size	Document Number	Rev
C	DY512	1.0

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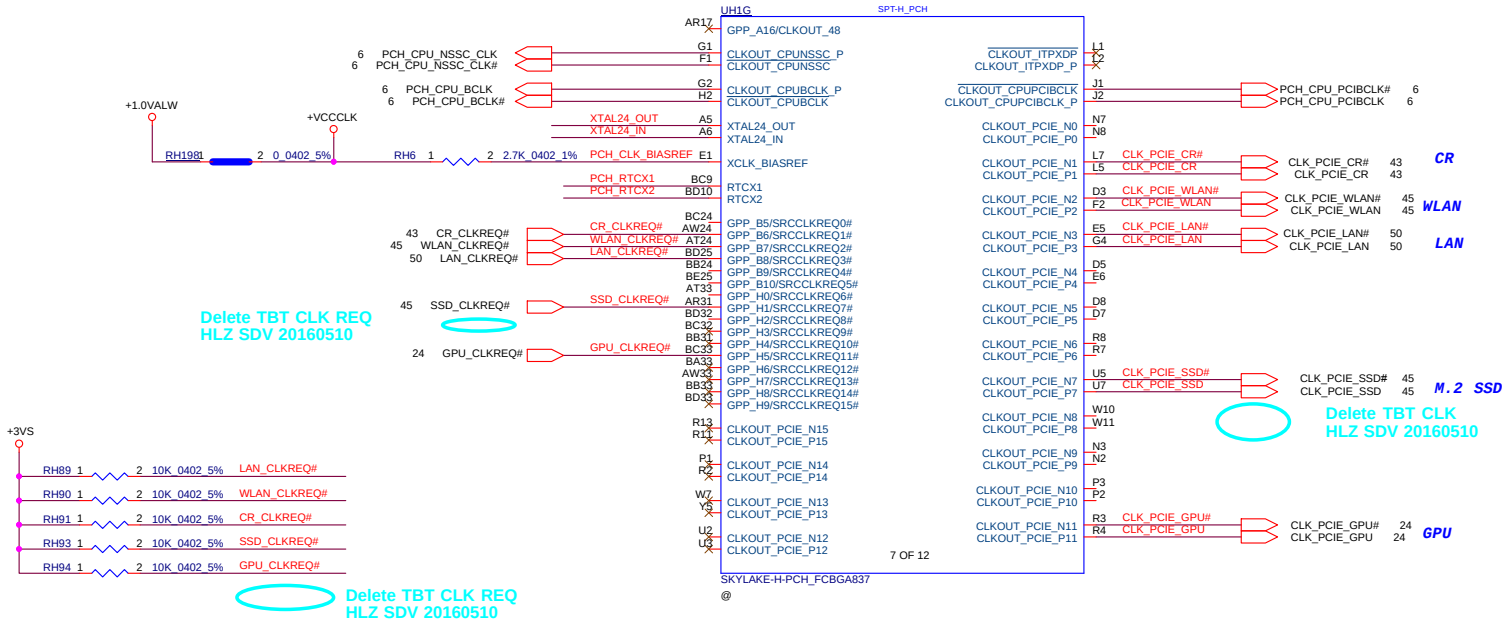
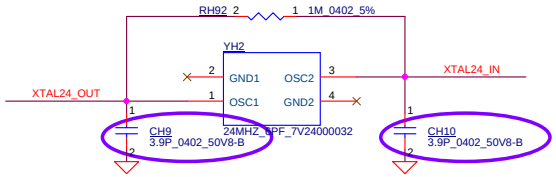
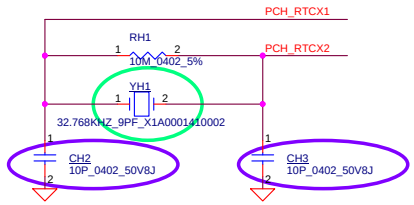




Change CH9 & CH10 from 3.3P to 3.9P HLZ SIT 0921

Change CH9 & CH10 from 4.7P to 3.3P HLZ SIV 0811



Change CH2 & CH3 from 6.8P to 10P HLZ SIT 0921

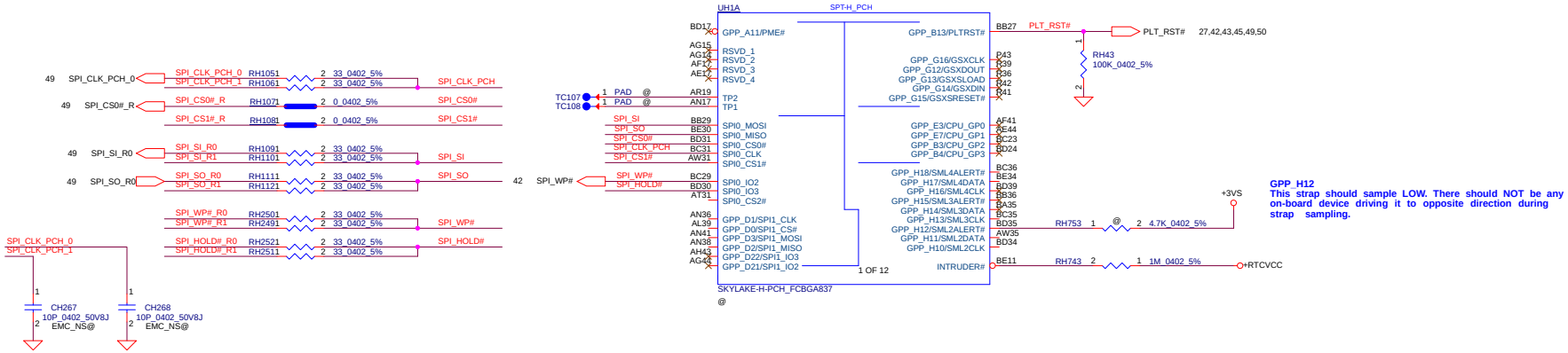
Change YH1 based on common pool HLZ SIV 0811

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: PCH (3/9) CLOCK,GPPBH

Size	Document Number	Rev
Custom	DY512	1.0

Date: Friday, November 25, 2016 Sheet 17 of 75



GPP_H12
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

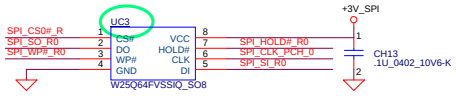
SPI0_MOSI
SPI0_MISO
This signal has an internal pull-up.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

500mA **500mA**

+3V_SPI

1. If support DS3, connect to +3VS and don't support EC mirror code;
2. If don't support DS3, connect to +3VALW_PCH and support EC mirror code.

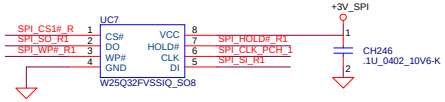
64Mb Flash ROM **250mA**



Change UC3 Value from W25Q64FVSSIG_SO8 to W25Q64FVSSIQ_SO8
HLZ SIV 0811

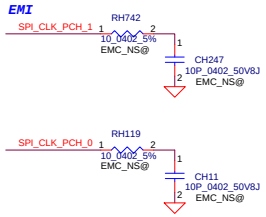
Delete socket

32Mb Flash ROM **250mA**



Delete socket

For EMI



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: **PCH (5/9) SPI,SMBUS,GPPBEGH**

Size	Document Number	Rev
Custom	DY512	1.0

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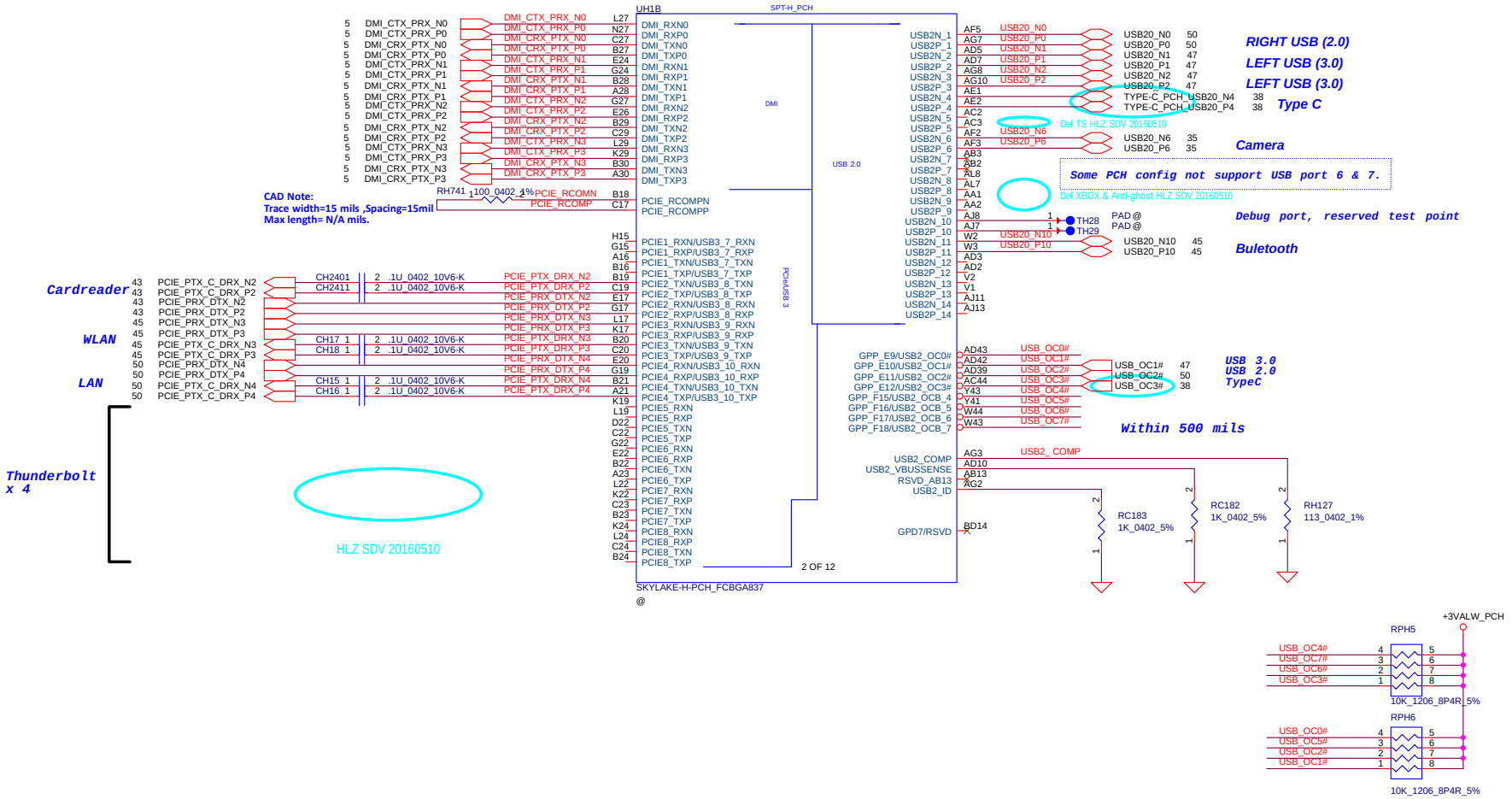

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: PCH (5/9) DMI, PCIe, USB2, GP

Size	Document Number	Rev
Custom	DY512	1.0

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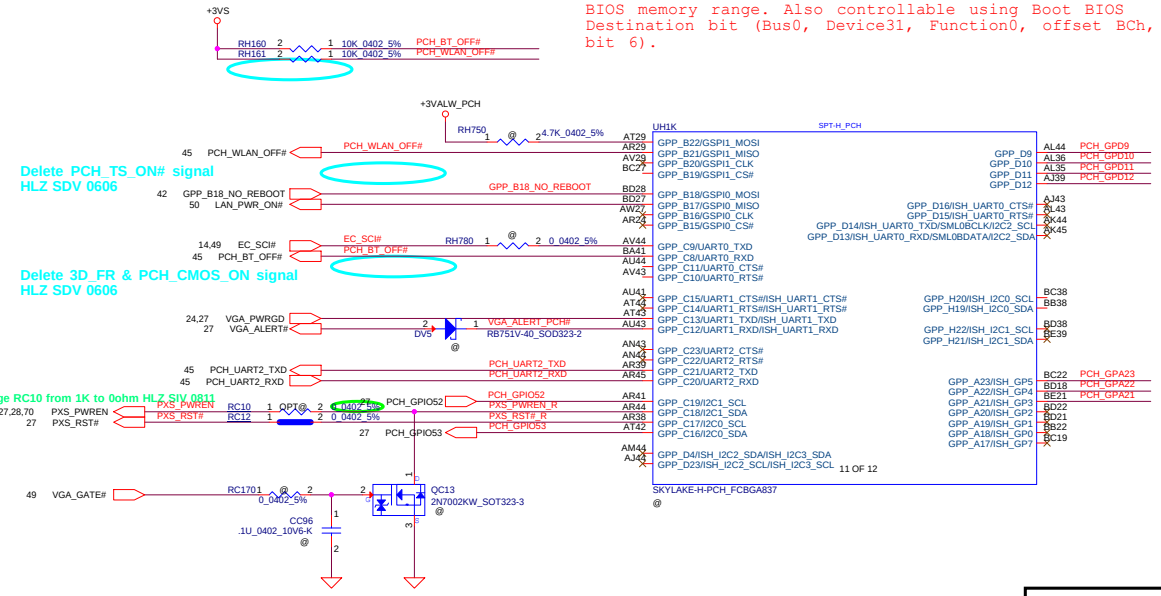
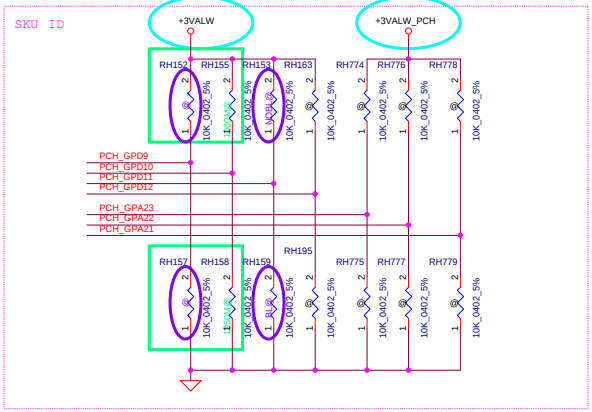
GSPI1_MOSI / GPP_B22
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6).

Bit 6	Boot BIOS Destination
0	SPI (Default)
1	LPC





1. Add KB BL GPIO
2. Delete DZ510 / DY512 BOM structure
HLZ SIT 0923

Function	PCH_GPD9	PCH_GPD10	PCH_GPD11	PCH_GPD12	PCH_GPD21	PCH_GPD22	PCH_GPD23
DY512	X	X	X	X	X	X	X
DZ510	X	X	X	X	X	X	X
NV 1050M	X	0	X	X	X	X	X
NV 1060M	X	1	X	X	X	X	X
KB BL	X	X	0	X	X	X	X
No KB BL	X	X	1	X	X	X	X
PCIE SSD	X	X	X	0	X	X	X
Optane memory	X	X	X	1	X	X	X
RSV	X	X	X	X	X	X	X
RSV	X	X	X	X	X	X	X

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: PCH (6/9) GPPPABCD, I2C

Size	Document Number	Rev
C	DY512	1.0

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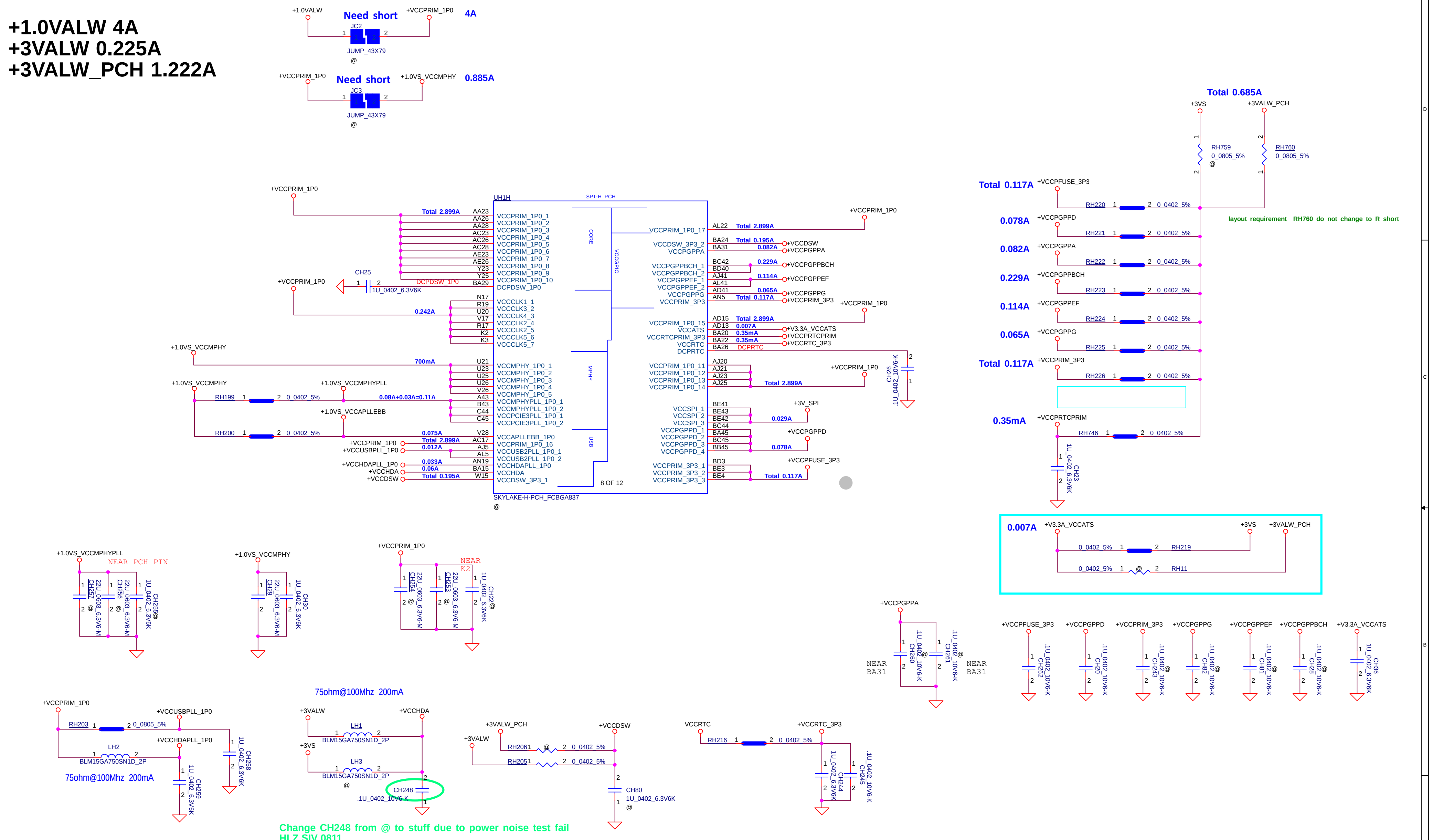

+1.0VALW 4A
+3VALW 0.225A
+3VALW_PCH 1.222A
Need short
JC2
JUMP_43X79
Need short
JC3
JUMP_43X79
4A
0.885A
+1.0VALW
+VCCPRIM_1P0
+1.0VS_VCCMPHY
Total 0.685A
+3VS
+3VALW_PCH
RH759 0_0805_5%
RH760 0_0805_5%
layout requirement RH760 do not change to R short
Total 0.117A
+VCCPFUSE_3P3
0.078A
+VCCPGPPD
0.082A
+VCCPGPPA
0.229A
+VCCPGPPBCH
0.114A
+VCCPGPPEF
0.065A
+VCCPGPPG
Total 0.117A
+VCCPRIM_3P3
0.35mA
+VCCPRTCPRIM
UH1H
SPT-H_PCH
SKYLAKE-H-PCH_FCBGA837
8 OF 12
CORE
VCCGPIO
MPHY
USB
VCCPRIM_1P0_1 … VCCPRIM_1P0_17
DCPDSW_1P0
VCCCLK1_1, VCCCLK3_2, VCCCLK4_3, VCCCLK2_4, VCCCLK2_5, VCCCLK5_6, VCCCLK5_7
VCCMPHY_1P0_1 … VCCMPHY_1P0_5
VCCMPHYPLL_1P0_1, VCCMPHYPLL_1P0_2
VCCPCIE3PLL_1P0_1, VCCPCIE3PLL_1P0_2
VCCAPLLEBB_1P0
VCCUSB2PLL_1P0_1, VCCUSB2PLL_1P0_2
VCCHDAPLL_1P0
VCCHDA
VCCDSW_3P3_1, VCCDSW_3P3_2
VCCPGPPA
VCCPGPPBCH_1, VCCPGPPBCH_2
VCCPGPPEF_1, VCCPGPPEF_2
VCCPGPPG
VCCPRIM_3P3
VCCATS
VCCRTCPRIM_3P3
VCCRTC
DCPRTC
VCCSPI_1, VCCSPI_2, VCCSPI_3
VCCPGPPD_1 … VCCPGPPD_4
VCCPRIM_3P3_1, VCCPRIM_3P3_2, VCCPRIM_3P3_3
Total 2.899A
0.242A
700mA
0.08A+0.03A=0.11A
0.075A
0.012A
0.033A
0.06A
Total 0.195A
0.082A
0.007A
0.35mA
0.029A
0.078A
CH25 1U_0402_6.3V6K
CH26 .1U_0402_10V6-K
RH199 0_0402_5%
RH200 0_0402_5%
RH220 … RH226 0_0402_5%
RH746 0_0402_5%
CH23 1U_0402_6.3V6K
0.007A
+V3.3A_VCCATS
RH219 0_0402_5%
RH11 0_0402_5%
NEAR PCH PIN
NEAR K2
NEAR BA31
CH257, CH256 22U_0603_6.3V6-M
CH255 1U_0402_6.3V6K
CH29 22U_0603_6.3V6-M
CH30 1U_0402_6.3V6K
CH254, CH253 22U_0603_6.3V6-M
CH22 1U_0402_6.3V6K
CH260, CH261 .1U_0402_10V6-K
CH262, CH20, CH243, CH82, CH81, CH28 .1U_0402_10V6-K
CH36 1U_0402_6.3V6K
75ohm@100Mhz 200mA
RH203 0_0805_5%
LH2 BLM15GA750SN1D_2P
CH258 1U_0402_6.3V6K
CH259 1U_0402_6.3V6K
LH1 BLM15GA750SN1D_2P
LH3 BLM15GA750SN1D_2P
CH248 .1U_0402_10V6-K
RH206 0_0402_5%
RH205 0_0402_5%
CH80 1U_0402_6.3V6K
VCCRTC
+VCCRTC_3P3
RH216 0_0402_5%
CH244 1U_0402_6.3V6K
CH245 .1U_0402_10V6-K

Change CH248 from @ to stuff due to power noise test fail
HLZ SIV 0811

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Title: PCH (7/9) PWR

Size: C | Document Number: DY512 | Rev: 1.0

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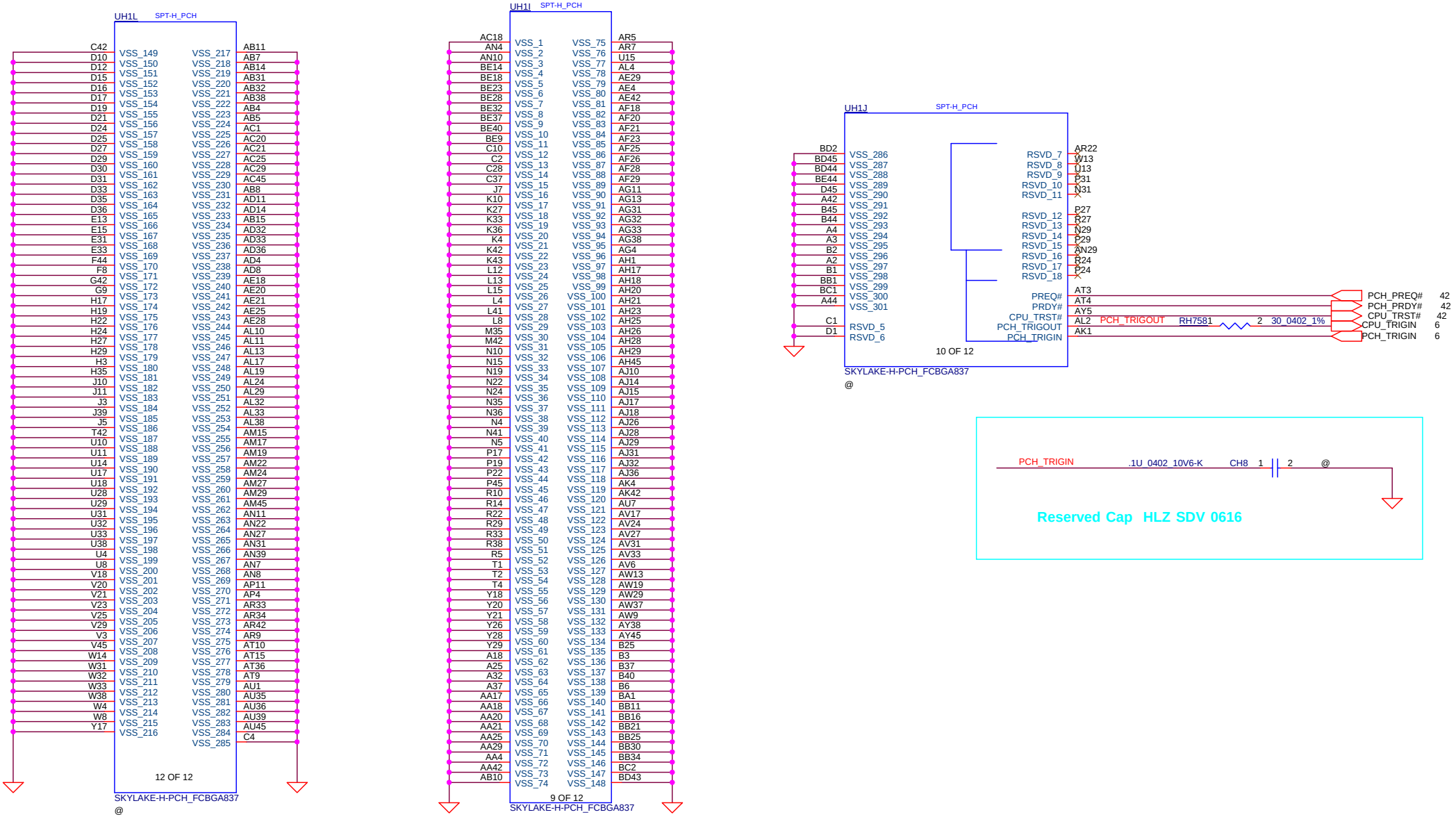

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: **PCH (9/9) VSS**

Size	Document Number	Rev
B	DY512	1.0

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N17P-G1 GPIO

GPIO	I/O	ACTIVE	Function Description	I/O Termination
GPIO0	OUT	-	PWM Output to control NVVDD	
GPIO1	OUT	-	FB Enable for GC6 2.1	
GPIO2	IN	-	GPU wake signal for GC6 2.1	
GPIO3	OUT	-	PWM Output to control the SRAM power supply	
GPIO4	OUT	-	GPU power sequencing for GC6 2.1 --- 1V8_MAIN_EN	
GPIO5	IN	N/A	Active low Frame Lock	
GPIO6	OUT	-	Phase Shedding, NVVDD_PSI	
GPIO7	OUT	N/A	Panel Backlight enable	
GPIO8	OUT	-	Memory voltage Control	
GPIO9	I/O	-	Active Low Thermal Alert	
GPIO10	OUT	-	Memory VREF Control (100K pull Down)	
GPIO11	OUT	-	Panel Power enable	
GPIO12	IN	-	AC power detect or power supply overdraw input	(10K pull High)
GPIO13	OUT	N/A	LCD Panel Backlight Enable	
GPIO14	IN	N/A	Hot Plug Detect for IFPA	
GPIO15	IN	N/A	Hot Plug Detect for IFPB	
GPIO16	OUT	-	System side PCIe reset monitor	
GPIO17	IN	N/A	Hot Plug Detect for IFPD	
GPIO18	IN	N/A	Hot Plug Detect for IFPE	
GPIO19	OUT	N/A	3D Vision L/R Signal	
GPIO20		N/A	GC5_MODE	
GPIO21	I/O	N/A	UNUSED	
GPIO22	I/O	N/A	UNUSED	
GPIO23	OUT	-	GPU PCIe self-reset control	
GPIO24	IN	N/A	Hot Plug Detect for IFPF	
GPIO25		N/A	UNUSED	
GPIO26		N/A	UNUSED	
GPIO27	IN	N/A	Hot Plug Detect for IFPC	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111

H=High: Tied to 1.8V
M=Middle: Tied to 0.9V
L=Low: Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
L	L	L	1111 DEFAULT
L	L	H	1110
L	H	L	1101
L	H	H	1100
H	L	L	1011
H	L	H	1010
H	H	L	1001
H	H	H	1000
L	L	M	0111
L	M	L	0110
L	M	H	0101
L	H	M	0100
H	L	M	0011
H	M	L	0010
H	M	H	0001
H	H	M	0000

1:ENABLE 0:DISABLE

SOR0/1/2/3 ENABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

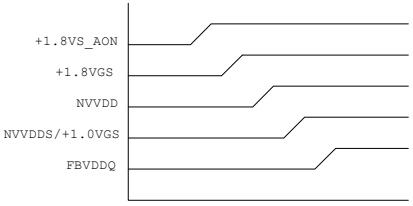
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

N17P-G1 Power Sequence

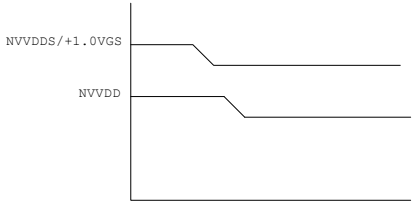


1. All power rail ramp up time should be larger than 40us and is recommended to be less than 2ms.

2. T (from 1V8_MAIN_EN to PEX_DVDD/NVVDD_Pgood) must NOT exceed 4ms.

3. All 3.3V devices that connect to the GPU must be powered after 1V8_AON; GPU can NOT have any 3.3V leakage path before 1V8_AON present.

4. The previous power rail must ramp up to 90% before the next power rail can start ramping up.



1. NVVDDS/PEX_DVDD must ramp down before NVVDD, all other power rails can ramp down together with NVVDD.

2. All 3.3V devices that connect to the GPU must be ramp down before 1V8_AON; GPU can NOT have any 3.3V leakage path after 1V8_AON and 1.8V_MAIN power down.

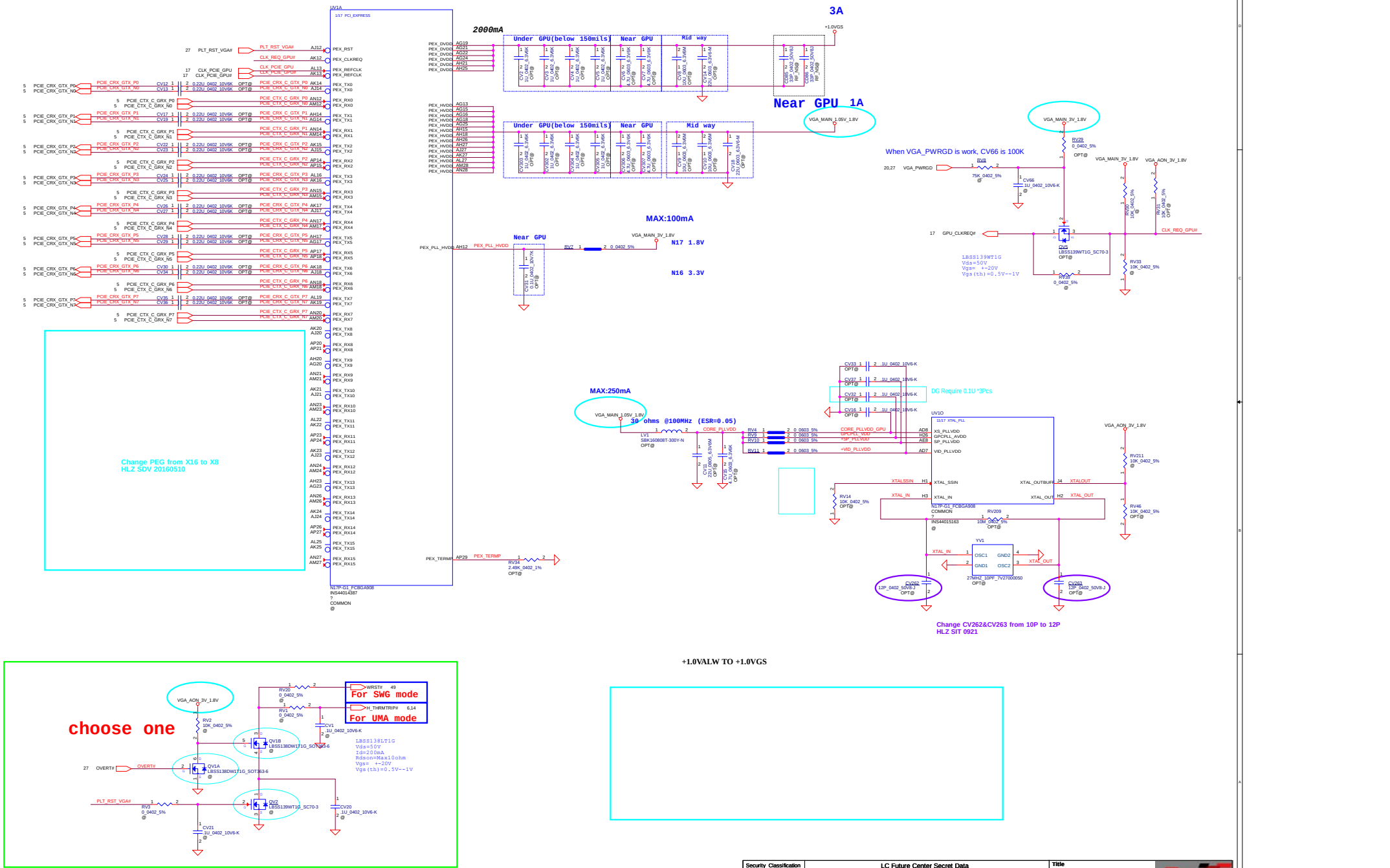
3. The previous power rail must ramp down to 10% before the next power rail can start ramping down.

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: VGA Notes List

Size	Document Number	Rev
C	DY512	1.0

Date: Friday, November 25, 2016 Sheet 23 of 75



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

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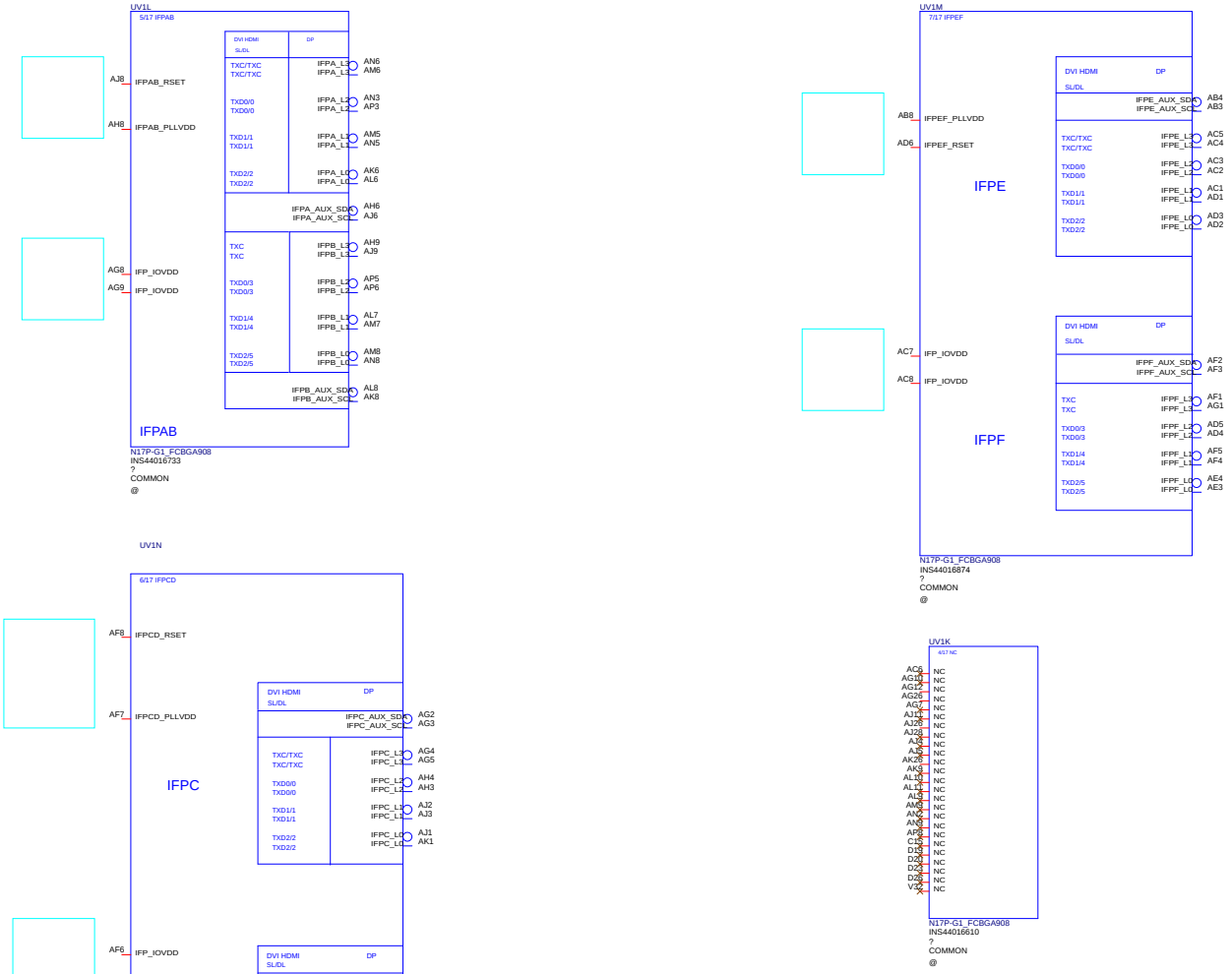
Title: *N17P-G1_PEG I/F*

Size: Custom | Document Number: *DY512* | Rev: 1.0

Date: Friday, November 25, 2016 | Sheet 24 of 75



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

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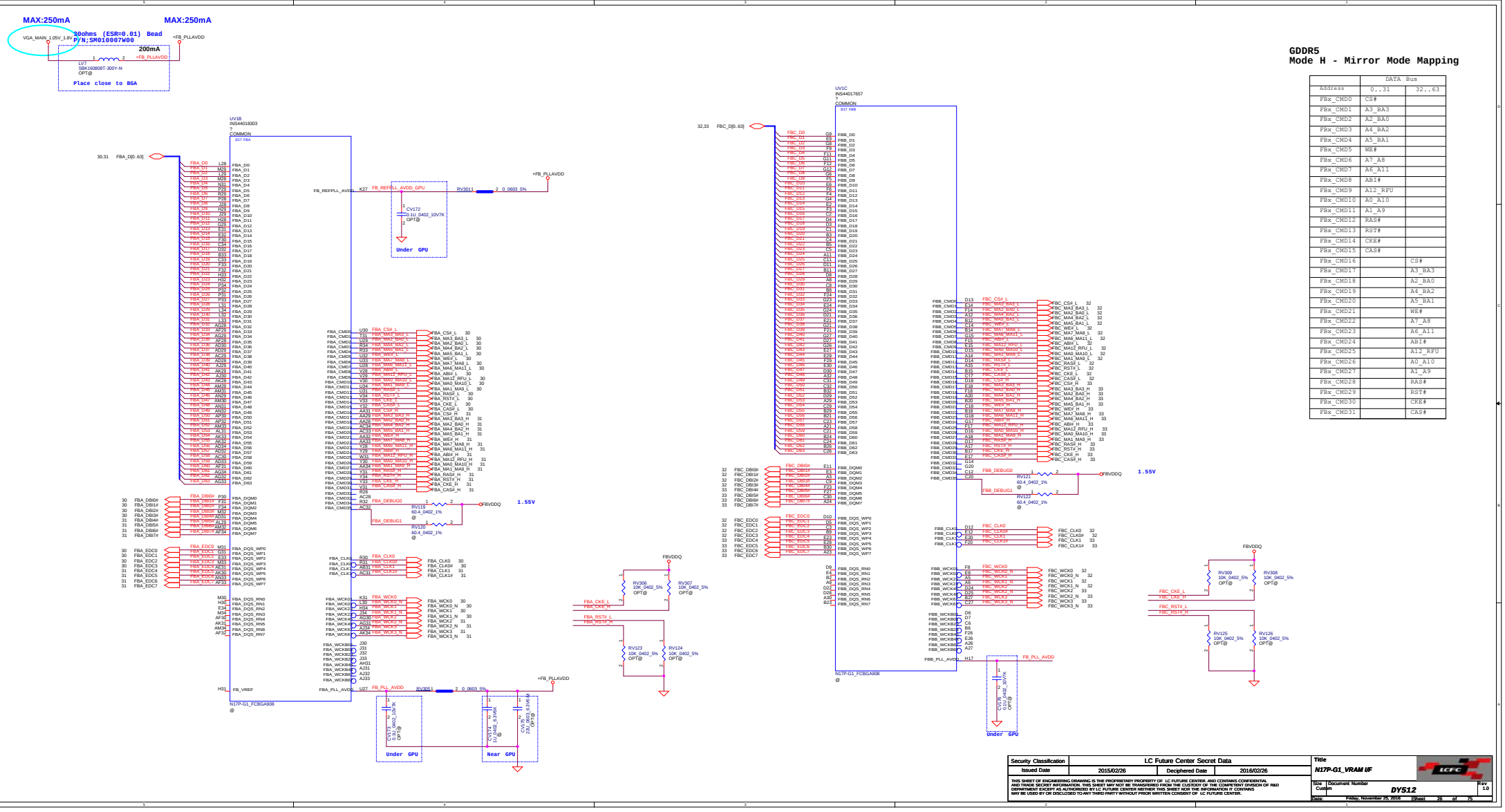
Title: N17P-G1_DIGITAL OUT I/F

Size	Document Number	Rev
Custom	DY512	1.0

Date: Friday, November 25, 2016 Sheet 25 of 75

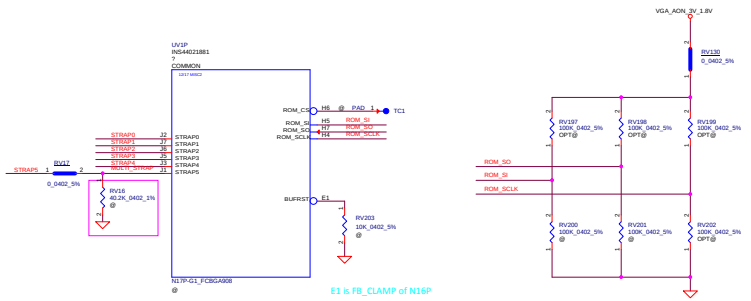


GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	N17P-G1_VRAM I/F		
Size	Document Number		Rev
Custom	DY512		1.0
Date:	Friday, November 25, 2016	Sheet 28 of 75	



ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
H	H	M	0000

1:ENABLE 0:DISABLE

SOR0/1/2/3 DISABLE

GPU	FB Memory (GDDR5)		RAMCFG[4:0]	STRAP2	STRAP1	STRAP0
8Gb	Samsung 8Gb	K4G80325FB-HC28	0(0x0000)	L	L	L
	Micron 8Gb	MT51J256M32HF-70:A	1(0x0001)	L	L	H
	Hynix 8Gb	H5GC8H24MJR-R0C	2(0x0010)	L	H	L
4Gb	Samsung 4Gb	K4G41325FE-HC28	7(0x0111)	H	H	H
	Hynix 4Gb	H5GC4H24AJR-R0C	6(0x0110)	H	H	L
	Micron 4Gb	EDW4032BABG-70-F	8(0x1000)	L	L	M

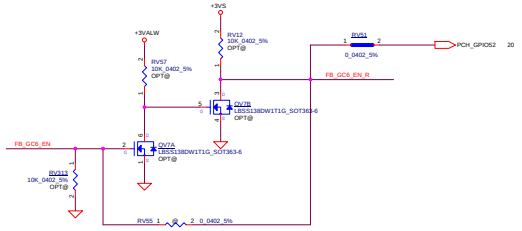
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

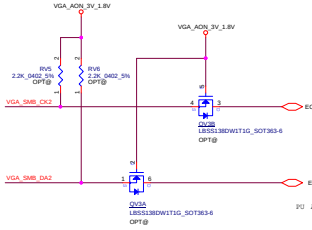
1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE

1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGNAL

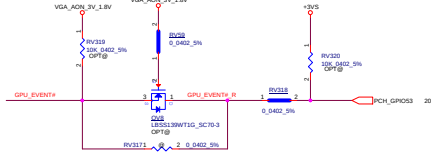
1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER

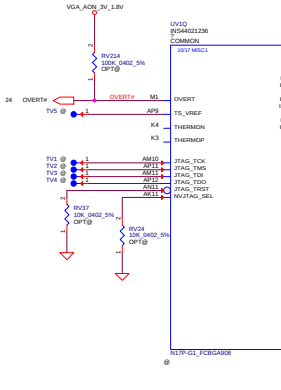
1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE



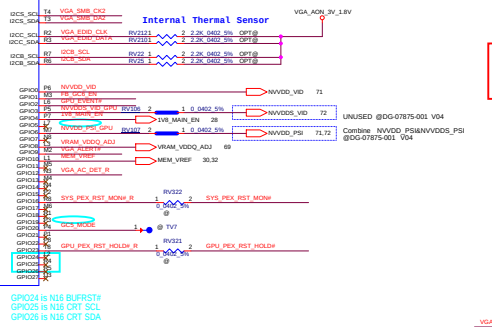


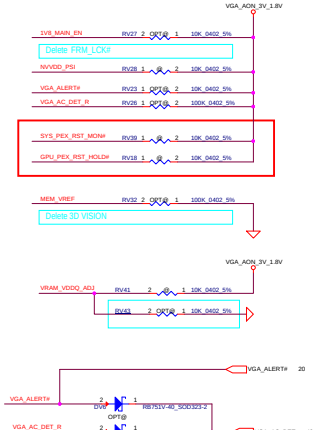
PU AT EC SIDE, +3VS AND 4.7K

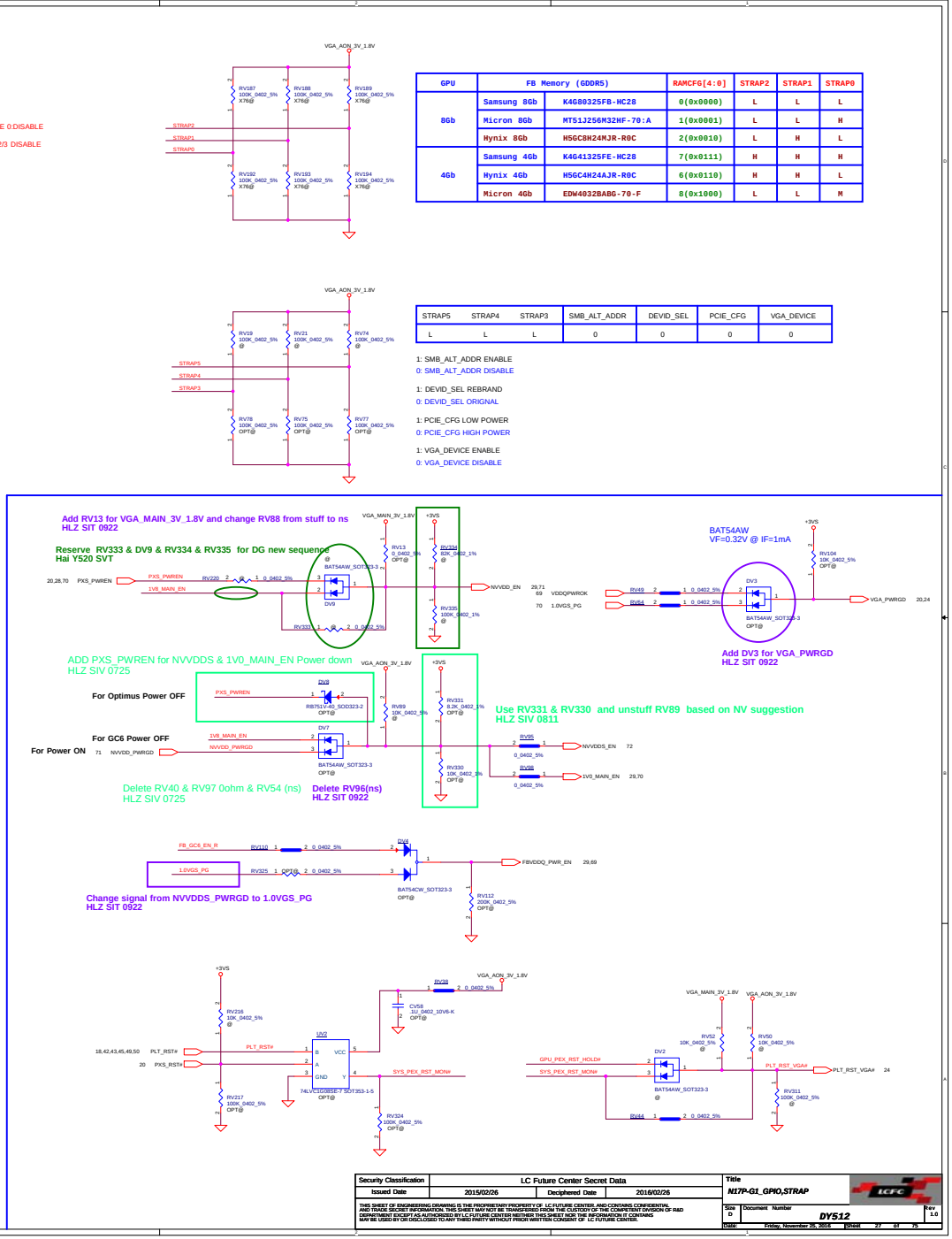




Internal Thermal Sensor







Security Classification	LC Future Center Secret Data		Title
Issued Date	2015/02/26	Deciphered Date 2016/02/26	N17P-G1_GPIO,STRAP

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D	DY512	1.0

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5A Peak 8A

Cost down list:
1U 2Pcs

Under GPU(below 150mils)

only for N16

Near GPU

Add CV300 for power noise issue

Delete CV300 330U HLZ SDV 0610

CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.20hm
FB_CAL_x_PU_GND	40.20hm
FB_CAL_xTERM_GND	60.40hm

Place near balls

PLACE MIDWAY BETWEEN FBA AND FBB

1.8V Total 1A (AON+MAIN)

0.5A VGA_AON_3V_1.8V

0.5A VGA_MAIN_3V_1.8V

trace width: 16mils
differential voltage sensing.
differential signal routing.

19A Peak 42A

Cost down list:
4.7U 1Pcs
1U 1Pcs

POSCAP

Follow NV suggestion for NVVDDS Hai Y520 SVT

Delete +3.3V_AON

Change QV18 from LBSS138LT1G_SOT-23-3 to LBSS138LT1G_SC70-3 Hai Y520 SVT

Add +1.8V-AON discharger circuit HLZ SIV 0811

Delete PD3503 and Reserve PD3/PR4/PR5/CV38
HLZ SIT 0923

V20B+

Vg=16.4V@AC
Vg=7.38V@Battery

2A

AON7408L
Vds=30V
Ids=15A
Rdson=28mohm@Vgs=4.66V
=20mohm@Vgs=6V
=18mohm@Vgs>10V
Vgs=+-20V
Vgsth=1~3V

Add +1.8V_MAIN discharger circuit
HLZ SIT 0928

2A

1.5A

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: N17P-G1_POWER

Size: Custom | Document Number: DY512 | Rev: 1.0

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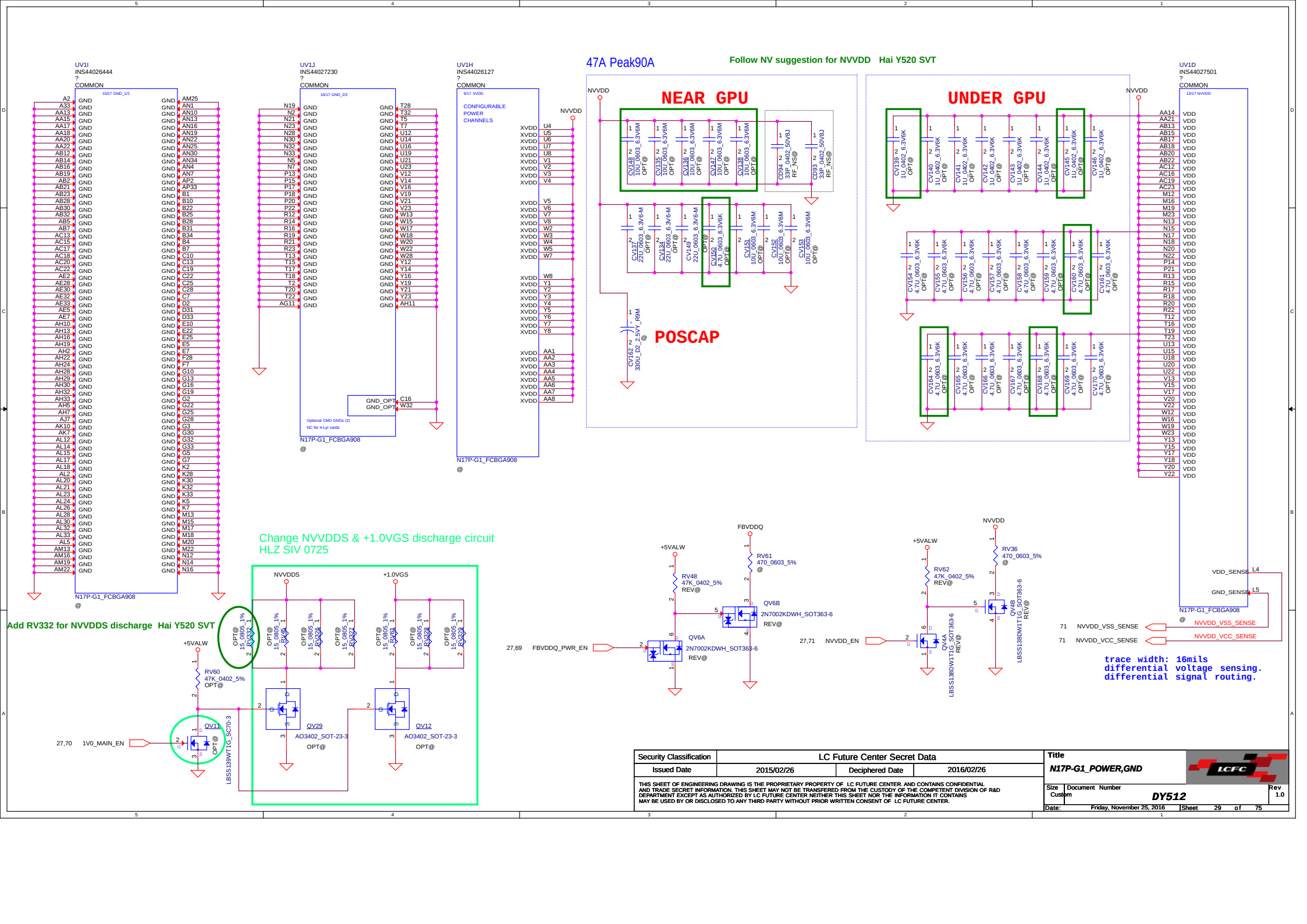


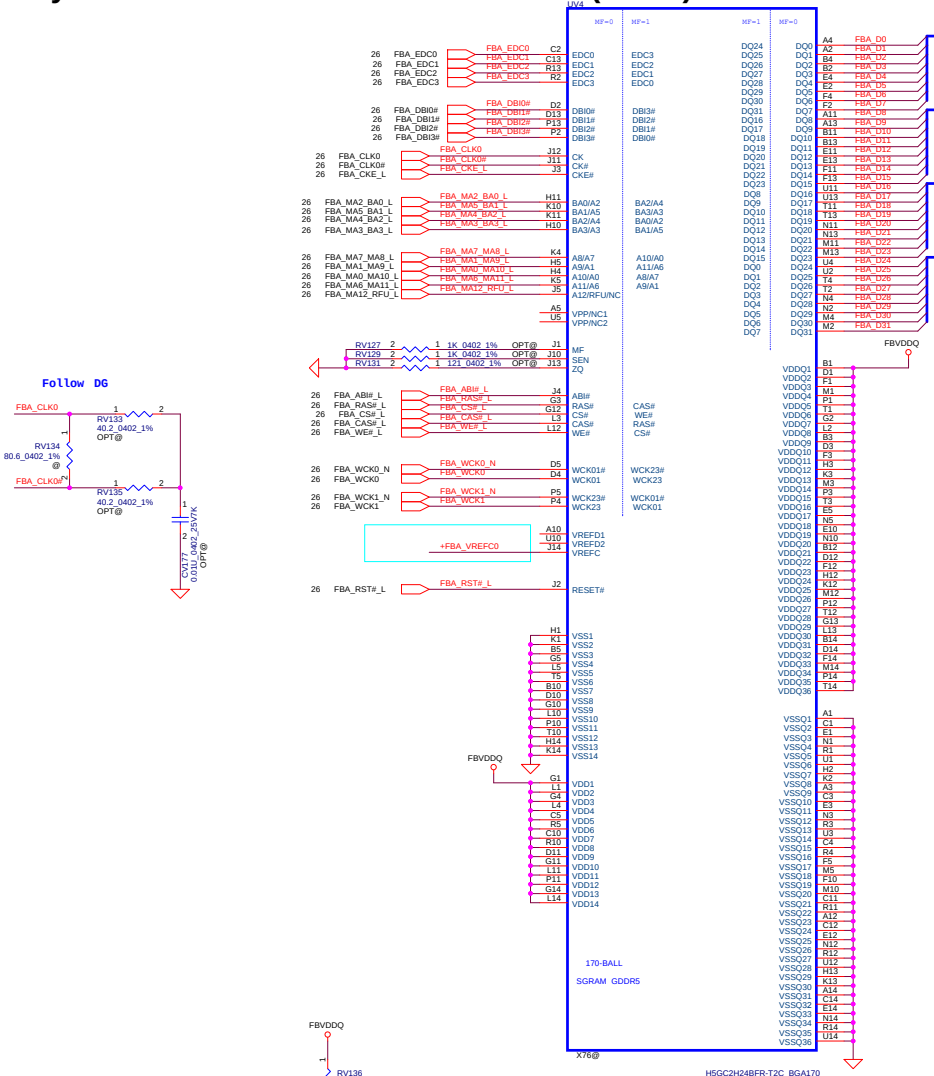
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: *N17P-G1_POWER,GND*

Size: Custom | Document Number: *DY512* | Rev: 1.0

Date: Friday, November 25, 2016 | Sheet 29 of 75

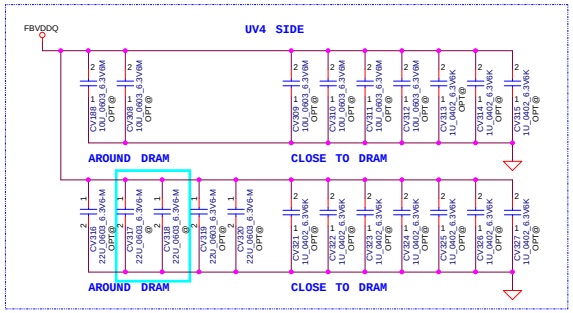
Memory Partition A - Lower 64 bits(MF=0)

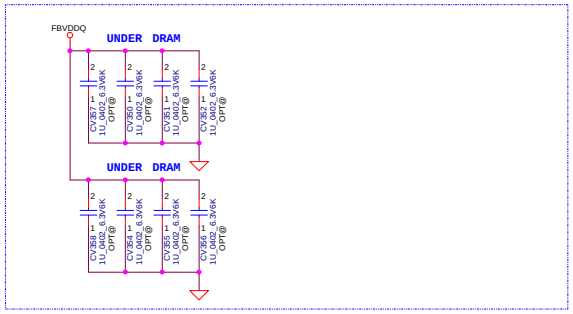


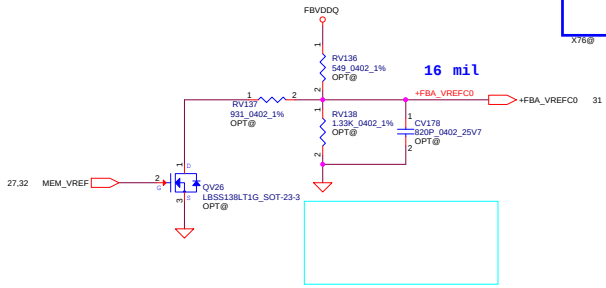
Follow DG

2A Peak 3A

Cost down list:
22U 2Pcs







GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Title: N17P-G1_VRAM A Lower

Size: Custom | Document Number: DY512 | Rev: 1.0

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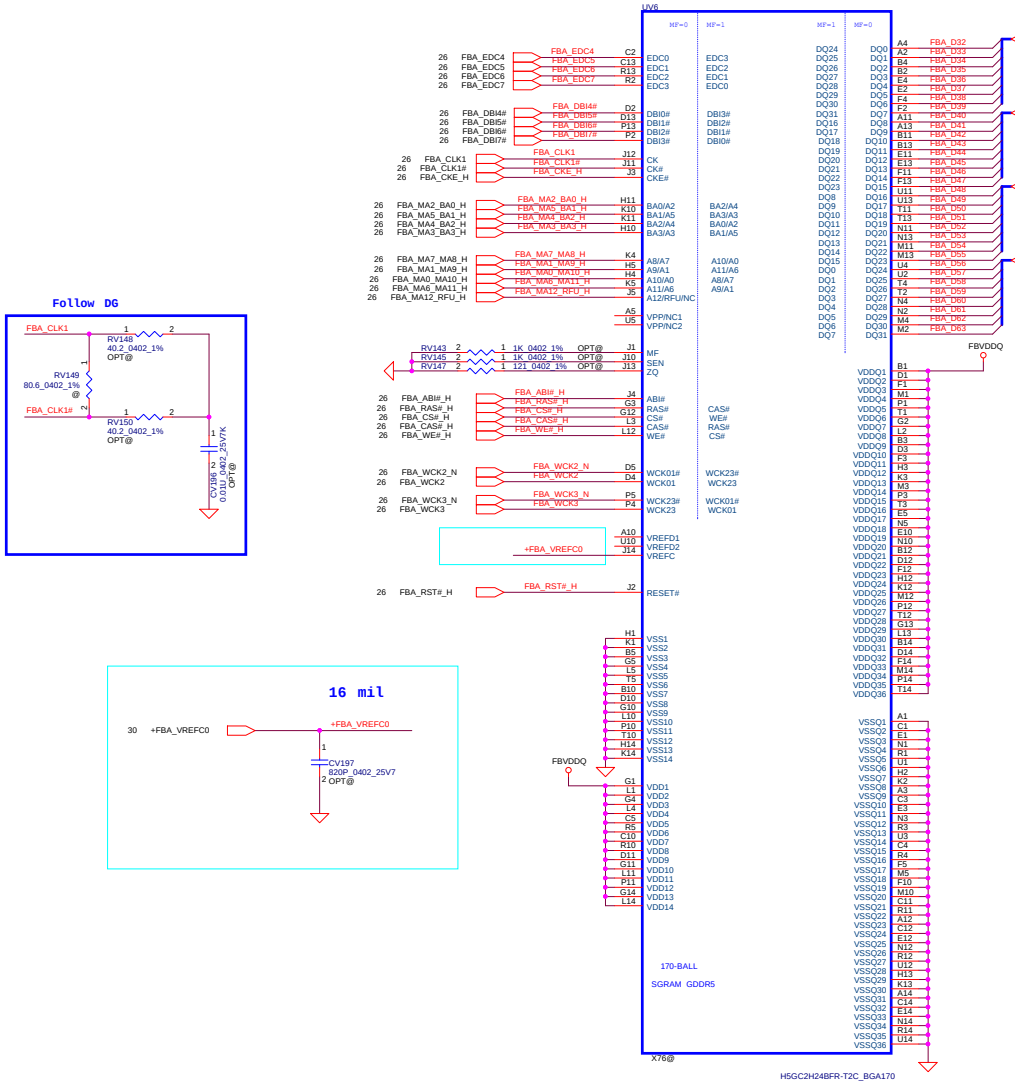
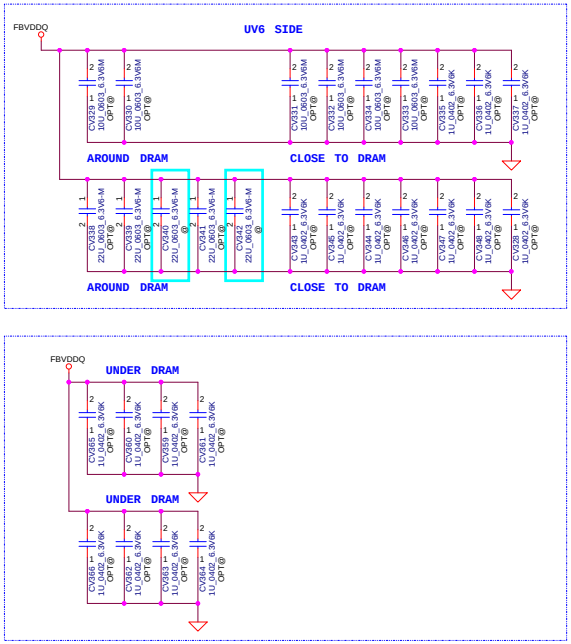
Memory Partition A- Upper 64 bits(MF=0)



2A Peak 3A Cost down list: 22U 2Pcs



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Title		
N17P-G1_VRAM A Upper		
Size: Custom	Document Number: DY512	Rev: 1.0
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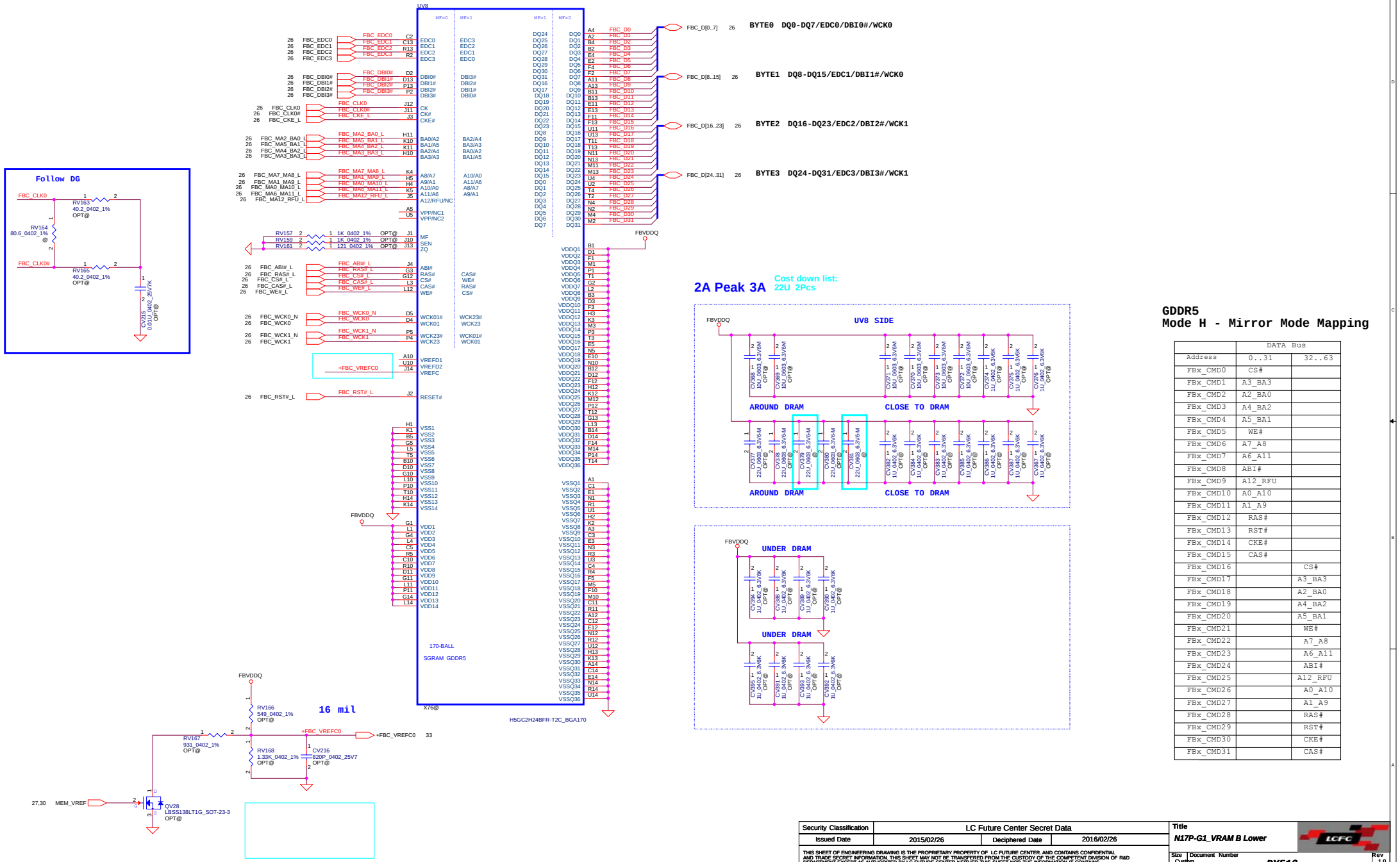
Memory Partition B - Lower 32 bits(MF=0)



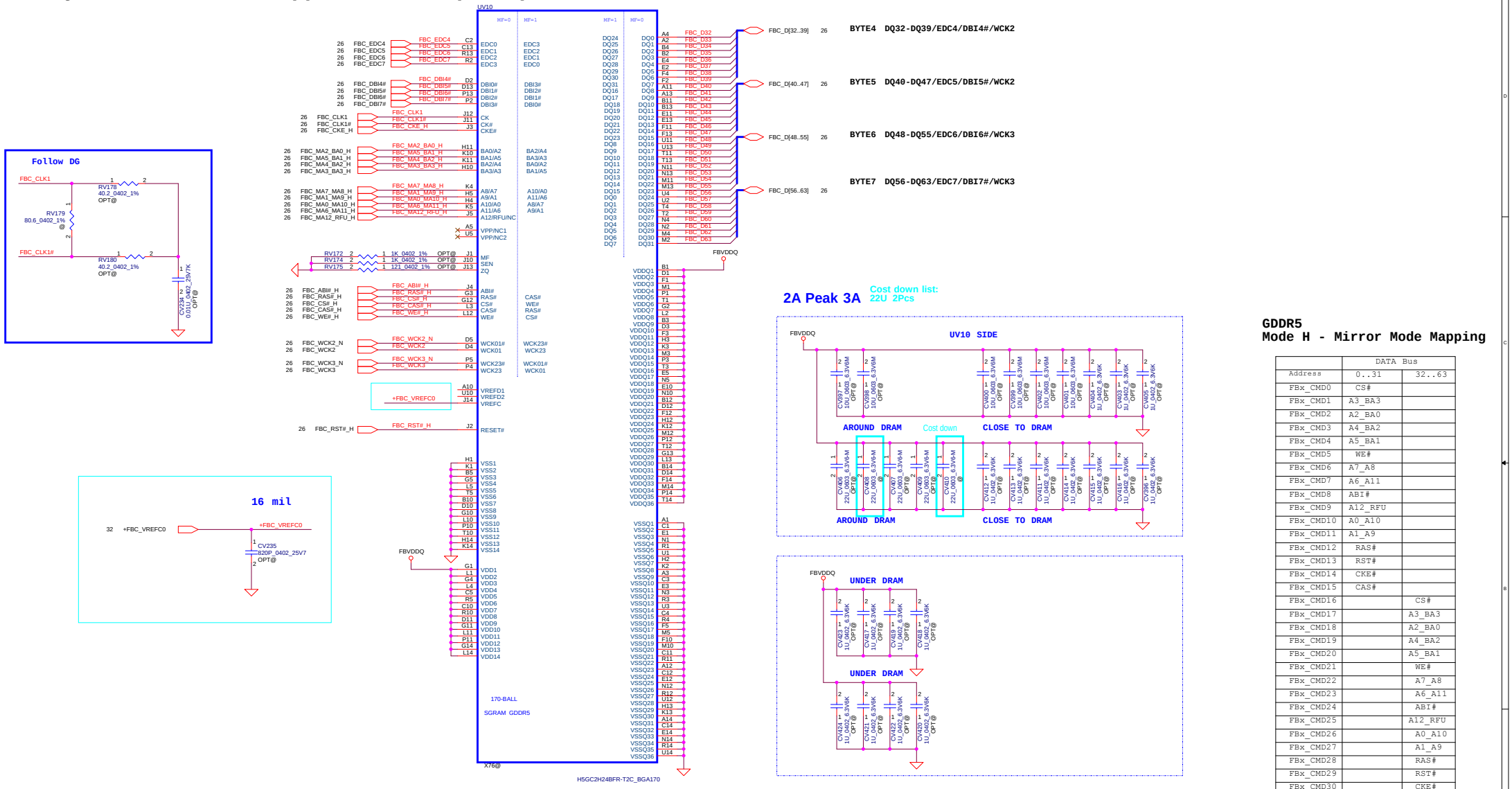
GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	N17P-G1_VRAM B Lower		
Size	Document Number		Rev
Custom	DY512		1.0
Date:	Friday, November 25, 2016	Sheet 32 of 75	

Memory Partition B - Upper 32 bits(MF=0)



2A Peak 3A

Cost down list:
22U 2Pcs

GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: N17P-G1_VRAM B Upper

Size: Custom | Document Number: DY512 | Rev: 1.0

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Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: ***Blank***

Size D	Document Number: ***DY512***	Rev 1.0
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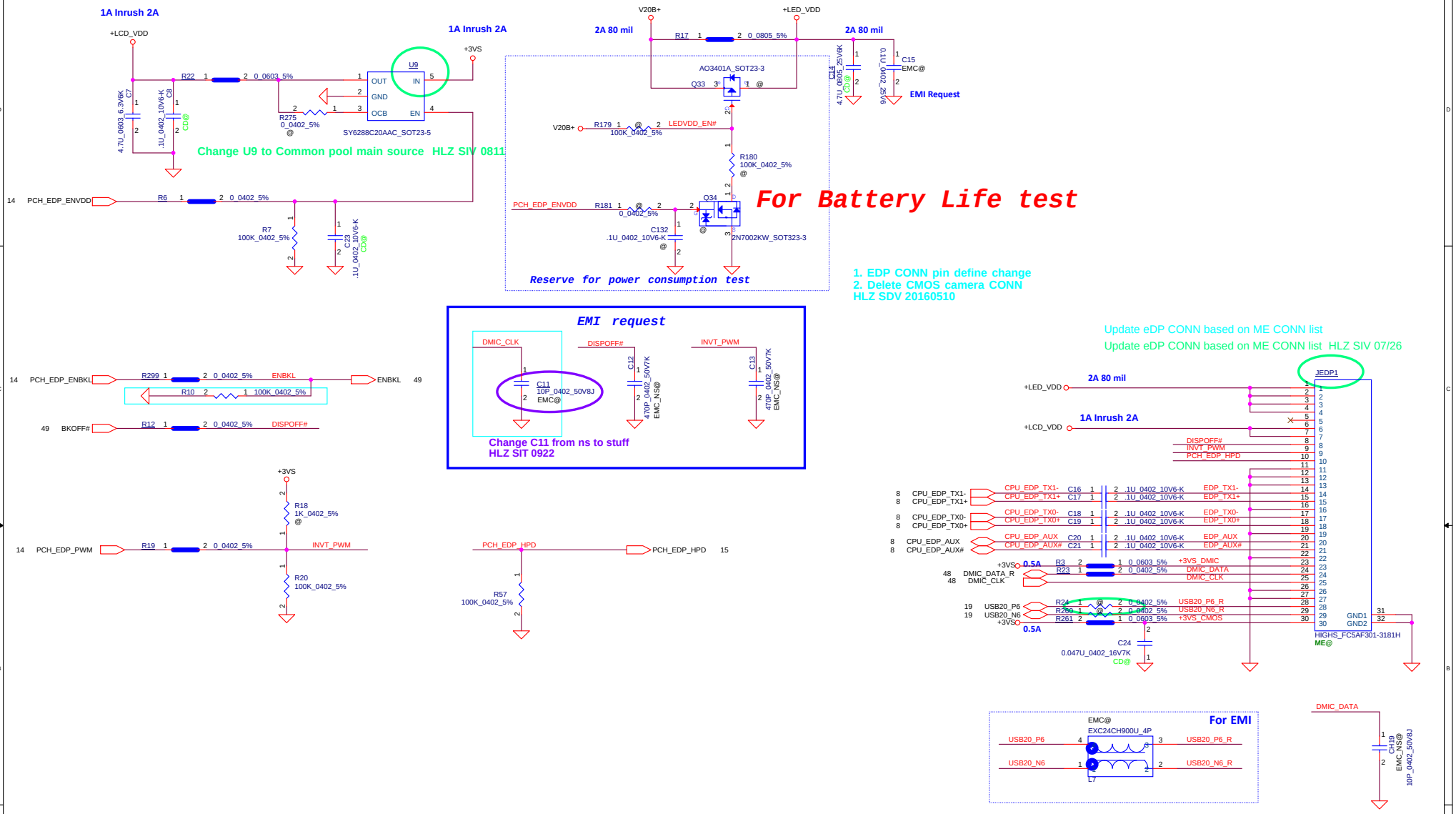
LCD POWER CIRCUIT



1. EDP CONN pin define change
2. Delete CMOS camera CONN
HLZ SDV 20160510

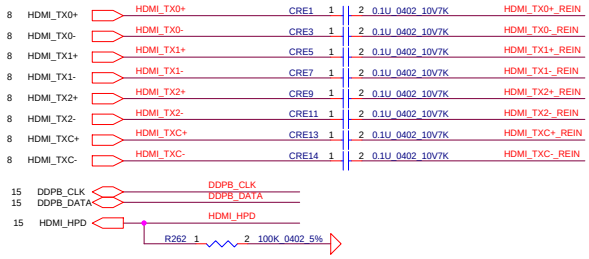
Update eDP CONN based on ME CONN list
Update eDP CONN based on ME CONN list HLZ SIV 07/26

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: eDP/ CMOS/Touch screen

Size	Document Number	Rev
Custom	DY512	1.0

Date: Friday, November 25, 2016 Sheet 35 of 75



	ISET
H	Increase +13%
L	default
M	Reduce -13%

	EQ
H	EQ for channel loss up to 4.3 dB
L	EQ for channel loss up to 12.4 dB
M	EQ for channel loss up to 8.6 dB

	PRE
H	1.6dB pre-emphasis
L	no pre-emphasis
M	2.5dB pre-emphasis

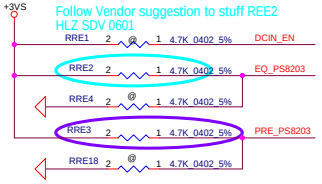
	DDCBUF
H	active DDC buffer with default threshold
L	default,passive DDC pass-through
M	active DDC buffer without default threshold

	I2C_CTL_EN
H	I2C control is selected
L	Pin control is selected

	CFG
H	HDMI ID enable
L	HDMI ID disable

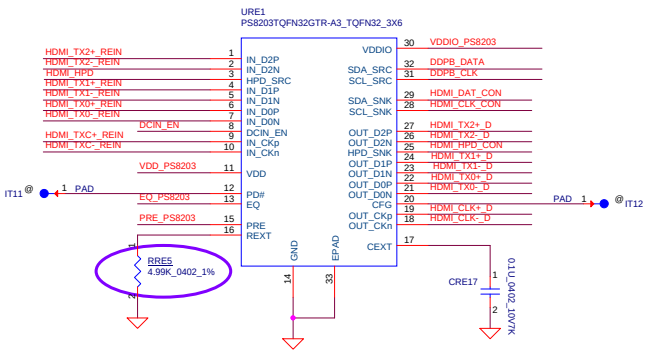
	DCIN_EN
H	DC coupling input
L	default,AC coupling input

	PD#
H	Normal operation
L	Chip power down



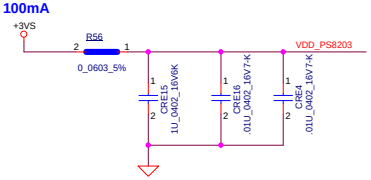
Change RRE3 from @ to stuff due to 4K*2K Eye-diagram fail
HLZ SIT 0920

HDMI Repeater

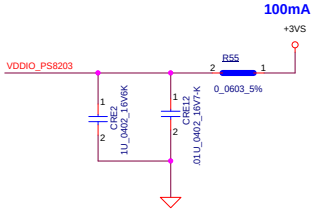


Change RRE5 from 5.9K to 4.99K due to 4K*2K Eye-diagram fail
HLZ SIT 0920

100mA

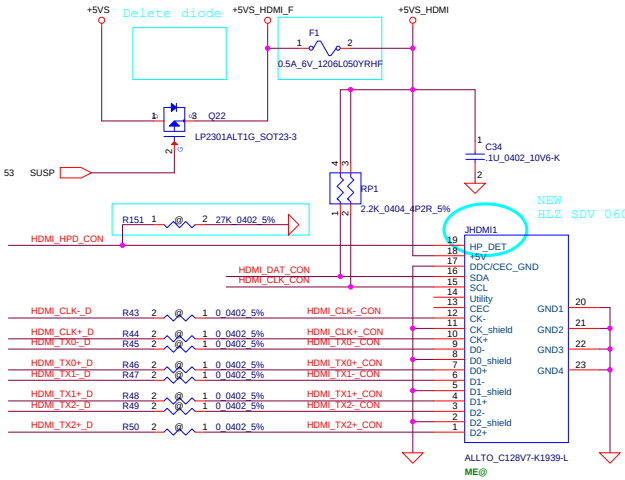


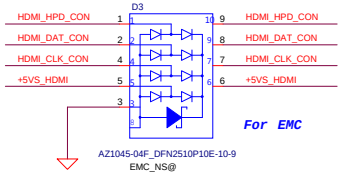
100mA

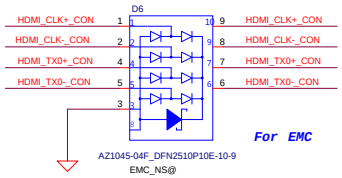


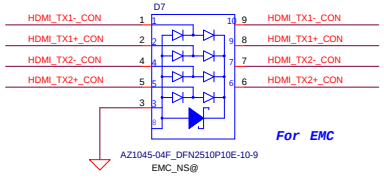
Modify HDMI fuse based on PUR requirement

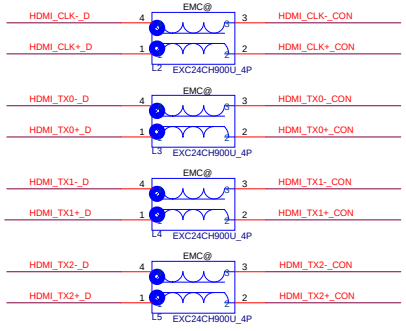
200mA 200mA



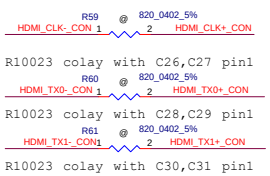








0427 Kerry Del Q25B



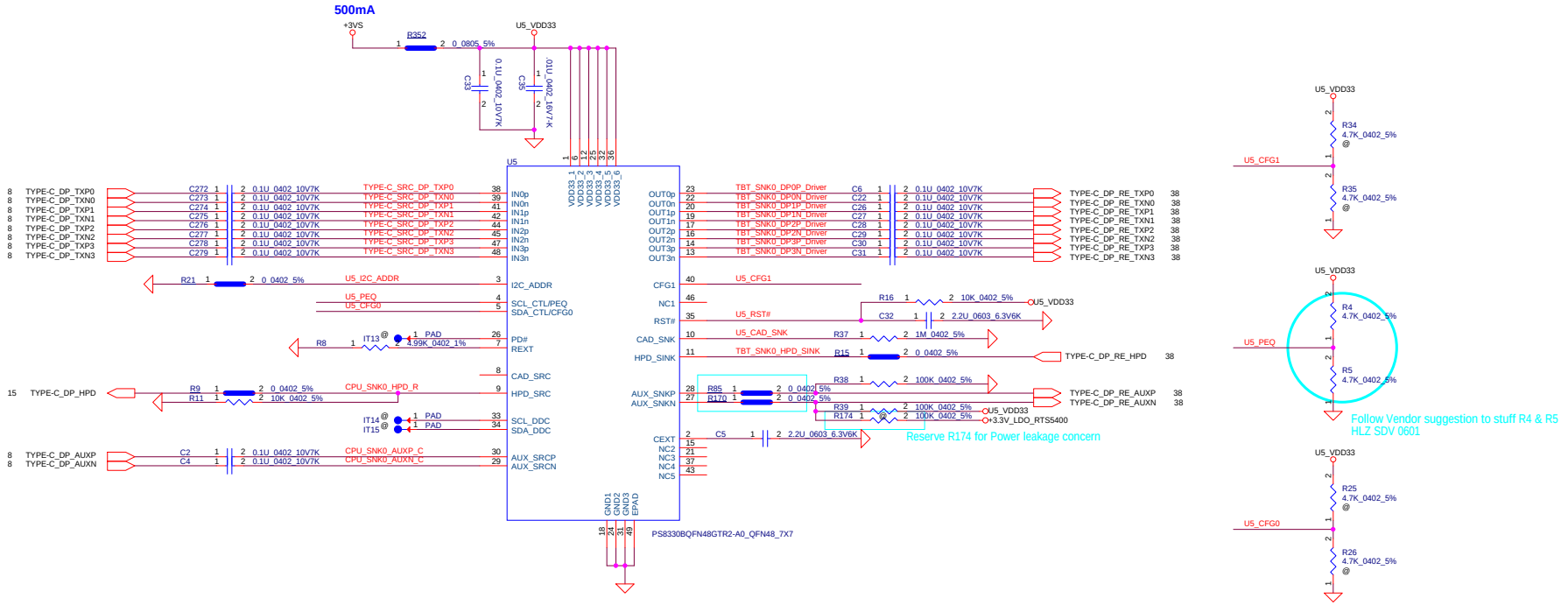
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: HDMI_CONN

Size	Document Number	Rev
C	DY512	1.0

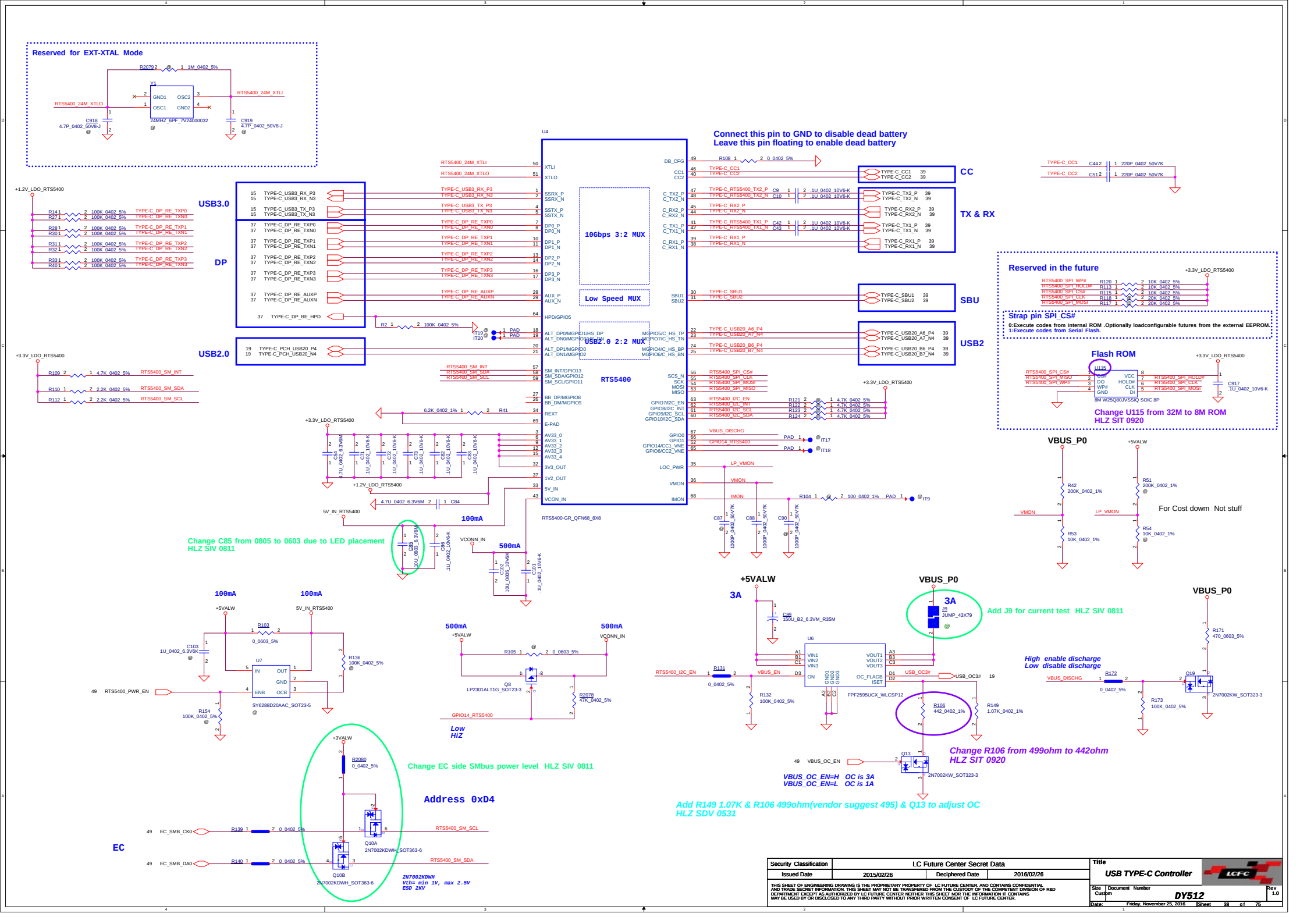
Date: Friday, November 25, 2016 Sheet 36 of 75

DP Redriver



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	DDI Redriver PS8330		
Size C	Document Number DY512		Rev 1.0
Date: Friday, November 25, 2016	Sheet 37 of 75		

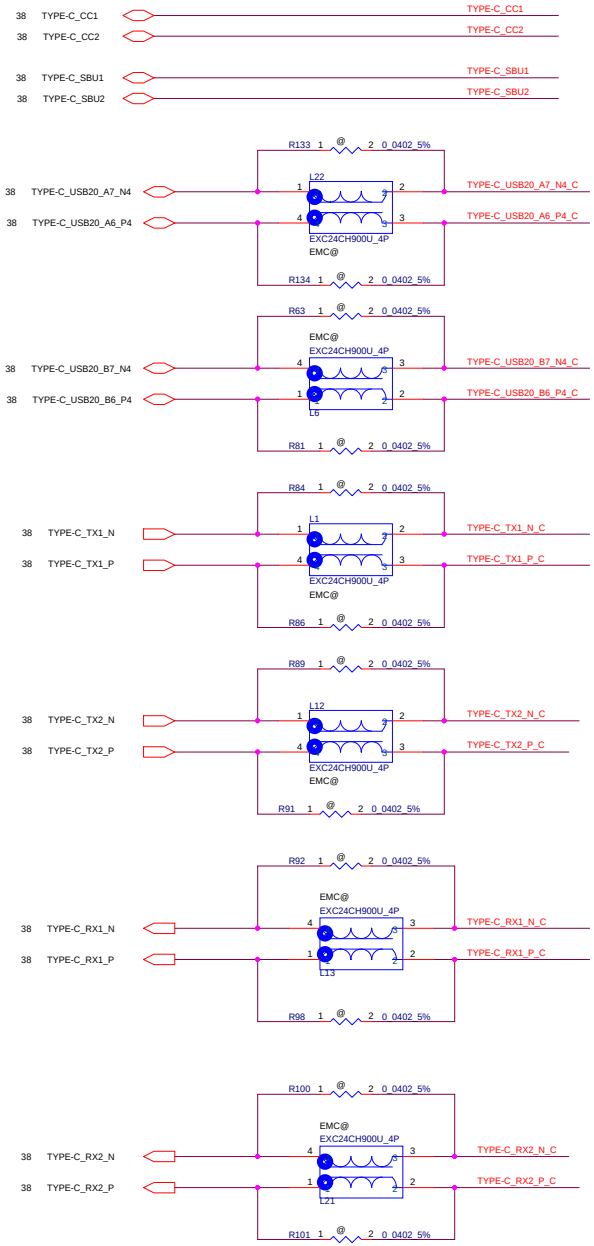


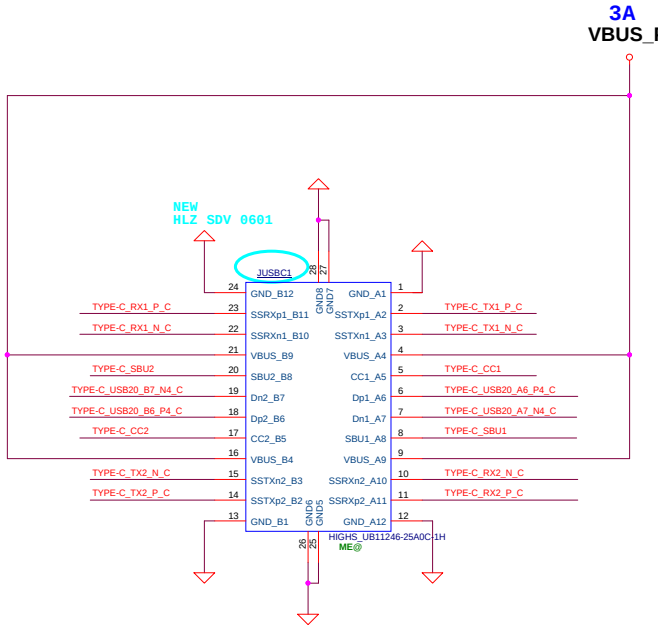
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

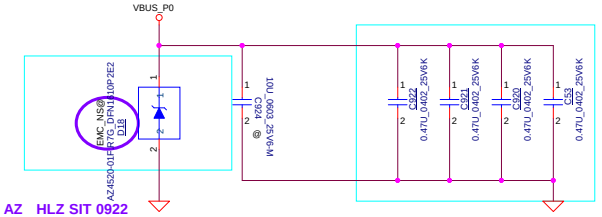
Title: USB TYPE-C Controller

Size: Custom | Document Number: DY512 | Rev: 1.0

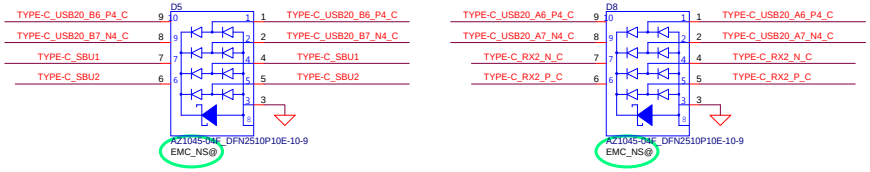
Date: Friday, November 25, 2016 | Sheet 38 of 75



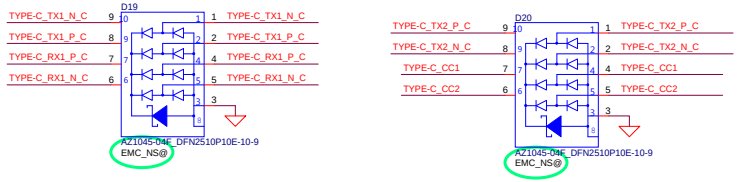




Change D18 from NXP to AZ HLZ SIT 0922
Change D18 from stuff to@ HLZ SIV 0811



Change D5&D8&D19&D20 from stuff to@ HLZ SIV 0811



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	USB TYPE-C Port		
Size C	Document Number DY512		Rev 1.0
Date: Friday, November 25, 2016	Sheet 39 of 75		

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title

USB TYPE-C Controller

Size	Document Number	Rev
Custom	***DY512***	1.0

Date: Friday, November 25, 2016 Sheet 40 of 75

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title

Anti-ghost KB

Size	Document Number	Rev
A3	***DY512***	1.0

Date: Friday, November 25, 2016 | Sheet 41 of 75

TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

LOGIC

TABLE : PCH ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

LOGIC

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

LOGIC

16 JTAGX — JTAGX — R591 1 — 2 0_0402_5% — XDP_TCK

16 PCH_TMS — PCH_TMS — R593 1 — 2 0_0402_5% — XDP_TMS

16 PCH_TDI — PCH_TDI — R594 1 — 2 0_0402_5% — XDP_TDI

22 CPU_TRST# — CPU_TRST# — R595 1 — 2 0_0402_5% — XDP_TRST#

16 PCH_TDO — PCH_TDO — R596 1 — 2 0_0402_5% — XDP_TDO

22 PCH_PRDY# — PCH_PRDY# — R657 1 — 2 0_0402_5% — XDP_PRDY#

22 PCH_PREQ# — PCH_PREQ# — R658 1 — 2 0_0402_5% — XDP_PREQ#

18 SPI_WP# — R597 1K_0402_1% @

Reference Intel document 546884 SKL PHG

Delete R93

PCH_TDI — R217 1 @ 2 0_0402_5% — TDI

PCH_TDO — R218 1 @ 2 0_0402_5% — TDO

VCCST — R168 51_0402_1% @ — R169 51_0402_1% @ — XDP_TMS — XDP_TDI

VCCST — R233 51_0402_1%

+3VALW — @ 1K_0402_5% R234

+1.0VALW — @ C70 0.1U_0402_25V6

16 PCH_TCK — R99 1 @ 2 0_0402_5% — R219 1 @ 2 0_0402_5% — PAD 1 — @ IT21

6 XDP_TCK

PCH_TMS — R220 1 @ 2 0_0402_5%

6 XDP_TMS — R221 1 @ 2 0_0402_5% — PAD 1 — @ IT22

6 XDP_TDI — R222 1 @ 2 0_0402_5% — TDI — PAD 1 — @ IT23

6 XDP_TRST# — R223 1 @ 2 0_0402_5% — PAD 1 — @ IT24

6 XDP_TDO — R224 1 @ 2 0_0402_5% — TDO — PAD 1 — @ IT25

16 SYS_RESET# — R225 1 @ 2 1K_0402_5% — PAD 1 — @ IT26

18,27,43,45,49,50 PLT_RST# — R226 1 @ 2 1K_0402_5% — PAD 1 — @ IT27

16,49 PCH_PWROK

16,49 SYS_PWROK — R228 1 @ 2 0_0402_5% — PAD 1 — @ IT29

EC_RSMRST# — R229 1 @ 2 1K_0402_5% — PAD 1 — @ IT30

16,49 EC_RSMRST#

6 CFG3 — R230 1 @ 2 0_0402_5% — PAD 1 — @ IT31

6 XDP_PRDY# — R231 1 @ 2 0_0402_5% — PAD 1 — @ IT32

6 XDP_PREQ# — R232 1 @ 2 0_0402_5% — PAD 1 — @ IT33

R322 1K_0402_1% @

Change XDP CONN to Test Point
HLZ SVD 0527

+3VS

* GPP_B18_NO_REBOOT
0 = Disable "No Reboot" mode. (Default)
1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

R563 1K_0402_5% @ Place near PCH

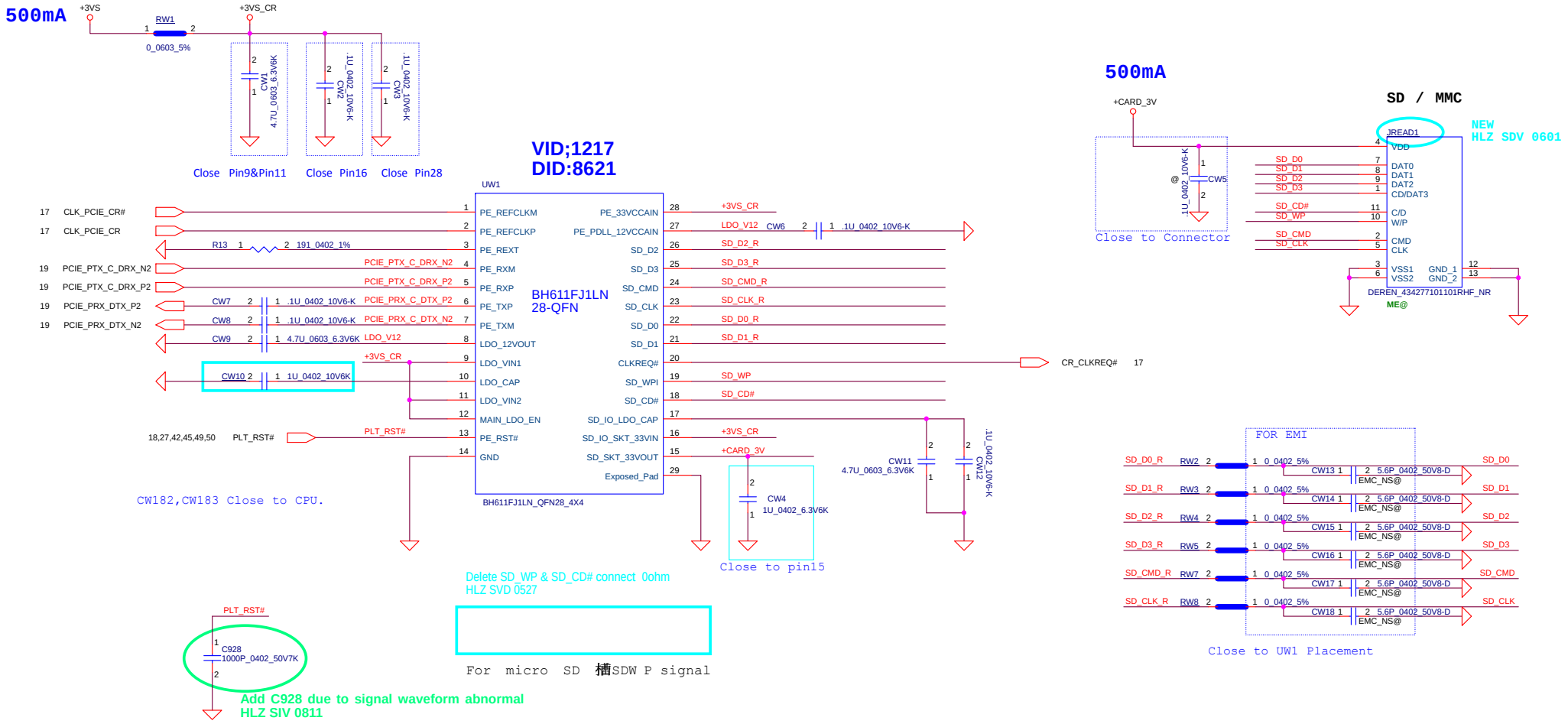
GPP_B18_NO_REBOOT — GPP_B18_NO_REBOOT 20

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: XDP

Size: Custom | Document Number: DY512 | Rev: 1.0

Date: Friday, November 25, 2016 | Sheet 42 of 75

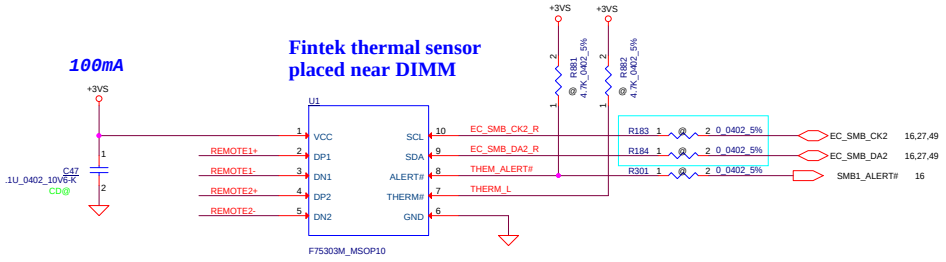


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2016/02/26

Title: **Card Reader**

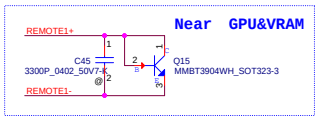
Size	Document Number	Rev
Custom	DY512	1.0

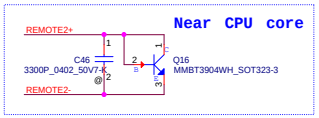
Date: Friday, November 25, 2016 Sheet 43 of 75

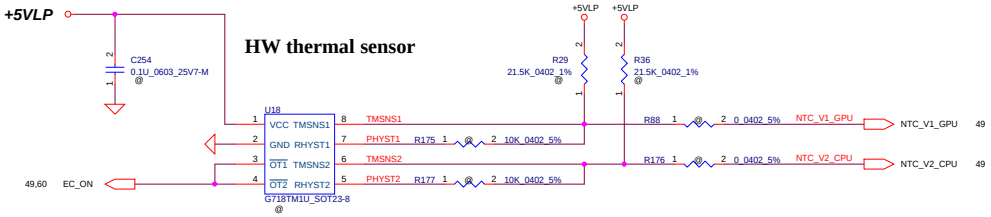


Address 1001_101xb

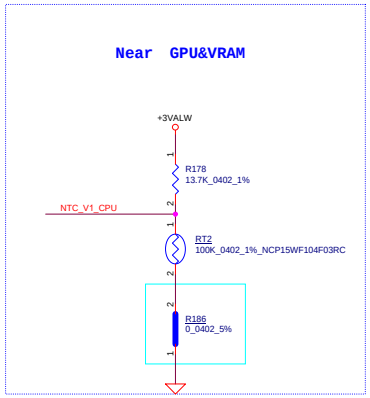
REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

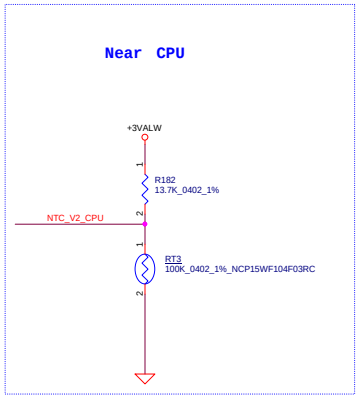




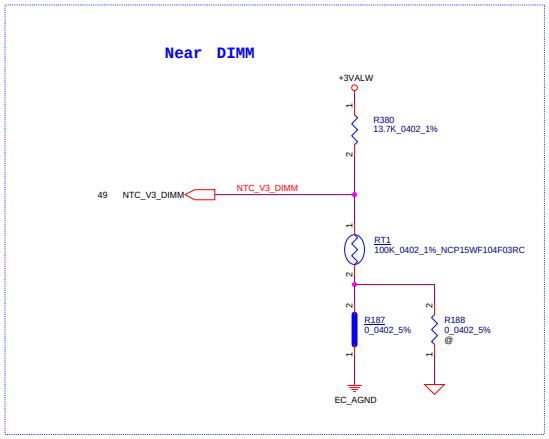


over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C





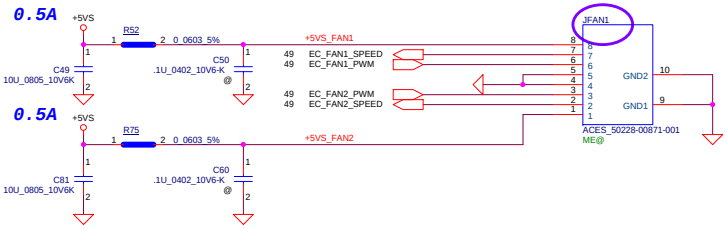
for layout optimized, change the EC_AGND to GND



FAN Conn

Update FAN CONN based on ME SDV CONN list

Update FAN CONN based on ME SIT CONN list



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: Thermal sensor/FAN CONN

Size: Custom | Document Number: DY512 | Rev: 1.0

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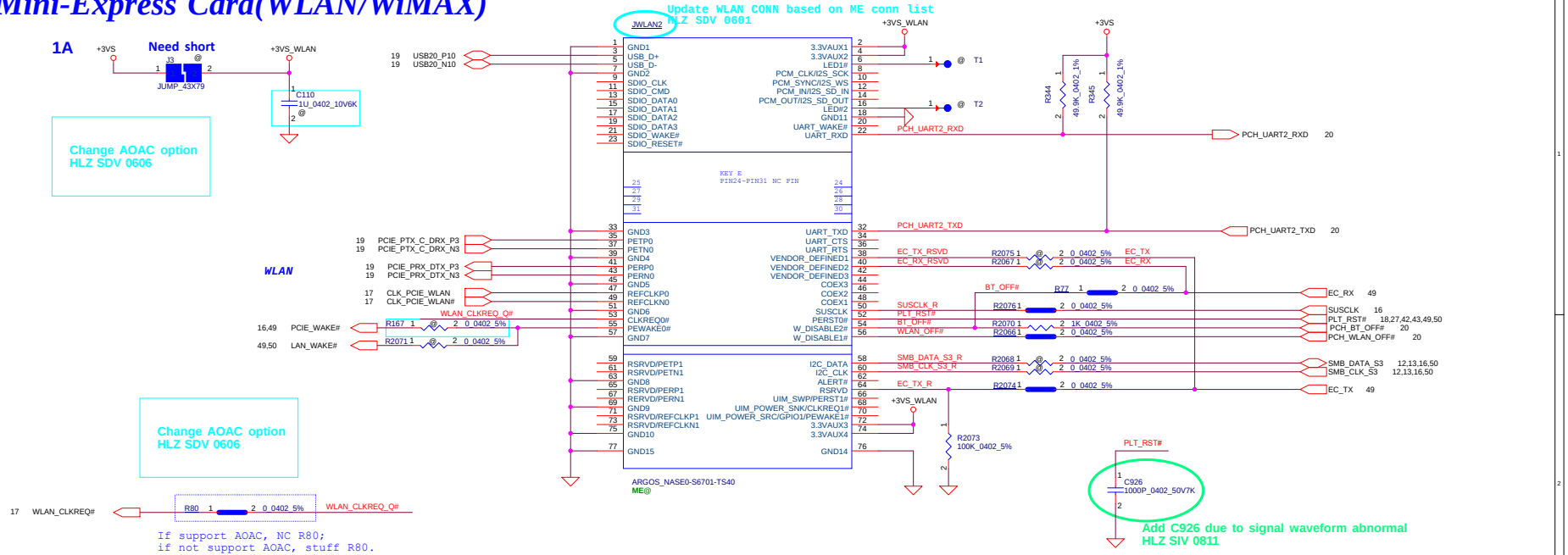
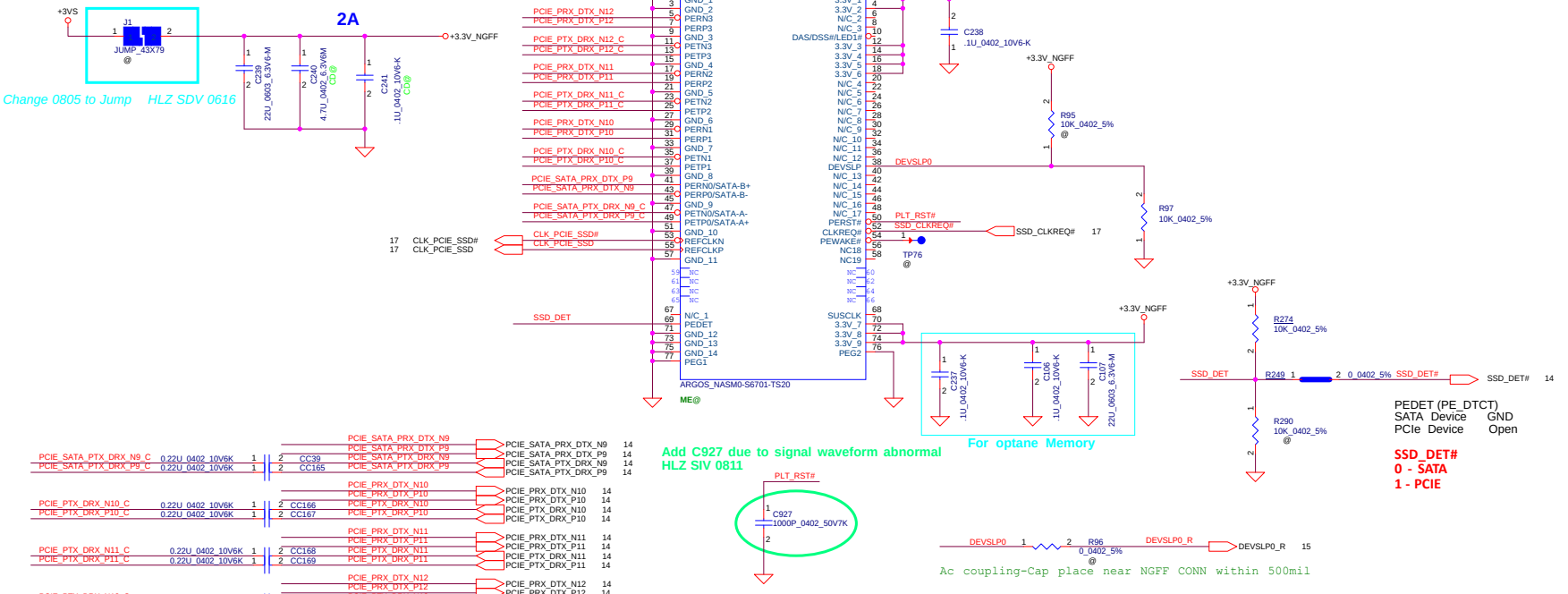
Mini-Express Card(WLAN/WiMAX)



M.2 SSD(SATA/PCIE)



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: **NGFF WLAN**

Size	Document Number	Rev
Custom	DY512	1.0

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Delete C74&C75&C76&C77&C78
HLZ SIT 0922

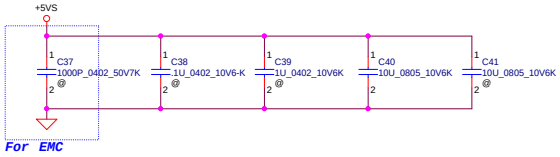
Reserved

SATA HDD Cable

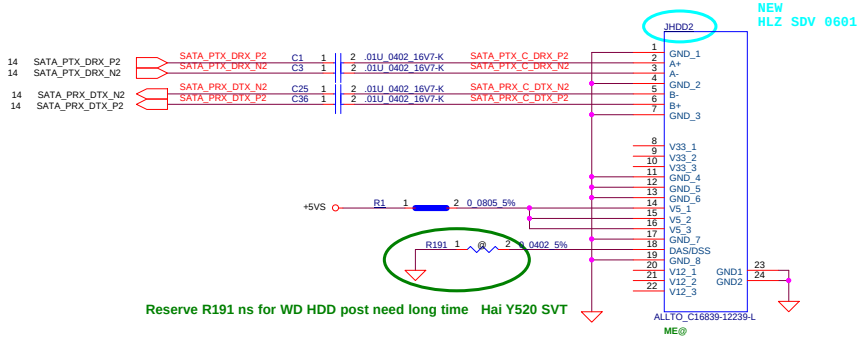
Delete C66&C67&C68&C69&R342&JHDD1
HLZ SIT 0922

SATA HDD Conn.

1A



NEW
HLZ SDV 0601



Reserve R191 ns for WD HDD post need long time Hai Y520 SVT

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: HDD/XBOX CONN

Size	Document Number	Rev
C	DY512	1.0

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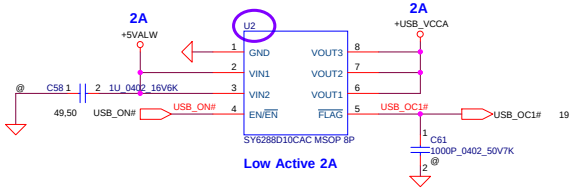
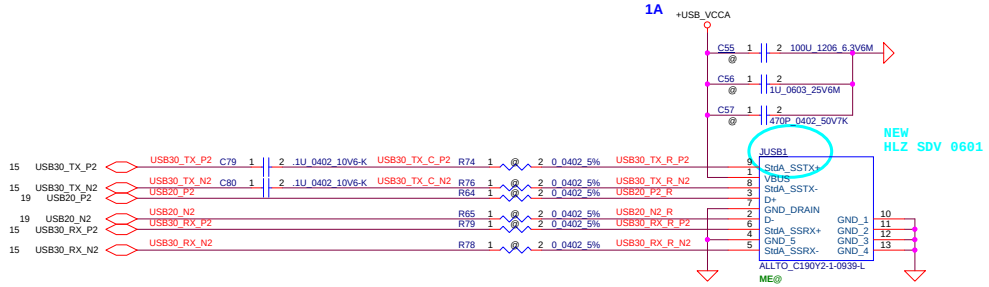
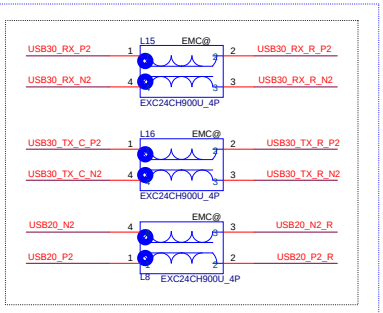
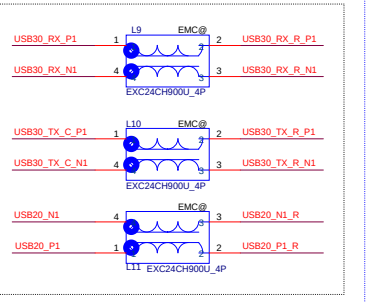
LEFT SIDE USB3.0 PORT X2



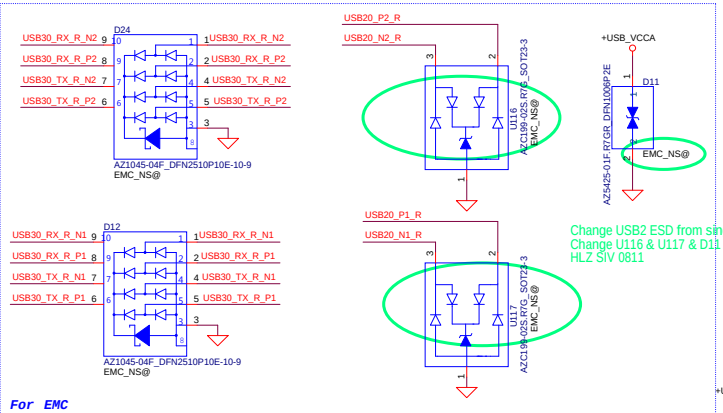
Change USB3.0 PWR SW from BCD to SILERGY due to BCD will EOL
HLZ SIT 0920





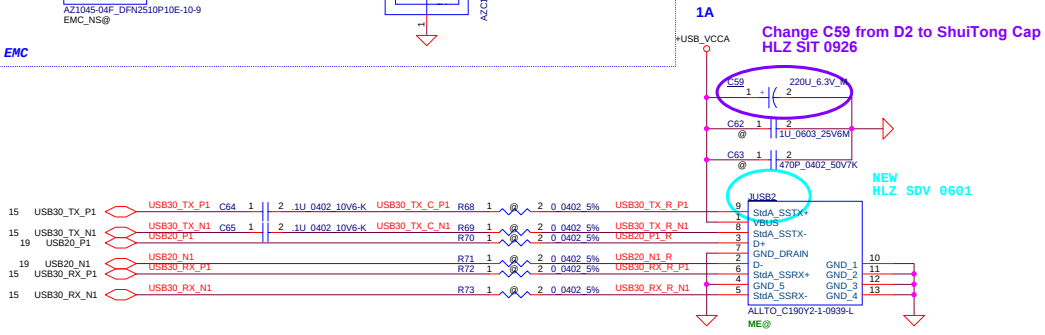


For EMC



Change USB2 ESD from single to 2in1
Change U116 & U117 & D11 from stuff to @
HLZ SIV 0811

For EMC



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: **USB2.0/USB3.0 PORT (LEFT)**

Size	Document Number	Rev
C	DY512	1.0

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100mA

Y700 A+A is 1.5V

100mA

100mA

Y700 A+A is 1.5V

2A

60ohm@100Mhz 1.7A

Change CH269 from ns to stuff
HLZ SIT 0922

Trace width is 70mils

Change RA1&RA2 from 49ohm to 75ohm
HLZ SIT 0928

Trace width is 10mils

ALC3248

Delete MONO-OUT & CODEC_WF_MUTE# signal
HLZ SDV 0603

To solve the background noise while combojack connecting to an active speaker and system entry into S3/S4/S5 without analog power.

Change SPK CON from 5pin to 4pin HLZ SDV 0615

Update SPK CONN based on ME SIT CONN list HLZ SIT 0922

80ohm@100Mhz 2.3A

Trace width is 30mils

2W

Bead modify symbol

Follow Y700 A+A

Delete SPK ESD

For EMI

Change RA7&CA8 from @ to stuff due to power noise test fail
HLZ SIV 0611

For EMI

Delete WF AMP
HLZ SDV 0603

PC-BEEP

STUFF for power consumption test
2015/07/06 ADD

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

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Title	Codec_CX20752	
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For EMI

For SPI ROM Mirror

Close EC

All capacitors close to EC

For Cost down

minimum trace width 12 mil

Reserved Cap HLZ SDV 0616

change CE1 from @ to stuff due to signal waveform abnormal
HLZ SIV 0811

change GPB5 from PCHCMOSP to PCH_PWR_EN
HLZ SIV 0811

IT8226E-128/BX
LQFP128

Change CHG_MOD1 to RTS5400_PWR_EN
HLZ SDV 0613

Change to NTC_V1_GPU & NTC_V2_CPU
HLZ SDV 0613

Change CHG_MOD2 to NTC_V3_DIMM
HLZ SDV 0613

Change CHG_MOD3 to VBUS_OC_EN
HLZ SDV 0531

Add SMBUS0 for RTS5400
HLZ SIV 0811

IT34 DEL 0727

Add SMBUS0 for RTS5400
HLZ SIV 0811

Change SUSACK# from GPF2 to GPF7
HLZ SIV 0811

Change USB_CHG_EN to SYSON_VDDQ
HLZ SDV 0531

Mount RE30 Reserve for VGA_AC_DET

Delete AOAC_ON#
HLZ SDV 0606

Delete EC_WF_MUTE#
HLZ SDV 0531

Change RE30 to 0ohm jump

Clear CMOS issue

Delete 2nd RTCRST#
HLZ SDV 0606

Unmount QE3,QE4,RE99,RE50 by Intel request

For factory EC flash

same net name with PCH

when mirror, GPG2 pull high
when no mirror, GPG2 pull low

Reserved Cap HLZ SDV 0616

Delete MOS

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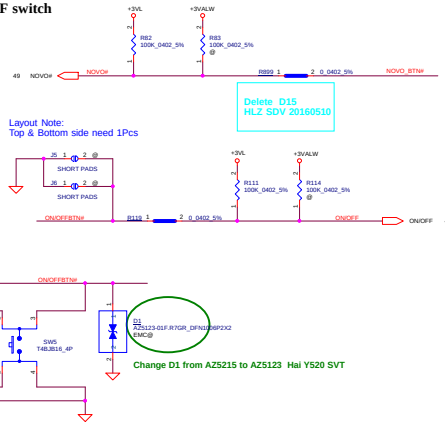
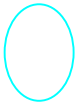
ON/OFF switch



NOVO Button

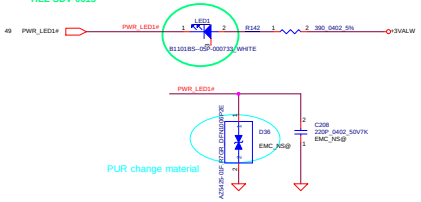


change NOVO button from MB to DB
HLZ SDV 20160510

PWR LED

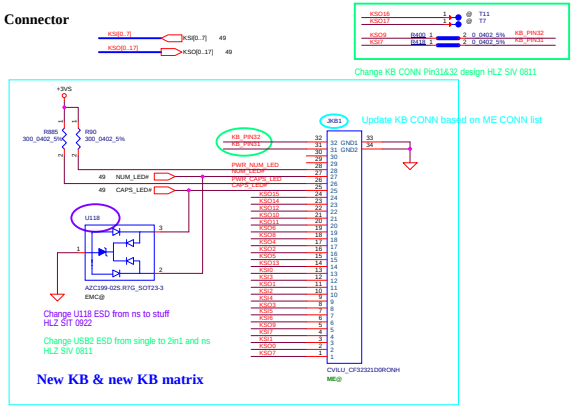
Chnage LED HLZ SDV 0615

Chnage LED value from B1101BS--05P-000233_WHITE to B1101BS--05P-000733_WHITE
HLZ SDV 0615

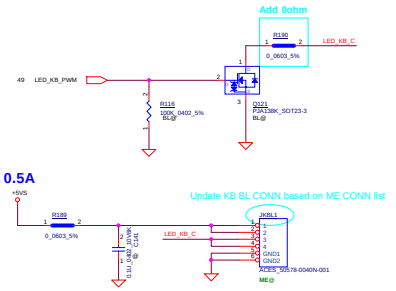


PUR change material

K/B Connector

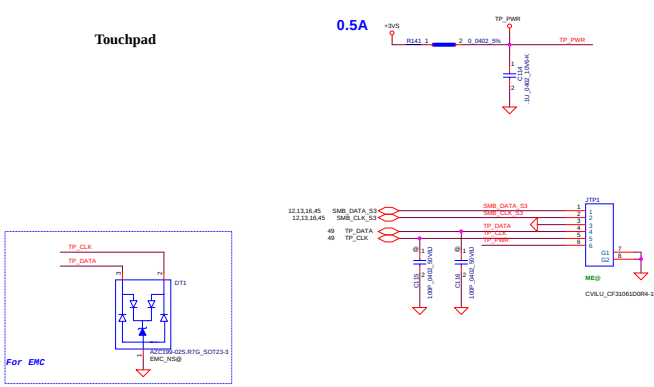


K/B BL Connector

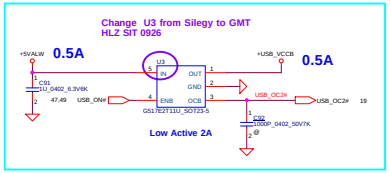


R116 & R190 & Q121 & R189 add KB_BL BOM structure
HLZ SIT 0920

Touchpad

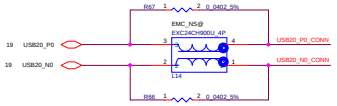


Change U3 from Silegy to GMT
HLZ SIT 0926



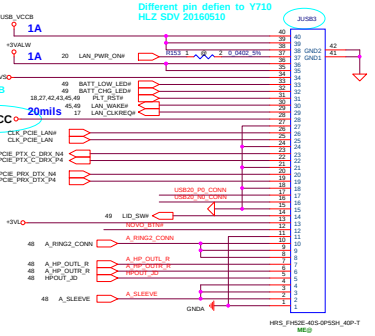
Change U3 from USB charger to Power SW
HLZ SDV 20160510

Right Side USB2.0 Port X 1 (USB/B)



USB I/O Connector

Different pin defien to Y710
HLZ SDV 20160510



Modify RTC battery from MB to DB
HLZ SDV 0615

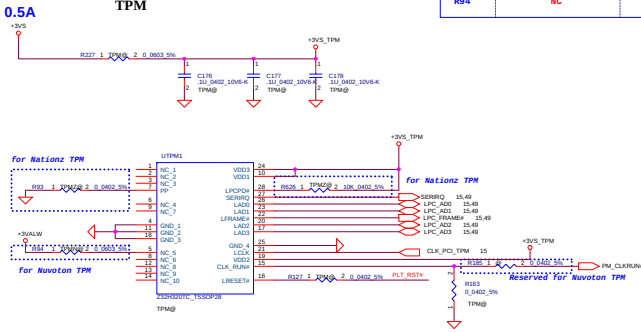
	pin number	6	7	8	4
	pin name	CTL1	CTL2	CTL3	ILM_SEL
Charge port Pin5 Enable H for all	S0 CDP	1	1	1	1
	S3 DCP	0	1	1	0/1
	S4/S5 DCP	0	0	1	0/1
Normal port Pin5 Enable H for S0/S3 L for S4/S5	S0 SDP1	1	1	0	0/1
	S3 SDP1	0	1	0	0/1
	S4/S5 Disable	0	0	0	0/1

SDP2 (No Discharge from/to CDP)
SDP1(Discharge from/to any charging state including CDP)

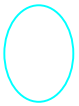
1. Add R93 for NationZ TPM
2. Add R94 & +3VALW for Nuvoton TPM
3. Add R163 PD & R185 for PM_CLKRUN# of Nuvoton TPM
HLZ SIT 0920

	Nationz TPM	Nuvoton TPM
R626	Stuff	NC
R93	Stuff	NC
R94	NC	Stuff

TPM

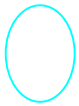


LID Hall Sensor

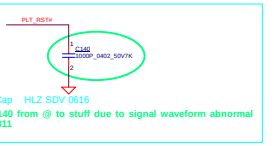


Change Hall Sensor from MB to DB
HLZ SDV 20160510

3D Camera



Delete 3D camera
HLZ SDV 20160510



Reserved Cap HLZ SDV 0616
Change C140 from @ to stuff due to signal waveform abnormal
HLZ SIV 0811

Security Classification	LC Future Center Secret Data		
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Title	KBD/PWR/IO/LED/TP Conn.		
Size D	Document Number DY512		Rev 1.0
Date: Friday, November 25, 2016	Sheet 50 of 75		

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title

ITE8371LQFP

Size	Document Number	Rev
C	***DY512***	1.0

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Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title

RGB KBD LED CONN

Size	Document Number	Rev
A2	DY512	1.0

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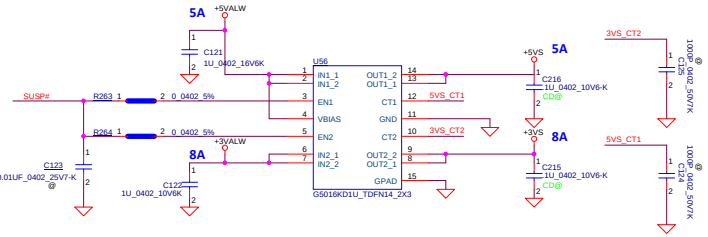
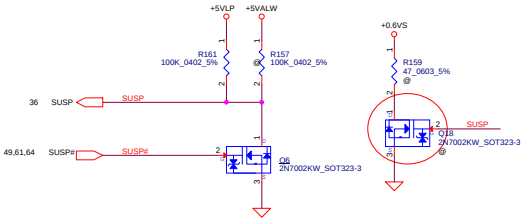
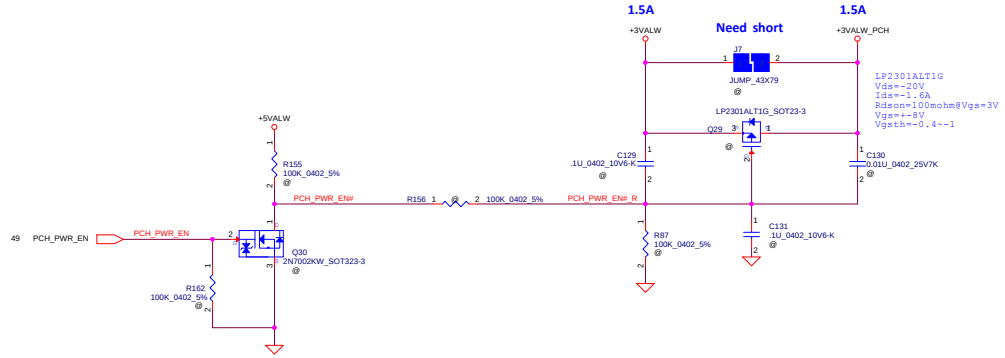
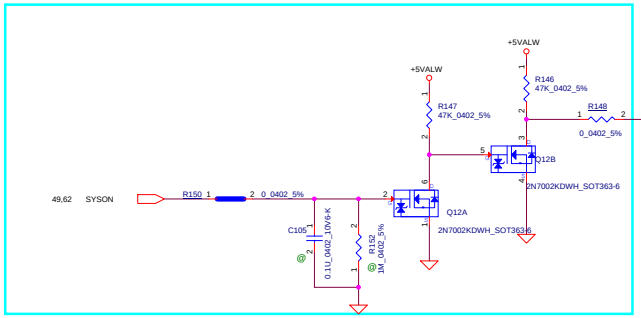
+5VALW to +5VS

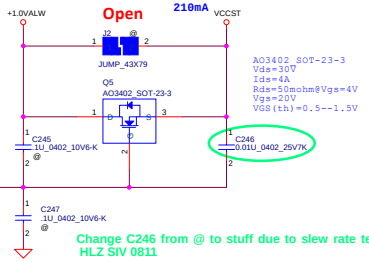




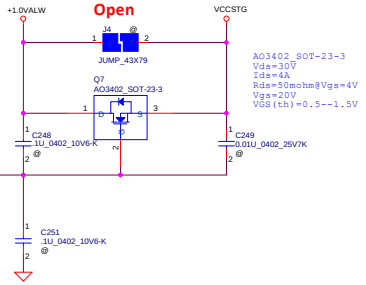


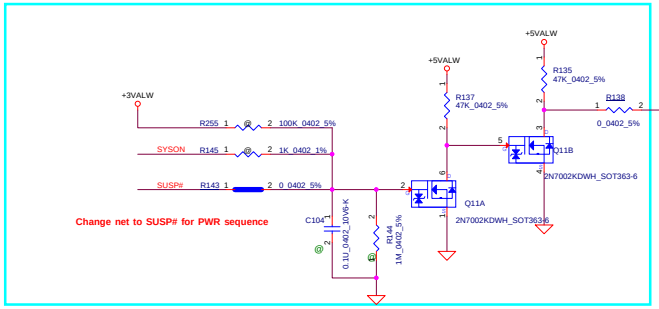
Add VCCST & VCCSTG Level shift
HLZ SDV 20160530





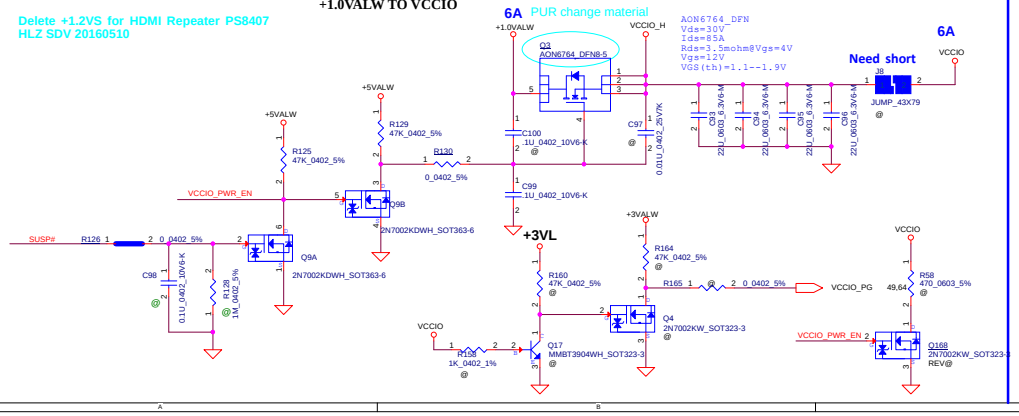
Change C246 from @ to stuff due to slew rate test fail
HLZ SIV 0811





+1.0VALW TO VCCIO

Delete +1.2VS for HDMI Repeater PS8407
HLZ SDV 20160510



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: DC V TO VS INTERFACE

Size: Custom | Document Number: DY512 | Rev: 1.0

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Title

Virtual symbol

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Custom	***DZ510/DY512***	1.0

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H2 HOLEA
H19 HOLEA
H1 HOLEA
pad_r6p4x8p0d2p8-offl0p8
pad_r6p4x6p5d2p8-offl0p8
pad_r6p4x8p0d2p8-offl0p8

Update footprint name HLZ SDV 0615

H3 HOLEA
H4 HOLEA
pad_C6p0d3p2
PAD_ST8P0CB8P0D2p5

Update H3 footprint name HLZ SIT 0923

Update footprint name HLZ SDV 0616

H7 HOLEA
pad_st6p0cb6p0d2p5

H8 HOLEA
H9 HOLEA
pad_st8p0cb6p0d2p5
pad_st8p0cb6p0d2p5

H17 HOLEA
H20 HOLEA
pad_shapet8p0x8p0cb8p0d2p5
pad_cb6p0d2p5

Delete H10 HLZ SDV 0618

Delete H11 HLZ SDV 0615

H5 HOLEA
H6 HOLEA
pad_o2p5x3p5d2p5x3p5n
pad_o2p5x3p5d2p5x3p5n

H12 HOLEA
H13 HOLEA
H14 HOLEA
H15 HOLEA
H16 HOLEA
pad_c4p0d4p0n
pad_c4p0d4p0n
pad_c4p0d4p0n
pad_c4p0d4p0n
pad_c4p0d4p0n

H18 HOLEA
PAD_C2P5D2P5N

FD1 FD2 FD3 FD4 FD5 FD6

For USB3 shielding Clip

Delete SH1 SH2 SH3 SH4 SH5 SH6 0726

For DDR4 shielding Clip

SH7 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P
SH8 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P
SH9 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P
SH10 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P
SH11 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P
SH12 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P
SH13 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P
SH14 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P
SH15 ME@ SHIELDING_SUL-35A2M_9P2X3P3_1P

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: Hole

Size B	Document Number DY512	Rev 1.0
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Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: ***Blank***

Size D	Document Number: ***DY512***	Rev 1.0
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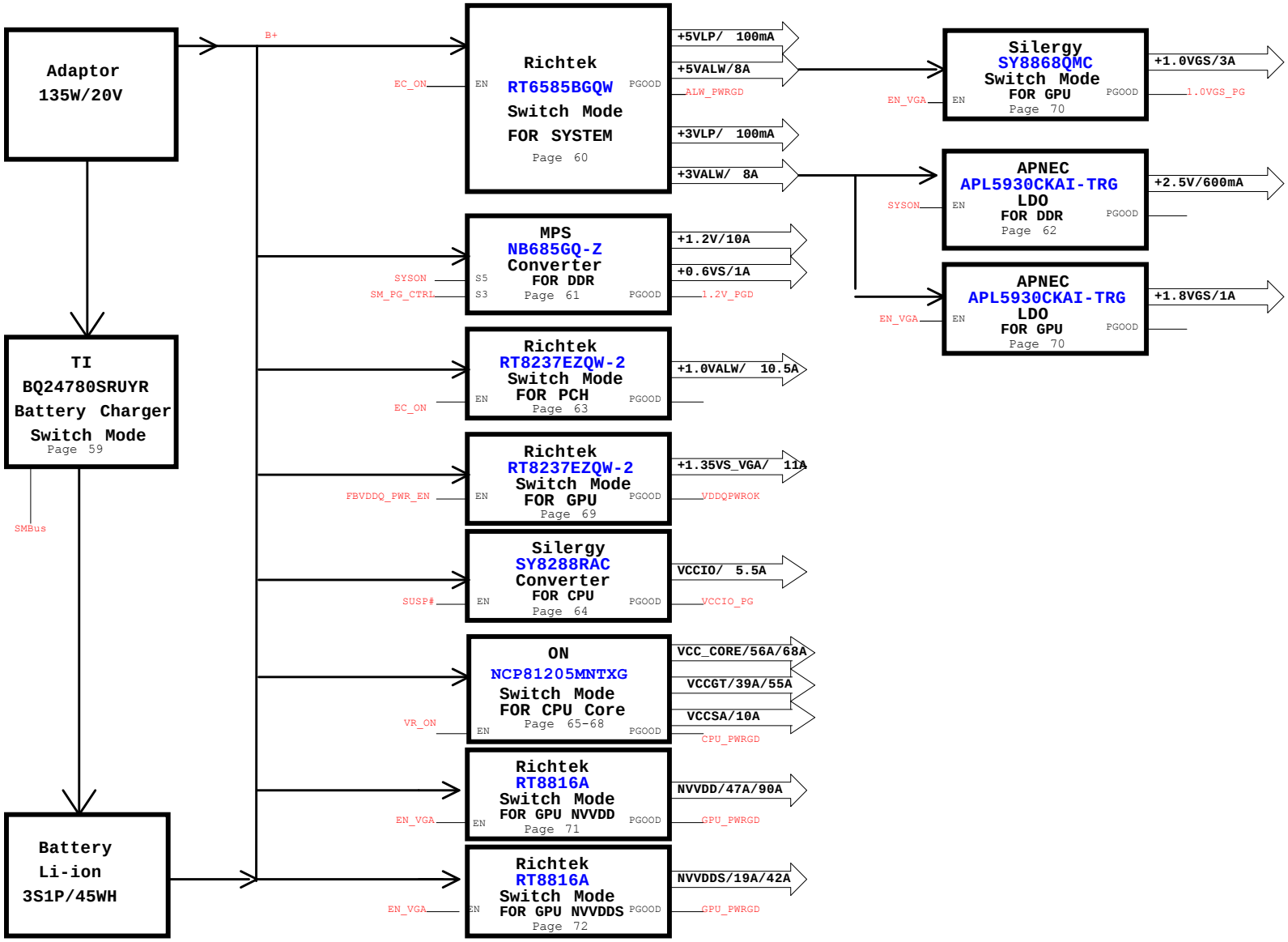

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: **Power Diagram**

Size	Document Number	Rev
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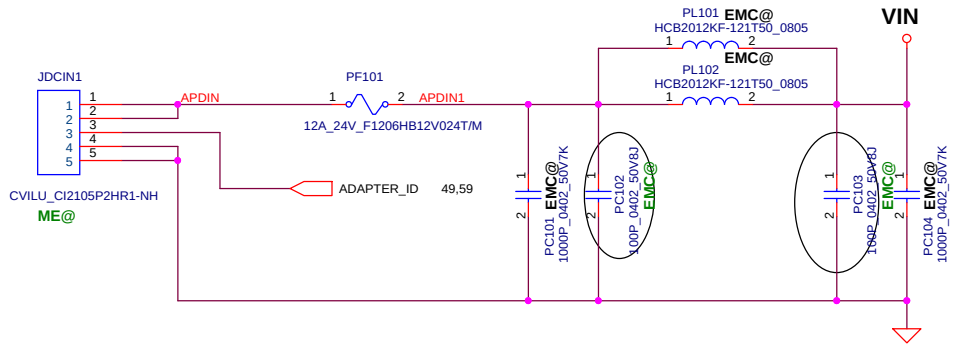
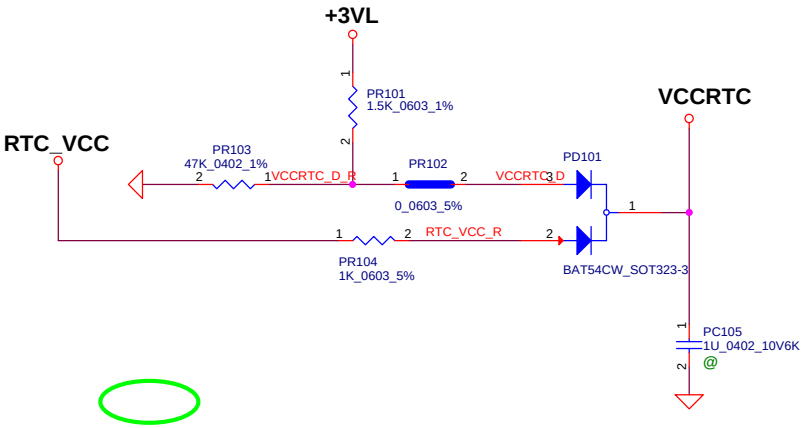
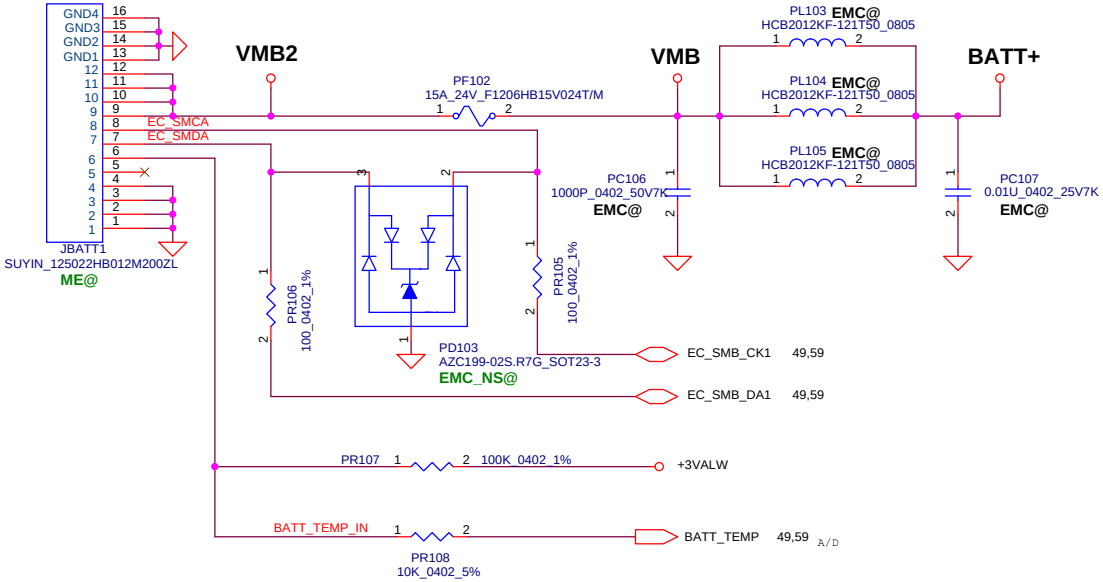




Chnage JPTC1 based on ME CONN list
HLZ SDV 0530

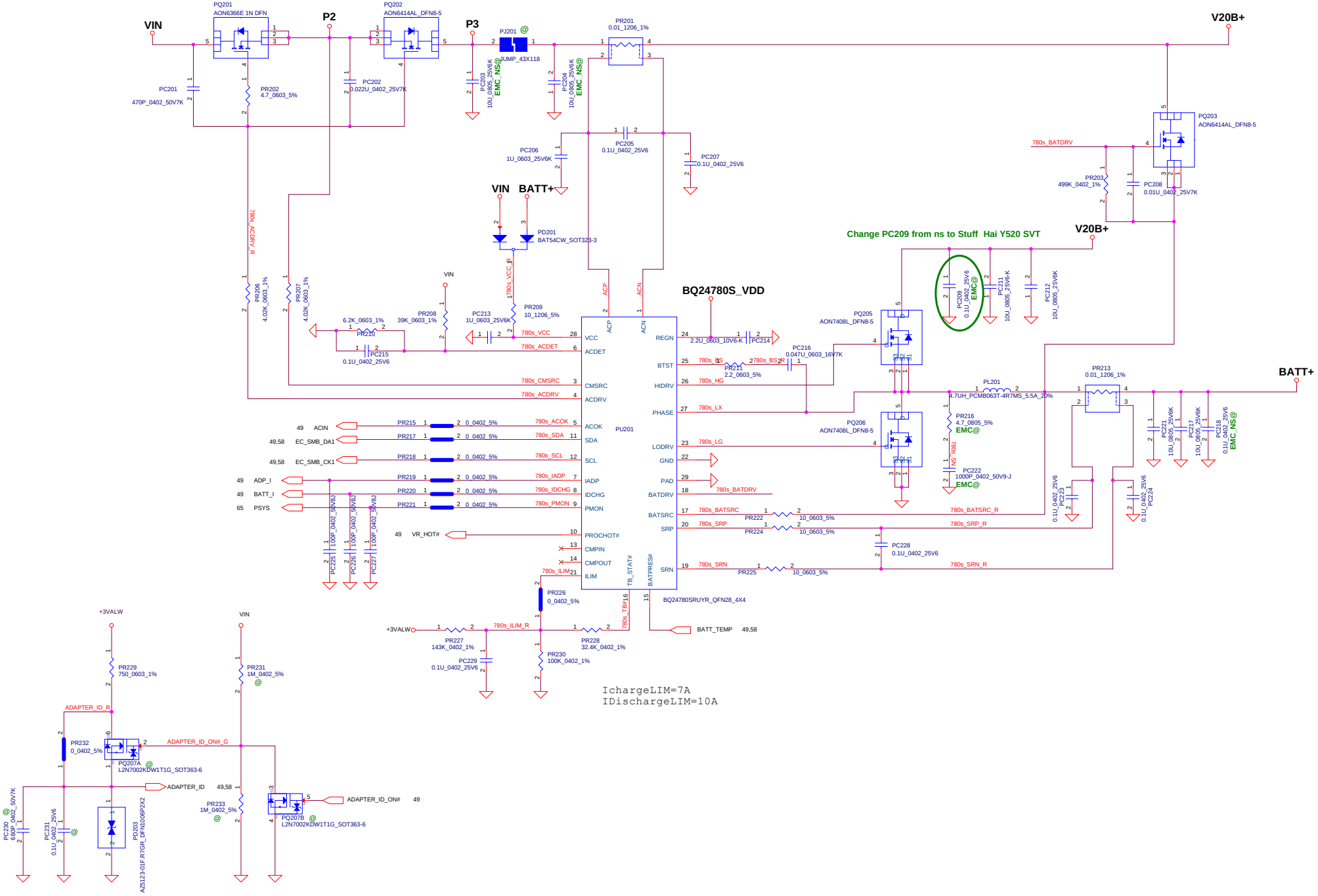
Chnage RTC battery from MB to DB HLZ SDV 0615



Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

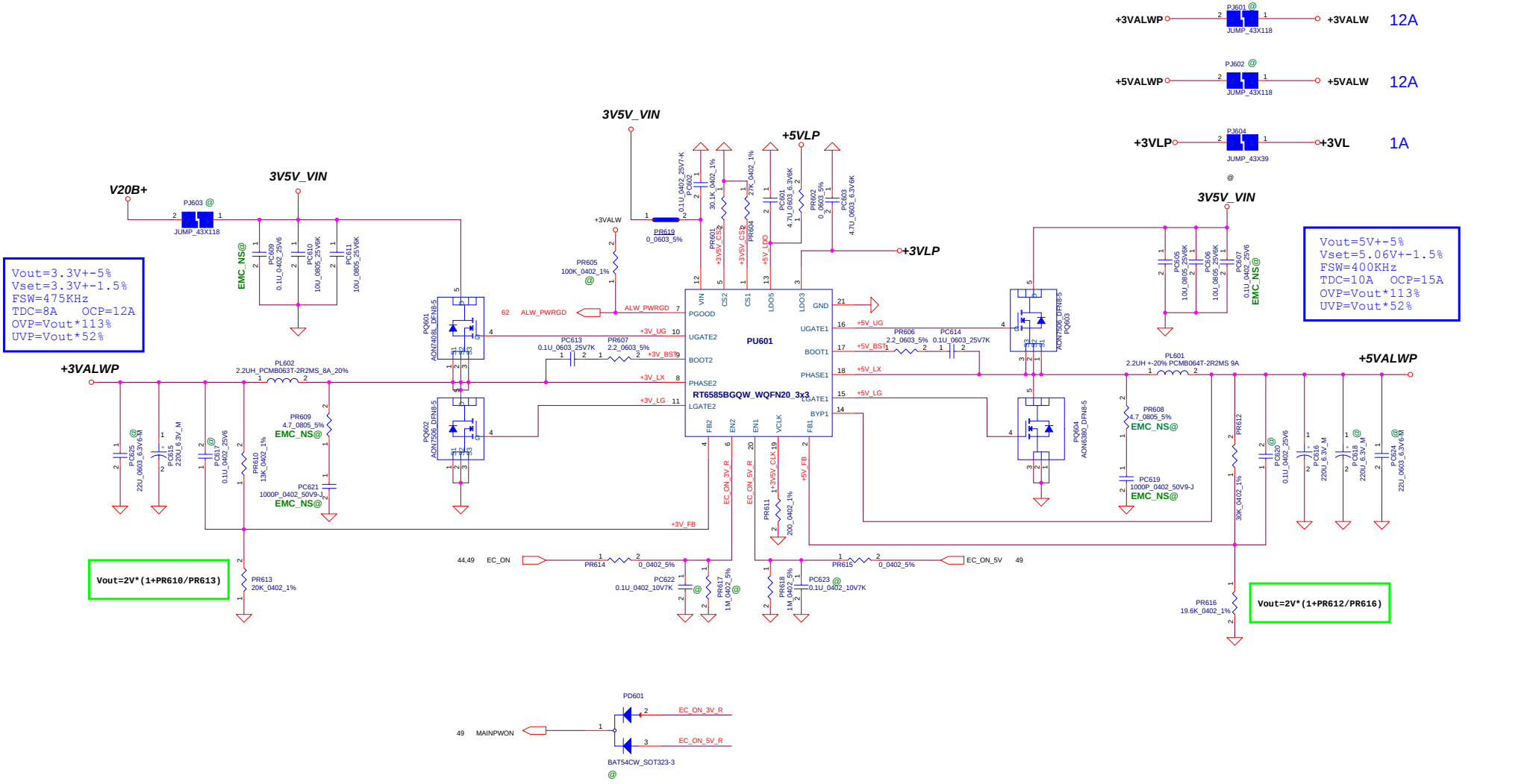
Title: **PWR-DCIN/BATT/RTC**

Size: Custom	Document Number: DZ510/DY512	Rev: 1.0
Date: Friday, November 25, 2016	Sheet 58 of 75	



Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title	PWR-charger		
Size: Custom	Document Number: DZ510/DY512		Rev: 1.0
Date: Friday, November 25, 2016	Sheet 59 of 75		



Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

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Title: PWR-3/5VALW

Size	Document Number	Rev
C	DZ510/DY512	1.0

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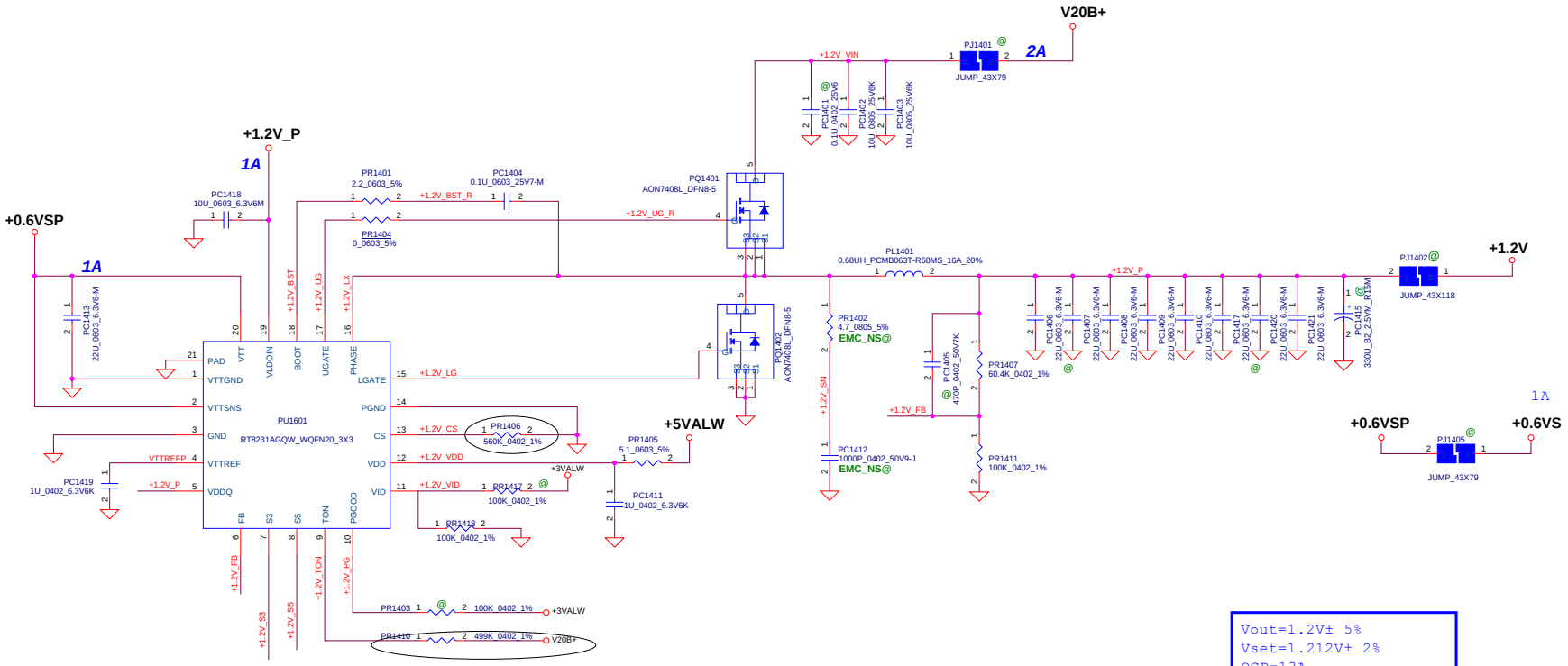

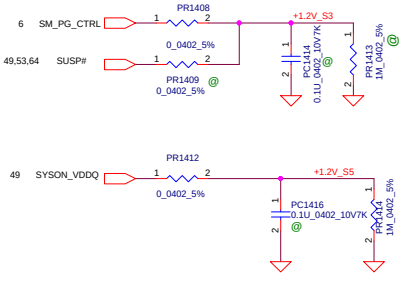

Vout=1.2V± 5%
Vset=1.212V± 2%
OCP=13A
Vref=0.6V
OVP=(1.25~1.35)*Vref
UVP=(0.7~0.8)*Vref
Fsw=700Khz(Rmode=0)
Fsw=500Khz(Rmode=150K)

Vout=0.6V± 5%
OCP=1.5A
VTT=1/2VDDQ

STATE	EN1	EN2	VDDQ	VTT_REFP	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off

Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: PWR-VDDQ/VTT

Size	Document Number	Rev
C	DZ510/DY512	1.0

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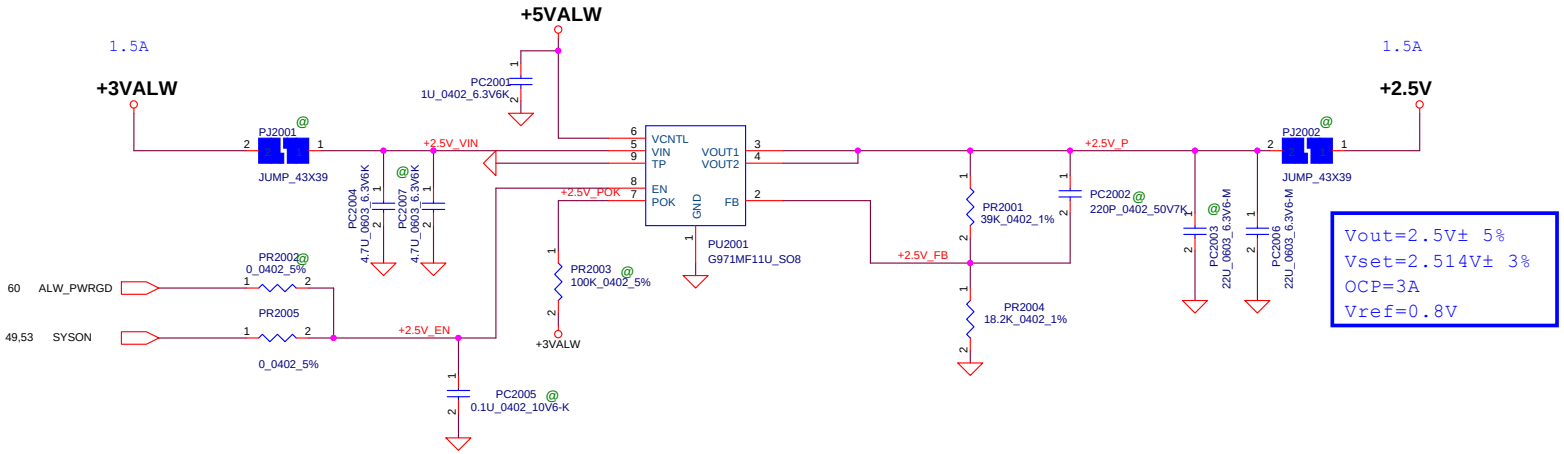

Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: PWR-2.5V

Size	Document Number	Rev
Custom	DZ510/DY512	1.0

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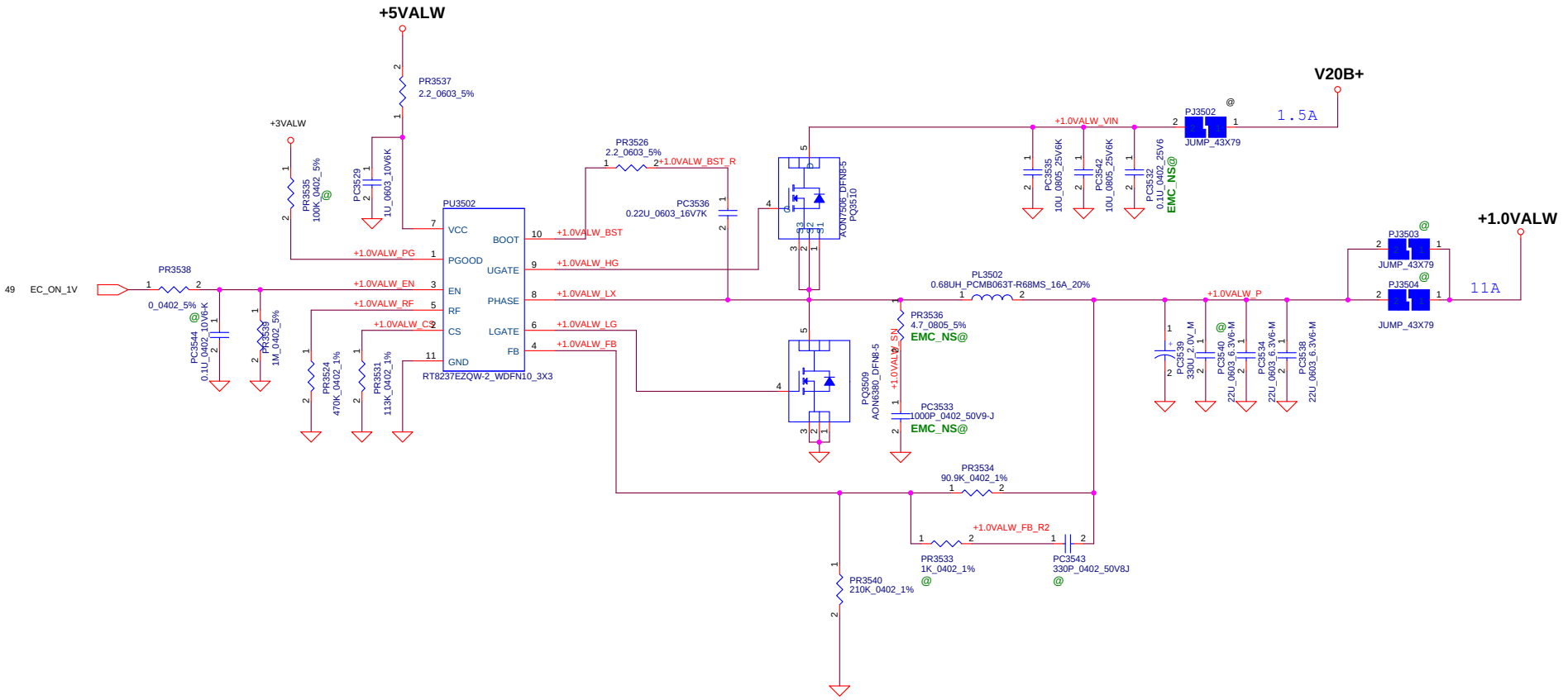

Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: **PWR-1VALW**

Size	Document Number	Rev
Custom	DZ510/DY512	1.0

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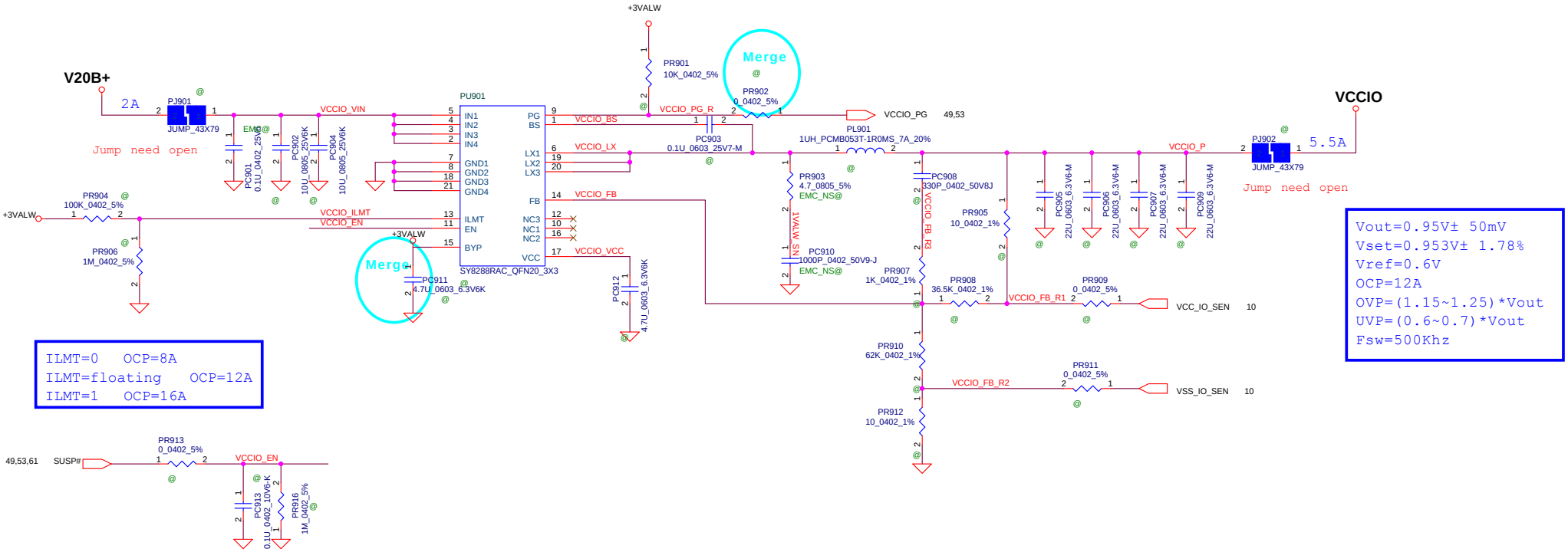

Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: **PWR-VCCIO**

Size	Document Number	Rev
Custom	DZ510/DY512	1.0

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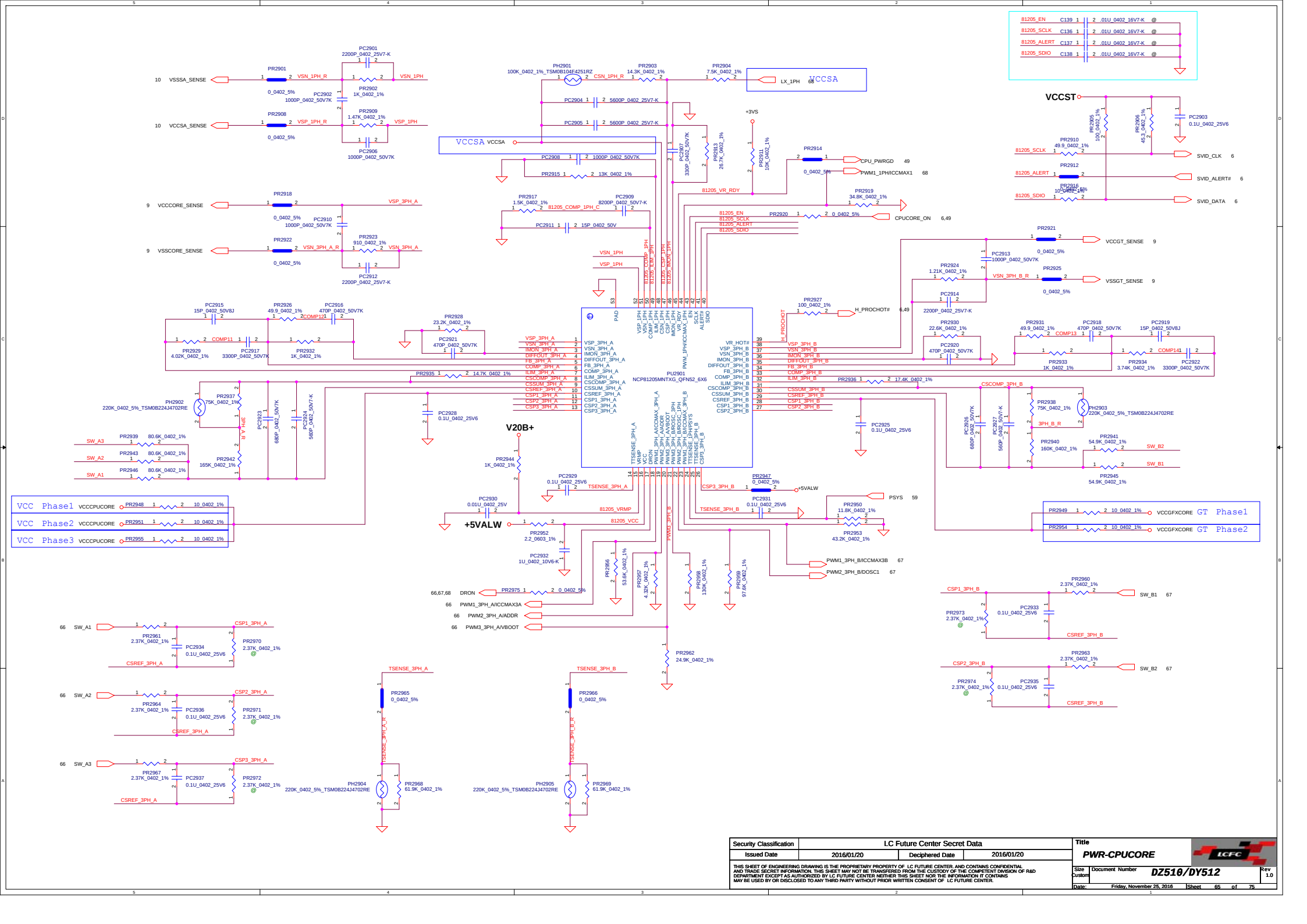

Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title	PWR-CPUCORE		
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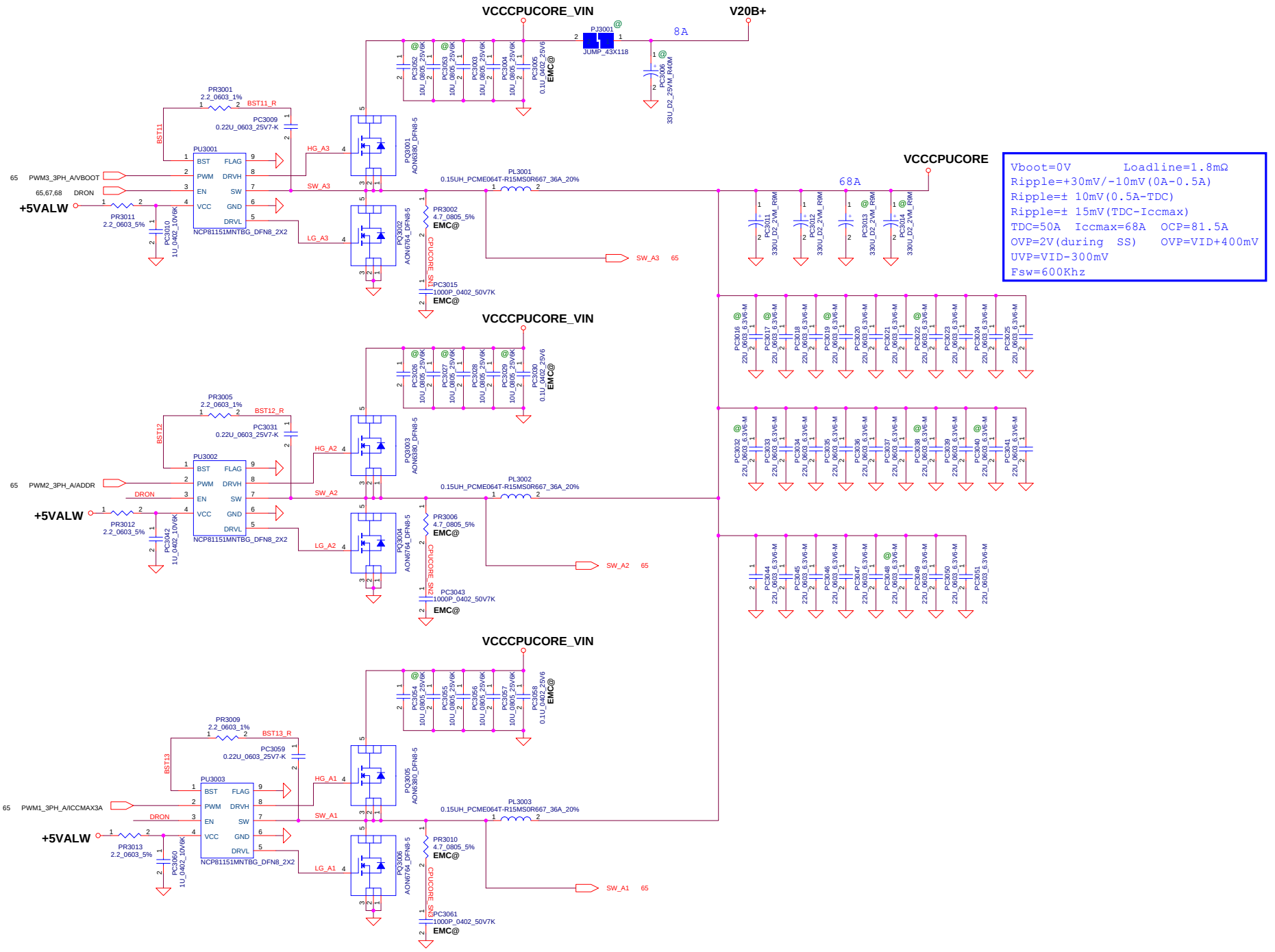

Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: **PWR-VCCCPUCORE**

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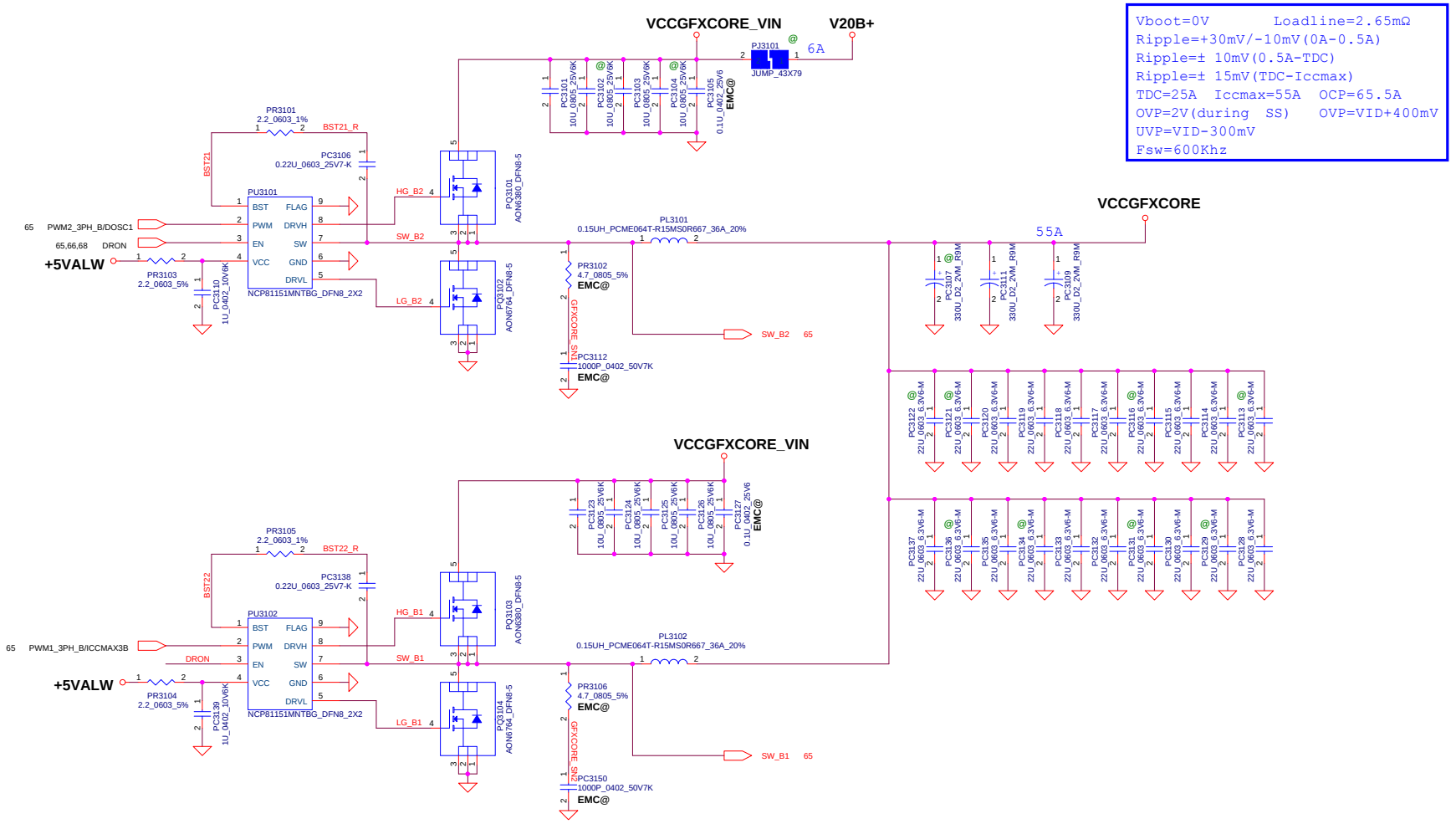

Vboot=0V Loadline=2.65mΩ
Ripple=+30mV/-10mV(0A-0.5A)
Ripple=± 10mV(0.5A-TDC)
Ripple=± 15mV(TDC-Iccmax)
TDC=25A Iccmax=55A OCP=65.5A
OVP=2V(during SS) OVP=VID+400mV
UVP=VID-300mV
Fsw=600Khz

Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: PWR-VCCGFXCORE

Size	Document Number	Rev
Custom	DZ510/DY512	1.0

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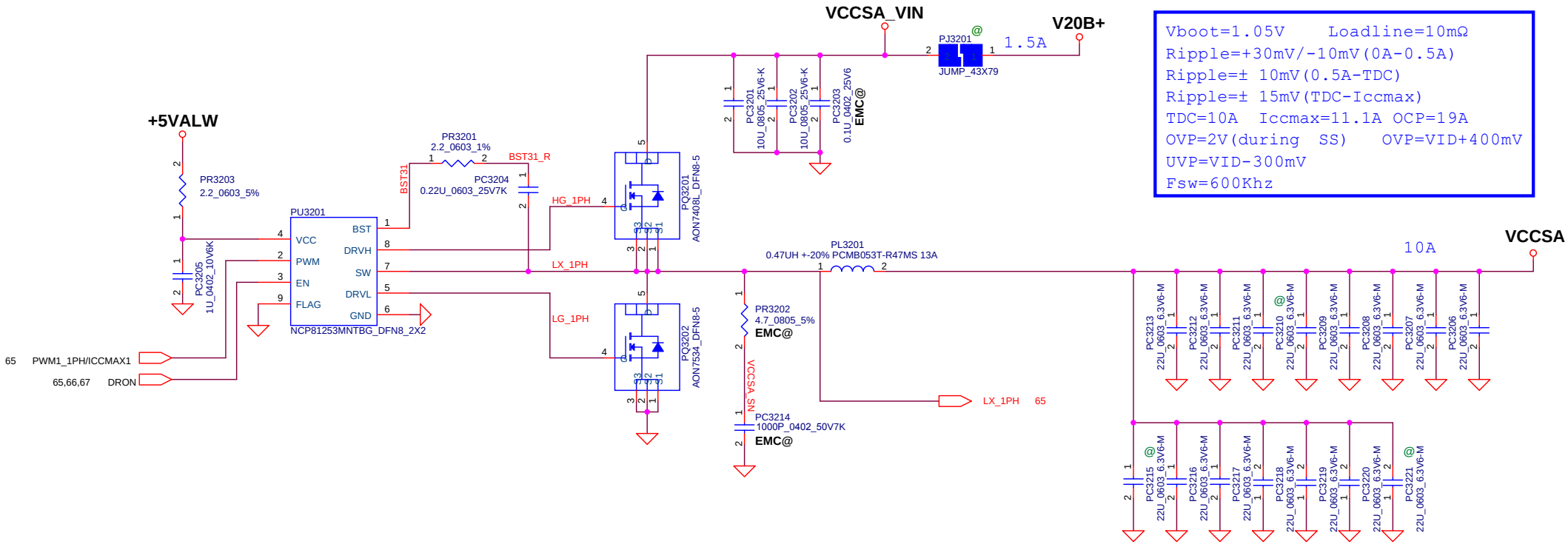

Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title	PWR-VCCSA		
Size B	Document Number	DZ510/DY512	Rev 1.0
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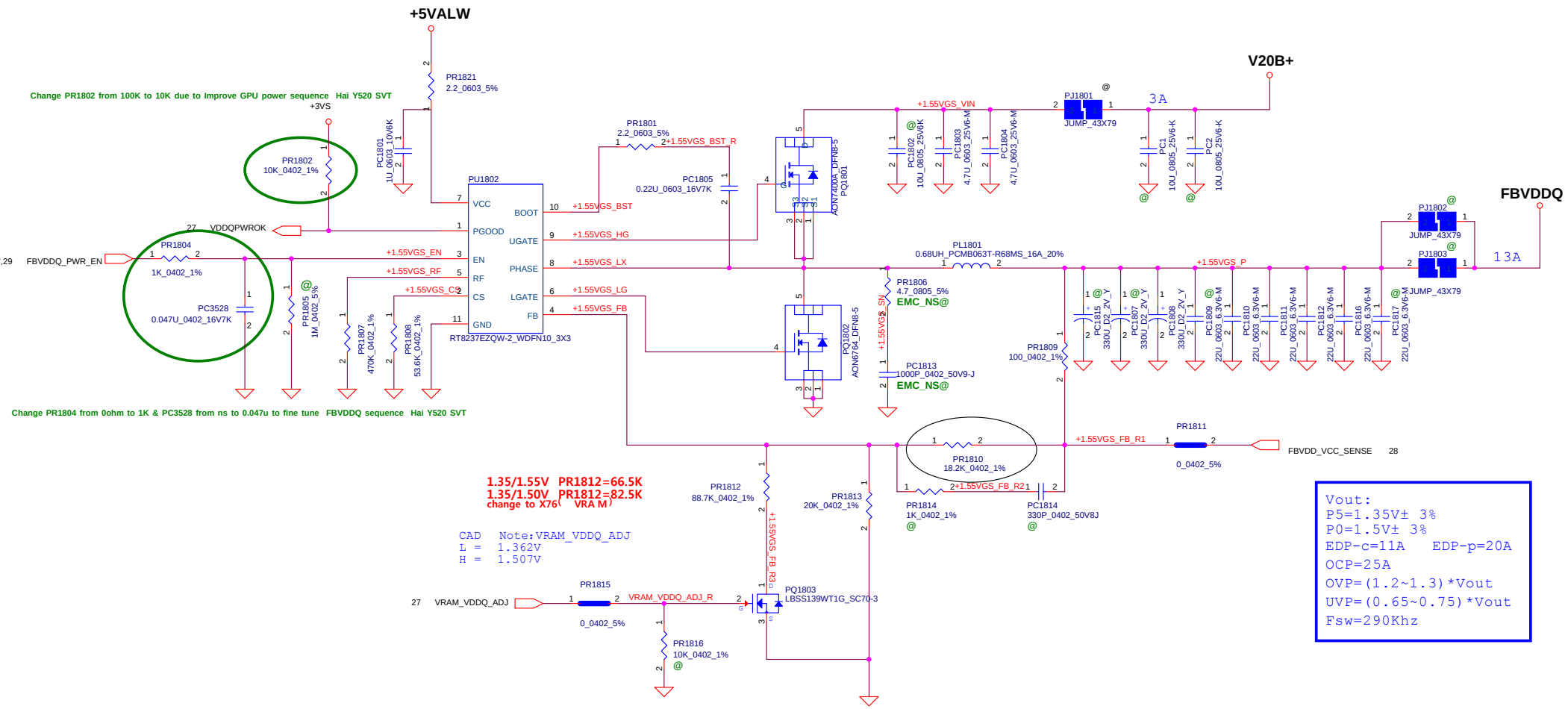
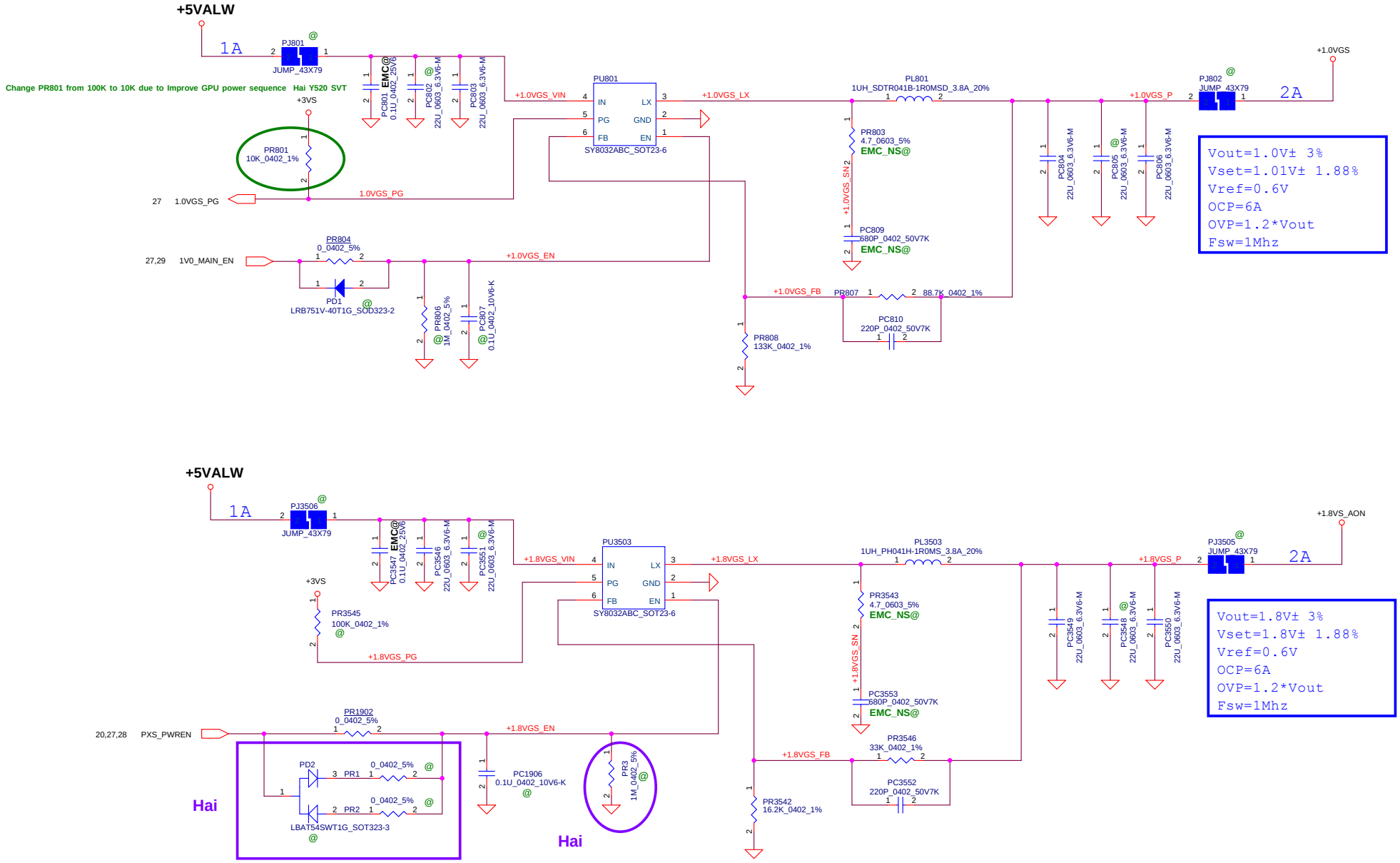


RRF (kΩ)	Fsw(kHz)
470	290
200	340
100	380
39	430

Note: DEM RRF to GND
CCM RRF to PGOOD

Title			
PWR-FBVDDQ			
Size: Custom	Document Number: DZ510/DY512		Rev: 1.0
Date: Friday, November 25, 2016	Sheet 69 of 75		



Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title	PWR-1.8/1.0VGS		
Size	Document Number	DZ510/DY512	Rev 1.0
Custom			
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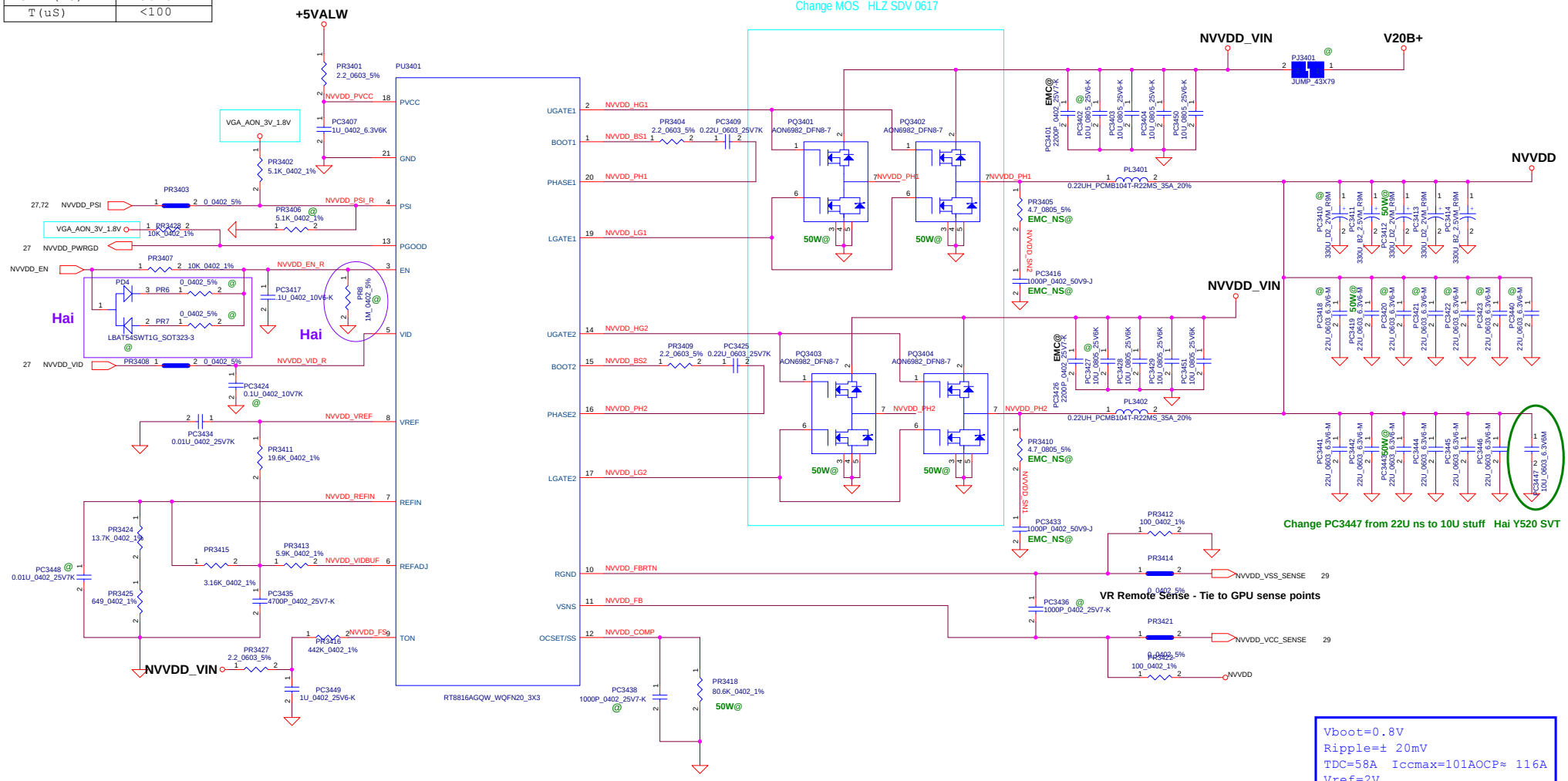
PWM-VID Specification	
	Config
Vmin(V)	0.3
Vmax(V)	1.3
Vboot(V)	0.8
Vstep(mV)	6.25
N(level)	160
Fpwm(KHz)	675
Tdmin(nS)	9.26
T(uS)	<100

Component	Value	
R1(KΩ)	PR9440	6.19
R2(KΩ)	PR9434	20.5
R3(KΩ)	PR9436	4.32
R4(KΩ)	PR9437	16.5
R5(KΩ)	PR9431	0.309
C(nF)	PC1277	4.7

PSI Level	Power Mode	Phase Configuration
Connected to PVCC	PSH	2Phase Auto CCM/DCM
High	PS0	2Phase FCCM
Intermediate	PS1	2Phase Auto CCM/DCM
Low	PS2	1Phase Auto CCM/DCM

Change MOS HLZ SDV 0617



Vboot=0.8V
Ripple=± 20mV
TDC=58A Iccmax=101AOCP≈ 116A
Vref=2V
FUVP:Vfb=0.2V
SUVP:Vcomp=3V
OVP:Vfb=2V
Fsw=400KHz

Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: PWR-NVVDD

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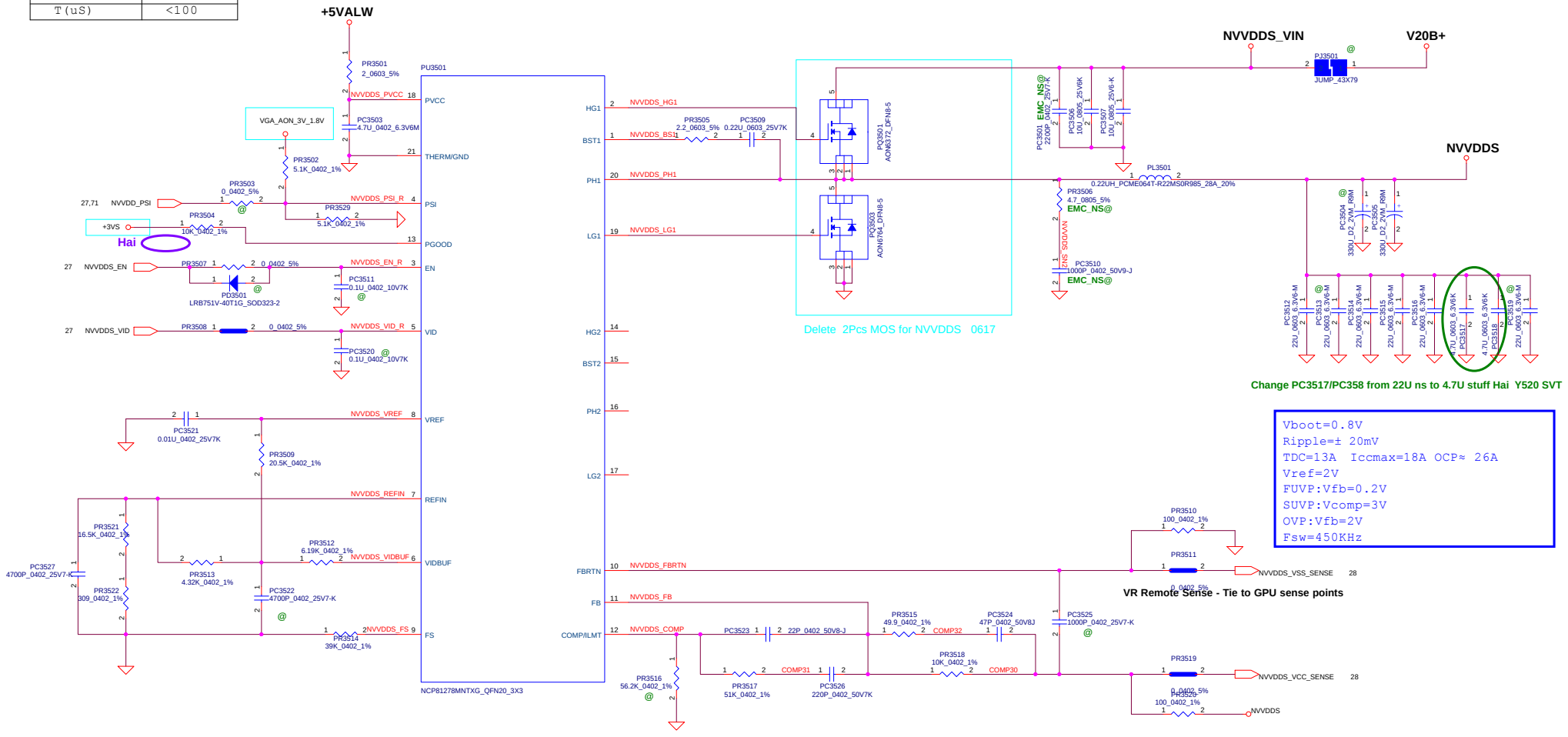
PWM-VID Specification	
	Config
Vmin(V)	0.3
Vmax(V)	1.3
Vboot(V)	0.8
Vstep(mV)	6.25
N(level)	160
Fpwm(KHz)	675
Tdmin(nS)	9.26
T(uS)	<100

Component	Value	
R1(KΩ)	PR9440	6.19
R2(KΩ)	PR9434	20.5
R3(KΩ)	PR9436	4.32
R4(KΩ)	PR9437	16.5
R5(KΩ)	PR9431	0.309
C(nF)	PC1277	4.7

PSI Level	Power Mode	Phase Configuration
Connected to PVCC	PSH	2Phase Auto CCM/DCM
High	PS0	2Phase FCCM
Intermediate	PS1	2Phase Auto CCM/DCM
Low	PS2	1Phase Auto CCM/DCM



Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: PWR-NVVDDS

Size: C | Document Number: DZ510/DY512 | Rev: 1.0

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Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title

PWR-Power schematic history

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Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: ***Blank***

Size: D	Document Number: ***DZ510/DY512***	Rev: 1.0
Date: Friday, November 25, 2016	Sheet 74 of 75	

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: ***Blank***

Size D	Document Number: ***DZ510/DY512***	Rev 1.0
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