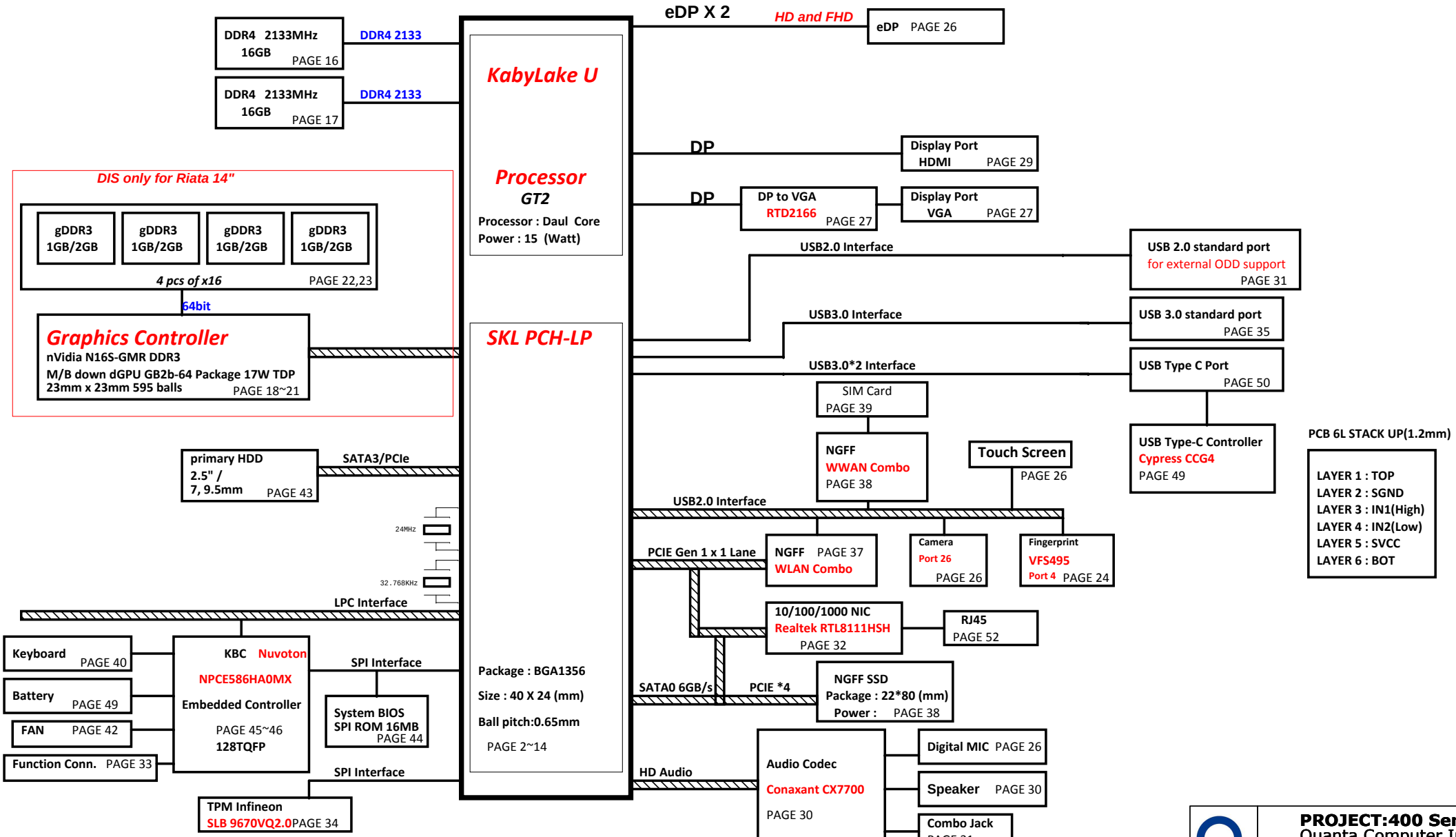
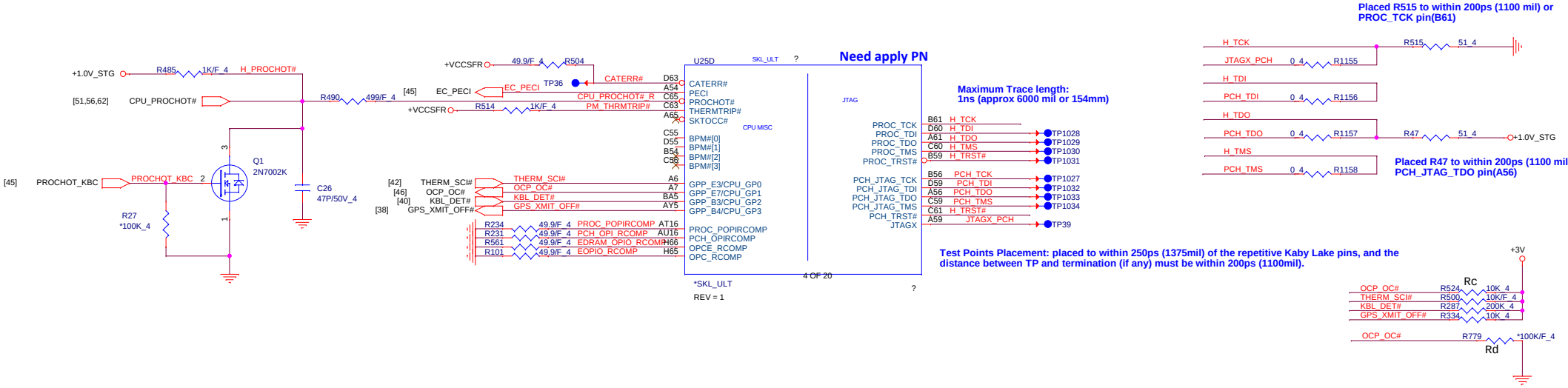
Reilly 13"/Rourke 14" KabyLake -U (UMA/DIS) Schematics 01



NB5	PROJECT:400 Series Quanta Computer Inc.	
Size: Custom	Document Number: Block Diagram	Rev: 1A
Date: Thursday, May 12, 2016	Sheet 1 of 65	



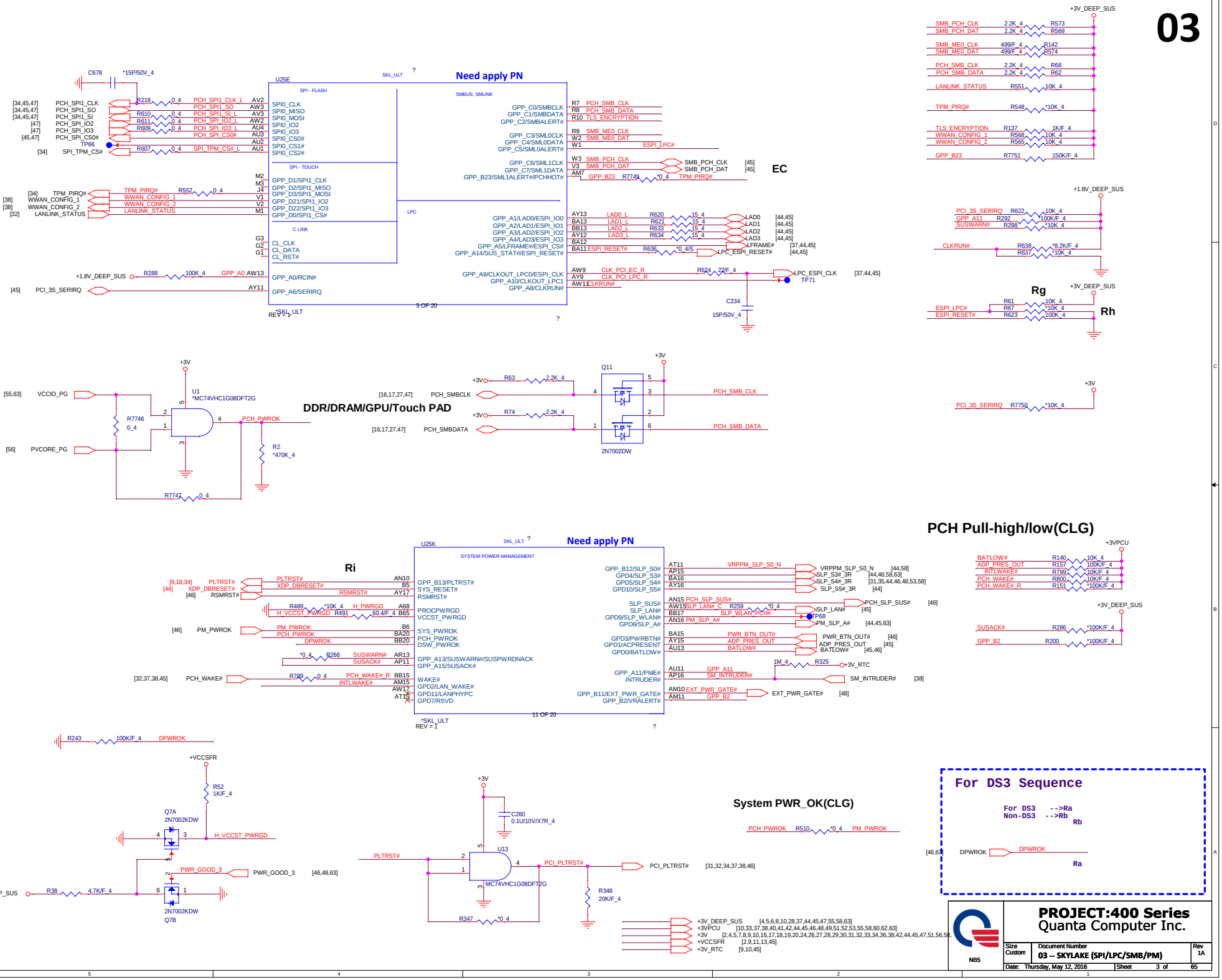
+1.0V_STG [11,13]
+VCCSFR [3,9,11,13,45]
+3V [3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63]

NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	02 -- SKYLAKE 2/20(MISC/ JTAG)	1A

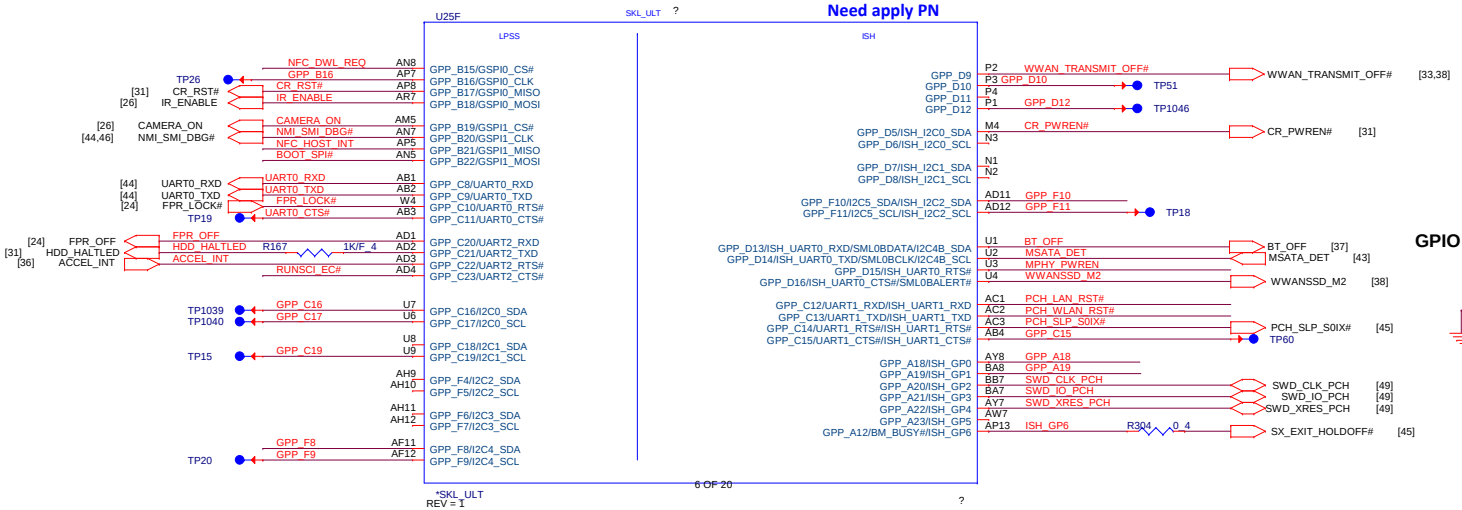
Date: Thursday, May 12, 2016 Sheet 2 of 65


Need apply PN
EC
Rg
Rh
DDR/DRAM/GPU/Touch PAD
2N7002DW
Need apply PN
Ri
PCH Pull-high/low(CLG)
System PWR_OK(CLG)
For DS3 Sequence
For DS3 -->Ra
Non-DS3 -->Rb
Rb
Ra
PROJECT:400 Series
Quanta Computer Inc.
NB5
Size Custom
Document Number
03 -- SKYLAKE (SPI/LPC/SMB/PM)
Rev 1A
Date: Thursday, May 12, 2016
Sheet 3 of 65

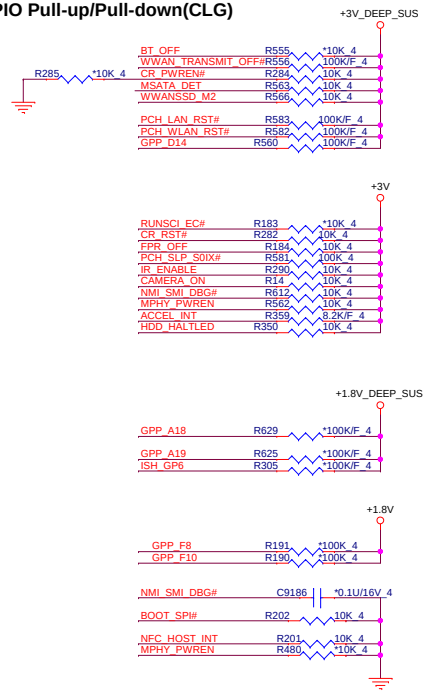
Skylake (GPIO)

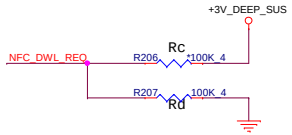
04

Need apply PN



GPIO Pull-up/Pull-down(CLG)





Codec table		
	CX7700	CX7501
R206	INSTAL	UNINSTAL
R207	UNINSTAL	INSTAL

[2,3,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63] +3V

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	04 – SKYLAKE (GPIO)	1A
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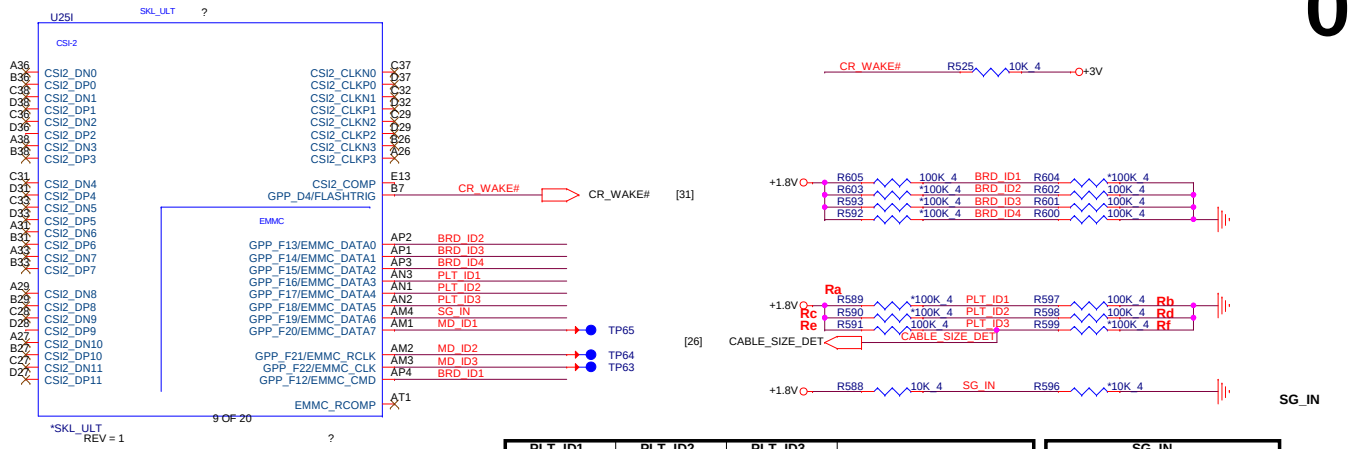
NB5

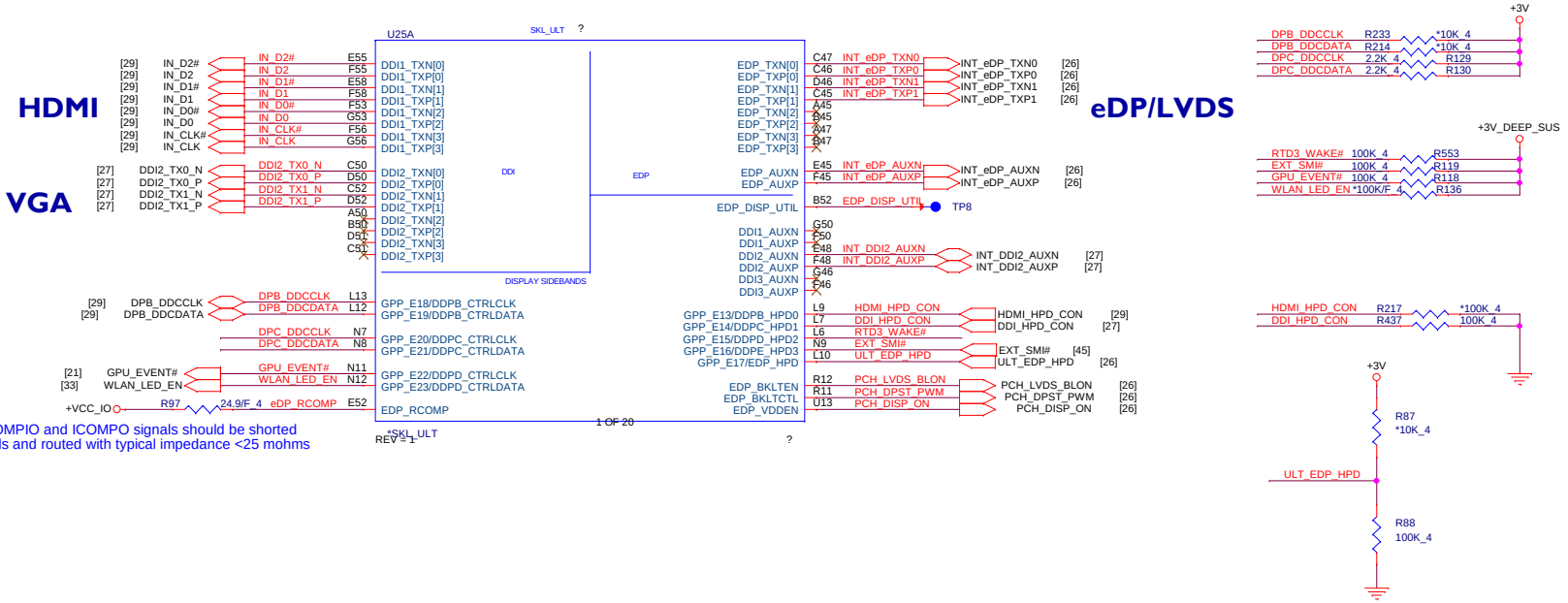
	BRD_ID1	BRD_ID2	BRD_ID3	BRD_ID4	
	GPIO201	GPIO202	GPIO203	GPIO204	AMD_FCH
	GPIO14	GPIO34	GPIO35	GPIO40	PPMT
	GPIO15	GPIO34	GPIO35	GPIO40	LPI-H
BOARD REVISION	GPIO76	GPIO77	GPIO78	GPIO79	LPT-LP
DB0	0	0	0	0	
DB1	0	0	0	1	
DB2	0	0	1	0	
	0	0	1	1	
SI1	0	1	0	0	
SIB	0	1	0	1	
SI2	0	1	1	0	
	0	1	1	1	
Pre-PV	1	0	0	0	
PV	1	0	0	1	
	1	0	1	0	
	1	0	1	1	
MV1	1	1	0	0	
	1	1	0	1	
	1	1	1	0	
	1	1	1	1	



PLT_ID1	PLT_ID2	PLT_ID3	
Ra	Rc	Re	H
Rb	Rd	Rf	L
0	0	0	13.3"
0	0	1	14"
0	1	0	15.6"
0	1	1	17.3"

SG_IN	
DIS=1	R588 (Default)
UMA=0	R596

UNINSTAL



PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	05 -- SKYLAKE (eDP/DDI/Board ID)	1A
Date: Thursday, May 12, 2016	Sheet 5 of 65	

NB5

SkyLake ULT Processor (DDR4)

06

[16] M_A_DQ[63:0]
[17] M_B_DQ[63:0]
[16] M_A_DQSN[7:0]
[16] M_A_DQSP[7:0]
[17] M_B_DQSN[7:0]
[17] M_B_DQSP[7:0]

Need apply PN

U25B SKL_ULT

DDR0_CKN[0] AU53 M_A_CLKN0 [16]
DDR0_CKP[0] AT53 M_A_CLKP0 [16]
DDR0_CKN[1] AU55 M_A_CLKN1 [16]
DDR0_CKP[1] AT55 M_A_CLKP1 [16]

DDR0_CKE[0] BA56 M_A_CKE0 [16]
DDR0_CKE[1] BB56 M_A_CKE1 [16]
DDR0_CKE[2] AW56
DDR0_CKE[3] AY56

DDR0_CS#[0] AU45 M_A_CS#0 [16]
DDR0_CS#[1] AU43 M_A_CS#1 [16]
DDR0_ODT[0] AT45 M_A_ODT0 [16]
DDR0_ODT[1] AT43 M_A_ODT1 [16]

BA51 M_A_A5
BB54 M_A_A9
BA52 M_A_A6
AY52 M_A_A8
AW52 M_A_A7
AY55 M_A_BG#0 M_A_BG#0 [16]
AW54 M_A_A12 M_A_A12 [16]
BA54 M_A_A11 M_A_A11 [16]
BA55 M_A_ACT# [16]
AY54 M_A_BG#1 [16]

AU46 M_A_A13 M_A_A13 [16]
AU48 M_A_CAS# [16]
AT46 M_A_WE# [16]
AU50 M_A_RAS# [16]
AU52 M_A_BS#0 [16]
AY51 M_A_A2 M_A_A2 [16]
AT48 M_A_BS#1 [16]
AT50 M_A_A10 M_A_A10 [16]
BB50 M_A_A1 [16]
AY50 M_A_A0 [16]
BA50 M_A_A3 [16]
BB52 M_A_A4 [16]

AM70 M_A_DQSN0
AM69 M_A_DQSP0
AT69 M_A_DQSN1
AT70 M_A_DQSP1
BA64 M_A_DQSN4
AY64 M_A_DQSP4
AY60 M_A_DQSN5
BA60 M_A_DQSP5
BA38 M_B_DQSN0
AY38 M_B_DQSP0
AY34 M_B_DQSN1
BA34 M_B_DQSP1
BA30 M_B_DQSN4
AY30 M_B_DQSP4
AY26 M_B_DQSN5
BA26 M_B_DQSP5

AW50 M_A_ALERT# M_A_ALERT# [16]
AT52 M_A_PARITY M_A_PARITY [16]

AY67 SM_VREF SM_VREF [16]
AY68 SMDDR_VREF_DQ0_M3 TP127
BA67 SMDDR_VREF_DQ1_M3 SMDDR_VREF_DQ1_M3 [17]
AW67 DDR_PG_CNTL

20mils width

DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5]
DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9]
DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6]
DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8]
DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7]
DDR0_BA[2]/DDR0_CAA[5]/DDR0_BG[0]
DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12]
DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11]
DDR0_MA[15]/DDR0_CAA[8]/DDR0_ACT#
DDR0_MA[14]/DDR0_CAA[9]/DDR0_BG[1]

DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13]
DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15]
DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14]
DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16]
DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0]
DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2]
DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1]
DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10]
DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1]
DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0]
DDR0_MA[3]
DDR0_MA[4]

DDR0_DQSN[0]
DDR0_DQSP[0]
DDR0_DQSN[1]
DDR0_DQSP[1]
DDR0_DQSN[2]/DDR0_DQSN[4]
DDR0_DQSP[2]/DDR0_DQSP[4]
DDR0_DQSN[3]/DDR0_DQSN[5]
DDR0_DQSP[3]/DDR0_DQSP[5]
DDR0_DQSN[4]/DDR1_DQSN[0]
DDR0_DQSP[4]/DDR1_DQSP[0]
DDR0_DQSN[5]/DDR1_DQSN[1]
DDR0_DQSP[5]/DDR1_DQSP[1]
DDR0_DQSN[6]/DDR1_DQSN[4]
DDR0_DQSP[6]/DDR1_DQSP[4]
DDR0_DQSN[7]/DDR1_DQSN[5]
DDR0_DQSP[7]/DDR1_DQSP[5]

DDR0_ALERT#
DDR0_PAR

DDR_VREF_CA
DDR0_VREF_DQ
DDR1_VREF_DQ

DDR_VTT_CNTL

DDR CH - A

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*SKL_ULT
REV = 1

U25C SKL_ULT

Need apply PN

M_A_DQ16 AF65 DDR1_DQ[0]/DDR0_DQ[16]
M_A_DQ17 AF64 DDR1_DQ[1]/DDR0_DQ[17]
M_A_DQ18 AK65 DDR1_DQ[2]/DDR0_DQ[18]
M_A_DQ19 AK64 DDR1_DQ[3]/DDR0_DQ[19]
M_A_DQ20 AF66 DDR1_DQ[4]/DDR0_DQ[20]
M_A_DQ21 AF67 DDR1_DQ[5]/DDR0_DQ[21]
M_A_DQ22 AK67 DDR1_DQ[6]/DDR0_DQ[22]
M_A_DQ23 AK66 DDR1_DQ[7]/DDR0_DQ[23]
M_A_DQ24 AF70 DDR1_DQ[8]/DDR0_DQ[24]
M_A_DQ25 AF68 DDR1_DQ[9]/DDR0_DQ[25]
M_A_DQ26 AH71 DDR1_DQ[10]/DDR0_DQ[26]
M_A_DQ27 AH68 DDR1_DQ[11]/DDR0_DQ[27]
M_A_DQ28 AF71 DDR1_DQ[12]/DDR0_DQ[28]
M_A_DQ29 AF69 DDR1_DQ[13]/DDR0_DQ[29]
M_A_DQ30 AH70 DDR1_DQ[14]/DDR0_DQ[30]
M_A_DQ31 AH69 DDR1_DQ[15]/DDR0_DQ[31]
M_A_DQ48 AT66 DDR1_DQ[16]/DDR0_DQ[48]
M_A_DQ49 AU66 DDR1_DQ[17]/DDR0_DQ[49]
M_A_DQ50 AP65 DDR1_DQ[18]/DDR0_DQ[50]
M_A_DQ51 AN65 DDR1_DQ[19]/DDR0_DQ[51]
M_A_DQ52 AN66 DDR1_DQ[20]/DDR0_DQ[52]
M_A_DQ53 AP66 DDR1_DQ[21]/DDR0_DQ[53]
M_A_DQ54 AT65 DDR1_DQ[22]/DDR0_DQ[54]
M_A_DQ55 AU65 DDR1_DQ[23]/DDR0_DQ[55]
M_A_DQ56 AT61 DDR1_DQ[24]/DDR0_DQ[56]
M_A_DQ57 AU61 DDR1_DQ[25]/DDR0_DQ[57]
M_A_DQ58 AP60 DDR1_DQ[26]/DDR0_DQ[58]
M_A_DQ59 AN60 DDR1_DQ[27]/DDR0_DQ[59]
M_A_DQ60 AN61 DDR1_DQ[28]/DDR0_DQ[60]
M_A_DQ61 AP61 DDR1_DQ[29]/DDR0_DQ[61]
M_A_DQ62 AT60 DDR1_DQ[30]/DDR0_DQ[62]
M_A_DQ63 AU60 DDR1_DQ[31]/DDR0_DQ[63]
M_B_DQ16 AU40 DDR1_DQ[32]/DDR1_DQ[16]
M_B_DQ17 AT40 DDR1_DQ[33]/DDR1_DQ[17]
M_B_DQ18 AT37 DDR1_DQ[34]/DDR1_DQ[18]
M_B_DQ19 AU37 DDR1_DQ[35]/DDR1_DQ[19]
M_B_DQ20 AR40 DDR1_DQ[36]/DDR1_DQ[20]
M_B_DQ21 AP40 DDR1_DQ[37]/DDR1_DQ[21]
M_B_DQ22 AP37 DDR1_DQ[38]/DDR1_DQ[22]
M_B_DQ23 AR37 DDR1_DQ[39]/DDR1_DQ[23]
M_B_DQ24 AT33 DDR1_DQ[40]/DDR1_DQ[24]
M_B_DQ25 AU33 DDR1_DQ[41]/DDR1_DQ[25]
M_B_DQ26 AU30 DDR1_DQ[42]/DDR1_DQ[26]
M_B_DQ27 AT30 DDR1_DQ[43]/DDR1_DQ[27]
M_B_DQ28 AR33 DDR1_DQ[44]/DDR1_DQ[28]
M_B_DQ29 AP33 DDR1_DQ[45]/DDR1_DQ[29]
M_B_DQ30 AR30 DDR1_DQ[46]/DDR1_DQ[30]
M_B_DQ31 AP30 DDR1_DQ[47]/DDR1_DQ[31]
M_B_DQ48 AU27 DDR1_DQ[48]
M_B_DQ49 AT27 DDR1_DQ[49]
M_B_DQ50 AT25 DDR1_DQ[50]
M_B_DQ51 AU25 DDR1_DQ[51]
M_B_DQ52 AP27 DDR1_DQ[52]
M_B_DQ53 AN27 DDR1_DQ[53]
M_B_DQ54 AN25 DDR1_DQ[54]
M_B_DQ55 AP25 DDR1_DQ[55]
M_B_DQ56 AT22 DDR1_DQ[56]
M_B_DQ57 AU22 DDR1_DQ[57]
M_B_DQ58 AU21 DDR1_DQ[58]
M_B_DQ59 AT21 DDR1_DQ[59]
M_B_DQ60 AN22 DDR1_DQ[60]
M_B_DQ61 AP22 DDR1_DQ[61]
M_B_DQ62 AP21 DDR1_DQ[62]
M_B_DQ63 AN21 DDR1_DQ[63]

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DDR1_CKN[1] AN46 M_B_CLKN1 [17]
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DDR1_CKP[1] AP46 M_B_CLKP1 [17]

DDR1_CKE[0] AN56 M_B_CKE0 [17]
DDR1_CKE[1] AP55 M_B_CKE1 [17]
DDR1_CKE[2] AN55
DDR1_CKE[3] AP53

DDR1_CS#[0] BB42 M_B_CS#0 [17]
DDR1_CS#[1] AY42 M_B_CS#1 [17]
DDR1_ODT[0] BA42 M_B_ODT0 [17]
DDR1_ODT[1] AW42 M_B_ODT1 [17]

AY48 M_B_A5
AP50 M_B_A9
BA48 M_B_A6
BB48 M_B_A8
BA48 M_B_A7
AP52
AN50 M_B_A12
AN48 M_B_A11
AN53
AN52

BA43 M_B_A13
AY43
AY44
AW44
BB44
AY47 M_B_A2
BA44
AW46 M_B_A10
AY46 M_B_A1
BA46 M_B_A0
BB46 M_B_A3
BA47 M_B_A4

M_B_A5 [17]
M_B_A9 [17]
M_B_A6 [17]
M_B_A8 [17]
M_B_A7 [17]
M_B_BG#0 [17]
M_B_A12 [17]
M_B_A11 [17]
M_B_ACT# [17]
M_B_BG#1 [17]

M_B_A13 [17]
M_B_CAS# [17]
M_B_WE# [17]
M_B_RAS# [17]
M_B_BS#0 [17]
M_B_A2 [17]
M_B_BS#1 [17]
M_B_A10 [17]
M_B_A1 [17]
M_B_A0 [17]
M_B_A3 [17]
M_B_A4 [17]

DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5]
DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9]
DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6]
DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8]
DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7]
DDR1_BA[2]/DDR1_CAA[5]/DDR1_BG[0]
DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12]
DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11]
DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT#
DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1]

DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13]
DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15]
DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14]
DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16]
DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0]
DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2]
DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1]
DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10]
DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1]
DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0]
DDR1_MA[3]
DDR1_MA[4]

DDR1_DQSN[0]/DDR0_DQSN[2]
DDR1_DQSP[0]/DDR0_DQSP[2]
DDR1_DQSN[1]/DDR0_DQSN[3]
DDR1_DQSP[1]/DDR0_DQSP[3]
DDR1_DQSN[2]/DDR0_DQSN[6]
DDR1_DQSP[2]/DDR0_DQSP[6]
DDR1_DQSN[3]/DDR0_DQSN[7]
DDR1_DQSP[3]/DDR0_DQSP[7]
DDR1_DQSN[4]/DDR1_DQSN[2]
DDR1_DQSP[4]/DDR1_DQSP[2]
DDR1_DQSN[5]/DDR1_DQSN[3]
DDR1_DQSP[5]/DDR1_DQSP[3]
DDR1_DQSN[6]
DDR1_DQSP[6]
DDR1_DQSN[7]
DDR1_DQSP[7]

AM66 M_A_DQSN2
AH65 M_A_DQSP2
AG69 M_A_DQSN3
AG70 M_A_DQSP3
AR66 M_A_DQSN6
AR65 M_A_DQSP6
AR61 M_A_DQSN7
AR60 M_A_DQSP7
AT38 M_B_DQSN2
AR38 M_B_DQSP2
AT32 M_B_DQSN3
AR32 M_B_DQSP3
AR25 M_B_DQSN6
AR27 M_B_DQSP6
AR22 M_B_DQSN7
AR21 M_B_DQSP7

AN43 M_B_ALERT# M_B_ALERT# [17]
AP43 M_B_PARITY M_B_PARITY [17]
AT13
AR18 SM_RCOMP_0 R237 121/F_4
AT18 SM_RCOMP_1 R870 80.6/F_4
AU18 SM_RCOMP_2 R869 100/F_4

DDR1_ALERT#
DDR1_PAR
DRAM_RESET#
DDR_RCOMP[0]
DDR_RCOMP[1]
DDR_RCOMP[2]

DDR CH - B

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*SKL_ULT
REV = 1

+1.2VSUS
R871 470_4
DDR3_DRAMRST# [16,17]

+3V_DEEP_SUS
R874 10K/F_4
R876 10K/F_4
Q65 2N7002K
DDR_VTT_PG_CTRL [48,53]
R873 *100K/F_4
DDR_PG_CNTL
R875 10K/F_4
Q66 PMST3904_SOT-323
R877 100K/F_4

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	06 -- SKYLAKE (DDR3-A/B I/F)	1A

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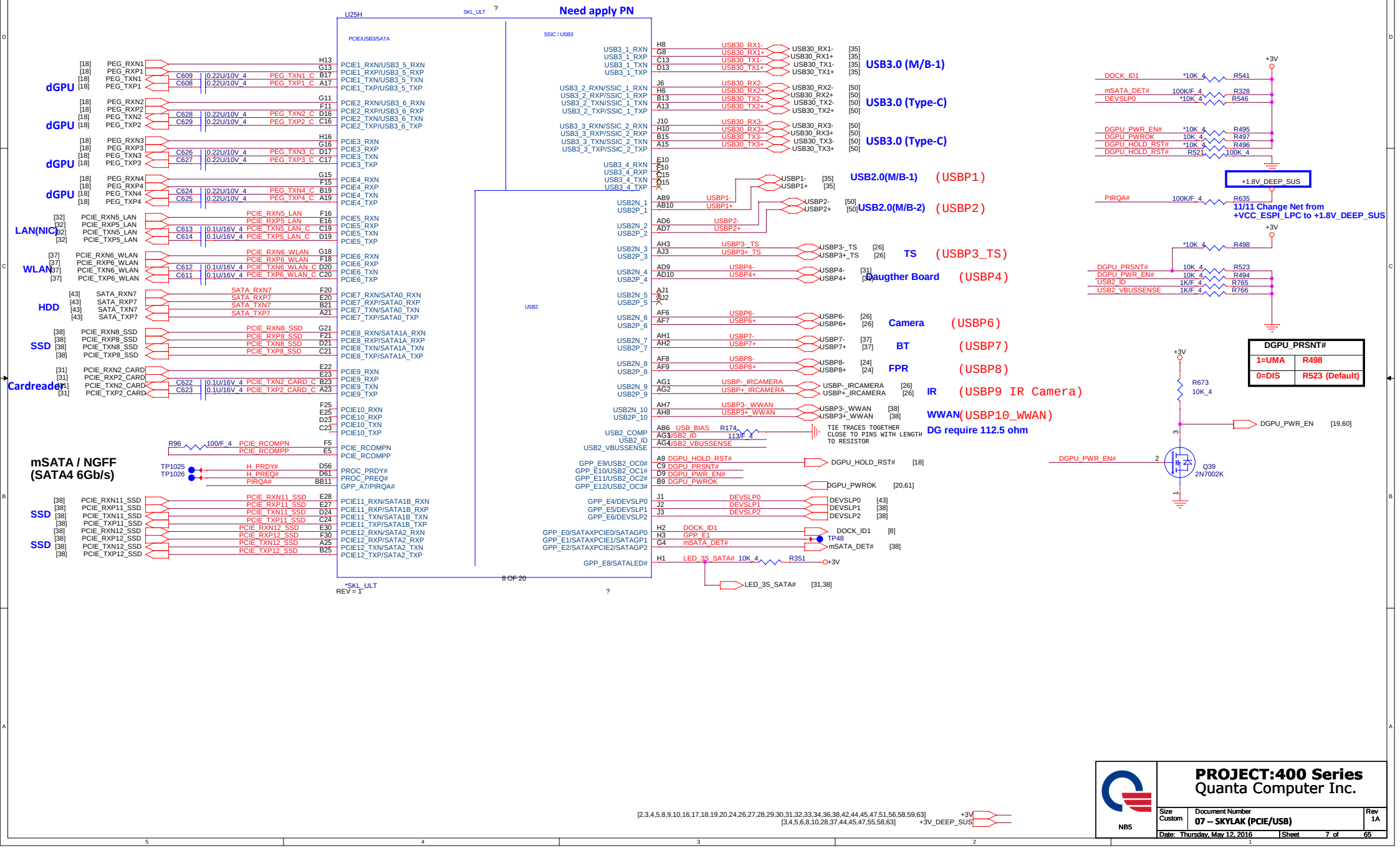
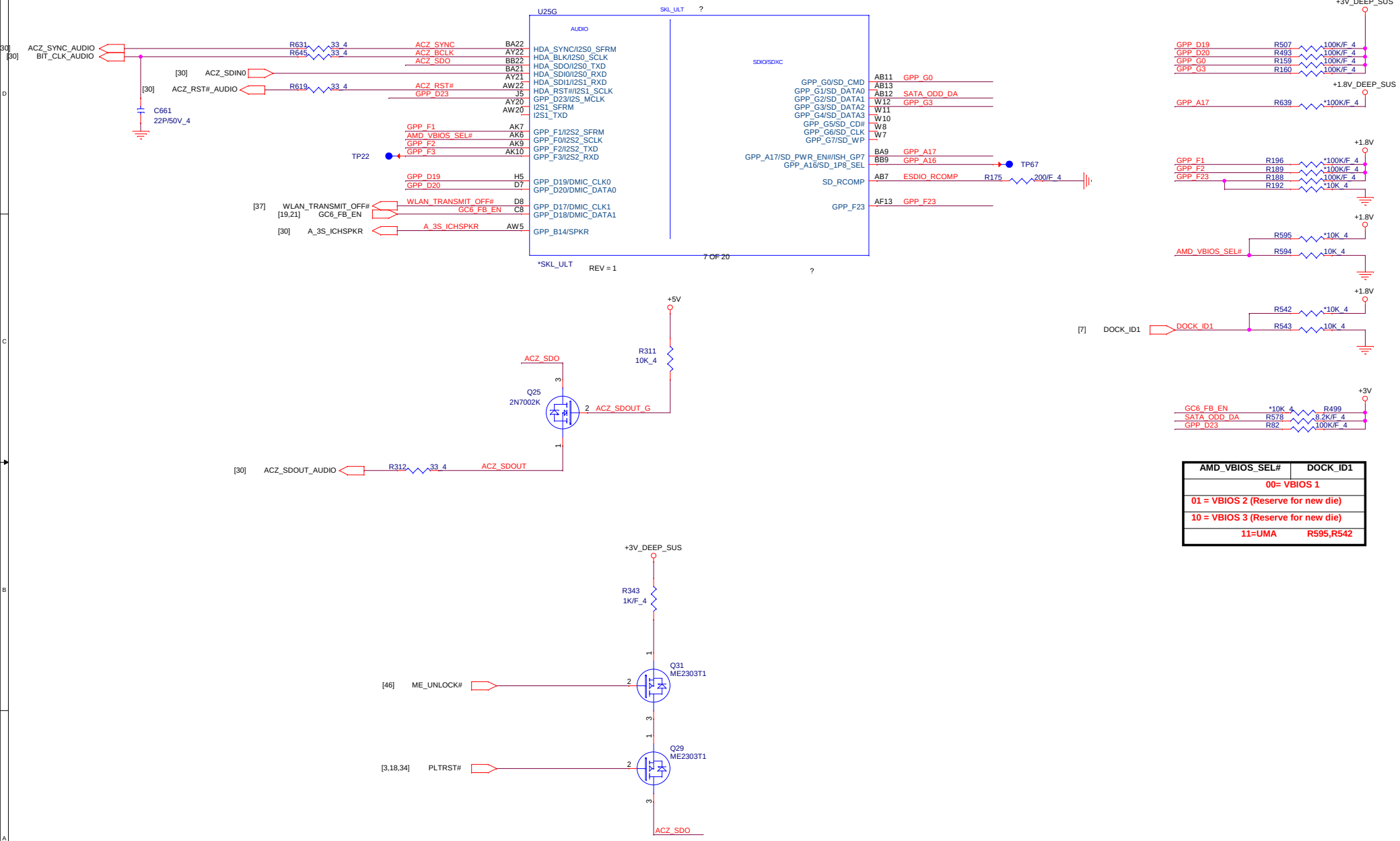


[2,3,4,5,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63] +3V
[3,4,5,6,8,10,28,37,44,45,47,55,58,63] +3V_DEEP_SUS

NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	07 -- SKYLAK (PCIE/USB)	1A
Date: Thursday, May 12, 2016	Sheet 7 of 65	



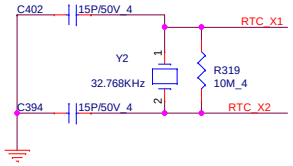
AMD_VBIOS_SEL#	DOCK_ID1
00= VBIOS 1	
01 = VBIOS 2 (Reserve for new die)	
10 = VBIOS 3 (Reserve for new die)	
11=UMA	R595,R542

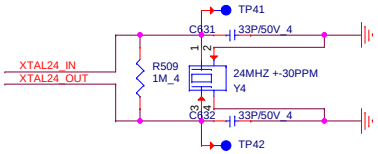
PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	08 -- SKYLAKE (HDA)	1A
Date: Thursday, May 12, 2016	Sheet 8 of 65	

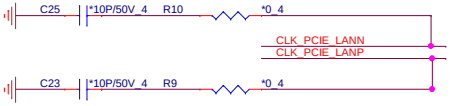
NB5

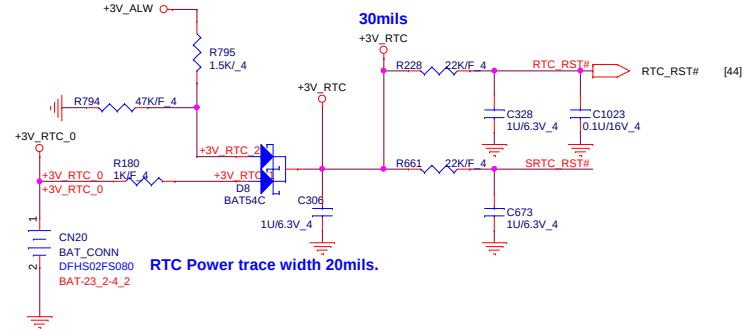
RTC Clock 32.768KHz



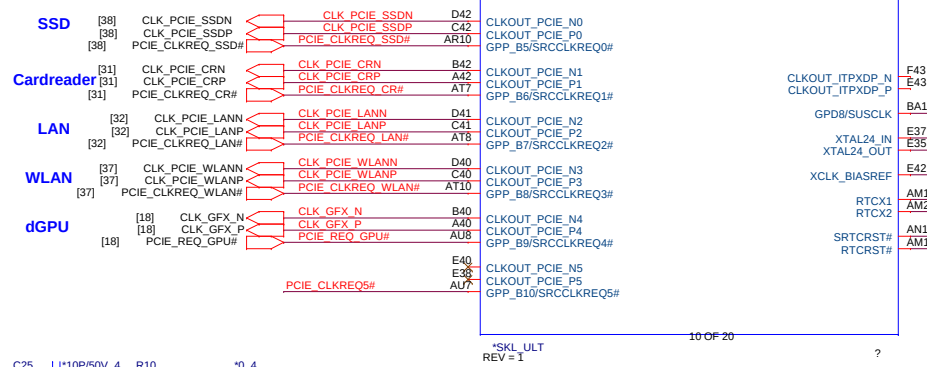


RTC Circuitry(RTC)

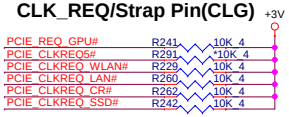




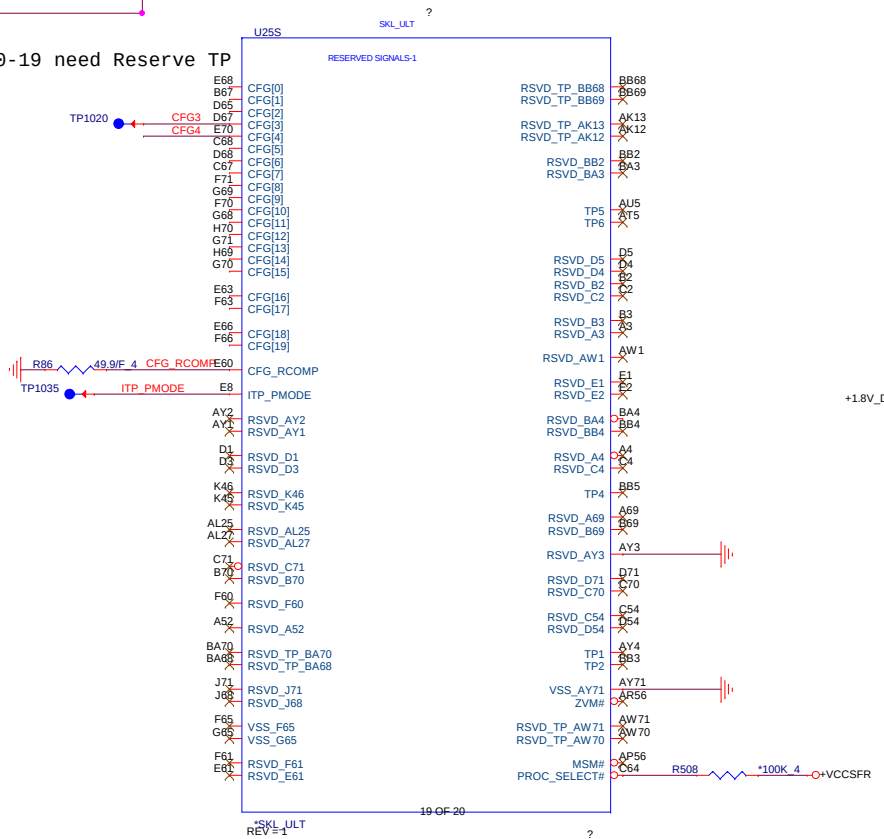
+VCCSFR [2,3,11,13,45]
+1.0V_DEEP_SUS [10,54,55,58]
+3V [2,3,4,5,7,8,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63]

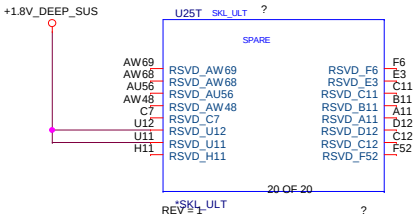


CLK_REQ/Strap Pin(CLG)



CFG0-19 need Reserve TP





NB5	PROJECT:400 Series Quanta Computer Inc.		
	Size: Custom	Document Number: 09 -- SKYLAKE (CLK/RSV/RTC)	Rev: 1A
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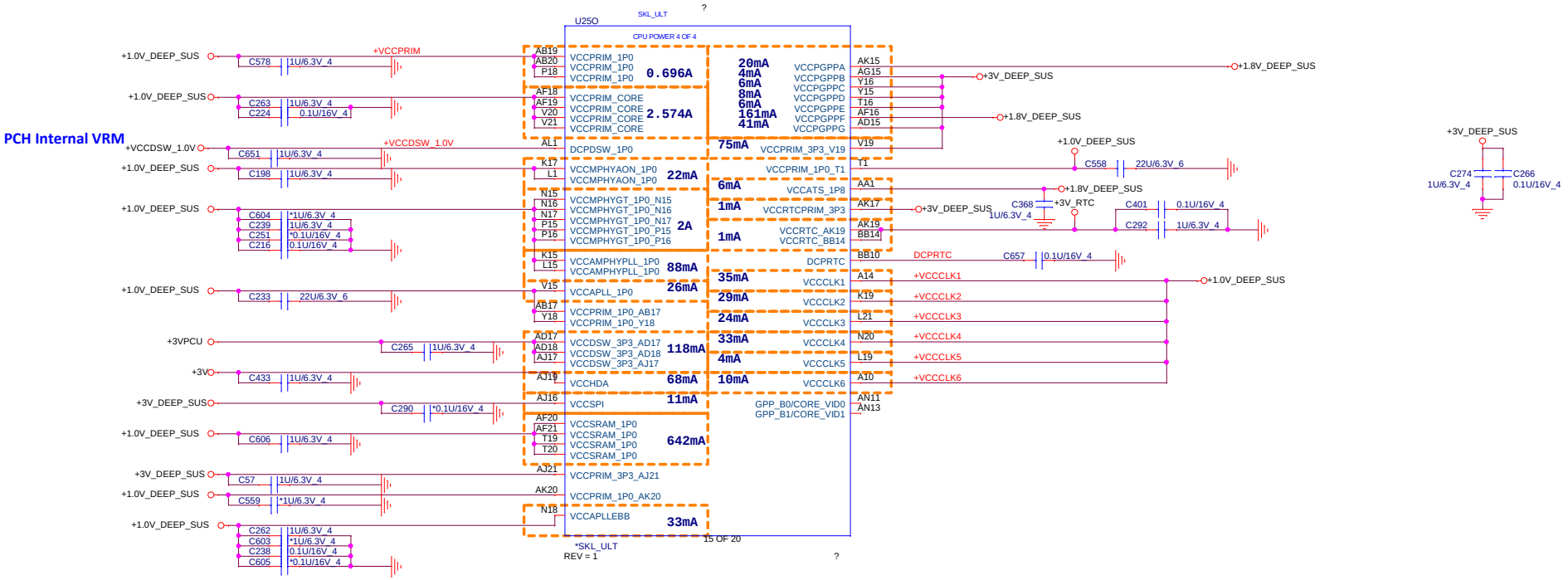
PCH Internal VRM



+3V_DEEP_SUS [3,4,5,6,8,28,37,44,45,47,55,58,63]
+3VPCU [3,33,37,38,40,41,42,44,45,46,48,49,51,52,53,55,58,60,62,63]
+1.0V_DEEP_SUS [9,54,55,58]
+VCC_PRIM
+3V [2,3,4,5,7,8,9,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63]
+1.8V_DEEP_SUS [3,4,7,8,9,45,54,63]

NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	10 -- SKYLAKE (PCH POWER)	1A

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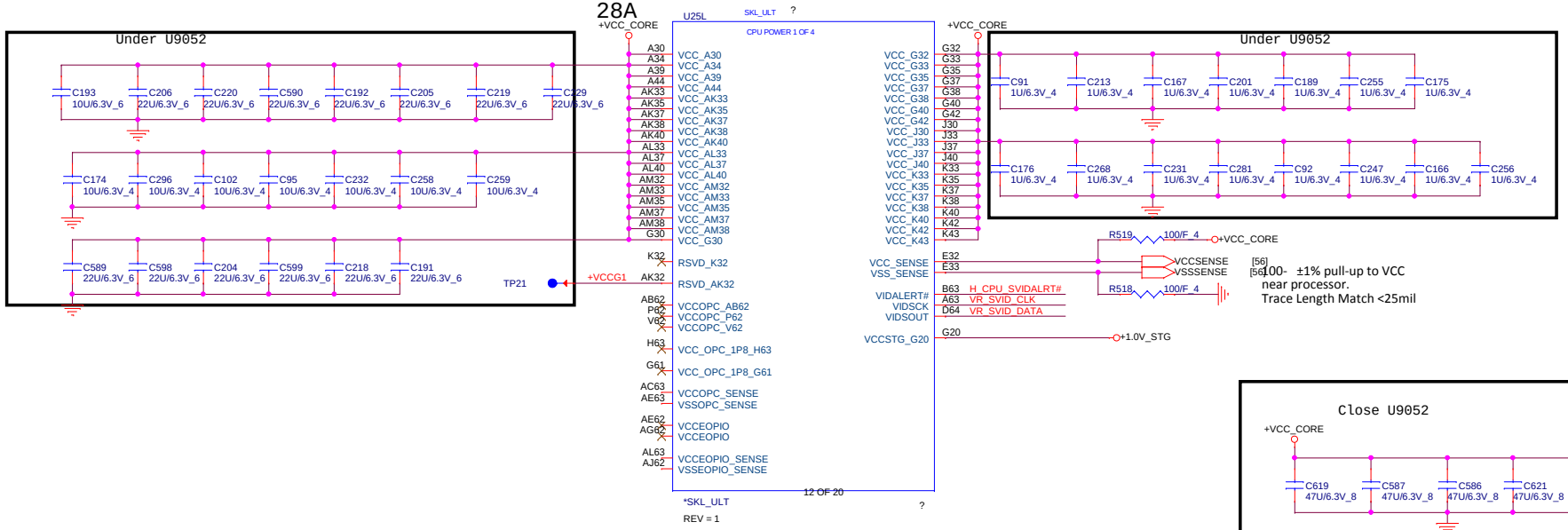
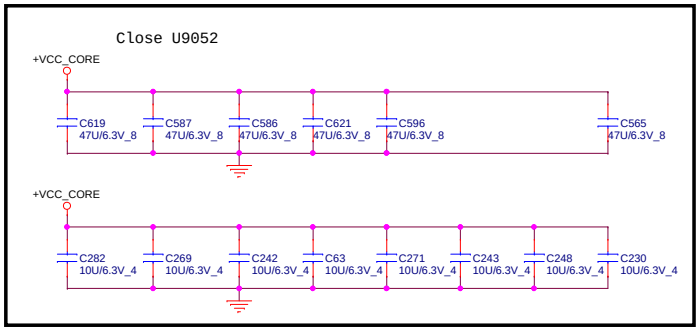
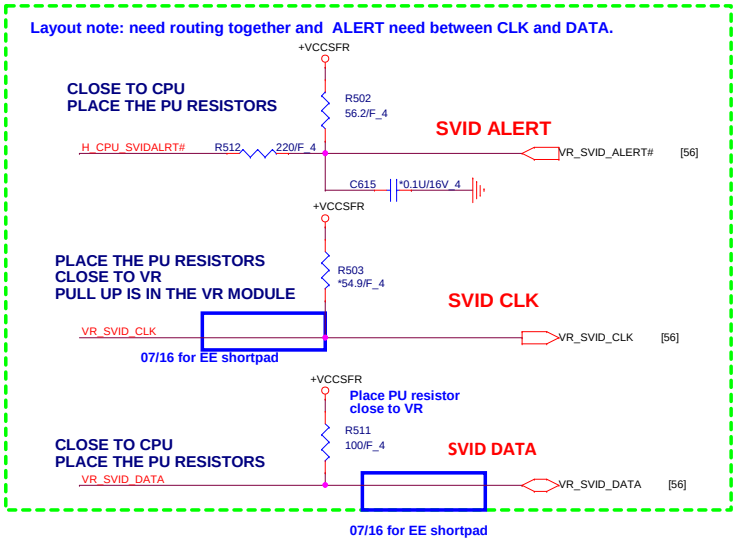
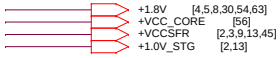




Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
$V_{CC_{GT}}$	Processor Graphics Power Rails	SVID
$V_{CC_{GTX}}$	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
$V_{CC_{SA}}$	System Agent Power Rail	SVID/Fixed (SKU dependent)
$V_{CC_{IO}}$	IO Power Rail	Fixed
$V_{CC_{ST}}$	Sustain Power Rail	Fixed
$V_{CC_{PLL}}$	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
$V_{CC_{OPC}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{OPC\_1P8}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{EOPIO}}$	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed





PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	11 -- SKYLAKE (POWER-1)	1A
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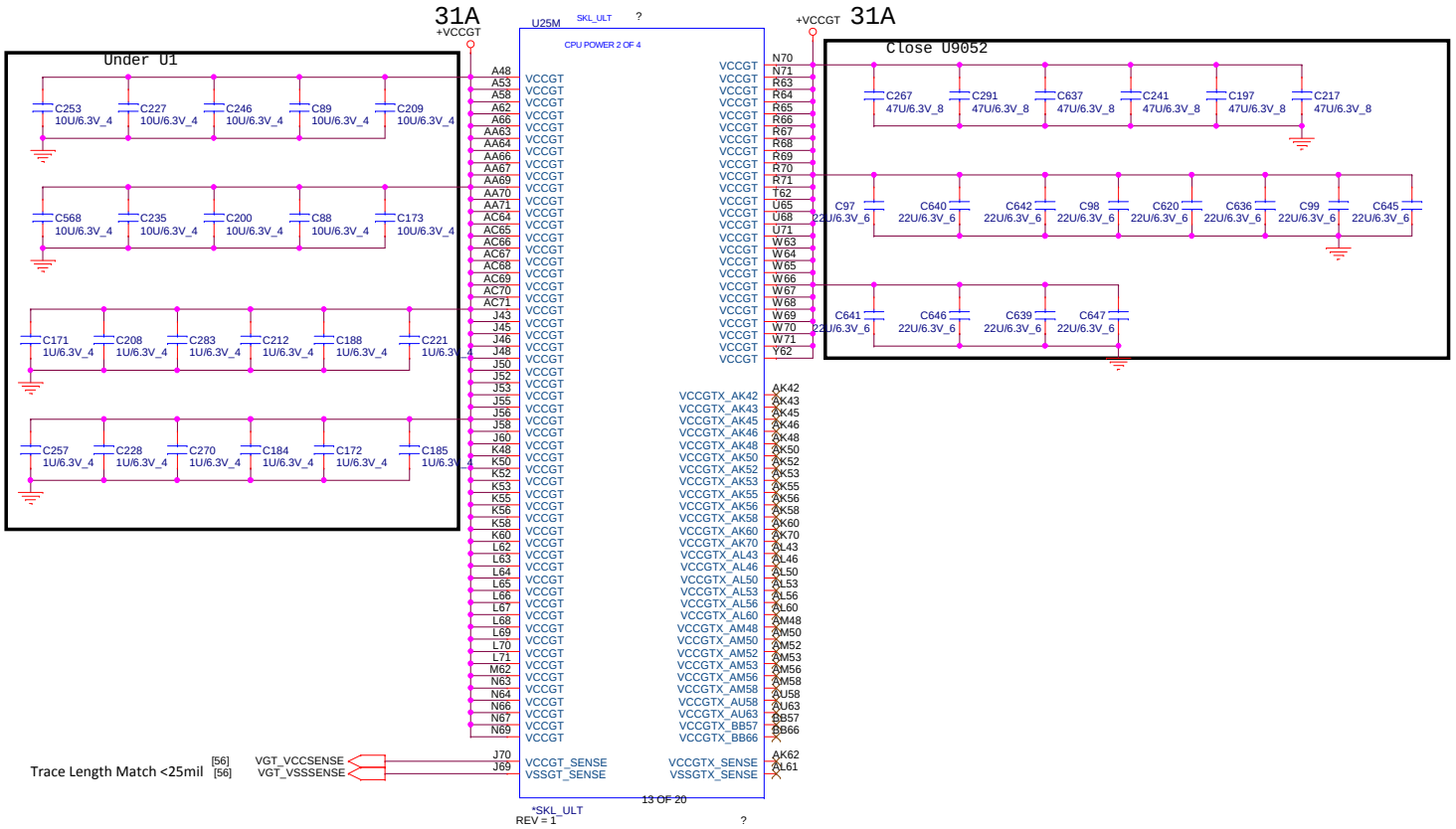
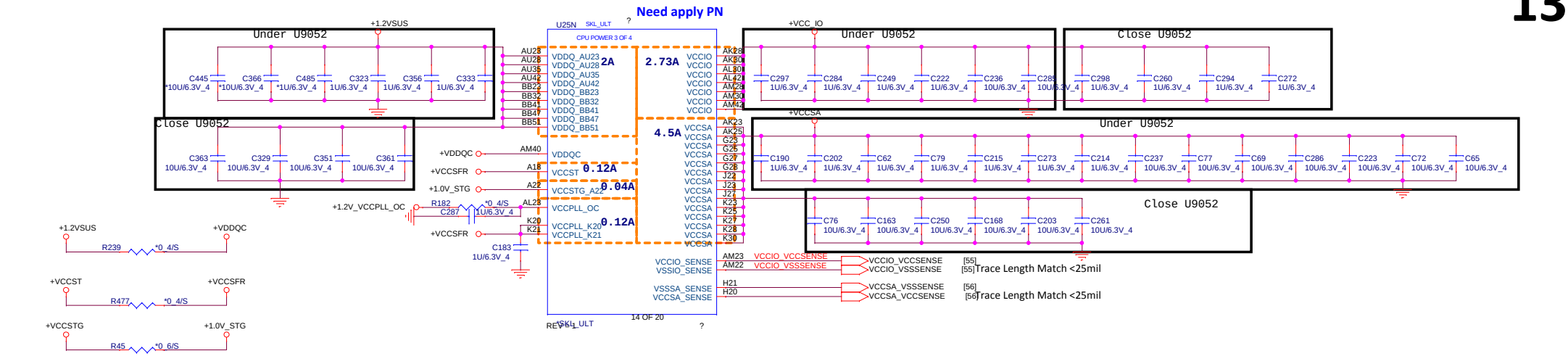
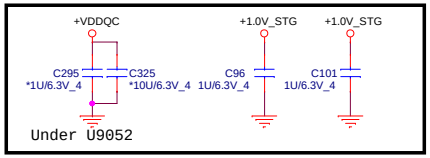
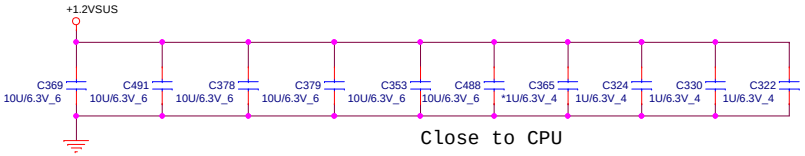
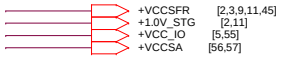


Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed









Power Rail	Description	Control
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Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	13 -- SKYLAKE (POWER-3)	1A
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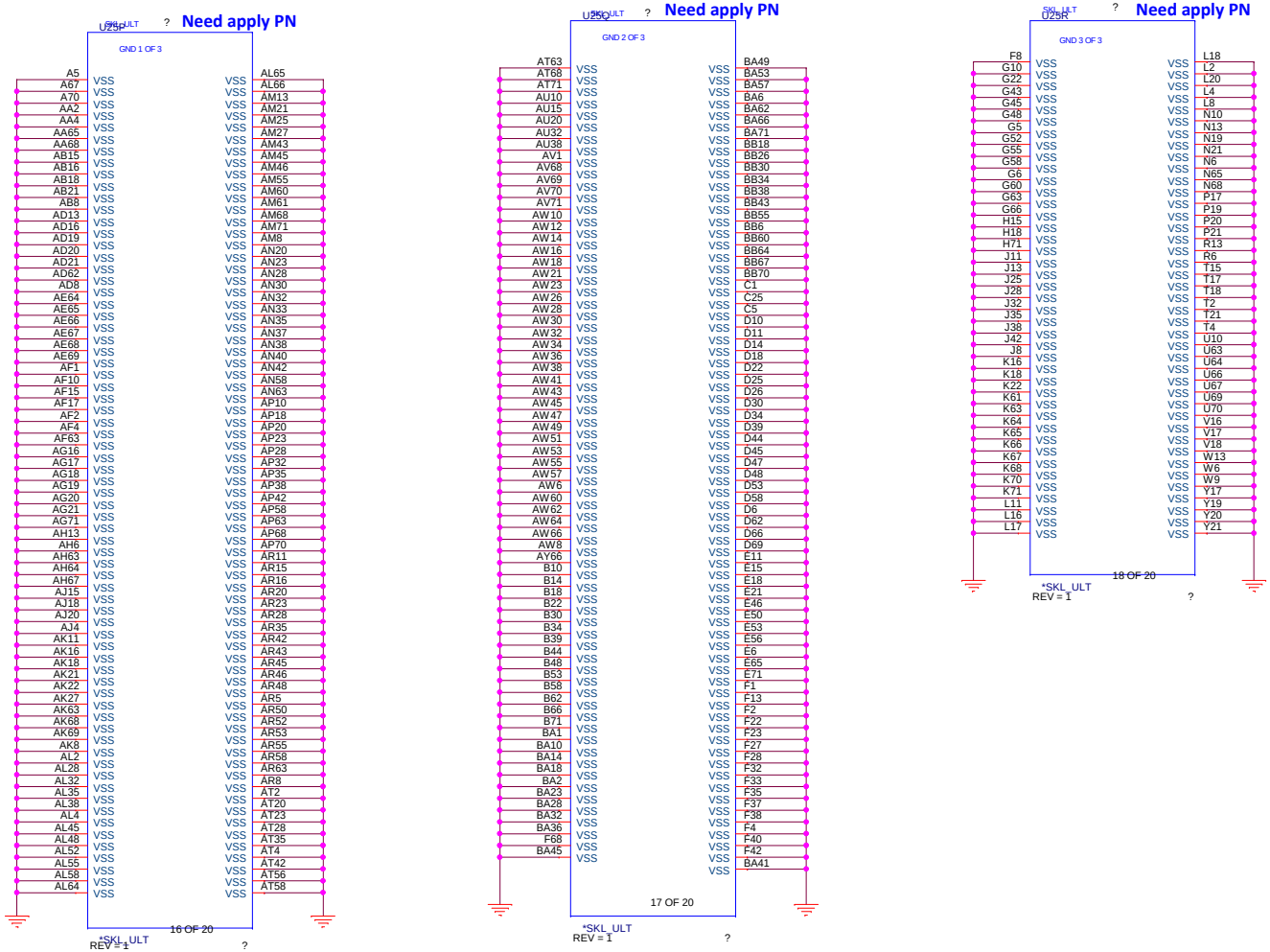

Size: Custom	Document Number: 14 -- SKYLAKE (GND)
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Quanta Computer Inc.

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NB5

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Quanta Computer Inc.

Size	Document Number	Rev
	15 -- HSW XDP & APS	1A
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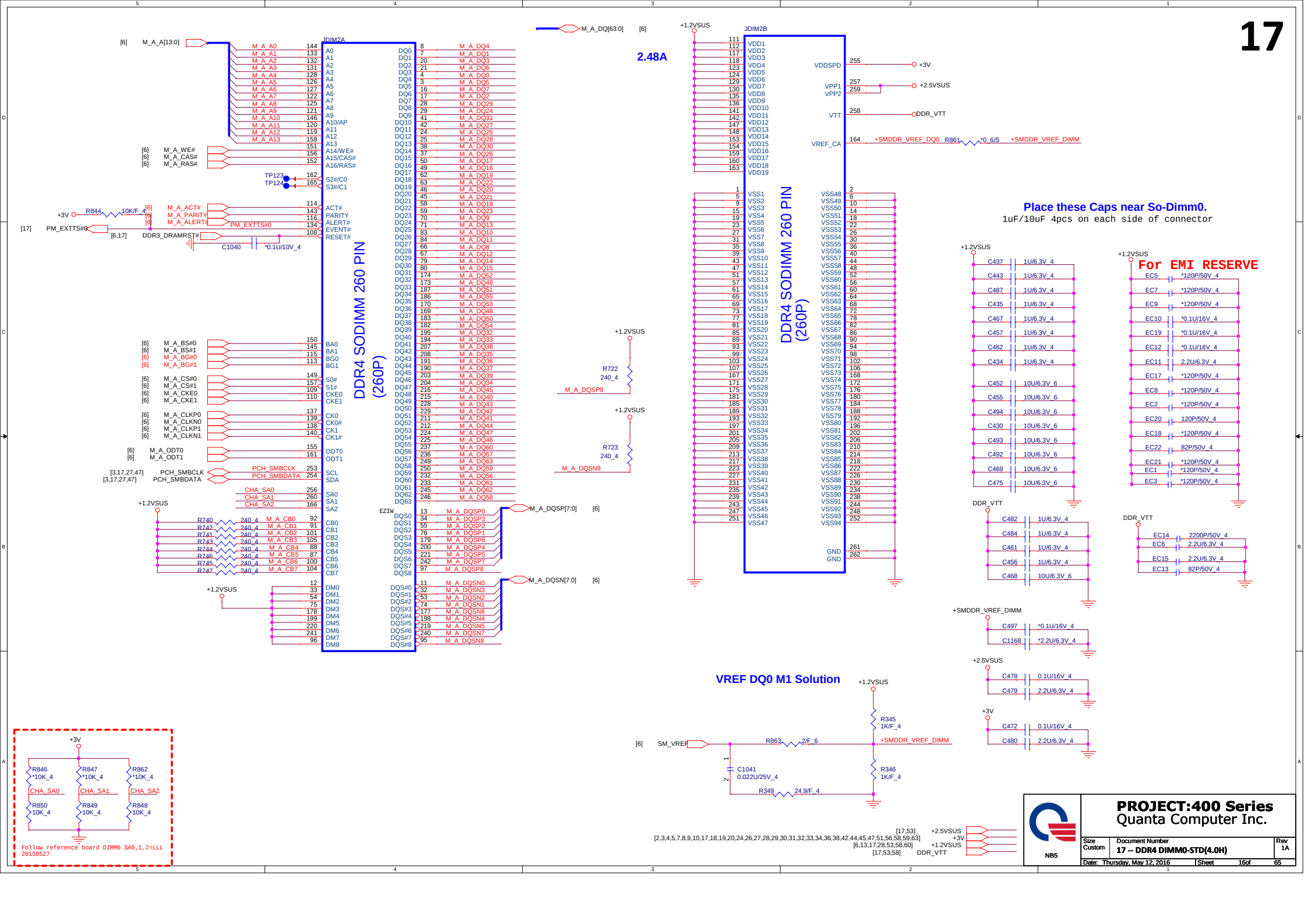
JDIM2A
DDR4 SODIMM 260 PIN (260P)
JDIM2B
DDR4 SODIMM 260 PIN (260P)
2.48A
Place these Caps near So-Dimm0.
1uF/10uF 4pcs on each side of connector
For EMI RESERVE
VREF DQ0 M1 Solution
Follow reference board DIMM0 SA0,1,2=LLL 20150527
PROJECT:400 Series
Quanta Computer Inc.
NB5
Size Custom
Document Number
17 -- DDR4 DIMM0-STD(4.0H)
Rev 1A
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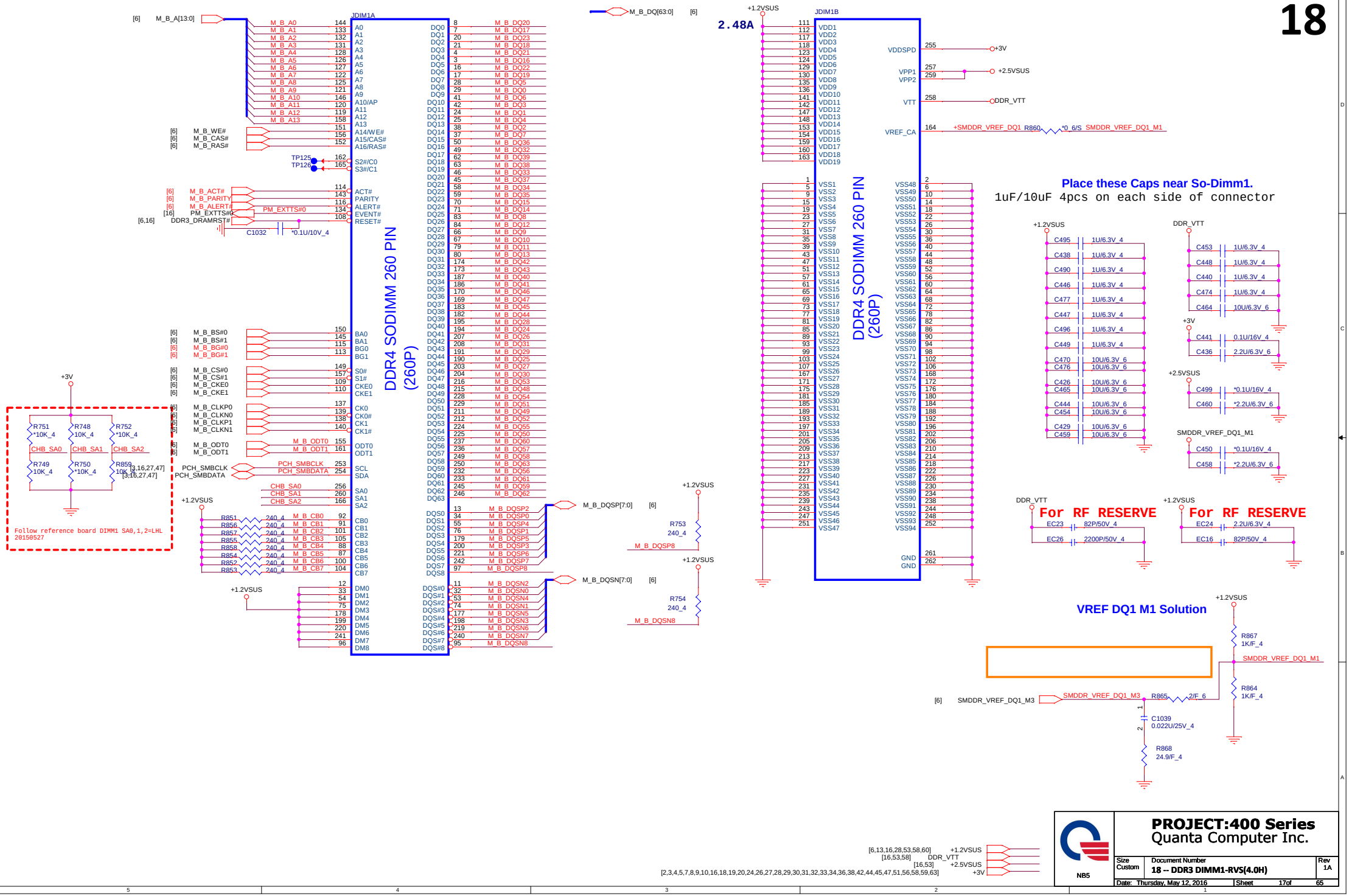
JDIM1A
DDR4 SODIMM 260 PIN (260P)
JDIM1B
DDR4 SODIMM 260 PIN (260P)
2.48A
M_B_A[13:0]
M_B_DQ[63:0]
Follow reference board DIMM1 SA0,1,2=LHL 20150527
Place these Caps near So-Dimm1.
1uF/10uF 4pcs on each side of connector
For RF RESERVE
For RF RESERVE
VREF DQ1 M1 Solution
PROJECT:400 Series
Quanta Computer Inc.
Document Number
18 -- DDR3 DIMM1-RVS(4.0H)
Rev 1A
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PEX_IOVDD + PEX_IOVDDQ = 1.042A

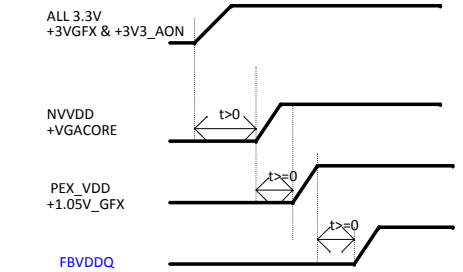
PEX_PLL_HVDD + PEX_SVDD_3V3 = 143mA

PEX_PLLVDD = 130mA

NVDD = 32.22 ~ 26.66 A

VDD33 = 56mA

Power up sequence



if stuff Da,Db,Ra,Rb, do not stuff Ua,Ub,Ca,Cb,Rc,Rd

NB5	**PROJECT:400 Series** Quanta Computer Inc.	
Size Custom	Document Number **N16S-GMR (PCIE I/F) /NVDD**	Rev 1A
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U1001B

R1012 10K/F_4 PS_FB_CLAMP F3

NC	GF119
FB_CLAMP	GF117

FBA_ODT_L FBA_CMD2 R1014 10K/F_4
FBA_ODT_H FBA_CMD18 R1016 10K/F_4
FBA_RST# FBA_CMD5 R1013 10K/F_4
FBA_CKE_L FBA_CMD3 R1017 10K/F_4
FBA_CKE_H FBA_CMD19 R1015 10K/F_4

[22]	FBA_CMD0	C27	FBA_CMD0
[22]	FBA_CMD1	C26	FBA_CMD1
[22]	FBA_CMD2	E24	FBA_CMD2
[22]	FBA_CMD3	F24	FBA_CMD3
[22,23]	FBA_CMD4	D27	FBA_CMD4
[22,23]	FBA_CMD5	D26	FBA_CMD5
[22,23]	FBA_CMD6	F25	FBA_CMD6
[22,23]	FBA_CMD7	F26	FBA_CMD7
[22,23]	FBA_CMD8	F23	FBA_CMD8
[22,23]	FBA_CMD9	G22	FBA_CMD9
[22,23]	FBA_CMD10	G23	FBA_CMD10
[22,23]	FBA_CMD11	G24	FBA_CMD11
[22,23]	FBA_CMD12	F27	FBA_CMD12
[22,23]	FBA_CMD13	G25	FBA_CMD13
[22,23]	FBA_CMD14	G27	FBA_CMD14
[22,23]	FBA_CMD15	G26	FBA_CMD15
[23]	FBA_CMD16	M24	FBA_CMD16
[23]	FBA_CMD17	M23	FBA_CMD17
[23]	FBA_CMD18	K24	FBA_CMD18
[23]	FBA_CMD19	K23	FBA_CMD19
[22,23]	FBA_CMD20	M27	FBA_CMD20
[22,23]	FBA_CMD21	M26	FBA_CMD21
[22,23]	FBA_CMD22	M25	FBA_CMD22
[22,23]	FBA_CMD23	K26	FBA_CMD23
[22,23]	FBA_CMD24	K22	FBA_CMD24
[22,23]	FBA_CMD25	J23	FBA_CMD25
[22,23]	FBA_CMD26	J25	FBA_CMD26
[22,23]	FBA_CMD27	J24	FBA_CMD27
[22,23]	FBA_CMD28	K27	FBA_CMD28
[22,23]	FBA_CMD29	K25	FBA_CMD29
[22,23]	FBA_CMD30	J27	FBA_CMD30
		J26	FBA_CMD31

+1.5V_GFX
R1021 *60.4_4 F22 FBA_DEBUG0
R1022 *60.4_4 J22 FBA_DEBUG1

[22]	VMA_CLK0	D24	FBA_CLK0
[22]	VMA_CLK0#	D25	FBA_CLK0
[23]	VMA_CLK1	N22	FBA_CLK1
[23]	VMA_CLK1#	M22	FBA_CLK1

D18		FBA_WCK01
C18		FBA_WCK01
D17		FBA_WCK23
D16		FBA_WCK23
T24		FBA_WCK45
U24		FBA_WCK45
V24		FBA_WCK67
V25		FBA_WCK67

FB_PLLAVDD = 55mA

Add La (0402) for co-lay

+1.05V_GFX L1001 *PBY160808T-300Y-N L1002 HCB1005KF-330T30 +FB_PLLAVDD
La
C1069 22U/6.3VS_6
C1070 0.1U/16V_4
C1071 0.1U/16V_4
C1072 0.1U/16V_4

F16	FB_PLLAVDD
P22	FB_PLLAVDD
H22	

FB_DLLAVDD	GF119
FB_PLLAVDD	GF117

FB_DLLAVDD = 15mA

2/14 FBA

FBA_D0	E18	VMA_DQ0
FBA_D1	F18	VMA_DQ1
FBA_D2	E16	VMA_DQ2
FBA_D3	F17	VMA_DQ3
FBA_D4	D20	VMA_DQ4
FBA_D5	D21	VMA_DQ5
FBA_D6	F20	VMA_DQ6
FBA_D7	E21	VMA_DQ7
FBA_D8	E15	VMA_DQ8
FBA_D9	D15	VMA_DQ9
FBA_D10	F15	VMA_DQ10
FBA_D11	F13	VMA_DQ11
FBA_D12	C13	VMA_DQ12
FBA_D13	B13	VMA_DQ13
FBA_D14	E13	VMA_DQ14
FBA_D15	D13	VMA_DQ15
FBA_D16	B15	VMA_DQ16
FBA_D17	C16	VMA_DQ17
FBA_D18	A13	VMA_DQ18
FBA_D19	A15	VMA_DQ19
FBA_D20	B18	VMA_DQ20
FBA_D21	A18	VMA_DQ21
FBA_D22	A19	VMA_DQ22
FBA_D23	C19	VMA_DQ23
FBA_D24	B24	VMA_DQ24
FBA_D25	C23	VMA_DQ25
FBA_D26	A25	VMA_DQ26
FBA_D27	A24	VMA_DQ27
FBA_D28	A21	VMA_DQ28
FBA_D29	B21	VMA_DQ29
FBA_D30	C20	VMA_DQ30
FBA_D31	C21	VMA_DQ31
FBA_D32	R22	VMA_DQ32
FBA_D33	R24	VMA_DQ33
FBA_D34	T22	VMA_DQ34
FBA_D35	R23	VMA_DQ35
FBA_D36	N25	VMA_DQ36
FBA_D37	N26	VMA_DQ37
FBA_D38	N23	VMA_DQ38
FBA_D39	N24	VMA_DQ39
FBA_D40	V23	VMA_DQ40
FBA_D41	V22	VMA_DQ41
FBA_D42	T23	VMA_DQ42
FBA_D43	U22	VMA_DQ43
FBA_D44	Y24	VMA_DQ44
FBA_D45	AA24	VMA_DQ45
FBA_D46	Y22	VMA_DQ46
FBA_D47	AA23	VMA_DQ47
FBA_D48	AD27	VMA_DQ48
FBA_D49	AB25	VMA_DQ49
FBA_D50	AD26	VMA_DQ50
FBA_D51	AC25	VMA_DQ51
FBA_D52	AA27	VMA_DQ52
FBA_D53	AA26	VMA_DQ53
FBA_D54	W26	VMA_DQ54
FBA_D55	Y25	VMA_DQ55
FBA_D56	R26	VMA_DQ56
FBA_D57	T25	VMA_DQ57
FBA_D58	N27	VMA_DQ58
FBA_D59	R27	VMA_DQ59
FBA_D60	V26	VMA_DQ60
FBA_D61	V27	VMA_DQ61
FBA_D62	W27	VMA_DQ62
FBA_D63	W25	VMA_DQ63

VMA_DM[7:0] [22,23]

FBA_DQM0	D19	VMA_DM0
FBA_DQM1	D14	VMA_DM1
FBA_DQM2	C17	VMA_DM2
FBA_DQM3	C22	VMA_DM3
FBA_DQM4	P24	VMA_DM4
FBA_DQM5	W24	VMA_DM5
FBA_DQM6	AA25	VMA_DM6
FBA_DQM7	U25	VMA_DM7

VMA_WDQS[7:0] [22,23]

FBA_DQS_WP0	E19	VMA_WDQS0
FBA_DQS_WP1	C15	VMA_WDQS1
FBA_DQS_WP2	B16	VMA_WDQS2
FBA_DQS_WP3	B22	VMA_WDQS3
FBA_DQS_WP4	R25	VMA_WDQS4
FBA_DQS_WP5	W23	VMA_WDQS5
FBA_DQS_WP6	AB26	VMA_WDQS6
FBA_DQS_WP7	T26	VMA_WDQS7

VMA_RDQS[7:0] [22,23]

FBA_DQS_RN0	F19	VMA_RDQS0
FBA_DQS_RN1	C14	VMA_RDQS1
FBA_DQS_RN2	A16	VMA_RDQS2
FBA_DQS_RN3	A22	VMA_RDQS3
FBA_DQS_RN4	P25	VMA_RDQS4
FBA_DQS_RN5	W22	VMA_RDQS5
FBA_DQS_RN6	AB27	VMA_RDQS6
FBA_DQS_RN7	T27	VMA_RDQS7

FB_VREF_PROBE D23

bga595-nvidia-n13p-gv2-s-a2 COMMON

VMA_DQ[63:0] VMA_DQ[63:0] [22,23]

FBVDDQ + FBVDD = 3.116A

+1.5V_GFX

C1060 0.1U/16V_4
C1061 0.1U/16V_4
C1062 1U/6.3V_4
C1065 1U/6.3V_4
C1066 4.7U/6.3V_6
C1063 4.7U/6.3V_6
C1067 10U/6.3V_6
C1064 22U/6.3V_6

U1001D 12/14 FBVDDQ

B26	FBVDDQ
C25	FBVDDQ
E23	FBVDDQ
E26	FBVDDQ
F14	FBVDDQ
F21	FBVDDQ
G13	FBVDDQ
G14	FBVDDQ
G15	FBVDDQ
G16	FBVDDQ
G18	FBVDDQ
G19	FBVDDQ
G20	FBVDDQ
G21	FBVDDQ
H24	FBVDDQ
H26	FBVDDQ
J21	FBVDDQ
K21	FBVDDQ
L22	FBVDDQ
L24	FBVDDQ
L26	FBVDDQ
M21	FBVDDQ
N21	FBVDDQ
R21	FBVDDQ
T21	FBVDDQ
V21	FBVDDQ
W21	FBVDDQ

bga595-nvidia-n13p-gv2-s-a2 COMMON

FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ R1018 40.2/F_4 +1.5V_GFX
FB_CAL_PU_GND C24 FB_CAL_PU_GND R1019 42.2/F_4
FB_CALTERM_GND B25 FB_CAL_TERM_GND R1020 51.1/F_4

U1001F 13/14 GND

A2	GND	GND	M13
AB17	GND	GND	M15
AB20	GND	GND	M17
AB24	GND	GND	N10
AC2	GND	GND	N12
AC22	GND	GND	N14
AC26	GND	GND	N16
AC5	GND	GND	N18
AC8	GND	GND	P11
AD12	GND	GND	P13
AD13	GND	GND	P15
A26	GND	GND	P17
AD15	GND	GND	P2
AD16	GND	GND	P23
AD18	GND	GND	P26
AD19	GND	GND	P5
AD21	GND	GND	R10
AD22	GND	GND	R12
AE11	GND	GND	R14
AE14	GND	GND	R16
AE17	GND	GND	R18
AE20	GND	GND	T11
AB11	GND	GND	T13
AF1	GND	GND	T15
AF11	GND	GND	T17
AF14	GND	GND	U10
AF17	GND	GND	U12
AF20	GND	GND	U14
AF23	GND	GND	U16
AF5	GND	GND	U18
AF8	GND	GND	U2
AG2	GND	GND	U23
AG26	GND	GND	U26
AB14	GND	GND	U5
B1	GND	GND	V11
B11	GND	GND	V13
B14	GND	GND	V15
B17	GND	GND	V17
B20	GND	GND	Y2
B23	GND	GND	Y23
B27	GND	GND	Y26
B5	GND	GND	Y5
B8	GND		
E11	GND		
E14	GND		
E17	GND		
E2	GND		
E20	GND		
E22	GND		
E25	GND		
E5	GND		
E8	GND		
H2	GND		
H23	GND		
H25	GND		
H5	GND		
K11	GND		
K13	GND		
K15	GND		
K17	GND		
L10	GND		
L12	GND		
L14	GND		
L16	GND		
L18	GND		
L2	GND		
L23	GND		
L25	GND		
L5	GND	GND	AA7
M11	GND	GND	AB7

bga595-nvidia-n13p-gv2-s-a2 COMMON

if stuff Da,Ra, do not stuff Ua,Ca,Rb,Rc

GC6_FB_EN
DGPU_VC_EN
D1004 *BAT54CW-7-F Da
R1123 Ra *100K/F_4
DGPU_FB_EN

For support GC6 2.0

+3V
Ua
[60] PVPCIE_PG R7748 0_4
[7,60] DGPU_PWR_EN R1023 *0_4
[59,60] DGPU_VC_EN R1024 *0_4
[8,21] GC6_FB_EN
Rc
U1003 NL17SZ32DFT2G
Ca C1068 0.1U/16V_4
Rb R1025 100K/F_4
DGPU_FB_EN [61]

NB5

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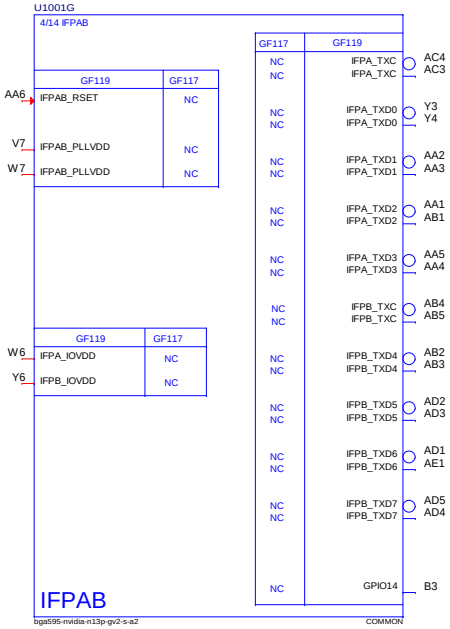

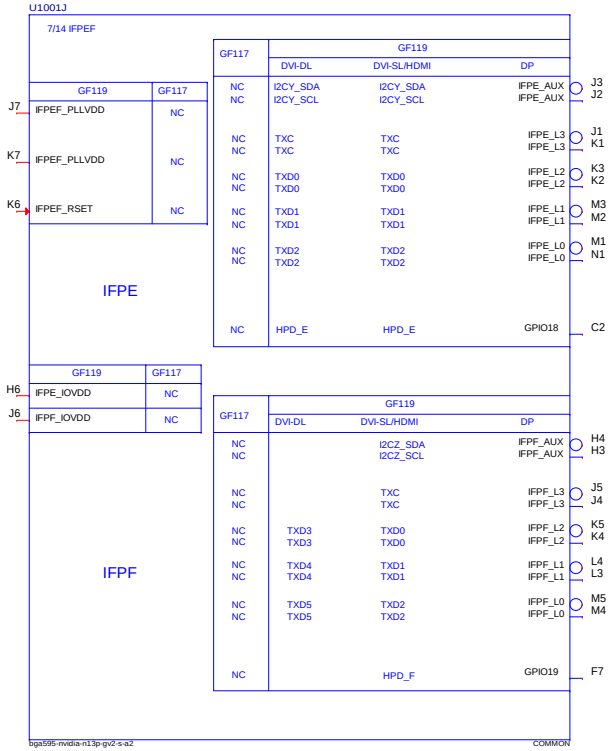

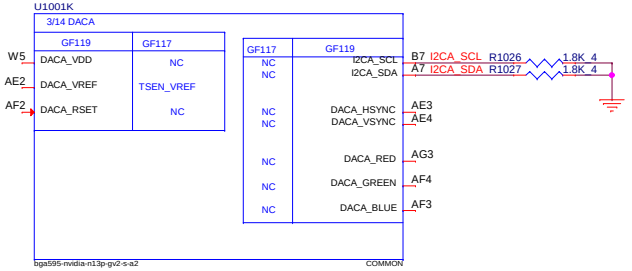

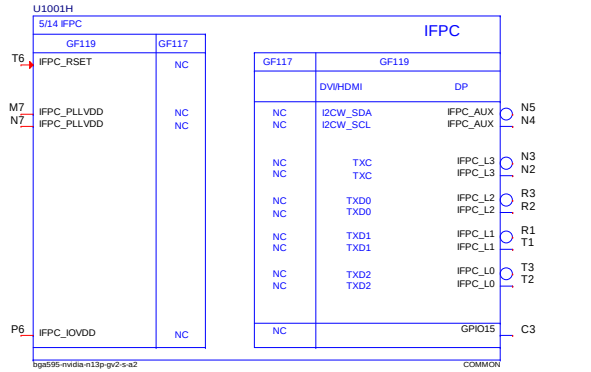

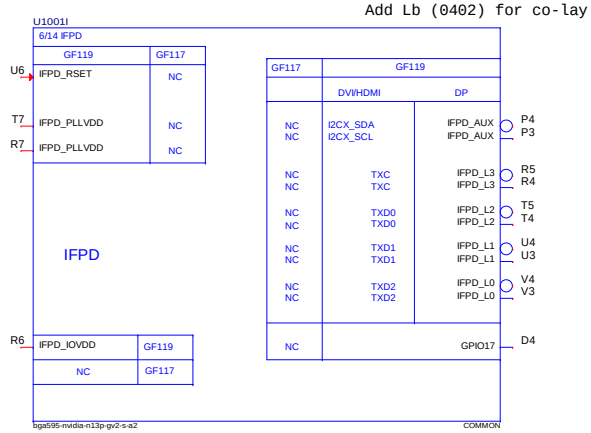

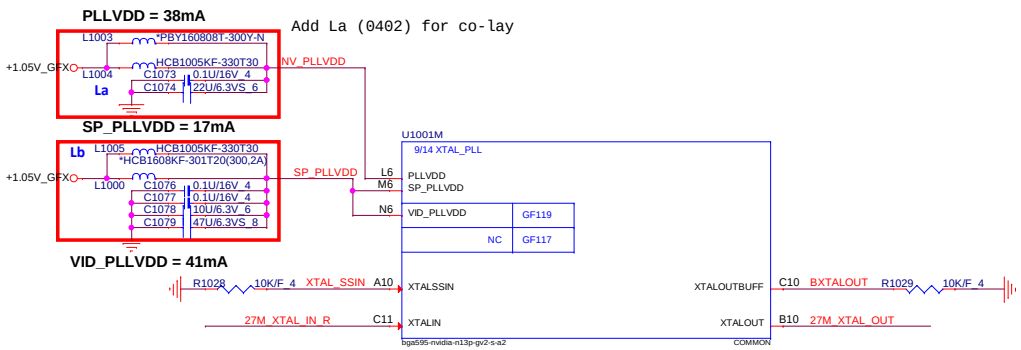

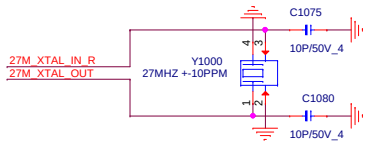

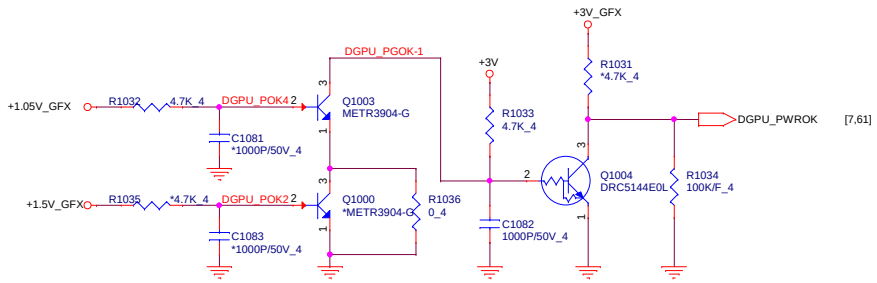

NB5
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Quanta Computer Inc.
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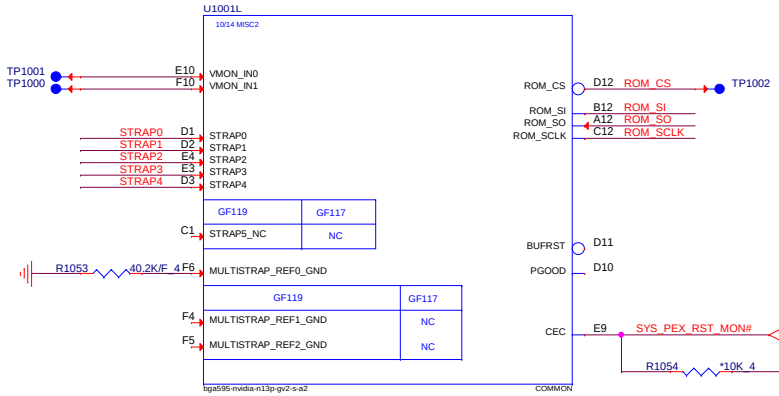

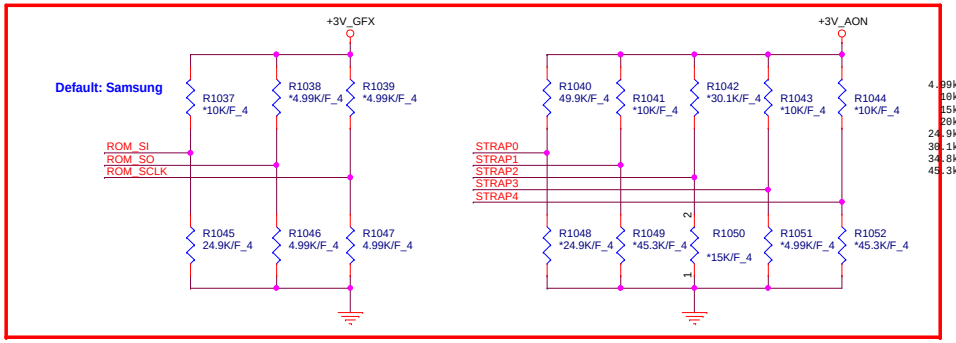

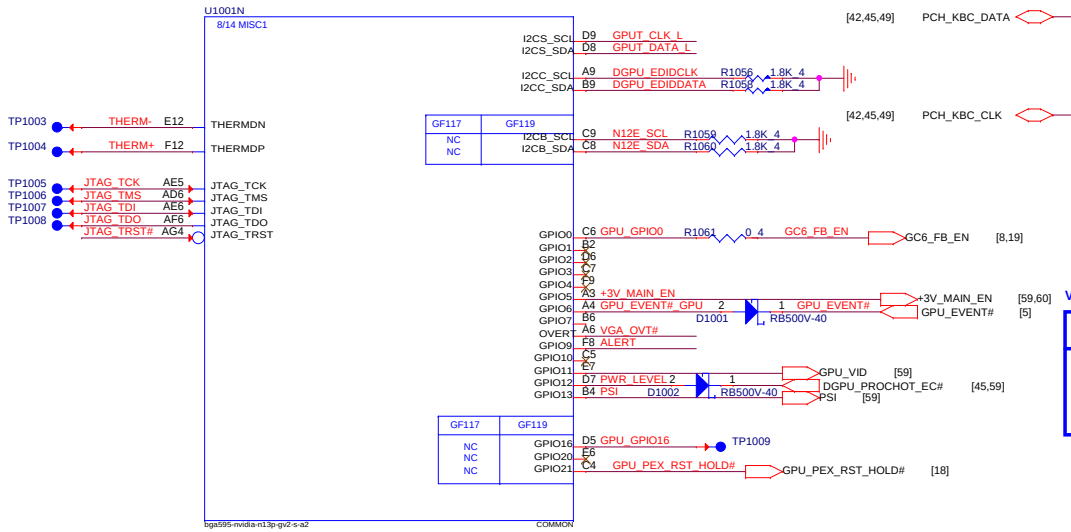

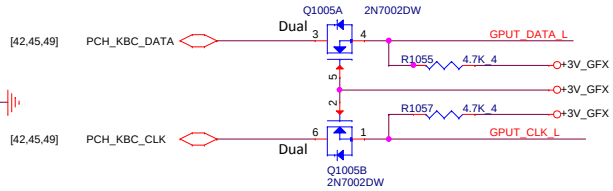

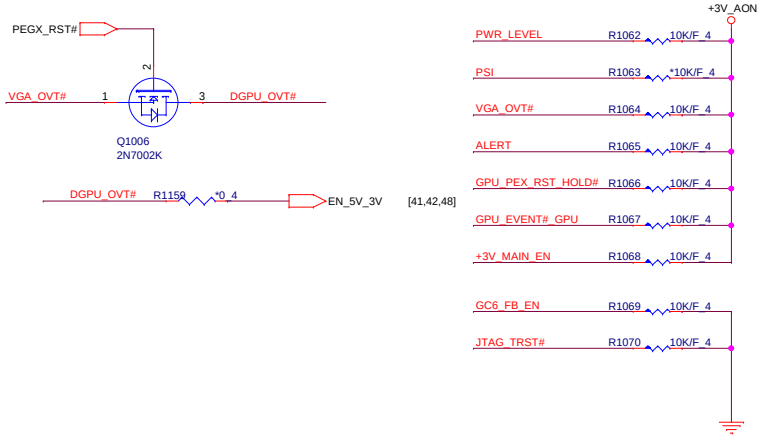

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

VRAM Configuration Table

ROM_SI	DESCRIPTION	Vendor	Vendor P/N	Straping	*TOP B/S*	QBC
0000						
0101	DDR3 - 256Mx16, 1.5V, 1.1Ghz/1.35V 1Ghz	HYNIX	H5TC4G63CFR-N0C	0x5	AKD5PZDTW01	AKD5PZDTW02
0011	DDR3 - 256Mx16, 1.5V, 1.1Ghz/1.35V 1Ghz	Micron	MT41J256M16LY-091G:N	0x3	AKD59GSTL01	AKD59GSTL00
0100	DDR3 - 256Mx16, 1.5V, 1Ghz/1.35V 900Mhz	SAMSUNG	K4W4G1646E-BC1A	0x4	AKD5PGDT500	AKD5PGDT501

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

Rank0

HYU 256Mx16, H5TC4G63AFR-11C QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646D-BC1A QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502

U1004

VRAM _DDR3_HYNIX_256MX16

stuff R1124 for
Hynix 8Gb DDP VRAM

U1005

VRAM _DDR3_HYNIX_256MX16

stuff R1125 for
Hynix 8Gb DDP VRAM

162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

reserve for Hynix 8Gb DDP VRAM

SDDR3_BGA100

	0..31	32..63
CMD0	CS0*	
CMD1	CS1*	
CMD2	ODT	
CMD3	CKE	
CMD16		CS0*
CMD17		CS1*
CMD18		ODT
CMD19		CKE

SNN_FBAO_ODT1	J1	NC/ODT1
SNN_FBAO_CKE1	J9	NC/CKE1
SNN_FBAO_CS1	L1	NC/CS1
SNN_FBAO_ZQ1	L9	NC/ZQ1

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Rank0

HYU 256Mx16, H5TC4G63AFR-11C QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646D-BC1A QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502

U1006

VREFC_VMA3 M8 VREFCA
VREFD_VMA3 H1 VREFDQ

[19,22] FBA_CMD9 N3 A0
[19,22] FBA_CMD11 P7 A1
[19,22] FBA_CMD8 P3 A2
[19,22] FBA_CMD25 N2 A3
[19,22] FBA_CMD10 P8 A4
[19,22] FBA_CMD24 P2 A5
[19,22] FBA_CMD22 R8 A6
[19,22] FBA_CMD7 R2 A7
[19,22] FBA_CMD21 T8 A8
[19,22] FBA_CMD6 R3 A9
[19,22] FBA_CMD29 L7 A10/AP
[19,22] FBA_CMD23 R7 A11
[19,22] FBA_CMD28 N7 A12/BC
[19,22] FBA_CMD20 T3 A13
[19,22] FBA_CMD4 T7 A14
[19,22] FBA_CMD14 M7 A15

[19,22] FBA_CMD12 M2 BA0
[19,22] FBA_CMD27 N8 BA1
[19,22] FBA_CMD26 M3 BA2

[19] VMA_CLK1 J7 CK
[19] VMA_CLK1# K7 CK
[19] FBA_CMD19 K9 CKE

[19] FBA_CMD18 K1 ODT
[19] FBA_CMD16 L2 CS
[19,22] FBA_CMD30 J3 RAS
[19,22] FBA_CMD15 K3 CAS
[19,22] FBA_CMD13 L3 WE

[19] VMA_WDQS4 F3 DQSL
[19] VMA_RDQS4 G3 DQSL

[19] VMA_DM4 E7 DML
[19] VMA_DM7 D3 DMU

[19] VMA_WDQS7 C7 DQSU
[19] VMA_RDQS7 B7 DQSU

[19,22] FBA_CMD5 T2 RESET

GND — 243_4 R1079 — FBA_ZQ4 L8 ZQ

DQL0 E3 VMA_DQ34 [19]
DQL1 F7 VMA_DQ37 [19]
DQL2 F2 VMA_DQ33 [19]
DQL3 F8 VMA_DQ39 [19]
DQL4 H3 VMA_DQ32 [19]
DQL5 H8 VMA_DQ38 [19]
DQL6 G2 VMA_DQ35 [19]
DQL7 H7 VMA_DQ36 [19]

DQU0 D7 VMA_DQ57 [19]
DQU1 C3 VMA_DQ61 [19]
DQU2 C8 VMA_DQ58 [19]
DQU3 C2 VMA_DQ62 [19]
DQU4 A7 VMA_DQ59 [19]
DQU5 A2 VMA_DQ63 [19]
DQU6 B8 VMA_DQ56 [19]
DQU7 A3 VMA_DQ60 [19]

VDD#B2 B2, VDD#D9 D9, VDD#G7 G7, VDD#K2 K2, VDD#K8 K8, VDD#N1 N1, VDD#N9 N9, VDD#R1 R1, VDD#R9 R9 — +1.5V_GFX — 4.7U/6.3V_6 C1115 — 0.1U/16V_4 C1116, 0.1U/16V_4 C1117 — GND

VDDQ#A1 A1, VDDQ#A8 A8, VDDQ#C1 C1, VDDQ#C9 C9, VDDQ#D2 D2, VDDQ#E9 E9, VDDQ#F1 F1, VDDQ#H2 H2, VDDQ#H9 H9 — +1.5V_GFX — 4.7U/6.3V_6 C1121 — 0.1U/16V_4 C1122, 0.1U/16V_4 C1123 — GND

VSS#A9 A9, VSS#B3 B3, VSS#E1 E1, VSS#G8 G8, VSS#J2 J2, VSS#J8 J8, VSS#M1 M1, VSS#M9 M9, VSS#P1 P1, VSS#P9 P9, VSS#T1 T1, VSS#T9 T9 — GND

VSSQ#B1 B1, VSSQ#B9 B9, VSSQ#D1 D1, VSSQ#D8 D8, VSSQ#E2 E2, VSSQ#E8 E8, VSSQ#F9 F9, VSSQ#G1 G1, VSSQ#G9 G9

[19] FBA_CMD17 — FBA_CMD18 J1 NC#J1, FBA_CMD17 L1 NC#L1, FBA_CMD19 J9 NC#J9, FBA_ZQ6 L9 NC#L9 — GND — 243_4 R1126

96-BALL SDRAM DDR3 VRAM _DDR3_HYNIX_256MX16

stuff R1124 for Hynix 8Gb DDP VRAM

162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

VMA_CLK1 — R1078 162_4 — VMA_CLK1#

+1.5V_GFX — R1081 1.33K/F_4 — VREFC_VMA3 — R1083 1.33K/F_4 — C1127 0.01U/50V_4

+1.5V_GFX — R1082 1.33K/F_4 — VREFD_VMA3 — R1084 1.33K/F_4 — C1128 0.01U/50V_4

+1.5V_GFX — C1134 1U/6.3V_4, C1137 1U/6.3V_4, C1139 1U/6.3V_4, C1142 1U/6.3V_4

+1.5V_GFX — C1135 1U/6.3V_4, C1138 1U/6.3V_4, C1140 1U/6.3V_4, C1143 1U/6.3V_4

+1.5V_GFX — C1129 10U/6.3V_6, C1130 10U/6.3V_6, C1131 10U/6.3V_6, C1132 0.1U/16V_4, C1133 0.1U/16V_4, C1136 0.1U/16V_4, C1141 0.1U/16V_4, C1144 0.1U/16V_4, C1145 0.1U/16V_4

U1007

VREFC_VMA3 M8 VREFCA
VREFD_VMA3 H1 VREFDQ

FBA_CMD9 N3 A0
FBA_CMD11 P7 A1
FBA_CMD8 P3 A2
FBA_CMD25 N2 A3
FBA_CMD10 P8 A4
FBA_CMD24 P2 A5
FBA_CMD22 R8 A6
FBA_CMD7 R2 A7
FBA_CMD21 T8 A8
FBA_CMD6 R3 A9
FBA_CMD29 L7 A10/AP
FBA_CMD23 R7 A11
FBA_CMD28 N7 A12/BC
FBA_CMD20 T3 A13
FBA_CMD4 T7 A14
FBA_CMD14 M7 A15

FBA_CMD12 M2 BA0
FBA_CMD27 N8 BA1
FBA_CMD26 M3 BA2

VMA_CLK1 J7 CK
VMA_CLK1# K7 CK
FBA_CMD19 K9 CKE

FBA_CMD18 K1 ODT
FBA_CMD16 L2 CS
FBA_CMD30 J3 RAS
FBA_CMD15 K3 CAS
FBA_CMD13 L3 WE

[19] VMA_WDQS5 F3 DQSL
[19] VMA_RDQS5 G3 DQSL

[19] VMA_DM5 E7 DML
[19] VMA_DM6 D3 DMU

[19] VMA_WDQS6 C7 DQSU
[19] VMA_RDQS6 B7 DQSU

FBA_CMD5 T2 RESET

GND — 243_4 R1080 — FBA_ZQ5 L8 ZQ

DQL0 E3 VMA_DQ41 [19]
DQL1 F7 VMA_DQ47 [19]
DQL2 F2 VMA_DQ42 [19]
DQL3 F8 VMA_DQ45 [19]
DQL4 H3 VMA_DQ40 [19]
DQL5 H8 VMA_DQ46 [19]
DQL6 G2 VMA_DQ43 [19]
DQL7 H7 VMA_DQ44 [19]

DQU0 D7 VMA_DQ51 [19]
DQU1 C3 VMA_DQ52 [19]
DQU2 C8 VMA_DQ48 [19]
DQU3 C2 VMA_DQ55 [19]
DQU4 A7 VMA_DQ49 [19]
DQU5 A2 VMA_DQ54 [19]
DQU6 B8 VMA_DQ50 [19]
DQU7 A3 VMA_DQ53 [19]

VDD#B2 B2, VDD#D9 D9, VDD#G7 G7, VDD#K2 K2, VDD#K8 K8, VDD#N1 N1, VDD#N9 N9, VDD#R1 R1, VDD#R9 R9 — +1.5V_GFX — 4.7U/6.3V_6 C1118 — 0.1U/16V_4 C1119, 0.1U/16V_4 C1120 — GND

VDDQ#A1 A1, VDDQ#A8 A8, VDDQ#C1 C1, VDDQ#C9 C9, VDDQ#D2 D2, VDDQ#E9 E9, VDDQ#F1 F1, VDDQ#H2 H2, VDDQ#H9 H9 — +1.5V_GFX — 4.7U/6.3V_6 C1124 — 0.1U/16V_4 C1125, 0.1U/16V_4 C1126 — GND

VSS#A9 A9, VSS#B3 B3, VSS#E1 E1, VSS#G8 G8, VSS#J2 J2, VSS#J8 J8, VSS#M1 M1, VSS#M9 M9, VSS#P1 P1, VSS#P9 P9, VSS#T1 T1, VSS#T9 T9 — GND

VSSQ#B1 B1, VSSQ#B9 B9, VSSQ#D1 D1, VSSQ#D8 D8, VSSQ#E2 E2, VSSQ#E8 E8, VSSQ#F9 F9, VSSQ#G1 G1, VSSQ#G9 G9

FBA_CMD18 J1 NC#J1, FBA_CMD17 L1 NC#L1, FBA_CMD19 J9 NC#J9, FBA_ZQ7 L9 NC#L9 — GND — 243_4 R1127

96-BALL SDRAM DDR3 VRAM _DDR3_HYNIX_256MX16

stuff R1124 for Hynix 8Gb DDP VRAM

NB5

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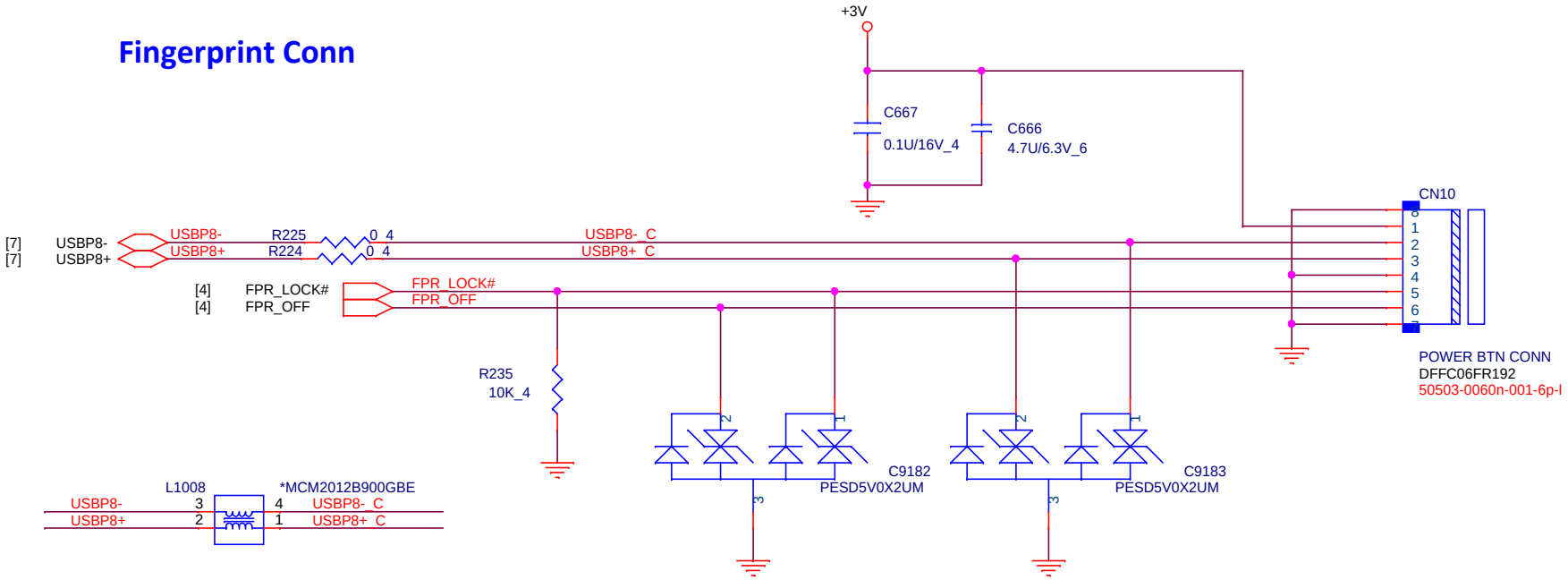

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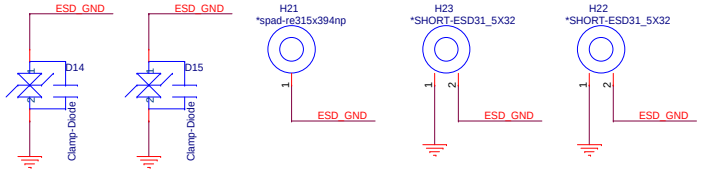

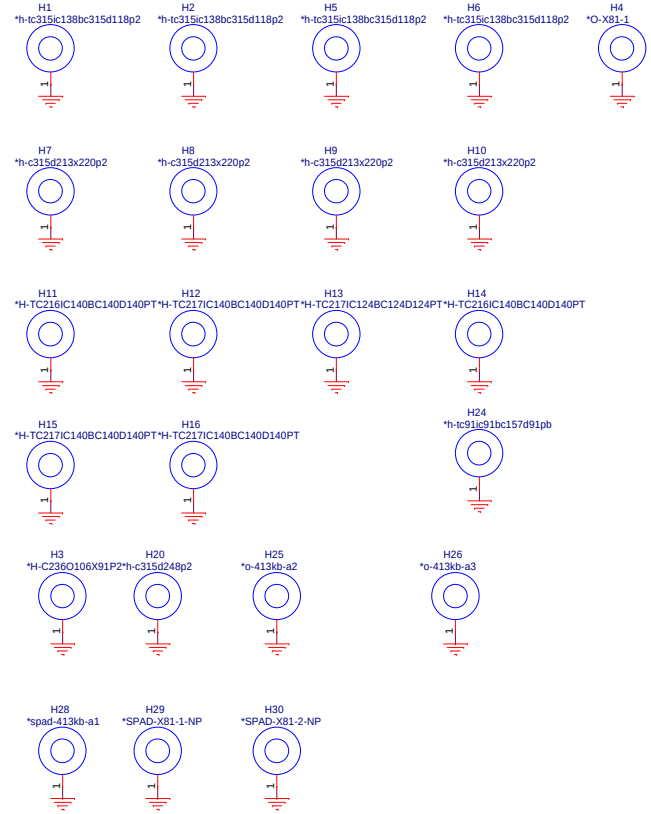

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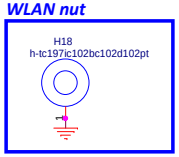

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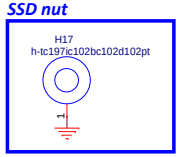
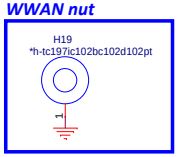
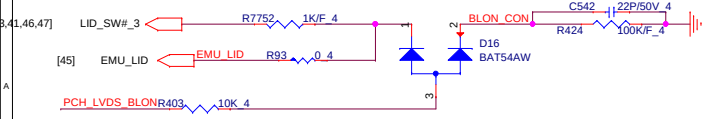


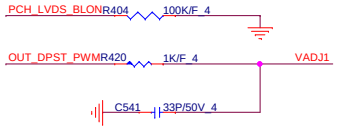
WWAN nut

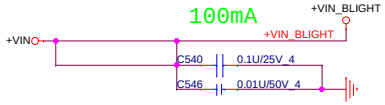


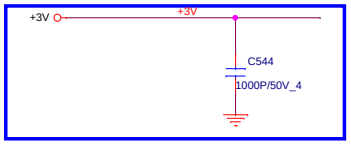
NB5	**PROJECT:400 Series** Quanta Computer Inc.	
Size: Custom	Document Number: **25 -- LVDS converter RTD2136**	Rev: 1A
Date: Thursday, May 12, 2016	Sheet: 25of 65	

LID Switch

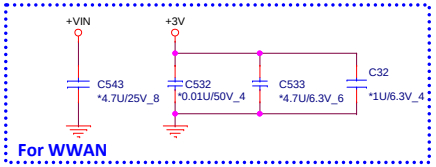


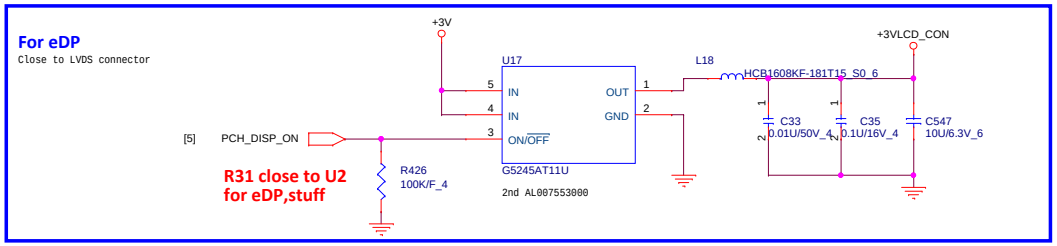


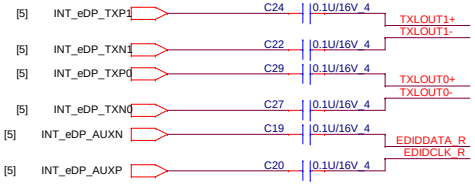


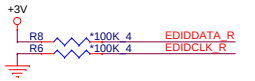


ALF@20151019:
1. Designed Reserve 4Pins for IR CCD Pin 26 to Pin29
2.Combined the +3V & +3V_CAM & +3V_IR at Pin26~25



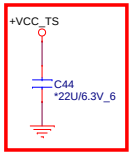


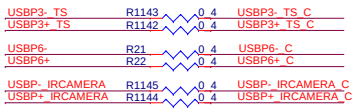




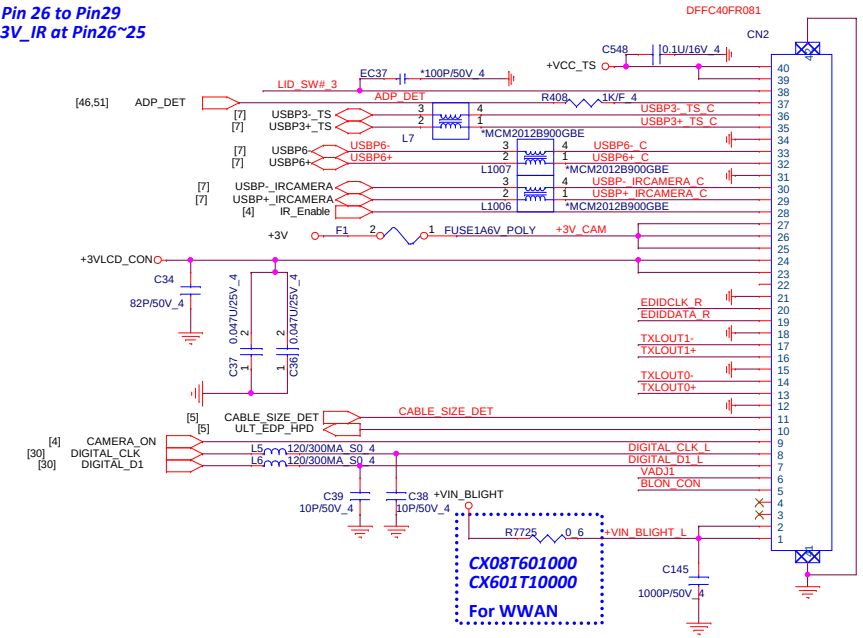
LVDS Conn.

26





GS12401-1011-9H
lvds-50671-04041-001-40p-l

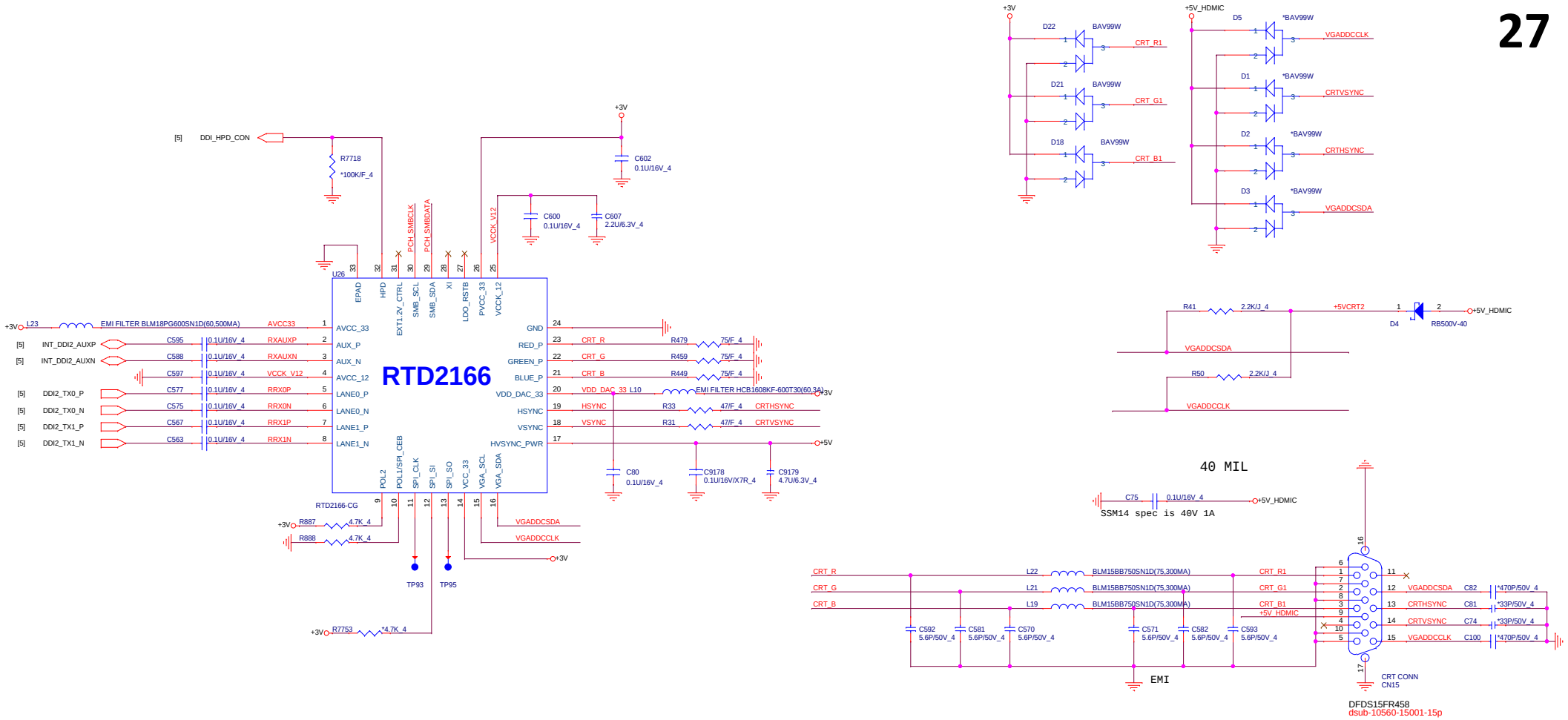


[2,3,4,5,7,8,9,10,16,17,18,19,20,24,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63] +3V
[8,27,29,30,40,42,43,54,58,63] +5V
[28,44,51,52,53,54,55,56,57,58,59,61,66] +VIN

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	26 -- LCD CONN/LID/CAM/D-MIC	1A
Date: Thursday, May 12, 2016	Sheet 26 of 65	

NB5



CIIC_SCL, CIIC_SDA Connection

EP mode: Pin2, Pin3 connect to EC SMBUS

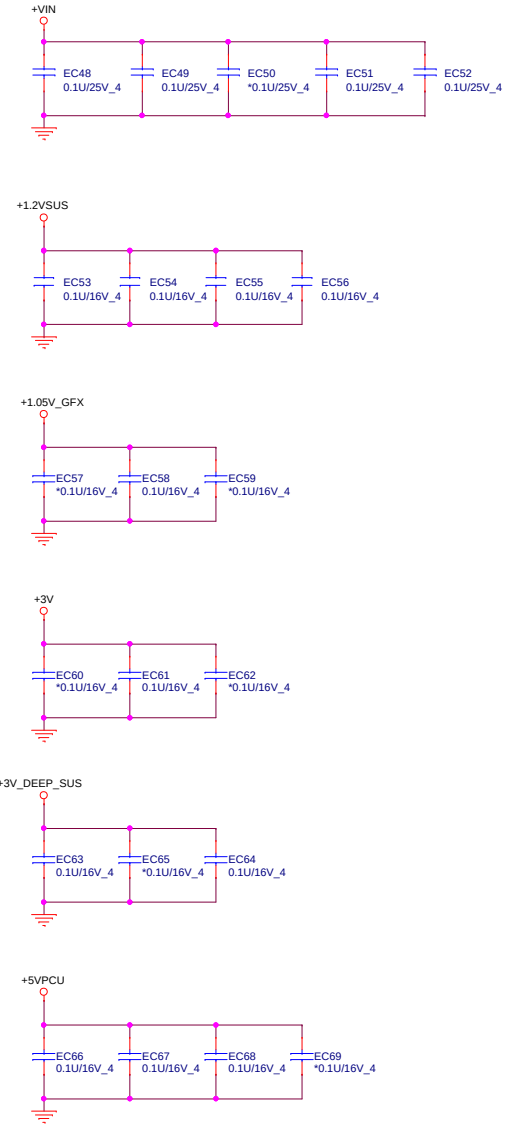
ROM or EEPROM mode: connect to PCH SMBUS

IIC Protocol is used

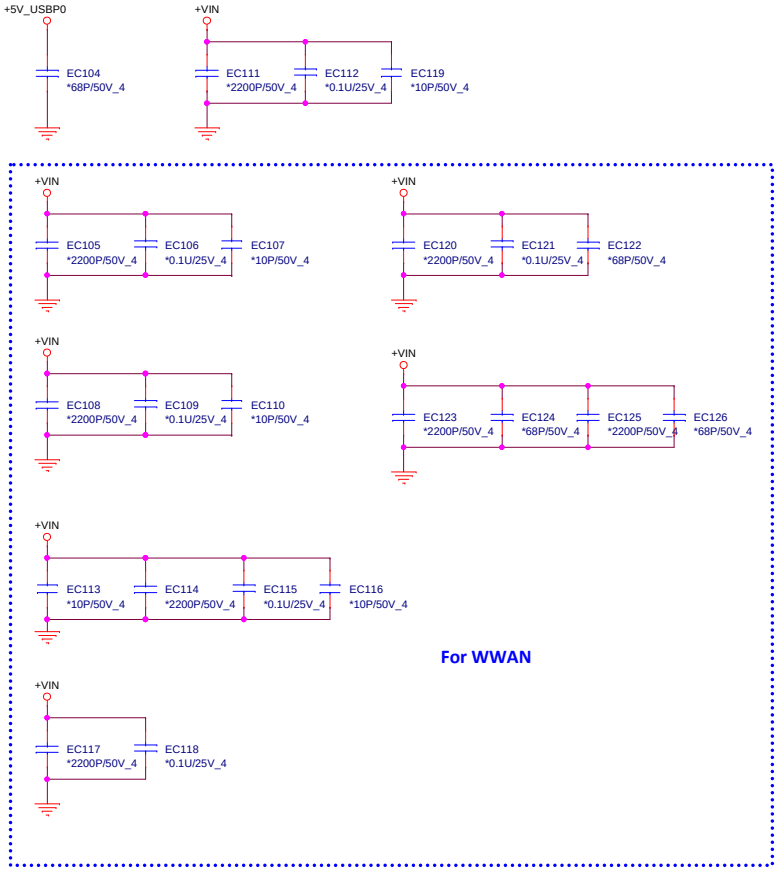
RTD2168 Slave Address:
0x64/0x65 and 0x68/0x69

NB5	PROJECT:400 Series Quanta Computer Inc.	
Size: Custom	Document Number: DP to VGA	Rev: 1A
Date: Thursday, May 12, 2016	Sheet 27 of 65	

EMI CAP

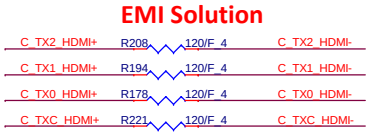


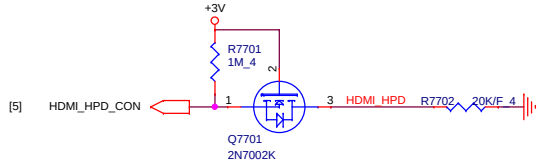
RF Cap

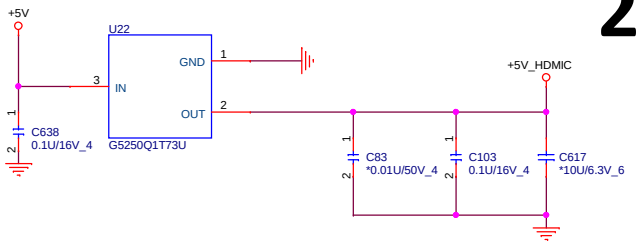


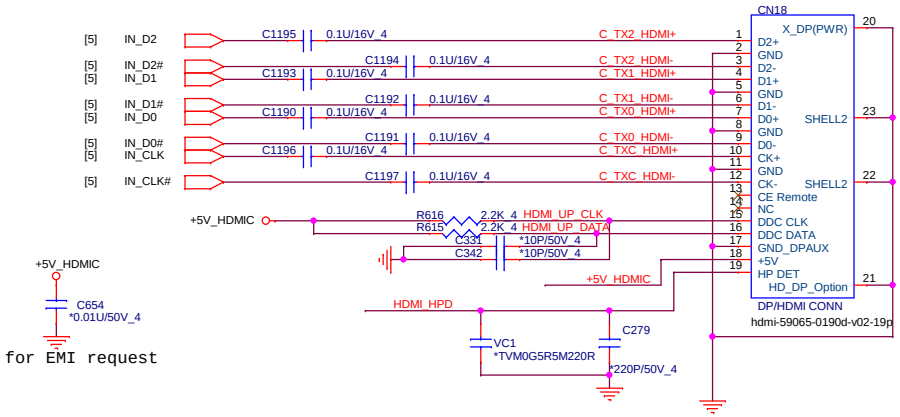
NB5	**PROJECT:400 Series** Quanta Computer Inc.	
Size: Custom	Document Number: **28 – REPEATER PS8407A**	Rev: 1A
Date: Thursday, May 12, 2016	Sheet 28 of 65	

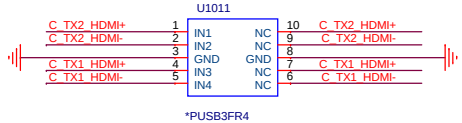
EMI Solution

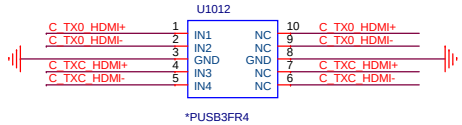




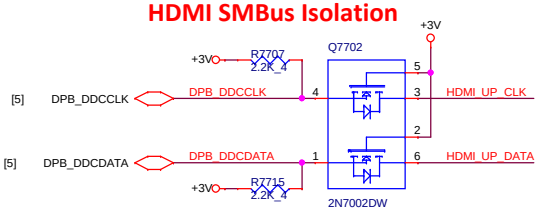




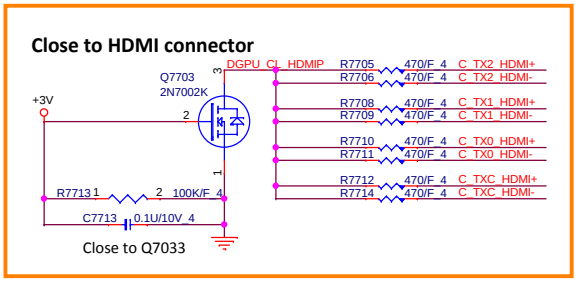




HDMI SMBus Isolation



Close to HDMI connector

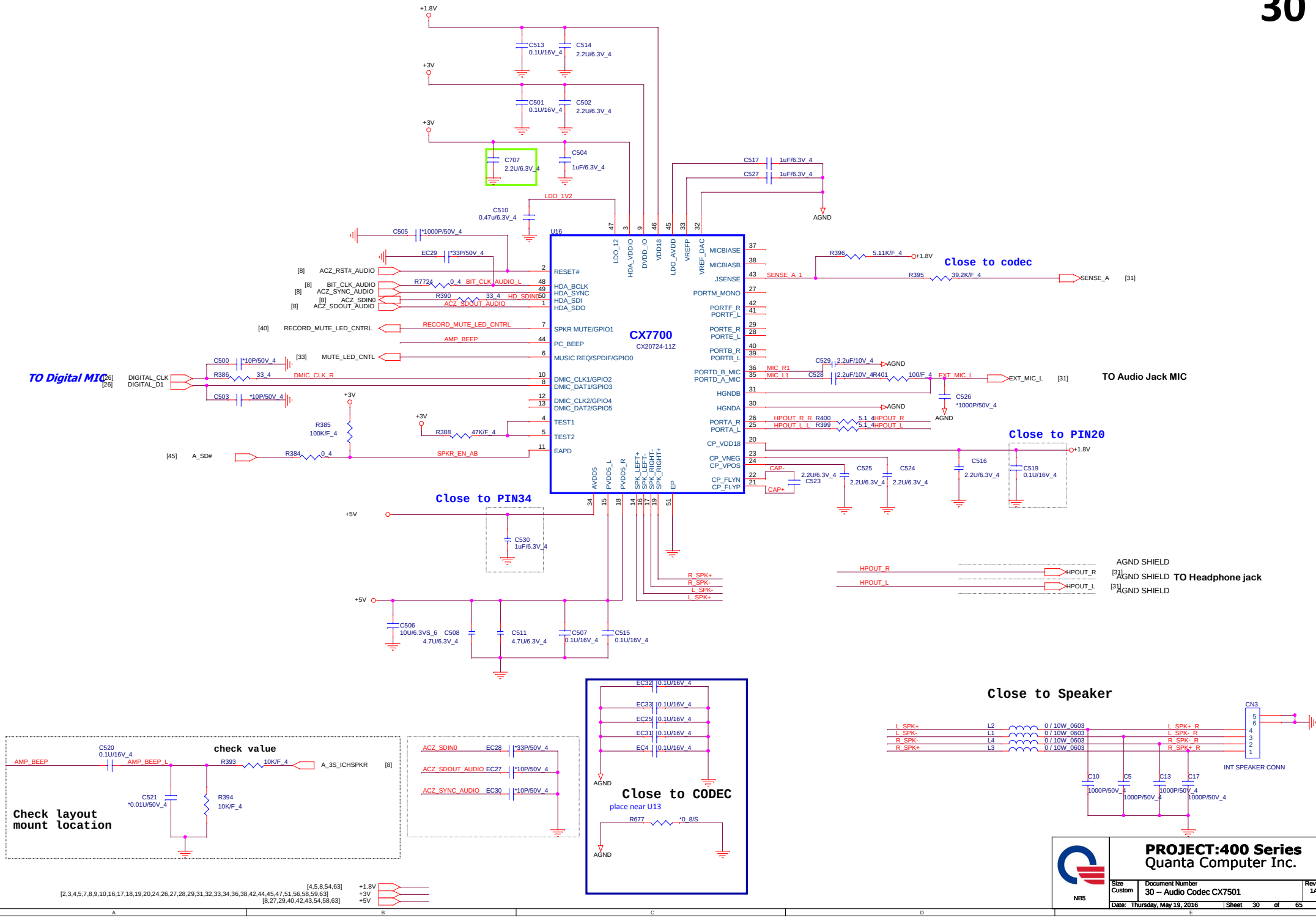


PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	29 -- HDMI CONNECTOR	1A
Date: Thursday, May 12, 2016	Sheet 29 of 65	

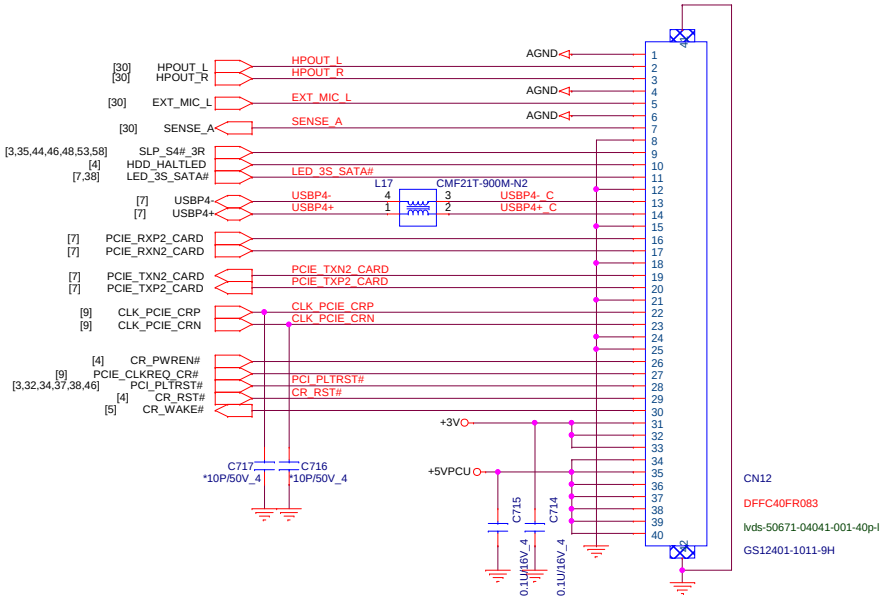
NB5

Audio Codec



NB5	PROJECT:400 Series Quanta Computer Inc.		
Size: Custom	Document Number: 30 -- Audio Codec CX7501		Rev: 1A
Date: Thursday, May 19, 2016	Sheet 30 of 65		

USB/Card Reader/Headphone_Mic Combo Jack Daugther Board Connector

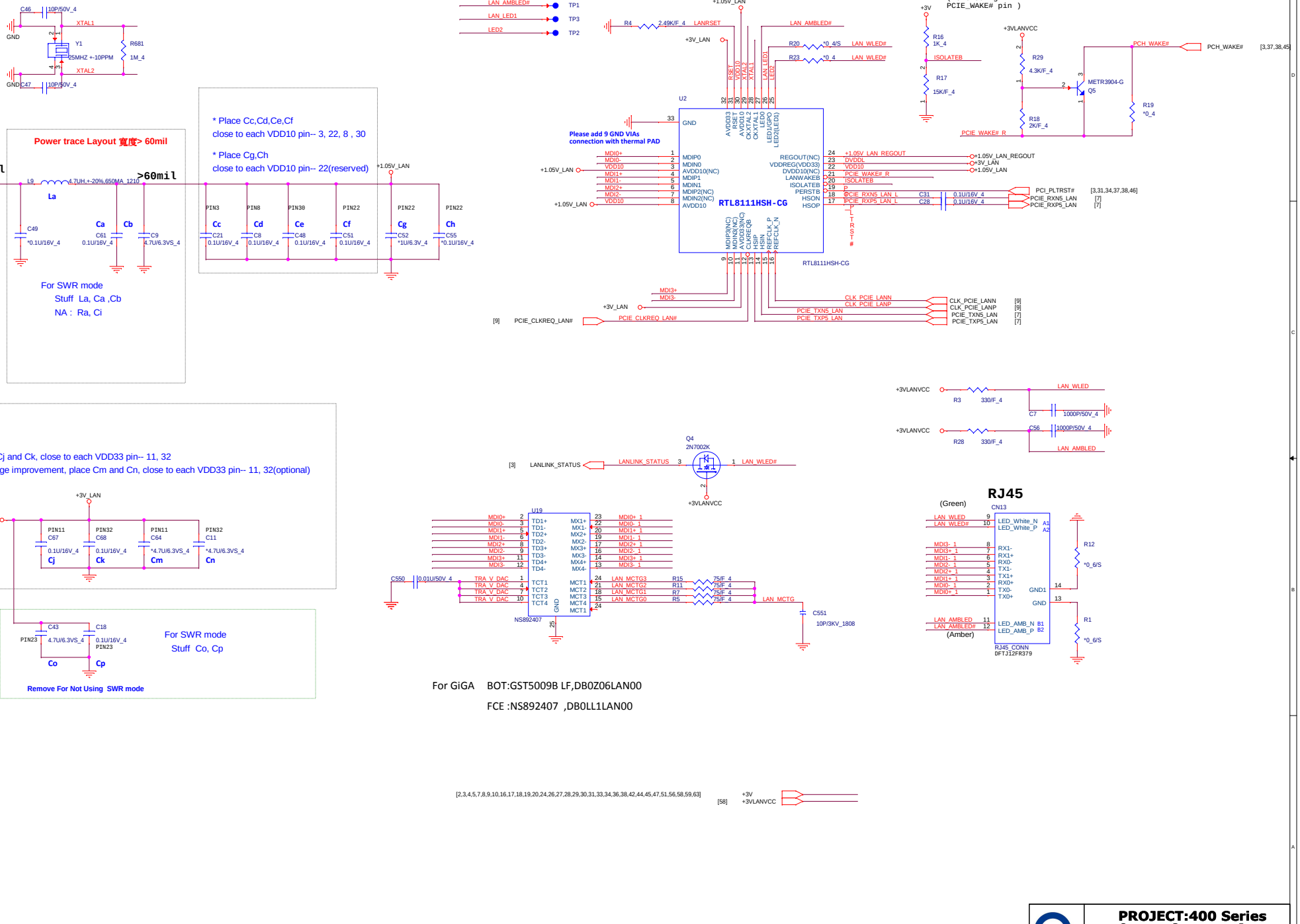


NB5	PROJECT:400 Series Quanta Computer Inc.	
Size: Custom	Document Number: 31 -- DAUGTHER BOARD CONN.	Rev: 1A
Date: Thursday, May 12, 2016	Sheet 31 of 65	

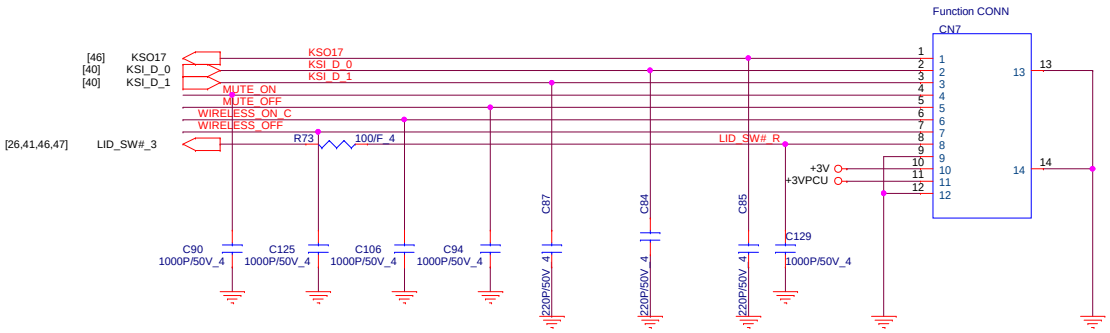
400 series 0930 whole page

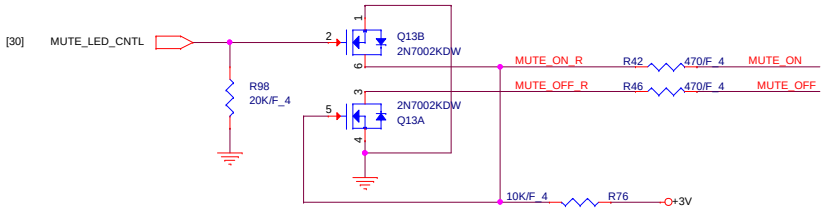
LAN & RJ45

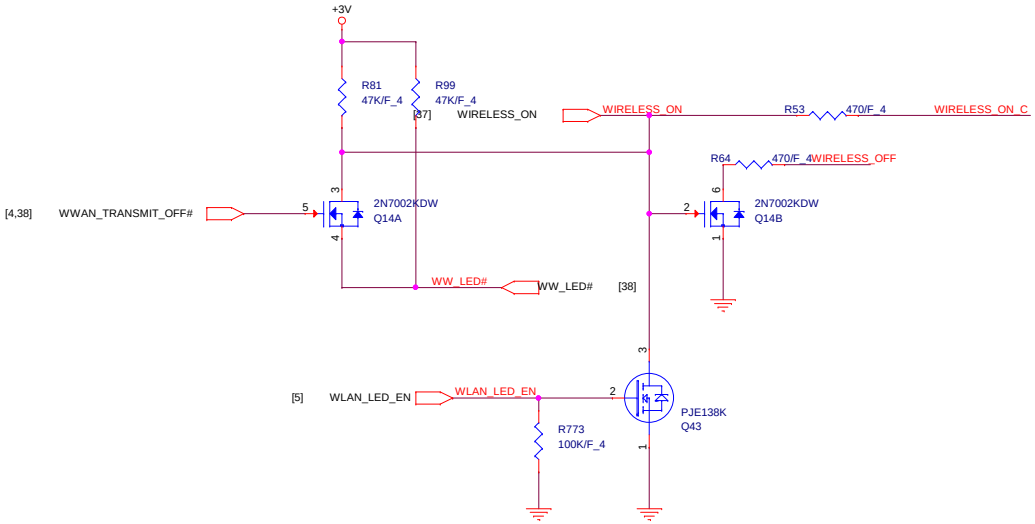
if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)



NB5	PROJECT:400 Series Quanta Computer Inc.		
	Size C	Document Number 32 -- LAN RTL8111HSH-CG/RJ45	Rev 1A
	Date: Thursday, May 12, 2016	Sheet 32 of 65	

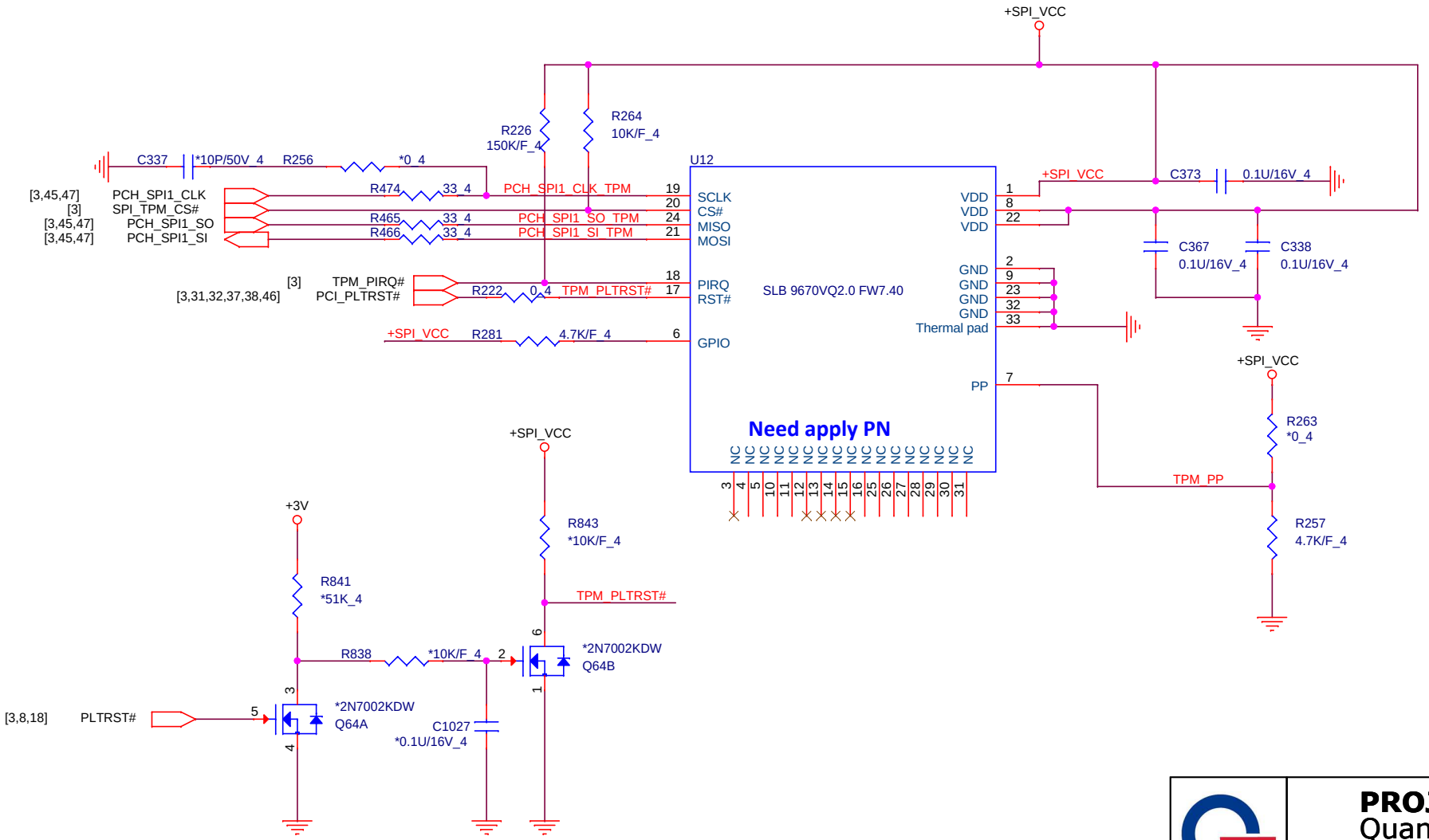






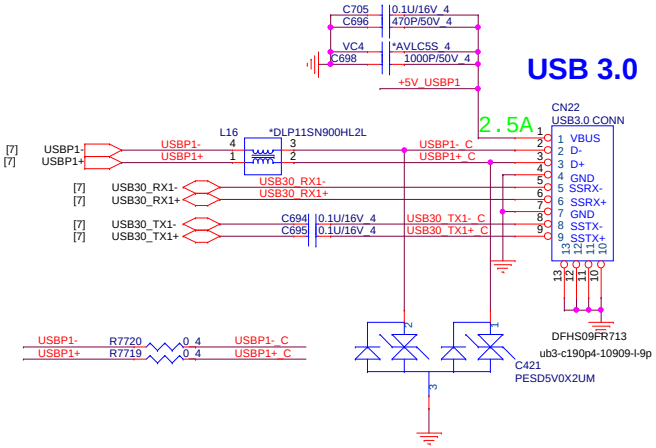
NB5	**PROJECT:400 Series** Quanta Computer Inc.	
Size: Custom	Document Number: **33 -- Function Conn.**	Rev: 1A
Date: Thursday, May 12, 2016	Sheet 33 of 65	

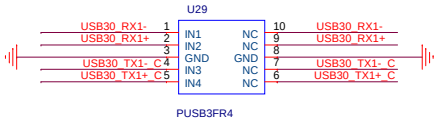
TPM (1.2 or 2.0)

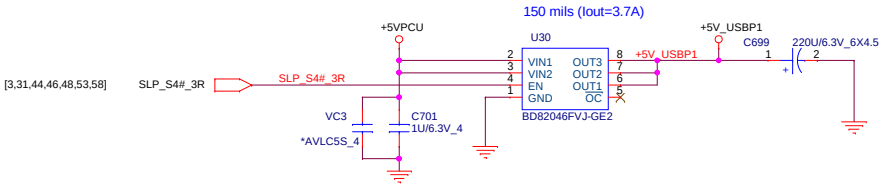


NB5	**PROJECT:400 Series** Quanta Computer Inc.	
Size: Custom	Document Number: **34 -- TPM SLB9670_QFN**	Rev: 1A
Date: Thursday, May 12, 2016	Sheet: 34of 65	

USB 2.0/3.0 Combo







[28,31,44,49,50,51,52,53,54,56,57,58,59,60,61,63] +5VPCU

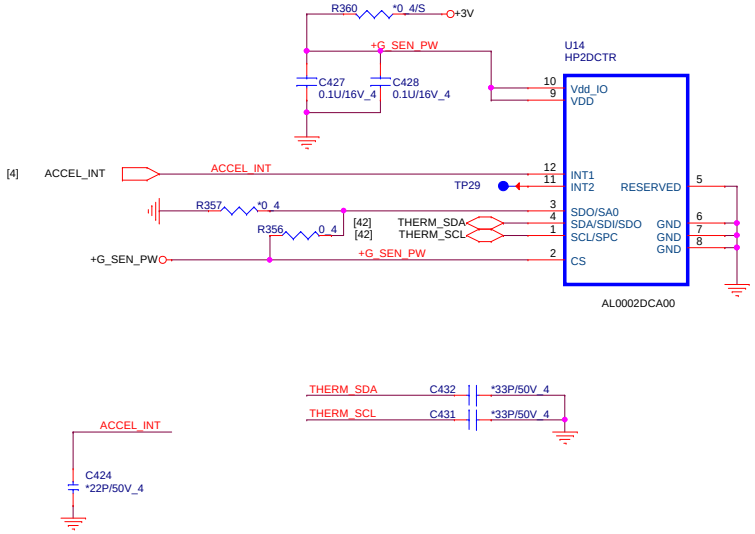
[3,10,33,37,38,40,41,42,44,45,46,48,49,51,52,53,55,58,60,62,63] +3VPCU

NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	35 – USB3.0 x2	1A
Date: Tuesday, May 17, 2016	Sheet 35 of 65	

Accelerometer Sensor



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[3,10,33,37,38,40,41,42,44,45,46,48,49,51,52,53,55,58,60,62,63] +3VPCU

NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	36 -- TS and Accelerometer	1A

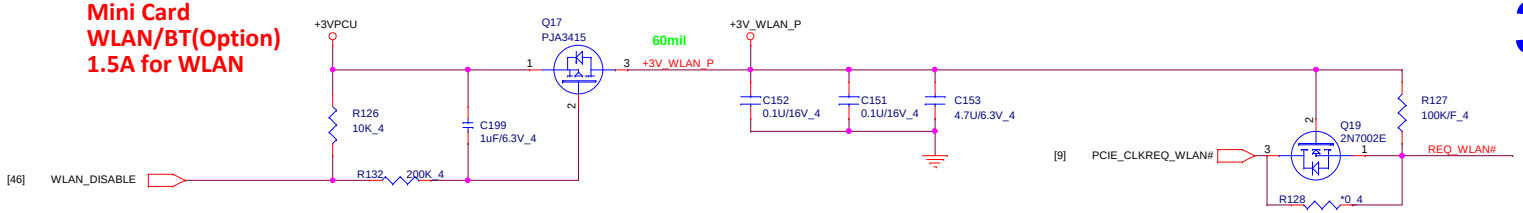
Date: Thursday, May 12, 2016 | Sheet 36of 65

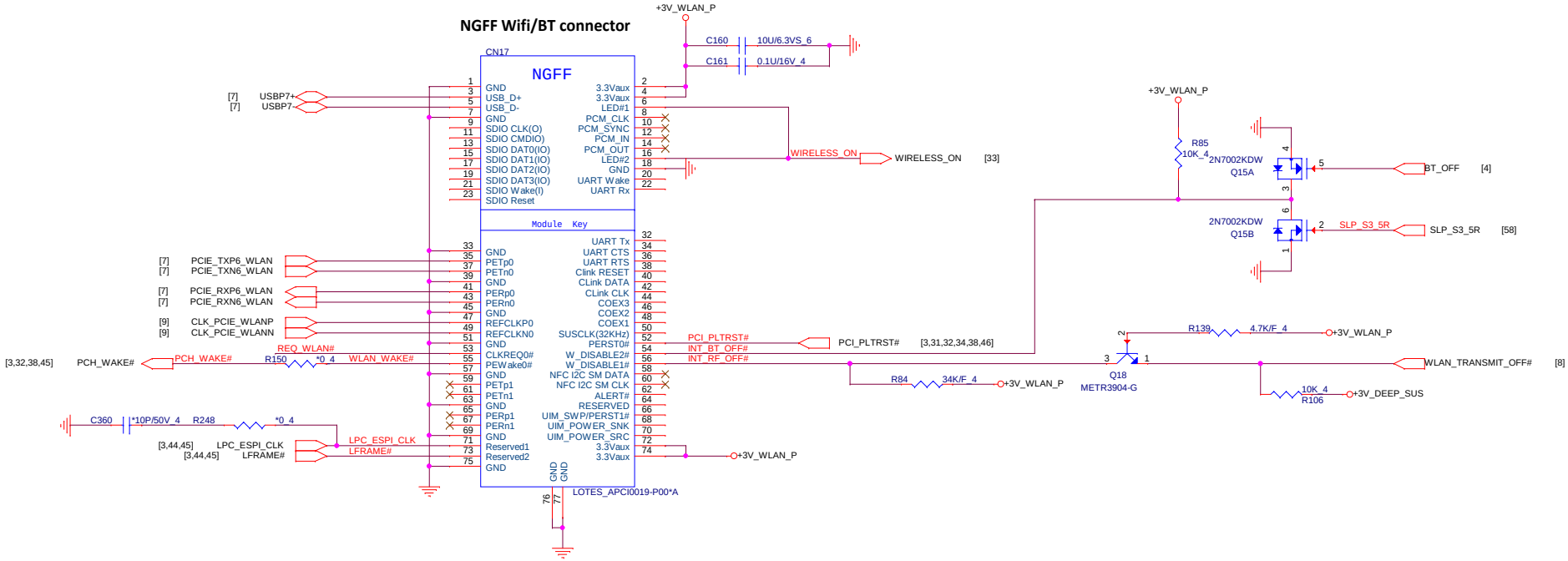
NGFF WLAN/BT

EC-B-03

Mini Card
WLAN/BT(Option)
1.5A for WLAN

37





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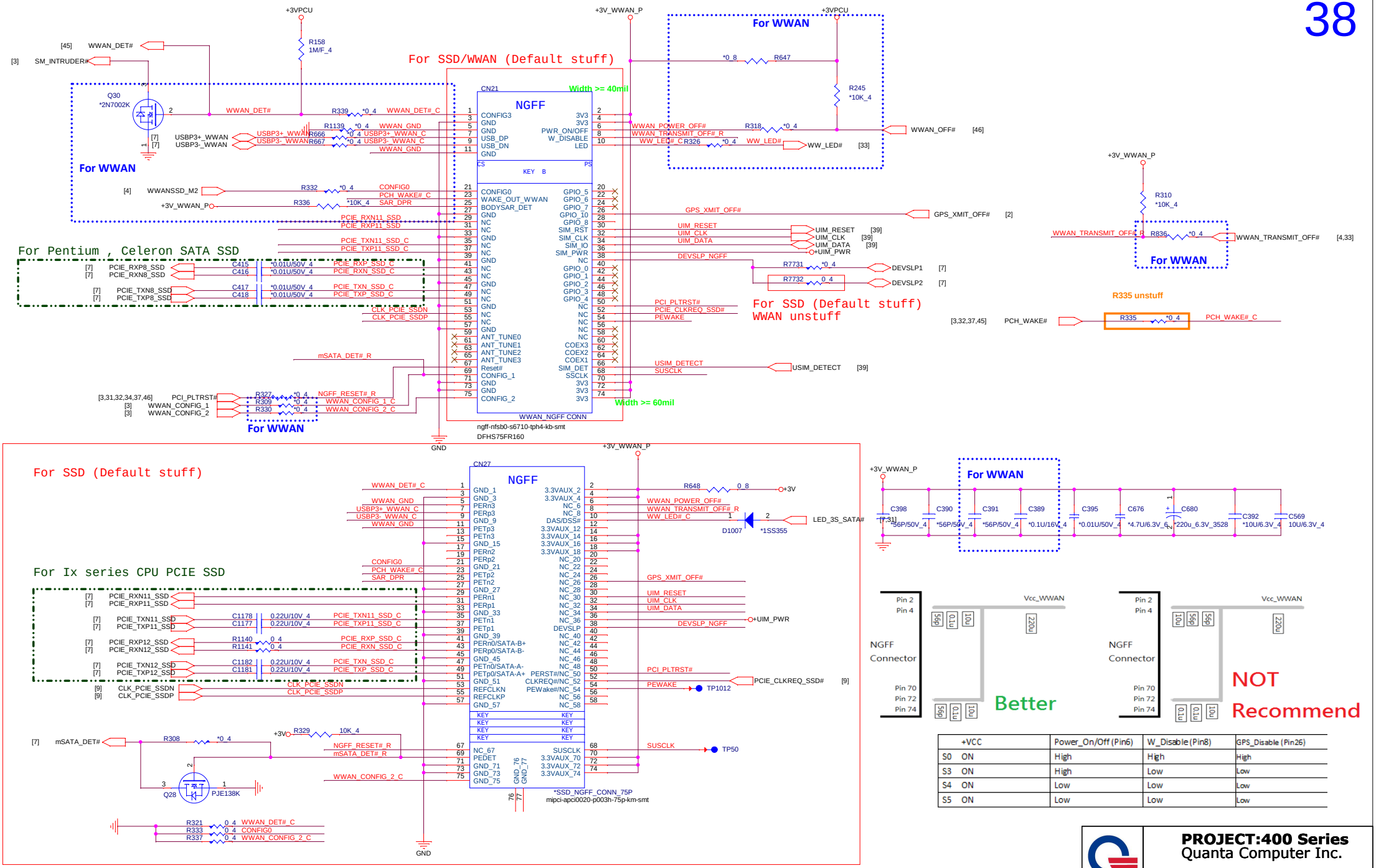
[8,27,29,30,40,42,43,54,58,63] +5V

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	37 -- NGFF WLAN/BT	1A

NB5

Date: Thursday, May 12, 2016 | Sheet 37of 65

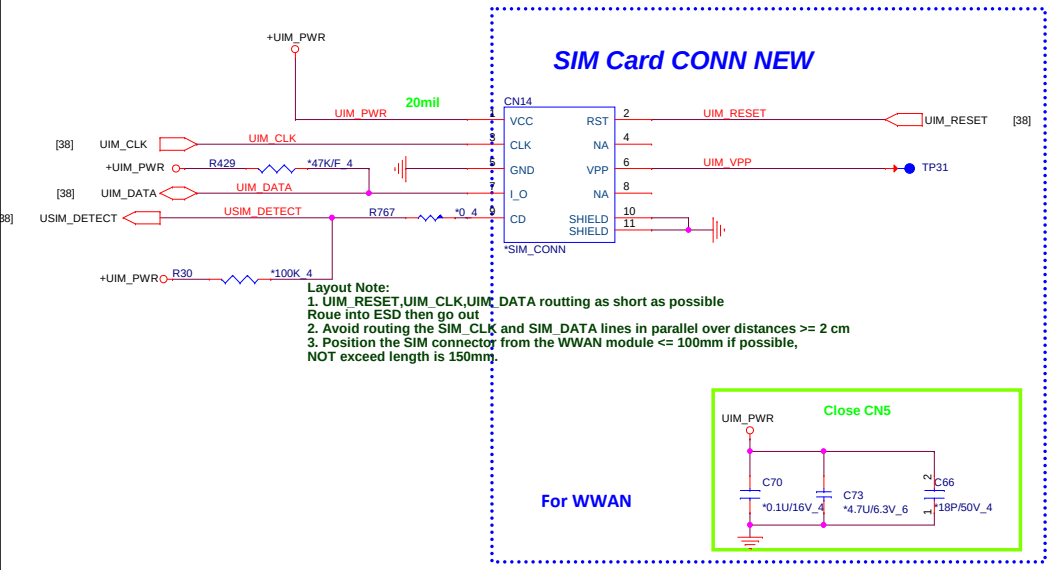


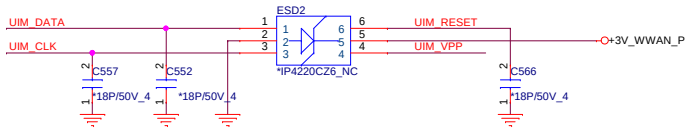
+VCC	Power_On/Off (Pin6)	W_Disable (Pin8)	GPS_Disable (Pin26)
S0 ON	High	High	High
S3 ON	High	Low	Low
S4 ON	Low	Low	Low
S5 ON	Low	Low	Low

PROJECT:400 Series
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	38 -- WWAN NGFF/ SSD	1A
Date: Thursday, May 12, 2016	Sheet 38 of 65	





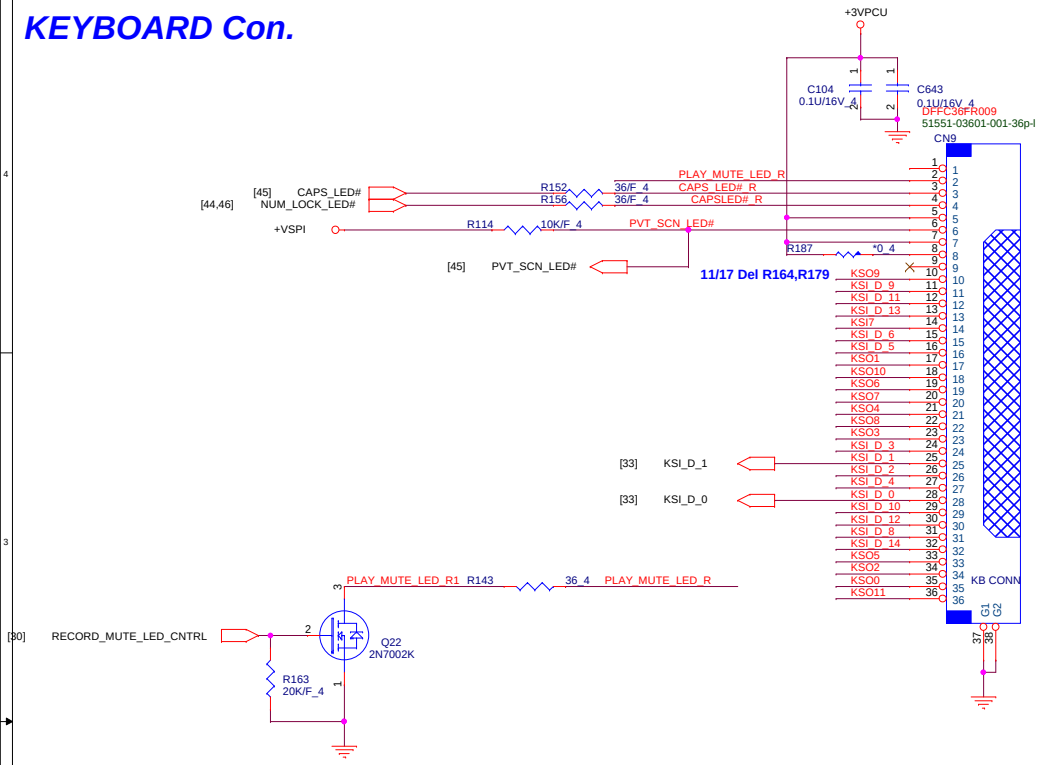
Trace Length and Routing

- Special attention should be paid to SIM traces (UIM_CLK, UIM_DATA and UIM_RST) to minimize the trace lengths between the SIM slot and the WAN NGFF slot. **Minimizing the signal lengths and traces will reduce possibility of SIM signal integrity issues.** Recommended maximum length is 100mm. Not to exceed length is 150mm.
- Minimum distance between UIM_CLK and UIM_DATA should be 20 mils. Static signals such as UIM_RST can be routed between UIM_CLK and UIM_DATA to conserve space if needed.
- It is recommended that SIM traces be isolated from other high-speed switching signals, as noise can couple into the SIM signals. Keep a minimum distance of 20 mils between UIM_CLK, UIM_DATA and any other high-speed switching signals.
- Placing the SIM card on a daughter card is also not recommended as the interconnect may impact SIM signal integrity.

SIM Power

- The UIM_PWR trace width must be at least 20 mils. Sub-planar routing is recommended.
- Implement additional power filtering to SIM card power to ensure clean power is supplied to minimize any possible noise ripple effects. At a minimum, place a 0.1uF and a 4.7uF capacitor on the UIM_PWR supply and locate near the SIM connector.

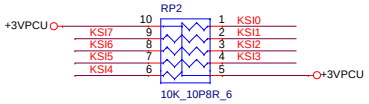
KEYBOARD Con.

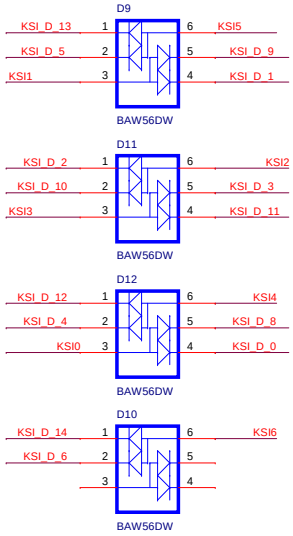


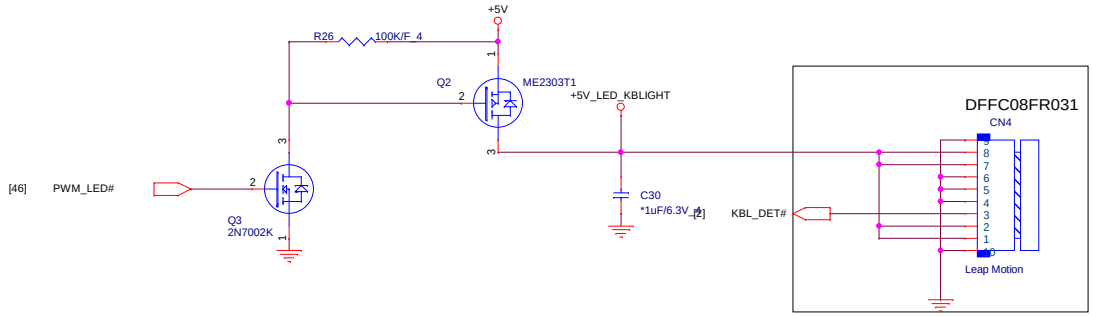
[44,46] KSO[0..13] KSO[0..13]

[46] KSI[0..7] KSI[0..7]

KEYBOARD PULL-UP







*100pF_2 C303 KSO9
*100pF_2 C305 KSI_D_9
*100pF_2 C308 KSI_D_11
*100pF_2 C309 KSI_D_13
*100pF_2 C311 KSI7
*100pF_2 C312 KSI_D_6
*100pF_2 C315 KSI_D_5
*100pF_2 C317 KSO1

*100pF_2 C321 KSO10
*100pF_2 C326 KSO6
*100pF_2 C336 KSO7
*100pF_2 C341 KSO4
*100pF_2 C352 KSO8
*100pF_2 C355 KSO3
*100pF_2 C364 KSI_D_3
*100pF_2 C370 KSI_D_1

*100pF_2 C374 KSI_D_2
*100pF_2 C376 KSI_D_4
*100pF_2 C381 KSI_D_0
*100pF_2 C383 KSI_D_10
*100pF_2 C385 KSI_D_12
*100pF_2 C388 KSI_D_8
*100pF_2 C393 KSI_D_14
*100pF_2 C397 KSO5

*100pF_2 C400 KSO2
*100pF_2 C405 KSO0
*100pF_2 C408 KSO11

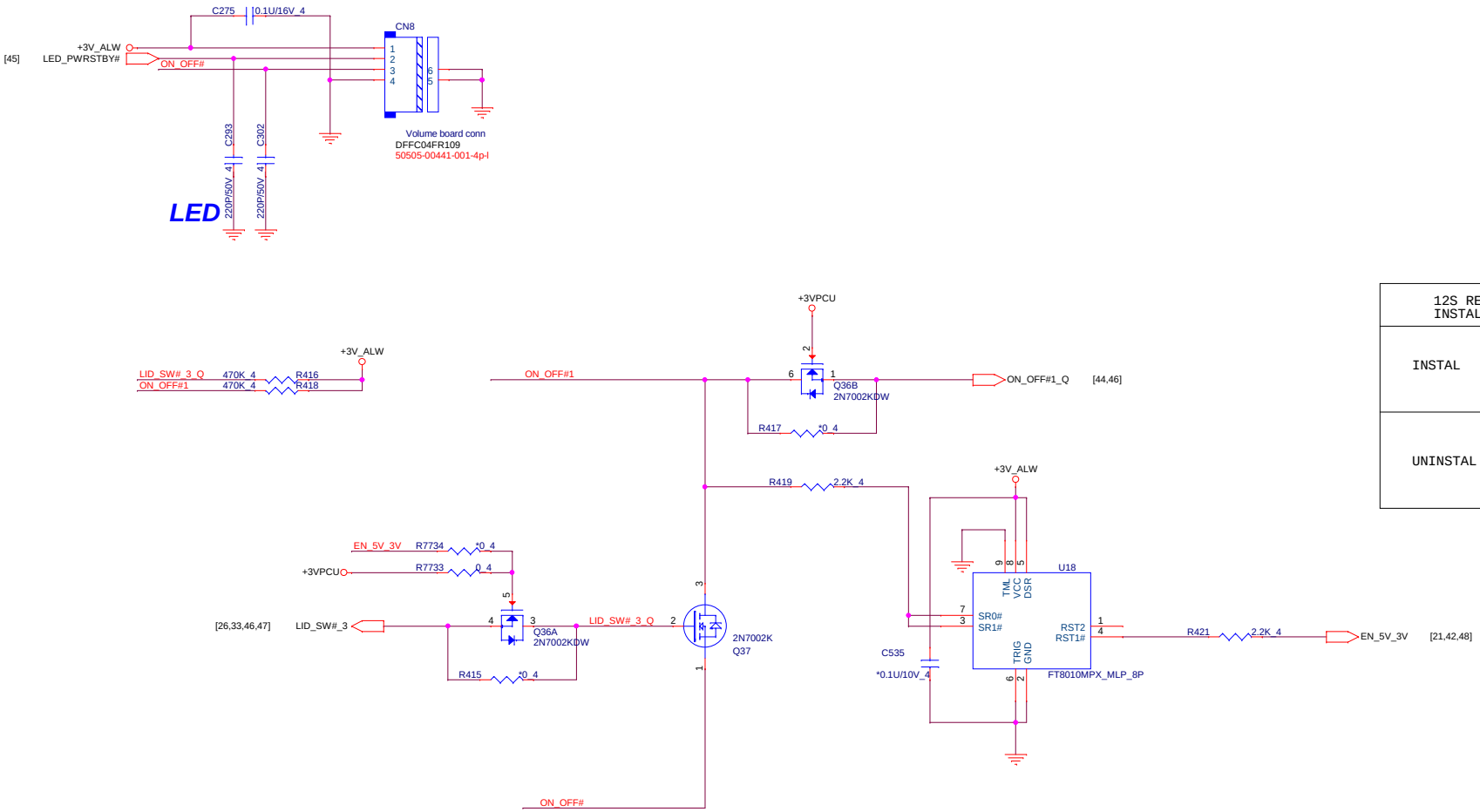
[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63] +3V
[8,27,29,30,42,43,54,58,63] +5V

NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	40 -- KB/ KB light CONN	1A
Date: Thursday, May 12, 2016	Sheet 40 of 65	

Power Botton Connector



12S RESET MODE INSTAL FOR DB0	
INSTAL	R10702 R10703 R10704 R581 R10701 R595 U9068
UNINSTAL	R10754 R10755 Q7080 Q7081

[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63] +3V
[8,27,29,30,40,42,43,54,58,63] +5V
[9,48,51,52,58,62,63] +3V_ALW

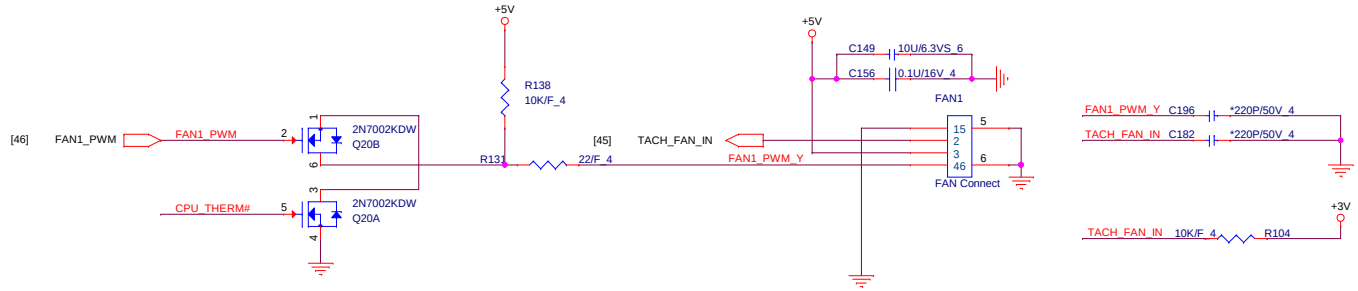
NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	41 -- Power Button/ HW Reset	1A

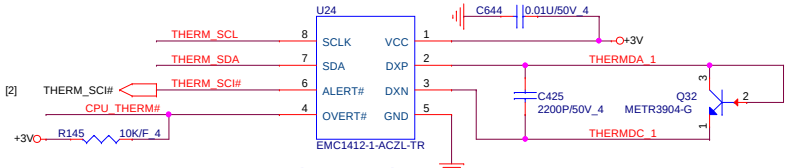
Date: Thursday, May 12, 2016 Sheet 41 of 65

FAN



Thermal sensor

CPU Thermal Sensor

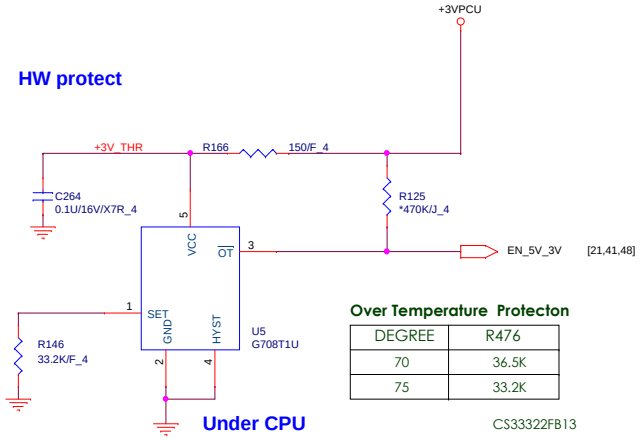


Under Heat Pipe

2nd:AL000431014 TMP431ADGKR

Main: AL000781012 G781P8(98h)

HW protect



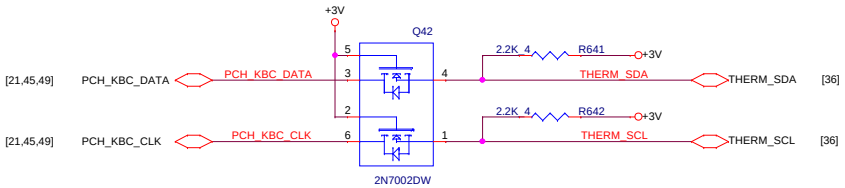
Over Temperature Protecton

DEGREE	R476
70	36.5K
75	33.2K

Under CPU

CS33322FB13

RSET (K OHM) = 0.0012T^2 - 0.9308T + 96.147



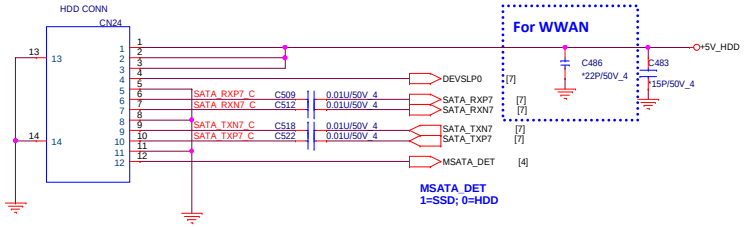
[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,44,45,47,51,56,58,59,63] [9,41,48,51,52,58,62,63] +3V +3V_ALW

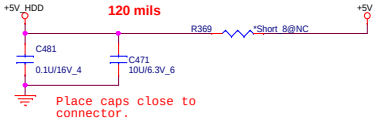
NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	42-- FAN and Thermal IC	1A
Date: Thursday, May 19, 2016	Sheet 42 of 65	

SATA-HDD





[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59,63]
[8,27,29,30,40,42,54,58,63]
+3V
+5V

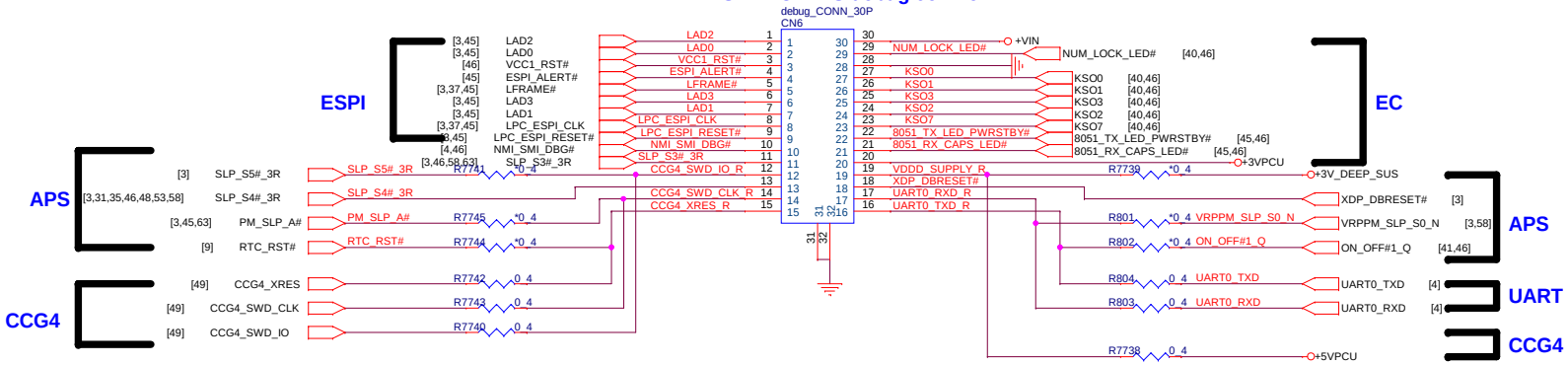
NB5

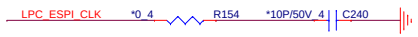
PROJECT:400 Series
Quanta Computer Inc.

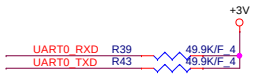
Size	Document Number	Rev
C	43 -- HDD/ EMI cap	1A

Date: Thursday, May 12, 2016 | Sheet 43of 65

ESPI+EC+APS debug conn on MB







LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
R771	INSTAL	UNINSTAL
R769	UNINSTAL	INSTAL
R770	INSTAL	UNINSTAL

LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
R658 **Ra**	INSTAL	UNINSTAL
R646 **Rb**	INSTAL	UNINSTAL
R659 **Rc**	INSTAL	UNINSTAL
R656 **Rd**	INSTAL	UNINSTAL
R649 **Re**	INSTAL	UNINSTAL
R657 **Rf**	INSTAL	UNINSTAL
R249 **Rg**	INSTAL	UNINSTAL
R147 **Rh**	INSTAL	UNINSTAL
R120 **Ri**	INSTAL	UNINSTAL
R276 **Rj**	INSTAL	UNINSTAL
R678 **Rk**	UNINSTAL	INSTAL

NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	44 -- EC & eSPI/UART debug conn	1A
Date: Thursday, May 12, 2016	Sheet 44 of 65	

for Battery charge/charge

for Thermal IC/ G-Sensor/GPU

EC

CPU I/O Rail Power Supply

NOTE:
Connect GND and AGND planes via an 0R resistor or a one-point layout connection.

NOTE:
Place a 1 uF capacitor as close to the CAP pin as possible.

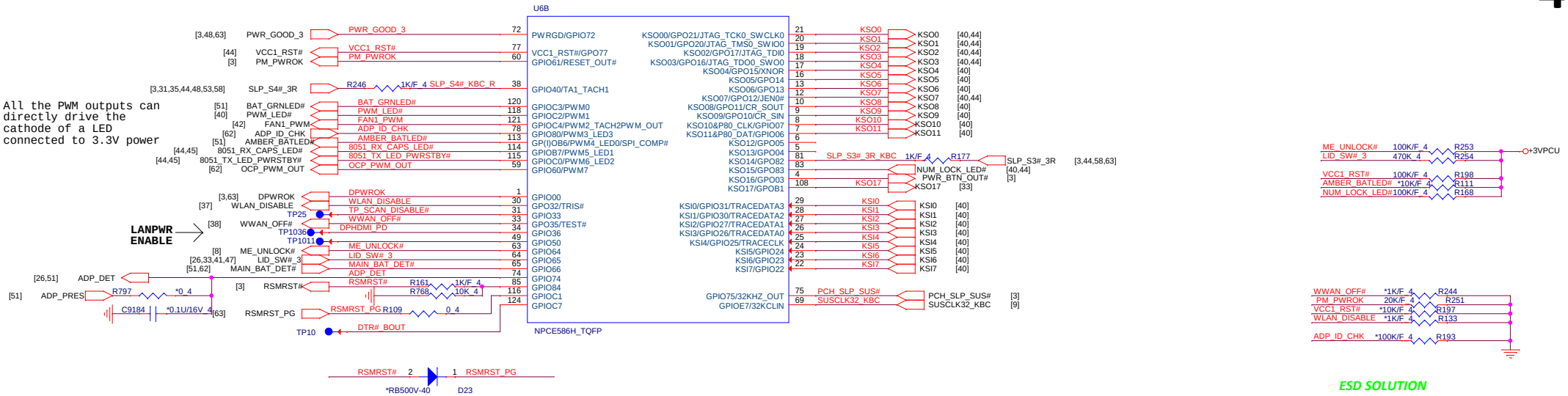
PLT_DET	PLT_DET
PD 100K	PU 10K
UMA	DIS

PROJECT:400 Series
Quanta Computer Inc.

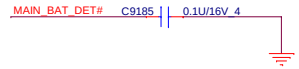
Size	Document Number	Rev
Custom	45 -- EC Nuvoton NPCE586H_1	1A
Date: Thursday, May 12, 2016	Sheet 45of 65	

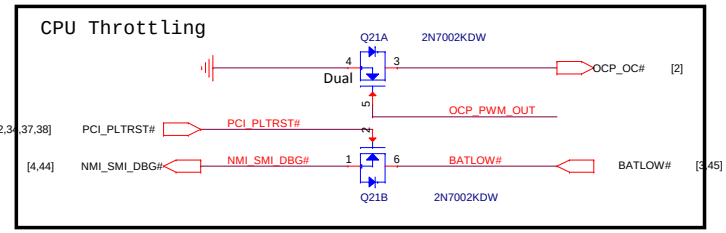
NB5

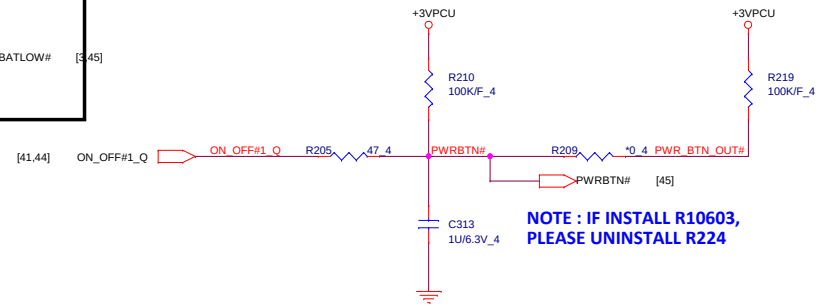
All the PWM outputs can directly drive the cathode of a LED connected to 3.3V power



ESD SOLUTION







NOTE : IF INSTALL R10603, PLEASE UNINSTALL R224

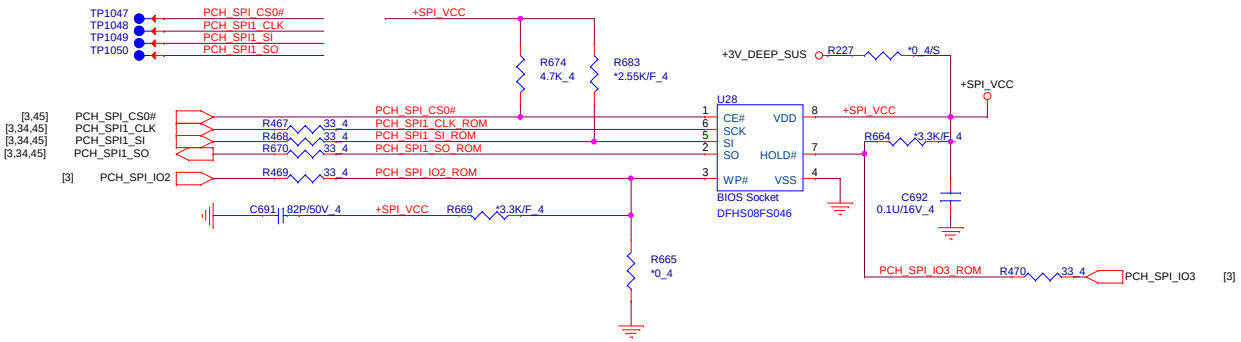
NB5	PROJECT:400 Series Quanta Computer Inc.	
Size: Custom	Document Number: 46 -- EC Nuvoton NPCE586H_2	Rev: 1A
Date: Thursday, May 12, 2016	Sheet: 46of 65	

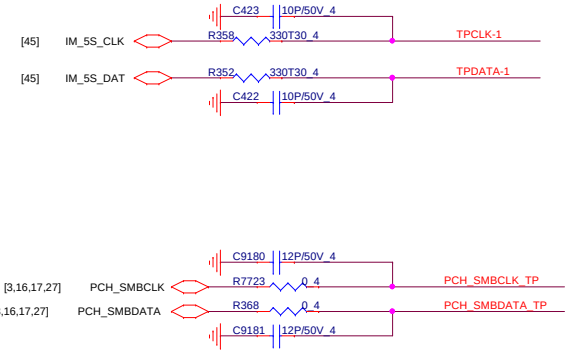
SPI ROM

Vender	Size	P/N
GD	128MB	AKE2DF0KQ00
Winbond	128MB	AKE3DZNKN00
Socket		DFHS08FS046

PCH SPI ROM(CLG)

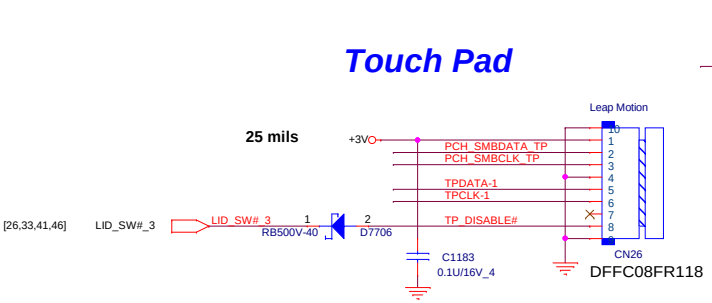
PCH 6*5mm WSON 16M
SPI ROM Socket

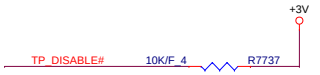




CLICK PAD
Address: 0x20(7 bit)

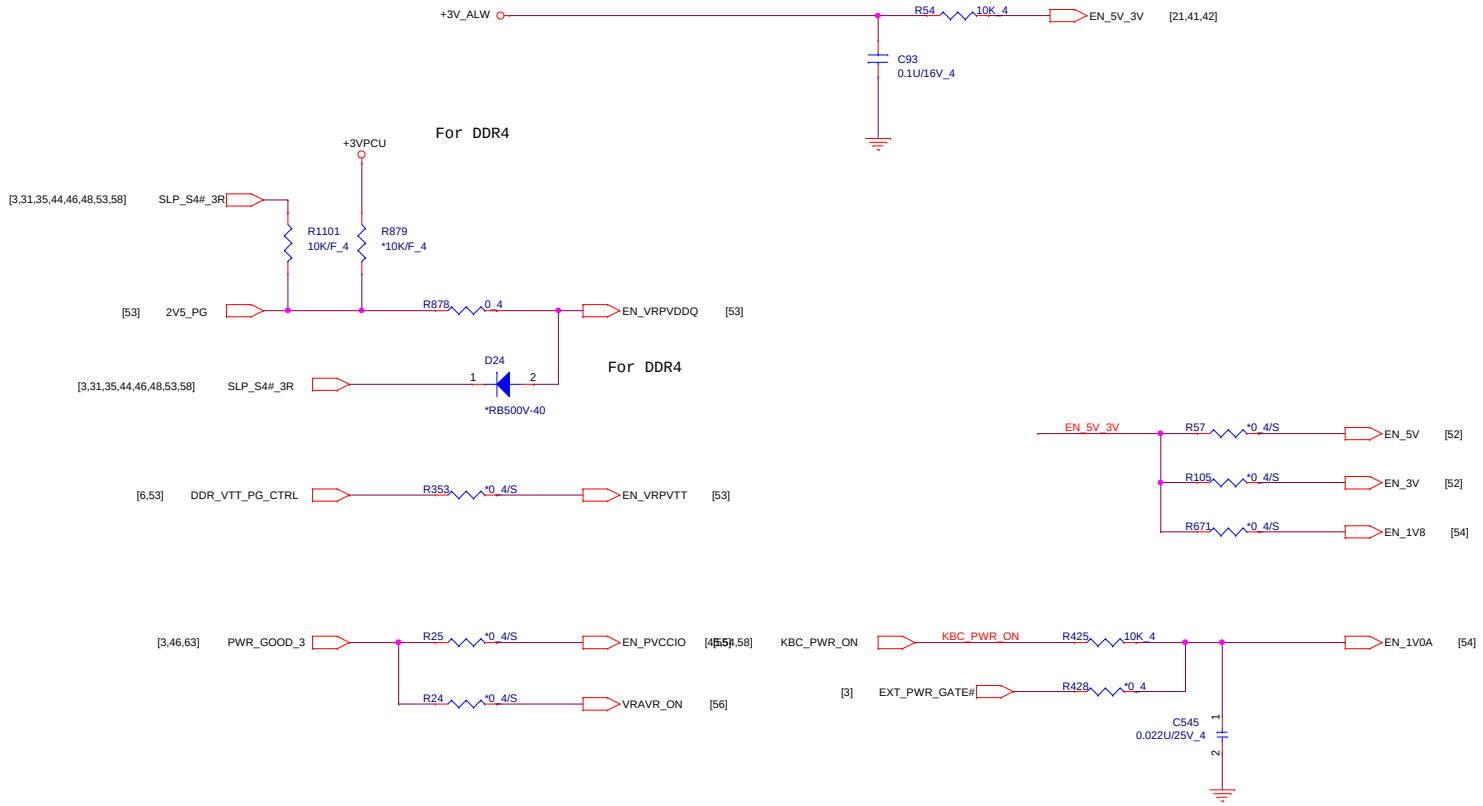
Touch Pad





NB5	PROJECT:400 Series Quanta Computer Inc.		
	Size: Custom	Document Number: 47 -- Flash(KBC+PCH)	Rev: 1A
	Date: Thursday, May 12, 2016	Sheet: 47of 65	

POWER TO EE NET NAME CONNECTION



NB5	PROJECT:400 Series Quanta Computer Inc.	
Size: Custom	Document Number: 48 -- POWER ENABLE	Rev: 1A
Date: Thursday, May 12, 2016	Sheet 48of 65	

SI, 2/22, Change 5V

+5VPCU
VDDD_SUPPLY
R1153 0_8
C1186 0.1U/16V_4
C1185 0.1U/16V_4
C700 1uF/6.3V_4

U1013
+5VPCU
GND
IN
OUT
*G5250Q1T73U
R837 0_3_6
C1184 0.1U/16V_4
C697 1uF/6.3V_4
R57
R839 0_4
VCONN_VMON_P1
R58
R1154 *2M/F_4

VCONN_5V_P1 trace width must be 25mil above.

Note:
The above resistor divider network is needed only when VDDD_SUPPLY is 3.3V.
Don't place R58 and R60 resistors when VDDD_SUPPLY is 5V.
Use 0ohm resistors for R57 and R59 when VDDD_SUPPLY is 5V.

T/I connect To EC 105 Pin, netname CYPRE_INT

+3VPCU
R1146 10K/F_4
[45] CYPRE_INT

VDDD_SUPPLY
R7754 *4.7K_4
CCG4_SWD_CLK
R7755 *4.7K_4

U1008
CCG4 40-QFN

VDDD_SUPPLY
C1189 1uF/6.3V_4

31	VDDD	VBUS_P_CTRL_P1	11
32	VDDIO	VBUS_C_CTRL_P1	12
33	VCCD	VBUS_DISCHARGE_P1/GPIO	20
8	VCONN_V5V_P1	HPD_P1	18
23	VCONN_V5V_P2	CC2_P1	7
3	I2C_SDA_SCB2_AR/GPIO	CC1_P1	9
4	I2C_SCL_SCB2_AR/GPIO		
5	I2C_INT_AR_P1/GPIO		
6	I2C_INT_AR_P2		
13	VBUS_MON_P1	MUX_CTRL3_P1/SDA_3/GPIO	26
		MUX_CTRL2_P1/SDA_4	28
		MUX_CTRL1_P1/SCL_4	29
37	VBUS_MON_P2		
1	SWD_IO/AR_RST#/GPIO	HPD_P2	30
2	SWD_CLK/I2C_INT_AR_P2/GPIO	CC1_P2	22
15	I2C_INT_EC		
16	I2C_SDA_SCB1_EC	CC2_P2	24
17	I2C_SCL_SCB1_EC		
19	VSEL1_P1/VCONN_VMON_P1		
14	VSEL2_P1/OVP_TRIP_P1	MUX_CTRL3_P2/GPIO	34
		MUX_CTRL2_P2/GPIO	35
		MUX_CTRL1_P2/GPIO	36
25	VSEL1_P2/SCL_3/VCONN_VMON_P2		
27	VSEL2_P2/GPIO		
21	OVP_TRIP_P2	VBUS_C_CTRL_P2	38
		VBUS_P_CTRL_P2	39
		VBUS_DISCHARGE_P2/GPIO	40
10	XRES	EPAD	41

CYPD4125-40LQXIT
PART_NUMBER = CYPD4225-40LQXIT
Manufacturer = Cypress

[44] CCG4_SWD_IO
[44] CCG4_SWD_CLK
[4] SWD_IO_PCH R1148 *0_4 CCG4_SWD_IO
[4] SWD_CLK_PCH R805 *0_4 CCG4_SWD_CLK
USB_C_INT#
[21,42,45] PCH_KBC_DATA PCH_KBC_DATA
[21,42,45] PCH_KBC_CLK PCH_KBC_CLK
VCONN_VMON_P1
[50] CCG4_OVP
MOD_ID1
MOD_ID2

VDDD_SUPPLY
R806 4.7K_4
[44] CCG4_XRES CCG4_XRES
C1188 0.1U/16V_4
[4] SWD_XRES_PCH
R807 *10K/F_4
*PJE138K Q1010

C704 0.1U/16V_4
R1147 100K/F_4
R1150 10K/F_4
+5V_USBP0

+5V_USBP0
R1149 100/F_4
PJE138K Q63
CCG1_VBUS_DISCHARGE
R7726 100K_4
TYPEC_EN [50]

+3VPCU
CCG4_HOTPLUG_DET_P1 R798 *10K/F_4
TYPEC_CC2 [50]
C702 390P/50V_4
TYPEC_CC1 [50]
C703 390P/50V_4

+3VPCU
CCG4_I2C_SDA_MUX R1152 *10K/F_4
CCG4_I2C_SCL_MUX R1151 *10K/F_4

MOD_ID	Pull high	Pull down
L0	None	1K
L1	7.1K	1K
L5	3.09K	5.1K
L6	2.2K	5.9K

VDDD_SUPPLY
R7729 2.2K_4
R7727 *7.15K/F_4
MOD_ID1
MOD_ID2
R7728 5.9K/F_4
R7730 1K/F_4

MOD_ID1 and MOD_ID2 pins connect to ADC in CCG4.

	Platform ID		Dual Port		Single Port		
	MOD_ID1	MOD_ID2	Description (Dual port)	Dual Port CFGID	Description (Single)	Single Port CFGID	
Non TBT Slice Modules	L7	L0	Discrete GFX module for Slice	CFG0			L0 = 0V
	L7	L1	HDD module for Slice	CFG1			L1 = VDDD/3
	L7	L2	ODD module for Slice	CFG1			L2 = 2* VDDD/8
	L7	L3	Legacy I/O module for Slice	CFG1			L3 = 3* VDDD/8
	L7	L4			Communication	CFG0	L4 = 4* VDDD/8
	L7	L5	Future use				L5 = 5* VDDD/8
	L7	L6	Future use				L6 = 6* VDDD/8
	L7	L7	Future use				L7 = 7* VDDD/8
TBT platforms	L0	x	TBT Module for Slice	CFG2			
	L1	x			Slice Gen2	CFG1	
	L2	x			800 & 600, AIO Addon Card	CFG2	
Non TBT Desktop Platforms	L5	L0	Slice Gen1 & Gen2	CFG3	Slice Gen1	CFG3	
	L5	L1	800 & 600 Series	CFG4	800 & 600, 400 Series (DFP)	CFG4	
	L5	L2	Future		800 & 600 (DFP+DP)	CFG5	
Non TBT Notebook Platforms	L6	L0	DFP+DP on two ports	CFG5	DFP only	CFG4	
	L6	L1			DFP + DP on single port	CFG5	

test points sequence and pitch.
(2.54mm with PHY 1.02)

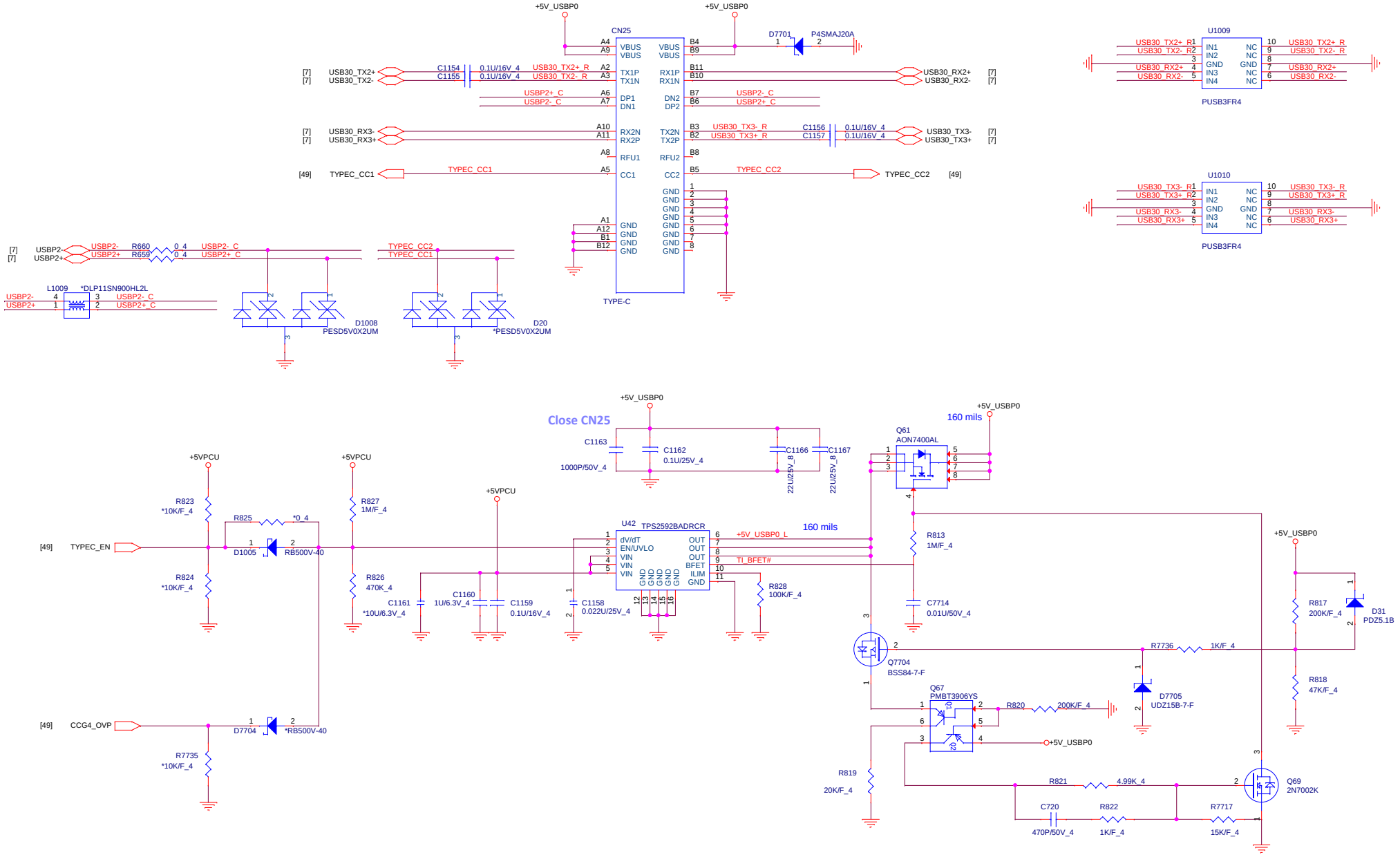
VDDD_SUPPLY
TP1041
TP1042
TP1043 CCG4_XRES
TP1044 CCG4_SWD_CLK
TP1045 CCG4_SWD_IO

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
	49 -- Cypress CCG1	1A

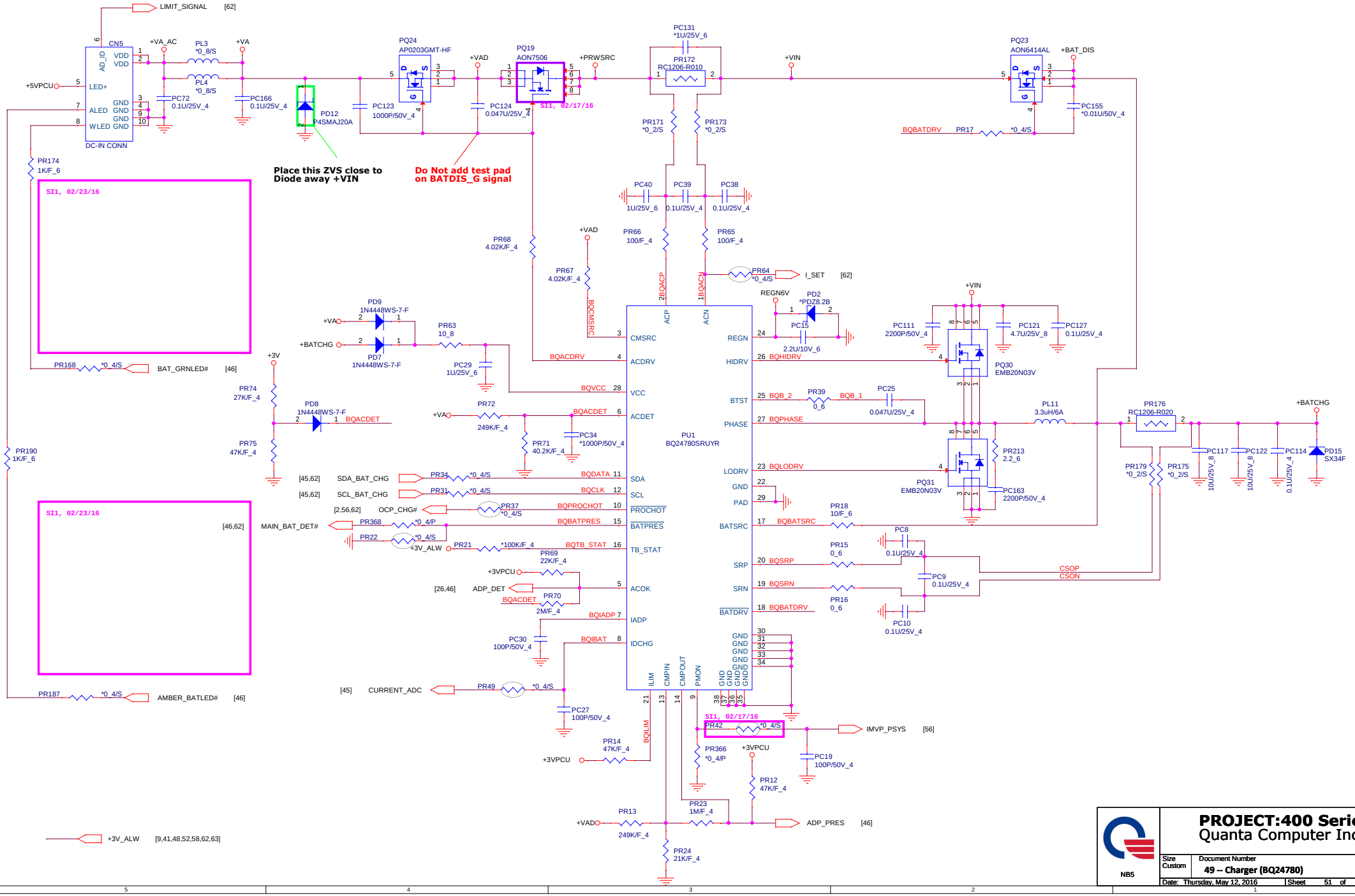
Date: Friday, May 20, 2016 Sheet 49 of 65

NB5



NB5	**PROJECT:400 Series** Quanta Computer Inc.	
Size	Document Number **50 -- TYPE-C**	Rev 1A
Date: Tuesday, May 17, 2016	Sheet 50 of 65	

90W DC_JACK



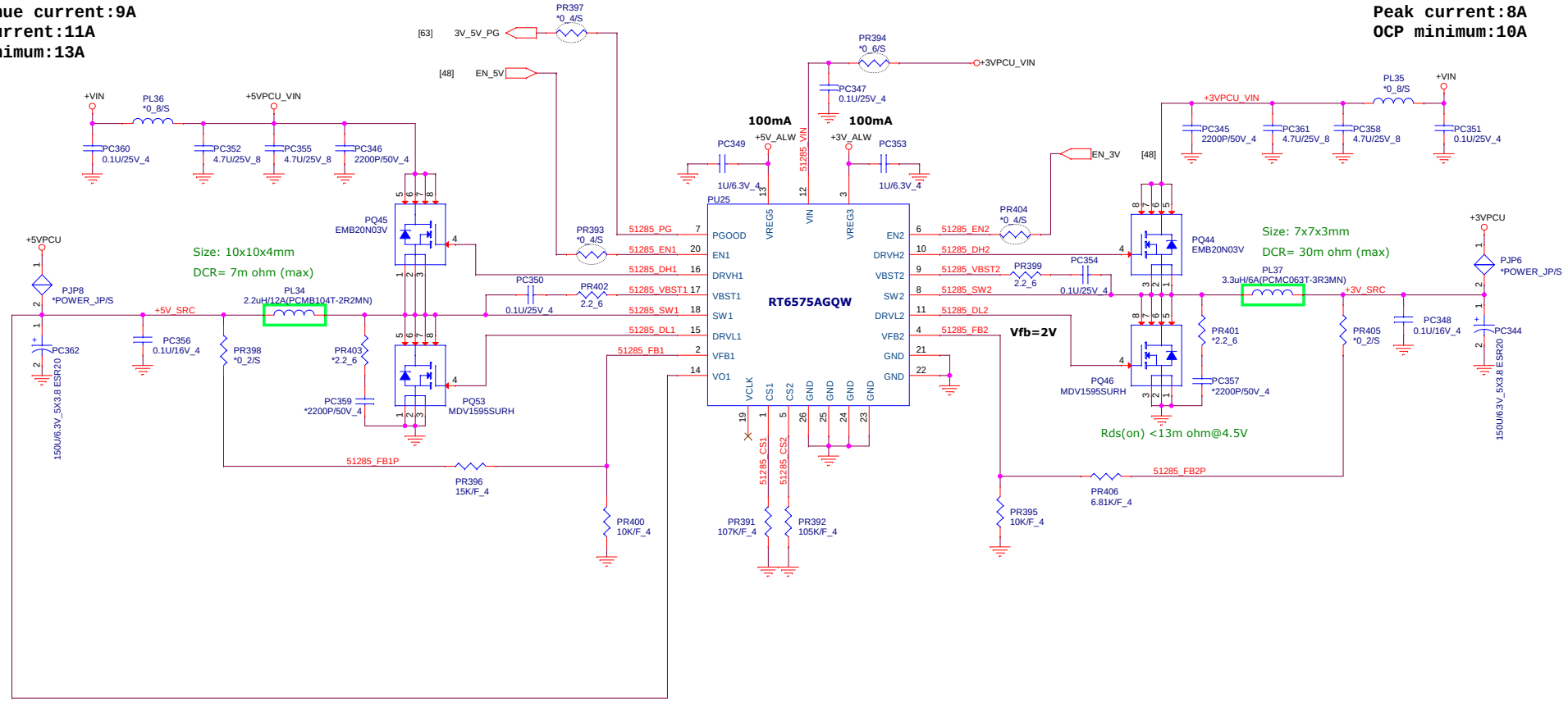
NB5	**PROJECT:400 Series** Quanta Computer Inc.	
Size Custom	Document Number 49 -- Charger (BQ24780)	Rev 1A
Date: Thursday, May 12, 2016	Sheet 51 of 65	

DC/DC +3VS5/+5VS5

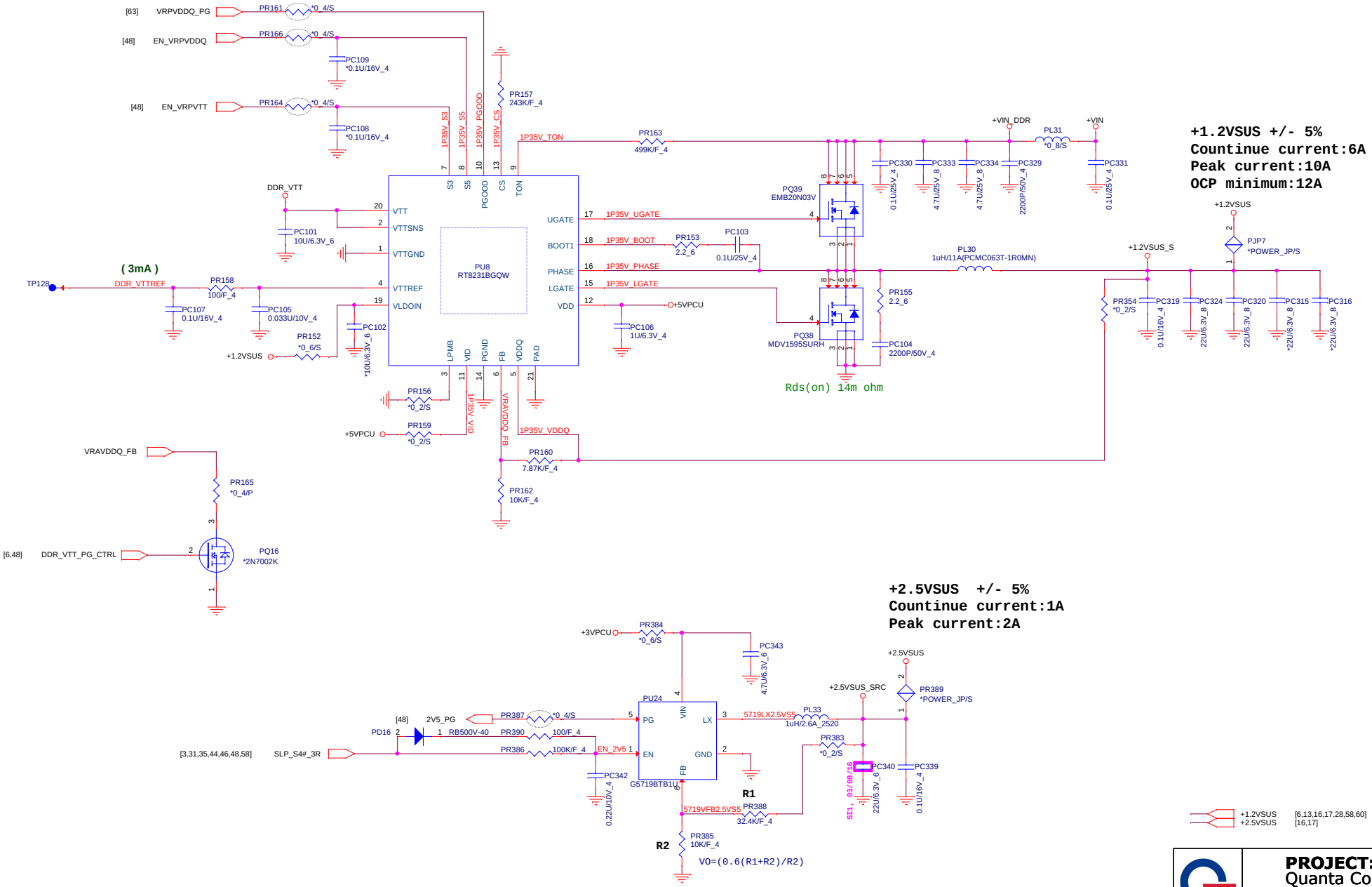
+3VPCU [3,10,33,37,38,40,41,42,44,45,46,48,49,51,53,55,58,60,62,63]
+5VPCU [28,31,35,44,49,50,51,53,54,56,57,58,59,60,61,63]

+5VPCU +/- 5%
Countinue current:9A
Peak current:11A
OCP minimum:13A

+3VPCU +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:10A



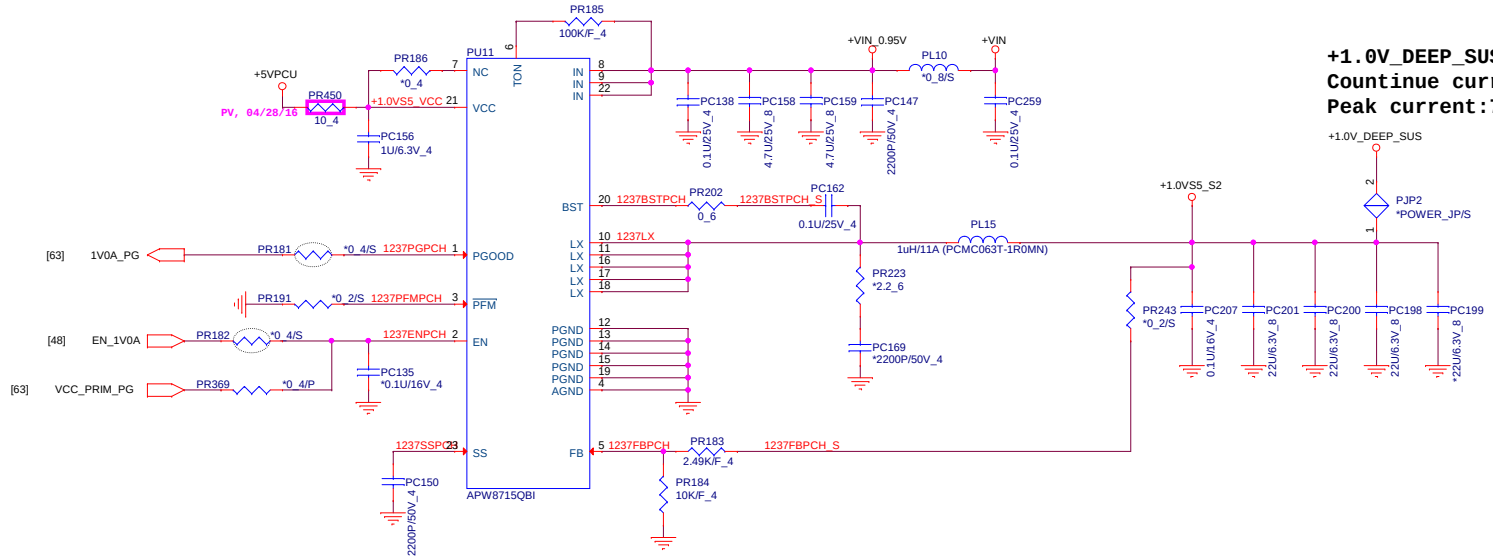
Quanta Computer Inc.	PROJECT:400 Series		
NB5	Size	Document Number: 50 -- 3/5VS5 (SY8208B/SY8208C)	Rev: 1A
	Date: Thursday, May 12, 2016	Sheet 52 of 65	



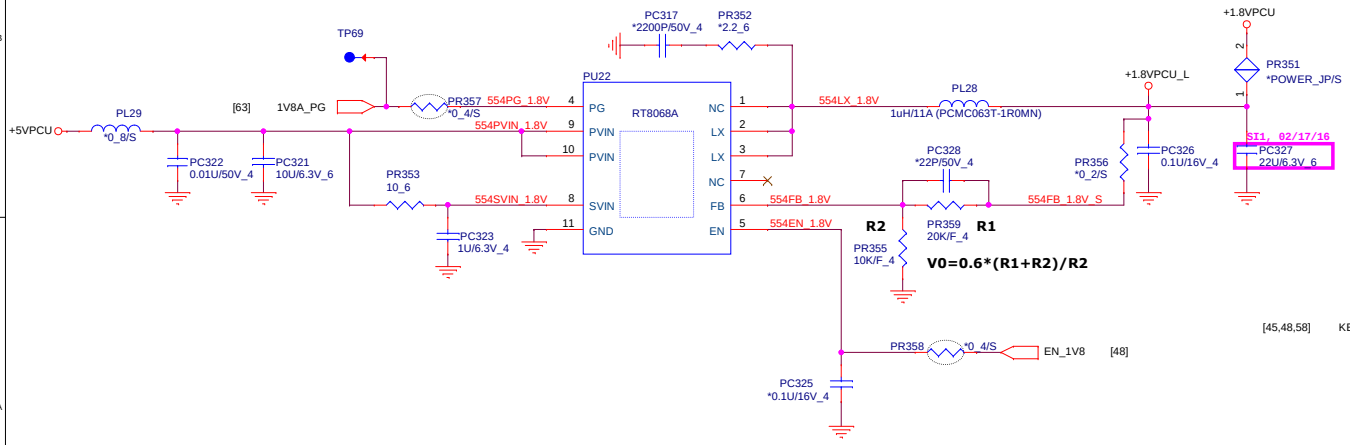
PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
	51 -- DDR4 (RT8231B)	1A
NB5	Date: Thursday, May 12, 2016	Sheet 53 of 65

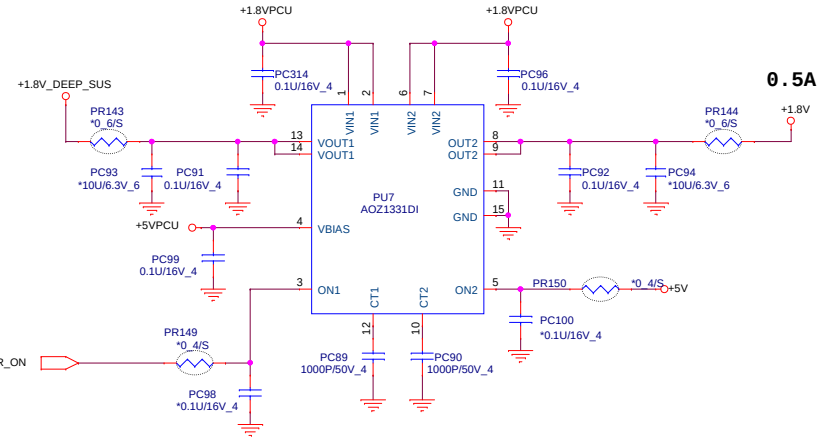
+1.0V_DEEP_SUS +/- 5%
Countinue current:6A
Peak current:7A



+1.8VPCU +/- 5%
Countinue current:2A
Peak current:4A



0.5A

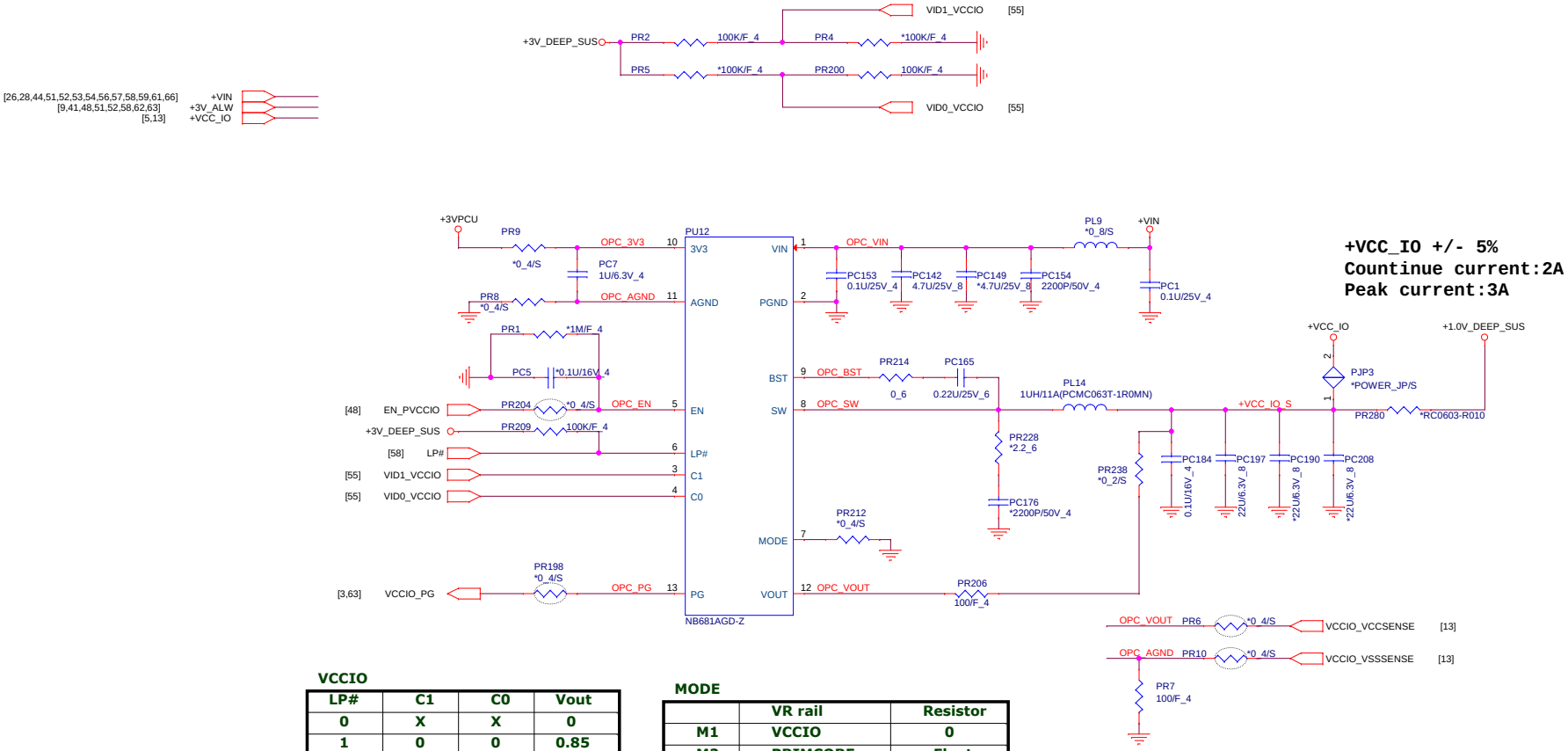


+VIN [26,28,44,51,52,53,55,56,57,58,59,61,66]
+3VPCU [3,10,33,37,38,40,41,42,44,45,46,48,49,51,52,53,55,58,60,62,63]
+5VPCU [28,31,35,44,49,50,51,52,53,56,57,58,59,60,61,63]

PROJECT:400 Series
Quanta Computer Inc.

NB5

Size	Document Number	Rev
	52 -- +1.0VS5/1.8VS5	1A
Date: Thursday, May 12, 2016	Sheet 54 of 65	



+VCC_IO +/- 5%
Countinue current:2A
Peak current:3A

VCCIO

LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.85
1	0	1	0.875
1	1	0	0.95
1	1	1	0.975

MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
	53 -- +VCC_IO (NB681)	1A
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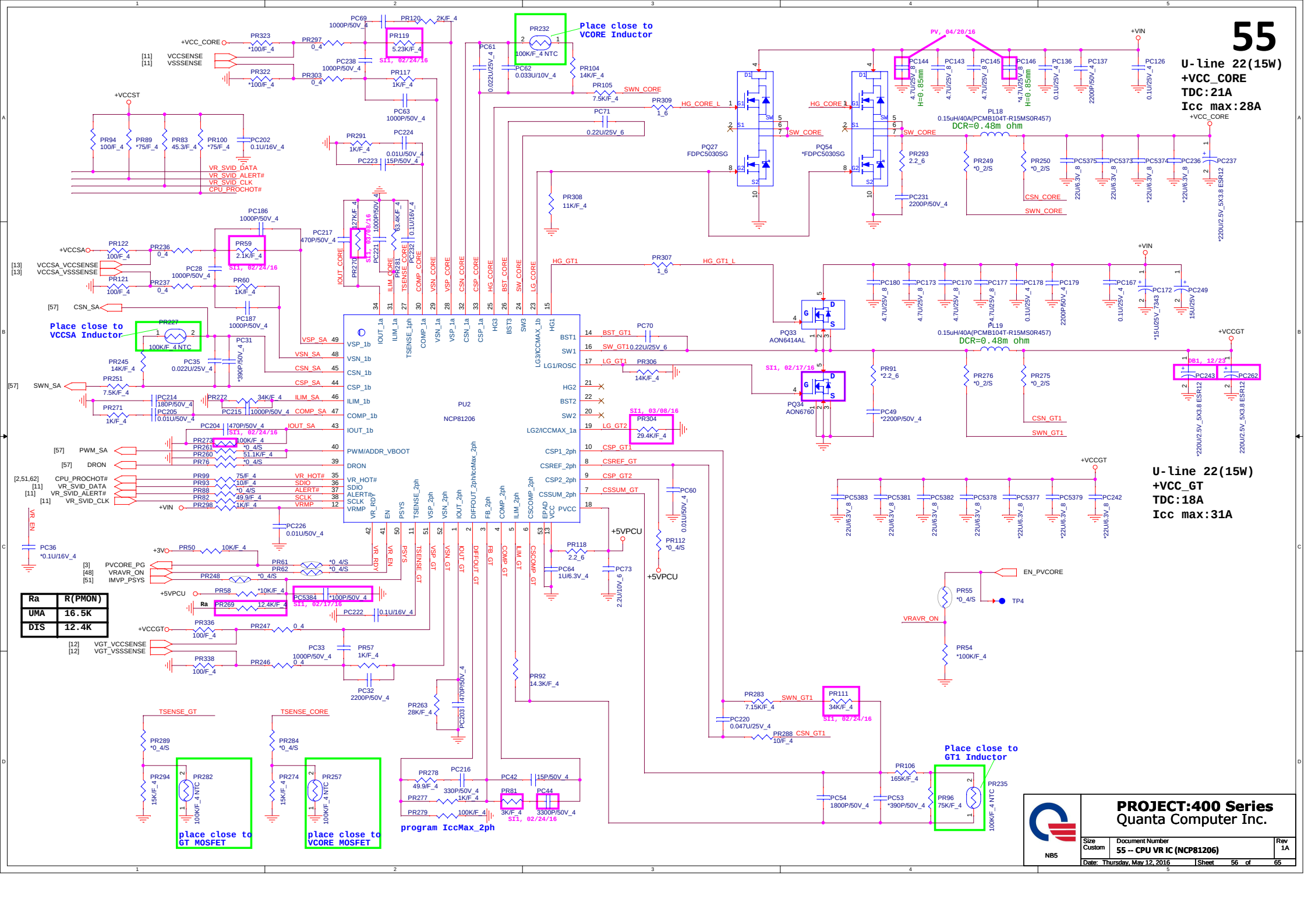
NB5



Ra	R(PMON)
UMA	16.5K
DIS	12.4K

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Size	Document Number	Rev
Custom	55 -- CPU VR IC (NCP81206)	1A
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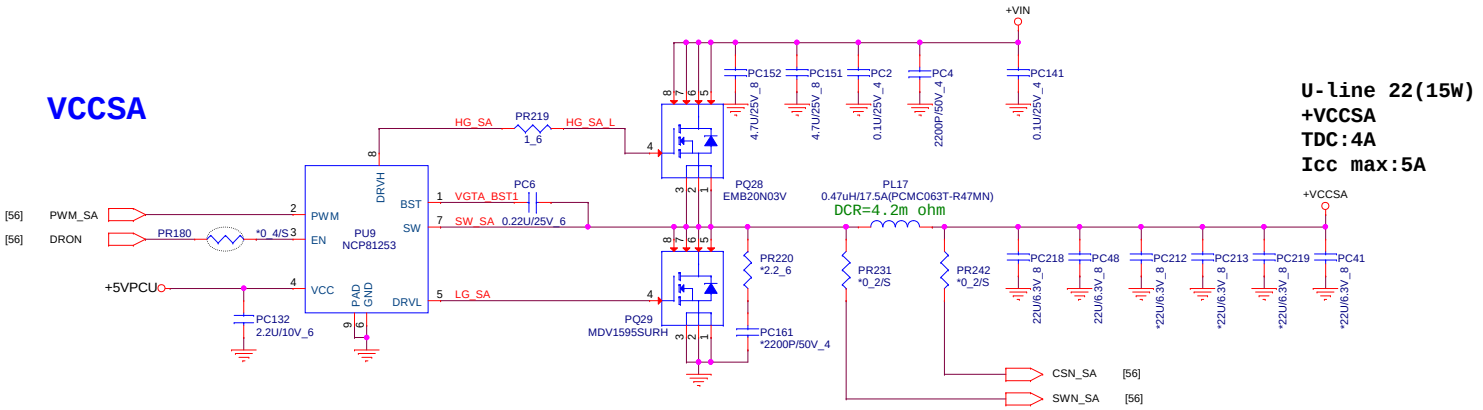
NB5

VCCSA



U-line 22(15W)
+VCCSA
TDC:4A
Icc max:5A

NB5	**PROJECT:400 Series** Quanta Computer Inc.	
Size: Custom	Document Number: **56 -- +VCCSA (NCP81253)**	Rev: 1A
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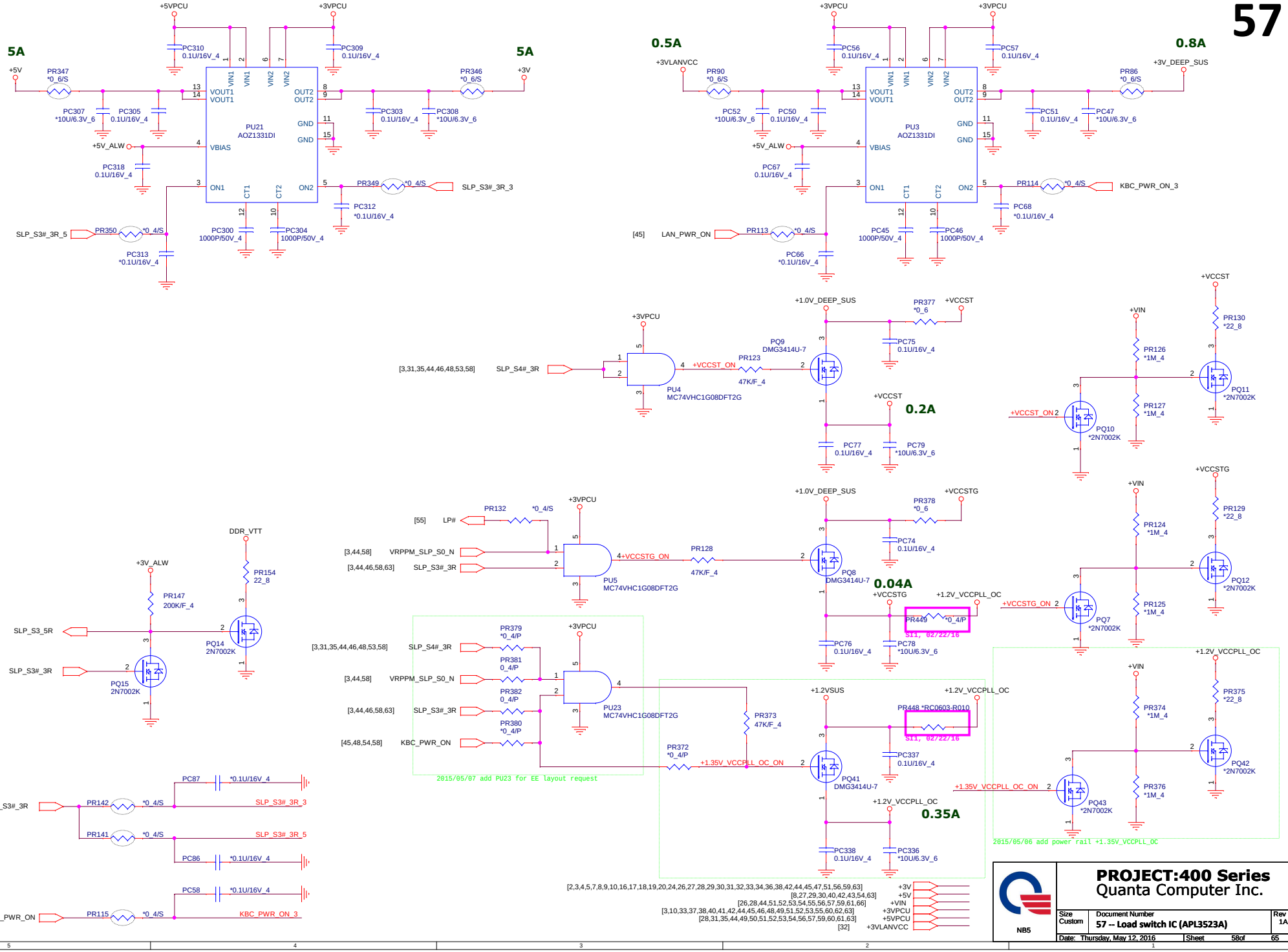
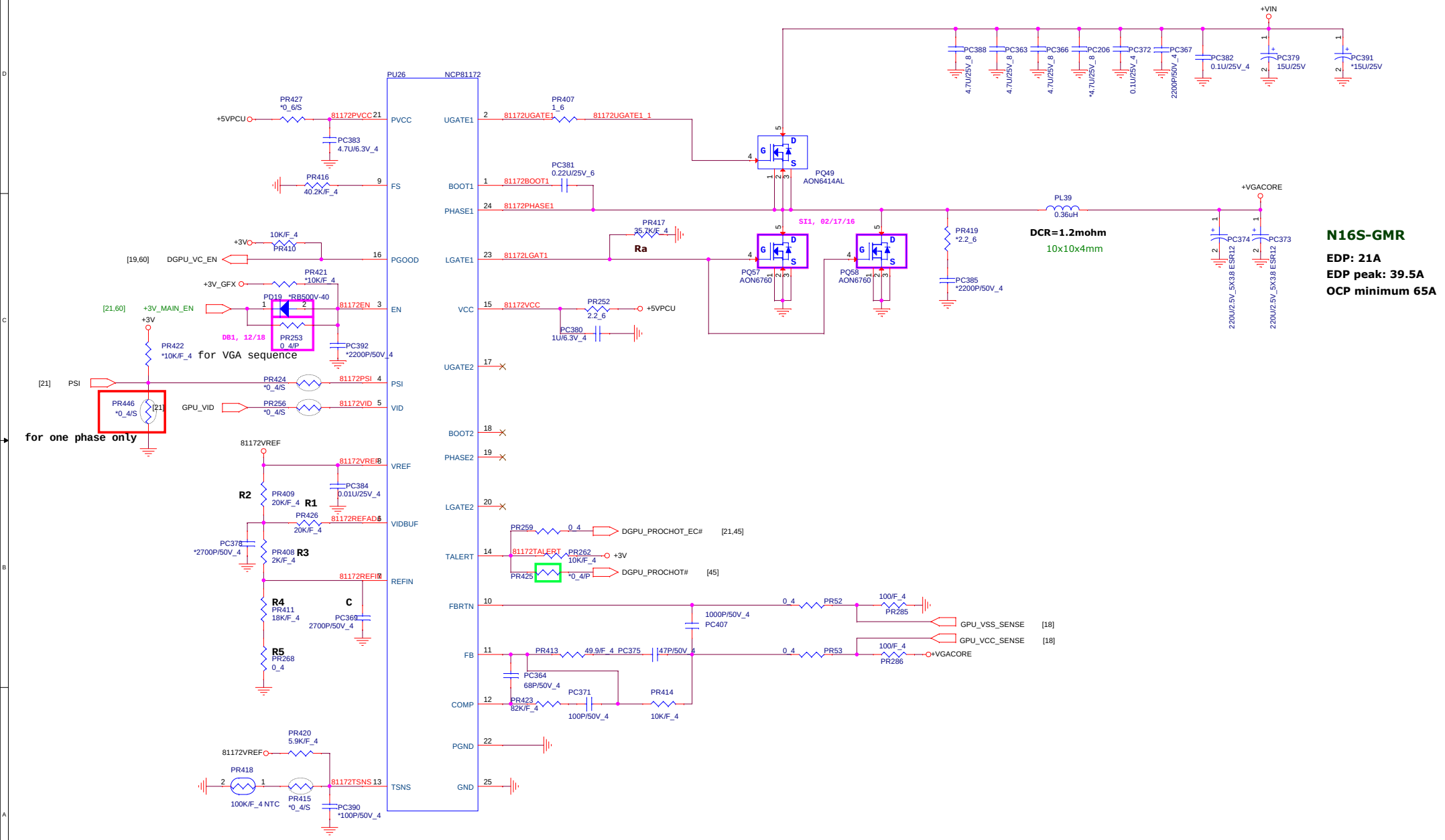


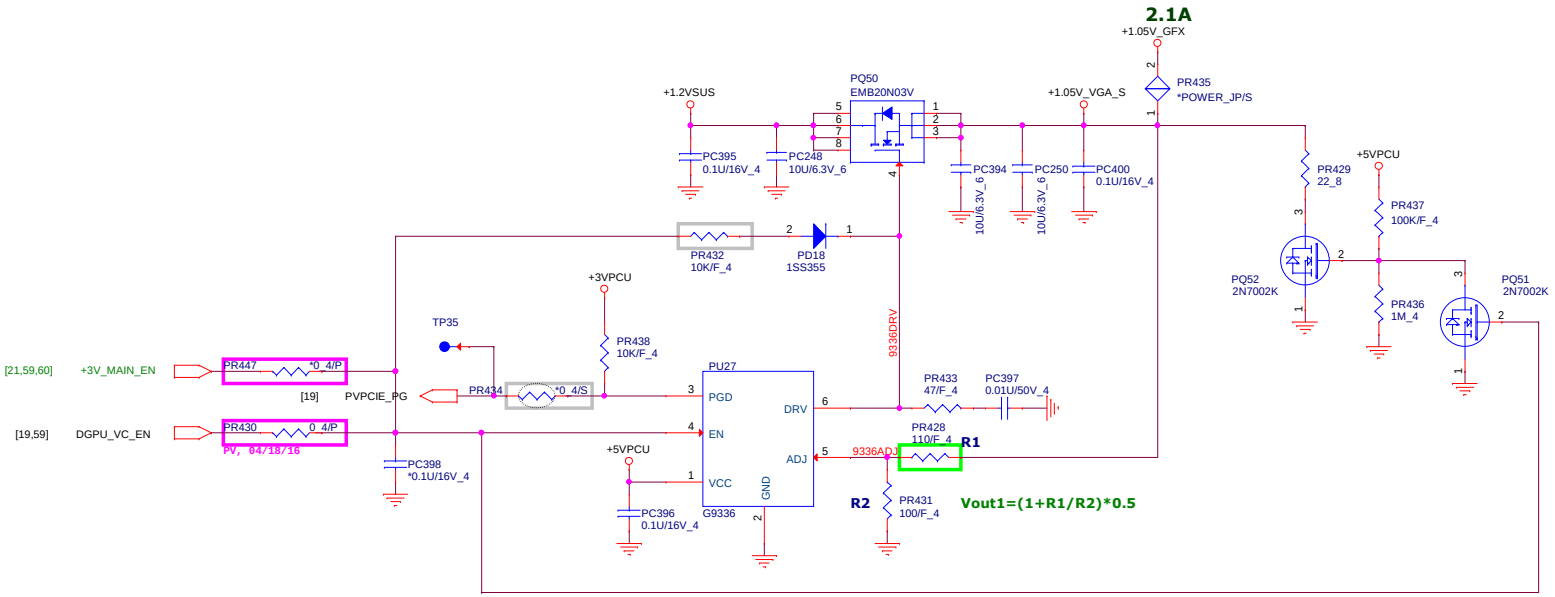
PROJECT:400 Series
Quanta Computer Inc.

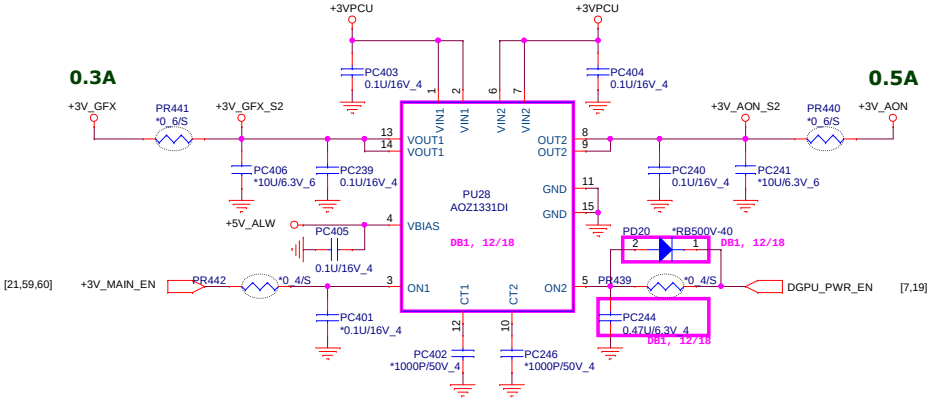
Size	Document Number	Rev
Custom	57 -- Load switch IC (APL3523A)	1A
Date: Thursday, May 12, 2016	Sheet 58of 65	

NB5



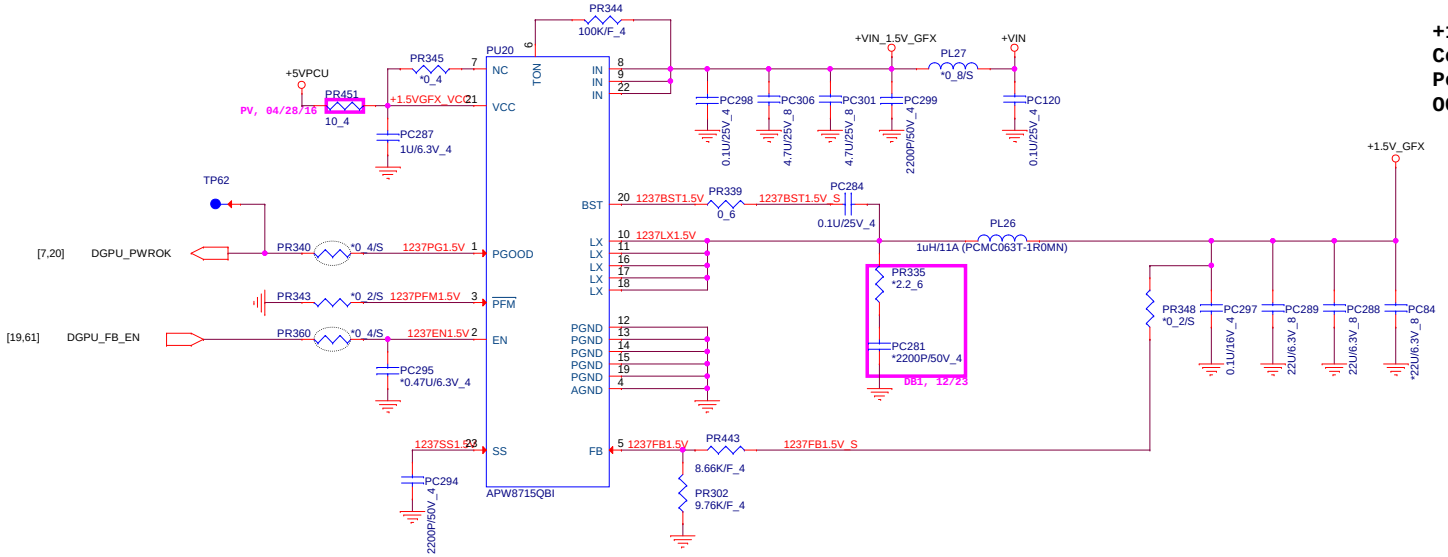
NB5	**PROJECT:400 Series** Quanta Computer Inc.		
	Size: Custom	Document Number: 58 -- VGA Core1 (ISL62771)	Rev: 1A
	Date: Thursday, May 12, 2016	Sheet: 59of	65

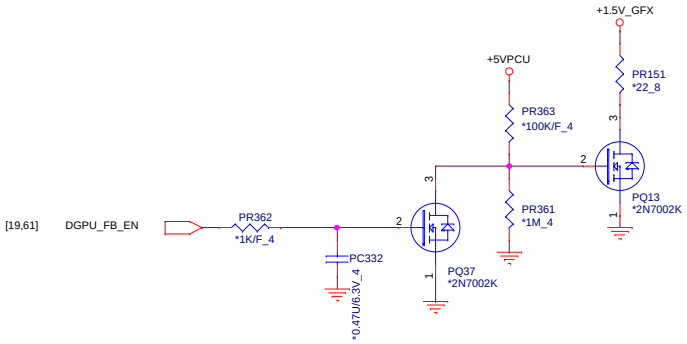




NB5	**PROJECT:400 Series** Quanta Computer Inc.	
Size: Custom	Document Number: 60 -- +1.0V_VGA/1.8V_VGA/3V_VGA	Rev: 1A
Date: Thursday, May 12, 2016	Sheet: 60of	65

+1.5V_GFX Volt +/- 5%
Countinue current:2.4A
Peak current:4.1A
OCP minimum:8A





NB5	**PROJECT:400 Series** Quanta Computer Inc.	
	Size: Custom — Document Number: **61 -- +1.35V_GFX (AOZ1267)**	Rev: 1A
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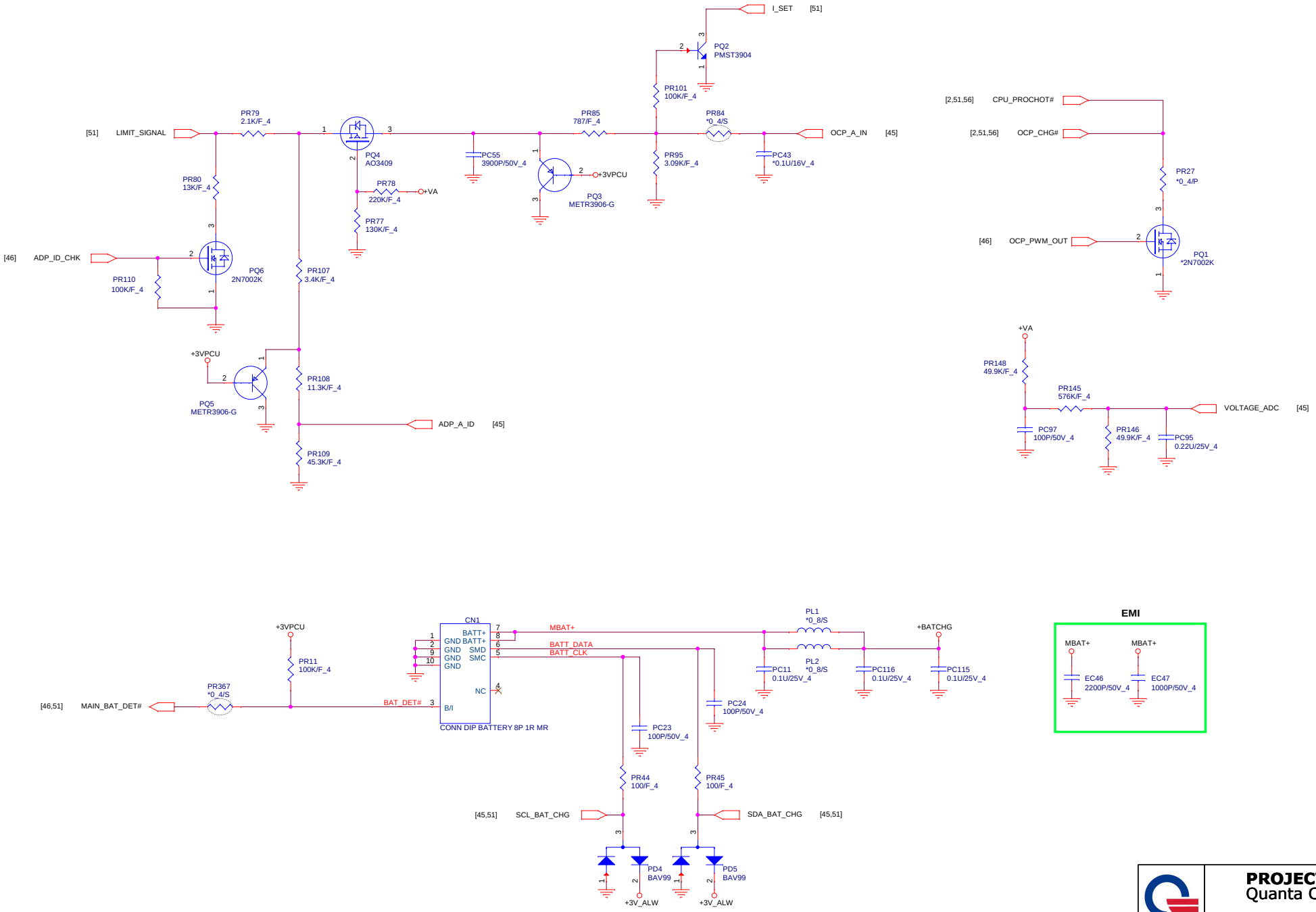
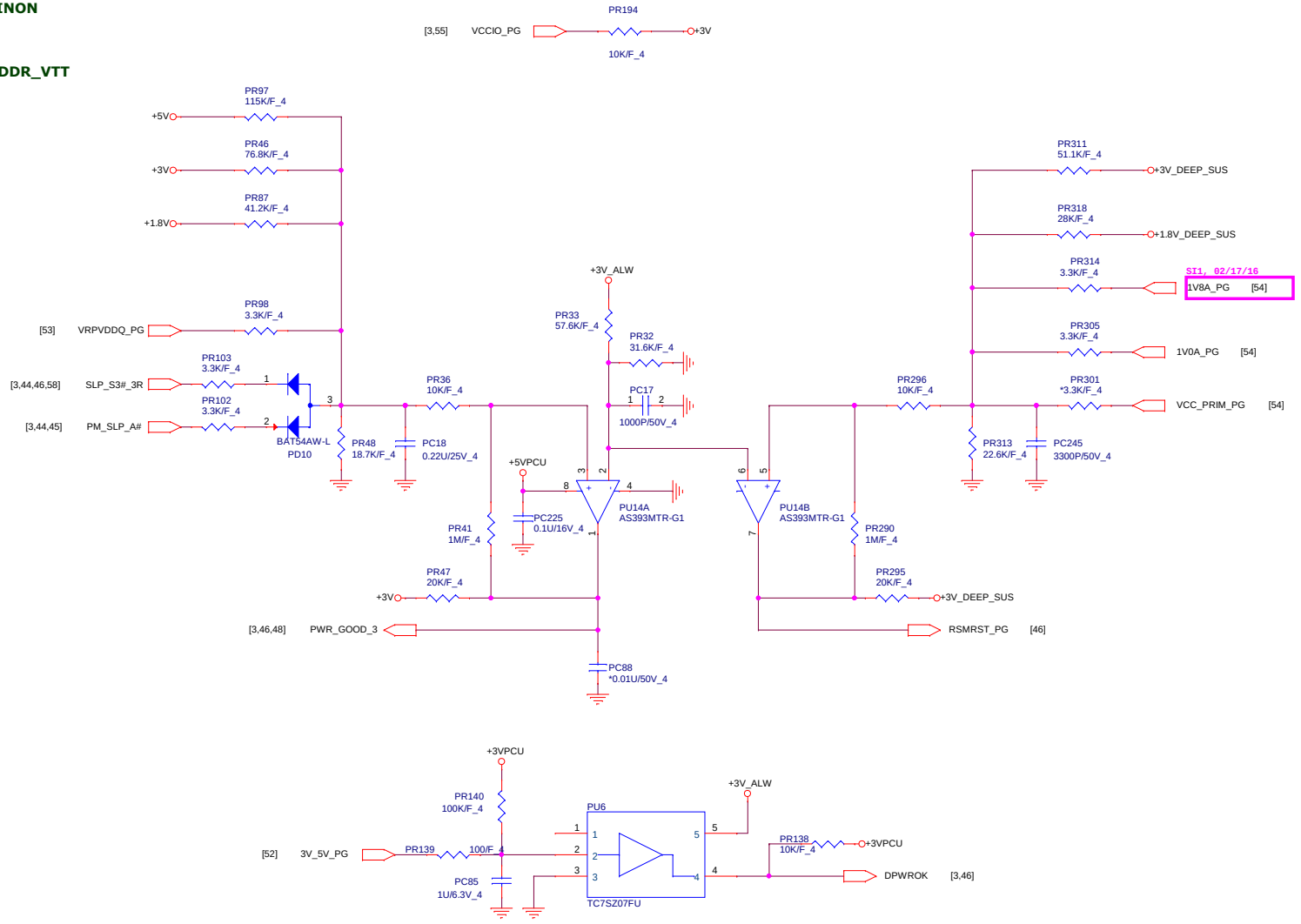
Adapter OCP



NB5	**PROJECT:400 Series** Quanta Computer Inc.	
	Size: Document Number: 62 -- CHARGER II	Rev: 1A
	Date: Thursday, May 12, 2016	Sheet 62 of 65

POK CKT

PM_SLP_S4# = SUSON
PM_SLP_S3# = MAINON
+V5S = +5V
+V3S = +3V
+V0.75S =+0.75V_DDR_VTT



[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,28,29,30,31,32,33,34,36,38,42,44,45,47,51,56,58,59] +3V
[8,27,29,30,40,42,43,54,58] +5V
[9,41,48,51,52,58,62] +3V_ALW

NB5

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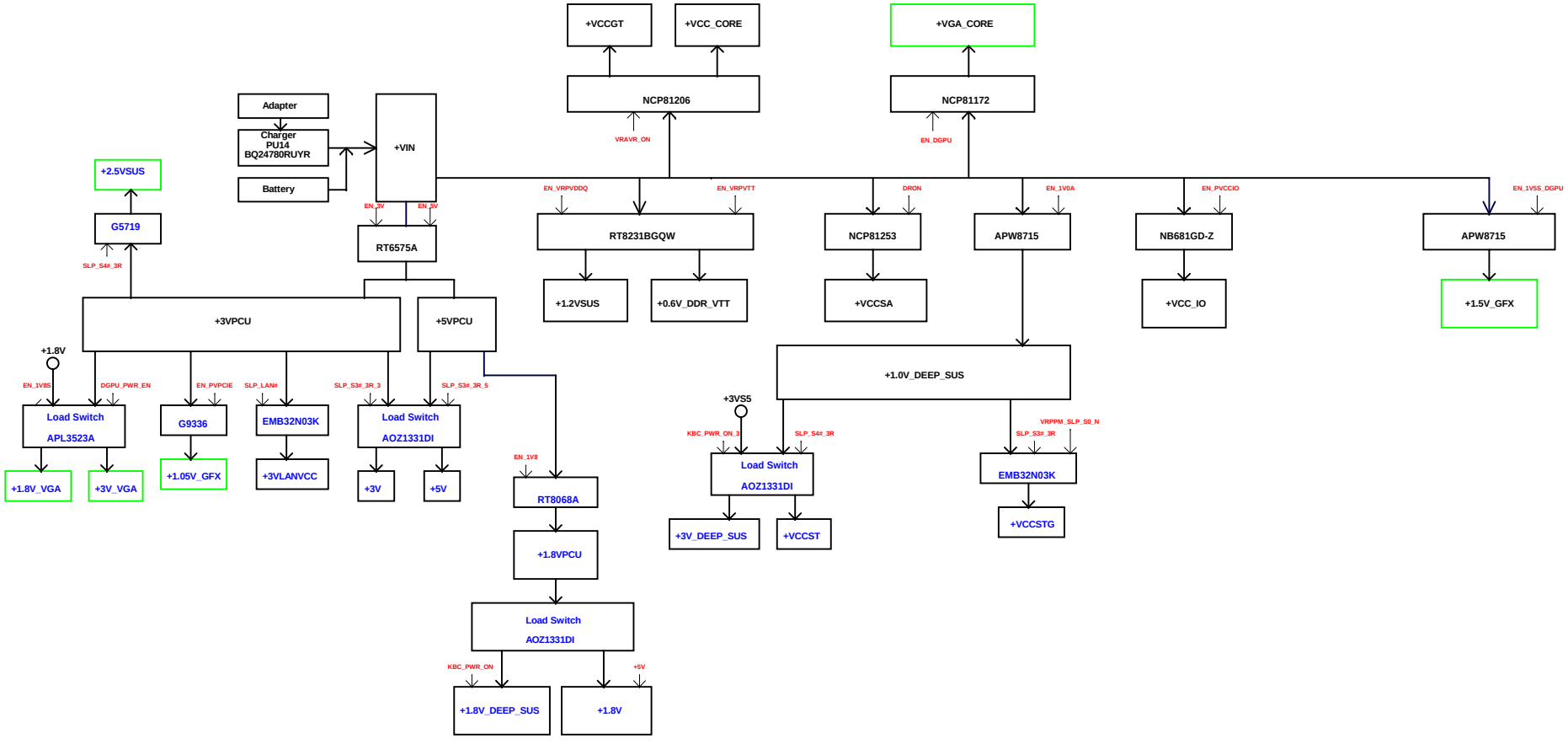
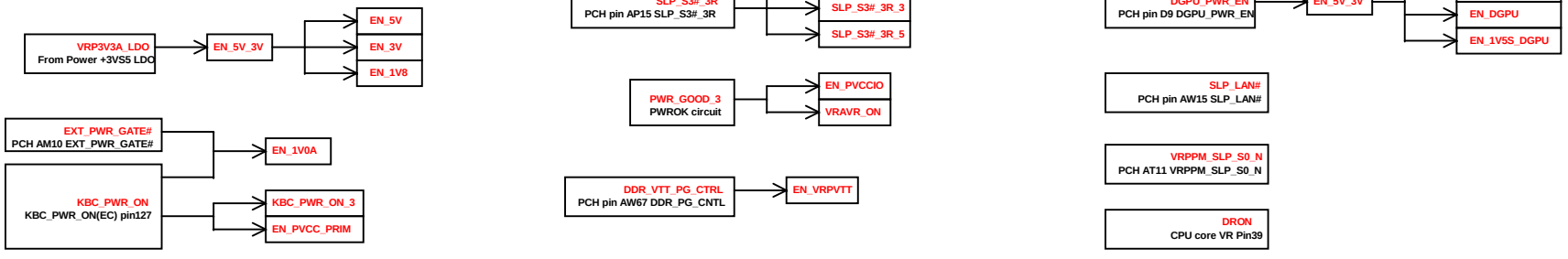
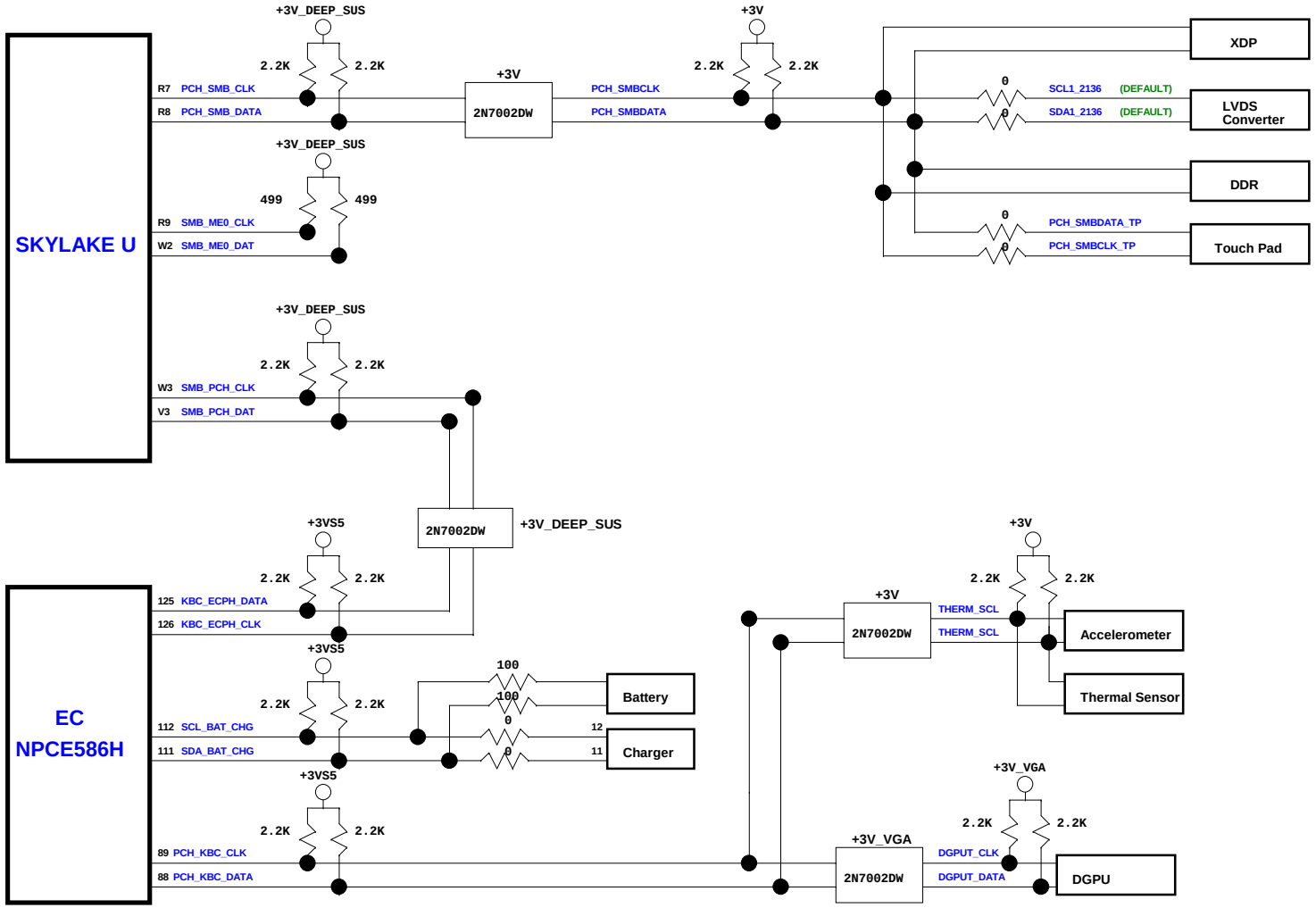
Quanta Computer Inc.

Size	Document Number	Rev
Custom	**63 -- PWROK**	1A
Date: Thursday, May 12, 2016	Sheet 63 of 65	



POWER ENABLE PIN





Example: *499/F_4 and *0_6/S
* means none-installed
499 means value
F means 1%
_4 means 0402 size
/S means short pad

Multiplexed HSIO Lane	Port Assignment
USB3 #1	USB2.0/USB3.0 Combo Jack(Left side down)
USB3 #2 / SSIC #1	USB2.0/USB3.0 Combo Jack(Left side up)
USB3 #3 / SSIC #2	NC
USB3 #4	NC
PCIE1 / USB3 #5	dGPU
PCIE2 / USB3 #6	dGPU
PCIE3	dGPU
PCIE4	dGPU
PCIE5	LAN
PCIE6	WLAN
PCIE7 / SATA #0	HDD (SATA)
PCIE8 / SATA #1	ODD (SATA)
PCIE9	Cardreader (PCIE)
PCIE10	NC
PCIE11 / SATA #1*	NC
PCIE12 / SATA #2	SSD (SATA)

USB2.0	Port Assignment
USB2 #1	USB2.0/USB3.0 Combo Jack(Left side down)
USB2 #2	USB2.0/USB3.0 Combo Jack(Left side up)
USB2 #3	WWAN
USB2 #4	USB2.0(Right side on USB Board)
USB2 #5	USB2.0(Right side on USB Board)
USB2 #6	Touch Screen
USB2 #7	Bluetooth
USB2 #8	Finger Print
USB2 #9	Camera
USB2 #10	NC

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Quanta Computer Inc.
Size: Custom | Document Number: 65 -- SMBus/Port Assignment | Rev: 1A
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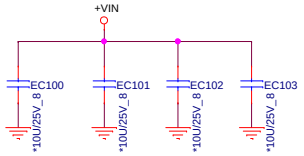
NB5



NB5

PROJECT:400 Series
Quanta Computer Inc.

Size	Document Number	Rev
Custom	**66 -- EMI and ISN**	1A
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