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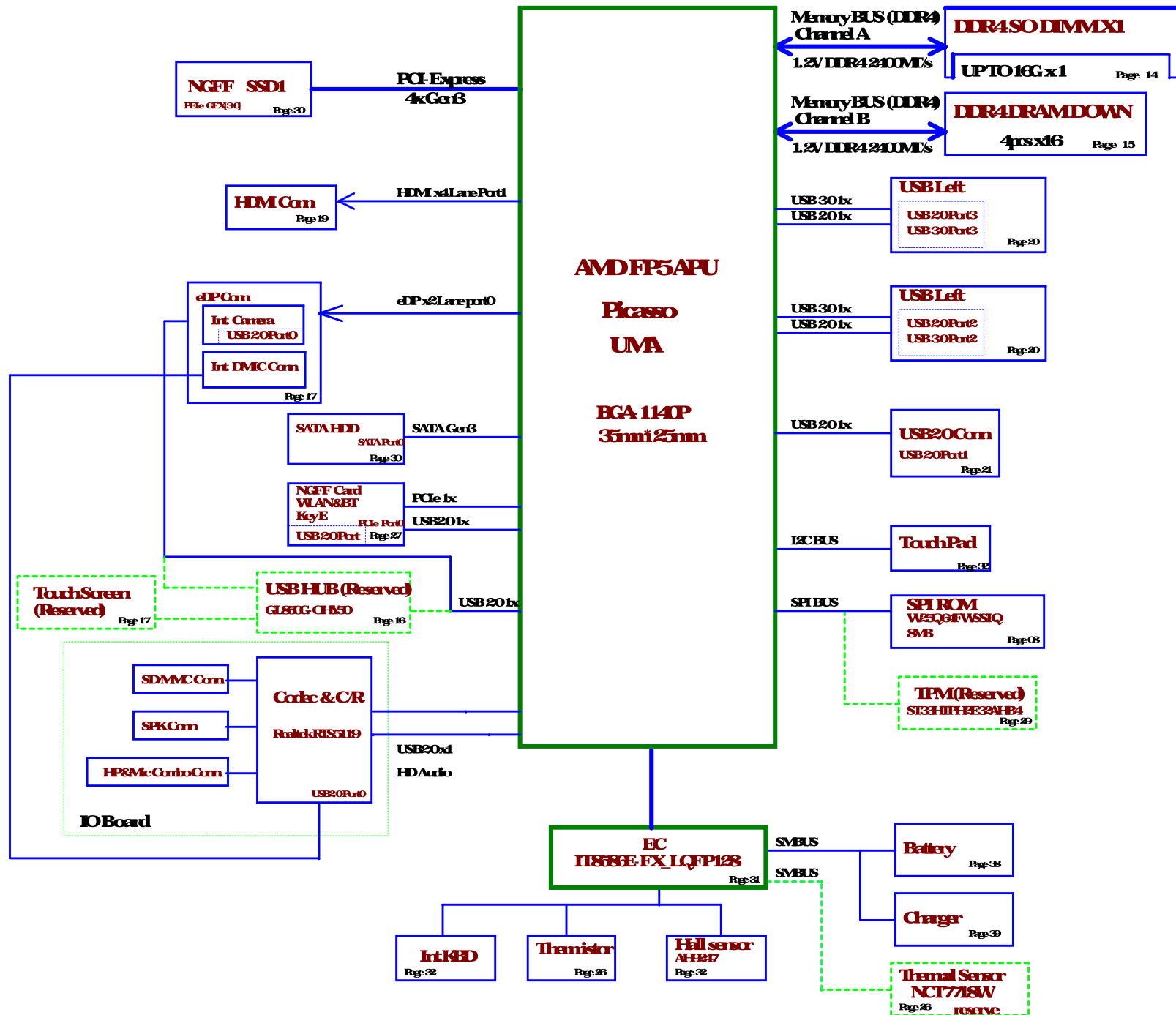
NM_C511 M/B Schematics Document

AMD FP5 PICASSO SOC with DDRIV

2019 05 28

REV: 1.0

Security Classification	LC Future Center Secret Data			Title		
Issued Date	20130815	Declassified Date	20130815	Cover Page		
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power plane State	B ₀ (+20VSB) +3ML +5MLP	+5VALW +3VALW (+3VALW/APU) +1.8VALW +0.9VALW	+1.2V	+5VS +3VS +1.8VS +0.9VS +0.6VS +2.5VS +VDDC_MIO +VDDC_SOC +VDDC +VDDI +3VGS +1.8VGS +1.35VGS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

EC Control Table

APU I2C address

SMBUS Control Table

EC SMBus1 address**EC SMBus2address**

EC SMBus3address

APU SMBus address



M2 SSDI

M2 SSDI

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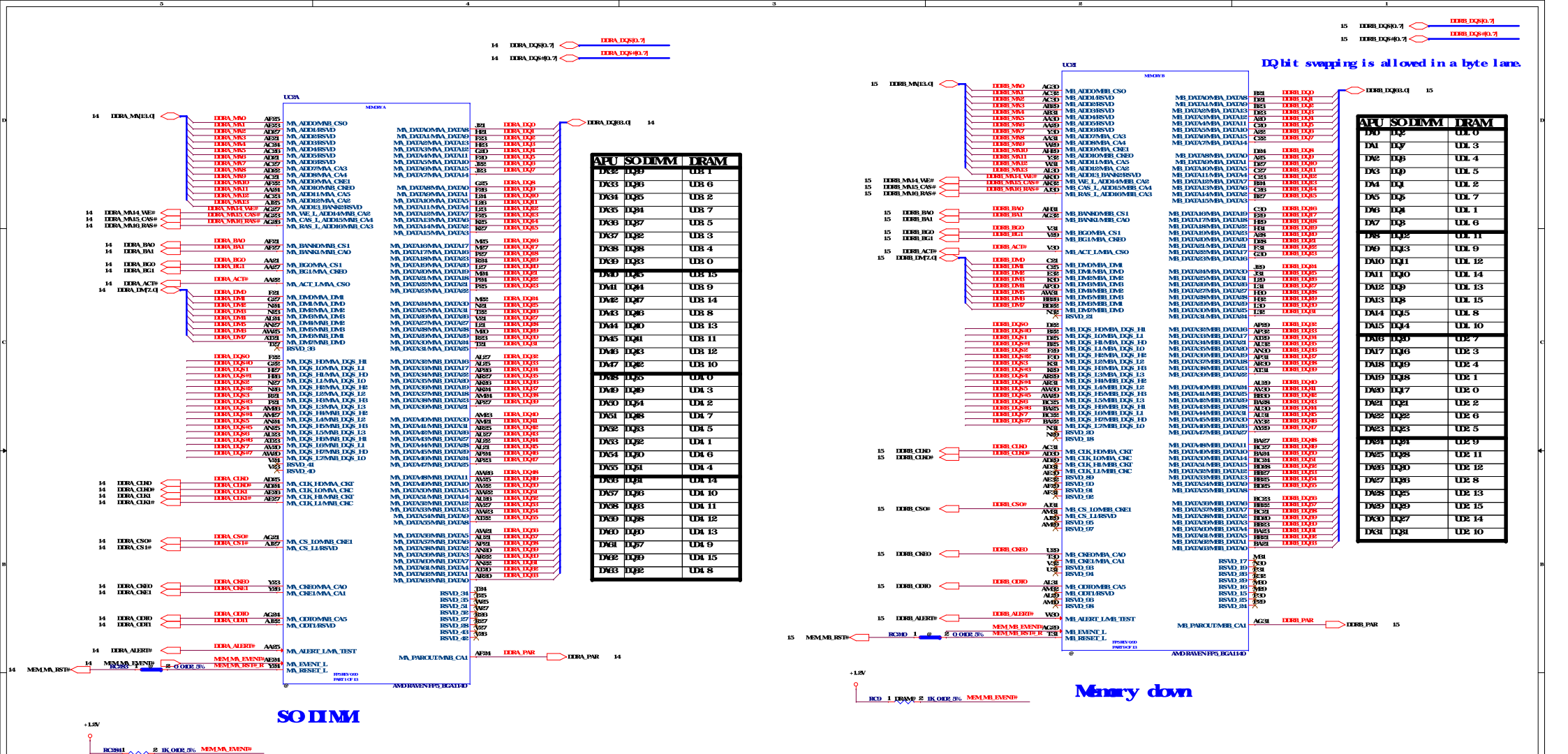
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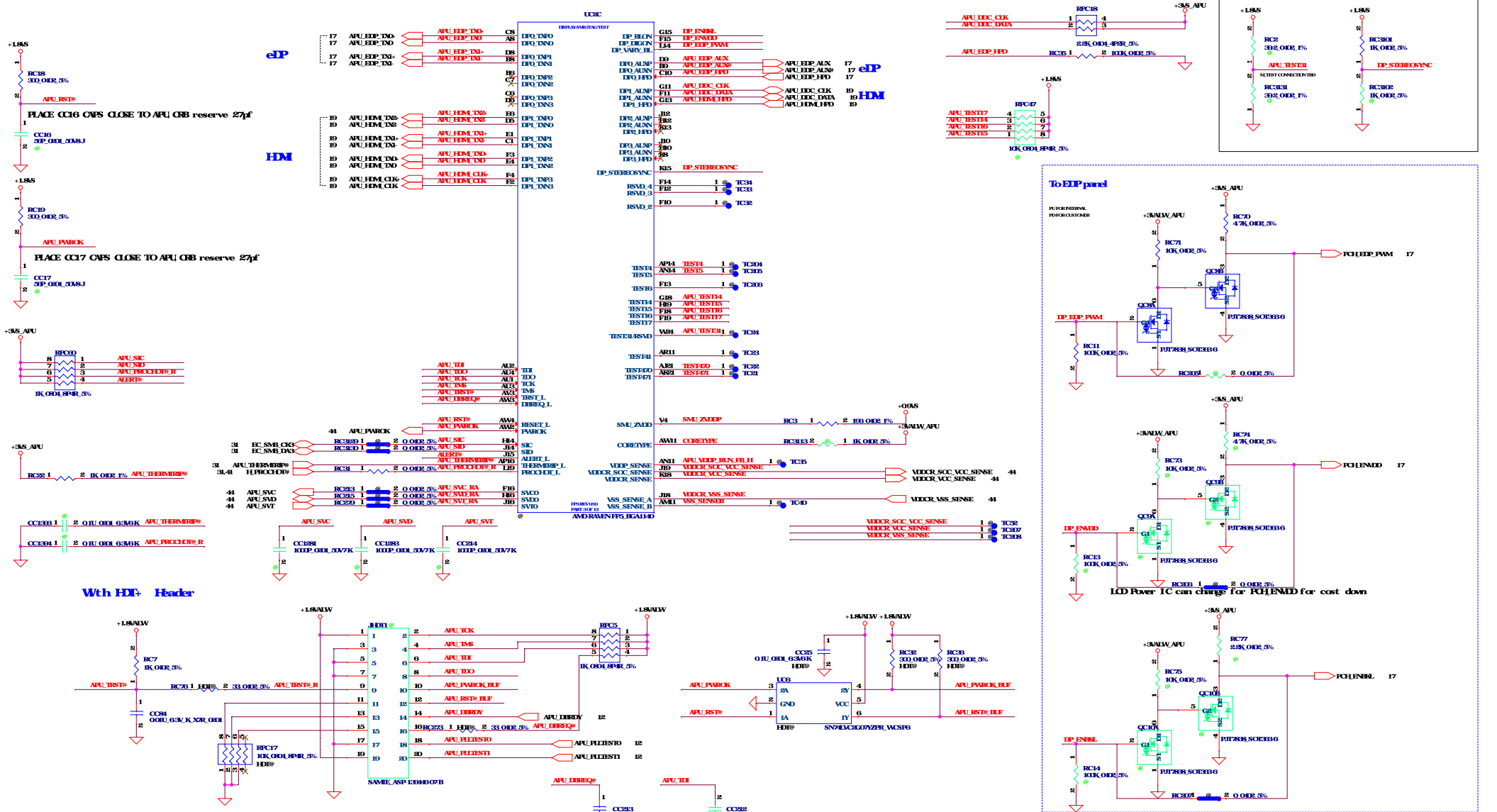
HDD

HDD

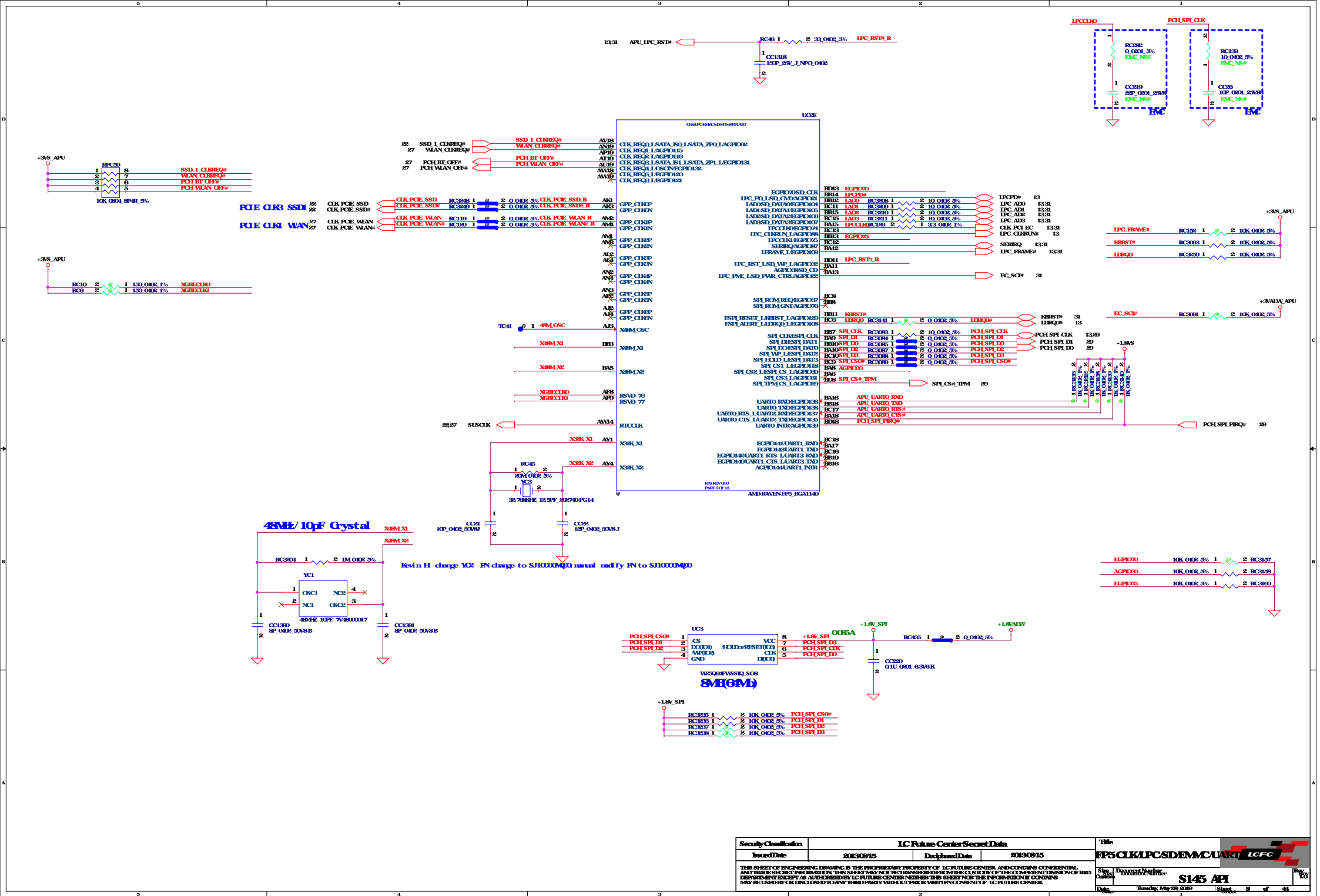
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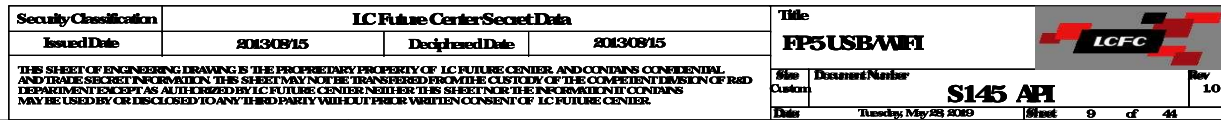
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FP5 (PCIe SATA IF)		1.0	
Size	Document Number	S145 AH	
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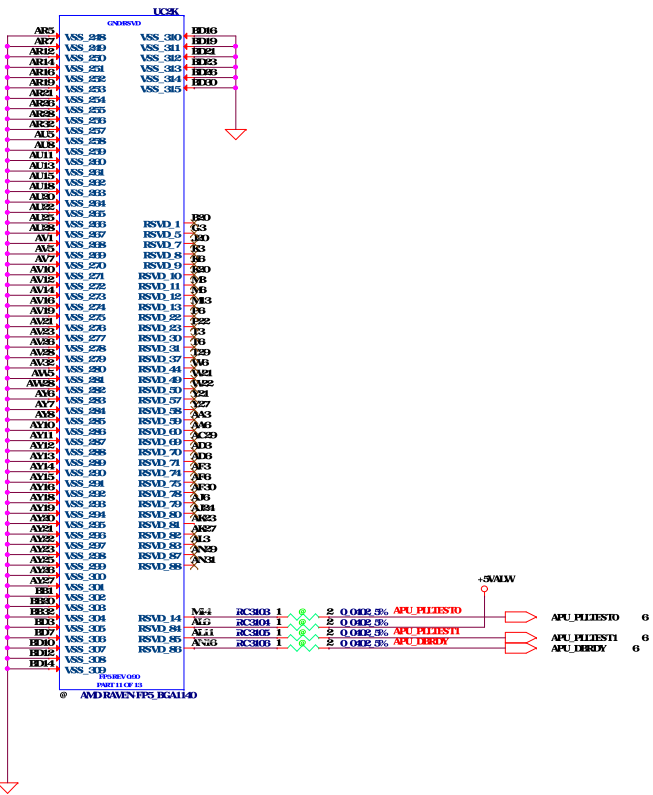
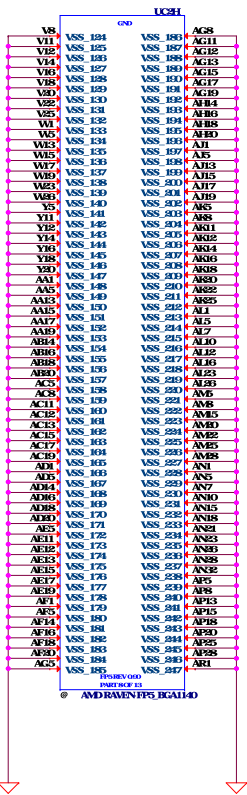
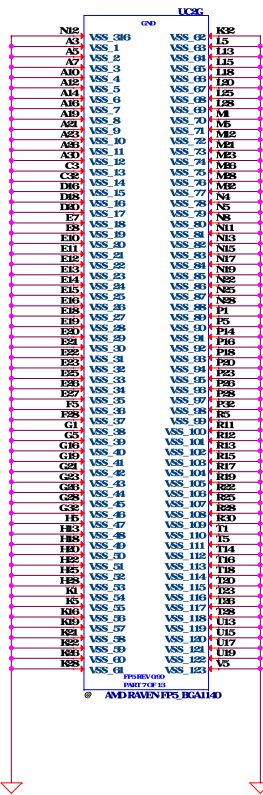


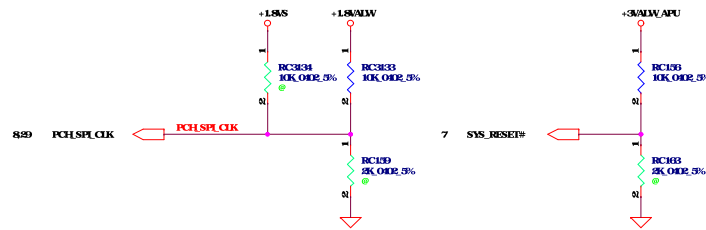


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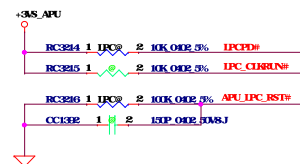
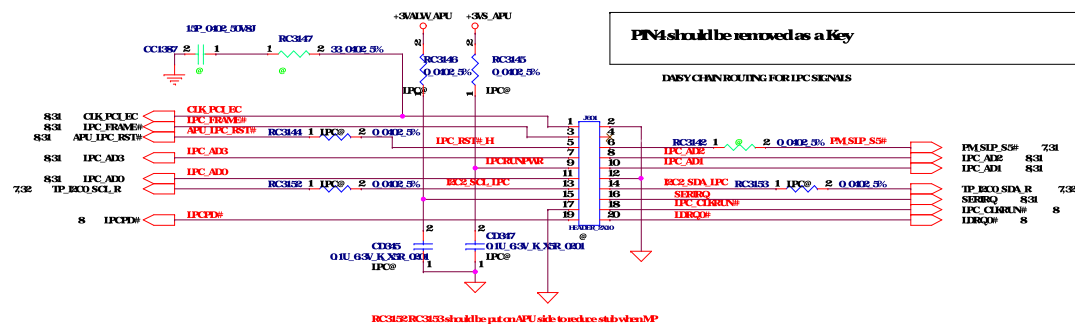




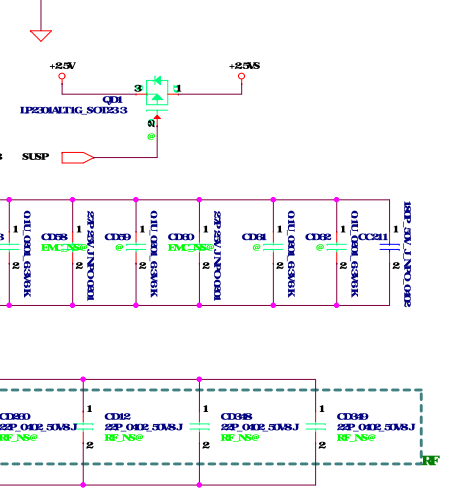
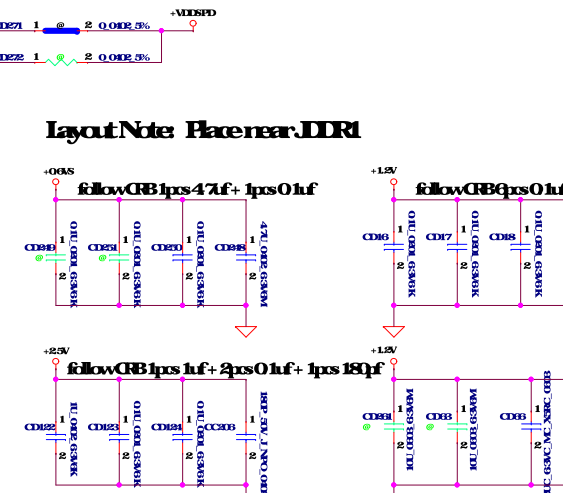
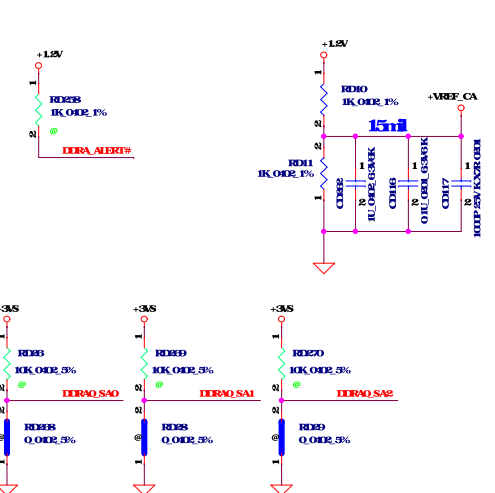


STRAP PINS	SYS_RESET#
PCH_SPL_CLK	1: USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS (DEFAULT) 0: USE 100MHZ PCIe CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RESET#	1: NORMAL RESET MODE (DEFAULT) 0: SHORT RESET MODE

IPC ROMULATOR HEADER

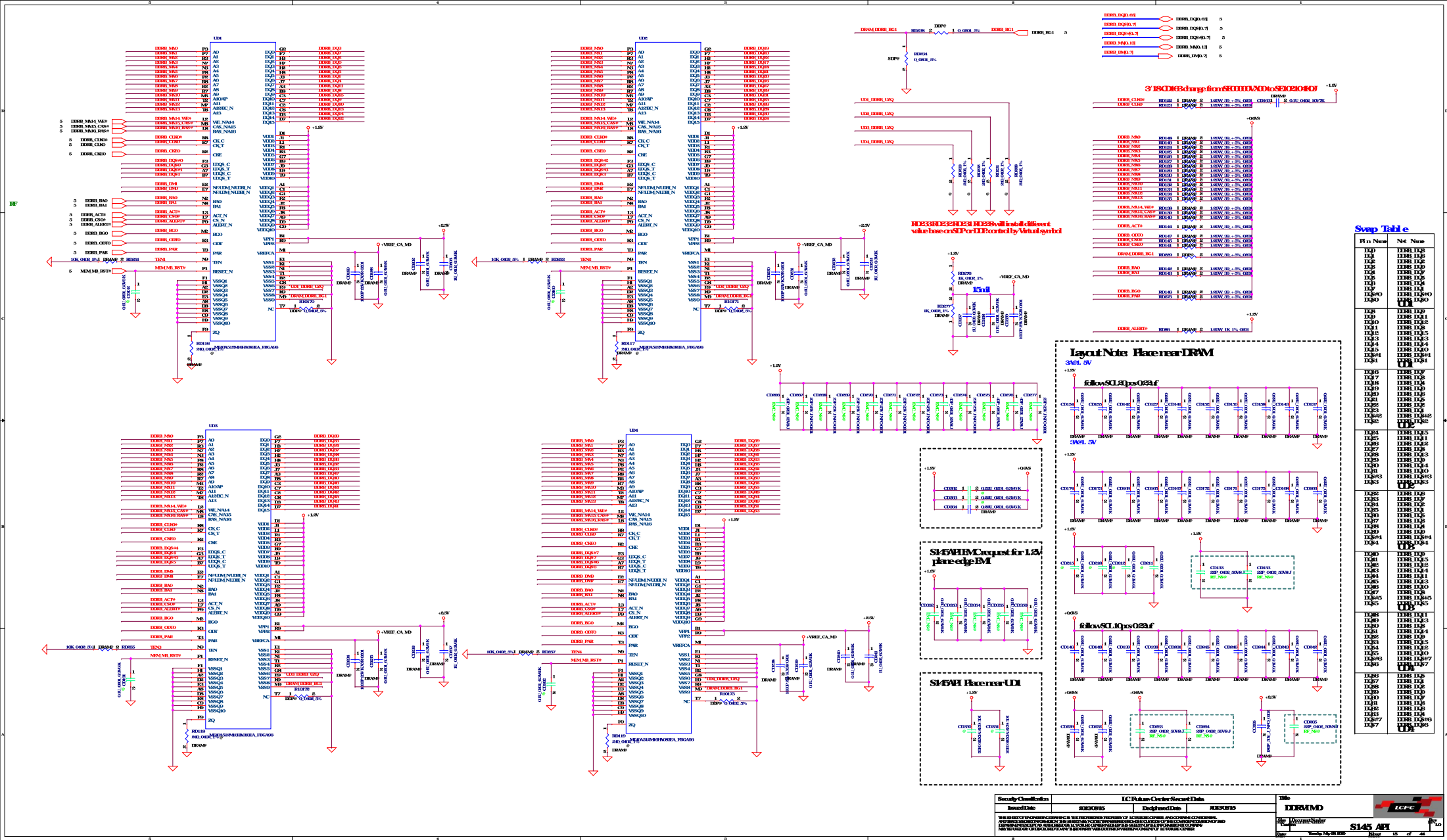


JDR1A



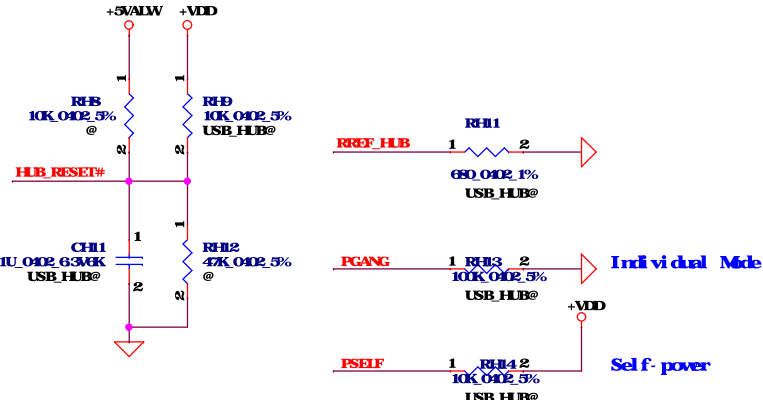
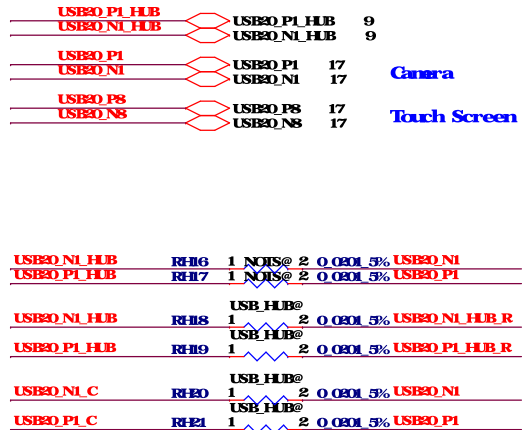
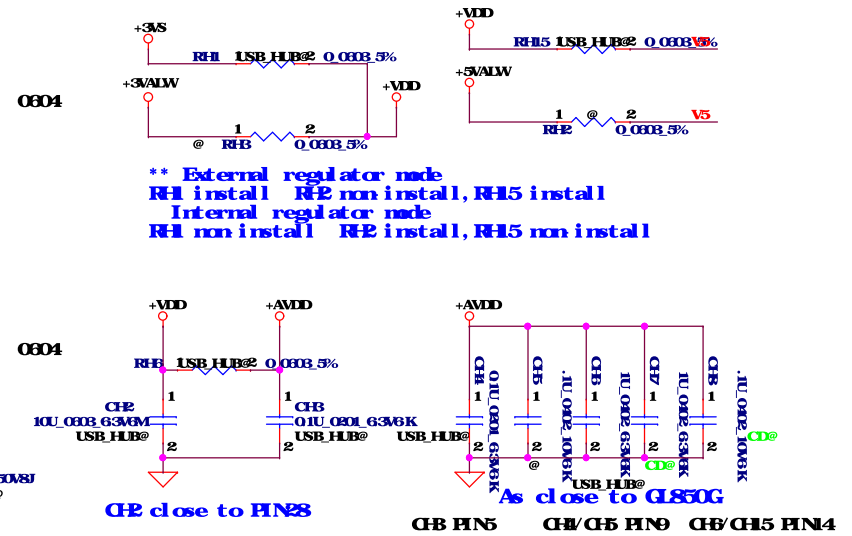
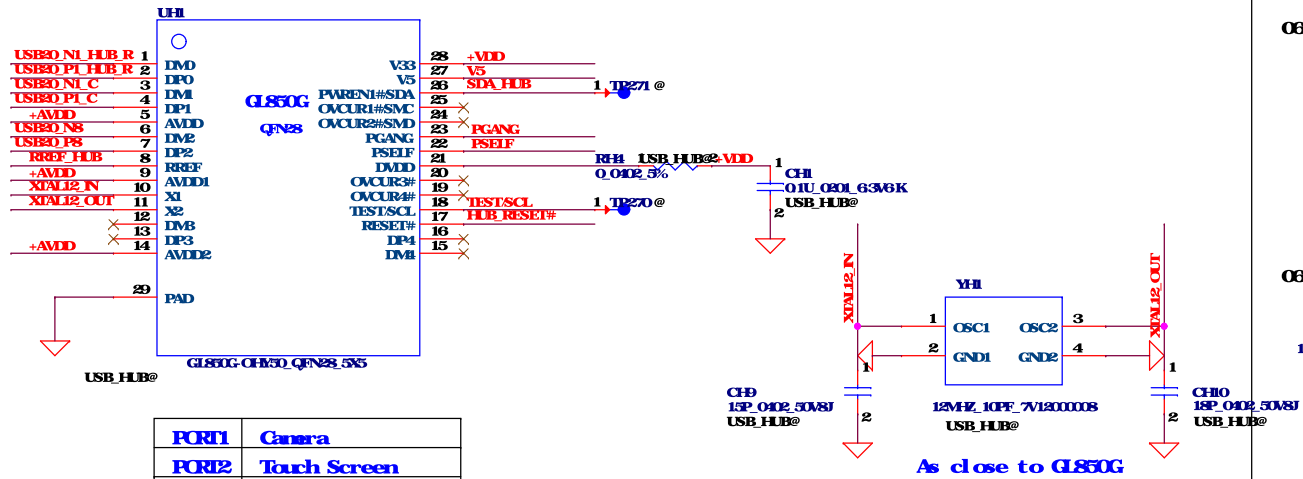
Flt Name	Net Name
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D1	DMA_D05
D2	DMA_D04
D3	DMA_D03
D4	DMA_D02
D5	DMA_D01
D6	DMA_D00
D7	DMA_D07
D8#0	DMA_D8#0
D80	DMA_D80
D8	DMA_D03
D9	DMA_D09
D10	DMA_D04
D11	DMA_D10
D12	DMA_D12
D13	DMA_D08
D14	DMA_D05
D15	DMA_D01
D16#1	DMA_D16#1
D18	DMA_D18
D16	DMA_D00
D17	DMA_D21
D18	DMA_D22
D19	DMA_D19
D20	DMA_D16
D21	DMA_D17
D22	DMA_D23
D23	DMA_D18
D24#2	DMA_D24#2
D28	DMA_D28
D24	DMA_D28
D25	DMA_D29
D26	DMA_D21
D27	DMA_D27
D28	DMA_D24
D29	DMA_D25
D30	DMA_D20
D31	DMA_D28
D32#3	DMA_D32#3
D33	DMA_D33
D32	DMA_D33
D33	DMA_D37
D34	DMA_D34
D35	DMA_D38
D36	DMA_D32
D37	DMA_D36
D38	DMA_D35
D39	DMA_D30
D39#4	DMA_D39#4
D39#4	DMA_D34
D40	DMA_D44
D41	DMA_D40
D42	DMA_D27
D43	DMA_D43
D44	DMA_D41
D45	DMA_D45
D46	DMA_D46
D47	DMA_D42
D48#5	DMA_D48#5
D485	DMA_D485
D48	DMA_D48
D49	DMA_D49
D50	DMA_D55
D51	DMA_D50
D52	DMA_D52
D53	DMA_D53
D54	DMA_D54
D55	DMA_D51
D56#6	DMA_D56#6
D56	DMA_D56
D56	DMA_D50
D57	DMA_D58
D58	DMA_D53
D59	DMA_D59
D60	DMA_D51
D61	DMA_D57
D62	DMA_D58
D63	DMA_D52
D64#7	DMA_D64#7
D67	DMA_D67

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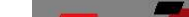


Swp Table	
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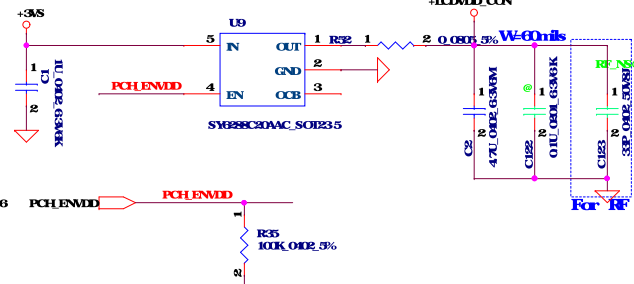
for USB Hub update to CH50, manual modify PN to G1850G-CH50



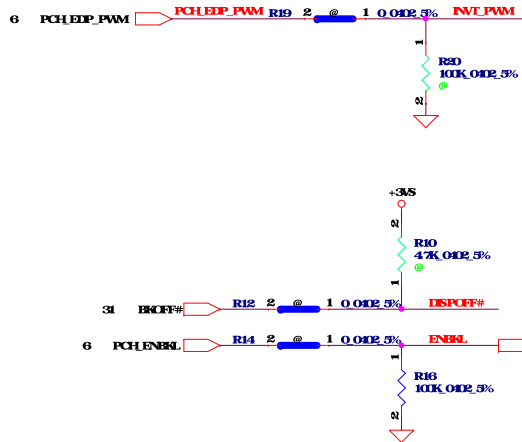
Security Classification	LC Future Center Secret Data		
Issued Date	20160816	Declassified Date	20170815
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Title			
USB Hub			
Size	Document Number	S145 API	
B		Rev 10	
Date	Tuesday, May 28, 2019	Sheet	16 of 44

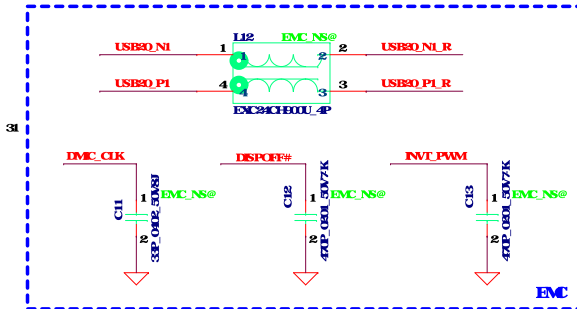
LCDPOWER CIRCUIT



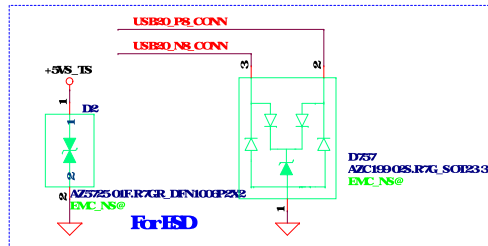
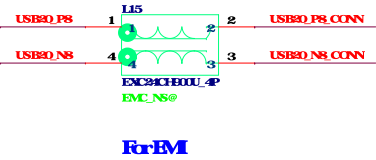
APU output enable Voh min is 1.8V/0.45V=1.35V



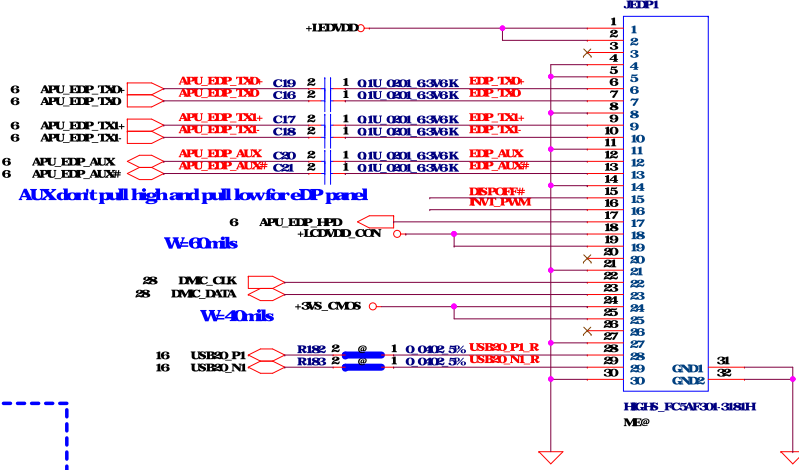
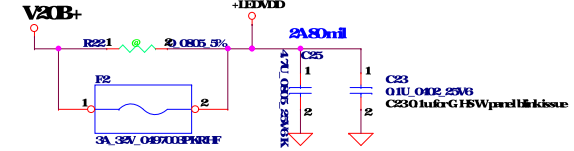
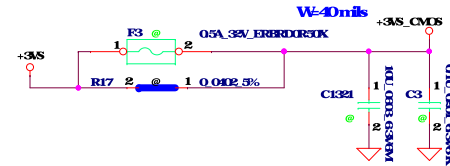
CMOS Camera



TouchScreen



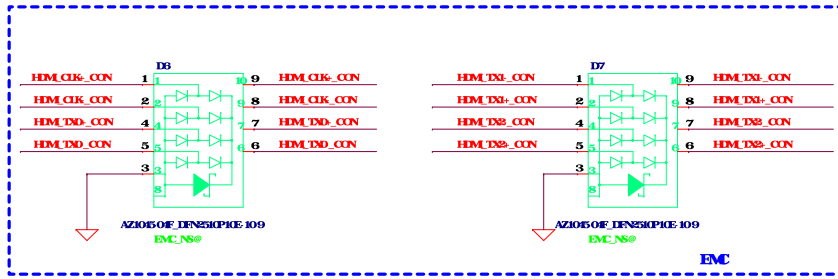
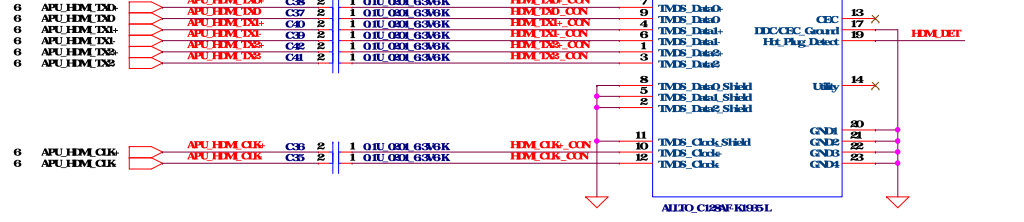
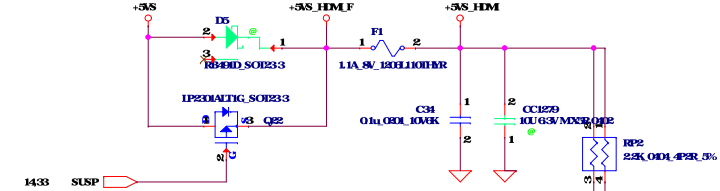
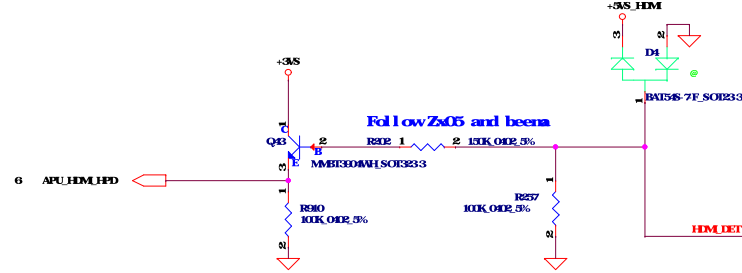
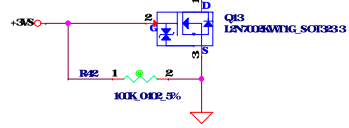
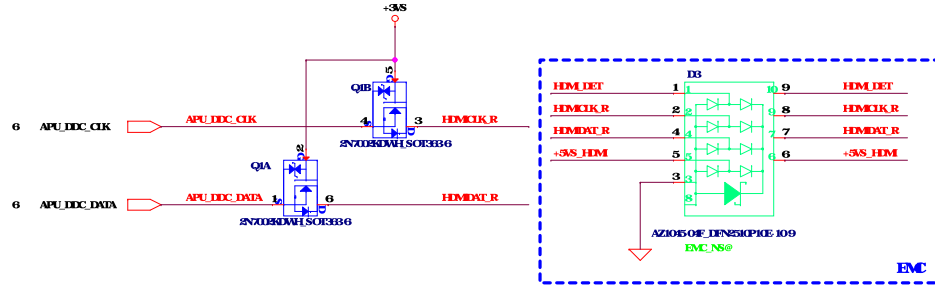
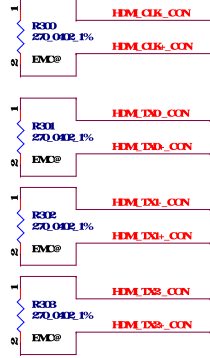
B+ to +LEDVDDPOWER



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Title	eDPC/MOS	
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3/19 S145AF EMC request for HDM

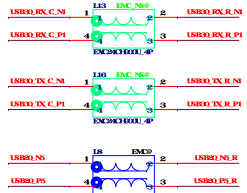


Security Classification		LC Future Center Secret Data		Title	
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				Custom	S145 AF
				Date	Tuesday, May 28, 2013
				Sheet	10 of 44

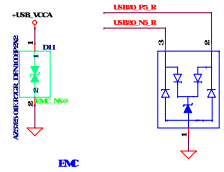
LEFT SIDE USB30PORT-2



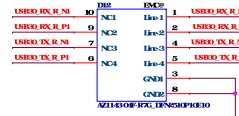
LowActive 2A



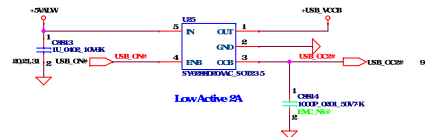
EMC



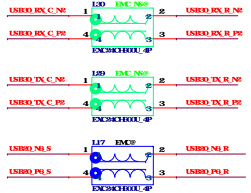
EMC



USB30PORT

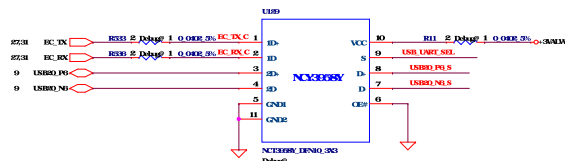


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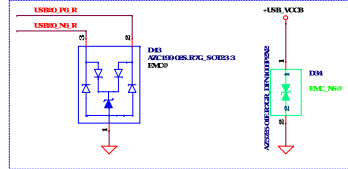
For USBDebugFunction

7 USB30PORT-2 Debug 1 USB VCC 2A



USB RX C, TX, PS pins connected to USB RX C, TX, PS pins of the USB connector.

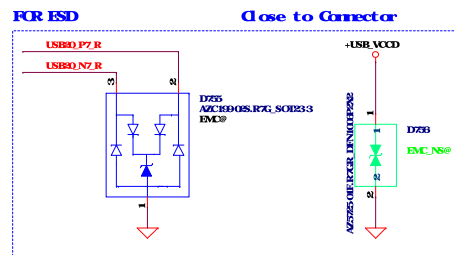
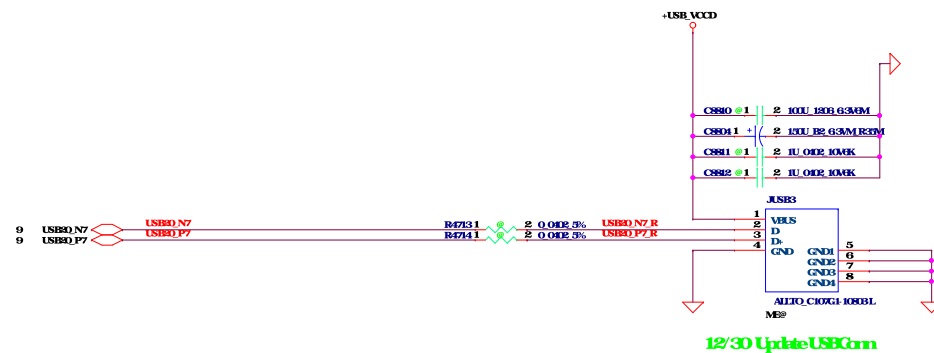
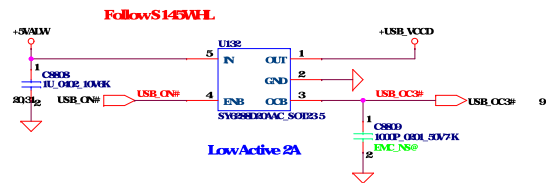
FOR ISD

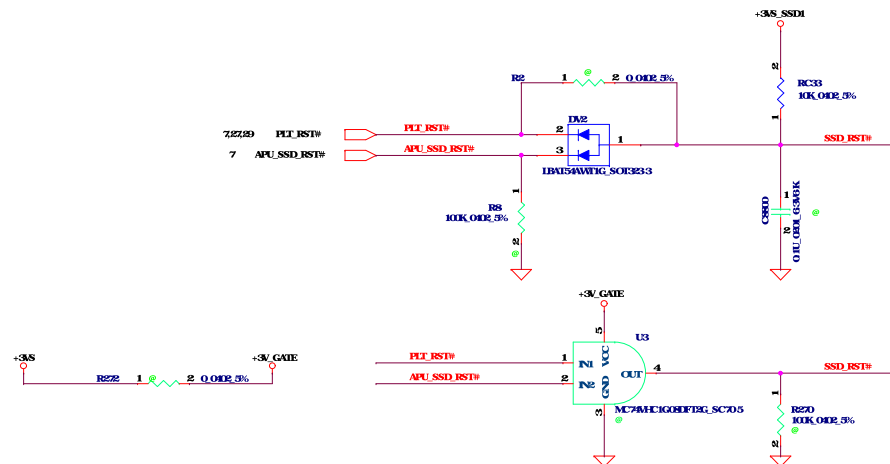
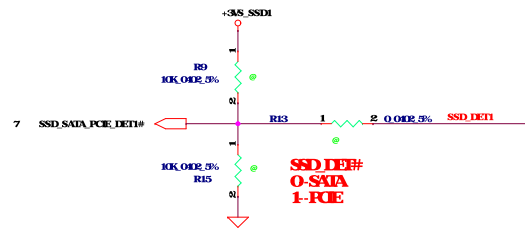
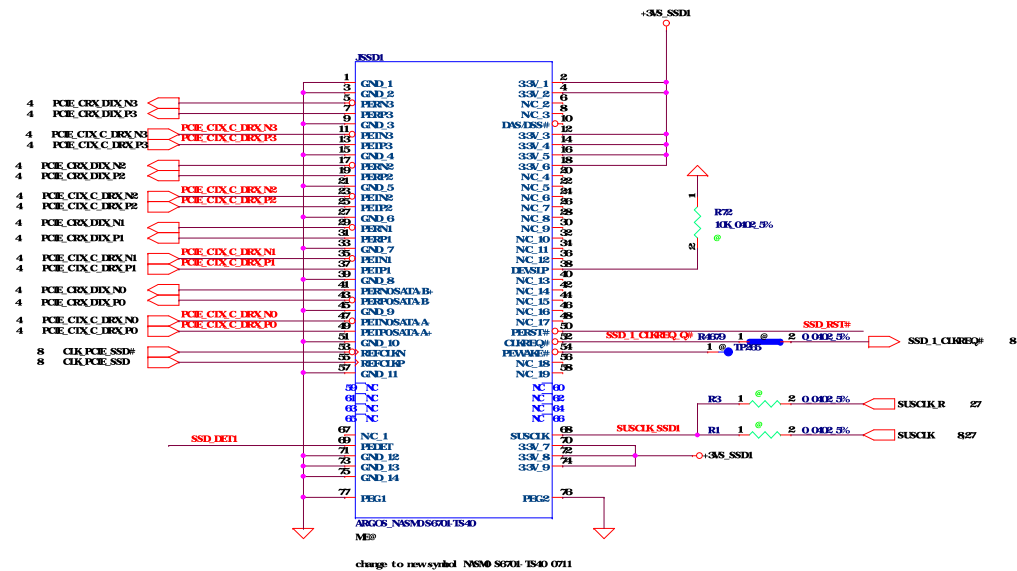
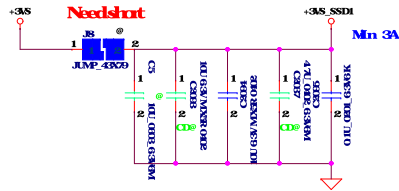


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Set Input	Set Input
Set output Low	ENABLE

USB30PORT	Remarking
Set Input	ENABLE
Set output Low	ENABLE

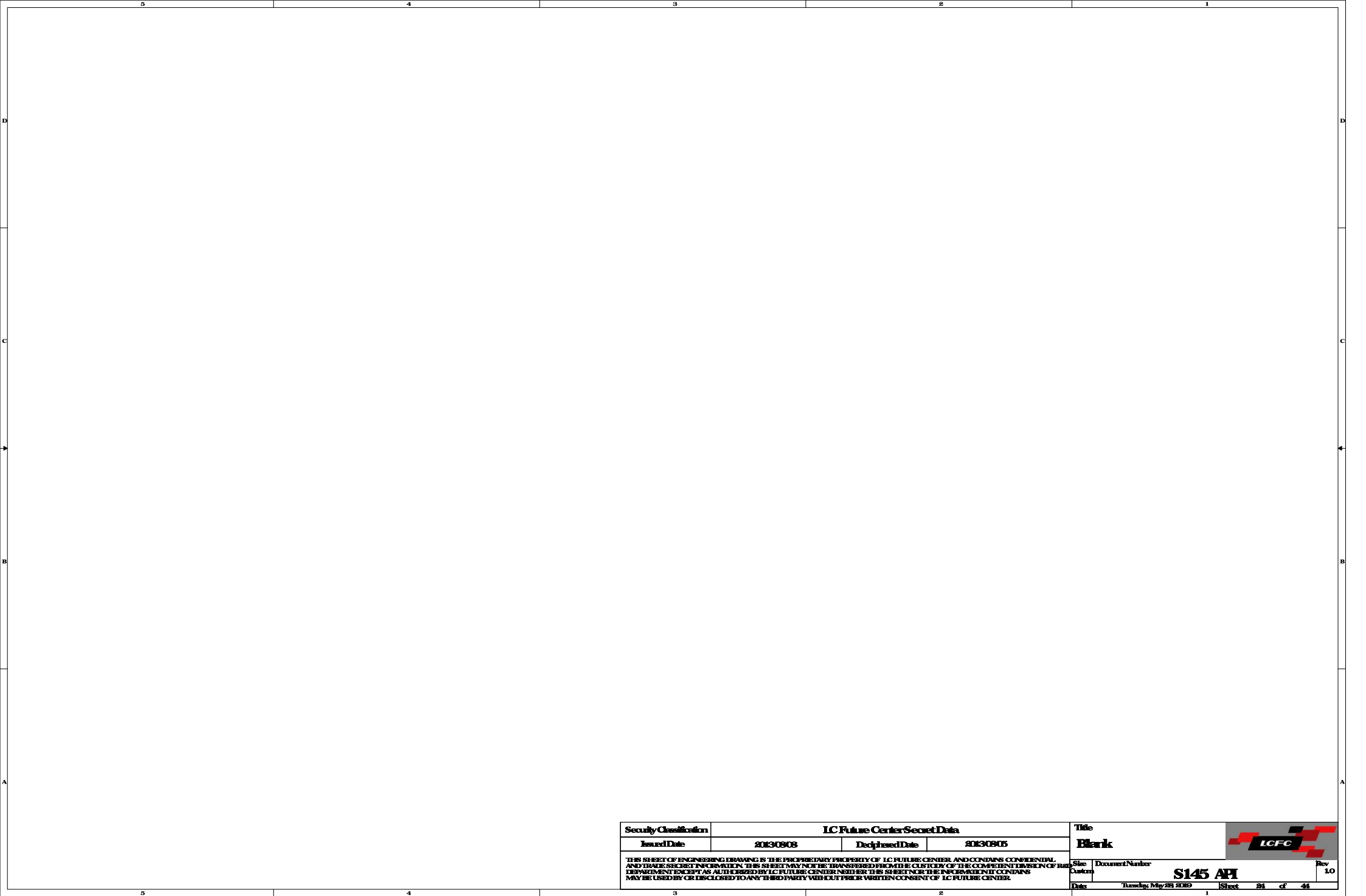
CS	S	FUNCTION
H	N	ENABLE
L	L	ENABLE
L	H	ENABLE





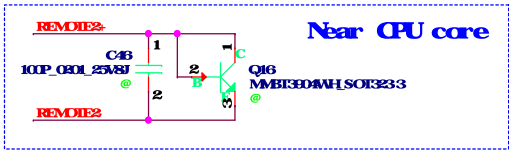
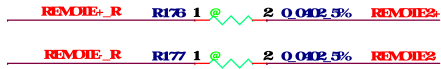
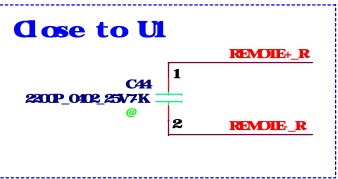
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D				D
C				C
B				B
A				A
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				Date	Tuesday, May 28 2019	Sheet	23 of 44



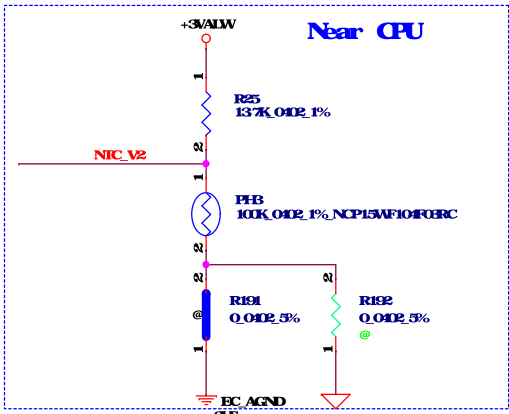
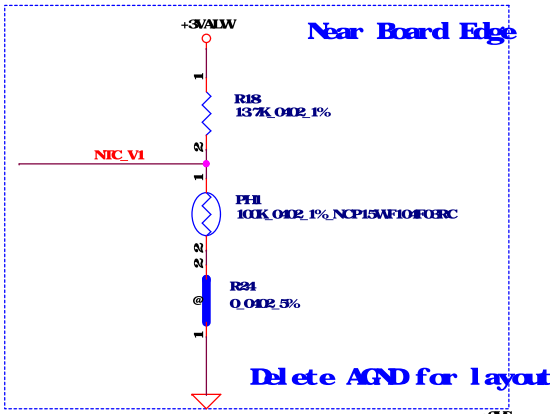
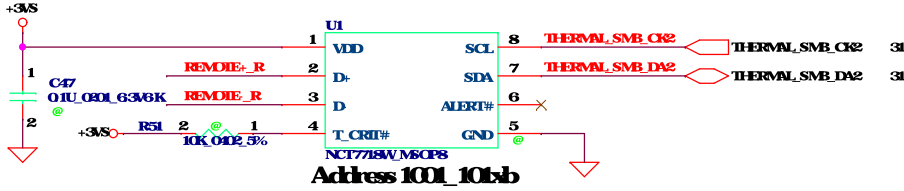
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				Date	Tuesday, May 25, 2010	Sheet 25 of 44

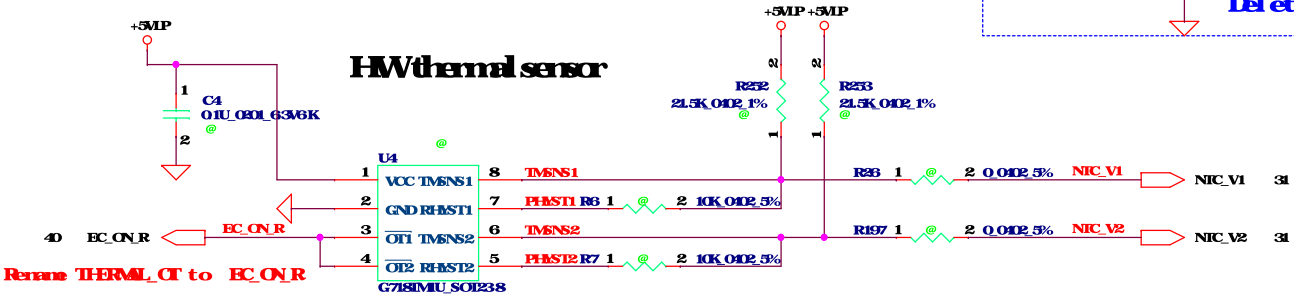


REMOIE+/-_R REMOIE1+/-, REMOIE2+/- :
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Trace length <8"

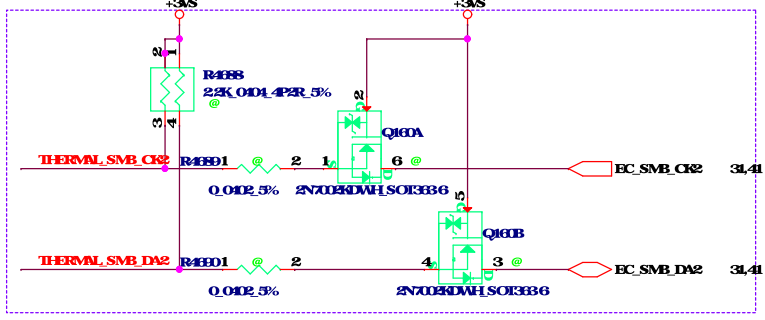
SMSC thermal sensor placed near DIMM



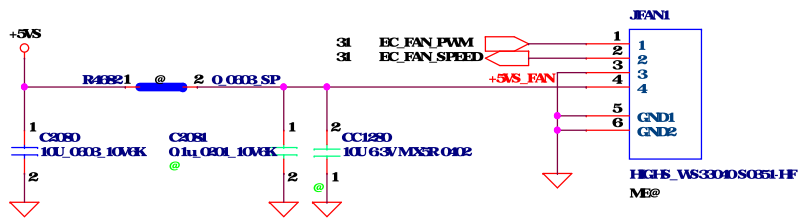
HW thermal sensor



over temperature threshold
RSET=3° RIM1
92+/- 30C
Hysteresis temperature threshold
RHST=(RSET RIM1) / (3° RIM1 RSET)
56+/- 30C

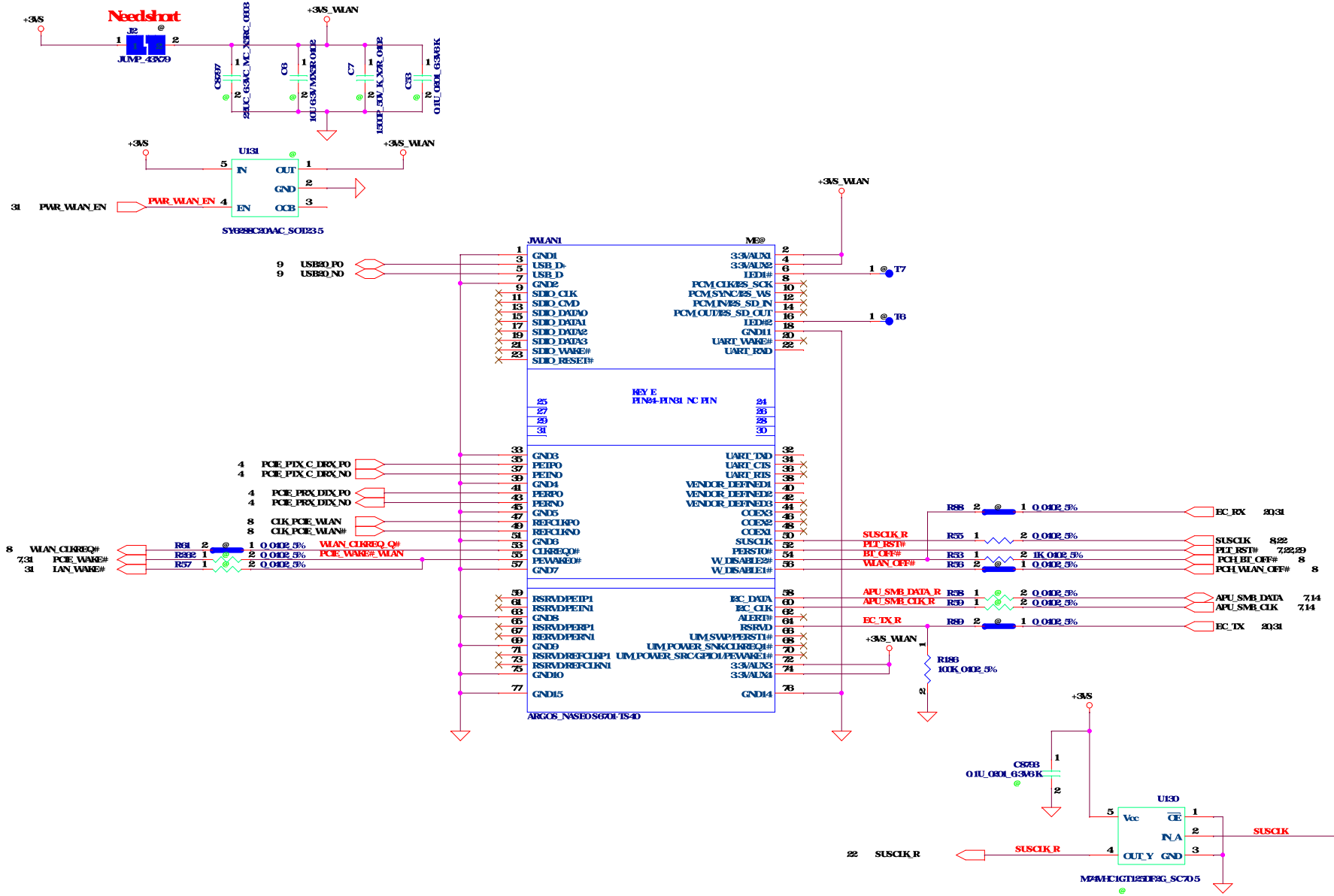


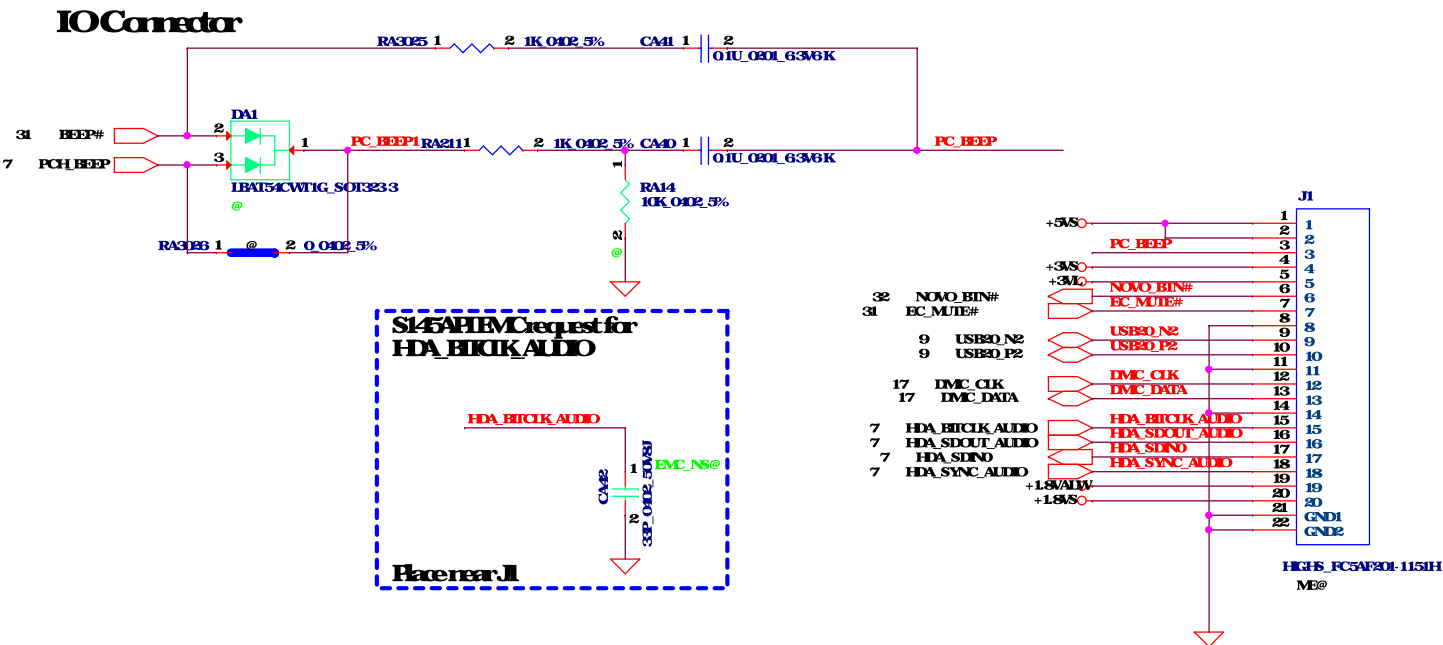
FAN Conn



Security Classification		LC Future Center Secret Data		Title	
Issued Date	20130808	Declassified Date	20130905	Thermal sensor/FAN CONN/IFM	
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				S145 AP1	
				Date	Rev
				Tuesday, May 28, 2013	1.0
				Sheet 83	of 44

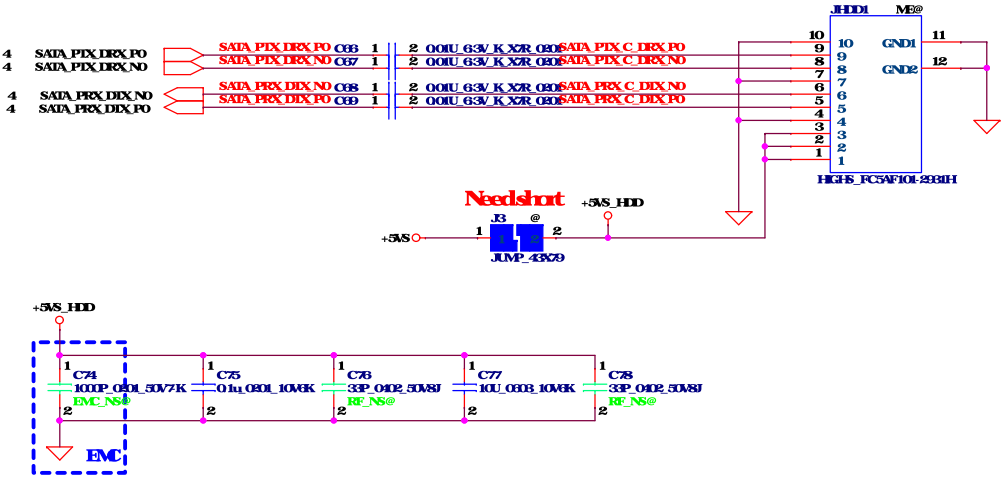
Mini-Express Card(WLAN/WMAX)





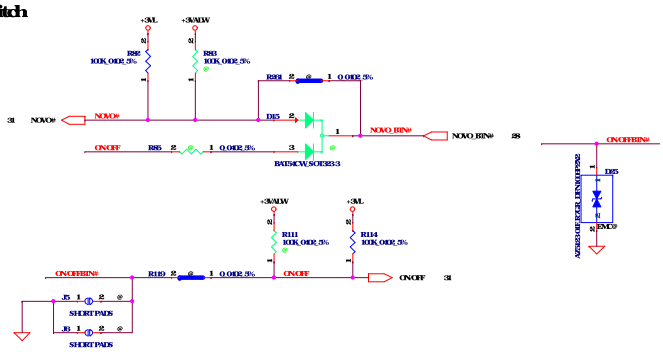
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SATA HDD Conn

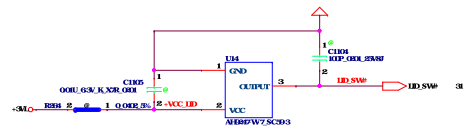


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D		↑		E		F			
						G		H	
						Date		Tuesday, May 28 2009	
						Sheet		30 of 44	

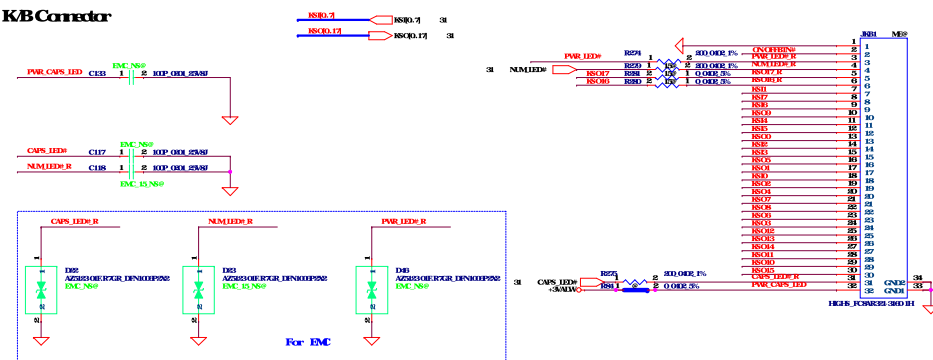
ON/OFF switch



LID switch



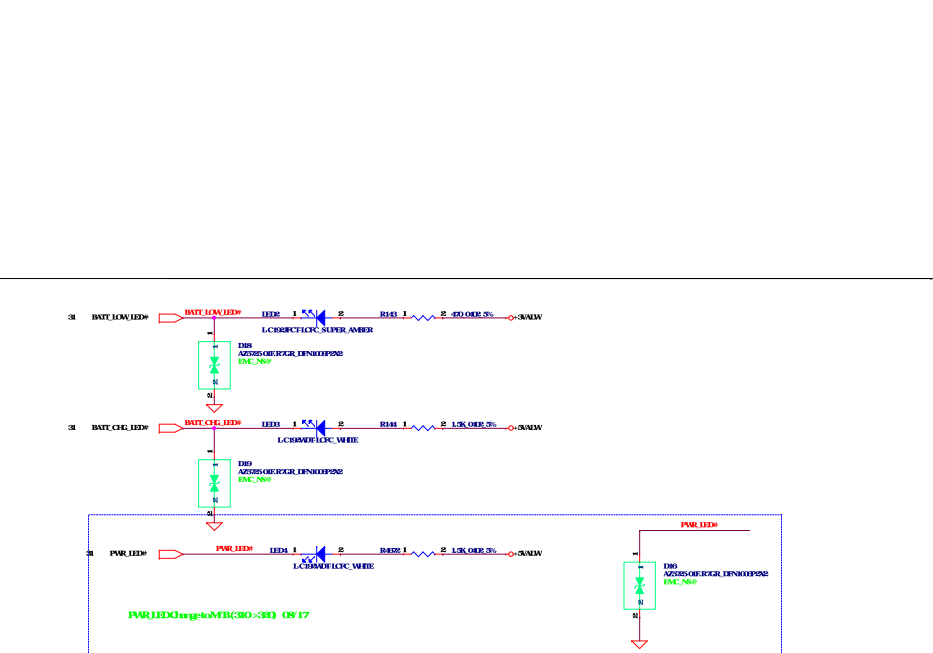
K/B Connector



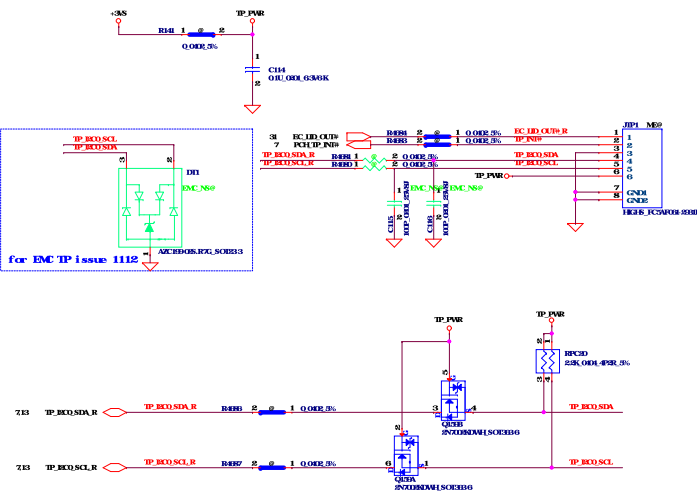
KB Backlight Connector



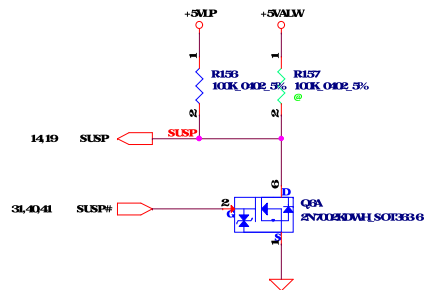
Finger Print Connector



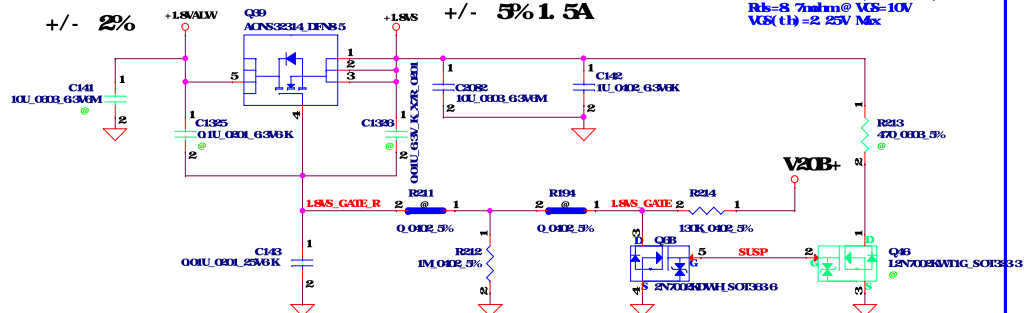
TPB Connector



Security Classification	ICF Phase Control Secret Data		Title	
Issued Date	2009/01/01	Declassified Date	2020/01/01	KEP/PWR/LED/TPB Conn
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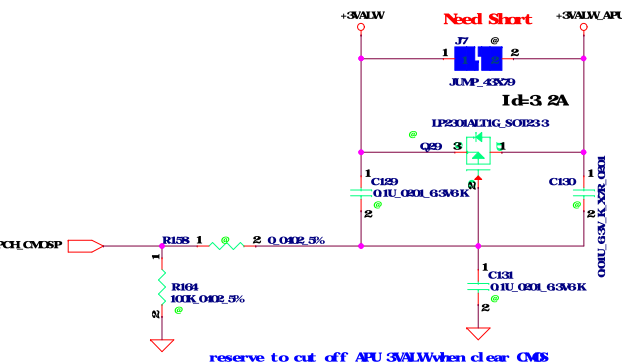
+1.8V_{ALW} to +1.8V_S



ACS832314
V_{DS}=30V V_{GS}=20V I_D=32A
R_{DS(on)}=8.7mΩ @ V_{GS}=10V
V_{GS(th)}=2.25V Max

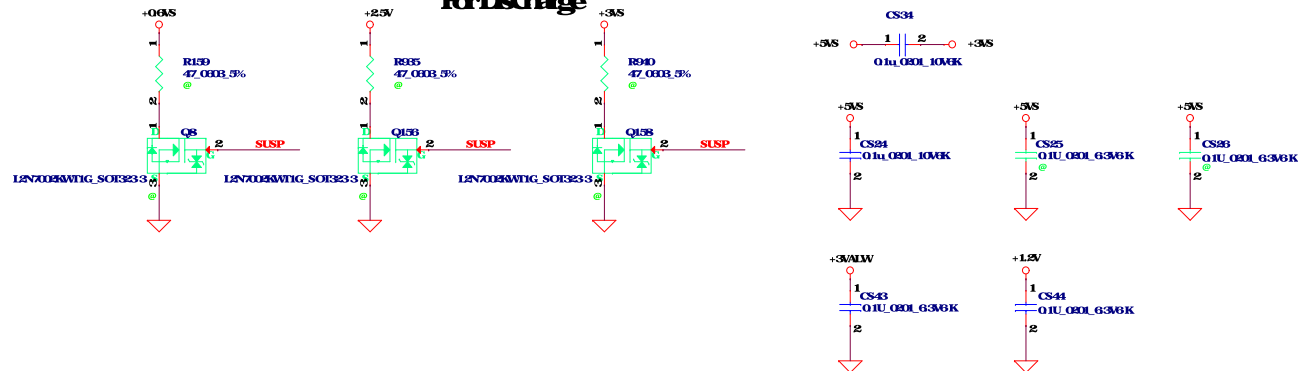
20VSB will change to 6V in DC mode, careful the Res divide voltage

+3V_{ALW} to +3V_{ALW}APU

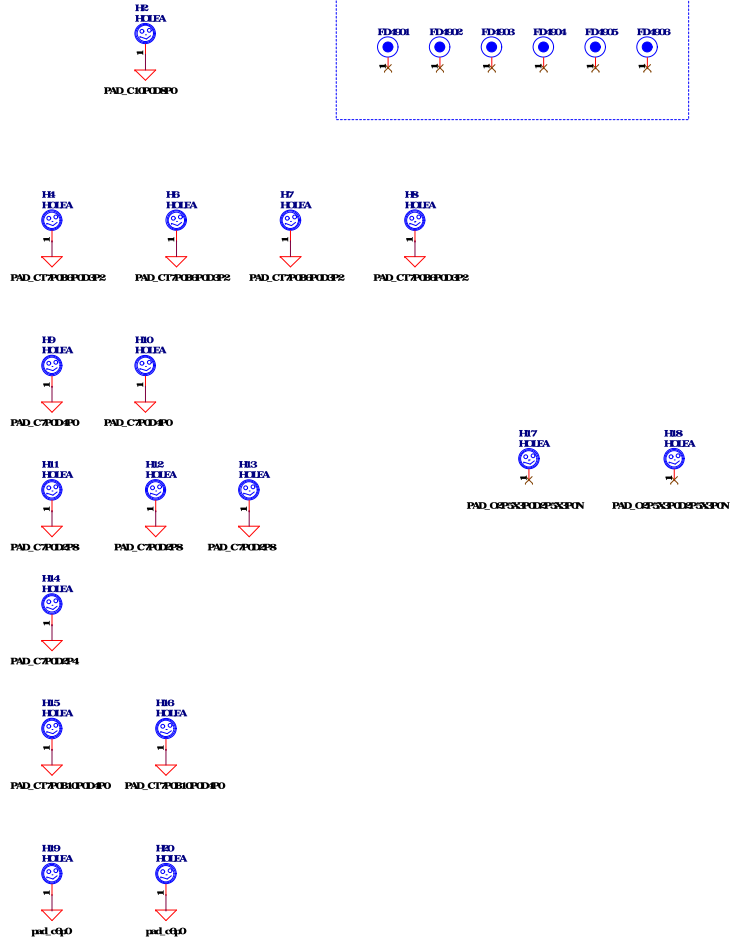


reserve to cut off APU 3V_{ALW} when clear OMS

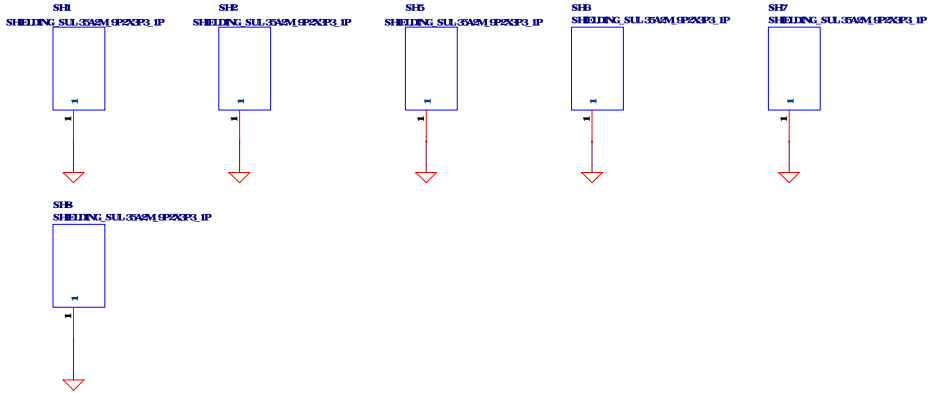
For Discharge



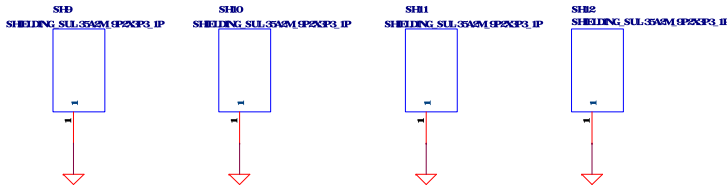
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Issued Date	20130815	Declassified Date	20130815	DCV TOVS INTERFACE
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Doc No	S145 AP		Date	Tuesday, May 28, 2013
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SO DIMM Shielding



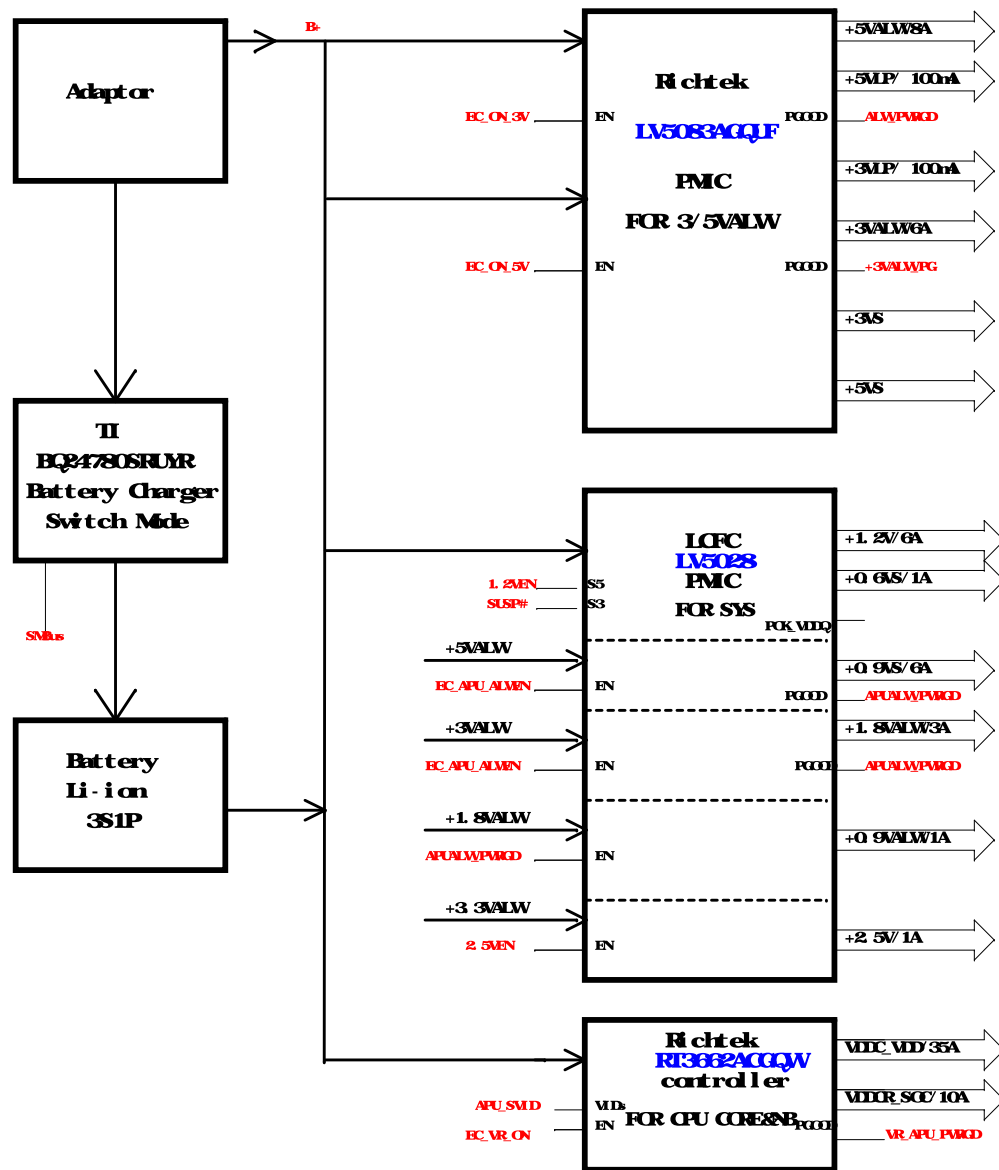
Memory Down Shielding

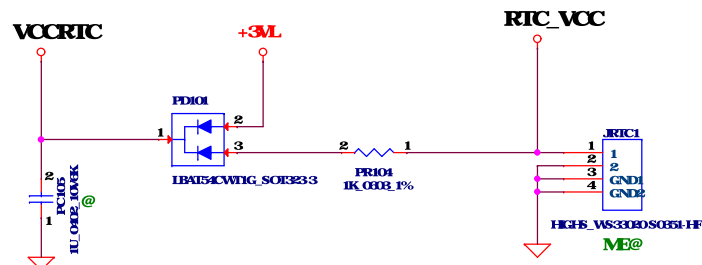
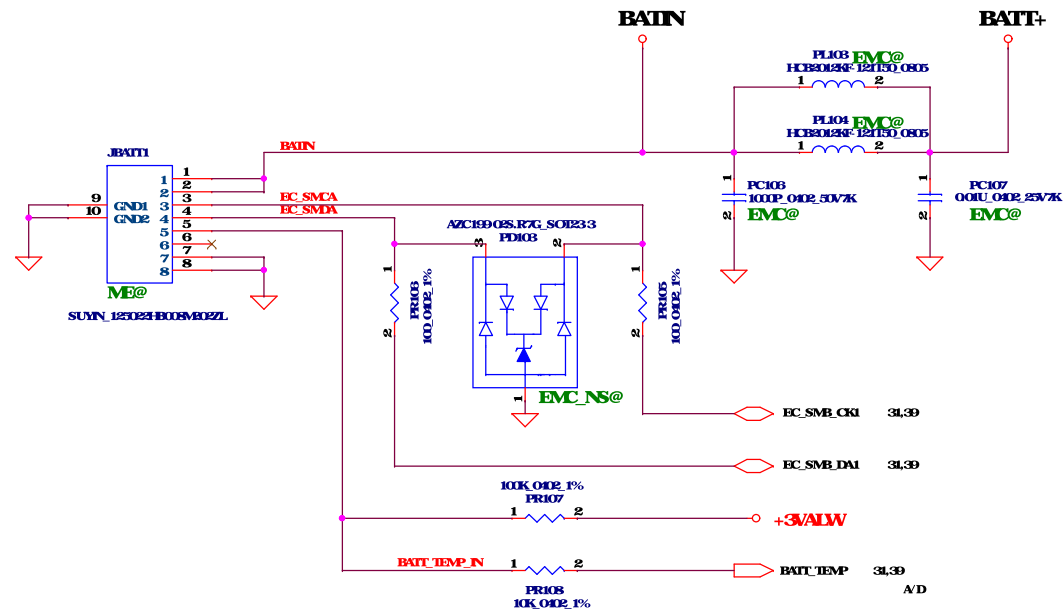
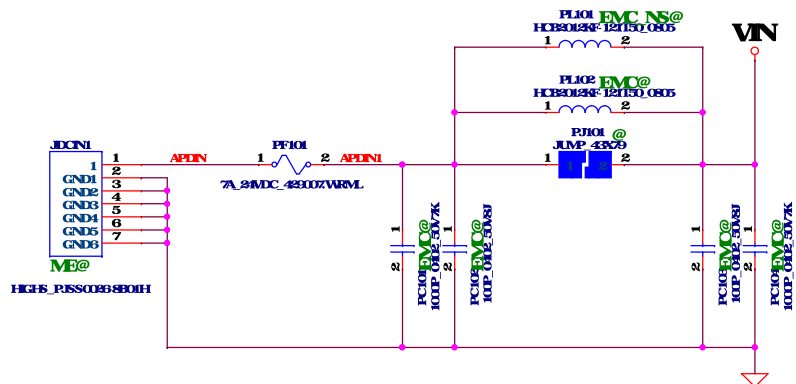


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				Date	Thursday May 28 2026
				Sheet	35 of 46



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				Custom		Date		Tuesday, May 25 2010		Sheet 36 of 44	

