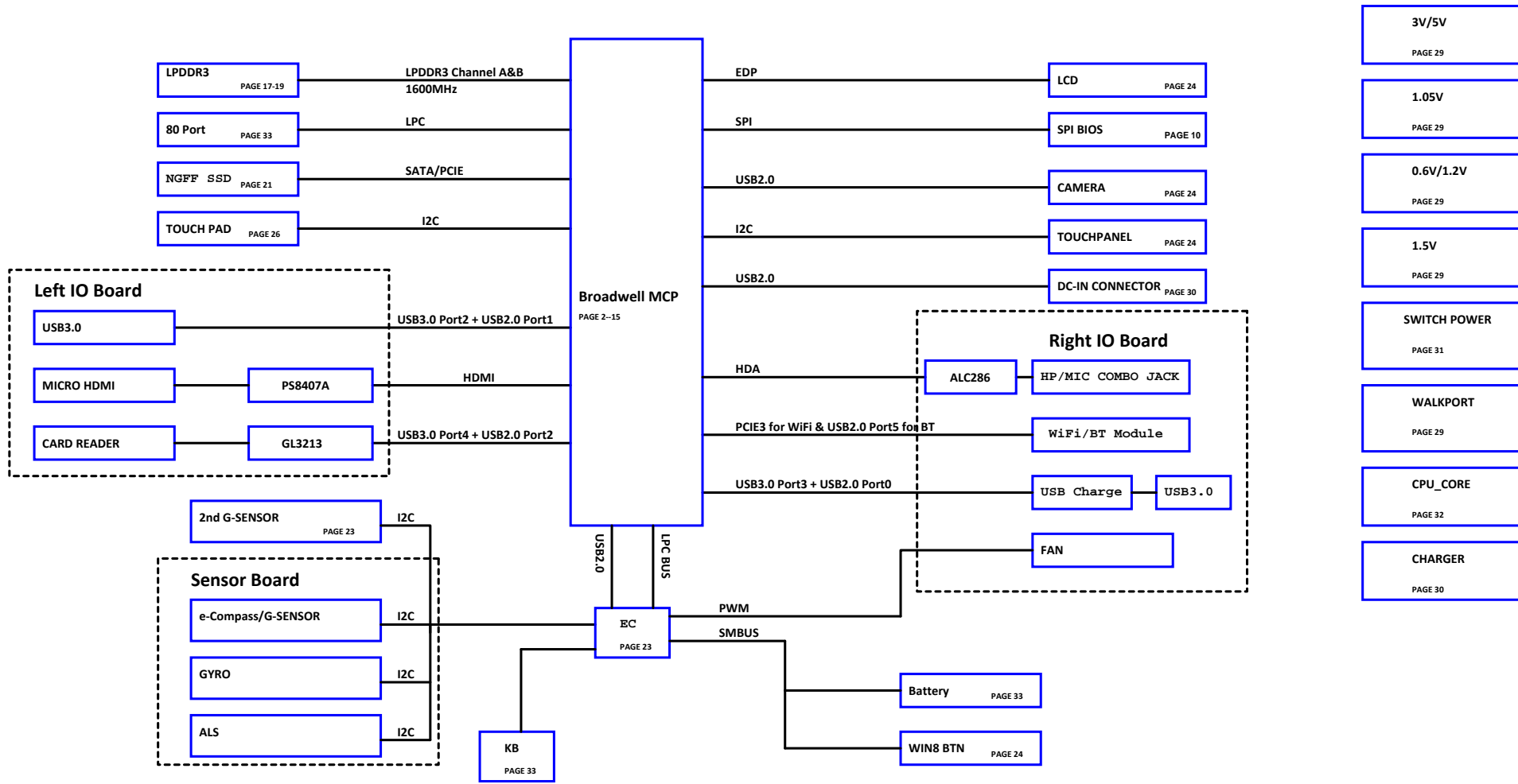
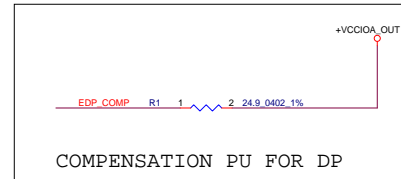
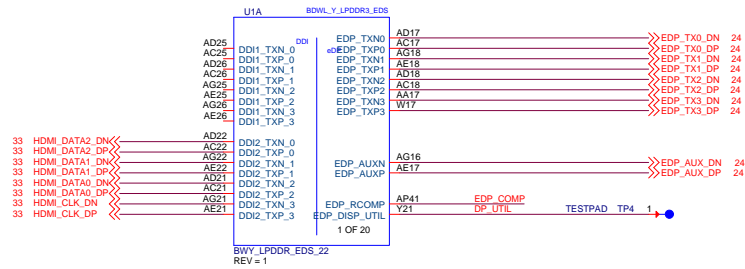


# BACH SVT Schematic Block Diagram



- 3V/5V  
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- 1.05V  
PAGE 29
- 0.6V/1.2V  
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- 1.5V  
PAGE 29
- SWITCH POWER  
PAGE 31
- WALKPORT  
PAGE 29
- CPU\_CORE  
PAGE 32
- CHARGER  
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17 M\_A\_DQ[63:0] <<>

M_A_DQ0	CT17	SA_DQ0
M_A_DQ1	CV17	SA_DQ1
M_A_DQ2	CN14	SA_DQ2
M_A_DQ3	CF15	SA_DQ3
M_A_DQ4	CN16	SA_DQ4
M_A_DQ5	CR16	SA_DQ5
M_A_DQ6	CN13	SA_DQ6
M_A_DQ7	CV15	SA_DQ7
M_A_DQ8	CT13	SA_DQ8
M_A_DQ9	CF13	SA_DQ9
M_A_DQ10	CP10	SA_DQ10
M_A_DQ11	CM10	SA_DQ11
M_A_DQ12	CN12	SA_DQ12
M_A_DQ13	CV13	SA_DQ13
M_A_DQ14	CV10	SA_DQ14
M_A_DQ15	CT10	SA_DQ15
M_A_DQ16	CT25	SA_DQ16
M_A_DQ17	CP25	SA_DQ17
M_A_DQ18	CF18	SA_DQ18
M_A_DQ19	CP23	SA_DQ19
M_A_DQ20	CN24	SA_DQ20
M_A_DQ21	CV25	SA_DQ21
M_A_DQ22	CV23	SA_DQ22
M_A_DQ23	CT23	SA_DQ23
M_A_DQ24	CN20	SA_DQ24
M_A_DQ25	CN18	SA_DQ25
M_A_DQ26	CT21	SA_DQ26
M_A_DQ27	CT19	SA_DQ27
M_A_DQ28	CP19	SA_DQ28
M_A_DQ29	CP21	SA_DQ29
M_A_DQ30	CV19	SA_DQ30
M_A_DQ31	CV21	SA_DQ31
M_A_DQ32	BU2	SA_DQ32
M_A_DQ33	BW2	SA_DQ33
M_A_DQ34	BW6	SA_DQ34
M_A_DQ35	BU4	SA_DQ35
M_A_DQ36	BW4	SA_DQ36
M_A_DQ37	BT3	SA_DQ37
M_A_DQ38	BU6	SA_DQ38
M_A_DQ39	BT5	SA_DQ39
M_A_DQ40	BN2	SA_DQ40
M_A_DQ41	BR2	SA_DQ41
M_A_DQ42	BN6	SA_DQ42
M_A_DQ43	BN4	SA_DQ43
M_A_DQ44	BR6	SA_DQ44
M_A_DQ45	BR4	SA_DQ45
M_A_DQ46	BN5	SA_DQ46
M_A_DQ47	BM3	SA_DQ47
M_A_DQ48	BT11	SA_DQ48
M_A_DQ49	BU10	SA_DQ49
M_A_DQ50	BW12	SA_DQ50
M_A_DQ51	BW10	SA_DQ51
M_A_DQ52	BR8	SA_DQ52
M_A_DQ53	BU8	SA_DQ53
M_A_DQ54	BU2	SA_DQ54
M_A_DQ55	BT9	SA_DQ55
M_A_DQ56	BN8	SA_DQ56
M_A_DQ57	BR8	SA_DQ57
M_A_DQ58	BN12	SA_DQ58
M_A_DQ59	BN10	SA_DQ59
M_A_DQ60	BR12	SA_DQ60
M_A_DQ61	BR10	SA_DQ61
M_A_DQ62	BM11	SA_DQ62
M_A_DQ63	BM9	SA_DQ63

3 OF 20  
BWY\_LPDDR\_EDS\_22  
REV = 1

UID

CG4	M_A_CLK_DDR0_DN	17,19
CG2	M_A_CLK_DDR0_DP	17,19
CC4	M_A_CLK_DDR1_DN	17,19
CC6	M_A_CLK_DDR1_DP	17,19
CH11	M_A_CKE0	17,19
CH9	M_A_CKE1	17,19
CA12	M_A_CKE2	17,19
CA10	M_A_CKE3	17,19
CA4	M_A_CS0_N	17,19
CA2	M_A_CS1_N	17,19
CA6	M_A_ODT0	17,19
CE2	M_A_CAB3	17,19
CE4	M_A_CAB2	17,19
CC8	M_A_CAB1	17,19
CB5	M_A_CAB4	17,19
CC2	M_A_CAB6	17,19
CF11	M_A_CAA5	17,19
CE8	M_A_CAB9	17,19
CE12	M_A_CAB8	17,19
CF5	M_A_CAB5	17,19
CE10	M_A_CAB8	17,19
CG6	M_A_CAA0	17,19
CH3	M_A_CAA2	17,19
CE8	M_A_CAA4	17,19
CB9	M_A_CAA3	17,19
CC12	M_A_CAA1	17,19
CF3	M_A_CAB7	17,19
CG12	M_A_CAA7	17,19
CH5	M_A_CAA6	17,19
CB3	M_A_CAB0	17,19
CF9	M_A_CAA9	17,19
CG10	M_A_CAA8	17,19
CU16	M_A_DQS_DN0	
CR12	M_A_DQS_DN1	
CR24	M_A_DQS_DN2	
CR20	M_A_DQS_DN3	
BU3	M_A_DQS_DN4	
BP3	M_A_DQS_DN5	
BU9	M_A_DQS_DN6	
BP9	M_A_DQS_DN7	
CT15	M_A_DQS_DP0	
CU12	M_A_DQS_DP1	
CU24	M_A_DQS_DP2	
CU20	M_A_DQS_DP3	
BU5	M_A_DQS_DP4	
BP5	M_A_DQS_DP5	
BU11	M_A_DQS_DP6	
BP11	M_A_DQS_DP7	
AP13	+V_DDR_CA_VREF	19
AU14	+V_DDR_VREF000	19
AT13	+V_DDR_VREFD01	19
CC14	+V_DDR_VREFD01	19

3 OF 20  
BWY\_LPDDR\_EDS\_22  
REV = 1

18 M\_B\_DQ[63:0] <<>

M_B_DQ0	BK3	SB_DQ0
M_B_DQ1	BK6	SB_DQ1
M_B_DQ2	BG6	SB_DQ2
M_B_DQ3	BG9	SB_DQ3
M_B_DQ4	BJ4	SB_DQ4
M_B_DQ5	B36	SB_DQ5
M_B_DQ6	BG9	SB_DQ6
M_B_DQ7	BG4	SB_DQ7
M_B_DQ8	BF3	SB_DQ8
M_B_DQ9	BF5	SB_DQ9
M_B_DQ10	BC6	SB_DQ10
M_B_DQ11	BE2	SB_DQ11
M_B_DQ12	BE4	SB_DQ12
M_B_DQ13	BE6	SB_DQ13
M_B_DQ14	BC2	SB_DQ14
M_B_DQ15	BC4	SB_DQ15
M_B_DQ16	BE10	SB_DQ16
M_B_DQ17	BC10	SB_DQ17
M_B_DQ18	BE8	SB_DQ18
M_B_DQ19	BC8	SB_DQ19
M_B_DQ20	BF11	SB_DQ20
M_B_DQ21	BC12	SB_DQ21
M_B_DQ22	BE12	SB_DQ22
M_B_DQ23	BF9	SB_DQ23
M_B_DQ24	BJ12	SB_DQ24
M_B_DQ25	BG12	SB_DQ25
M_B_DQ26	B38	SB_DQ26
M_B_DQ27	BJ10	SB_DQ27
M_B_DQ28	BG8	SB_DQ28
M_B_DQ29	BG10	SB_DQ29
M_B_DQ30	BK9	SB_DQ30
M_B_DQ31	BK11	SB_DQ31
M_B_DQ32	AM1	SB_DQ32
M_B_DQ33	AH2	SB_DQ33
M_B_DQ34	AJ3	SB_DQ34
M_B_DQ35	AM6	SB_DQ35
M_B_DQ36	AM3	SB_DQ36
M_B_DQ37	AJ1	SB_DQ37
M_B_DQ38	AJ5	SB_DQ38
M_B_DQ39	AH4	SB_DQ39
M_B_DQ40	AG3	SB_DQ40
M_B_DQ41	AG1	SB_DQ41
M_B_DQ42	AD2	SB_DQ42
M_B_DQ43	AE3	SB_DQ43
M_B_DQ44	AE11	SB_DQ44
M_B_DQ45	AG5	SB_DQ45
M_B_DQ46	AD4	SB_DQ46
M_B_DQ47	AES	SB_DQ47
M_B_DQ48	AM9	SB_DQ48
M_B_DQ49	AM7	SB_DQ49
M_B_DQ50	AH8	SB_DQ50
M_B_DQ51	AJ9	SB_DQ51
M_B_DQ52	AM11	SB_DQ52
M_B_DQ53	AJ7	SB_DQ53
M_B_DQ54	AJ11	SB_DQ54
M_B_DQ55	AH10	SB_DQ55
M_B_DQ56	AE11	SB_DQ56
M_B_DQ57	AG7	SB_DQ57
M_B_DQ58	AE7	SB_DQ58
M_B_DQ59	AE9	SB_DQ59
M_B_DQ60	AG11	SB_DQ60
M_B_DQ61	AD8	SB_DQ61
M_B_DQ62	AD6	SB_DQ62
M_B_DQ63	AD10	SB_DQ63

4 OF 20  
BWY\_LPDDR\_EDS\_22  
REV = 1

UID

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BK6	M_B_DQ1	SB_DQ1
BG6	M_B_DQ2	SB_DQ2
BG9	M_B_DQ3	SB_DQ3
BJ4	M_B_DQ4	SB_DQ4
B36	M_B_DQ5	SB_DQ5
BG9	M_B_DQ6	SB_DQ6
BG4	M_B_DQ7	SB_DQ7
BF3	M_B_DQ8	SB_DQ8
BF5	M_B_DQ9	SB_DQ9
BC6	M_B_DQ10	SB_DQ10
BE2	M_B_DQ11	SB_DQ11
BE4	M_B_DQ12	SB_DQ12
BE6	M_B_DQ13	SB_DQ13
BC2	M_B_DQ14	SB_DQ14
BC4	M_B_DQ15	SB_DQ15
BE10	M_B_DQ16	SB_DQ16
BC10	M_B_DQ17	SB_DQ17
BE8	M_B_DQ18	SB_DQ18
BC8	M_B_DQ19	SB_DQ19
BF11	M_B_DQ20	SB_DQ20
BC12	M_B_DQ21	SB_DQ21
BE12	M_B_DQ22	SB_DQ22
BF9	M_B_DQ23	SB_DQ23
BJ12	M_B_DQ24	SB_DQ24
BG12	M_B_DQ25	SB_DQ25
B38	M_B_DQ26	SB_DQ26
BJ10	M_B_DQ27	SB_DQ27
BG8	M_B_DQ28	SB_DQ28
BG10	M_B_DQ29	SB_DQ29
BK9	M_B_DQ30	SB_DQ30
BK11	M_B_DQ31	SB_DQ31
AM1	M_B_DQ32	SB_DQ32
AH2	M_B_DQ33	SB_DQ33
AJ3	M_B_DQ34	SB_DQ34
AM6	M_B_DQ35	SB_DQ35
AM3	M_B_DQ36	SB_DQ36
AJ1	M_B_DQ37	SB_DQ37
AJ5	M_B_DQ38	SB_DQ38
AH4	M_B_DQ39	SB_DQ39
AG3	M_B_DQ40	SB_DQ40
AG1	M_B_DQ41	SB_DQ41
AD2	M_B_DQ42	SB_DQ42
AE3	M_B_DQ43	SB_DQ43
AE11	M_B_DQ44	SB_DQ44
AG5	M_B_DQ45	SB_DQ45
AD4	M_B_DQ46	SB_DQ46
AES	M_B_DQ47	SB_DQ47
AM9	M_B_DQ48	SB_DQ48
AM7	M_B_DQ49	SB_DQ49
AH8	M_B_DQ50	SB_DQ50
AJ9	M_B_DQ51	SB_DQ51
AM11	M_B_DQ52	SB_DQ52
AJ7	M_B_DQ53	SB_DQ53
AJ11	M_B_DQ54	SB_DQ54
AH10	M_B_DQ55	SB_DQ55
AE11	M_B_DQ56	SB_DQ56
AG7	M_B_DQ57	SB_DQ57
AE7	M_B_DQ58	SB_DQ58
AE9	M_B_DQ59	SB_DQ59
AG11	M_B_DQ60	SB_DQ60
AD8	M_B_DQ61	SB_DQ61
AD6	M_B_DQ62	SB_DQ62
AD10	M_B_DQ63	SB_DQ63

4 OF 20  
BWY\_LPDDR\_EDS\_22  
REV = 1

BDWL\_Y\_LPDDR\_EDS

AW6	M_B_CLK_DDR0_DN	18,19
AP11	M_B_CLK_DDR0_DP	18,19
AP9	M_B_CLK_DDR1_DN	18,19
BA4	M_B_CLK_DDR1_DP	18,19
BA2	M_B_CKE0	18,19
AR8	M_B_CKE1	18,19
AP5	M_B_CKE2	18,19
AR10	M_B_CS0_N	18,19
AT11	M_B_CS1_N	18,19
AO10	M_B_ODT0	18,19
BA10	M_B_CAB3	18,19
AW12	M_B_CAB2	18,19
AW10	M_B_CAB1	18,19
AY11	M_B_CAB4	18,19
BA12	M_B_CAB6	18,19
AU2	M_B_CAA5	18,19
AT9	M_B_CAB9	18,19
AR4	M_B_CAB8	18,19
AU8	M_B_CAB5	18,19
AT5	M_B_CAB5	18,19
AT3	M_B_CAA0	18,19
BA8	M_B_CAA2	18,19
AV3	M_B_CAA4	18,19
AW2	M_B_CAA3	18,19
AV5	M_B_CAA1	18,19
AY9	M_B_CAA7	18,19
AU4	M_B_CAA6	18,19
AU6	M_B_CAB0	18,19
AW8	M_B_CAA9	18,19
BA6	M_B_CAA8	18,19
AR2	M_B_CAA8	18,19
BH5	M_B_DQS_DN0	
BD5	M_B_DQS_DN1	
BD11	M_B_DQS_DN2	
BH11	M_B_DQS_DN3	
AK2	M_B_DQS_DN4	
AF2	M_B_DQS_DN5	
AK8	M_B_DQS_DN6	
AF8	M_B_DQS_DN7	
BH3	M_B_DQS_DP0	
BD3	M_B_DQS_DP1	
BD9	M_B_DQS_DP2	
BH9	M_B_DQS_DP3	
AK4	M_B_DQS_DP4	
AF4	M_B_DQS_DP5	
AK10	M_B_DQS_DP6	
AF10	M_B_DQS_DP7	

4 OF 20  
BWY\_LPDDR\_EDS\_22  
REV = 1

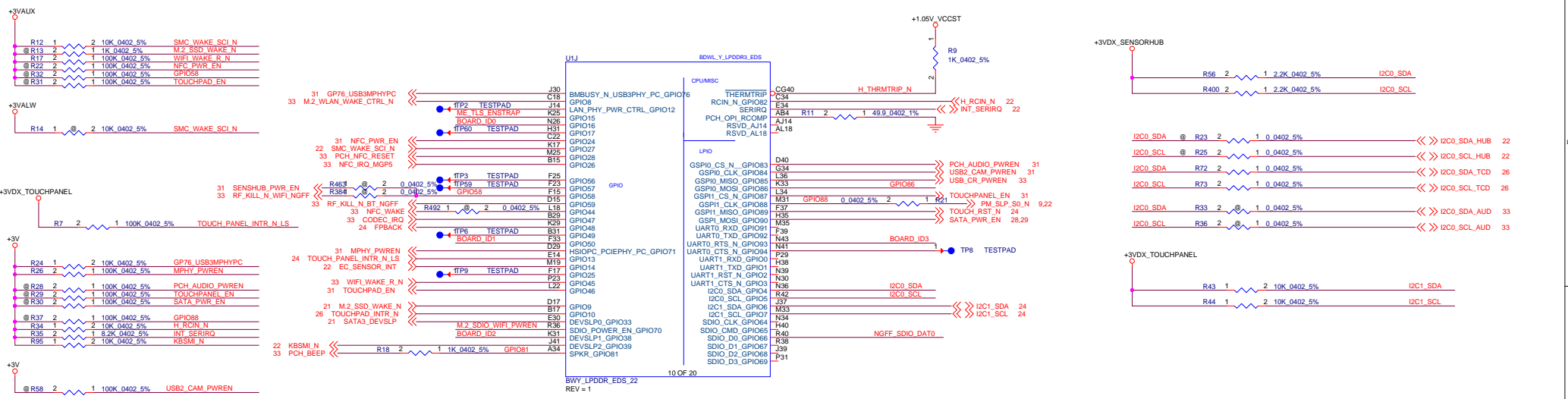
**lenovo** 联想 LENOVO.CRDN

Title: BROADWELL MCP ( PROCESSOR LPDDR3)

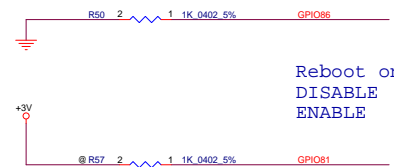
Size C Document Number: BDW CRESENT BAY Rev V1.0

Date: Monday, July 21, 2014 Sheet 3 of 37

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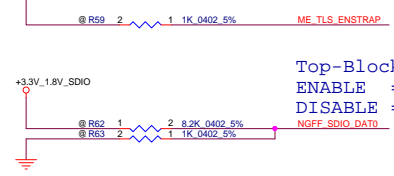


Boot BIOS Strap Bit  
 SPI(PCH) = PD (Default)  
 LPC(EC) = PU

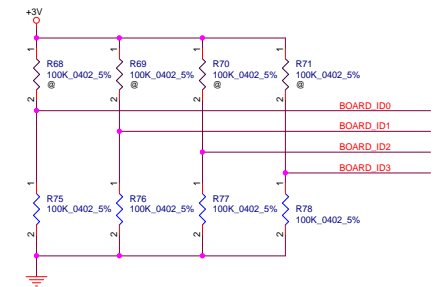
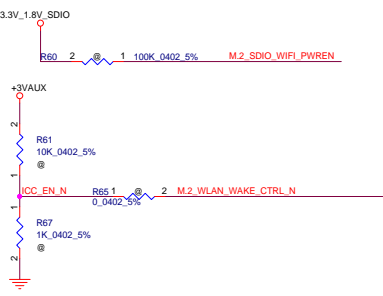


Reboot on TCO Timer expiration  
 DISABLE = PU  
 ENABLE = PD (Default)

TLS CONFIDENTIALITY STRAP  
 ENABLE = PU  
 DISABLE = PD (Default)



Top-Block Swap Override  
 ENABLE = PU  
 DISABLE = PD (Default)



BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0	Description
0	0	0	0	Samsung 8G
1	0	0	0	Hynix 8G
1	1	0	0	Hynix 4G
0	0	1	0	Elpida 8G
1	0	1	0	Samsung 4G
0	1	1	0	Elpida 4G

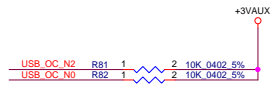
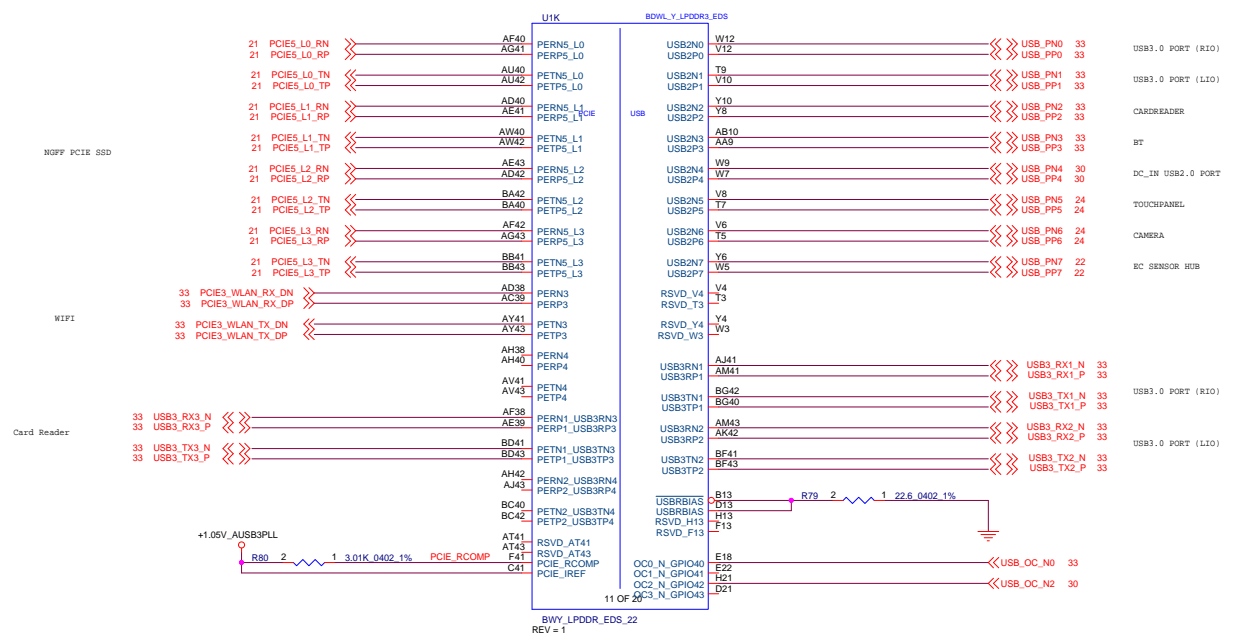
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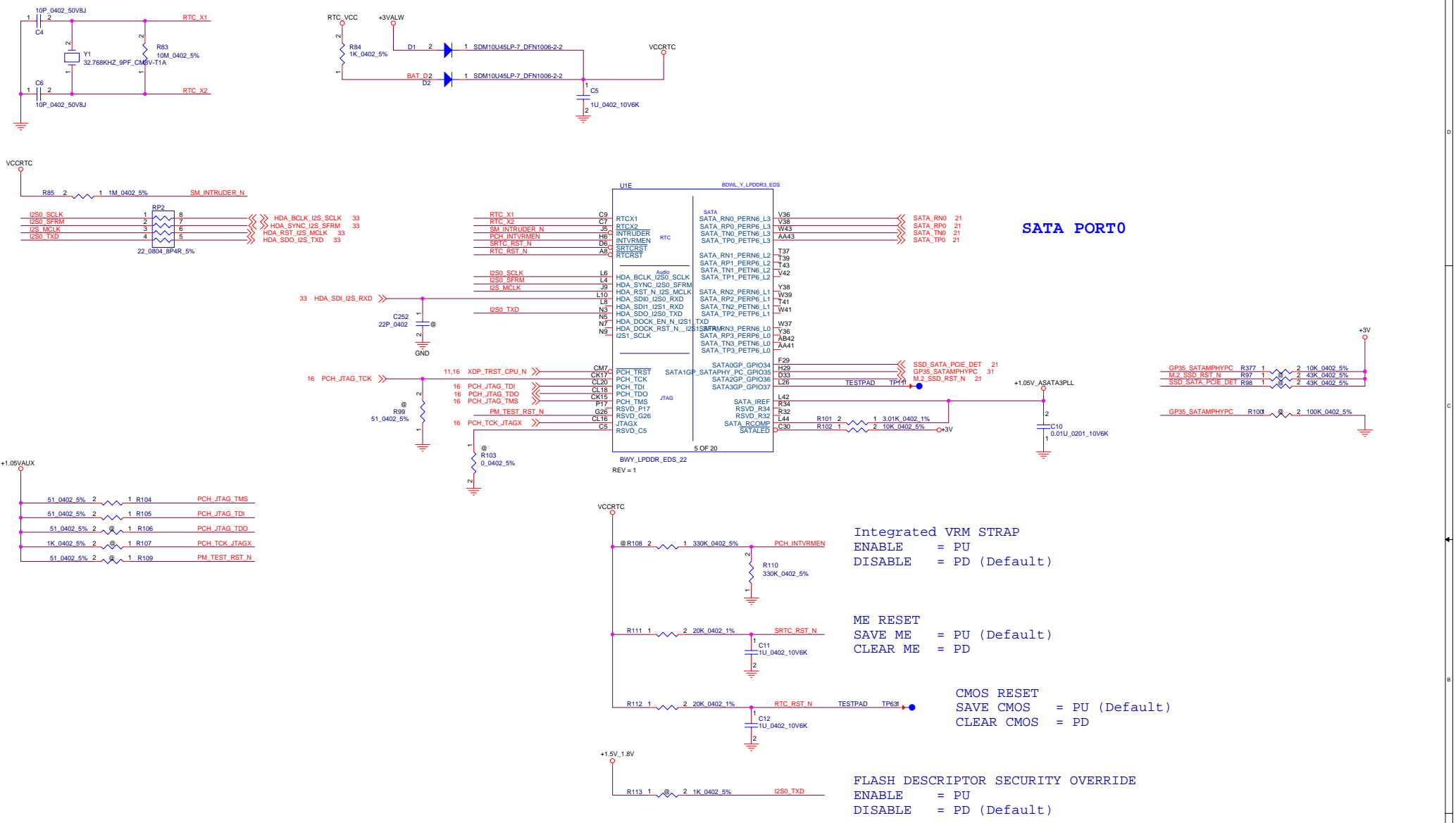
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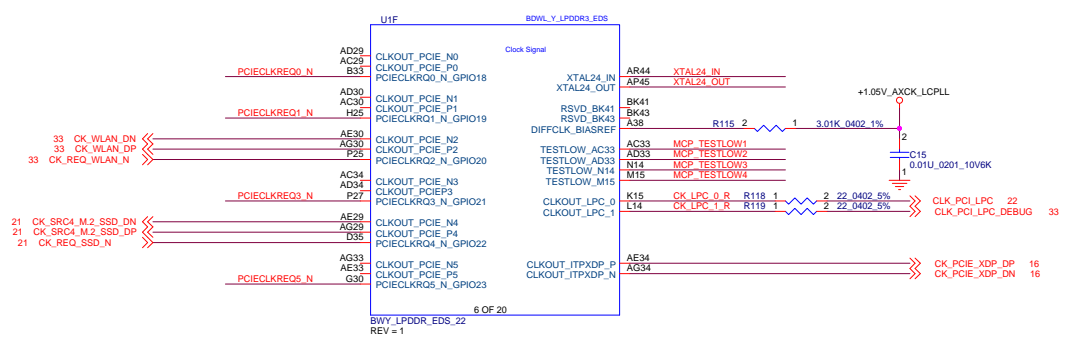
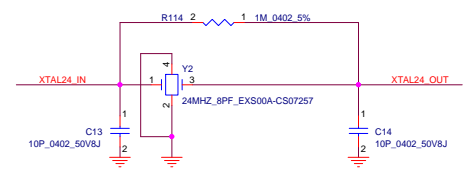
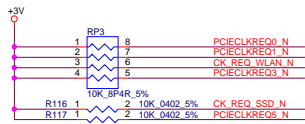
Size C Document Number: BDW CRESENT BAY Rev V1.0

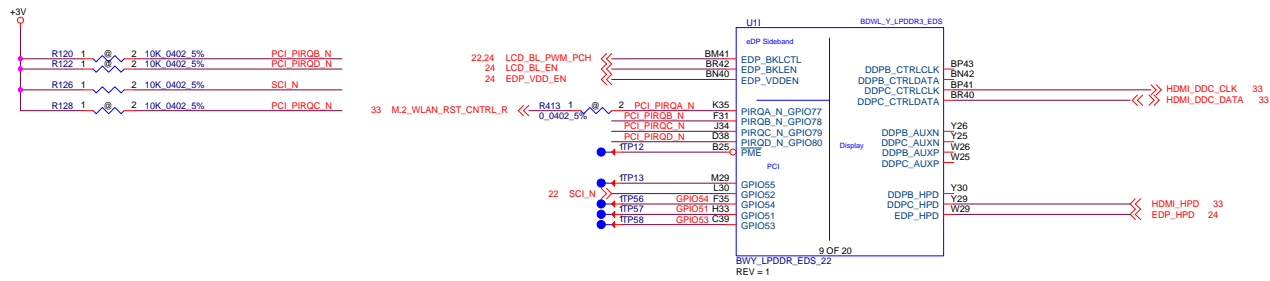
Date: Monday, July 21, 2014 Sheet 4 of 37

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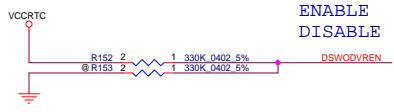
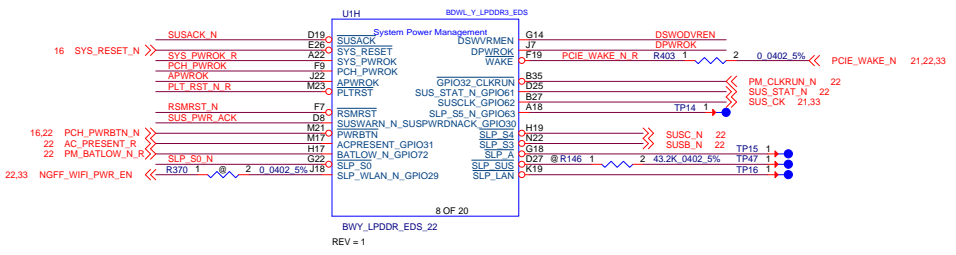
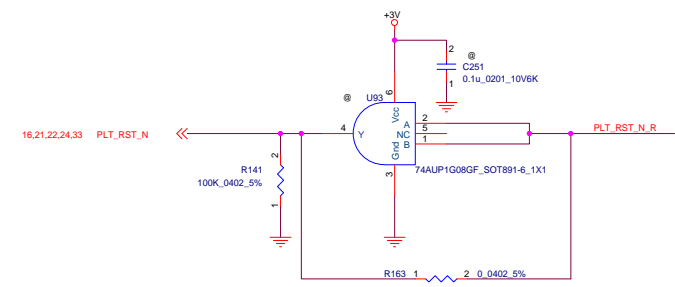
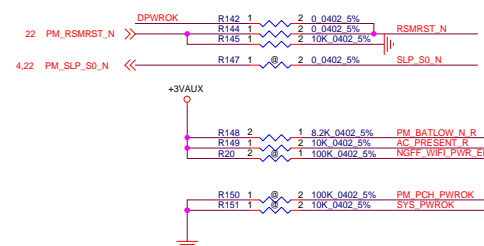
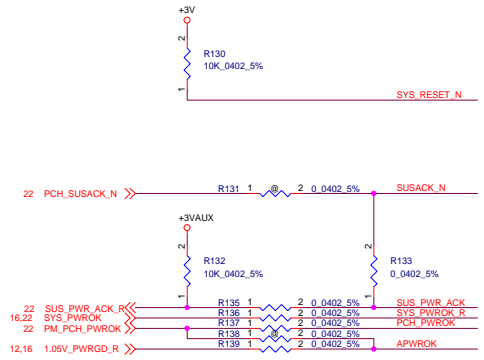




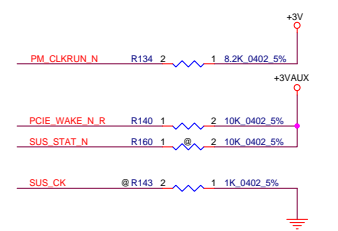


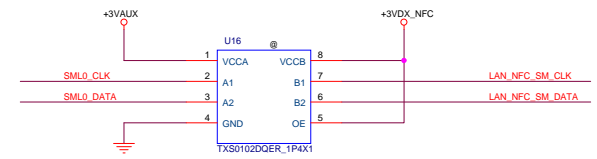
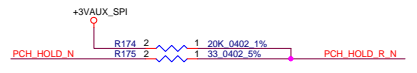
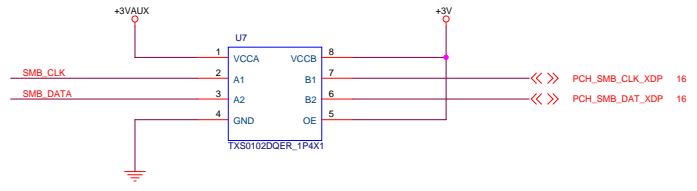
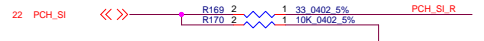
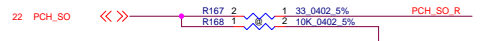
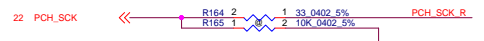
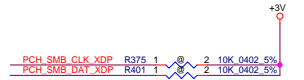
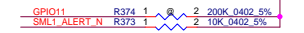
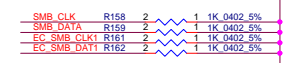
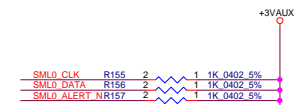
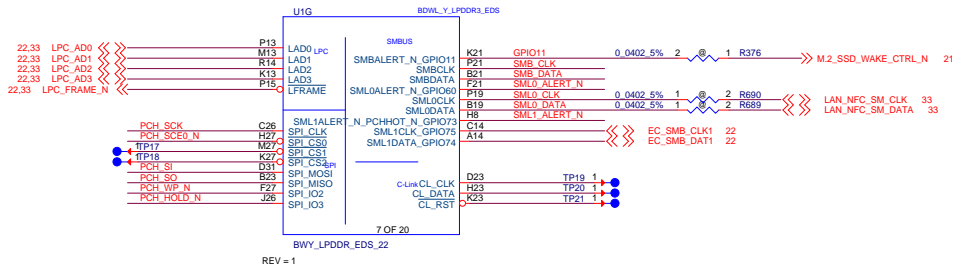
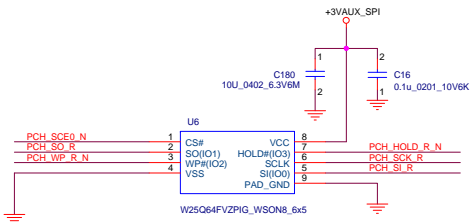
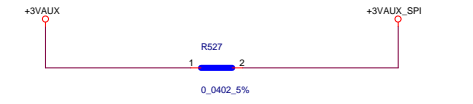





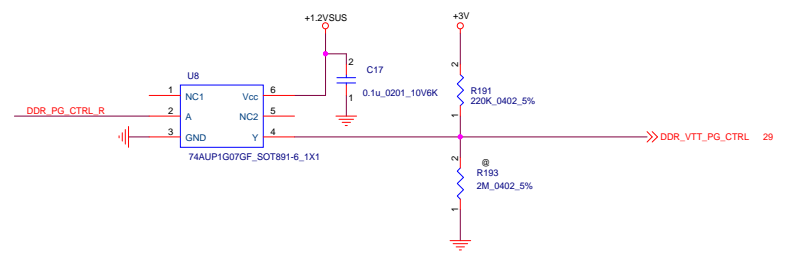
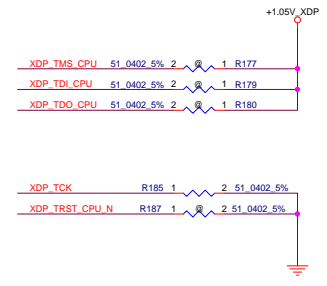
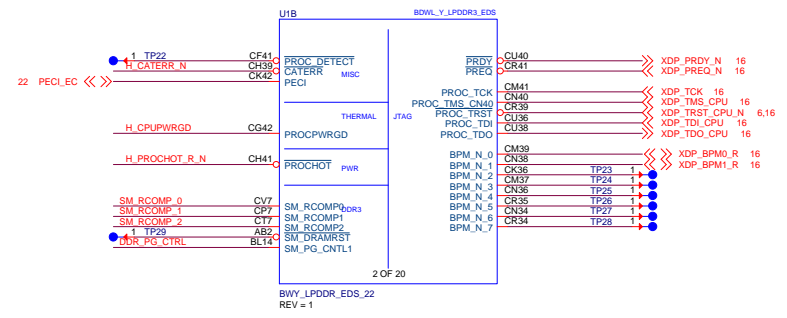
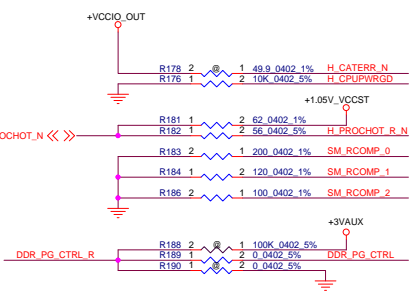


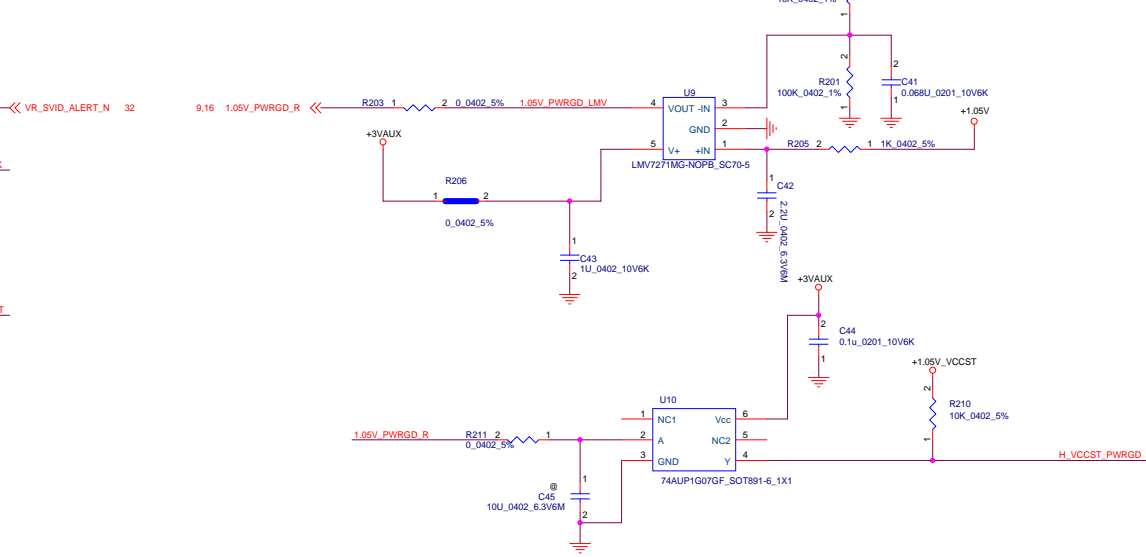
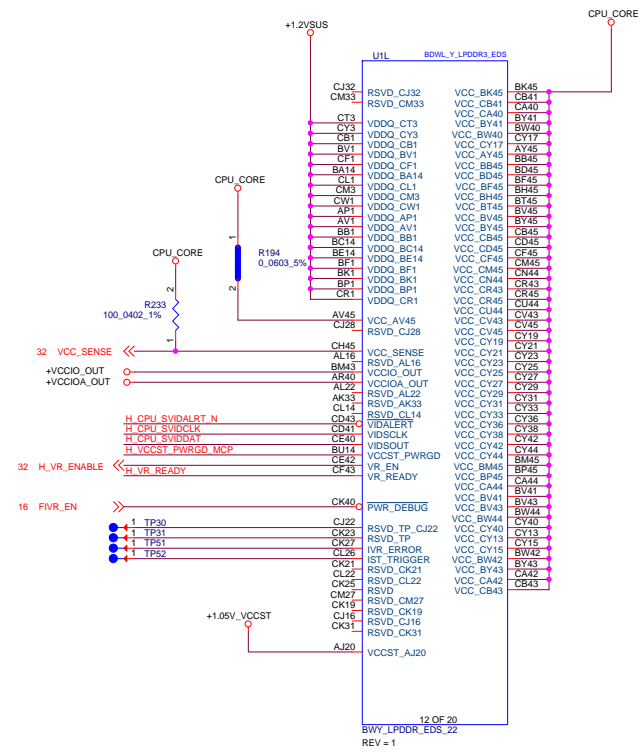
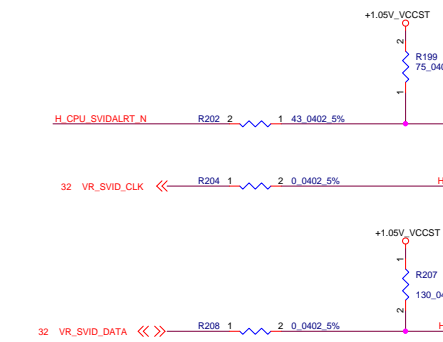
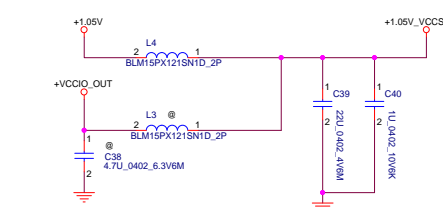
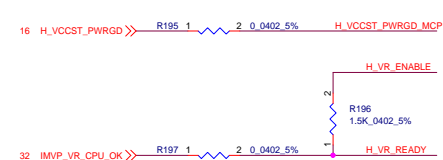
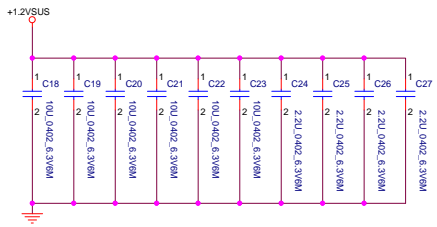
ON DIE DSW VR ENABLE  
 ENABLE = PU (Default)  
 DISABLE = PD



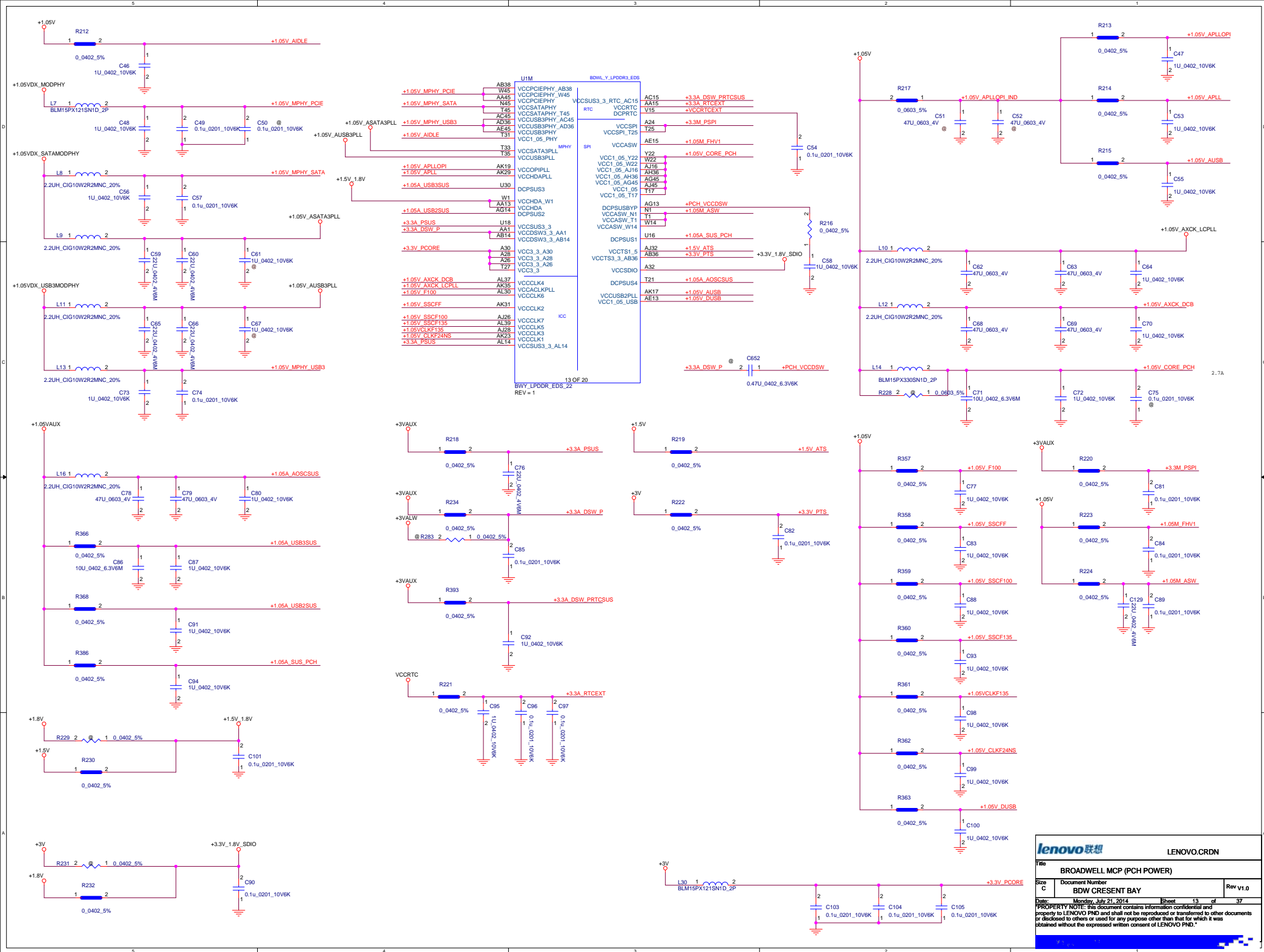



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 Title: **BROADWELL MCP (LPC SPI SMB CLINK)**  
 Size C Document Number: **BDW CRESENT BAY** Rev V1.0  
 Date: **Monday, July 21, 2014** Sheet 10 of 37  
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**BROADWELL MCP (PROCESSOR POWER)**  
**BDW CRESENT BAY**  
 Rev V1.0  
 Monday, July 21, 2014  
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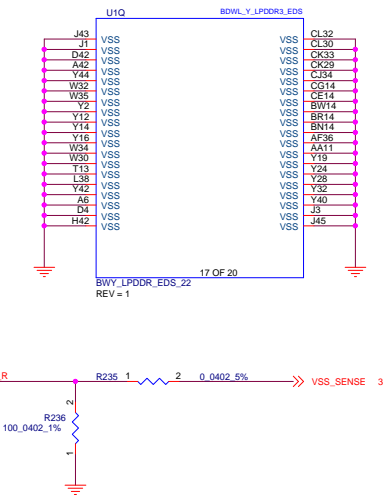
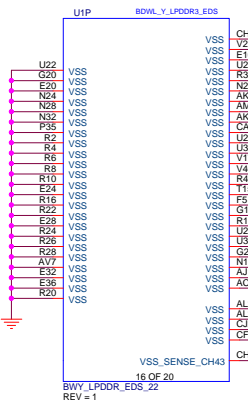
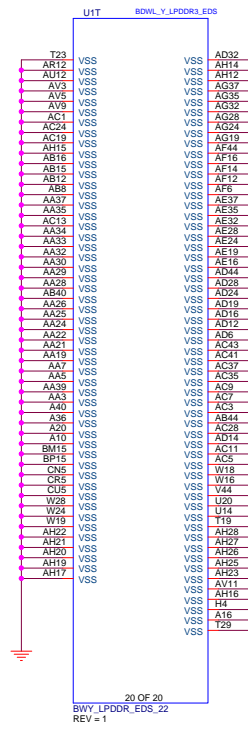
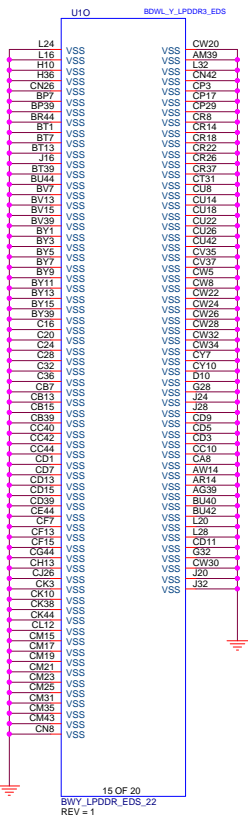
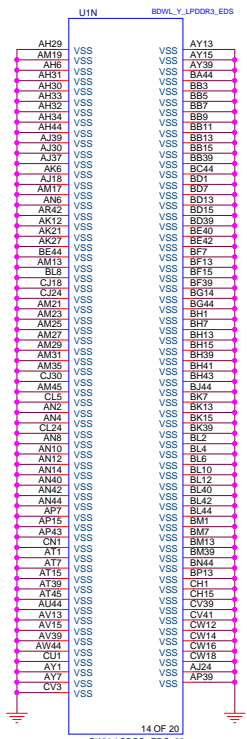
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Title: BROADWELL MCP (PCH POWER)

Size C Document Number: BDW CRESENT BAY Rev V1.0

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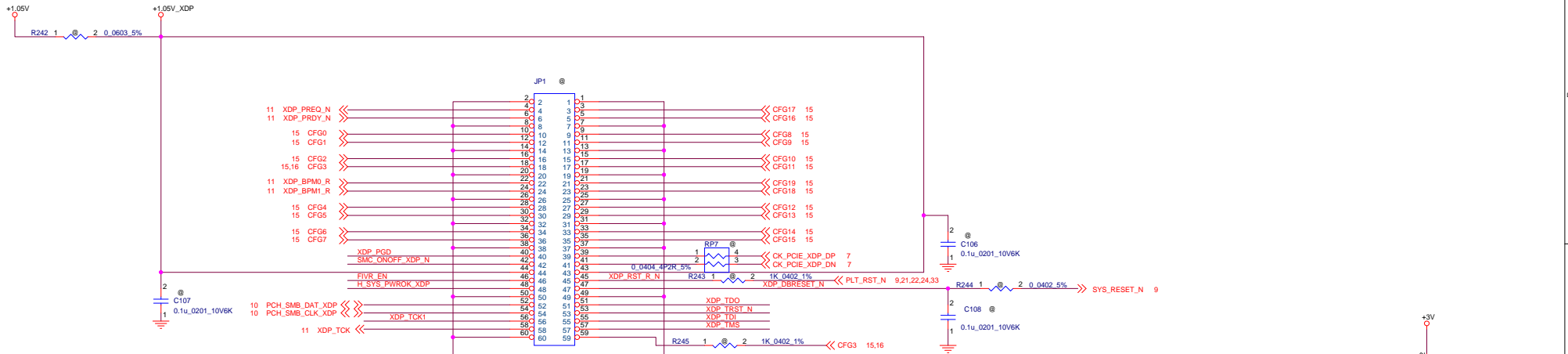
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Size C Document Number: BDW CRESENT BAY Rev V1.0

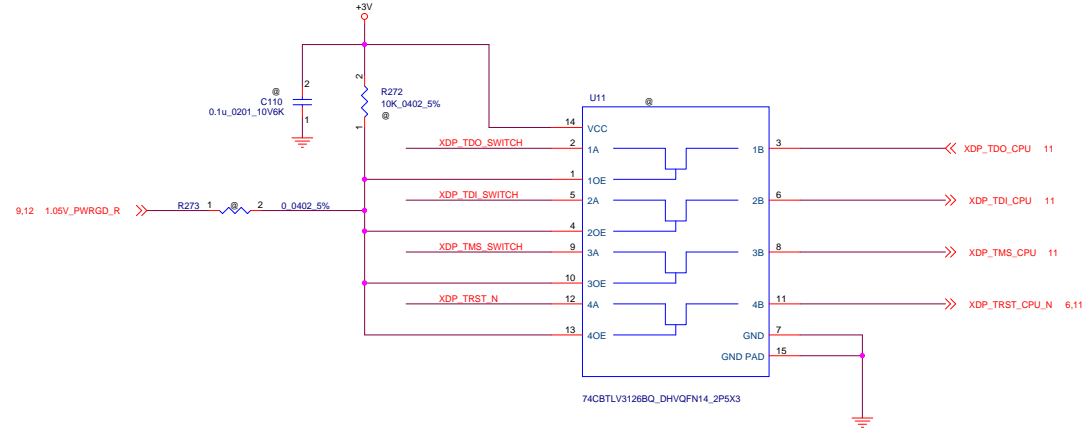
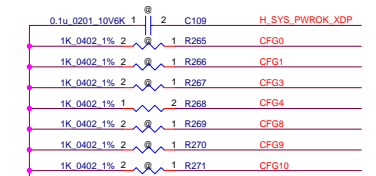
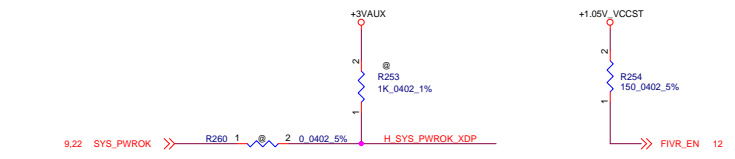
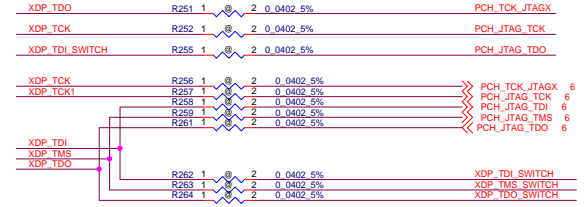
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JTAG Mode  
 DUAL TCKS = STUFFED R258, R259, R261, R262, R263, R264 (DEFAULT)  
 UNSTUFFED R251, R252, R255  
 SINGLE TCK = STUFFED R251, R252, R255  
 UNSTUFFED R258, R259, R261, R262, R263, R264



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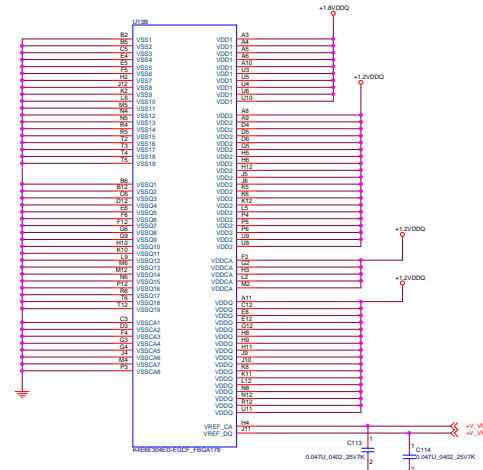
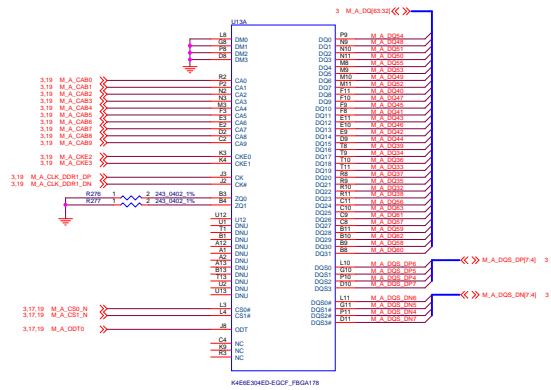
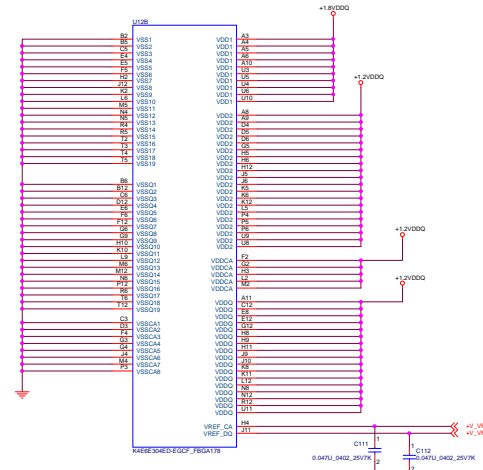
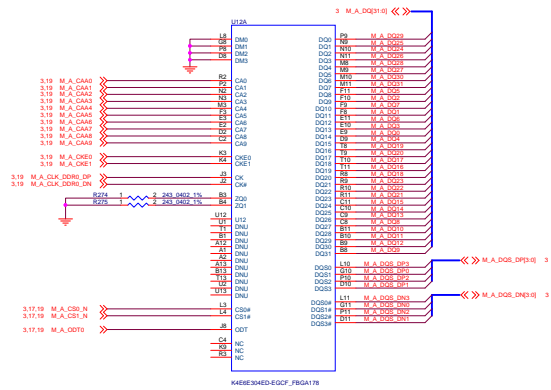
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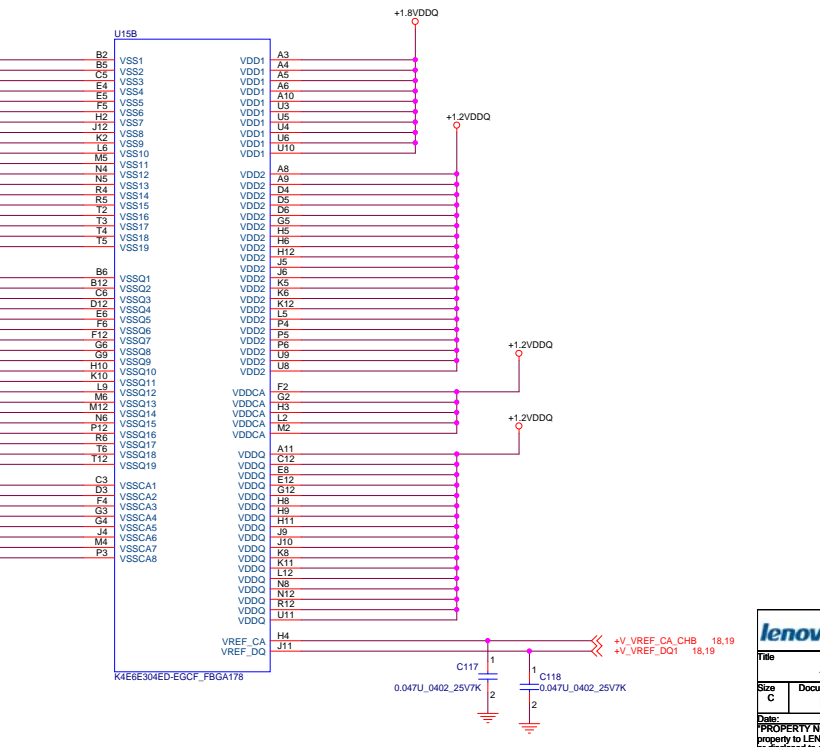
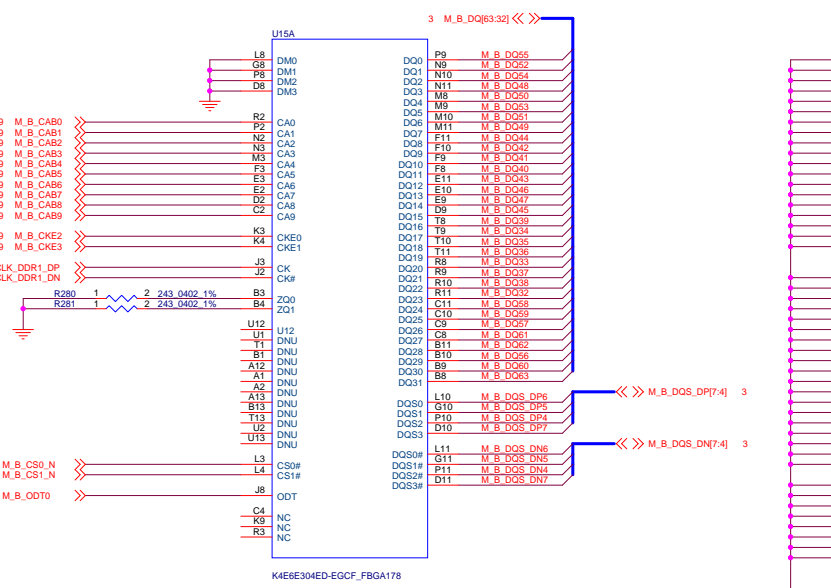
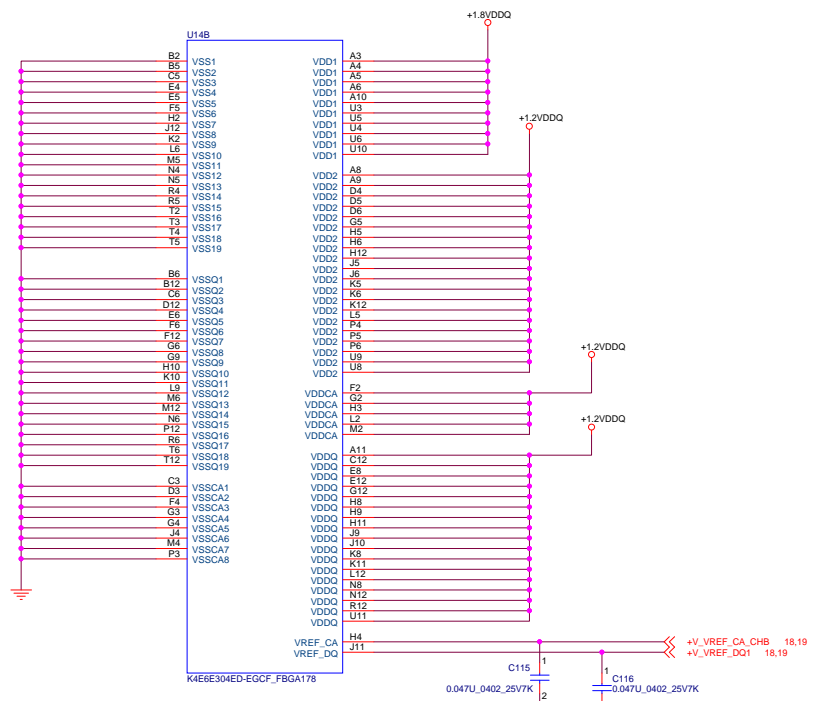
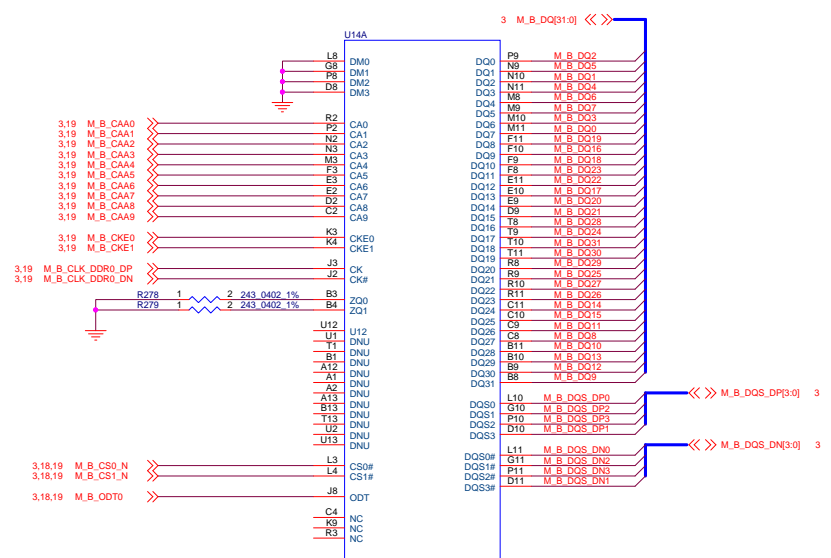
Size C Document Number BDW CRESENT BAY Rev V1.0

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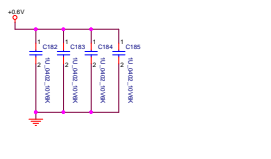
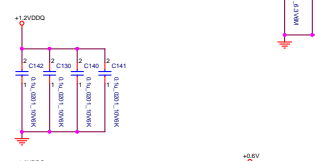
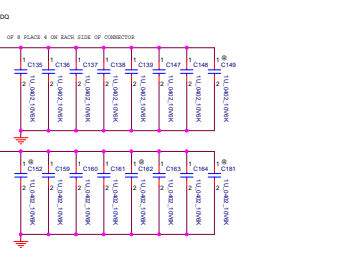
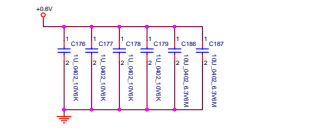
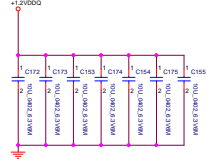
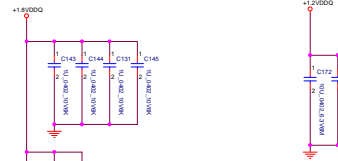
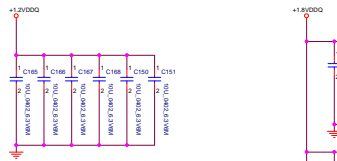
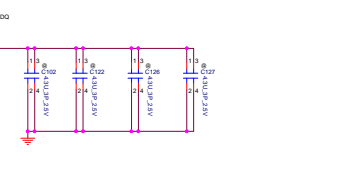
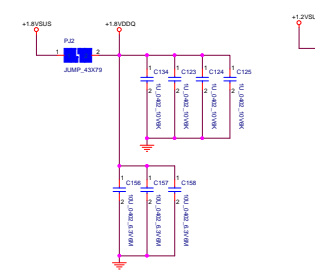
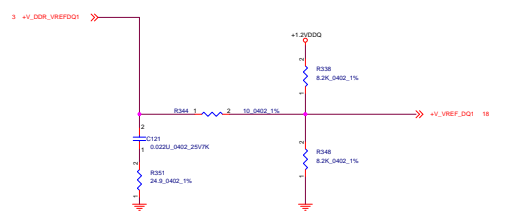
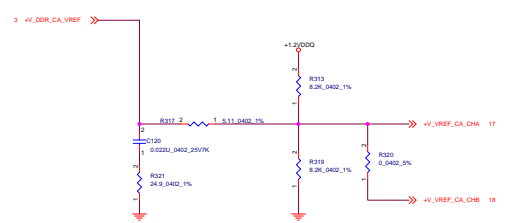
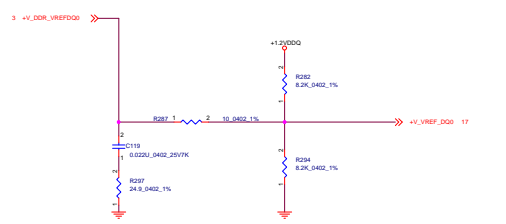
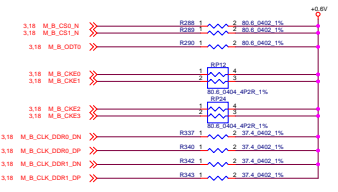
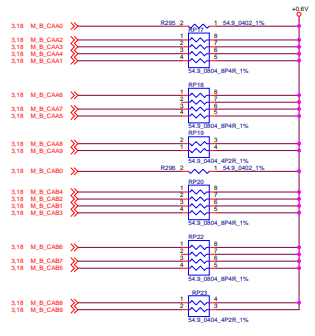
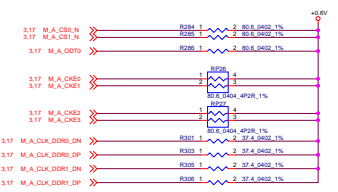
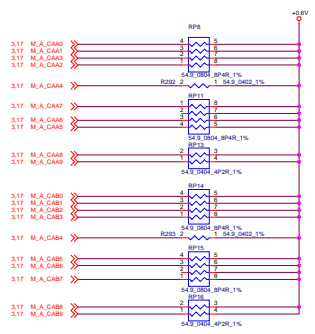
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Title: **AUDIO DSP**

Size: **C** Document Number: **BDW CRESENT BAY** Rev: **V1.0**

Date: **Monday, July 21, 2014** Sheet: **18** of **37**

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		LENOVO.CRDN	
Title			
AUDIO CODEC			
Size	Document Number	Rev	
C	BDW CRESENT BAY	V1.0	
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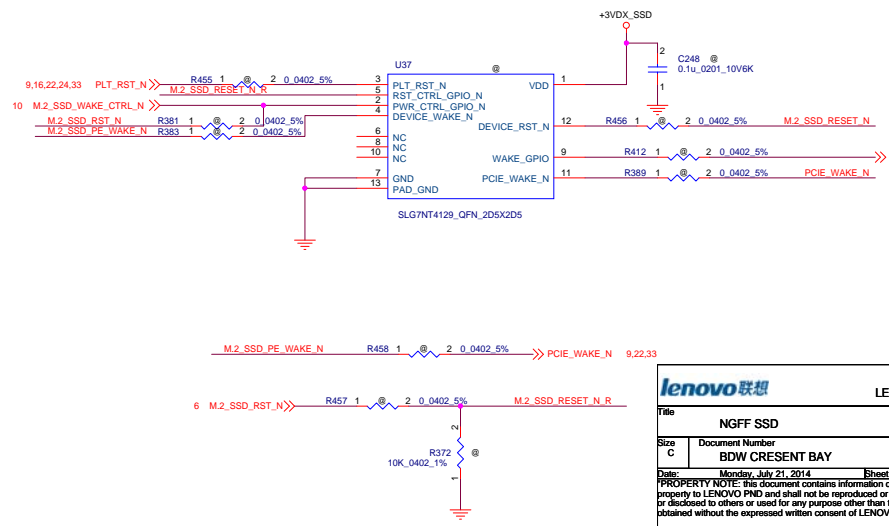
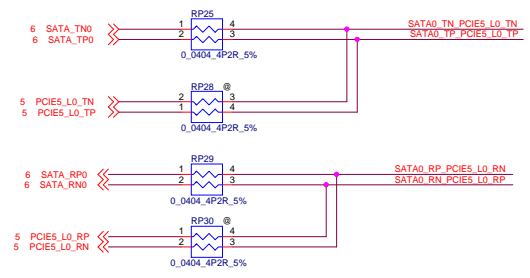
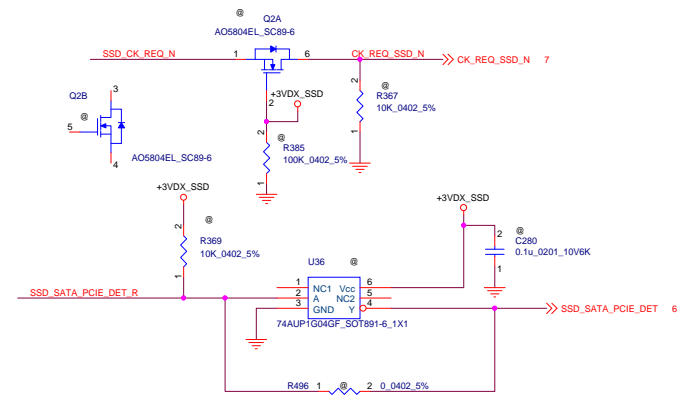
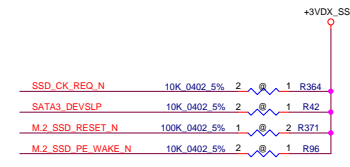
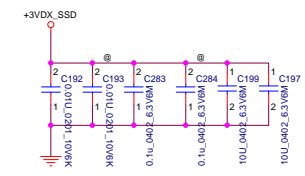
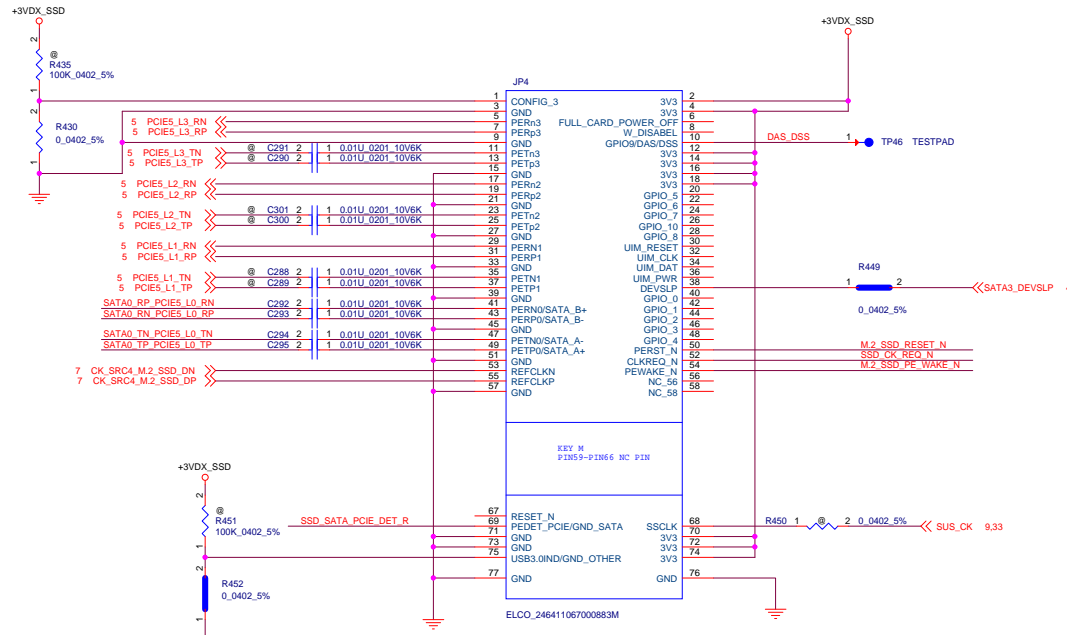
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**LENOVO.CRDN**

**Title**  
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**Size**  
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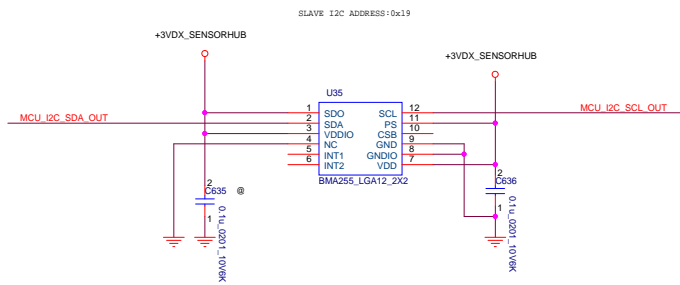
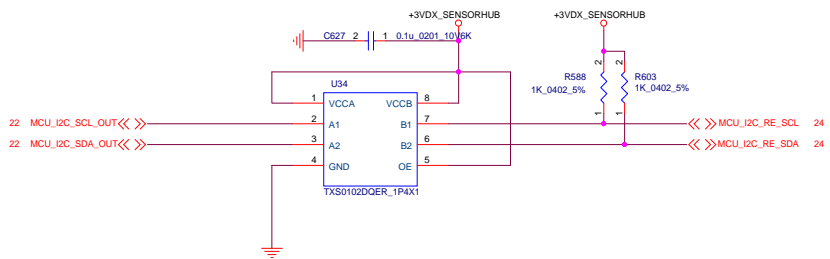
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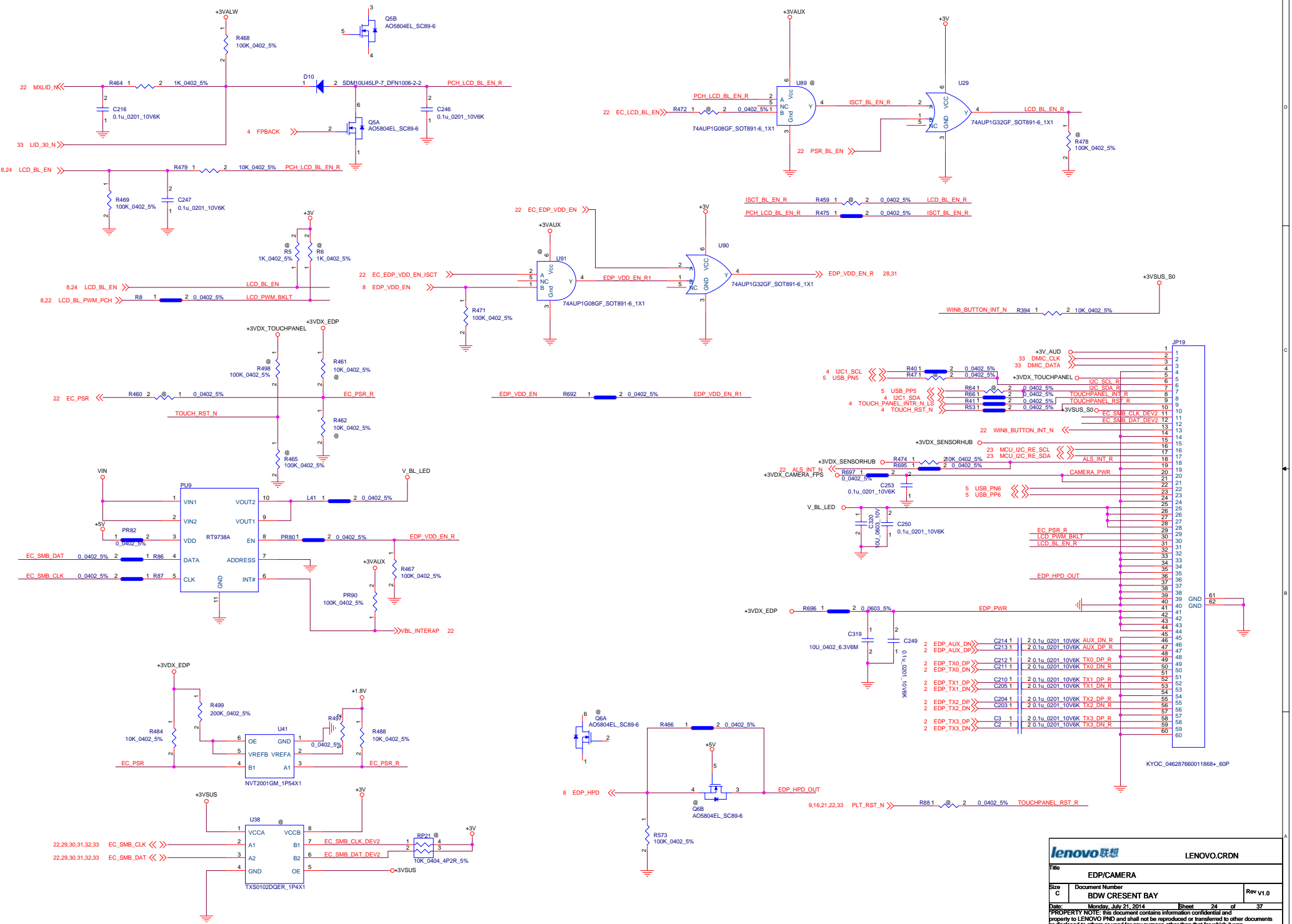
**Rev**  
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**Date:** Monday, July 21, 2014 **Sheet** 21 **of** 37

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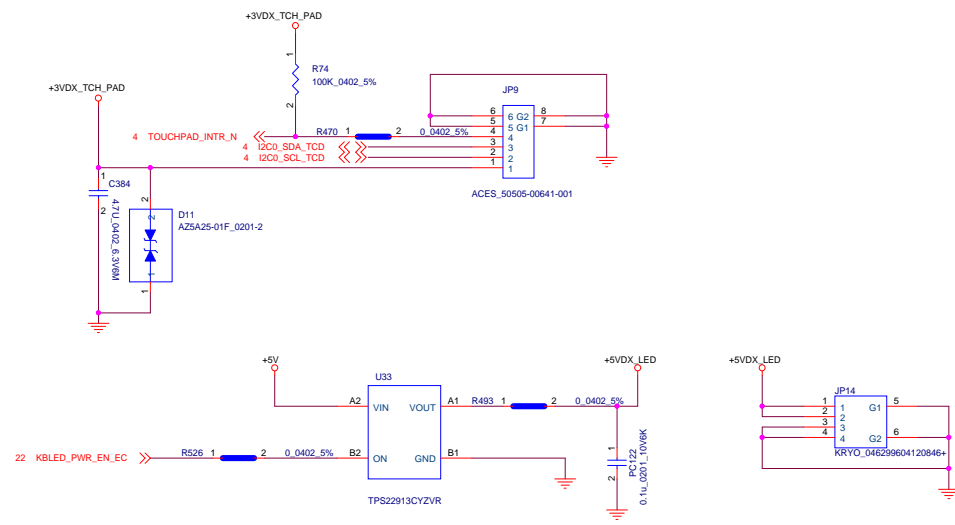
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Size	Document Number	Rev	
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		LENOVO.CRDN	
Title			
PWR LED CONN			
Size	Document Number	Rev	
C	BDW CRESNET BAY	V1.0	
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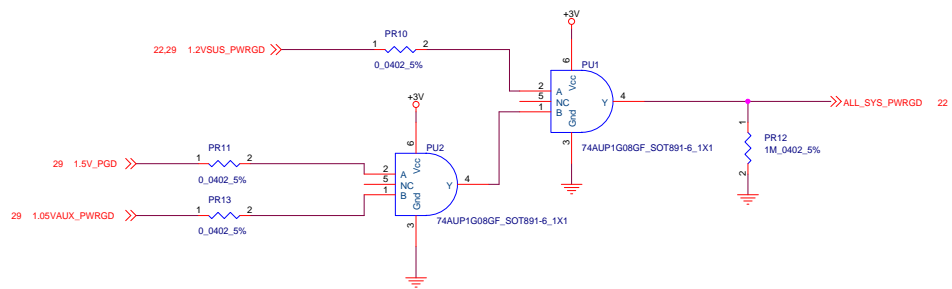
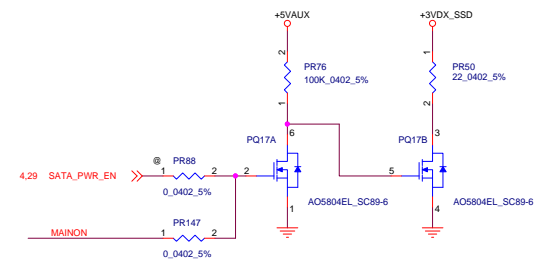
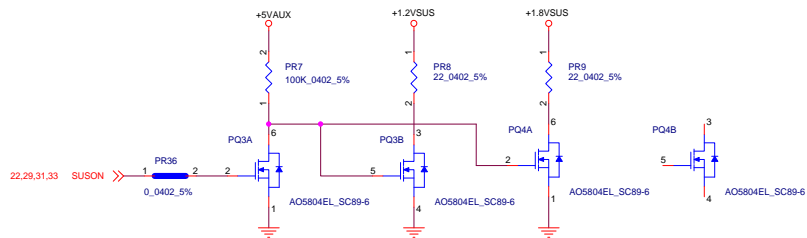
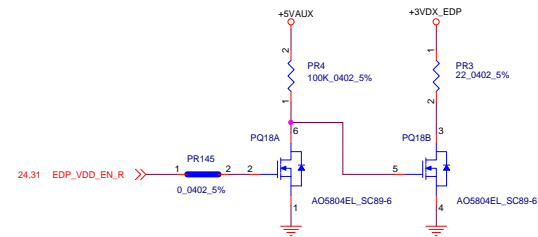
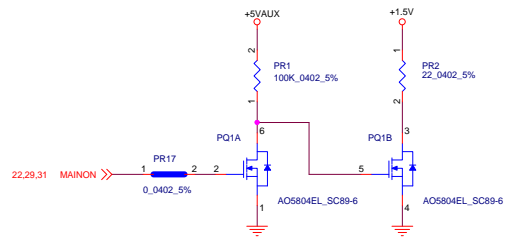
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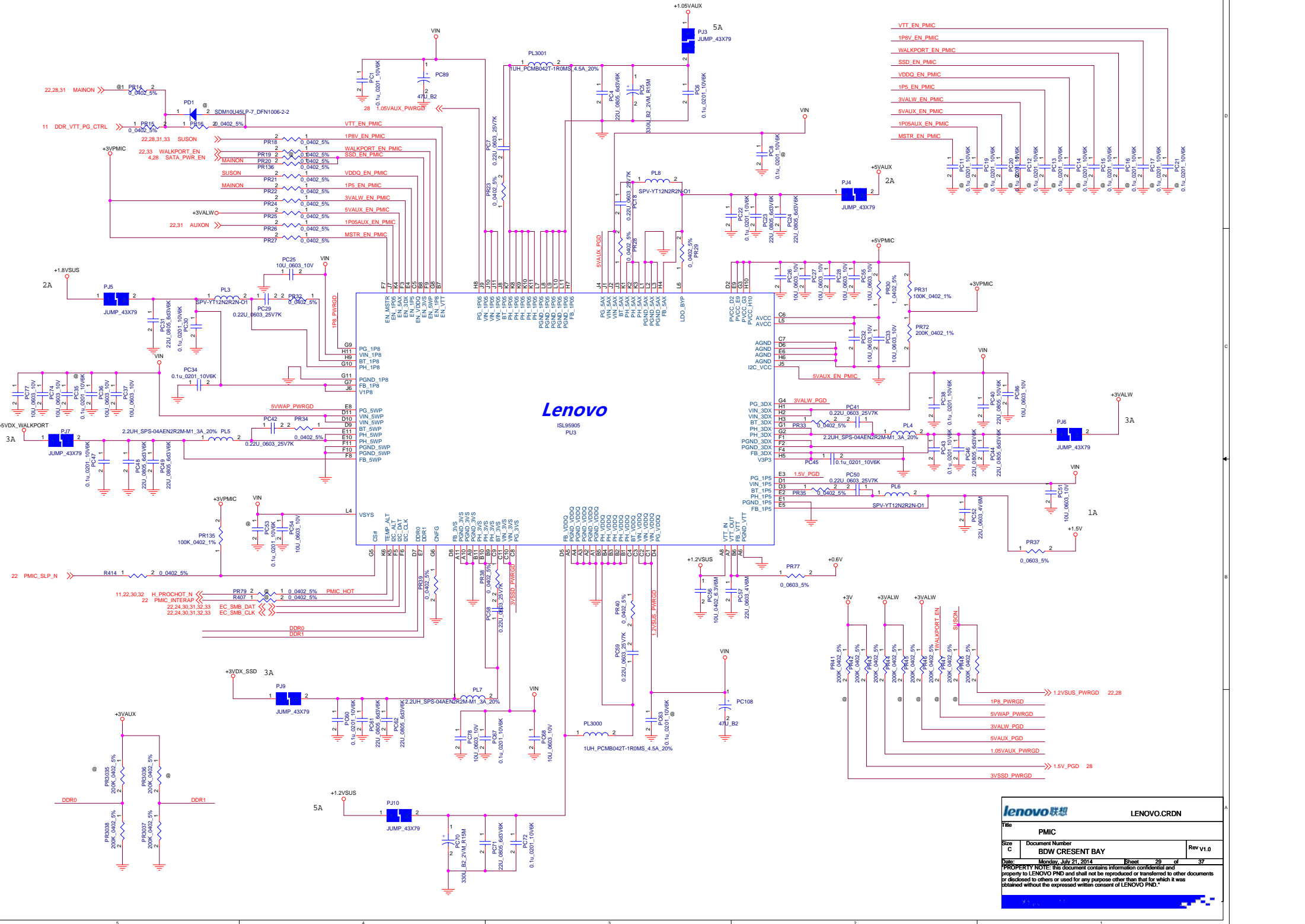
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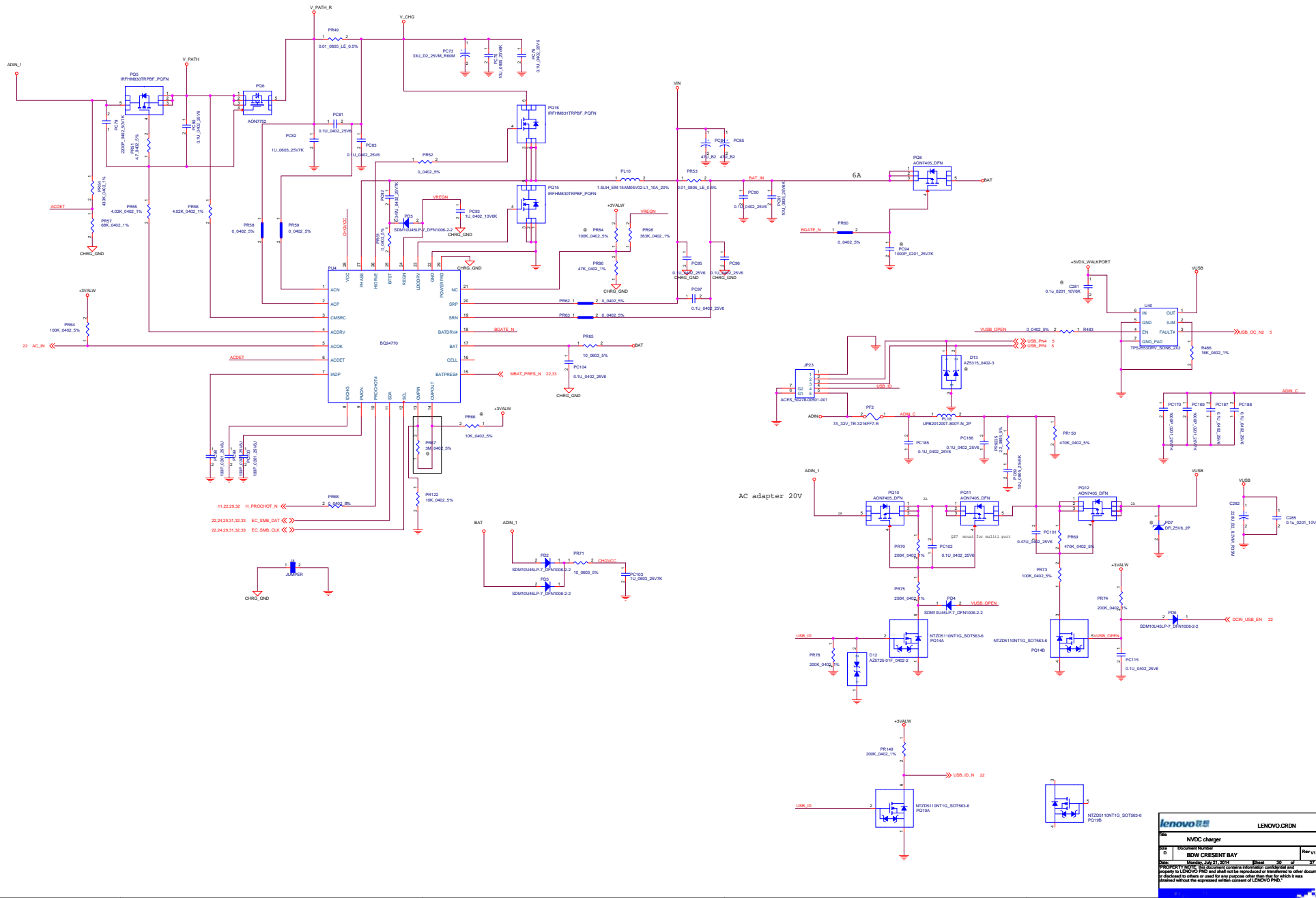


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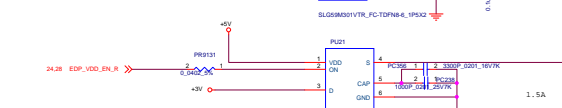
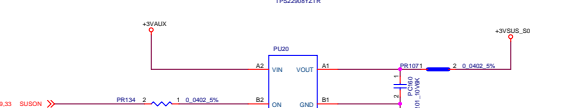
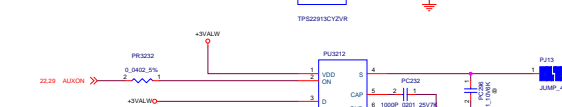
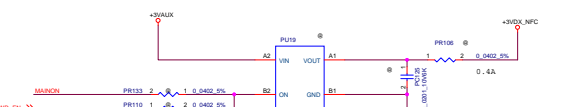
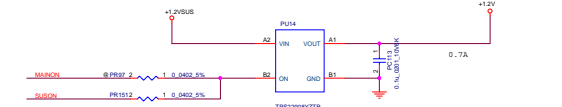
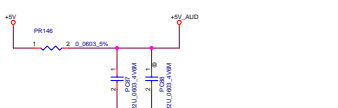
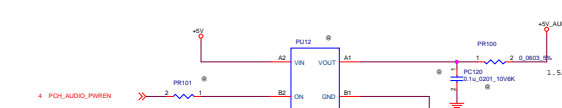
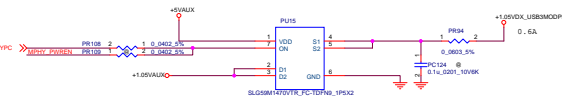
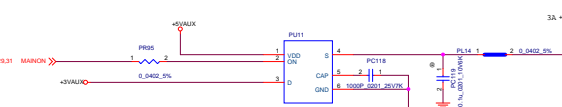
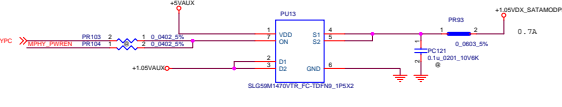
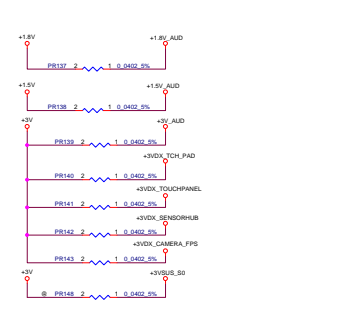
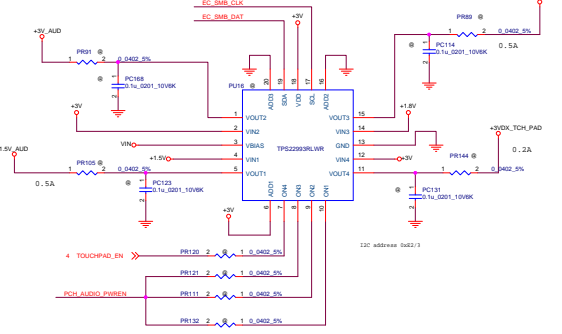
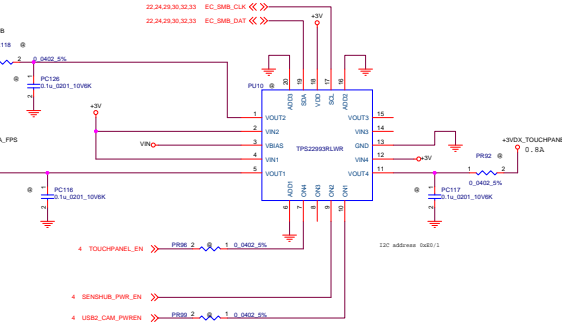
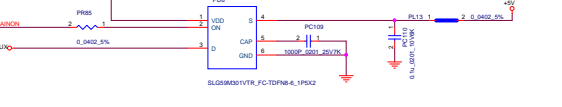
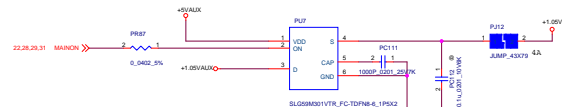
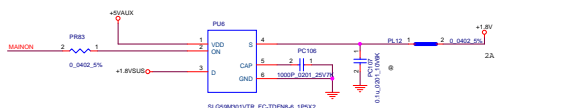
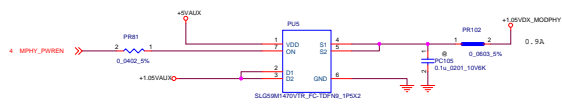
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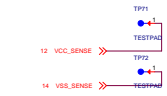
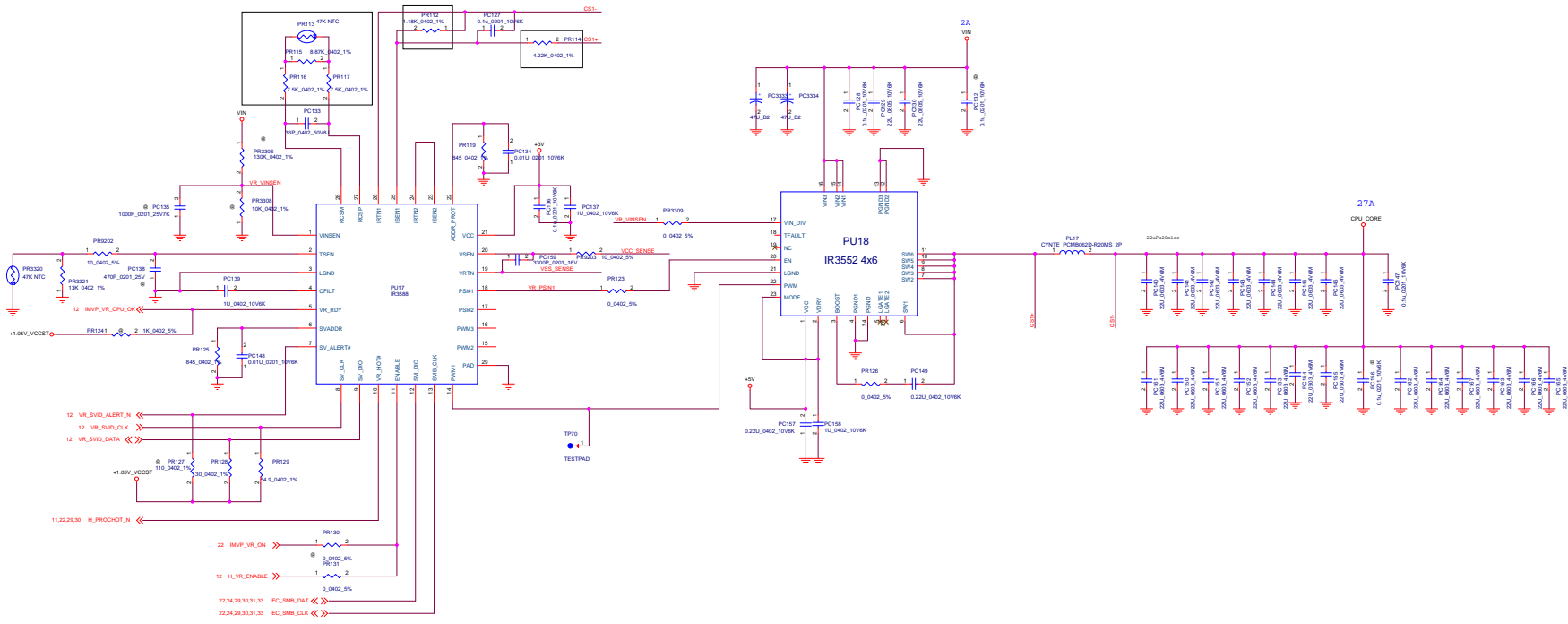




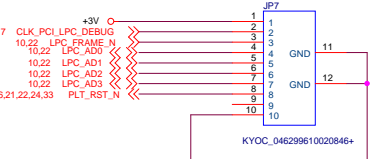
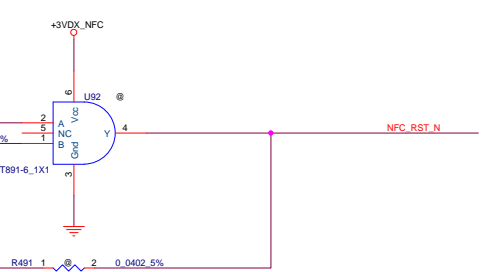
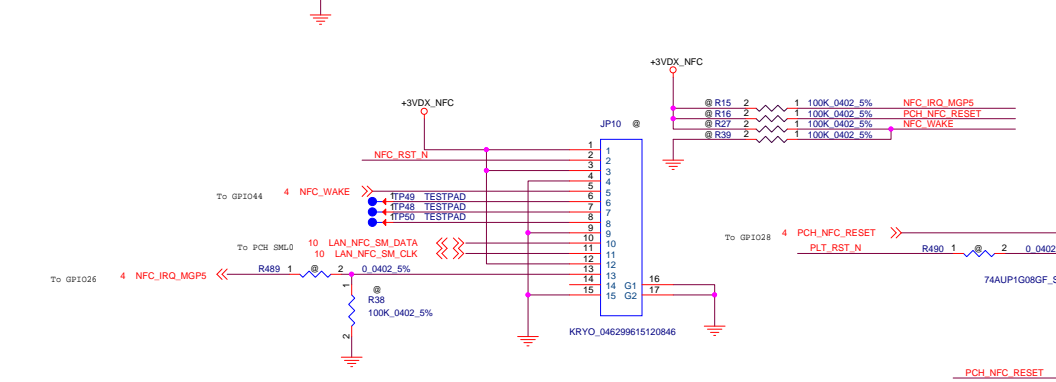
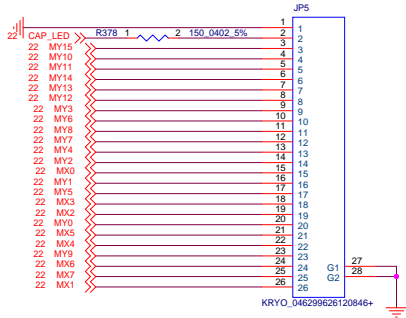
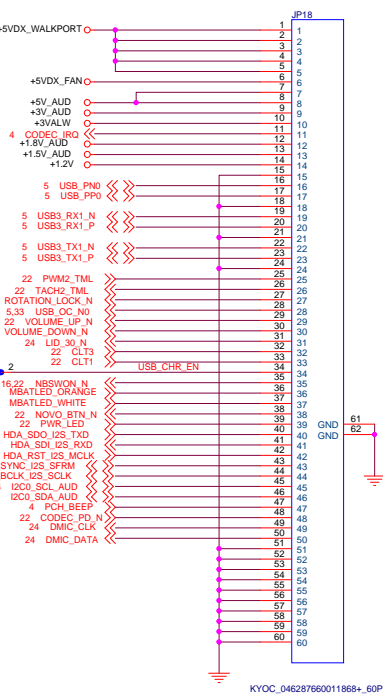
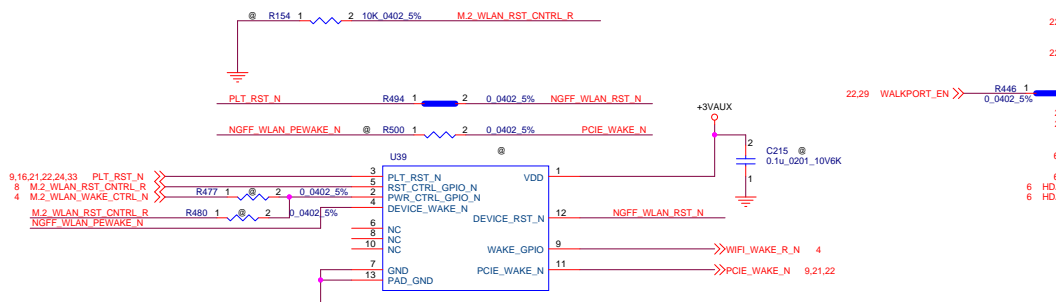
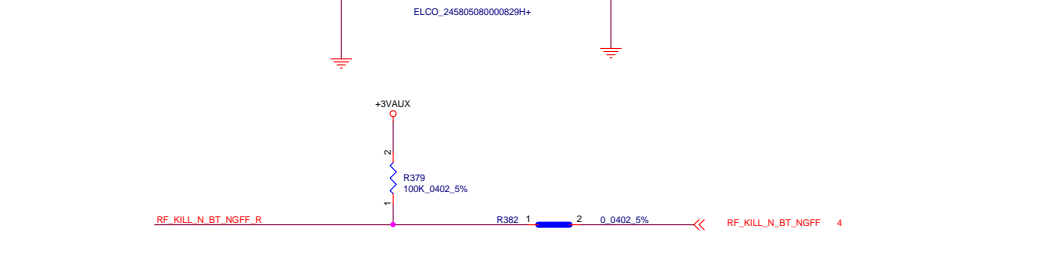
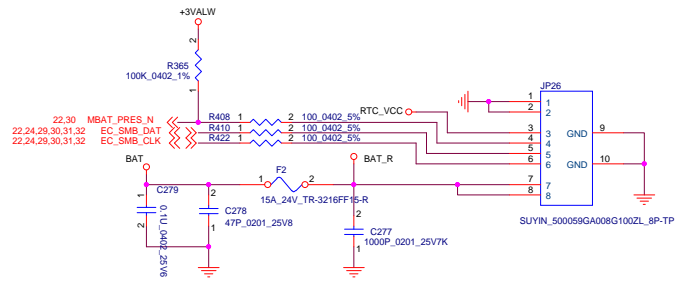
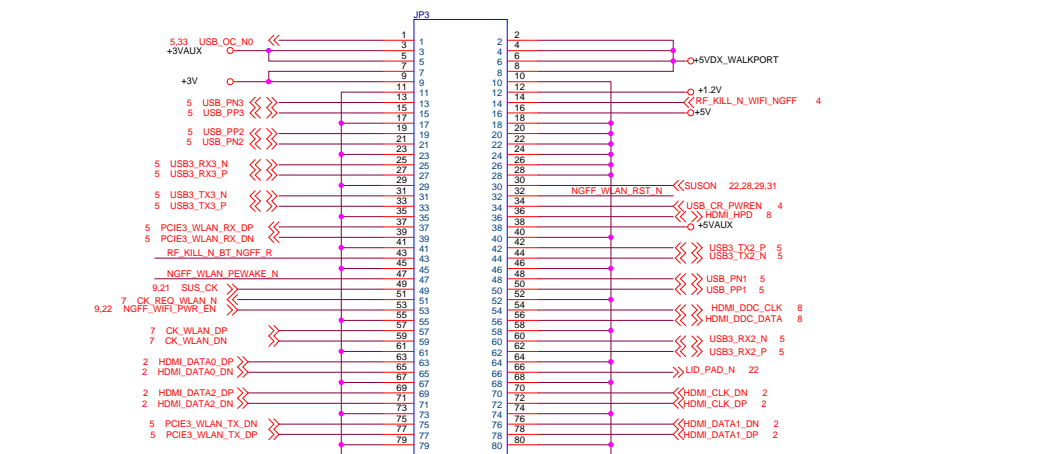
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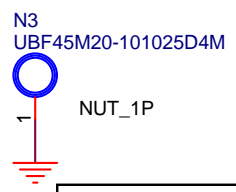
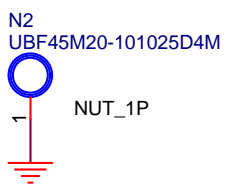
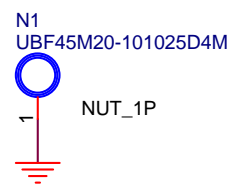
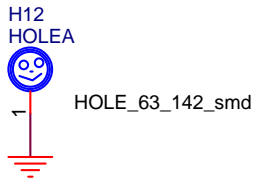
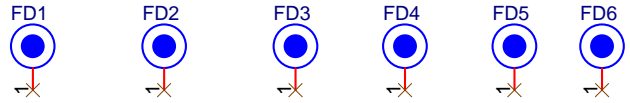
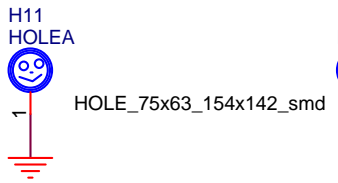
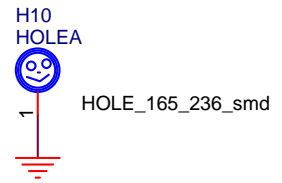
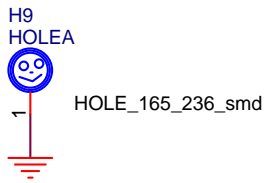
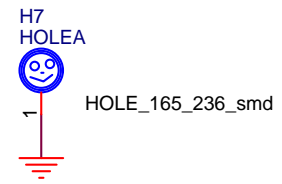
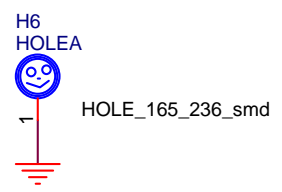
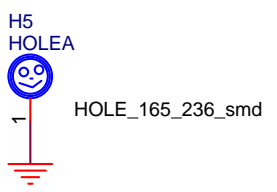
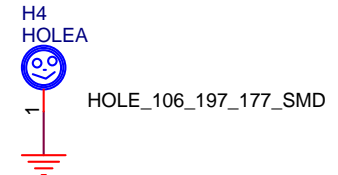
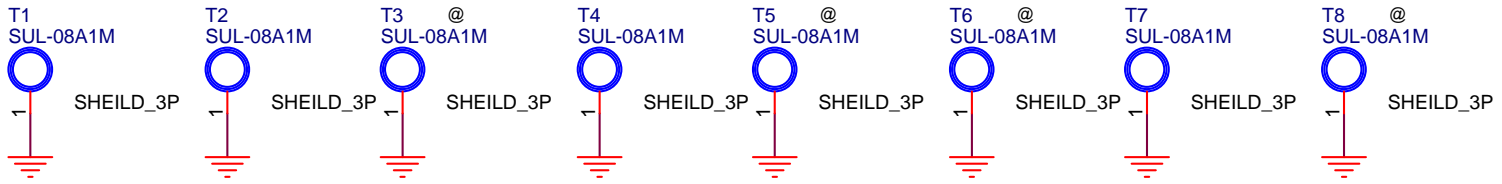
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