Model Name : P7YE0/P7YH0/P7YS0
File Name : LA-6911P
BOM P/N:43

Compal Confidential

P7YE0/P7YH0/P7YS0 M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
ATI Seymour/Whistler/Granville

2010-11-01

REV:0.3

Security Classification	Compal Secret Data		
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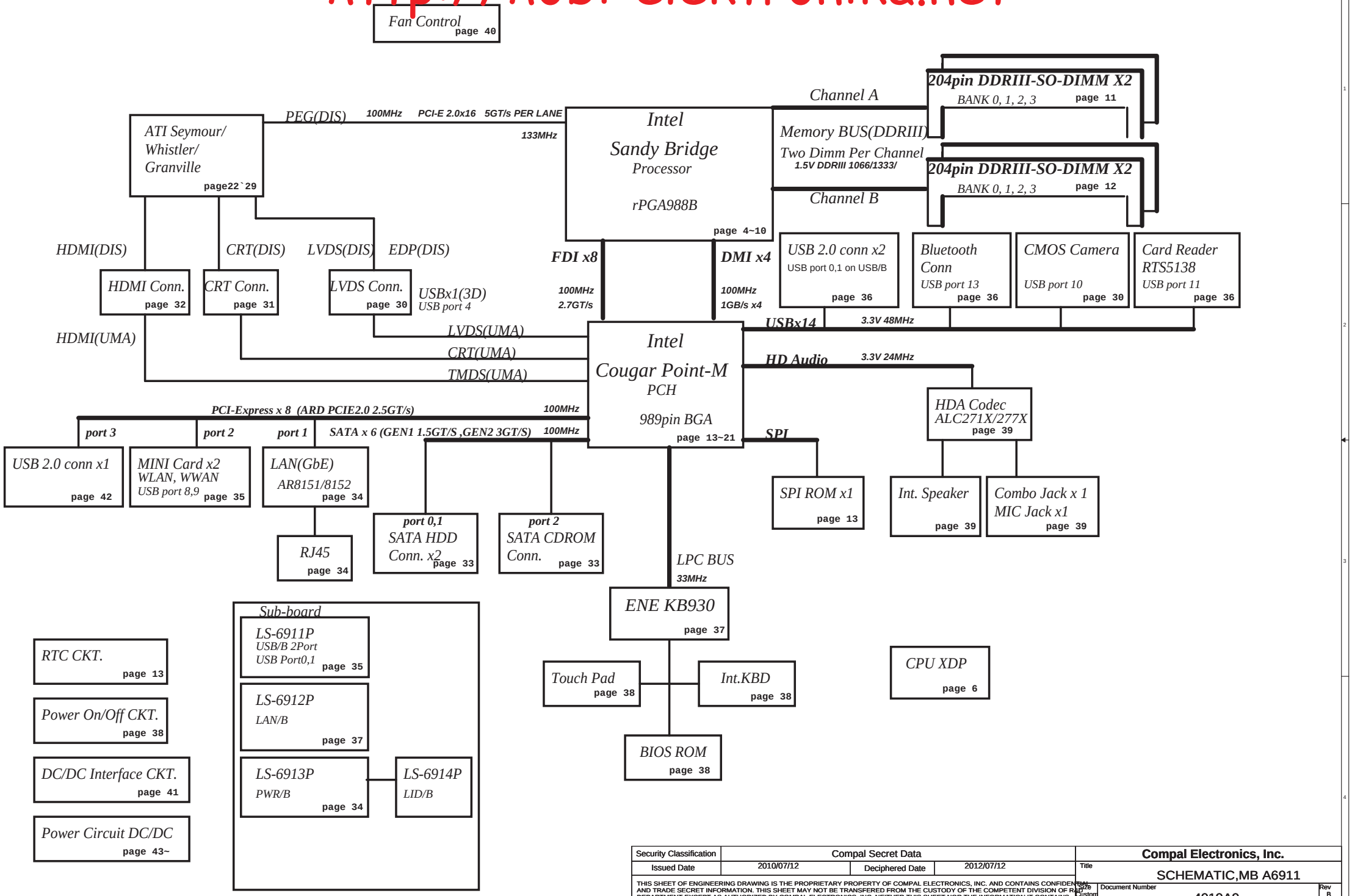
Date: Tuesday, November 09, 2010	Sheet 1 of 60	



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Title	SCHEMATIC,MB A6911	
Size: Custom	Document Number: 4019A9	Rev: B
Date: Tuesday, November 09, 2010	Sheet 2 of 60	

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5V to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure	
UMA Only	UMAO@	
Muxless/UMA	UMA@	
DIS Only	DISO@	P9,P19,P23,P30-32,P59
Muxless/DIS	DIS@	P4,P14
Muxless/DIS	VGA@	P.22-28
BACO mode	BACO@	P.26 ,P.29
nonBACO mode	NOBACO@	
VRAM	X76@	P.27,28
128bit VRAM	128@	P.27
Granville GPU	GRAN@	P.23,P.59
Whistler GPU	WHIS@	P.59
Seymour GPU	SEYM@	P.22-26
non Granville GPU	NOGRAN@	P.23,P.25
Blue Tooth	BT@	P.35
Connector	CONN@	
Unpop	@	
DIS eDP	DEDP@	P.30,59
UMA LVDS	ULVDS@	P.30
DIS LVDS	DLVDS@	
Muxless	MUXL@	P.18,P.32
non Muxless	NOMUXL@	P.18
USB2.0 Conn	USB2@	P.41
USB3.0 Conn	USB3@	P.41
4 Dimm	4DIMM@	P.11-12

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device			Address	
ChannelA	DIMM0	A0	1010 000X	JDIMM1
	DIMM1	A2	1010 001X	JDIMM3
ChannelB	DIMM0	A4	1010 010X	JDIMM2
	DIMM1	A6	1010 011X	JDIMM4

VRAM P/N

SAM	64*16	900M	SA00004GS10(S IC D3 64M16 K4W1G1646G-BC11 FBGA ABO!)
SAM	64*16	800M	SA000035720(S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)
SAM	128*16	800M	SA00003MQ60 (S IC D3 128M16 K4W2G1646C-HC12 FBGA ABO!)
HYN	64*16	900M	SA000041S40(S IC D3 64MX16 H5TQ1G63DFR-11C FBGA ABO!)
HYN	64*16	800M	SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO!)
HYN	128*16	800M	SA00003VS10 (S IC D3 128M16 H5TQ2G63BFR-12C FBGA ABO!)
HYN	64*16	800M	SA0000324G0(S IC D3 64M16 H5TQ1G63DFR-12C FBGA ABO!)

BT Config
BT SKU: BT@
4DIMM config
4 DIMM: 4DIMM@
LVDS/eDP config
UMA LVDS: ULVDS@
DIS LVDS: DLVDS@
DIS eDP: DEDP@

GPU config
Whistler: WHIS@
Seymour: SEYM@
Granville: GRAN@
Granville config
Granville: GRAN@ (VDDCI)
nonGranville: NOGRAN@ (VGA_CORE)
GPU Frame config
128bit: 128@ (WHIS,GRAN)

BACO config
BACO: BACO@
nonBACO: NOBACO@
Muxless config
Muxless: MUXL@
nonMuxless: NOMUXL@ (DISO,UMAO)

VRAM BOM Config

X76264BOL01:	64Mx16x4 Seymour	512M HYN NEW
X76264BOL02:	64Mx16x4 Seymour	512M HYN OLD
X76264BOL03:	64Mx16x8 Whistler/Granville	1G HYN NEW
X76264BOL04:	64Mx16x8 Whistler/Granville	1G HYN OLD
X76264BOL05:	128Mx16x8 Whistler/Granville	2G HYN
X76264BOL06:	128Mx16x8 Whistler/Granville	2G SAM
X76264BOL07:	128Mx16x4 Seymour	1G SAM
X76264BOL08:	128Mx16x4 Seymour	1G HYN

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B(Right side 2.0 option)
		1	USB/B(Right side 2.0 option)
	UHCI1	2	USB port(left side 2.0)
		3	USB/B(Right side 3.0 option)
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini Card(WLAN)
		9	Mini Card
	UHCI5	10	Camera
		11	Card Reader
	UHCI6	12	
		13	Blue Tooth

BOM Config

* UMA Only LVDS Panel:	BT@/UMAO@/UMA@/ULVDS@/NOMUXL@		+DIMM,USB option
* DIS Only LVDS Panel:	BT@/DIS@/VGA@/DISO@/DLVDS@/NOMUXL@	+X76+GPU	+DIMM,USB option
DIS Only EDP Panel:	BT@/DIS@/VGA@/DISO@/DEDP@/NOMUXL@	+X76+GPU	+DIMM,USB option
* Muxless BACO LVDS Panel:	BT@/UMA@/DIS@/VGA@/ULVDS@/BACO@/MUXL@	+X76+GPU(S,W)	+DIMM,USB option
Muxless nonBACO LVDS Panel:	BT@/UMA@/DIS@/VGA@/ULVDS@/NOBACO@/MUXL@	+X76+GPU(G)	+DIMM,USB option

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Size: Custom	Document Number: 4019A9		Rev: B
Date: Tuesday, November 09, 2010	Sheet 3 of 60		

PEG_ICOMPI and RCOMPO signals should be shorted and routed
with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils
- typical impedance = 14.5 mohms

PEG_GTX_HRX_N[0..15] 22
PEG_GTX_HRX_P[0..15] 22
PEG_HTX_C_GRX_N[0..15] 22
PEG_HTX_C_GRX_P[0..15] 22

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms
should not be left floating ,even if disable eDP function...

+1.05VS_VTT
R118 24.9_0402_1%
EDP_COMP

+1.05VS_VTT
R532 24.9_0402_1%
PEG_COMP

JCPU1A

DMI
15 DMI_CRX_PTX_N0 B27 DMI_RX#[0]
15 DMI_CRX_PTX_N1 B25 DMI_RX#[1]
15 DMI_CRX_PTX_N2 A25 DMI_RX#[2]
15 DMI_CRX_PTX_N3 B24 DMI_RX#[3]
15 DMI_CRX_PTX_P0 B28 DMI_RX[0]
15 DMI_CRX_PTX_P1 B26 DMI_RX[1]
15 DMI_CRX_PTX_P2 A24 DMI_RX[2]
15 DMI_CRX_PTX_P3 B23 DMI_RX[3]
15 DMI_CTX_PRX_N0 G21 DMI_TX#[0]
15 DMI_CTX_PRX_N1 E22 DMI_TX#[1]
15 DMI_CTX_PRX_N2 F21 DMI_TX#[2]
15 DMI_CTX_PRX_N3 D21 DMI_TX#[3]
15 DMI_CTX_PRX_P0 G22 DMI_TX[0]
15 DMI_CTX_PRX_P1 D22 DMI_TX[1]
15 DMI_CTX_PRX_P2 F20 DMI_TX[2]
15 DMI_CTX_PRX_P3 C21 DMI_TX[3]

Intel(R) FDI
15 FDI_CTX_PRX_N0 A21 FDI0_TX#[0]
15 FDI_CTX_PRX_N1 H19 FDI0_TX#[1]
15 FDI_CTX_PRX_N2 E19 FDI0_TX#[2]
15 FDI_CTX_PRX_N3 F18 FDI0_TX#[3]
15 FDI_CTX_PRX_N4 B21 FDI1_TX#[0]
15 FDI_CTX_PRX_N5 C20 FDI1_TX#[1]
15 FDI_CTX_PRX_N6 D18 FDI1_TX#[2]
15 FDI_CTX_PRX_N7 F17 FDI1_TX#[3]
15 FDI_CTX_PRX_P0 A22 FDI0_TX[0]
15 FDI_CTX_PRX_P1 G19 FDI0_TX[1]
15 FDI_CTX_PRX_P2 F20 FDI0_TX[2]
15 FDI_CTX_PRX_P3 G18 FDI0_TX[3]
15 FDI_CTX_PRX_P4 B20 FDI1_TX[0]
15 FDI_CTX_PRX_P5 C19 FDI1_TX[1]
15 FDI_CTX_PRX_P6 D19 FDI1_TX[2]
15 FDI_CTX_PRX_P7 F17 FDI1_TX[3]
15 FDI_FSYNC0 J18 FDI0_FSYNC
15 FDI_FSYNC1 J17 FDI1_FSYNC
15 FDI_INT H20 FDI_INT
15 FDI_LSYNC0 J19 FDI0_LSYNC
15 FDI_LSYNC1 H17 FDI1_LSYNC

eDP
A18 eDP_COMPIO
A17 eDP_ICOMPO
B16 eDP_HPD
C15 eDP_AUX
D15 eDP_AUX#
C17 eDP_TX[0]
F16 eDP_TX[1]
C16 eDP_TX[2]
G15 eDP_TX[3]
C18 eDP_TX#[0]
F16 eDP_TX#[1]
D16 eDP_TX#[2]
F15 eDP_TX#[3]

PCI EXPRESS* - GRAPHICS
J22 PEG_ICOMPI
J21 PEG_ICOMPO
H22 PEG_RCOMPO

PEG_RX#[0] K33 PEG_GTX_C_HRX_N15 C320 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N15
PEG_RX#[1] M35 PEG_GTX_C_HRX_N14 C316 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N14
PEG_RX#[2] L34 PEG_GTX_C_HRX_N13 C313 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N13
PEG_RX#[3] J35 PEG_GTX_C_HRX_N12 C308 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N12
PEG_RX#[4] J32 PEG_GTX_C_HRX_N11 C300 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N11
PEG_RX#[5] H34 PEG_GTX_C_HRX_N10 C297 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N10
PEG_RX#[6] H31 PEG_GTX_C_HRX_N9 C287 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N9
PEG_RX#[7] G33 PEG_GTX_C_HRX_N8 C275 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N8
PEG_RX#[8] G30 PEG_GTX_C_HRX_N7 C262 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N7
PEG_RX#[9] F35 PEG_GTX_C_HRX_N6 C249 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N6
PEG_RX#[10] E34 PEG_GTX_C_HRX_N5 C244 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N5
PEG_RX#[11] E32 PEG_GTX_C_HRX_N4 C233 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N4
PEG_RX#[12] D33 PEG_GTX_C_HRX_N3 C224 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N3
PEG_RX#[13] D31 PEG_GTX_C_HRX_N2 C207 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N2
PEG_RX#[14] B33 PEG_GTX_C_HRX_N1 C206 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N1
PEG_RX#[15] C32 PEG_GTX_C_HRX_N0 C194 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N0

PEG_RX[0] J33 PEG_GTX_C_HRX_P15 C318 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P15
PEG_RX[1] L35 PEG_GTX_C_HRX_P14 C314 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P14
PEG_RX[2] K34 PEG_GTX_C_HRX_P13 C309 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P13
PEG_RX[3] H35 PEG_GTX_C_HRX_P12 C303 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P12
PEG_RX[4] H32 PEG_GTX_C_HRX_P11 C298 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P11
PEG_RX[5] G34 PEG_GTX_C_HRX_P10 C288 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P10
PEG_RX[6] G31 PEG_GTX_C_HRX_P9 C278 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P9
PEG_RX[7] F33 PEG_GTX_C_HRX_P8 C265 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P8
PEG_RX[8] F30 PEG_GTX_C_HRX_P7 C255 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P7
PEG_RX[9] E35 PEG_GTX_C_HRX_P6 C246 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P6
PEG_RX[10] E33 PEG_GTX_C_HRX_P5 C235 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P5
PEG_RX[11] E32 PEG_GTX_C_HRX_P4 C225 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P4
PEG_RX[12] D34 PEG_GTX_C_HRX_P3 C214 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P3
PEG_RX[13] E31 PEG_GTX_C_HRX_P2 C210 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P2
PEG_RX[14] C33 PEG_GTX_C_HRX_P1 C196 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P1
PEG_RX[15] B32 PEG_GTX_C_HRX_P0 C190 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P0

PEG_TX#[0] M29 PEG_HTX_GRX_N15 C685 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N15
PEG_TX#[1] M32 PEG_HTX_GRX_N14 C683 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N14
PEG_TX#[2] M31 PEG_HTX_GRX_N13 C680 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N13
PEG_TX#[3] L32 PEG_HTX_GRX_N12 C676 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N12
PEG_TX#[4] L29 PEG_HTX_GRX_N11 C673 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N11
PEG_TX#[5] K31 PEG_HTX_GRX_N10 C671 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N10
PEG_TX#[6] K28 PEG_HTX_GRX_N9 C667 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N9
PEG_TX#[7] J30 PEG_HTX_GRX_N8 C663 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N8
PEG_TX#[8] J28 PEG_HTX_GRX_N7 C661 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N7
PEG_TX#[9] H29 PEG_HTX_GRX_N6 C659 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N6
PEG_TX#[10] G27 PEG_HTX_GRX_N5 C654 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N5
PEG_TX#[11] F29 PEG_HTX_GRX_N4 C648 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N4
PEG_TX#[12] F27 PEG_HTX_GRX_N3 C644 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N3
PEG_TX#[13] D28 PEG_HTX_GRX_N2 C640 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N2
PEG_TX#[14] F26 PEG_HTX_GRX_N1 C637 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N1
PEG_TX#[15] E25 PEG_HTX_GRX_N0 C631 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N0

PEG_TX[0] M28 PEG_HTX_GRX_P15 C684 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P15
PEG_TX[1] M33 PEG_HTX_GRX_P14 C681 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P14
PEG_TX[2] M30 PEG_HTX_GRX_P13 C677 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P13
PEG_TX[3] L31 PEG_HTX_GRX_P12 C674 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P12
PEG_TX[4] L28 PEG_HTX_GRX_P11 C670 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P11
PEG_TX[5] K30 PEG_HTX_GRX_P10 C668 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P10
PEG_TX[6] K27 PEG_HTX_GRX_P9 C664 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P9
PEG_TX[7] J29 PEG_HTX_GRX_P8 C662 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P8
PEG_TX[8] J27 PEG_HTX_GRX_P7 C658 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P7
PEG_TX[9] H28 PEG_HTX_GRX_P6 C657 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P6
PEG_TX[10] G28 PEG_HTX_GRX_P5 C650 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P5
PEG_TX[11] E28 PEG_HTX_GRX_P4 C645 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P4
PEG_TX[12] F28 PEG_HTX_GRX_P3 C641 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P3
PEG_TX[13] D27 PEG_HTX_GRX_P2 C636 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P2
PEG_TX[14] F26 PEG_HTX_GRX_P1 C635 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P1
PEG_TX[15] D25 PEG_HTX_GRX_P0 C626 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P0

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

Sandy Bridge_rPGA_Rev0p61
CONN@

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Size: Custom	Document Number: 4019A9		Rev: B
Date: Tuesday, November 09, 2010	Sheet 4 of 60		

+3VS R418 4.7K_0402_5% +3VS
14,34 PCH_SMBDATA — Q26A @ DMN66D0LDW-7_SOT363-6 — SMB_DATA_S3
+3VS R407 4.7K_0402_5% +3VS
14,34 PCH_SMBCLK — Q26B @ DMN66D0LDW-7_SOT363-6 — SMB_CLK_S3
Connect to CPU,PCH XDP

+1.05VS_VTT +1.05VS_VTT
JXDP1
XDP_PREQ# XDP_PRDY# XDP_BPM#0 XDP_BPM#1 XDP_BPM#2 XDP_BPM#3 XDP_BPM#4 XDP_BPM#5 XDP_BPM#6 XDP_BPM#7 XDP_TCK
GND0 OBSFN_A0 OBSFN_A1 GND2 OBSDATA_A0 OBSDATA_A1 GND4 OBSDATA_A2 OBSDATA_A3 GND6 OBSFN_B0 OBSFN_B1 GND8 OBSDATA_B0 OBSDATA_B1 GND10 OBSDATA_B2 OBSDATA_B3 GND12 PWRGOOD/HOOK0 HOOK1 VCC_OBS_AB HOOK2 HOOK3 GND14 SDA SCL TCK1 TCK0 GND16
GND1 OBSFN_C0 OBSFN_C1 GND3 OBSDATA_C0 OBSDATA_C1 GND5 OBSDATA_C2 OBSDATA_C3 GND7 OBSFN_D0 OBSFN_D1 GND9 OBSDATA_D0 OBSDATA_D1 GND11 OBSDATA_D2 OBSDATA_D3 GND13 ITPCLK/HOOK4 ITPCLK#/HOOK5 VCC_OBS_CD RESET#/HOOK6 DBR#/HOOK7 GND15 TDO TRST# TDI TMS GND17
SAMTE_BSH-030-01-L-D-A
CONN@
H_CPUPWRGD R605 1K_0402_5% H_CPUPWRGD_XDP
15,36 PBTN_OUT# — R603 0_0402_5% CFD_PWRBTN#_XDP
7 CFG0 — CFG0 R602 1K_0402_5% XDP_HOOK2
SYS_PWROK R600 0_0402_5% SYS_PWROK_XDP
SMB_DATA_S3
SMB_CLK_S3
CLK_CPU_ITP — CLK_CPU_ITP 14
CLK_CPU_ITP# — CLK_CPU_ITP# 14
XDP_RST#_R R601 1K_0402_5% — PLT_RST# 17,34,35,36,41
XDP_DBRESET#
XDP_TDO
XDP_TRST#
XDP_TDI
XDP_TMS

Debug port DG 0.65~
Note: 1. These signals are optional, can be left as OPEN/No-Connect if debug by Intel will not be needed

+1.05VS_VTT
CLK_CPU_DPLL# R116 1K_0402_5%
CLK_CPU_DPLL R117 1K_0402_5%
Checklist1.0 P.58 Graphis Disable Guide
DIS only SKU eDP disable
DPLL_REF_SSCLK PD 1K_5% to GND
DPLL_REF_SSCLK# PH 1K_5% to +1.05VS_VTT

PROC_SELECT#
Future platforms,PH VCPLL and connect to PCH DF_TVS
偵測CPU有無安裝
XBOX 三紅功能
PCH->CPU
UNCOREPWRGOOD:非CORE外的電OK
SM_DRAMPWROK:DRAM power ok
RESET#:都ok後請CPU做reset

JCPU1B
17 H_SNB_IVB# — C26 SNB_IVB# — MISC
AN34 SKTOCC#
T2 PAD H_CATERR# — AL33 CATERR# — THERMAL
18,36 H_PECI — H_PECI — AN33 PECI
36,45 H_PROCHOT# — R220 62_0402_5% — H_PROCHOT# — R216 56_0402_5% — H_PROCHOT#_R — AL32 PROCHOT#
18 H_THRMTRIP# — AN32 THERMTRIP#
15 H_PM_SYNC — AM34 PM_SYNC — PWR MANAGEMENT
18 H_CPUPWRGD — H_CPUPWRGD — AP33 UNCOREPWRGOOD
PM_DRAM_PWRGD_R — V8 SM_DRAMPWROK
BUF_CPU_RST# — AR33 RESET#
Sandy Bridge_rPGA_Rev0p61
CONN@

BCLK A28 — CLK_CPU_DMI 14
BCLK# A27 — CLK_CPU_DMI# 14 — CLOCKS
DPLL_REF_SSCLK A16 — CLK_CPU_DPLL — CLK_CPU_DPLL 14
DPLL_REF_SSCLK# A15 — CLK_CPU_DPLL# — CLK_CPU_DPLL# 14
SM_DRAMRST# — R8 — SM_DRAMRST# — SM_DRAMRST# 6 — DDR3 MISC
SM_RCOMP[0] AK1 — SM_RCOMP0 R149 140_0402_1%
SM_RCOMP[1] A5 — SM_RCOMP1 R486 25.5_0402_1%
SM_RCOMP[2] A4 — SM_RCOMP2 R484 200_0402_1%
DDR3 Compensation Signals
PRDY# AP29 XDP_PRDY#
PREQ# AP27 XDP_PREQ#
TCK AR26 XDP_TCK
TMS AR27 XDP_TMS
TRST# AP30 XDP_TRST#
TDI AR28 XDP_TDI
TDO AP26 XDP_TDO — JTAG & BPM
DBR# — AL35 XDP_DBRESET# — XDP_DBRESET# 15
BPM#[0] AT28 XDP_BPM#0
BPM#[1] AR29 XDP_BPM#1
BPM#[2] AR30 XDP_BPM#2
BPM#[3] AT30 XDP_BPM#3
BPM#[4] AP32 XDP_BPM#4
BPM#[5] AR31 XDP_BPM#5
BPM#[6] AT31 XDP_BPM#6
BPM#[7] AR32 XDP_BPM#7

PU/PD for JTAG signals
+1.05VS_VTT
XDP_TMS R202 51_0402_5%
XDP_TDI R210 51_0402_5%
XDP_TDO R200 51_0402_5%
XDP_TCK R209 51_0402_5%
XDP_TRST# R205 51_0402_5%
+3VS
XDP_DBRESET# R569 1K_0402_5%
CRB1.0 PH 1K +3VS
Check list 1.0 PH 5K +3VS
Check list 1.2 PH 10K +3VS
Debug port DG1.1-1.2 50~5K ohm

Follow DG 1.2 & CRB1.0
R223 10K_0402_5% H_CPUPWRGD

Processor Pullups follow CRB1.0

Follow DG 1.2 & CRB1.0
Buffered reset to CPU
+3VS C396 0.1U_0402_16V4Z
+1.05VS_VTT R226 75_0402_5%
R227 43_0402_1%
U15
PLT_RST# — @R249 0_0402_5% — BUFO_CPU_RST# — BUF_CPU_RST#
SN74LVC1G07DCKR SC-70 5P
R225 1K_0402_1% @
RESET#:都ok後請CPU做reset

Use open drain MOS:
+1.05VS_VTT PH pop 75ohm
series resister pop 43ohm
UNCOREPWRGOOD:非CORE外的電OK
SM_DRAMPWROK:DRAM power ok

Follow DG 1.2 & CRB1.0
+3VALW C101 0.1U_0402_16V4Z
+1.5V_CPU_VDDQ R88 200_0402_5%
U5
15 SYS_PWROK
15 PM_DRAM_PWRGD — PM_SYS_PWRGD_BUF — R97 130_0402_5% — PM_DRAM_PWRGD_R
MC74VHC1G09DFT2G SC70 5P
R104 1.3K_0402_1% @

Use open drain MOS:
+1.5V_CPU_VDDQ PH pop 200ohm
series resister pop 130ohm

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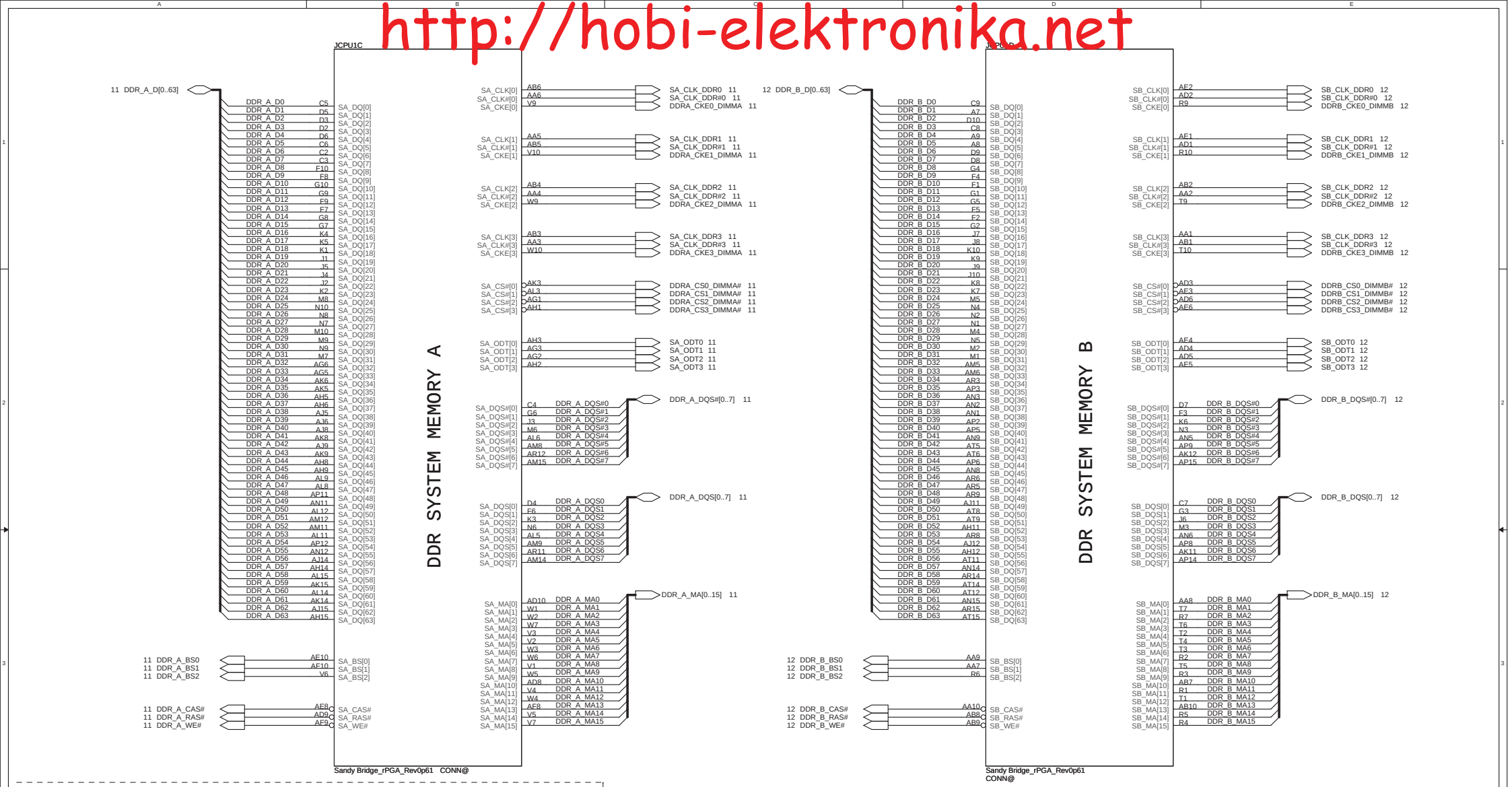
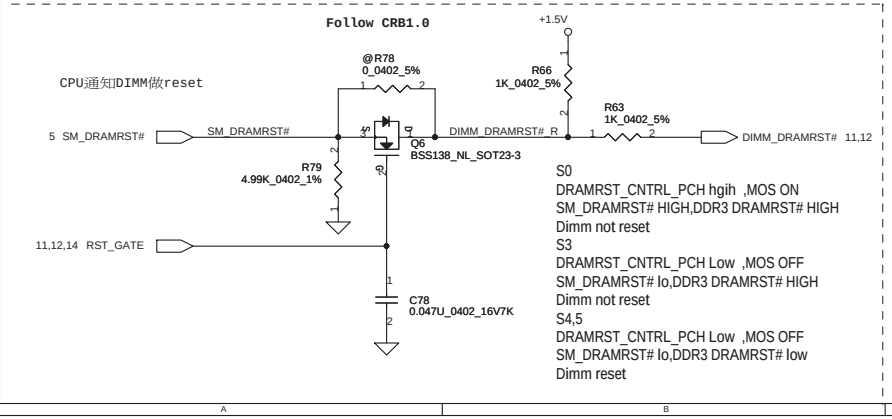
Title: SCHEMATIC,MB A6911
Size: Custom | Document Number: 4019A9 | Rev: B
Date: Tuesday, November 09, 2010 | Sheet 5 of 60





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Title: SCHEMATIC,MB A6911

Size	Document Number	Rev
Custom	4019A9	B

Date: Tuesday, November 09, 2010 Sheet 6 of 60

CFG Straps for Processor

CFG2 — R234 1K_0402_1%

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

CFG4 — R204 1K_0402_1% @ — UMA,Muxless eDP啓動 DISO eDP關閉

eDP enable	
CFG4	* 1:Disable 0:Enable

CFG6 — R230 1K_0402_1% @ — CFG5 — R228 1K_0402_1%

PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) 1x16 PCI Express 10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express

CFG7 — @ R224 1K_0402_1%

PEG DEFER TRAINING	CRB1.0 P.12
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

JCPU1E — RESERVED — Sandy Bridge_rPGA_Rev0p61 CONN@

5 CFG0 — CFG0 AK28 CFG[0]; CFG2 AK29 CFG[1]; AL26 CFG[2]; AL27 CFG[3]; CFG4 AK26 CFG[4]; CFG5 AL29 CFG[5]; CFG6 AL30 CFG[6]; CFG7 AM31 CFG[7]; AM32 CFG[8]; AM30 CFG[9]; AM28 CFG[10]; AM26 CFG[11]; AN28 CFG[12]; AN31 CFG[13]; AN26 CFG[14]; AM27 CFG[15]; AK31 CFG[16]; AN29 CFG[17]

VCC_VAL_SENSE — T4 PAD @ — AJ31 RSVD1
VSS_VAL_SENSE — T6 PAD @ — AH31 RSVD2
VAXG_VAL_SENSE — T5 PAD @ — AJ33 RSVD3
VSSAXG_VALSENSE — T3 PAD @ — AH33 RSVD4

AJ26 RSVD5

SA_DIMM_VREFDQ
SB_DIMM_VREFDQ
For Future CPU M3 support,
Sandey bridge not supportM3,
Check list1.0&CRB say can NC

11 SA_DIMM_VREFDQ — SA_DIMM_VREFDQ — B4 RSVD6
12 SB_DIMM_VREFDQ — SB_DIMM_VREFDQ — D1 RSVD7

R68 1K_0402_1% — R69 1K_0402_1%

F25 RSVD8; F24 RSVD9; F23 RSVD10; D24 RSVD11; G25 RSVD12; G24 RSVD13; E23 RSVD14; D23 RSVD15; C30 RSVD16; A31 RSVD17; B30 RSVD18; B29 RSVD19; D30 RSVD20; B31 RSVD21; A30 RSVD22; C29 RSVD23

J20 RSVD24; B18 RSVD25; A19 RSVD26

J15 RSVD27

VCCIO_SEL — R520 10K_0402_5% @

VCCIO_SEL — A19

VCCIO_SEL For 2012 CPU support	
A19	* 1/NC : (Default) +1.05VS_VTT 0: +1.0VS_VTT

RSVD28 L7; RSVD29 AG7; RSVD30 AE7; RSVD31 AK2; RSVD32 W8

RSVD33 AT26; RSVD34 AM33; RSVD35 AJ27

RSVD37 T8; RSVD38 J16; RSVD39 H16; RSVD40 G16

RSVD41 AR35; RSVD42 AT34; RSVD43 AT33; RSVD44 AP35; RSVD45 AR34

RSVD46 B34; RSVD47 A33; RSVD48 A34; RSVD49 B35; RSVD50 C35

RSVD51 AJ32; RSVD52 AK32

RSVD53 AH27 — PAD @ T1

RSVD54 AN35; RSVD55 AM35

RSVD56 AT2; RSVD57 AT1; RSVD58 AR1

KEY B1

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Issued Date	2010/07/12	Deciphered Date	2012/07/12

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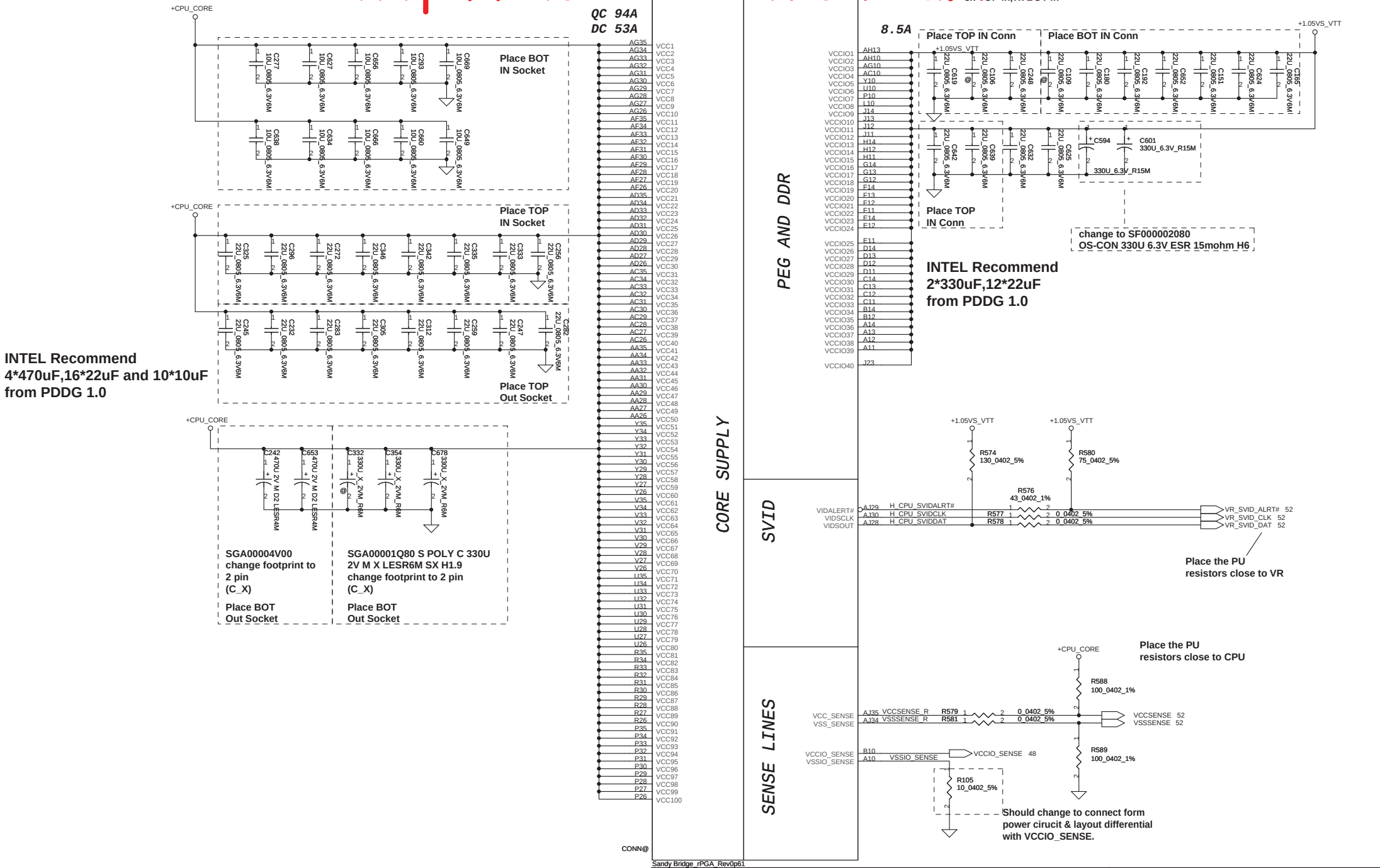
Title: SCHEMATIC,MB A6911

Size: Custom | Document Number: 4019A9 | Rev: B

Date: Tuesday, November 09, 2010 | Sheet 7 of 60

POWER



Sandy Bridge_rPGA_Rev0p61

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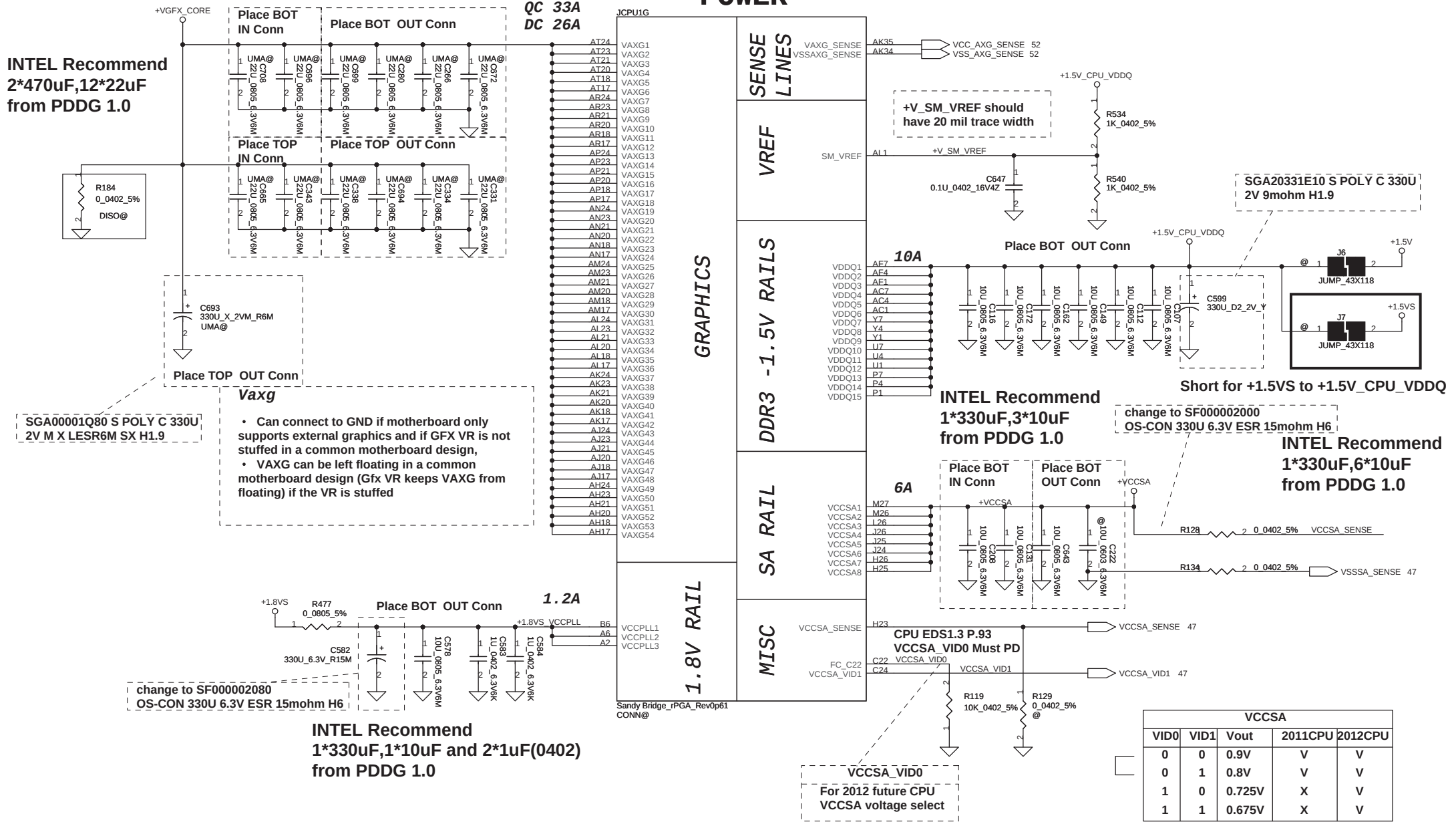
Size: Custom | Document Number: 4019A9 | Rev: B

Date: Tuesday, November 09, 2010 | Sheet 8 of 60

POWER



VCCSA				
VID0	VID1	Vout	2011CPU	2012CPU
0	0	0.9V	V	V
0	1	0.8V	V	V
1	0	0.725V	X	V
1	1	0.675V	X	V

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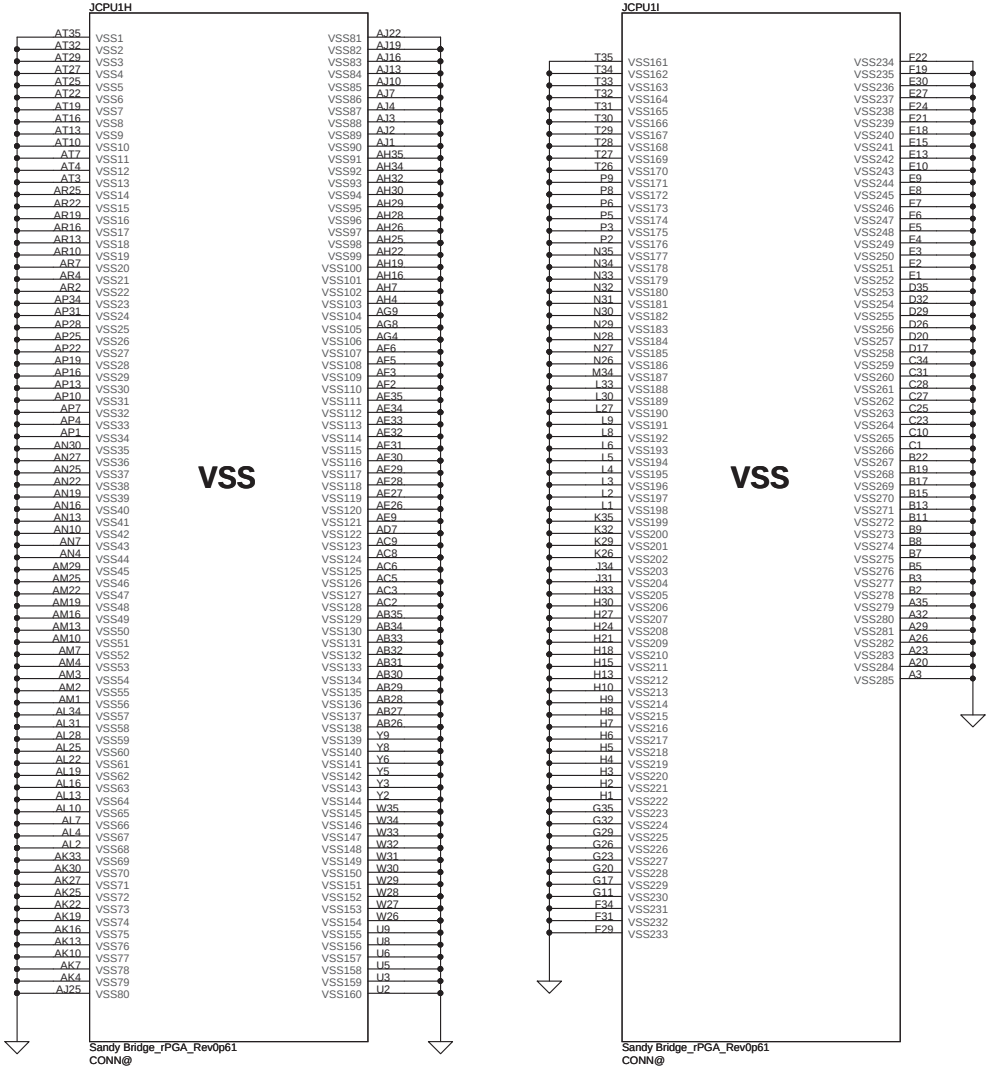
Title	SCHEMATIC,MB A6911		
Size: Custom	Document Number: 4019A9		Rev: B
Date: Tuesday, November 09, 2010	Sheet 9 of 60		



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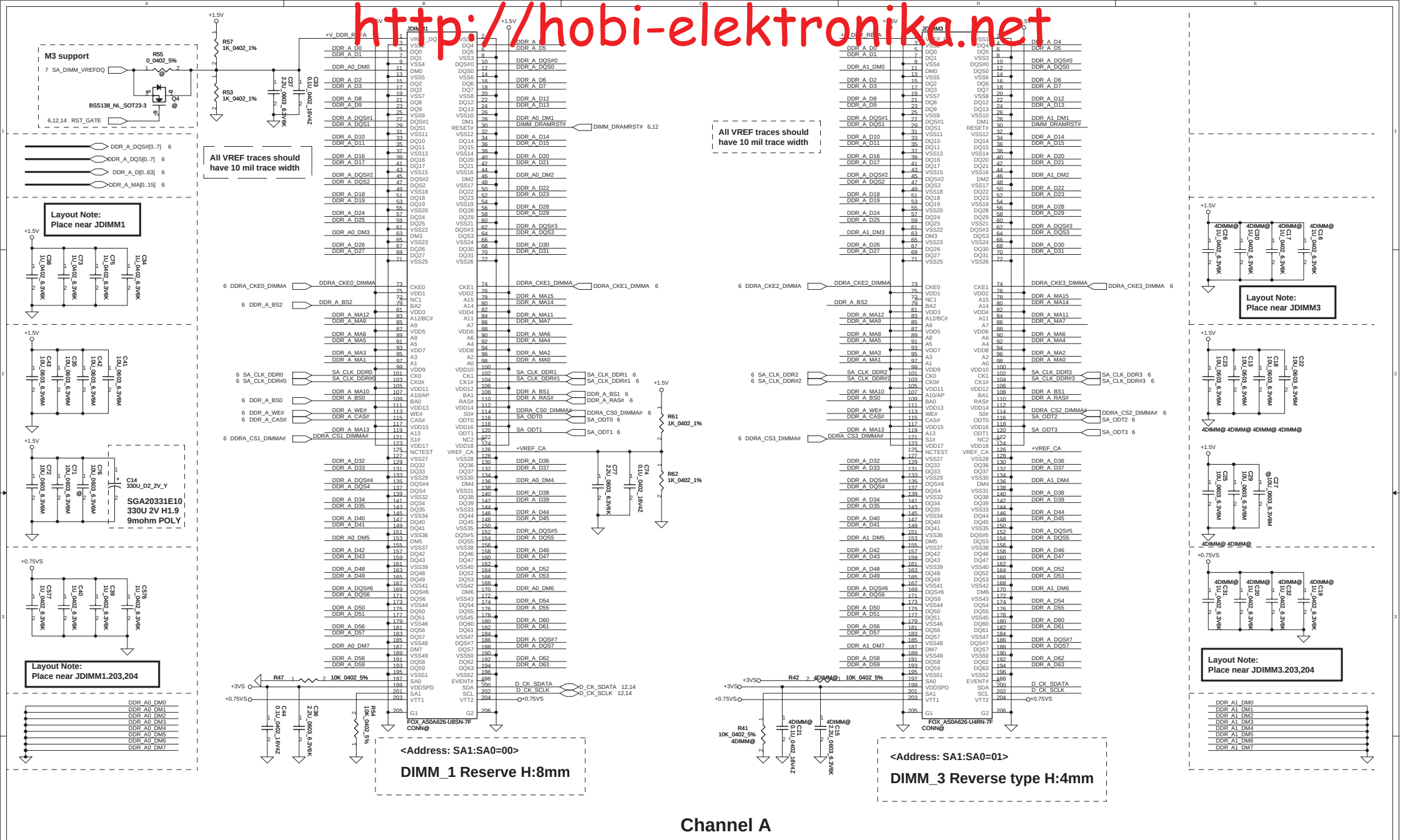
Size: Custom | Document Number: 4019A9 | Rev: B

Date: Tuesday, November 09, 2010 | Sheet 10 of 60



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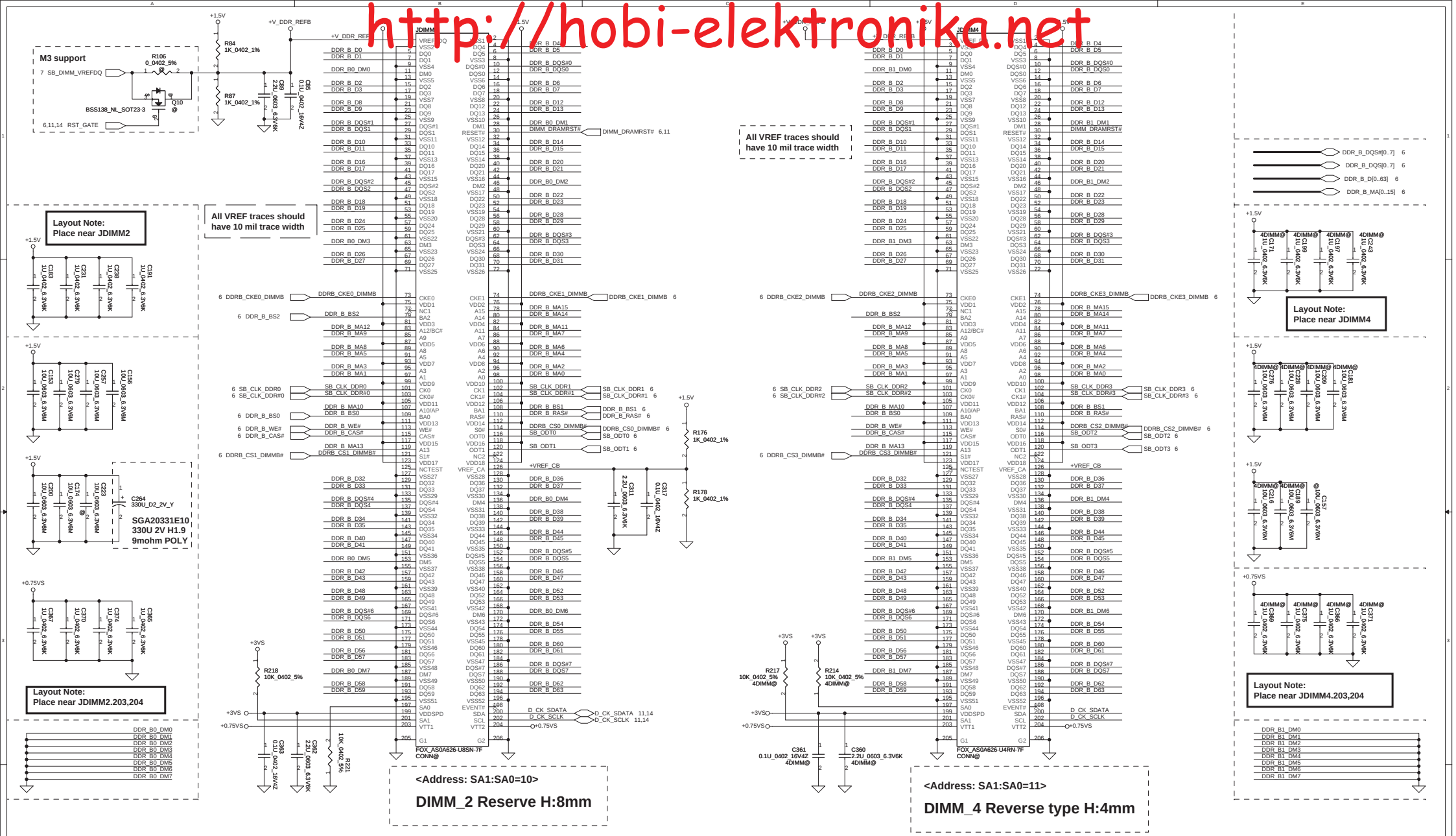
Size	Document Number	Rev
Custom	4019A9	B

Date: Tuesday, November 09, 2010 | Sheet 11 of 60



Channel B

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

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Title: SCHEMATIC,MB A6911

Size	Document Number	Rev
Custom	4019A9	B

Date: Tuesday, November 09, 2010 | Sheet 12 of 60

RTCRST close RAM door J1

+RTCVCC C516 1U_0603_10V6K

R568 0_0603_5% @

R338 20K_0402_5% PCH_RTCRST#

R337 20K_0402_5% PCH_SRTCRST#

C502 1U_0603_10V6K

R561 0_0603_5% @

SRTCRST close RAM door J2

+RTCVCC

R353 1M_0402_5% SM_INTRUDER#

R347 330K_0402_5% PCH_INTVRMEN

INTVRMEN

* H : Integrated VRM enable

L : Integrated VRM disable

(INTVRMEN should always be pull high.)

+3VS

R405 @ 1K_0402_5% PCH_SPKR

HIGH= Enable (No Reboot)Disable TCO timer system reboot feature

* LOW= Disable (Default internal PD)

+3VALW_PCH

@R322 1K_0402_5%

R320 0_0402_5%

36 HDA_SDO HDA_SDOUT_PCH

HDA_SDO

爲何接至EC

ME debug mode,this signal has a weak internal PD

* Low = Disabled (Default)

High = Enabled [Flash Descriptor Security Overide]

+3VALW_PCH

R328 1K_0402_5% HDA_SYNC_PCH

This signal has a weak internal pull-down

On Die PLL VR Select is supplied by

*1.5V when smapled high

1.8V when sampled low

Needs to be pulled High for Huron River platfrom

Prevent back drive issue.

38 HDA_BITCLK_AUDIO R677 33_0402_5% HDA_BITCLK_PCH

38 HDA_SYNC_AUDIO R676 33_0402_5% HDA_SYNC_PCH_R

38 HDA_RST_AUDIO# R673 33_0402_5% HDA_RST_PCH#

38 HDA_SDOUT_AUDIO R669 33_0402_5% HDA_SDOUT_PCH

+3VS

Q20 BSS138_NL_SOT23-3

HDA_SYNC_PCH

R302 @ 0_0402_5%

R468 1M_0402_5%

+3VALW_PCH

R660 200_0402_5% PCH_JTAG_TDO

R659 200_0402_5% PCH_JTAG_TMS

R658 200_0402_5% PCH_JTAG_TDI

R670 100_0402_1%

R671 100_0402_1%

R669 100_0402_1%

PCH_RTCX1

R638 10M_0402_5%

PCH_RTCX2

Y4 32.768KHZ_12.5PF_Q13MC14610002

C756 18P_0402_50V8J

C757 18P_0402_50V8J

U37A

PCH_RTCX1	A20	RTCX1	RTC		
PCH_RTCX2	C20	RTCX2			
PCH_RTCRST#	D20	RTCRST#			
PCH_SRTCRST#	G22	SRTCRST#			
SM_INTRUDER#	K22	INTRUDER#			
PCH_INTVRMEN	C17	INTVRMEN			
		FWH0 / LAD0	LPC	C38	LPC_AD0
		FWH1 / LAD1		A38	LPC_AD1
		FWH2 / LAD2		B37	LPC_AD2
		FWH3 / LAD3		C37	LPC_AD3
		FWH4 / LFRAME#		D36	LPC_FRAME#
		LDRQ0#		E36	
		LDRQ1# / GPIO23		K36	
		SERIRQ		V5	SERIRQ
HDA_BITCLK_PCH	N34	HDA_BCLK	IHDA		
HDA_SYNC_PCH	L34	HDA_SYNC			
38 PCH_SPKR	T10	SPKR			
HDA_RST_PCH#	K34	HDA_RST#			
38 HDA_SDIN0	E34	HDA_SDIN0			
	G34	HDA_SDIN1			
	C34	HDA_SDIN2			
	A34	HDA_SDIN3			
HDA_SDOUT_PCH	A36	HDA_SDO			
	C36	HDA_DOCK_EN# / GPIO33			
	N32	HDA_DOCK_RST# / GPIO13			
		SATA0RXN	SATA 6G	AM3	SATA_PRX_DTX_N0
		SATA0RXP		AM1	SATA_PRX_DTX_P0
		SATA0TXN		AP7	SATA_PTX_DRX_N0
		SATA0TXP		AP5	SATA_PTX_DRX_P0
		SATA1RXN		AM10	SATA_PRX_DTX_N1
		SATA1RXP		AM8	SATA_PRX_DTX_P1
		SATA1TXN		AP11	SATA_PTX_DRX_N1
		SATA1TXP		AP10	SATA_PTX_DRX_P1
		SATA2RXN	SATA	AD7	SATA_PRX_DTX_N2
		SATA2RXP		AD5	SATA_PRX_DTX_P2
		SATA2TXN		AH5	SATA_PTX_DRX_N2
		SATA2TXP		AH4	SATA_PTX_DRX_P2
		SATA3RXN		AB8	
		SATA3RXP		AB10	
		SATA3TXN		AF3	
		SATA3TXP		AF1	
		SATA4RXN		Y7	
		SATA4RXP		Y5	
		SATA4TXN		AD3	
		SATA4TXP		AD1	
		SATA5RXN		Y3	
		SATA5RXP		Y1	
		SATA5TXN		AB3	
		SATA5TXP		AB1	
		SATAICOMPO		Y11	
		SATAICOMPI		Y10	SATA_COMP
		SATA3RCOMPO		AB12	
		SATA3COMPI		AB13	SATA3_COMP
		SATA3RBIAS		AH1	RBIAS_SATA3
		SATALED#		P3	PCH_SATALED#
		SATA0GP / GPIO21		V14	PCH_GPIO21
		SATA1GP / GPIO19		P1	PCH_GPIO19
R672 51_0402_5% PCH_JTAG_TCK	J3	JTAG_TCK	JTAG		
PCH_JTAG_TMS	H7	JTAG_TMS			
PCH_JTAG_TDI	K5	JTAG_TDI			
PCH_JTAG_TDO	H1	JTAG_TDO			
PCH_SPI_CLK_1 R697 0_0402_5% PCH_SPI_CLK	T3	SPI_CLK	SPI		
PCH_SPI_CS0#_1 R696 0_0402_5% PCH_SPI_CS0#	Y14	SPI_CS0#			
	T1	SPI_CS1#			
PCH_SPI_MOSI_1 R678 0_0402_5% PCH_SPI_MOSI	V4	SPI_MOSI			
PCH_SPI_MISO_1 R689 0_0402_5% PCH_SPI_MISO	U3	SPI_MISO			

COUGARPOINT_FCBGA989~D

R389 37.4_0402_1% +1.05VS_PCH

R388 49.9_0402_1% +1.05VS_PCH

R650 750_0402_1%

No use PH 10K +3VS

GPIO19 has internal Pull up

U40

+3VSO R699 3.3K_0402_5% R700 3.3K_0402_5%

PCH_SPI_CS0#_1 SPI_WP1# SPI_HOLD1#

CS#	1	VCC	8
WP#	3	SCLK	6
HOLD#	7	SI	5
GND	4	SO	2

+3VS

PCH_SPI_CLK_1 PCH_SPI_MOSI_1 PCH_SPI_MISO_1

MX25L3206EM2I-12G SOP 8P

SA000041P00

SPI ROM FOR ME (4MB)

Footprint 200mil

+RTCCONN

+CHGRTC

R644 1K_0402_5%

20mil

+RTCCONN_R

D30 DAN202UT106_SC70-3

20mil

+RTCVCC

C761 0.1U_0402_16V4Z

JBATT1

SUYIN_060003HA002G202ZL

CONN@

SERIRQ R403 10K_0402_5%

PCH_SATALED# R662 10K_0402_5%

+3VS

R687 10K_0402_5%

PCH_GPIO21

R688 @ 10K_0402_5%

Switchable Graph	
	GPIO21
Switchable	0
* Non SG	1

R674 4.7K_0402_5% @

PCH_GPIO19

Debug Port DG 1.2 PH 4.7K +3VS

Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
-	1	0
* SPI	1	1

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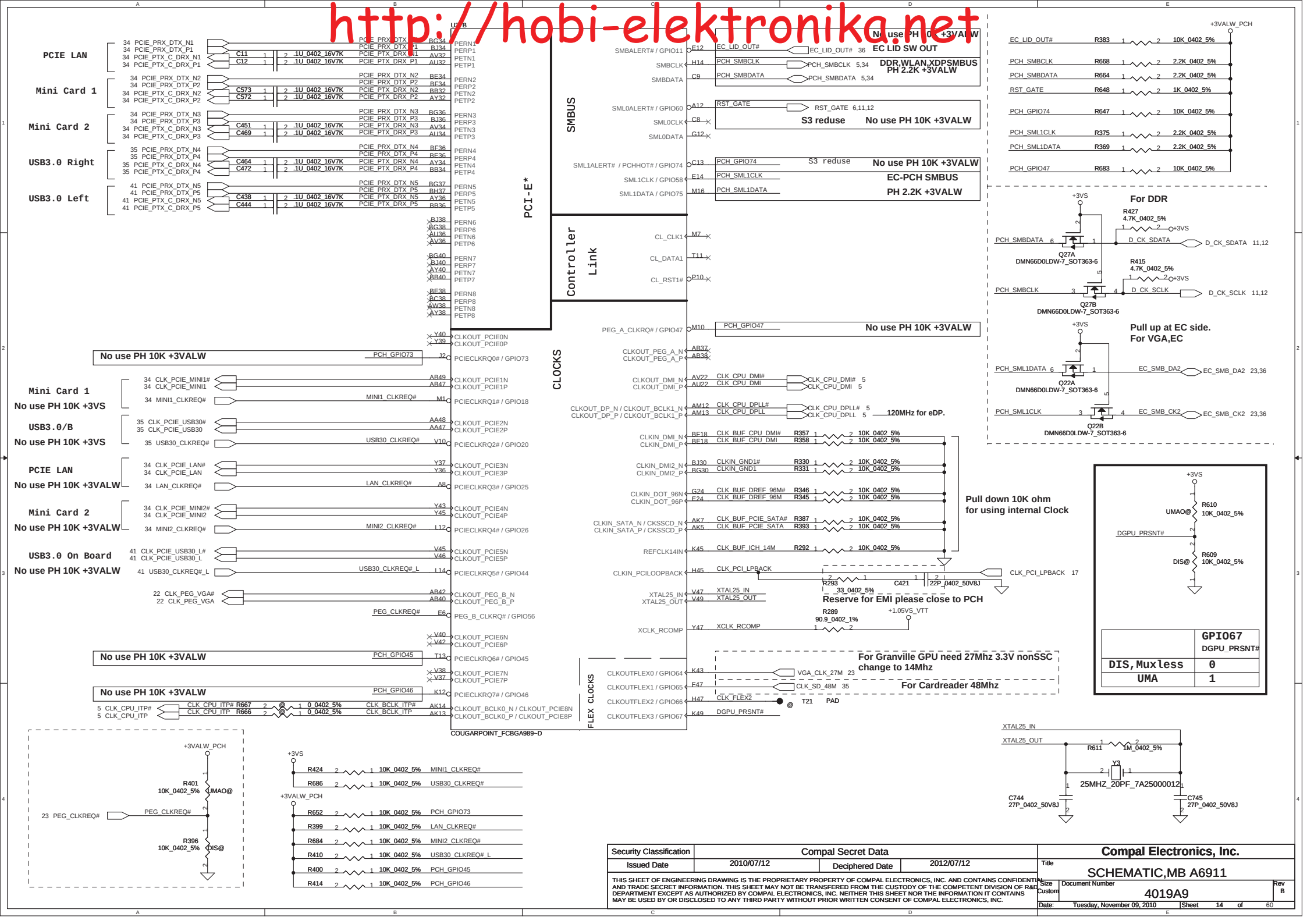
Size: Custom	Document Number: 4019A9
Rev: B	
Date: Tuesday, November 09, 2010	Sheet 13 of 60



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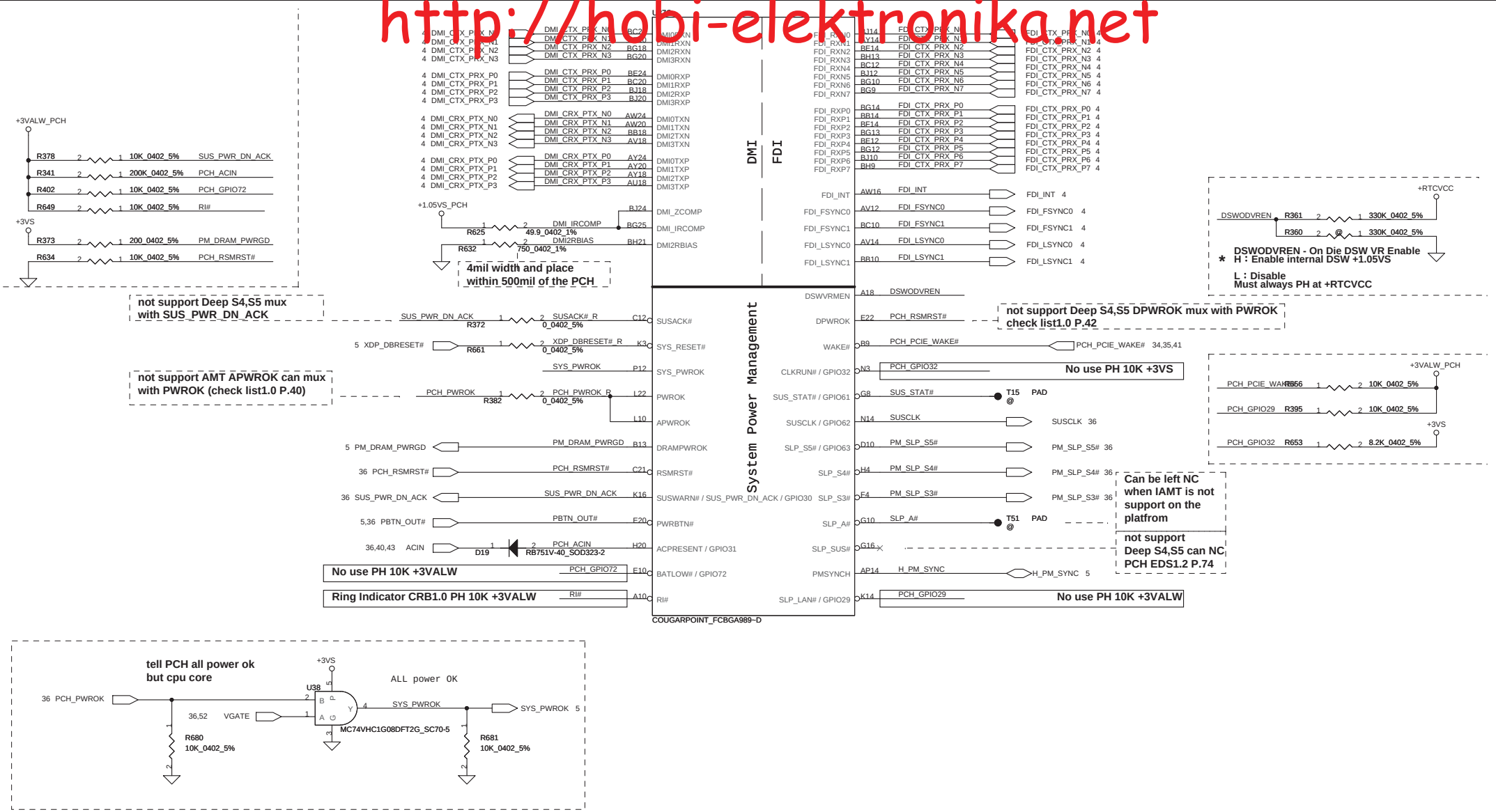
Size: Custom | Document Number: 4019A9 | Rev: B

Date: Tuesday, November 09, 2010 | Sheet 14 of 60



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Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.			
Title	SCHEMATIC,MB A6911		
Size: Custom	Document Number: 4019A9		Rev: B
Date: Tuesday, November 09, 2010	Sheet 15 of 60		

UMA Panel Backlight ON/OFF

23,36 ENBKL — ENBKL — R612 2 — 1 0_0402_5% — IGPU_BKLT_EN

UMA@

PD 100K at EC side

UMA LVDS DDC

+3VS

R259 1 — 2 2.2K_0402_5% CTRL_CLK (UMA@)

R260 1 — 2 2.2K_0402_5% CTRL_DATA (UMA@)

UMA CRT DDC

+3VS

R268 1 — 2 2.2K_0402_5% PCH_CRT_CLK (UMA@)

R269 1 — 2 2.2K_0402_5% PCH_CRT_DATA (UMA@)

UMA CRT RGB

R606 1 — 2 150_0402_1% PCH_CRT_B (UMA@)

R607 1 — 2 150_0402_1% PCH_CRT_G (UMA@)

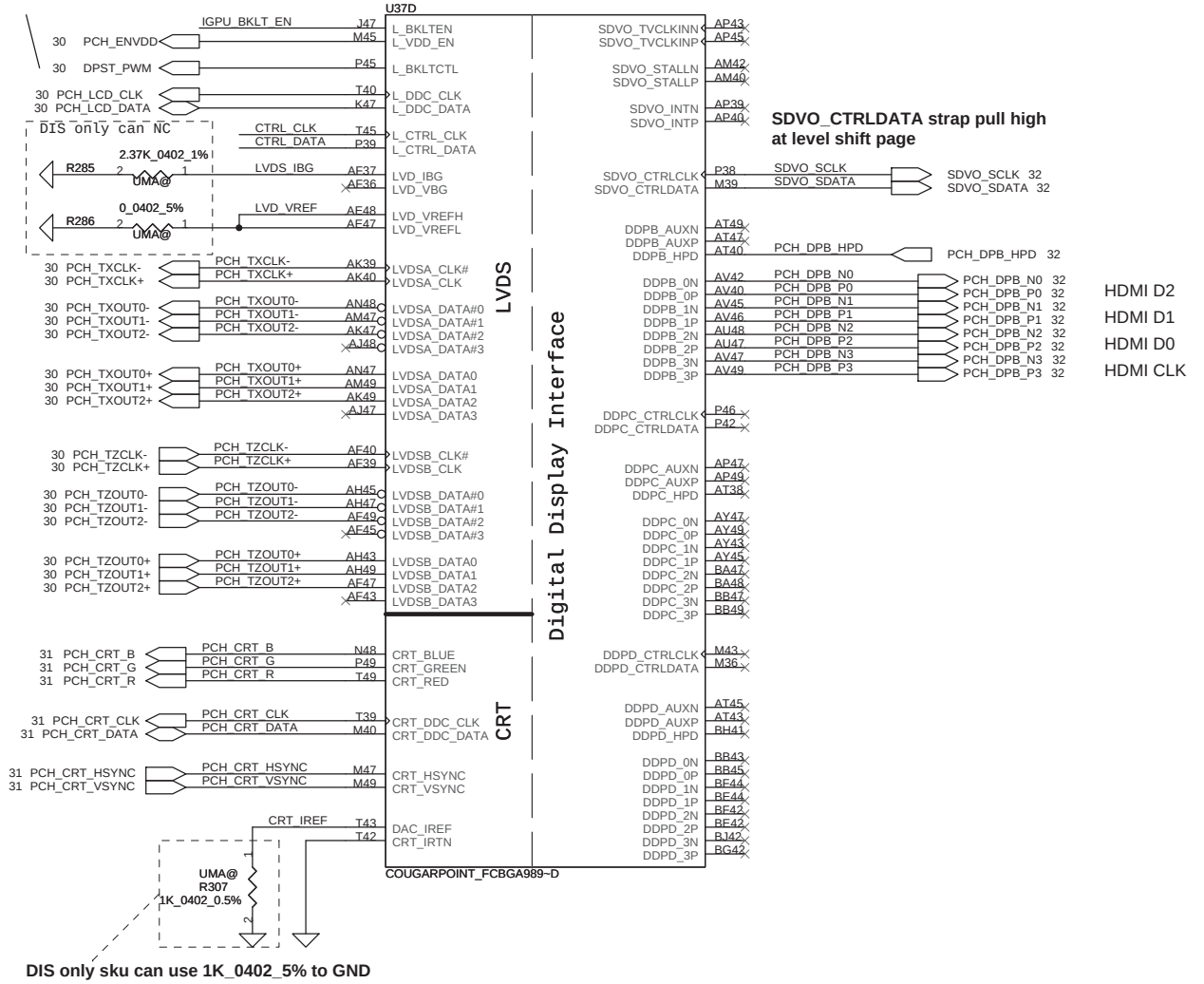
R608 1 — 2 150_0402_1% PCH_CRT_R (UMA@)

Check list1.0 P.55 disable Graphics
ALL Can NC
but DAC_IREF still need PD

LVDS disable:
DATA/Clock/Control an NC
VCC_TX_LVDS,VCCA_LVDS PD to GND

CRT disable:
DATA/Clock/Control an NC
VCCADAC connect to +3VS

Pull high at LVDS conn side.



SDVO_CTRLDATA strap pull high at level shift page

SDVO_SCLK — SDVO_SCLK 32

SDVO_SDATA — SDVO_SDATA 32

PCH_DPB_HPD — PCH_DPB_HPD 32

PCH_DPB_N0 — PCH_DPB_N0 32 — HDMI D2

PCH_DPB_P0 — PCH_DPB_P0 32

PCH_DPB_N1 — PCH_DPB_N1 32 — HDMI D1

PCH_DPB_P1 — PCH_DPB_P1 32

PCH_DPB_N2 — PCH_DPB_N2 32 — HDMI D0

PCH_DPB_P2 — PCH_DPB_P2 32

PCH_DPB_N3 — PCH_DPB_N3 32 — HDMI CLK

PCH_DPB_P3 — PCH_DPB_P3 32

DIS only sku can use 1K_0402_5% to GND

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

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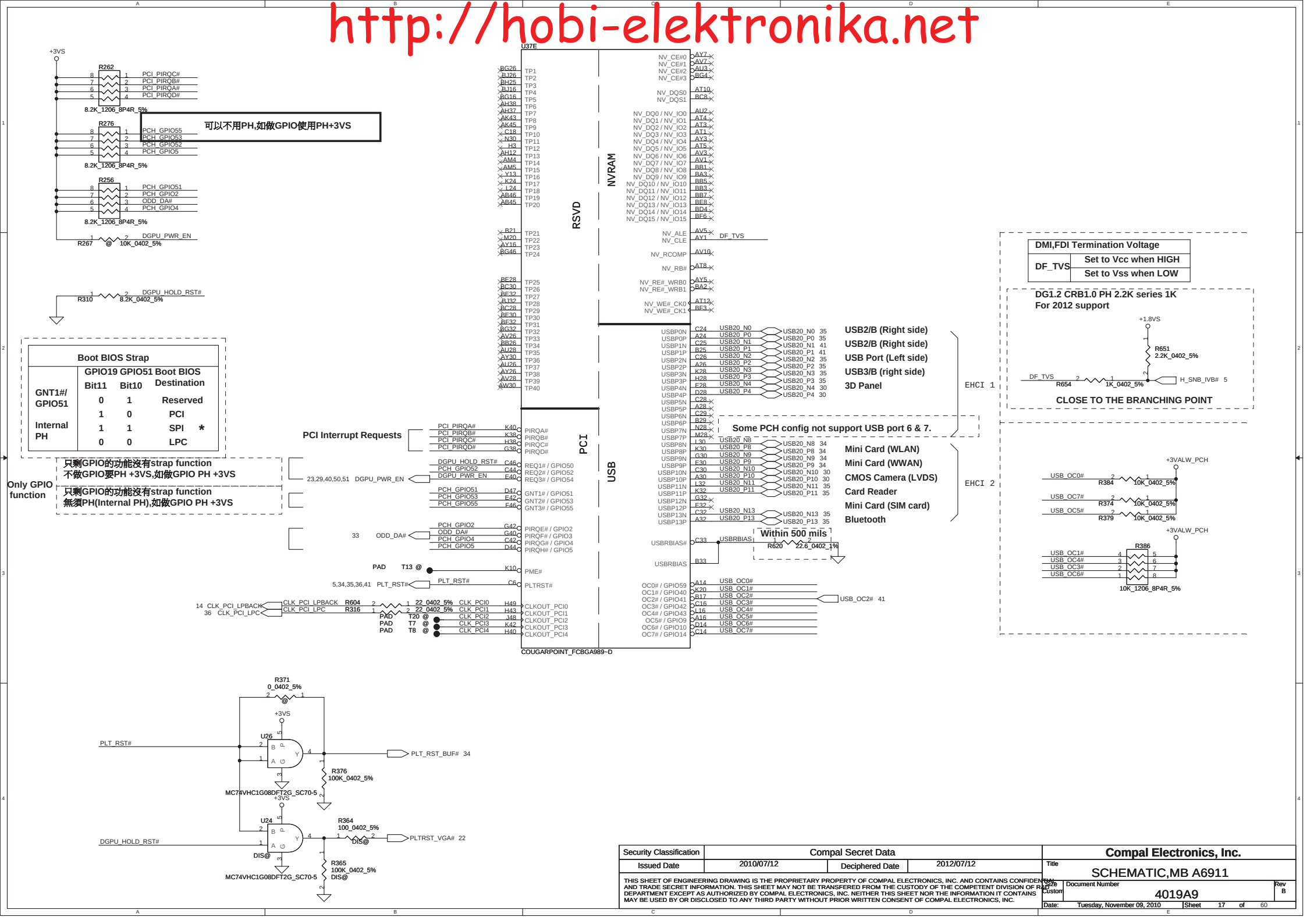
Title: SCHEMATIC,MB A6911

Size: Custom | Document Number: 4019A9 | Rev: B

Date: Tuesday, November 09, 2010 | Sheet 16 of 60



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.	
Title	SCHEMATIC,MB A6911
Size: Custom	Document Number: 4019A9
Rev	B
Date: Tuesday, November 09, 2010	Sheet 17 of 60

HDA_SYNC PH(PLL =+1.5VS)

GPIO28

On-Die PLL Voltage Regulator

This signal has a weak internal pull up
*** H : On-Die PLL voltage regulator enable**
L : On-Die PLL Voltage Regulator disable

+3VALW_PCH — R422 4.7K_0402_5% — PCH_GPIO28 — R417 1K_0402_5% — Debug Port DG 1.2 PH 4.7K +3VALW_PCH

Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal
No use PD to GND Check list1.0 P.70

R362 10K_0402_5% PCH_GPIO27

+3VS — R413 200K_0402_5% ODD_DETECT# — R370 200K_0402_5% WWAN_OFF#

SATA2GP/GPIO36 & SATA3GP/GPIO37
Sampled at Rising edge of PWROK.
Weak internal pull-down.
(weak internal pull-down is disabled after PLTRST# de-asserts)
NOTE: This signal should NOT be pulled high when strap is sampled

+3VS
R406 10K_0402_5% PCH_GPIO0
R614 10K_0402_5% WL_EN#
R326 10K_0402_5% DGPU_HPD_INT#
R663 10K_0402_5% PCH_GPIO16
R305 10K_0402_5% DGPU_PWROK
R412 10K_0402_5% PCH_GPIO22
R428 10K_0402_5% PCH_GPIO39
R675 10K_0402_5% BT_ON#
R679 10K_0402_5% PCH_GPIO48
R404 10K_0402_5% WL_OFF#

+3VALW_PCH
R398 10K_0402_5% PCH_GPIO24
R657 10K_0402_5% PCH_GPIO12
R391 1K_0402_5% SMIB
R397 10K_0402_5% PCH_GPIO57

+3VS — R324 10K_0402_5% — ODD_EN#

Fan Tachometer Inputs
TACH1~7 only on server can insted to GPIO

+3VS — @R615 10K_0402_5% PCH_GPIO71 — @R616 10K_0402_5% PCH_GPIO69 — @R617 10K_0402_5% PCH_GPIO70
R618 10K_0402_5% — R619 10K_0402_5% — R621 10K_0402_5%

Project ID	GPIO69	GPIO70	GPIO71
* P7YE0	0	0	0
x	0	0	1
x	0	1	0
x	0	1	1
x	1	0	0
x	0	0	1
x	0	1	0
x	0	1	1
x	1	0	0
x	1	0	1
x	1	1	0
x	1	1	1

U37F

No use PH 10K +3VS		PCH_GPIO0	T7	BMBUSY# / GPIO0
No use PH 10K +3VS	35 WL_EN#	WL_EN#	A42	TACH1 / GPIO1
No use PH 10K +3VS	32 DGPU_HPD_INT#	DGPU_HPD_INT#	H36	TACH2 / GPIO6
	36 EC_SCI#	EC_SCI#	E38	TACH3 / GPIO7
	36 EC_SMI#	EC_SMI#	C10	GPIO8
No use PH +3VALW		PCH_GPIO12	C4	LAN_PHY_PWR_CTRL / GPIO12
USB3.0 System management Interrupt signal "SMI#".	35,41 SMIB	SMIB	G2	GPIO15
No use PH +3VS		PCH_GPIO16	U2	SATA4GP / GPIO16
	29,49 VGA_PWROK — R304 0_0402_5%	DGPU_PWROK	D40	TACH0 / GPIO17
No use PH 10K +3VS		PCH_GPIO22	T5	SCLOCK / GPIO22
CRB1.0 PH 10K +3VALW		PCH_GPIO24	E8	GPIO24 / MEM_LED
No use PD 10K to GND		PCH_GPIO27	E16	GPIO27
No use PH 10K +3VALW		PCH_GPIO28	P8	GPIO28
No use PH 10K +3VS BT ON/OFF	34,35 BT_ON#	BT_ON#	K1	STP_PCI# / GPIO34
No use can NC	PAD T16 @	PCH_GPIO35	K4	GPIO35
Can't PH	33 ODD_DETECT#	ODD_DETECT#	V8	SATA2GP / GPIO36
Can't PH	34 WWAN_OFF#	WWAN_OFF#	M5	SATA3GP / GPIO37
No use PH 10K +3VS Optimus(L)/ non optimus(H)		OPTIMUS_EN#	N2	SLOAD / GPIO38
No use PH 10K +3VS		PCH_GPIO39	M3	SDATAOUT0 / GPIO39
No use PH 10K +3VS		PCH_GPIO48	V13	SDATAOUT1 / GPIO48
SATA5GP&TEMP_ALERT# CRB PH 10K +3VS	WL_OFF#	WL_OFF#	V3	SATA5GP / GPIO49
No use PH +3VALW or PD to GND		PCH_GPIO57	D6	GPIO57

GPIO

C40	ODD_EN#	ODD_EN# 33	
B41	PCH_GPIO69		TACH4 / GPIO68
C41	PCH_GPIO70		TACH5 / GPIO69
A40	PCH_GPIO71		TACH6 / GPIO70
			TACH7 / GPIO71

CPU/MISC

	+3VS — R419 10K_0402_5%	
P4	A20GATE	GATEA20 36
AU16	PECI	IPCH_PECI_R — R248 0_0402_5% — H_PECI 5,36
P5	RCIN#	EC_KBRST# — EC_KBRST# 36
AY11	PROCPWRGD	H_CPUPWRGD 5
AY10	THRMTRIP#	PCH_THRMTRIP#_R — R385 390_0402_5% — H_THRMTRIP# — H_THRMTRIP# 5
T14	INIT3_3V#	

PECI CPU-EC
CTRL+ALT+DEL
non CPU power ok
130c shut sown

INIT3_3V Checklist1.0 P.59
This signal has weak internal PU, can't pull low,leave NC

NC_1	AH8	
NC_2	AK11	
NC_3	AH10	
NC_4	AK10	
NC_5	P37	

TS_VSS1~4
PD to GND

+3VS — EC_KBRST# — R420 10K_0402_5%

NCTF

PAD T47 @	A4	VSS_NCTF_1	
PAD T30 @	A44	VSS_NCTF_2	
PAD T28 @	A45	VSS_NCTF_3	
PAD T27 @	A46	VSS_NCTF_4	
PAD T49 @	A5	VSS_NCTF_5	
PAD T46 @	A6	VSS_NCTF_6	
PAD T50 @	B3	VSS_NCTF_7	
PAD T26 @	B47	VSS_NCTF_8	
PAD T43 @	BD1	VSS_NCTF_9	
PAD T17 @	BD49	VSS_NCTF_10	
PAD T44 @	BE1	VSS_NCTF_11	
PAD T23 @	BE49	VSS_NCTF_12	
PAD T45 @	BE1	VSS_NCTF_13	
PAD T18 @	BE49	VSS_NCTF_14	
	BG2	VSS_NCTF_15	@T38 PAD
	BG48	VSS_NCTF_16	@T24 PAD
	BH3	VSS_NCTF_17	@T37 PAD
	BH47	VSS_NCTF_18	@T19 PAD
	BJ4	VSS_NCTF_19	@T36 PAD
	BJ44	VSS_NCTF_20	@T31 PAD
	BJ45	VSS_NCTF_21	@T29 PAD
	BJ46	VSS_NCTF_22	@T25 PAD
	BJ5	VSS_NCTF_23	@T35 PAD
	BJ6	VSS_NCTF_24	@T34 PAD
	C2	VSS_NCTF_25	@T39 PAD
	C48	VSS_NCTF_26	
	D1	VSS_NCTF_27	@T40 PAD
	D49	VSS_NCTF_28	@T22 PAD
	F1	VSS_NCTF_29	@T41 PAD
	F49	VSS_NCTF_30	
	F1	VSS_NCTF_31	@T42 PAD
	F49	VSS_NCTF_32	

COUGARPOINT_FCBGA989~D

+3VS — R429 NOMUXL@ 10K_0402_5% OPTIMUS_EN# — R430 MUXL@ 10K_0402_5%

	GPIO38 OPTIMUS_EN#
* Muxless	0
nonMuxless	1

GPIO24 Unmultiplexed
NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.
CRB1.0 PH10K to +3VALW

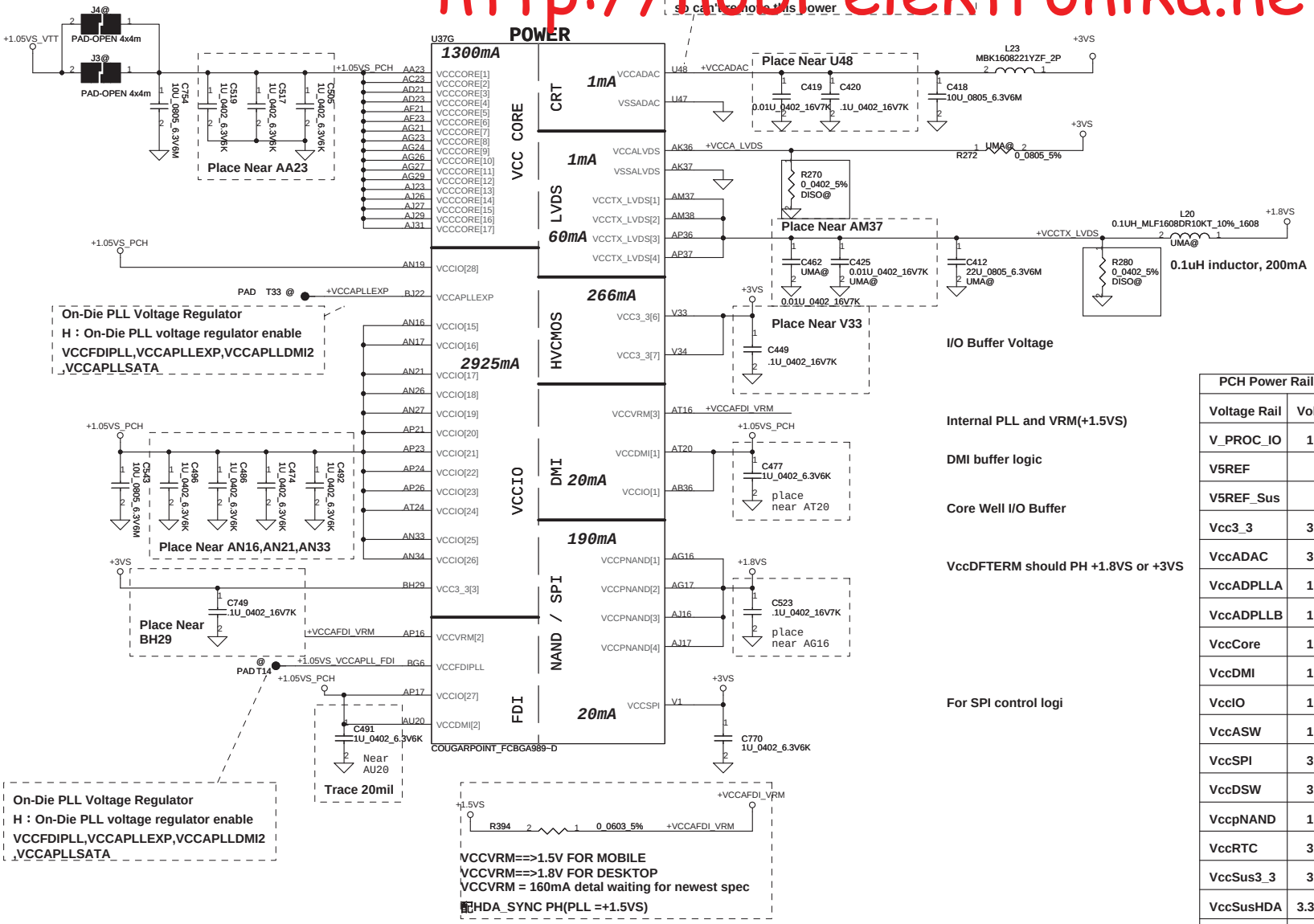
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: SCHEMATIC,MB A6911

Size: Custom | Document Number: 4019A9 | Rev: B

Date: Tuesday, November 09, 2010 | Sheet 18 of 60



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

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Title: SCHEMATIC,MB A6911

Size: Custom | Document Number: 4019A9 | Rev: B

Date: Tuesday, November 09, 2010 | Sheet 19 of 60

VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

+3VS
R329 0_0805_5%
L26 10UH_LB2012T100MR_20%
C465 10U_0805_10V4Z
C460 1U_0402_6.3V6K
Near T38
+3VS_VCC_CLKF33

+1.05V analog internal clock PLL Can NC

Not support Deep S4,S5 connect to +3VALW

suppied by internal 1.05V VR must NC

GPIO28
On-Die PLL Voltage Regulator
H：On-Die PLL voltage regulator enable
VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2 ,VCCAPLLSATA

+1.05VS_PCH
R273 0_0603_5%
+VCCACLK
+3VALW_PCH
C520 .1U_0402_16V7K
Near T16

U37J
POWER

AD49 VCCACLK
T16 VCCDSW3_3
V12 DCPSUSBYP 3mA
T38 VCC3_3[5]
BH23 VCCAPLLDMI2 119mA
AL29 VCCIO[14]
AL24 DCPSUS[3]
AA19 VCCASW[1] 1010mA
AA21 VCCASW[2]
AA24 VCCASW[3]
AA26 VCCASW[4]
AA27 VCCASW[5]
AA29 VCCASW[6]
AA31 VCCASW[7]
AC26 VCCASW[8]
AC27 VCCASW[9]
AC29 VCCASW[10]
AC31 VCCASW[11]
AD29 VCCASW[12]
AD31 VCCASW[13]
W21 VCCASW[14]
W23 VCCASW[15]
W24 VCCASW[16]
W26 VCCASW[17]
W29 VCCASW[18]
W31 VCCASW[19]
W33 VCCASW[20]
N16 DCPRTC
Y49 VCCVRM[4]
BD47 VCCADPLLA 80mA
BF47 VCCADPLLB 80mA
AF17 VCCIO[7]
AF33 VCCIO[8]
AG34 VCCIO[9]
AG34 VCCIO[11] 55mA
AG33 VCCIO[10] 95mA
V16 DCPSST
T17 DCPSUS[1]
V19 DCPSUS[2]
BJ8 V_PROC_IO 1mA
A22 VCCRTC

USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
CPU
MISC
RTC
HDA

PAD T12 @ +PCH_VCCDSW
PAD T32 @ +VCCAPLL_CPY_PCH
+1.05VS_PCH
PAD T9 @ +VCCSUS1
+3VS_VCC_CLKF33

+1.05VS_PCH
C547 22U_0805_6.3V6M
C552 22U_0805_6.3V6M
C518 1U_0402_6.3V6K
C478 1U_0402_6.3V6K
C513 1U_0402_6.3V6K
Near AA19

+1.05VS_PCH
L48 10UH_LB2012T100MR_20%
C746 220U_6.3V_M
C426 1U_0402_6.3V6K
Near BD47
+1.05VS_VCCA_A_DPL
L49 10UH_LB2012T100MR_20%
C750 220U_6.3V_M
C428 1U_0402_6.3V6K
Near BF47
+1.05VS_VCCA_B_DPL

SGA00001700
220U 2.5V M B2
ESR 35mohm@100Khz

SF000001580
220U 6.3V H6 OS-CON
ESR 15mohm@100Khz

Near M6
C521 1U_0402_16V7K
+VCCRTCEXT
+VCCAFDI_VRM

+1.05VS_PCH
C524 1U_0402_6.3V6K Place near AF17
C476 1U_0402_6.3V6K Place near AG33
+1.05VS_PCH
C467 1U_0402_6.3V6K
Place near AF33, AF34,AG34

+1.05VS_PCH
Near V16
C526 1U_0402_16V7K
+VCCSST

PAD T10 @
+1.05VM_VCCSUS

suppied by internal 1.05V VR Must NC

isolation between SSC (AG33) and DIFFCLKN(AF33,AF34,AG34)
18mil width(DIFFCLKN)
10mil (SSC)

+1.05VS_PCH
C554 4.7U_0603_6.3V6K
C537 .1U_0402_16V7K
C541 .1U_0402_16V7K
Place near BJ8

+RTCVCC
C493 1U_0402_6.3V6K
C494 1U_0402_16V7K
C505 1U_0402_16V7K
Near A22

COUGARPOINT_FCBGA989-D

VCCIO[29] N26
VCCIO[30] P26
VCCIO[31] P28
VCCIO[32] T27
VCCIO[33] T29
+1.05VS_PCH
C468 1U_0402_6.3V6K
Near N26

VCCSUS3_3[7] T23
VCCSUS3_3[8] T24
VCCSUS3_3[9] V23
VCCSUS3_3[10] V24
VCCSUS3_3[6] P24
+3VALW_PCH
C490 .1U_0402_16V7K
Near T23
C497 .1U_0402_16V7K
Near T24

VCCIO[34] T26
+1.05VS_PCH
Near M26
V5REF_SUS M26
+PCH_V5REF_SUS
C484 0.1U_0603_25V7K
DCPSUS[4] AN23
+VCCA_USBSUS T11 PAD @
VCCSUS3_3[1] AN24
+3VALW_PCH
suppied by internal 1.05V VR Must NC

+3VALW_PCH
+5VALW
D16 RB751V-40_SOD323-2
R334 100_0402_5%

+3VS
+5VS
D14 RB751V-40_SOD323-2
R321 100_0402_5%

V5REF P34
+PCH_V5REF_RUN
C470 1U_0603_10V6K
Near P34

VCCSUS3_3[2] N20
VCCSUS3_3[3] N22
VCCSUS3_3[4] P20
VCCSUS3_3[5] P22
+3VALW_PCH
C501 1U_0402_6.3V6K
Near N20

VCC3_3[1] AA16
VCC3_3[8] W16
VCC3_3[4] T34
+3VS
C771 1U_0402_16V7K Place near AJ2
C522 1U_0402_16V7K Place near AA16,W16
C471 1U_0402_16V7K Place near T34

VCC3_3[2] AJ2
+1.05VS_PCH
VCCIO[5] AF13
VCCIO[12] AH13
VCCIO[13] AH14
VCCIO[6] AF14
Near AH13,AH14,AF13
C533 1U_0402_6.3V6K

VCCAPLLSATA AK1
+VCCSATAPLL
@ T48 PAD
VCCVRM[1] AF11
+VCCAFDI_VRM

GPIO28
On-Die PLL Voltage Regulator
H：On-Die PLL voltage regulator enable
VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2 ,VCCAPLLSATA

VCCIO[2] AC16
VCCIO[3] AC17
VCCIO[4] AD17
+1.05VS_PCH
Near AC16
C482 1U_0402_6.3V6K

VCCASW[22] T21
VCCASW[23] V21
VCCASW[21] T19
+VCCME_22 R416 0_0603_5%
+VCCME_23 R421 0_0603_5%
+VCCME_21 R426 0_0603_5%
+1.05VS_PCH

VCCSUSHDA P32
+VCCSUSHDA R327 0_0603_5%
+3VALW_PCH
Need +3VALW and 0.1U close PCH
C473 0.1U_0402_16V4Z
Near P32

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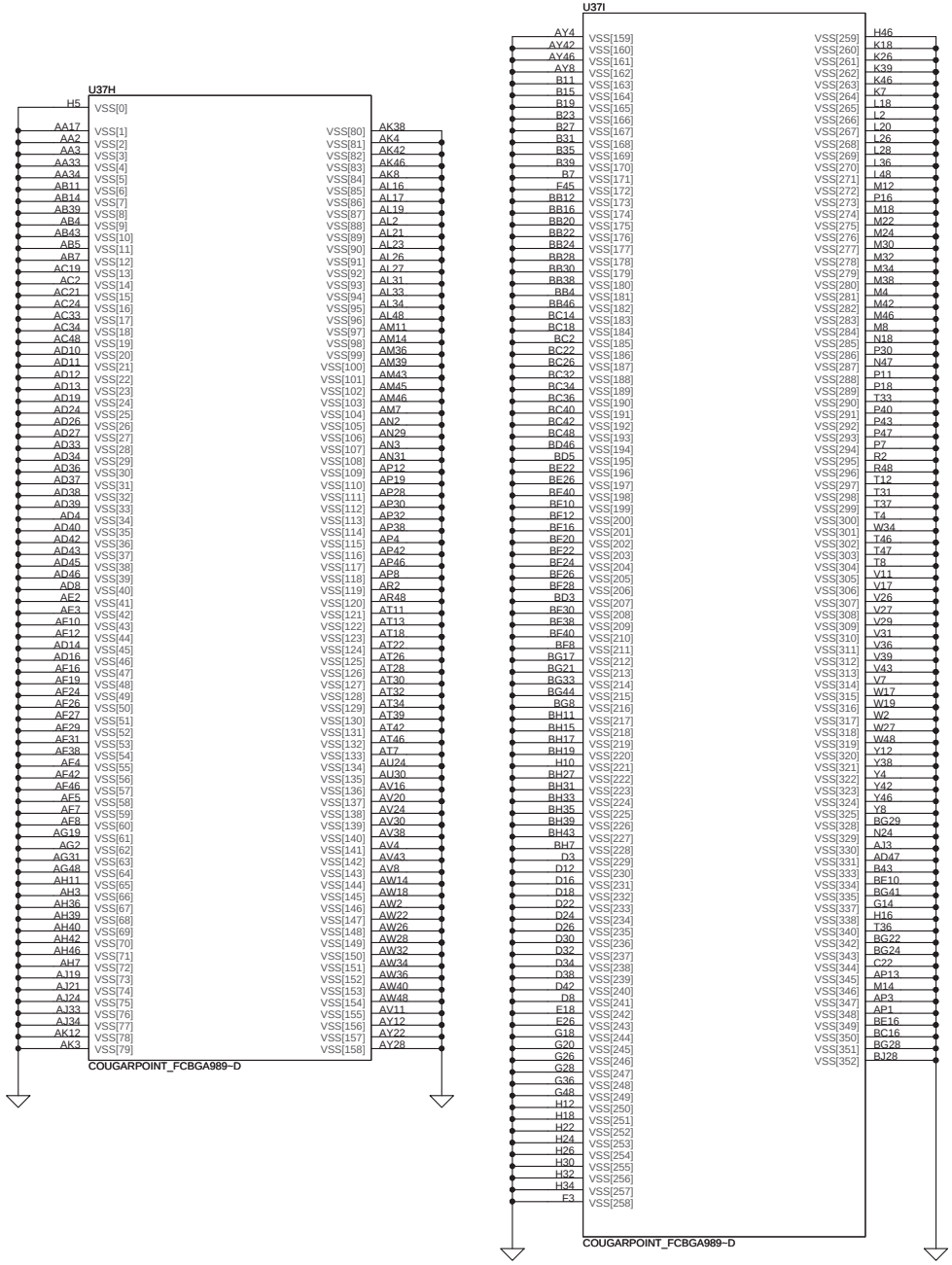
Title: SCHEMATIC,MB A6911

Size: Custom | Document Number: 4019A9 | Rev: B

Date: Tuesday, November 09, 2010 | Sheet 20 of 60



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Title: SCHEMATIC,MB A6911

Size: Custom | Document Number: 4019A9 | Rev: B

Date: Tuesday, November 09, 2010 | Sheet 21 of 60

GFX PCIE LANE REVERSAL

4 PEG_GTX_HRX_N[0..15]
4 PEG_GTX_HRX_P[0..15]
4 PEG_HTX_C_GRX_N[0..15]
4 PEG_HTX_C_GRX_P[0..15]

U30A

PEG_HTX_C_GRX_P0 / PEG_HTX_C_GRX_N0 — AA38 / Y37 — PCIE_RX0P / PCIE_RX0N
PEG_HTX_C_GRX_P1 / PEG_HTX_C_GRX_N1 — Y35 / W36 — PCIE_RX1P / PCIE_RX1N
PEG_HTX_C_GRX_P2 / PEG_HTX_C_GRX_N2 — W38 / V37 — PCIE_RX2P / PCIE_RX2N
PEG_HTX_C_GRX_P3 / PEG_HTX_C_GRX_N3 — V35 / U36 — PCIE_RX3P / PCIE_RX3N
PEG_HTX_C_GRX_P4 / PEG_HTX_C_GRX_N4 — U38 / T37 — PCIE_RX4P / PCIE_RX4N
PEG_HTX_C_GRX_P5 / PEG_HTX_C_GRX_N5 — T35 / R36 — PCIE_RX5P / PCIE_RX5N
PEG_HTX_C_GRX_P6 / PEG_HTX_C_GRX_N6 — R38 / P37 — PCIE_RX6P / PCIE_RX6N
PEG_HTX_C_GRX_P7 / PEG_HTX_C_GRX_N7 — P35 / N36 — PCIE_RX7P / PCIE_RX7N
PEG_HTX_C_GRX_P8 / PEG_HTX_C_GRX_N8 — N38 / M37 — PCIE_RX8P / PCIE_RX8N
PEG_HTX_C_GRX_P9 / PEG_HTX_C_GRX_N9 — M35 / L36 — PCIE_RX9P / PCIE_RX9N
PEG_HTX_C_GRX_P10 / PEG_HTX_C_GRX_N10 — L38 / K37 — PCIE_RX10P / PCIE_RX10N
PEG_HTX_C_GRX_P11 / PEG_HTX_C_GRX_N11 — K35 / J36 — PCIE_RX11P / PCIE_RX11N
PEG_HTX_C_GRX_P12 / PEG_HTX_C_GRX_N12 — J38 / H37 — PCIE_RX12P / PCIE_RX12N
PEG_HTX_C_GRX_P13 / PEG_HTX_C_GRX_N13 — H35 / G36 — PCIE_RX13P / PCIE_RX13N
PEG_HTX_C_GRX_P14 / PEG_HTX_C_GRX_N14 — G38 / F37 — PCIE_RX14P / PCIE_RX14N
PEG_HTX_C_GRX_P15 / PEG_HTX_C_GRX_N15 — F35 / E37 — PCIE_RX15P / PCIE_RX15N

PCI EXPRESS INTERFACE

PCIE_TX0P / PCIE_TX0N — Y33 / Y32 — PEG_GTX_HRX_P0 / PEG_GTX_HRX_N0
PCIE_TX1P / PCIE_TX1N — W33 / W32 — PEG_GTX_HRX_P1 / PEG_GTX_HRX_N1
PCIE_TX2P / PCIE_TX2N — U33 / U32 — PEG_GTX_HRX_P2 / PEG_GTX_HRX_N2
PCIE_TX3P / PCIE_TX3N — U30 / U29 — PEG_GTX_HRX_P3 / PEG_GTX_HRX_N3
PCIE_TX4P / PCIE_TX4N — T33 / T32 — PEG_GTX_HRX_P4 / PEG_GTX_HRX_N4
PCIE_TX5P / PCIE_TX5N — T30 / T29 — PEG_GTX_HRX_P5 / PEG_GTX_HRX_N5
PCIE_TX6P / PCIE_TX6N — P33 / P32 — PEG_GTX_HRX_P6 / PEG_GTX_HRX_N6
PCIE_TX7P / PCIE_TX7N — P30 / P29 — PEG_GTX_HRX_P7 / PEG_GTX_HRX_N7
PCIE_TX8P / PCIE_TX8N — N33 / N32 — PEG_GTX_HRX_P8 / PEG_GTX_HRX_N8
PCIE_TX9P / PCIE_TX9N — N30 / N29 — PEG_GTX_HRX_P9 / PEG_GTX_HRX_N9
PCIE_TX10P / PCIE_TX10N — L33 / L32 — PEG_GTX_HRX_P10 / PEG_GTX_HRX_N10
PCIE_TX11P / PCIE_TX11N — L30 / L29 — PEG_GTX_HRX_P11 / PEG_GTX_HRX_N11
PCIE_TX12P / PCIE_TX12N — K33 / K32 — PEG_GTX_HRX_P12 / PEG_GTX_HRX_N12
PCIE_TX13P / PCIE_TX13N — J33 / J32 — PEG_GTX_HRX_P13 / PEG_GTX_HRX_N13
PCIE_TX14P / PCIE_TX14N — K30 / K29 — PEG_GTX_HRX_P14 / PEG_GTX_HRX_N14
PCIE_TX15P / PCIE_TX15N — H33 / H32 — PEG_GTX_HRX_P15 / PEG_GTX_HRX_N15

CLOCK
14 CLK_PEG_VGA — AB35 — PCIE_REFCLKP
14 CLK_PEG_VGA# — AA36 — PCIE_REFCLKN

CALIBRATION
PCIE_CALRP — Y30 — R153 1 VGA@ 2 1.27K_0402_1%
PCIE_CALRN — Y29 — R156 1 VGA@ 2 2K_0402_1% — +1.0VSDGPU

For M96, AH16 is NC
For Boardway,Madison,Park, AH16 must connect to GND
R141 2 VGA@ 1 10K_0402_5% — AH16 — PWRGOOD

17 PLTRST_VGA# — AA30 — PERSTB

2160809000A11SEYMOU_FCBGA962
SEYM@

U30G

LVDS CONTROL
VARY_BL — AK27
DIGON — AJ27
R133 10K_0402_5% 1 VGA@ 2
R127 1 VGA@ 2 10K_0402_5%
VGA_PNL_PWM 30
ENVDD 30

LCD PWM (pulse width modulated) output to adjust LCD brightness
Active High ,external PD need

Controls panel digital power on/off.
Active High ,external PD need

TXCLK_UP_DPF3P / TXCLK_UN_DPF3N — AK35 / AL36 — VGA_TZCLK+ / VGA_TZCLK- — VGA_TZCLK+ 30 / VGA_TZCLK- 30
TXOUT_U0P_DPF2P / TXOUT_U0N_DPF2N — AJ38 / AK37 — VGA_TZOUT0+ / VGA_TZOUT0- — VGA_TZOUT0+ 30 / VGA_TZOUT0- 30
TXOUT_U1P_DPF1P / TXOUT_U1N_DPF1N — AH35 / AJ36 — VGA_TZOUT1+ / VGA_TZOUT1- — VGA_TZOUT1+ 30 / VGA_TZOUT1- 30
TXOUT_U2P_DPF0P / TXOUT_U2N_DPF0N — AG38 / AH37 — VGA_TZOUT2+ / VGA_TZOUT2- — VGA_TZOUT2+ 30 / VGA_TZOUT2- 30
TXOUT_U3P / TXOUT_U3N — AE35 / AG36

Display Port F config

LVTMDP

eDP
DP3
DP2
DP1
DP0

TXCLK_LP_DPE3P / TXCLK_LN_DPE3N — AP34 / AR34 — VGA_TXCLK+ / VGA_TXCLK- — VGA_TXCLK+ 30 / VGA_TXCLK- 30
TXOUT_L0P_DPE2P / TXOUT_L0N_DPE2N — AW37 / AU35 — VGA_TXOUT0+ / VGA_TXOUT0- — VGA_TXOUT0+ 30 / VGA_TXOUT0- 30
TXOUT_L1P_DPE1P / TXOUT_L1N_DPE1N — AR37 / AU39 — VGA_TXOUT1+ / VGA_TXOUT1- — VGA_TXOUT1+ 30 / VGA_TXOUT1- 30
TXOUT_L2P_DPE0P / TXOUT_L2N_DPE0N — AP35 / AR35 — VGA_TXOUT2+ / VGA_TXOUT2- — VGA_TXOUT2+ 30 / VGA_TXOUT2- 30
TXOUT_L3P / TXOUT_L3N — AN36 / AP37

Display Port E config

2160809000A11SEYMOU_FCBGA962
SEYM@

Park XT P/N : SA00003M570 (S IC 216-0774009 A11 PARK XT S3 631P C38)
Madision Pro P/N : SA00003M360 (S IC 216-0772000 MADISON PRO FCBGA 0FA)
Seymour XT P/N: SA000047H00 (S IC 216-0809000 A11 SEYMOUR XT M2 0FH)

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Title: SCHEMATIC,MB A6911

Size	Document Number	Rev
Custom	4019A9	B

Date: Tuesday, November 09, 2010 | Sheet 22 of 60

Strap Name		Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNC (GENLK_VSYNC)	VIP Device Strap Enable indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines (Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis diabled 1: Tx de-emphasis enabled	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : (Internal PD) memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. 128 MB 000 b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 256 MB 001 * 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device (Internal PD) 0: Diable, 1: Enable	0
AUD[1] AUD(0)	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

Don't have this strap o...
Whistler and Seymour

External VGA Thermal Sensor

U9 VGA@ ADM1032ARMZ-2REEL_MSOP8
GPU_THERM_D+ 2200P_0402_50V7K C161
VGA_SMB_CK2 VGA_SMB_DA2 THM_ALERT# R130 4.7K_0402_5% +3VSDGPU

+3VSDGPU

NOGRAN@ R492 0_0603_5%
AO3419L_SOT23-3 Q36 100mA
C579 1U_0402_16V7K GRAN@
R478 100K_0402_5% GRAN@
R479 24K_0402_1% GRAN@
DMN66D0LDW-7_SOT363-6 Q35A Q35B
C581 10U_0805_6.3V6M
R485 470_0603_5% GRAN@
R491 0_0402_5% GRAN@
C580 0.1U_0402_16V4Z
17,29,40,50,51 DGPU_PWR_EN
DGPU_PWR_EN# 40,51

Seymour XT

ID3-0	Vender	Size	Freq	P/N	Description	
* 0000	SAM	64*16	800M	SA000035720(S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO		X769
0001						
* 0010	SAM	64*16	900M	SA00004GS10(S IC D3 64M16 K4W1G1646G-BC11 FBGA ABO		X7611
* 0011	HYN	64*16	900M	SA000041S40(S IC D3 64MX16 H5TQ1G63DFR-11C FBGA AB		X7610
0100						
0101	SAM	128*16	800M	SA00003MQ60 (S IC D3 128M16 K4W2G1646C-HC12 FBGA AB		X767
0110						
0111						
1000						
1001						
1010						
1011						
1100	HYN	64*16	800M	SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO		X762
1101	HYN	128*16	800M	SA00003VS10 (S IC D3 128M16 H5TQ2G63BFR-12C FBGA ABO		X768
1110	HYN	64*16	800M	SA0000324G0(S IC D3 64M16 H5TQ1G63DFR-12C FBGA ABO		X761
1111						

Whistler/Granville(PRO)

ID3-0	Vender	Size	Freq	P/N	Description	
* 0000	SAM	64*16	800M	SA000035720(S IC D3 64MX16 K4W1G1646E-HC12 FBGA AB		X7612
0001	SAM	128*16	800M	SA00003MQ60 (S IC D3 128M16 K4W2G1646C-HC12 FBGA AB		X766
* 0010	SAM	64*16	900M	SA00004GS10(S IC D3 64M16 K4W1G1646G-BC11 FBGA ABO		X7614
* 0011	HYN	64*16	900M	SA000041S40(S IC D3 64MX16 H5TQ1G63DFR-11C FBGA AB		X7613
0100						
0101						
0110						
0111						
1000	HYN	64*16	800M	SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO		X764
1001	HYN	128*16	800M	SA00003VS10 (S IC D3 128M16 H5TQ2G63BFR-12C FBGA ABO		X765
1010	HYN	64*16	800M	SA0000324G0(S IC D3 64M16 H5TQ1G63DFR-12C FBGA ABO		X763
1011						
1100						
1101						
1110						
1111						

PD 100K at EC side
DISCRETE ONLY

NC on Park, Robson and Seymour
NC on Park, Robson

Global Swap Lock on Multiple GPUs

Move to DDCCLK_AUX3P,DDCDATA_AUX3N

GPIO0 Power-state indicator.
GPIO1 PCIE transmitter deemphasis enable.
GPIO2 Advertises the PCIe 0:2.5G 1:5G
GPIO3,4 SMBus data/CLK

GPIO5 fast-power reduction:
HW control will cause display disturb
should use SW method control

GPIO6 voltage control signal ,No use can NC

GPIO7 Controls backlight on/off.
Active High ,need external PD

If GPIO22 High ,GPIO 11-13->CFG[0:2]
Config ROM type ,GPU has internal PD

GPIO6,15,16,20
Voltage control signal
GPIO6,15 no use can NC
Thermal monitor interrupt

Critical temperature fault

Reserved

External BIOS device
ON(1)/OFF(0) inter PD

Internal Debug
no use can floating
ON(1)/OFF(0)

Stereo Sync
no use can NC

For ATI Cross fire
no use can NC

Park NC pins

Future ASIC call MLPS.
OLD ASIC is Fan PWM

2160809000A11SEYMOU_FCBGA962
SEYM@

NC on Park, Robson and Seymour

Not share via for other GND

70mA 100mA 10mil AMD ref:120ohm/0.3A

NC on Whistler and Seymour
SM010030010
200ma 120ohm@100mhz DCR 0.2
AMD ref:120ohm/0.3A

Reserved

In Whistler and Seymour, change to GENLK_CLK, GENLK_VSYNC for Global Swap Lock on multiple GPUs

Granville can NC when no use

Back compatibility(Manhattan)

100mA 2mA 10mil

Whistler and Seymour
Except A2VSSQ change to TSVSSQ, others are NC

HDMI

NC on Park, Robson and Seymour

CRT

NC on Park, Robson and Seymour

AMD ref:470ohm/1A
SM010030010
200ma 120ohm@100mhz DCR 0.2
AMD ref:470ohm/1A

20mil 75mA 125mA 10mil 20mA 120ohm/0.3A

HSYN:VSYNC
11: Audio for both DisplayPort and HDMI

AUD Strap

CRT,HDMI DDC

GPIO8 Serial-ROM output from ROM.
GPIO9 Serial-ROM input to ROM.
GPIO10 Serial-ROM clock to ROM.
GPIO22 erternal BIOS-ROM enable

GPIO8,GPIO9,GPIO10 no use can NC
GPIO22
Enable need 3K PH ,no use must NC

If GPIO22 High ,GPIO 11-13->CFG[0:2]
Config ROM type ,GPU has internal PD
If GPIO22 Low ,GPIO 11-13->CFG[0:2]
Config Primary memory-aperture size
CFG[3:0]
128MB 000
256MB 001 *
64MB 010

FLASH ROM
TYPE 1
M25P10-AVMN6P@

External 27MHZ 3.3V CLK

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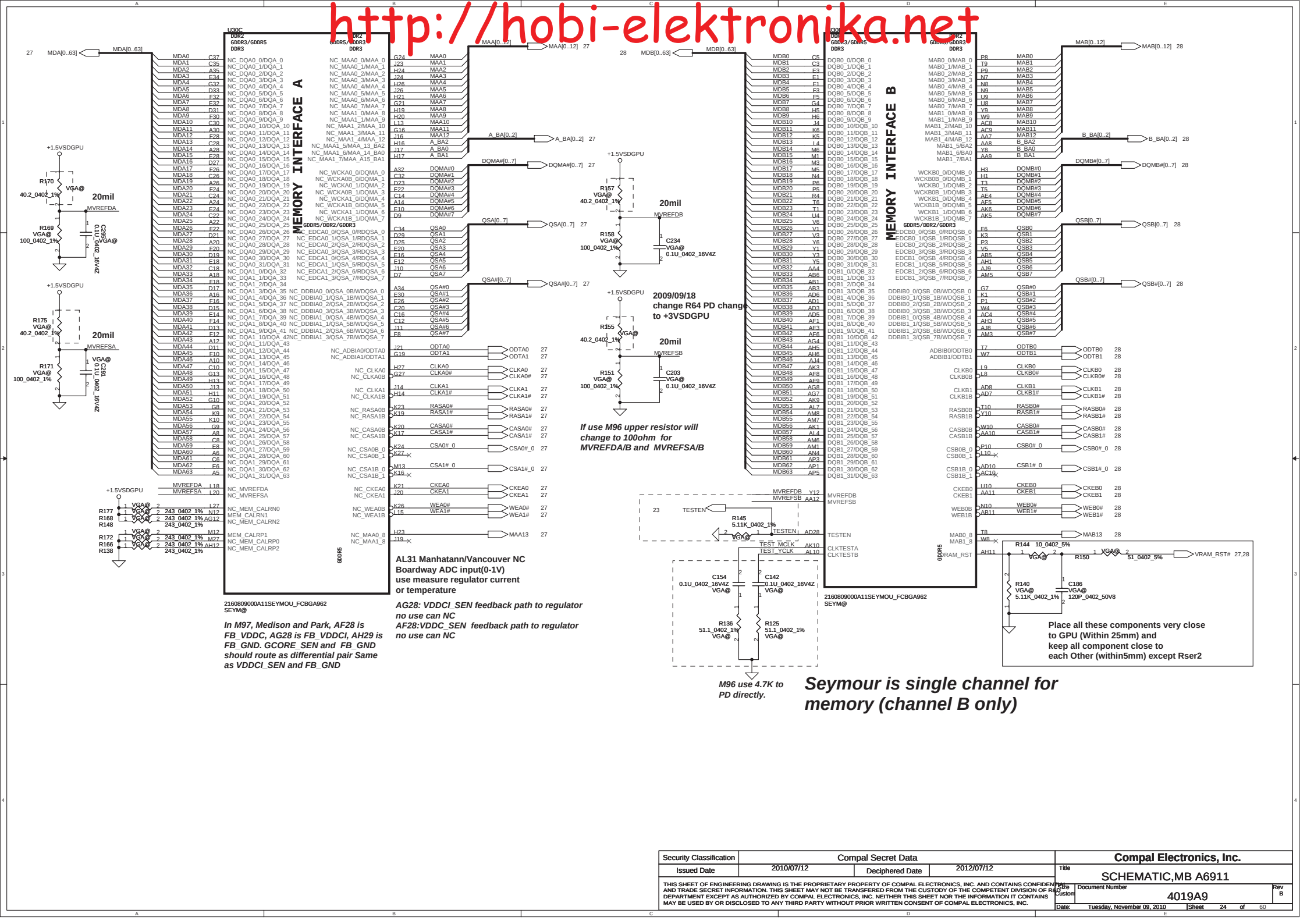

2009/09/18
change R64 PD change to +3VSDGPU

If use M96 upper resistor will change to 100ohm for MVREFDA/B and MVREFSA/B

AL31 Manhatann/Vancouver NC Boardway ADC input(0-1V) use measure regulator current or temperature

AG28: VDDCI_SEN feedback path to regulator no use can NC
AF28:VDDC_SEN feedback path to regulator no use can NC

In M97, Medison and Park, AF28 is FB_VDDC, AG28 is FB_VDDCI, AH29 is FB_GND. GCORE_SEN and FB_GND should route as differential pair Same as VDDCI_SEN and FB_GND

M96 use 4.7K to PD directly.

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within5mm) except Rser2

Seymour is single channel for memory (channel B only)

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Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.			
Title	SCHEMATIC,MB A6911		
Size: Custom	Document Number: 4019A9		Rev: B
Date: Tuesday, November 09, 2010	Sheet 24 of 60		

Seymour/Whistler
PCIE_VDDR,PCIE_VDD can combain to PCIE_VDDR

SM010014520 3000ma 220ohm@100mhz DCR 0.04

40mil

+PCIE_VDDR

L40 VGA@
FBMA-L11-201209-221LMA30T_0805
220ohm/2A

+1.8VSDGPU

+1.0VSDGPU

440mA

PCIE_VDDR/PCIE_PVDD

3400mA 2A

Granville VDDC:47A

+VGA_CORE

Granville PRO VDDC:47A
Madison PRO VDDC+VDDCI=31.3A
Whistler PRO VDDC+VDDCI=24A
SeymourXT VDDC+VDDCI=14.2A
RobsonXT VDDC+VDDCI=12.9A

Seymour/Whistler option
SGA20331E10 S POLY C 330U
2V 9mohm H1.9

Granville option
SGA00004200
S POLY C 470U 2V M D2
LESR4.5M SX H1.9

BOM option at page59

C604 330U_D2_2V_Y NOGRAN@
C591 330U_D2_2V_Y NOGRAN@

+1.5VSDGPU

330U_6.3V_R15M

C718 VGA@

SF000002080
330U 6.3V H5.9
15mohm

SF000002M00 330U 2.5V ESR 16mohm

SM010030010
300ma 120ohm@100mhz DCR 0.3

120ohm/0.3A

L41 VGA@
BLM18AG121SN1D_0603

Ref137-12~ remove Bead

+3VSDGPU

20mil

+VDD_CT

219mA

SM010030010
300ma 120ohm@100mhz DCR 0.3

120ohm/0.3A

L33 VGA@
BLM18AG121SN1D_0603

+VDDR3

10mil

20mil

+VDDR4_5

60mA

170mA

470ohm/1A
SM010030010
200ma 120ohm@100mhz DCR 0.2

L44
BLM18AG121SN1D_0603
VGA@

For M92/M96 only,
Manhattan are NC pin

SM010030010
200ma 120ohm@100mhz DCR 0.2

L34
BLM18AG121SN1D_0603
VGA@

20mil
+MPV_18

10mil
20mil
+SPV_18
+SPV10

150mA
75mA
120mA

L32
BLM18AG121SN1D_0603
VGA@

+1.0VSDGPU

470ohm/1A
SM010030010
200ma 120ohm@100mhz DCR 0.2

10mil
GCORE_SEN
VDDCI_SEN

49 GCORE_SEN
50 VDDCI_SEN

FB_GND
R142 0_0402_5% @

2160809000A11SEYMOU_FCBGA962
SEYM@

47A
55mA
5A

+BIF_VDDC

BIF_VDDC
Park/Madison:Connect to VDDC
Seymour/Whistler:
dGPU operating:VDDC
BACO mode:+1.0V

2010/04/27
non-BACO design,N27,T27
connect BIF_VDDC to VDDC
For BACO design

VDDCI and VDDC should have seperate regulators with a merge option on PCB
For Madison and Park, VDDCI and VDDC can share one common regulator

(GDDR3/DDR3 1.12V@4A VDDCI)
(GDDR5 1.12V@16A VDDCI)

Granville GPU short
Jumper at power side

+VDDCI

SM01000BY00 5000ma 120ohm@100mhz DCR 0.02

Granville VDDCI:4.6A

160mil

L45
FBMA-L11-201209-121LMA50T_0805

L46
FBMA-L11-201209-121LMA50T_0805

Seymour/Whistler

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Title: SCHEMATIC,MB A6911

Size	Document Number	Rev
Custom	4019A9	B

Date: Tuesday, November 09, 2010 Sheet 25 of 60

U30F

GND

2160809000A11SEYMOU_FCBGA962
SEYM@

REF137-13 update

DPA_VDD18,DPA_PVDD,DPB_VDD18,DPB_PVDD
can combian to DPAB_VDD18
DPC_VDD18,DPC_PVDD,DPD_VDD18,DPD_PVDD
can combian to DPCD_VDD18
(DPD_VDD18,DPD_PVDD not applicable on Robson/Park)
DPE_VDD18,DPE_PVDD,DPF_VDD18,DPF_PVDD
can combian to DPEF_VDD18

Seymour/Whistler :
DPA_VDD10,DPB_VDD10
can combian to DPAB_VDD10
DPC_VDD10,DPD_VDD10
can combian to DPCD_VDD10
DPE_VDD10,DPD_VDD10
can combian to DPEF_VDD10

DPx-VSSR,DPx_PVSS can combian to DP_VSSR
(Manhatann should have individual GND)
where x is A,B,C,D,E,F

U30H

Manhatann:300mA
Seymour:150mA

Manhatann:220mA
Seymour:110mA

DP mode:300mA
LVDS mode:440mA

DP mode:220mA
LVDS mode:240mA

SM01000AX00
550ma 220ohm@100mhz DCR 0.3

SM01000BL00
1000ma 470ohm@100mhz DCR 0.2

PX_EN:
SBIOS will control VGA power on/off.
High :BACO mode enable
LOWLBACO disable

Park/Madison :AL21left NC

Seymour/Whistler:
AL21:PX_EN
use to control discreate GPU regulators
for power express BACO mode
Support BACO:
output High3.3V:turn off regulators (BACO mode on)
output Low0V:turn on regulators (BACO mode off)
need PD resistor
No support BACO:
left NC

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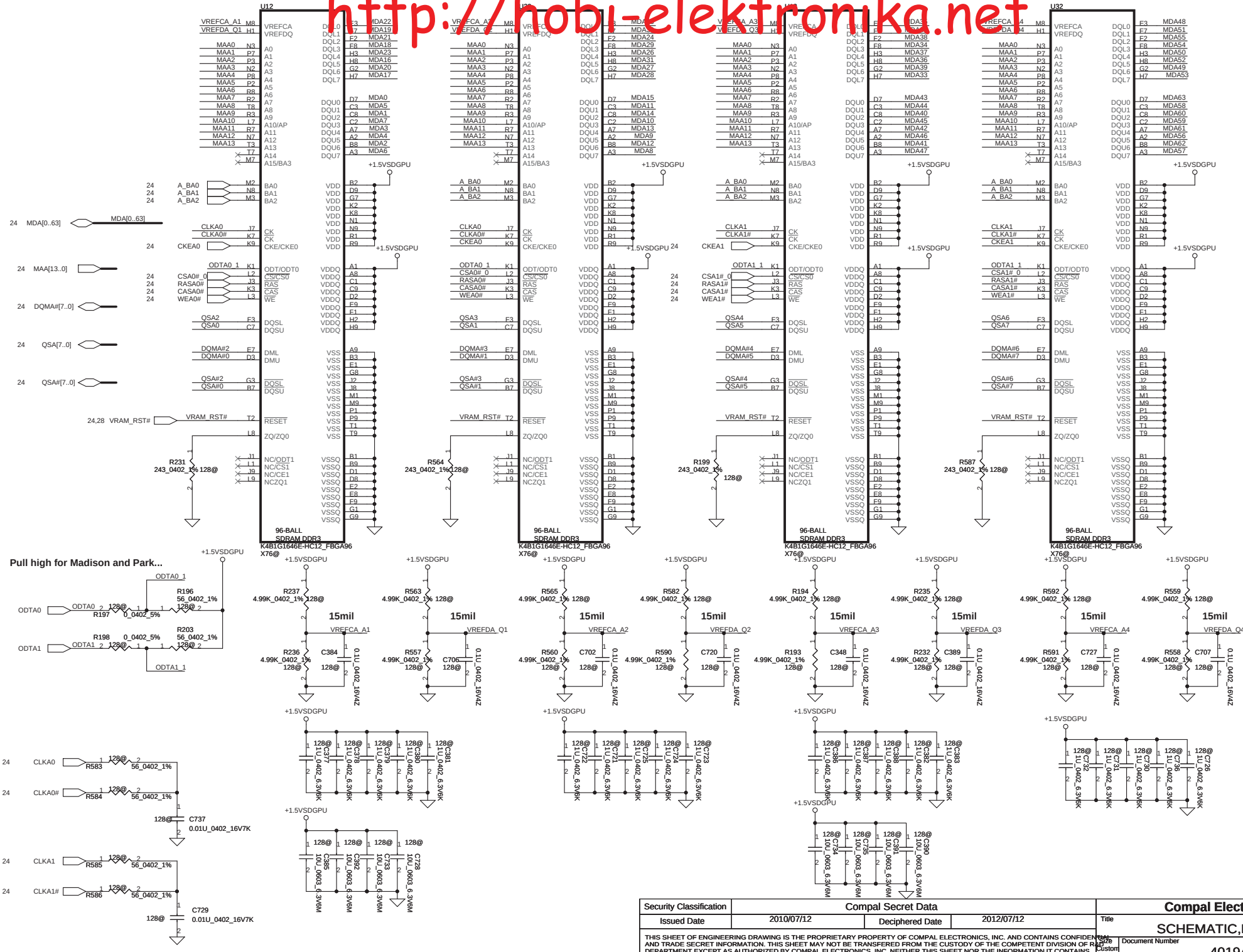
Date: Tuesday, November 09, 2010 | Sheet 26 of 60



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Custom	4019A9	B

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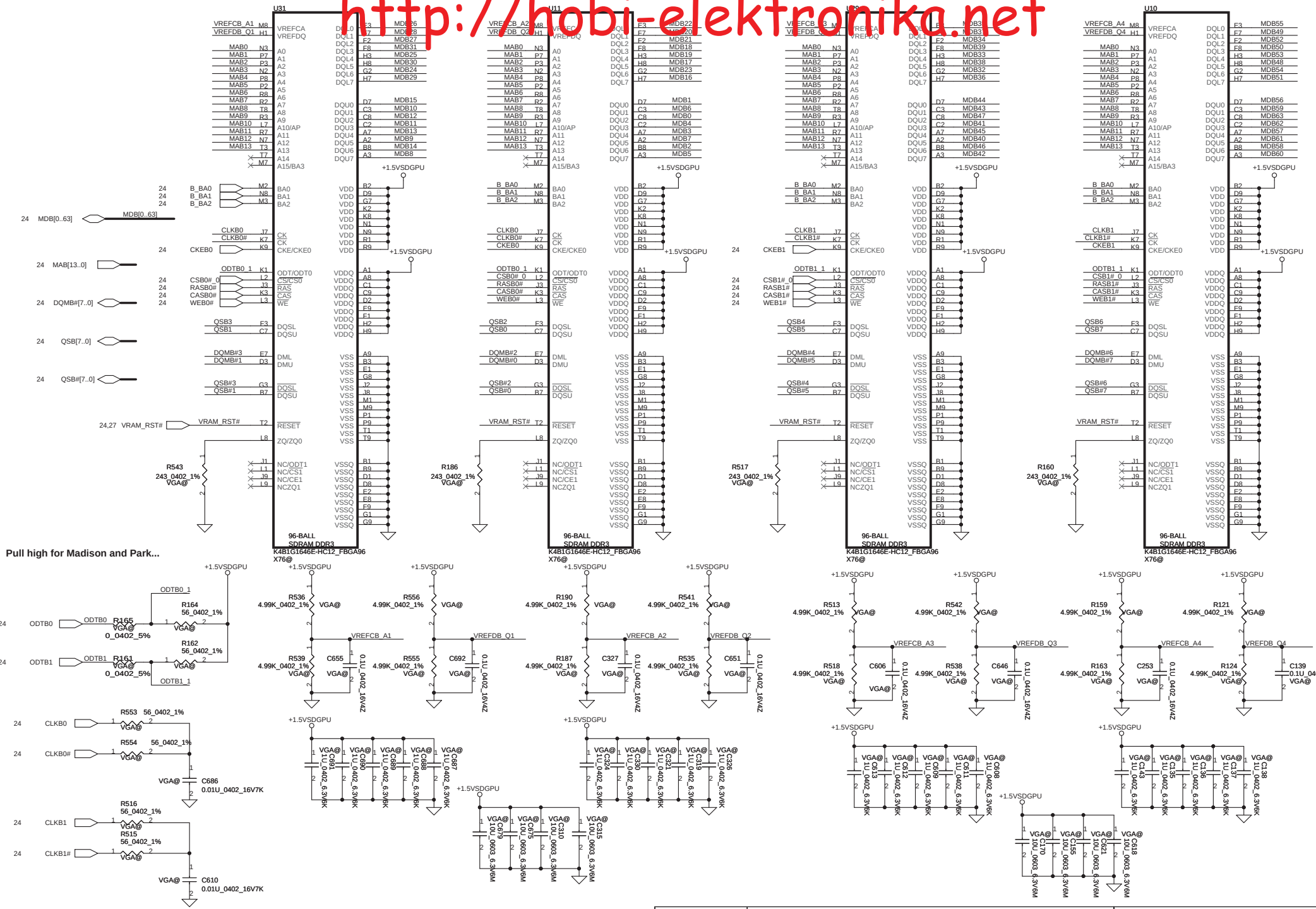

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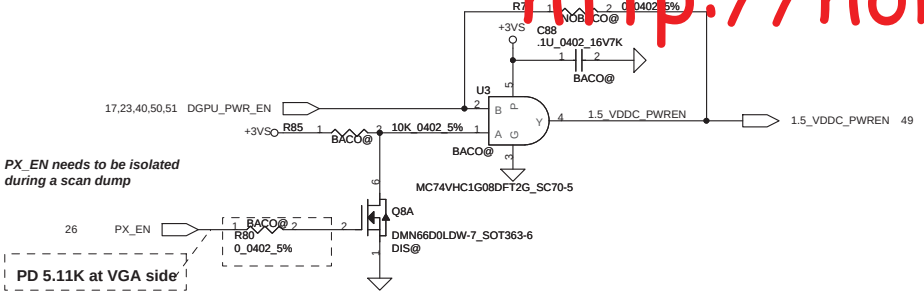
Date: Tuesday, November 09, 2010 | Sheet 28 of 60



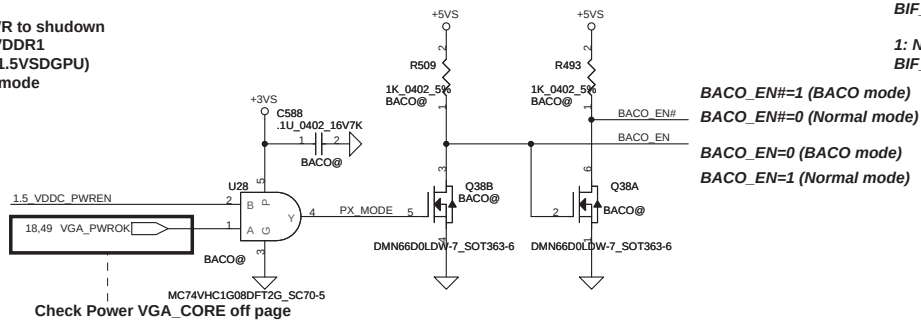
PX_EN needs to be isolated during a scan dump

PX_EN = 1, For BACO Mode
PX_EN = 0, For Normal Mode

PX_EN:
Connect to PWR to shudown VDDC/VDDCI/VDDR1 (VGA_CORE,+1.5VSDGPU) High in BACO mode

BACO_EN/BACO_EN#:
0: BACO Mode->BACO_EN High->
BIF_VDDC=+1.0VSDGPU(N-MOS),VGA_CORE(P-MOS)

1: Normal mode->BACO_EN# High->
BIF_VDDC=+VGA_CORE(N-MOS),VGA_CORE(N-MOS)

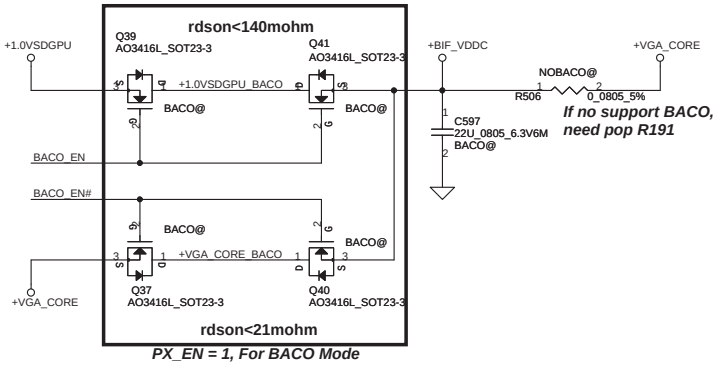


BACO_EN#=1 (BACO mode)
BACO_EN#=0 (Normal mode)

BACO_EN=0 (BACO mode)
BACO_EN=1 (Normal mode)

VGA Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
BACO_EN#	1	0
BACO_EN	0	1
+3VSDGPU	ON	ON
+1.8VSDGPU	ON	ON
+1.0VSDGPU	ON	ON
+VGA_CORE	ON	OFF
+1.5VSDGPU	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSDGPU

VGA Power Enable Signal Mapping table		
	Graville	Whistler and Seymour
+3VSDGPU	DGPU_PWR_EN	SUSP#
+1.8VSDGPU	DGPU_PWR_EN	DGPU_PWR_EN
+1.0VSDGPU	DGPU_PWR_EN	DGPU_PWR_EN
+VDDCI	DGPU_PWR_EN	Combine with +VGA_CORE
+VGA_CORE	DGPU_PWR_EN	1.5_VDDC_PWREN
+1.5VSDGPU	DGPU_PWR_EN	1.5_VDDC_PWREN

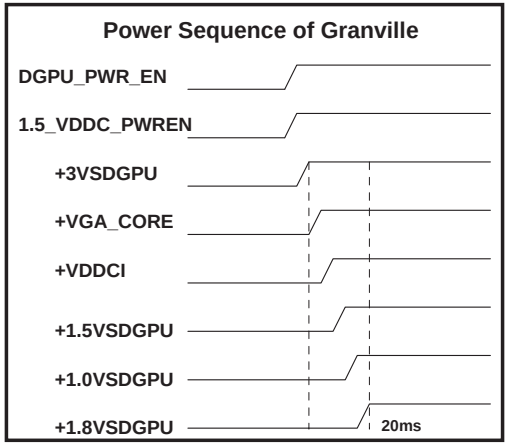


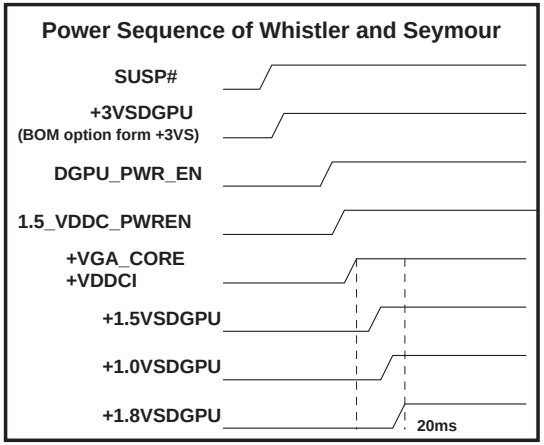
If no support BACO, need pop R191

PX_EN = 1, For BACO Mode
BACO_EN=0
BACO_EN#=1(5V)==> BIF_VDDC=+1.0VSDGPU
PX_EN = 0, For Normal Mode
BACO_EN=1(5V) ==> BIF_VDDC=VGA_CORE
BACO_EN#=0

For the MOSFETs on the path of delivering PCIE_VDDC(+1.0VSDGPU) to BIF_VDDC Rdson of 140 mOhms or less is required.

For the MOSFETs on the path of delivering VGA_CORE to BIF_VDDC, Rdson of 21 mOhms or less is required.



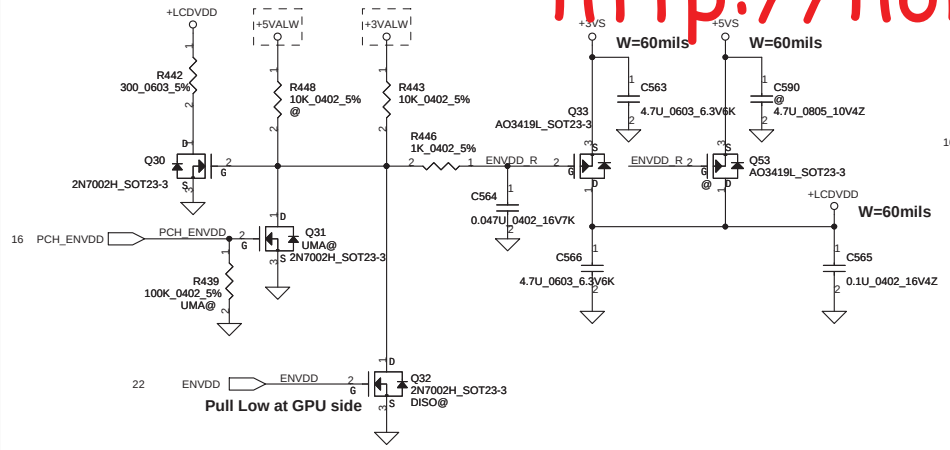


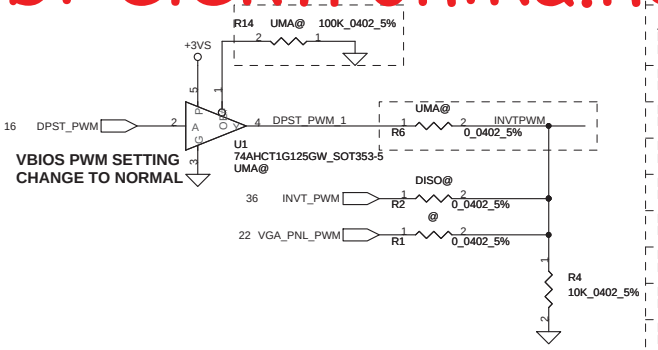
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.	
Title	SCHEMATIC,MB A6911
Size: Custom	Document Number: 4019A9
Rev	B
Date: Tuesday, November 09, 2010	Sheet 29 of 60

100505 change to +3VALW
101029 add +5VALW

LCD POWER CIRCUIT

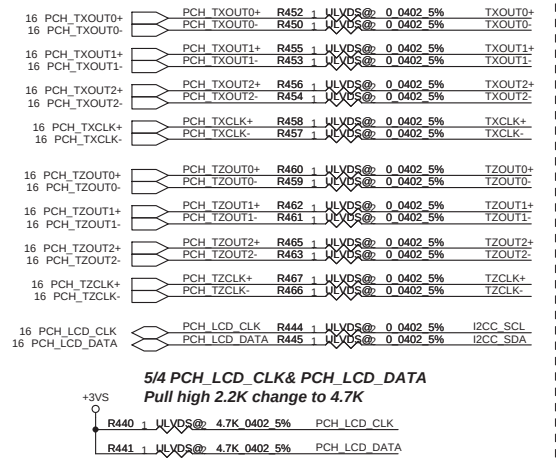




UMA/DIS LVDS/eDP Mapping table

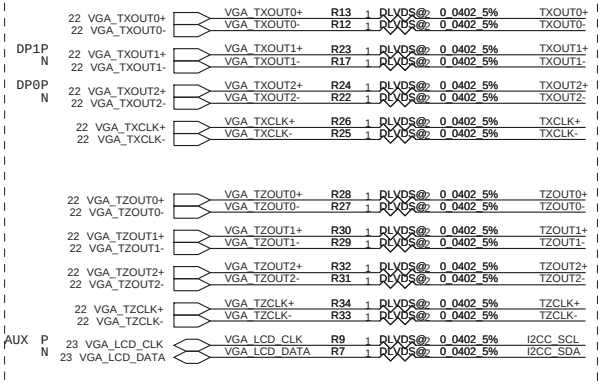
UMA		DIS		Panel
LVDS	eDP	LVDS	eDP	Conn.
PCH_TXOUT0+ PCH_TXOUT0-		VGA_TXOUT0+ VGA_TXOUT0-		TXOUT0+ TXOUT0-
PCH_TXOUT1+ PCH_TXOUT1-	EDP_TXP1 EDP_TXN1	VGA_TXOUT1+ VGA_TXOUT1-	DP1P DP1N	TXOUT1+ TXOUT1-
PCH_TXOUT2+ PCH_TXOUT2-	EDP_TXP0 EDP_TXN0	VGA_TXOUT2+ VGA_TXOUT2-	DP0P DP0N	TXOUT2+ TXOUT2-
PCH_TXCLK+ PCH_TXCLK-		VGA_TXCLK+ VGA_TXCLK-		TXCLK+ TXCLK-
PCH_TZOUT0+ PCH_TZOUT0-		VGA_TZOUT0+ VGA_TZOUT0-		TZOUT0+ TZOUT0-
PCH_TZOUT1+ PCH_TZOUT1-		VGA_TZOUT1+ VGA_TZOUT1-		TZOUT1+ TZOUT1-
PCH_TZOUT2+ PCH_TZOUT2-		VGA_TZOUT2+ VGA_TZOUT2-		TZOUT2+ TZOUT2-
PCH_TZCLK+ PCH_TZCLK-		VGA_TZCLK+ VGA_TZCLK-		TZCLK+ TZCLK-
PCH_TZCLK+ PCH_TZCLK-	EDP_AUXP EDP_AUXN	VGA_LCD_CLK VGA_LCD_DATA	AUXP AUXN	I2CC_SCL I2CC_SDA

UMA ONLY/Muxless

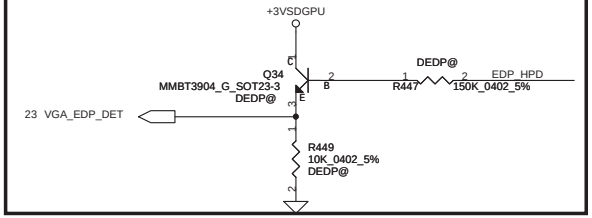


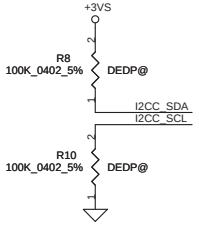
5/4 PCH_LCD_CLK& PCH_LCD_DATA
Pull high 2.2K change to 4.7K

Discrete ONLY

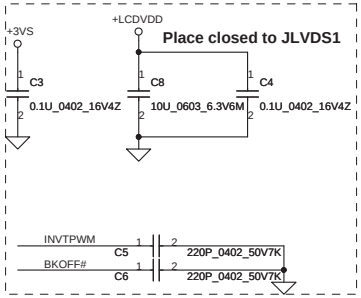


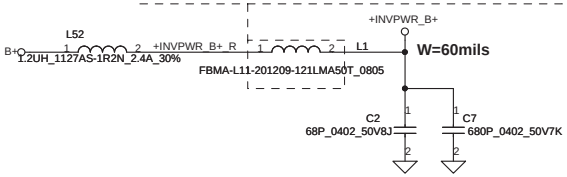
BOM option for Discrete eDP

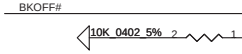


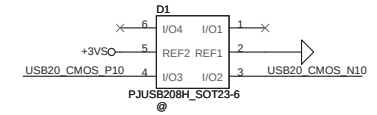


SM010014520 3000ma 220ohm@100mhz DCR 0.04
SM01000BY00 5000ma 120ohm@100mhz DCR 0.02

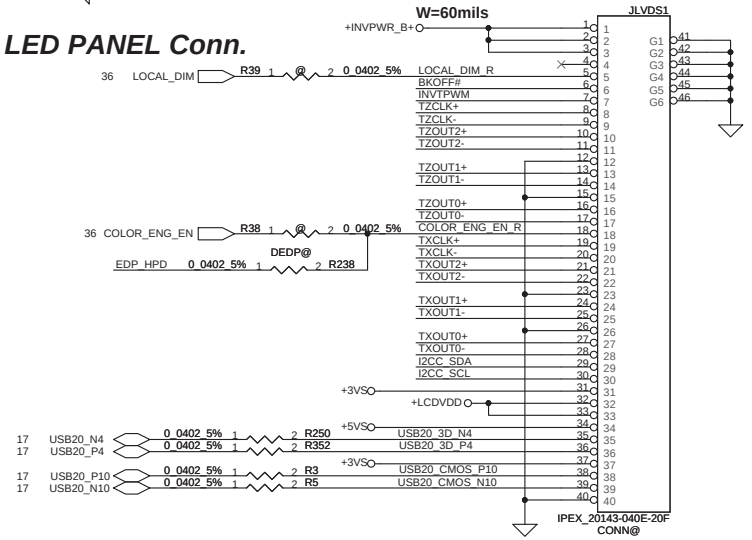








LED PANEL Conn.



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

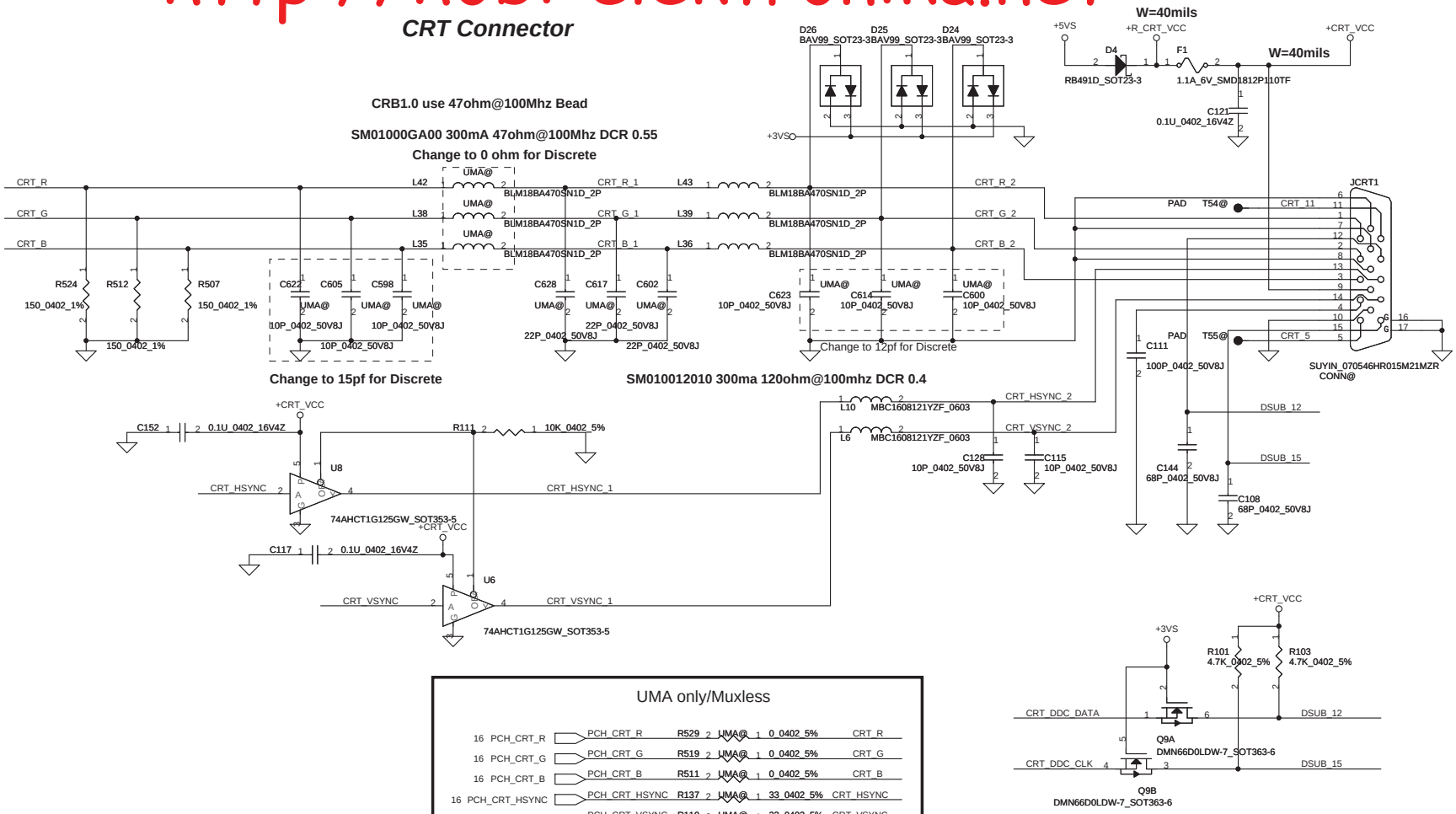
Compal Electronics, Inc.

Title: SCHEMATIC,MB A6911

Size: Custom | Document Number: 4019A9 | Rev: B

Date: Tuesday, November 09, 2010 | Sheet 30 of 60

CRT Connector



UMA only/Muxless

16 PCH_CRT_R	PCH_CRT_R	R529	UMA@	0_0402_5%	CRT_R
16 PCH_CRT_G	PCH_CRT_G	R519	UMA@	0_0402_5%	CRT_G
16 PCH_CRT_B	PCH_CRT_B	R511	UMA@	0_0402_5%	CRT_B
16 PCH_CRT_HSYNC	PCH_CRT_HSYNC	R137	UMA@	33_0402_5%	CRT_HSYNC
16 PCH_CRT_VSYNC	PCH_CRT_VSYNC	R110	UMA@	33_0402_5%	CRT_VSYNC
16 PCH_CRT_CLK	PCH_CRT_CLK	R102	UMA@	0_0402_5%	CRT_DDC_CLK
16 PCH_CRT_DATA	PCH_CRT_DATA	R89	UMA@	0_0402_5%	CRT_DDC_DATA

PCH DDC PU 2.2K on Page 17

Discrete only

23 VGA_CRT_R	VGA_CRT_R	R527	DISC@	0_0402_5%	CRT_R
23 VGA_CRT_G	VGA_CRT_G	R514	DISC@	0_0402_5%	CRT_G
23 VGA_CRT_B	VGA_CRT_B	R510	DISC@	0_0402_5%	CRT_B
23 VGA_CRT_HSYNC	VGA_CRT_HSYNC	R131	DISC@	0_0402_5%	CRT_HSYNC
23 VGA_CRT_VSYNC	VGA_CRT_VSYNC	R107	DISC@	0_0402_5%	CRT_VSYNC
23 VGA_DDC_CLK	VGA_DDC_CLK	R98	DISC@	0_0402_5%	CRT_DDC_CLK
23 VGA_DDC_DATA	VGA_DDC_DATA	R86	DISC@	0_0402_5%	CRT_DDC_DATA

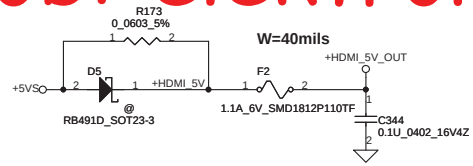
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

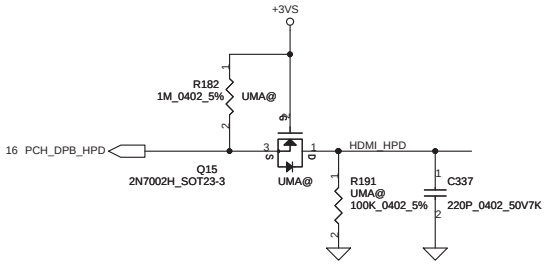
Compal Electronics, Inc.

Title: SCHEMATIC,MB A6911

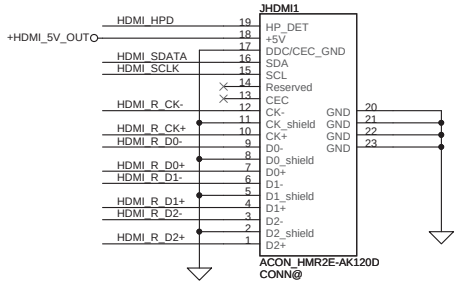
Size	Document Number	Rev
Custom	4019A9	B

Date: Tuesday, November 09, 2010 | Sheet 31 of 60

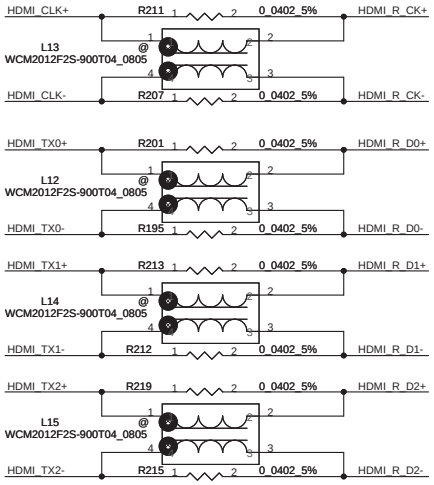


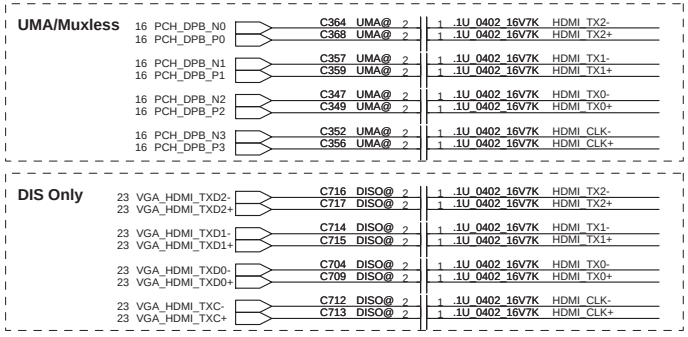


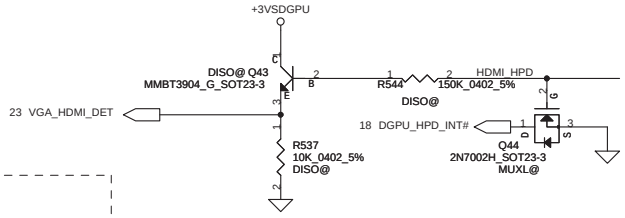
HDMI connector

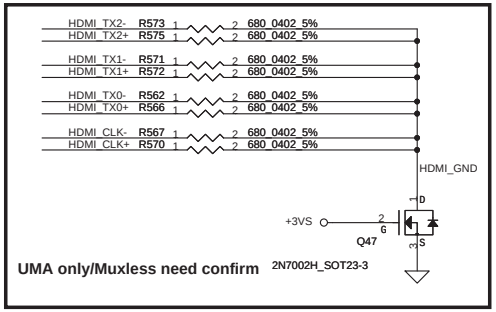


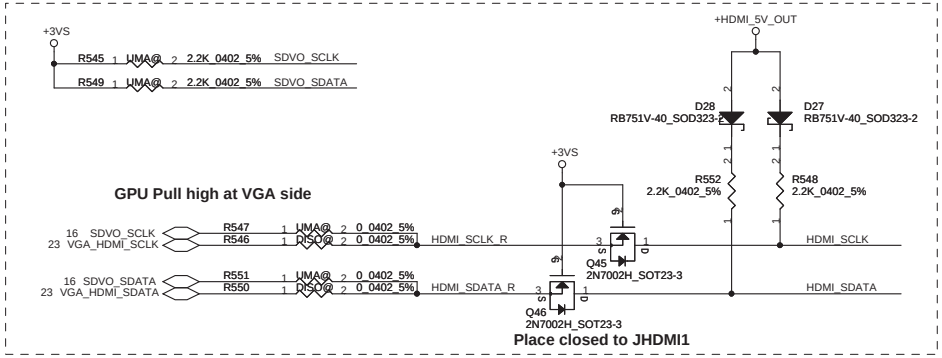
SM070001310 400ma 90ohm@100mhz DCR 0.3











Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

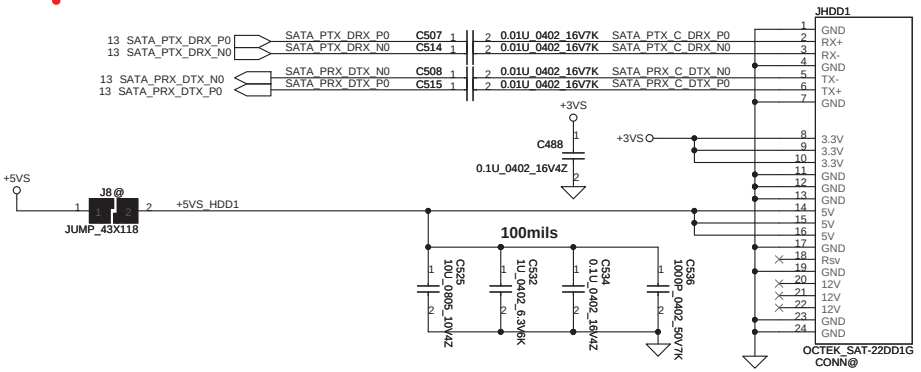
Title: SCHEMATIC,MB A6911

Size	Document Number	Rev
Custom	4019A9	B

Date: Tuesday, November 09, 2010 | Sheet 32 of 60

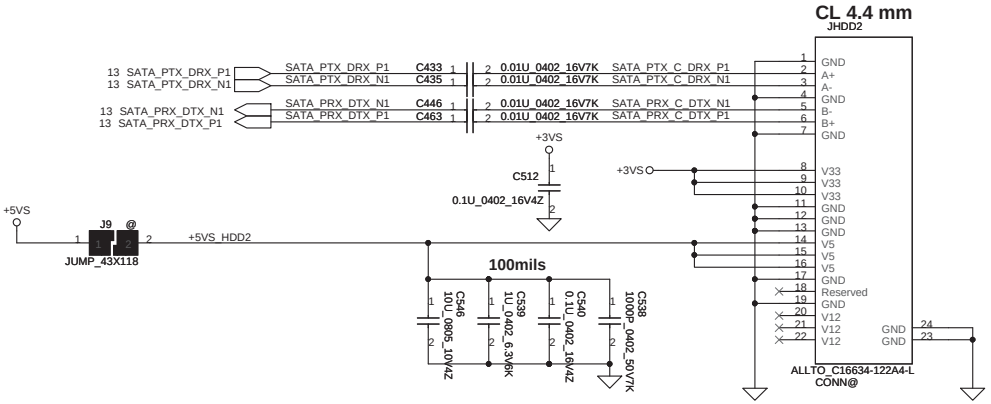
SATA HDD1 Conn.

CL 2.9 mm

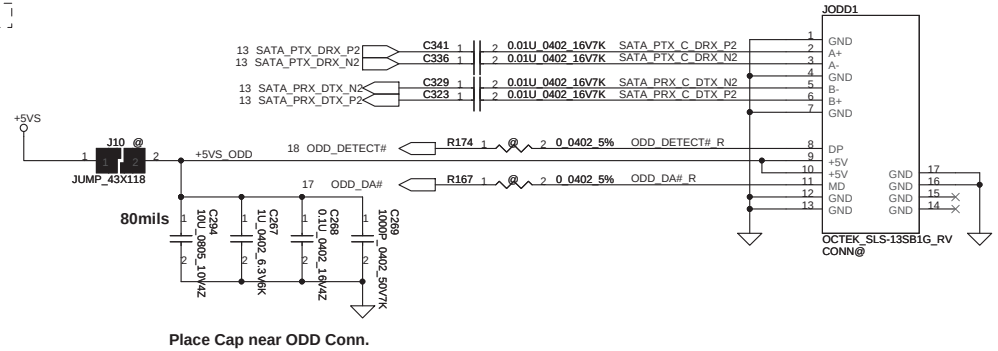


SATA HDD2 Conn.

CL 4.4 mm

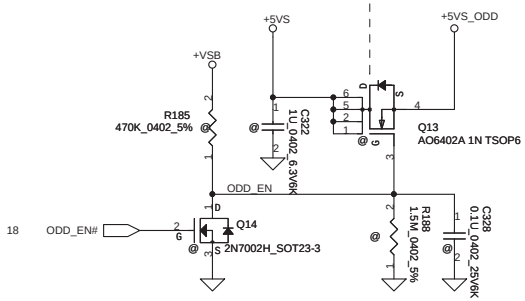


SATA ODD Conn.



Place Cap near ODD Conn.

SB564020020(S TR AO6402A 1N TSOP-6 W/D)



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

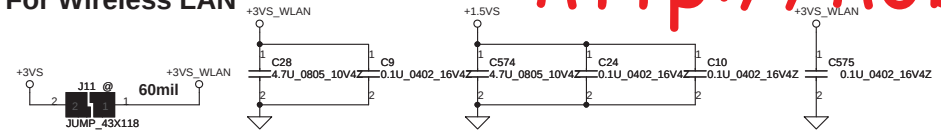
Compal Electronics, Inc.

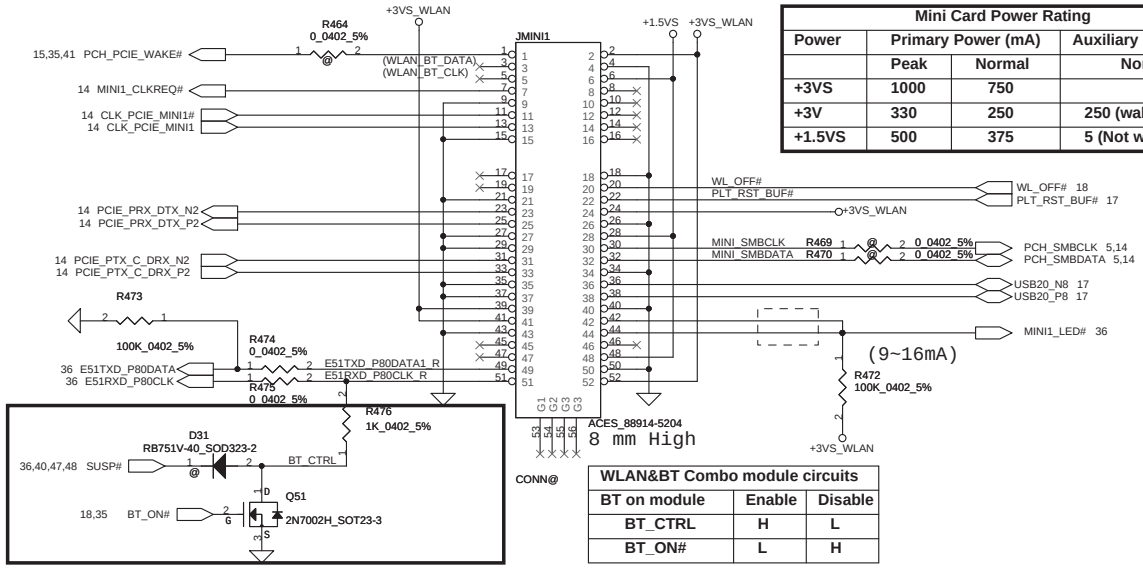
Title: SCHEMATIC,MB A6911

Size: Custom | Document Number: 4019A9 | Rev: B

Date: Tuesday, November 09, 2010 | Sheet 33 of 60

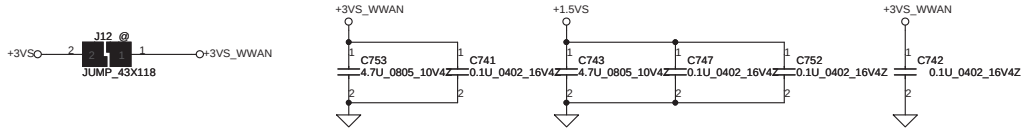
For Wireless LAN

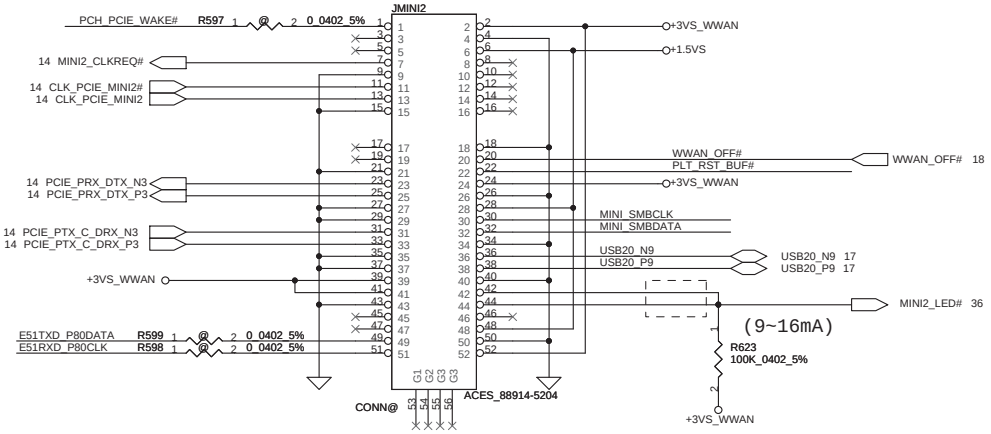




Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

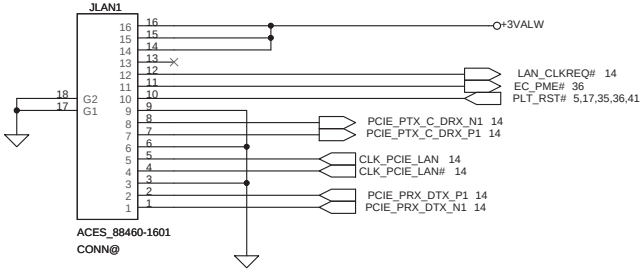
WLAN&BT Combo module circuits		
BT on module	Enable	Disable
BT_CTRL	H	L
BT_ON#	L	H





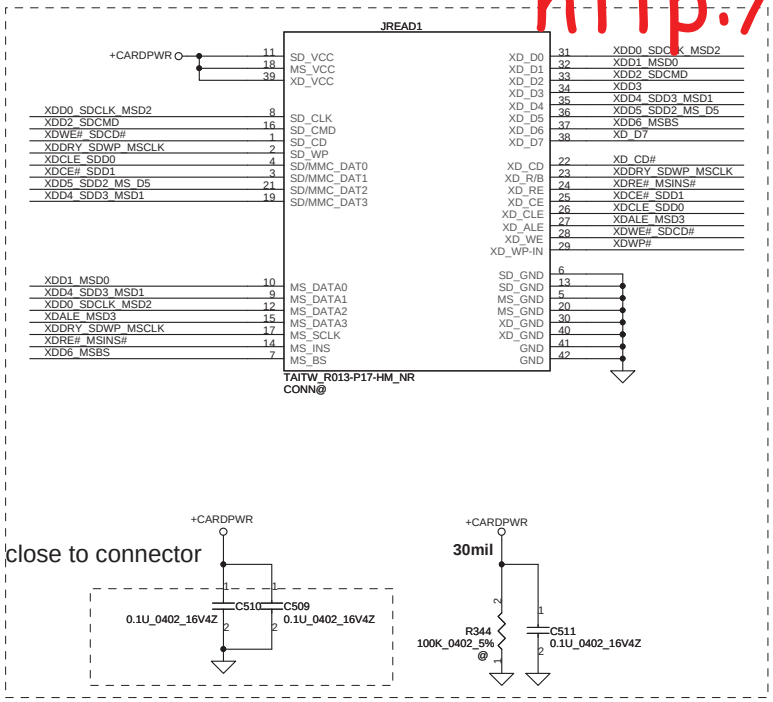
8 mm High

LAN CONN. *LS-6912P*



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

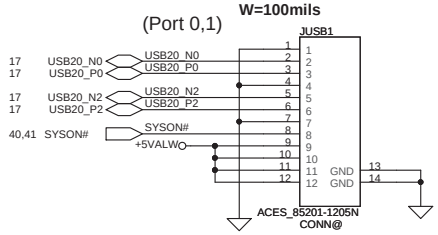
Compal Electronics, Inc.			
Title	SCHEMATIC,MB A6911		
Size: Custom	Document Number: 4019A9		Rev: B
Date: Tuesday, November 09, 2010	Sheet 34 of 60		



close to connector

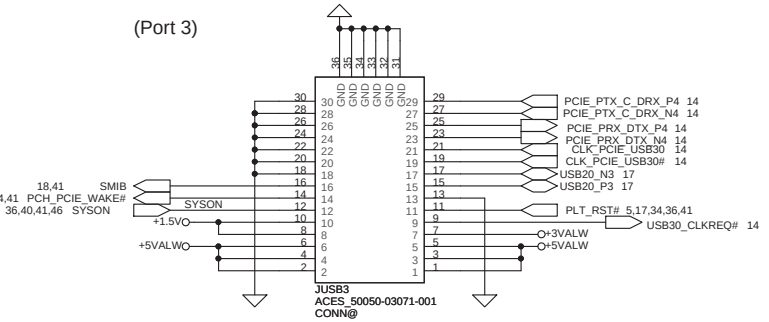
LS-6911P
USB/B Conn. (USB2.0 SKU)

(Port 0,1)



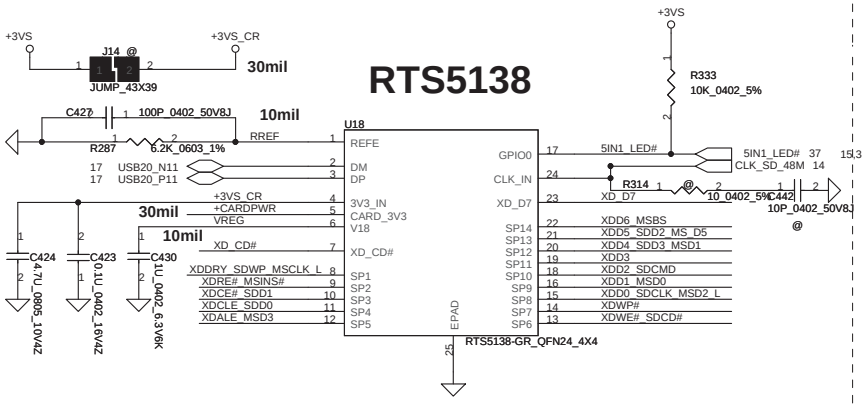
USB/B USB3.0 Conn.(USB3.0 SKU)

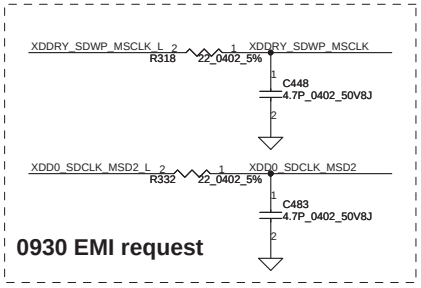
(Port 3)



Pull high @ USB3.0/B side

RTS5138

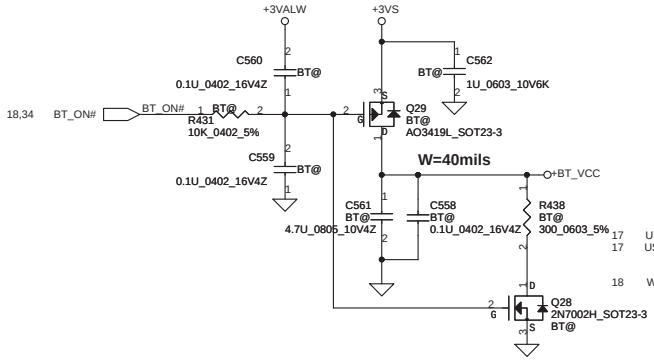




0930 EMI request

	XD	SD	MS
	XD_CD#		
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	
SP5	XD_ALE		MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP		
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1		MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3		
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	
SP14	XD_D6		MS_BS
	XD_D7		

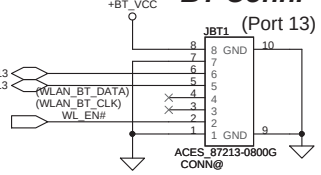
Share Pin



BT Wire Cable Note:
Pin 3, Pin 4 NC

BT Conn.

(Port 13)



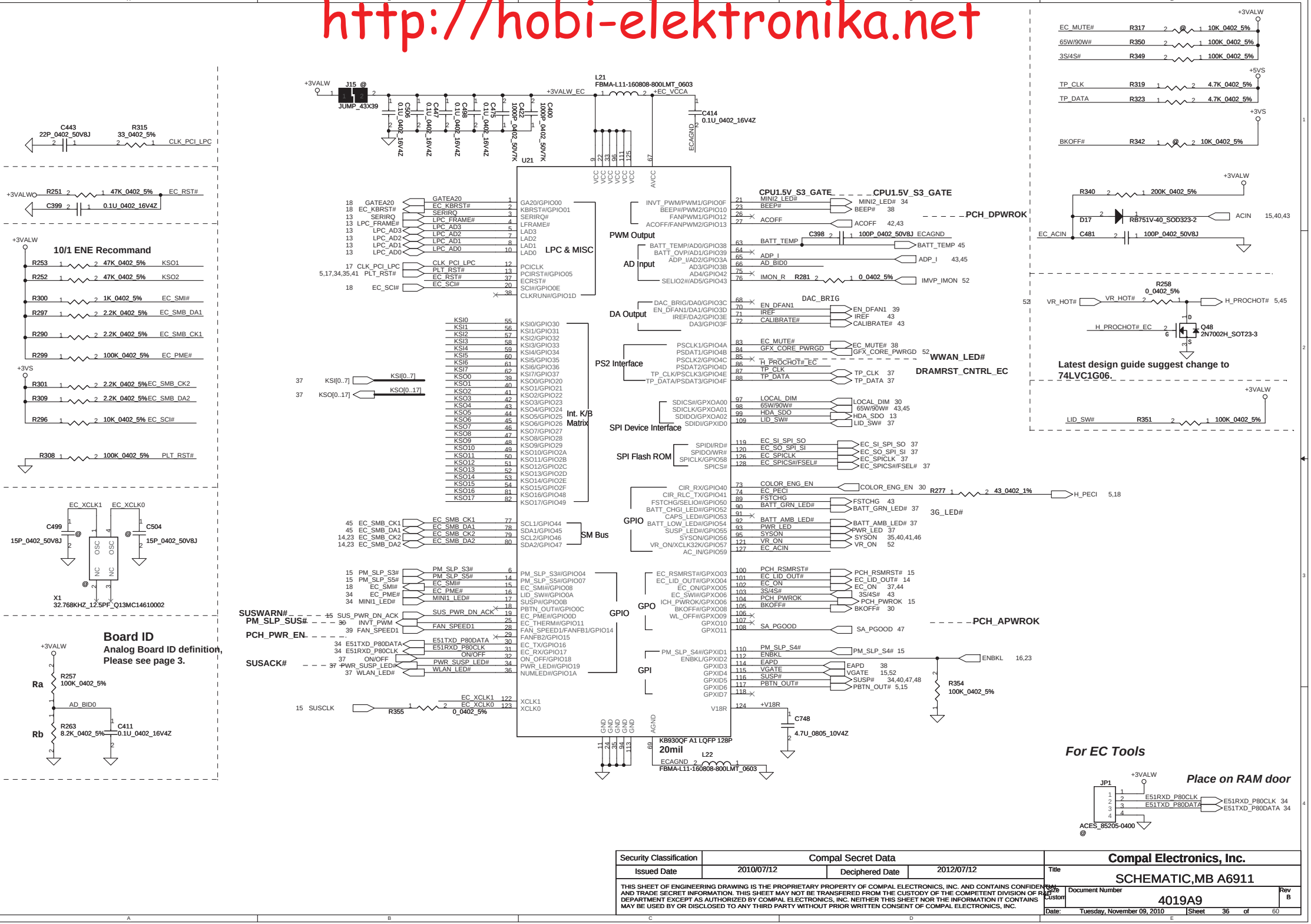
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: SCHEMATIC,MB A6911

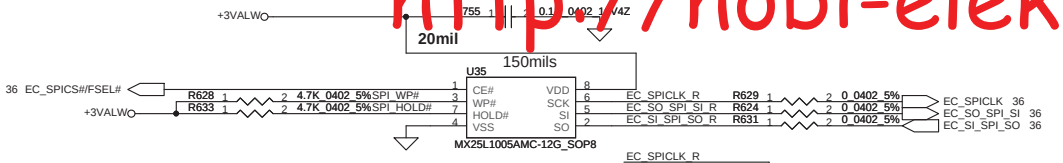
Size: Custom | Document Number: 4019A9 | Rev: B

Date: Tuesday, November 09, 2010 | Sheet 35 of 60

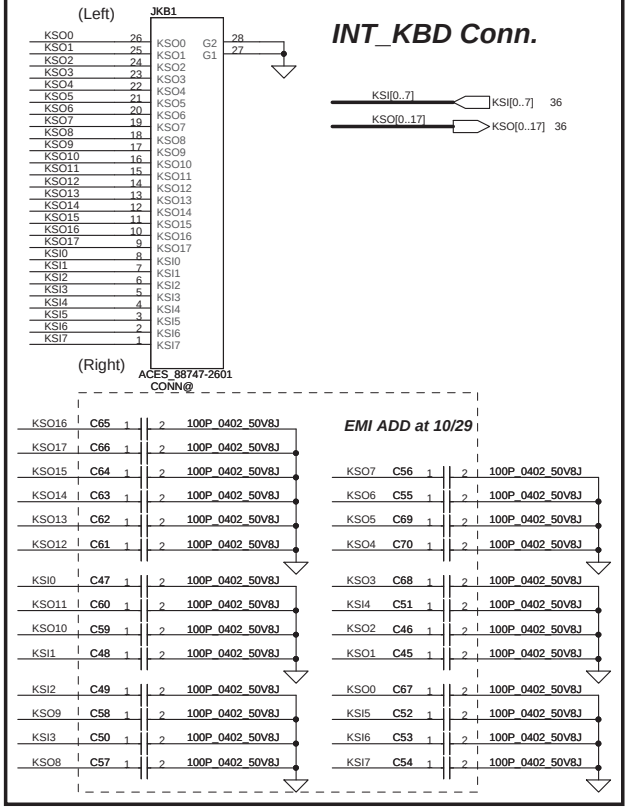


Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

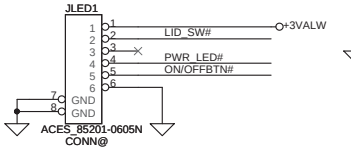
Compal Electronics, Inc.	
Title	SCHEMATIC,MB A6911
Size: Custom	Document Number: 4019A9
Rev	B
Date: Tuesday, November 09, 2010	Sheet 36 of 60



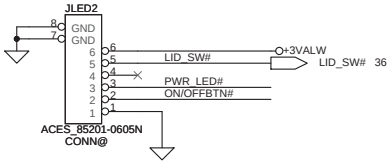
INT_KBD Conn.



LED/B P7YE0/P7YH0 LS-6913P



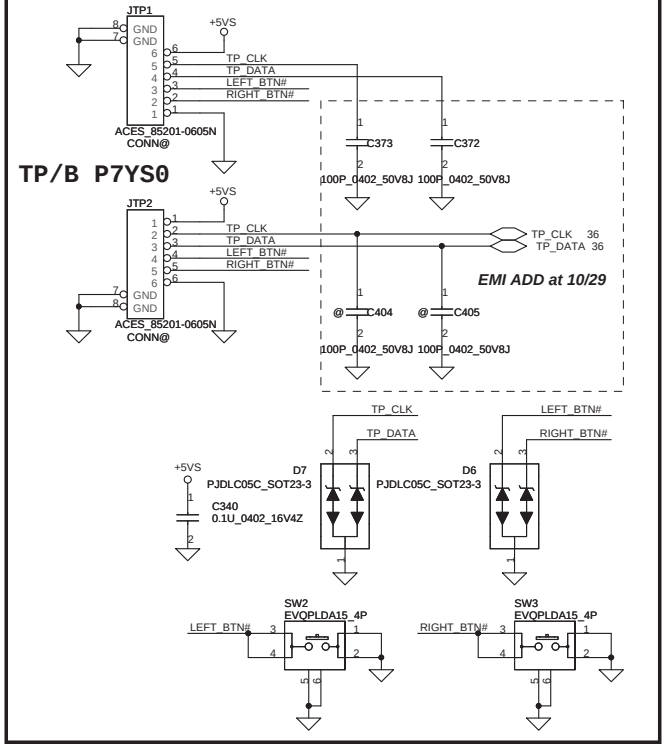
LED/B P7YS0 LS-6913P

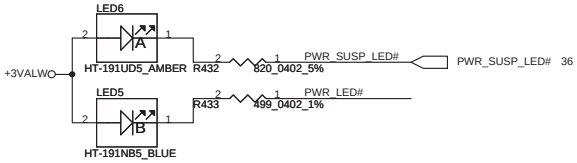


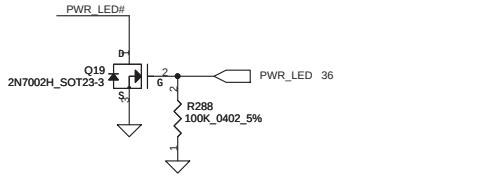
LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
NEW70/80/90	Blue	Amber	Blue		Blue	Amber		

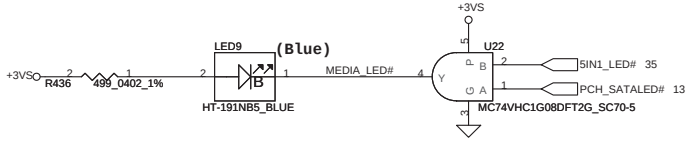
TP/B P7YE0/P7YH0

TP/B P7YS0



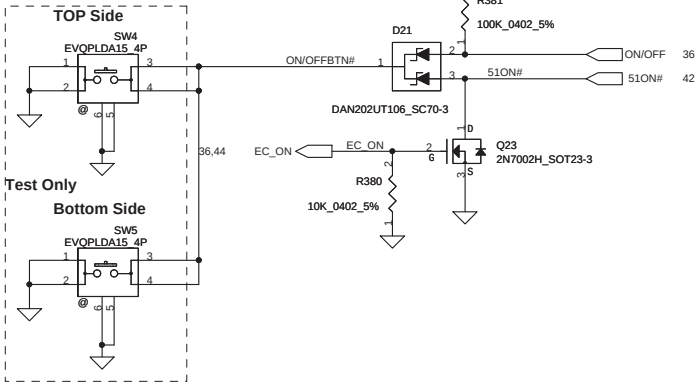


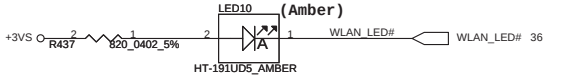




Power Button

ON/OFF switch





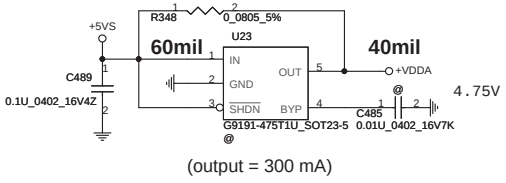
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

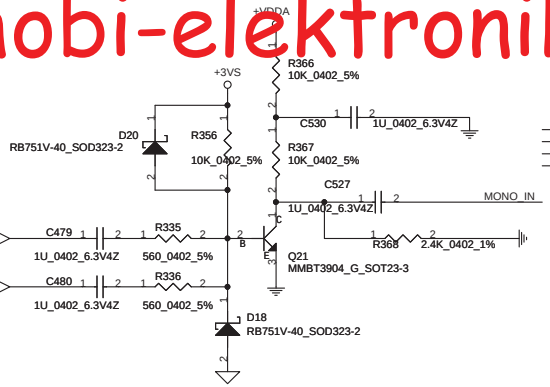
Title: SCHEMATIC,MB A6911

Size: Custom | Document Number: 4019A9 | Rev: B

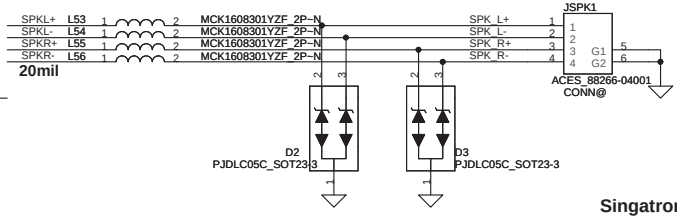
Date: Tuesday, November 09, 2010 | Sheet 37 of 60



(output = 300 mA)

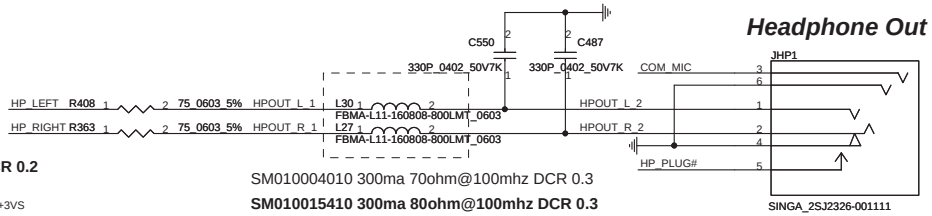


Int. Speaker Conn.



Singatron 2SJ2326
DC021007151

Headphone Out

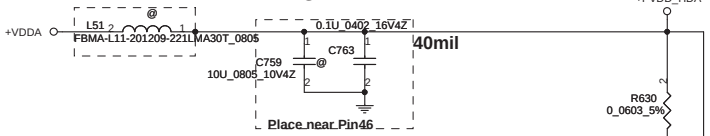


SM010004010 300ma 70ohm@100mhz DCR 0.3
SM010015410 300ma 80ohm@100mhz DCR 0.3

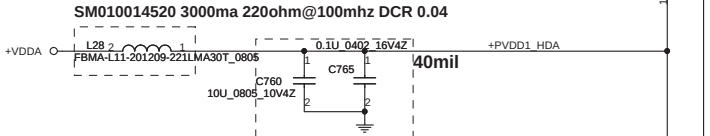
FootPrint

HD Audio Codec

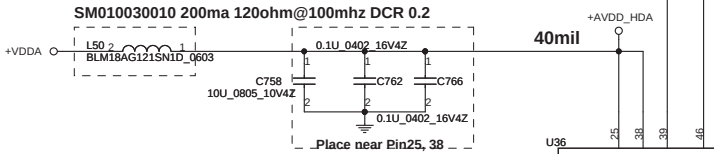
SM010014520 3000ma 220ohm@100mhz DCR 0.04



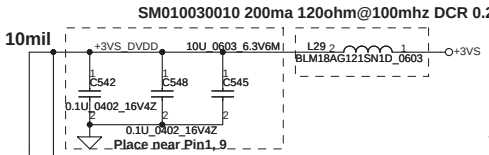
SM010014520 3000ma 220ohm@100mhz DCR 0.04

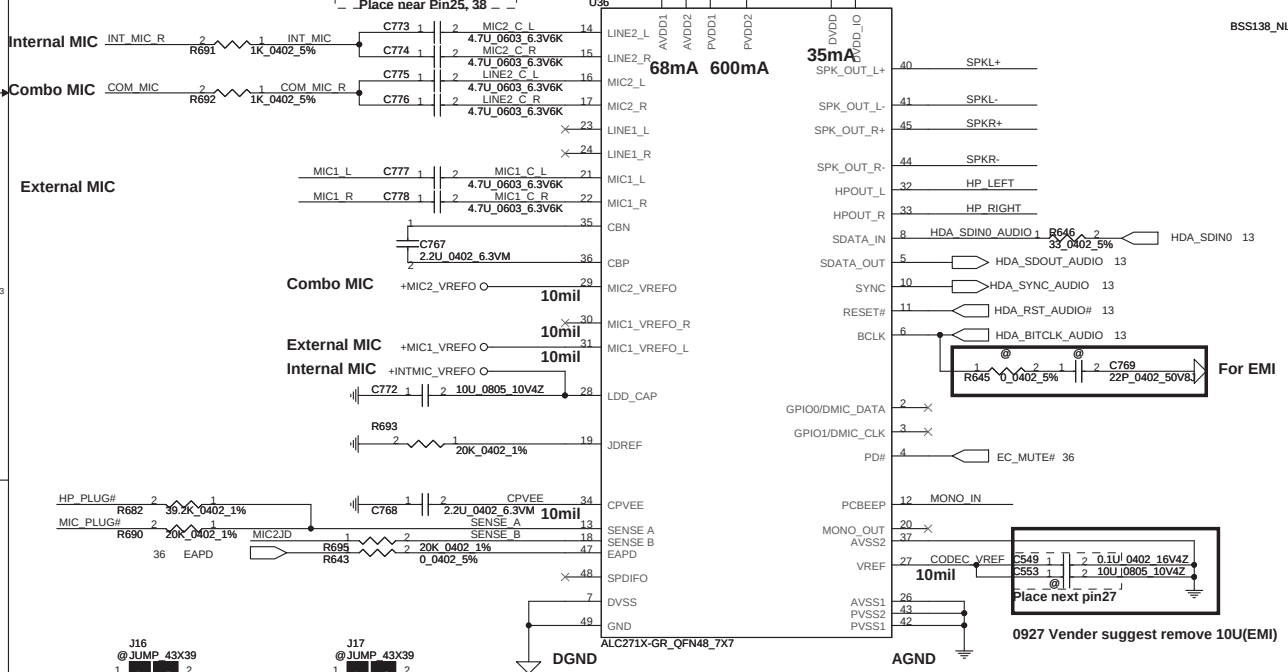


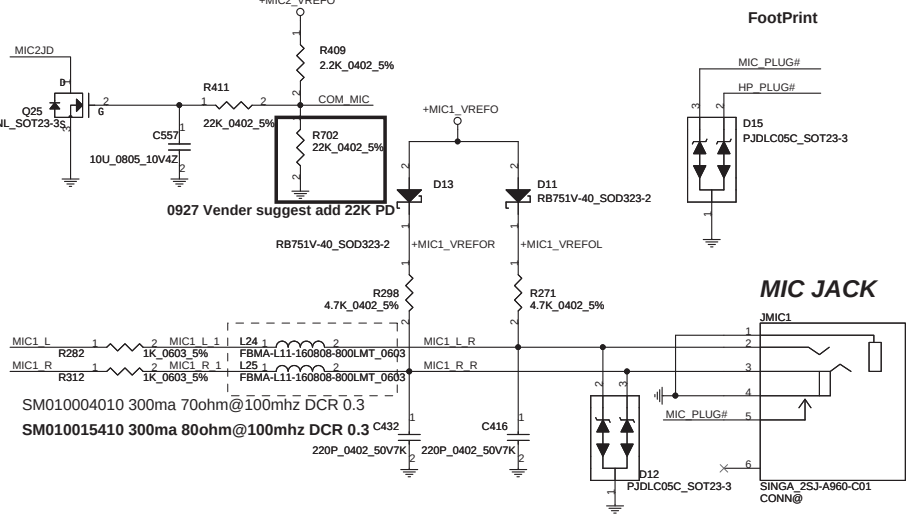
SM010030010 200ma 120ohm@100mhz DCR 0.2



SM010030010 200ma 120ohm@100mhz DCR 0.2



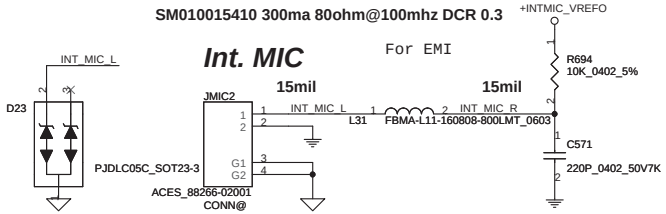


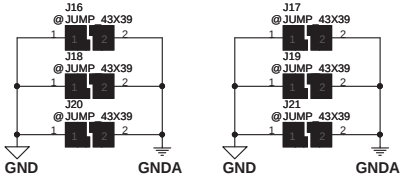


SM010004010 300ma 70ohm@100mhz DCR 0.3
SM010015410 300ma 80ohm@100mhz DCR 0.3

MIC JACK

Int. MIC





Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

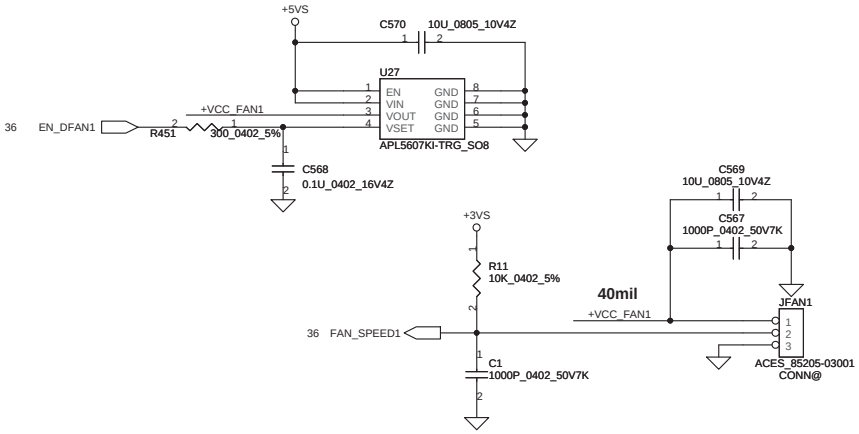
Compal Electronics, Inc.

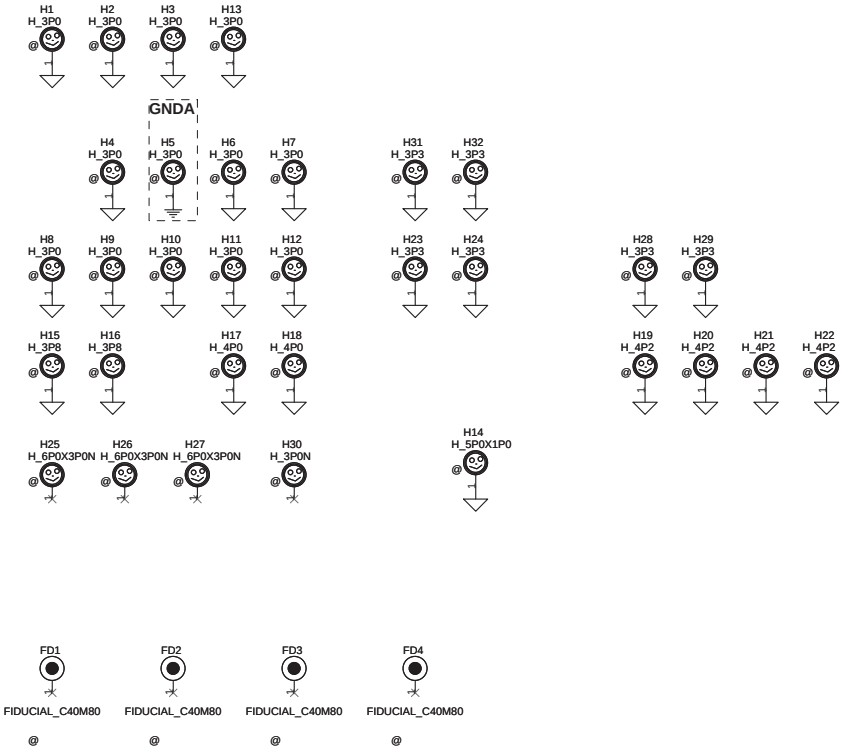
Title: SCHEMATIC,MB A6911

Size: Custom | Document Number: 4019A9 | Rev: B

Date: Tuesday, November 09, 2010 | Sheet 38 of 60

FAN1 Conn





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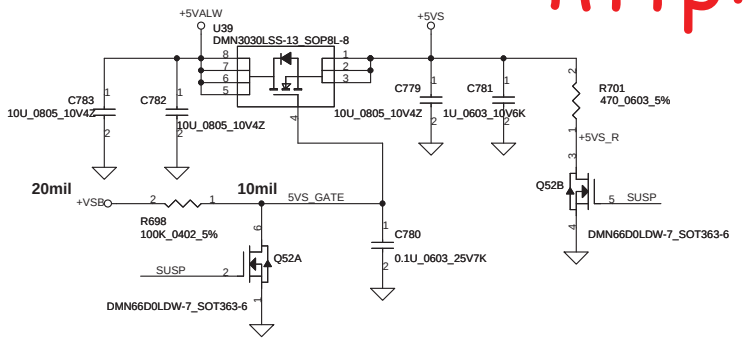
Issued Date	2010/07/12	Deciphered Date	2012/07/12

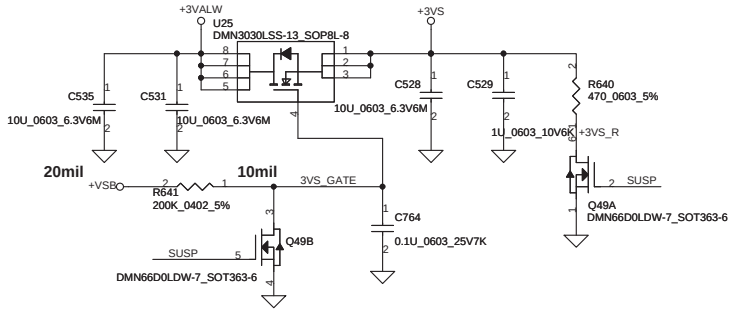
Compal Electronics, Inc.

Title	SCHEMATIC,MB A6911	
Size: Custom	Document Number: 4019A9	Rev: B
Date: Tuesday, November 09, 2010	Sheet 39 of 60	

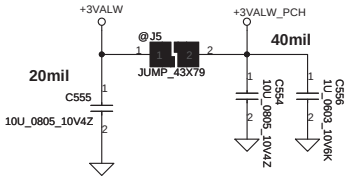
+5VALW TO +5VS



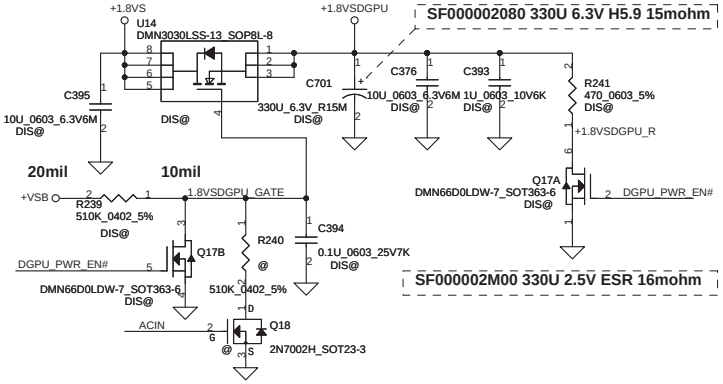
+3VALW TO +3VS



+3VALW to +3VALW(PCH AUX) Power

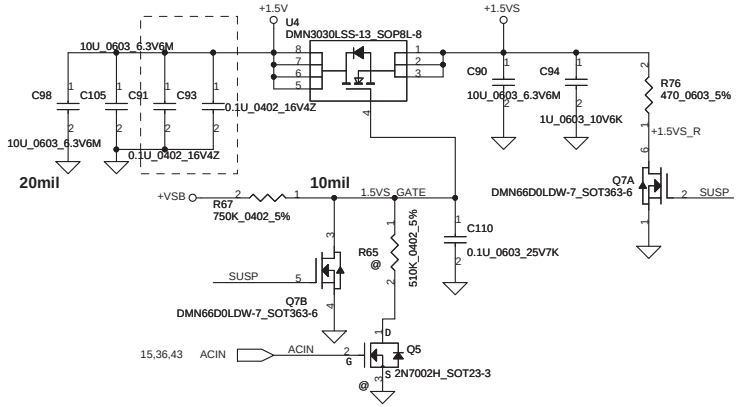


+1.8VS to +1.8VSDGPU for GPU

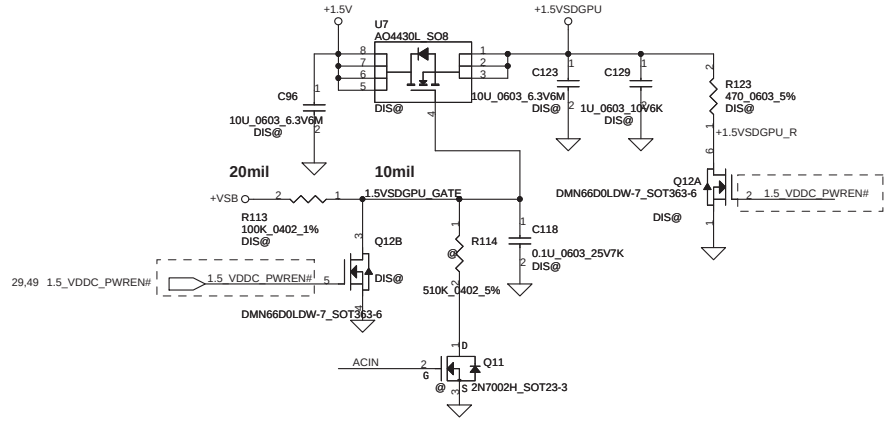


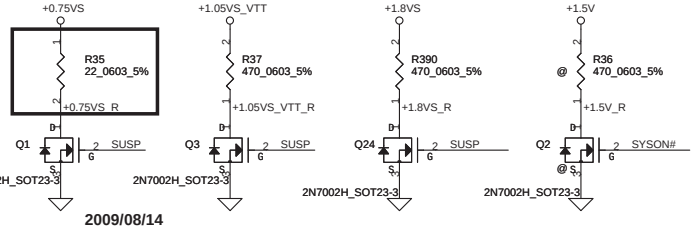
1211 EMI ADD 0.1U close PJ5

+1.5V to +1.5VS

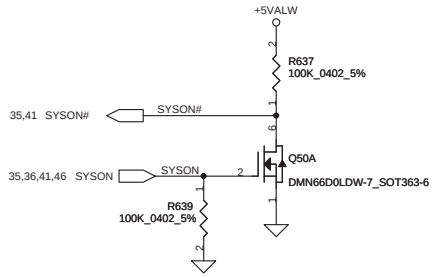


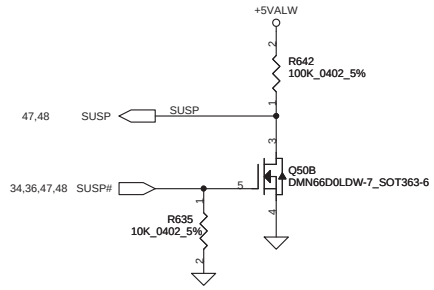
+1.5V to +1.5VSDGPU for GPU

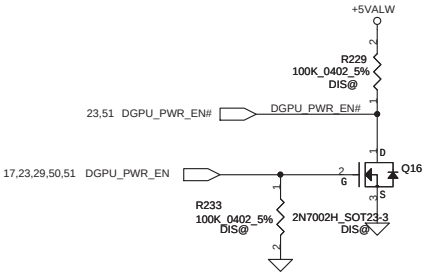




2009/08/14
CP_S3PowerReduction
WhitePaper_Rev0.9
0.75VS speed up discharge







Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: SCHEMATIC,MB A6911

Size	Document Number	Rev
Custom	4019A9	B

Date: Tuesday, November 09, 2010 | Sheet 40 of 60

+1.5V to +1.05V Transfer

Vout=0.8(1+10K/32.4K)
1.042 ~ 1.0469 ~ 1.0519V
Spec: 0.9975 ~ 1.05 ~ 1.1025

+3VALW to +3V Transfer

Close to U41.D7

Close to U41.P13

7K for customer request, can use other kind of capacitor, like Y5V.

For EMI request

For USB2.0 ESD diode

For USB3.0 ESD diode

SPEC Max:+3V---200mA;+1.05V---800mA
Idle mode:0.489W:
+3V---43mA;+1.05V---328mA
D3 mode:0.066W:
+3V---5.4mA;+1.05V---45mA

Can be attach to EC, either.

PCI Express/ExpressCard select signal
1:others
0:Express Card or Mini card

As short as possible

W=100mils

Resister overlap with L70

USB2.0 Conn SKU

SF000002Y00 220U 6.3V 17mohm H4.5

Place as close as possibile to U41.N14 and U41.M14

USB2.0 Conn

P/N: SA000048H10 (S IC UPD720200AF1-DAP-SSA-A FBGA USB3.0)

Pin compare table for support USB remote wakeup or not

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y5,R816,C879,C880
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

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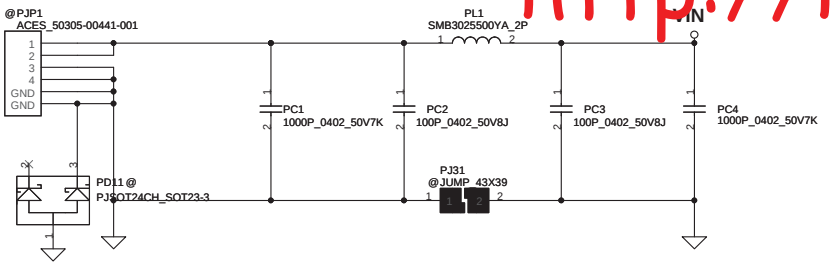
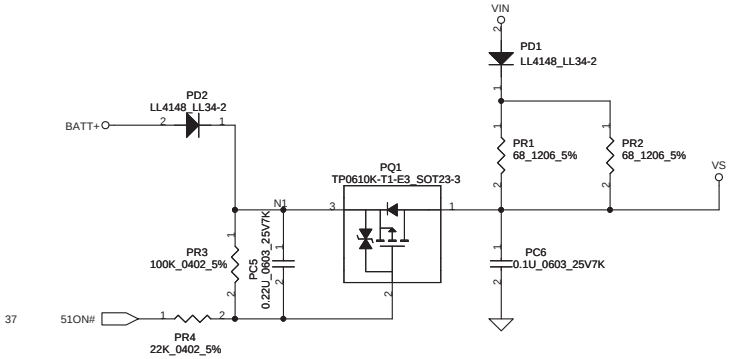
Compal Electronics, Inc.

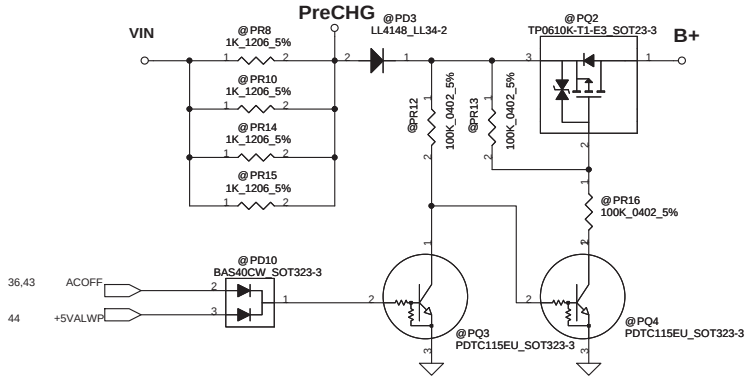
Title: SCHEMATIC,MB A6911

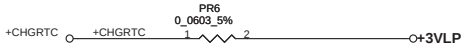
Size: Custom | Document Number: 4019A9 | Rev: B

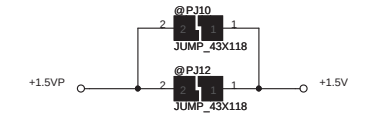
Date: Tuesday, November 09, 2010 | Sheet 41 of 60

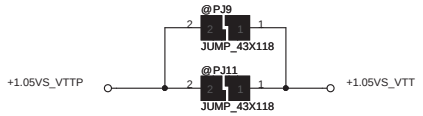


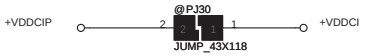


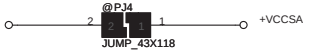


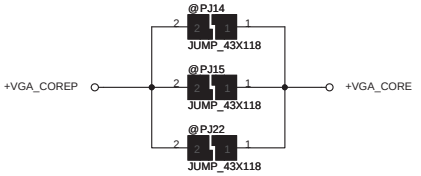


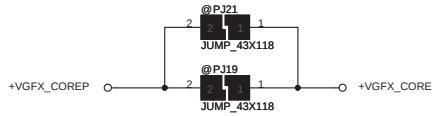












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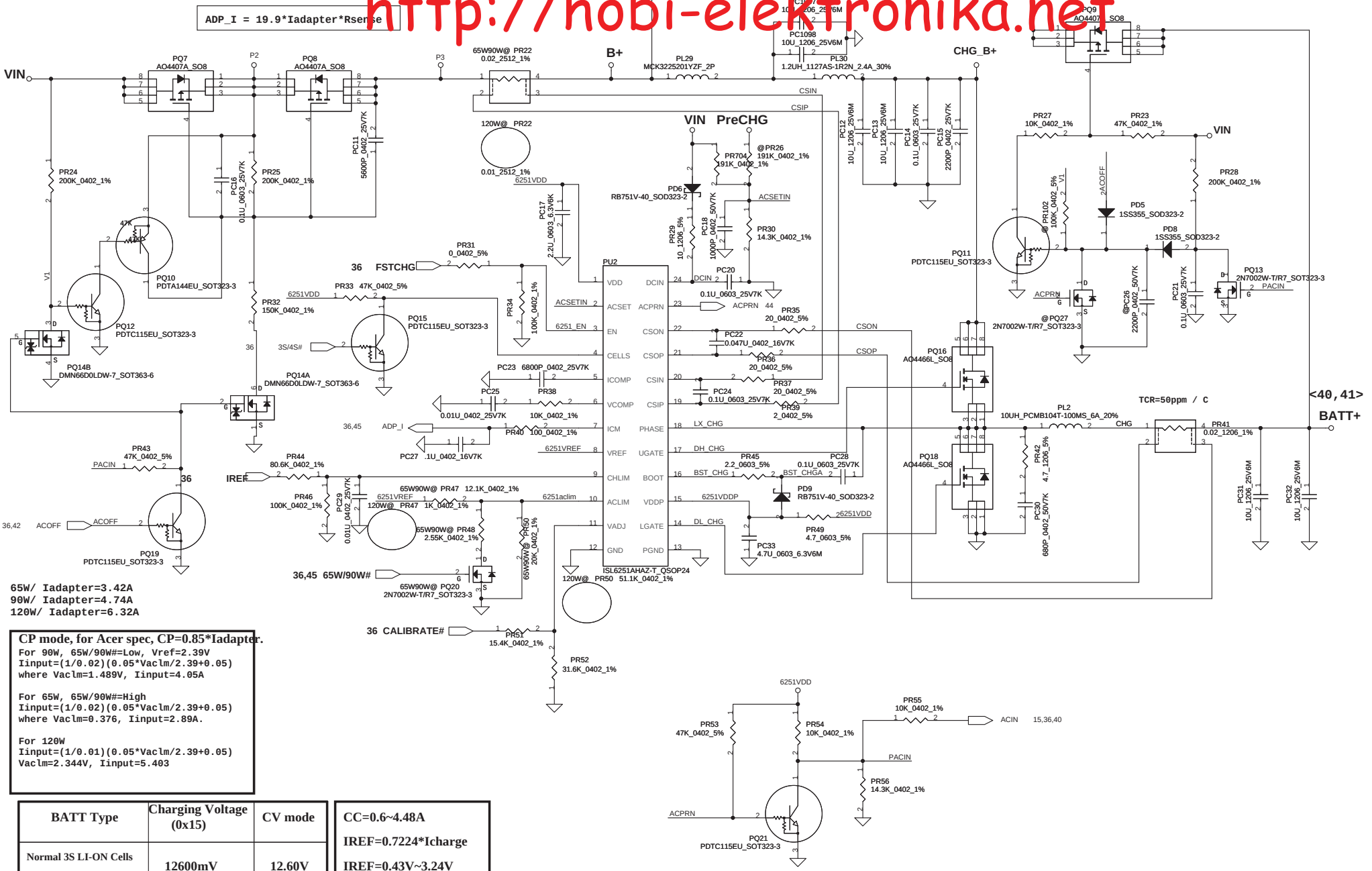
Title: SCHEMATIC,MB A6911

Size	Document Number	Rev
Custom	4019A9	B

Date: Tuesday, November 09, 2010 | Sheet 42 of 60



65W/ Iadapter=3.42A
90W/ Iadapter=4.74A
120W/ Iadapter=6.32A

CP mode, for Acer spec, CP=0.85*Iadapter.

For 90W, 65W/90W#=Low, Vref=2.39V
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.489V, Iinput=4.05A

For 65W, 65W/90W#=High
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=0.376, Iinput=2.89A.

For 120W
Iinput=(1/0.01)(0.05*Vaclm/2.39+0.05)
Vaclm=2.344V, Iinput=5.403

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

CC=0.6~4.48A

IREF=0.7224*Icharge

IREF=0.43V~3.24V

Ki
Vchlim=Iref*(PR46/(PR44+PR46))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Ichanrge=(165mV/PR22)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.3842*Iref
Iref=0.7224*Ichanrge =>Ki=0.7224

Kv
Rinternal ic=514K Rec=3K R1=PR379=15.4K
R2=PR381=31.6K
R=514K//31.6K//(15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451

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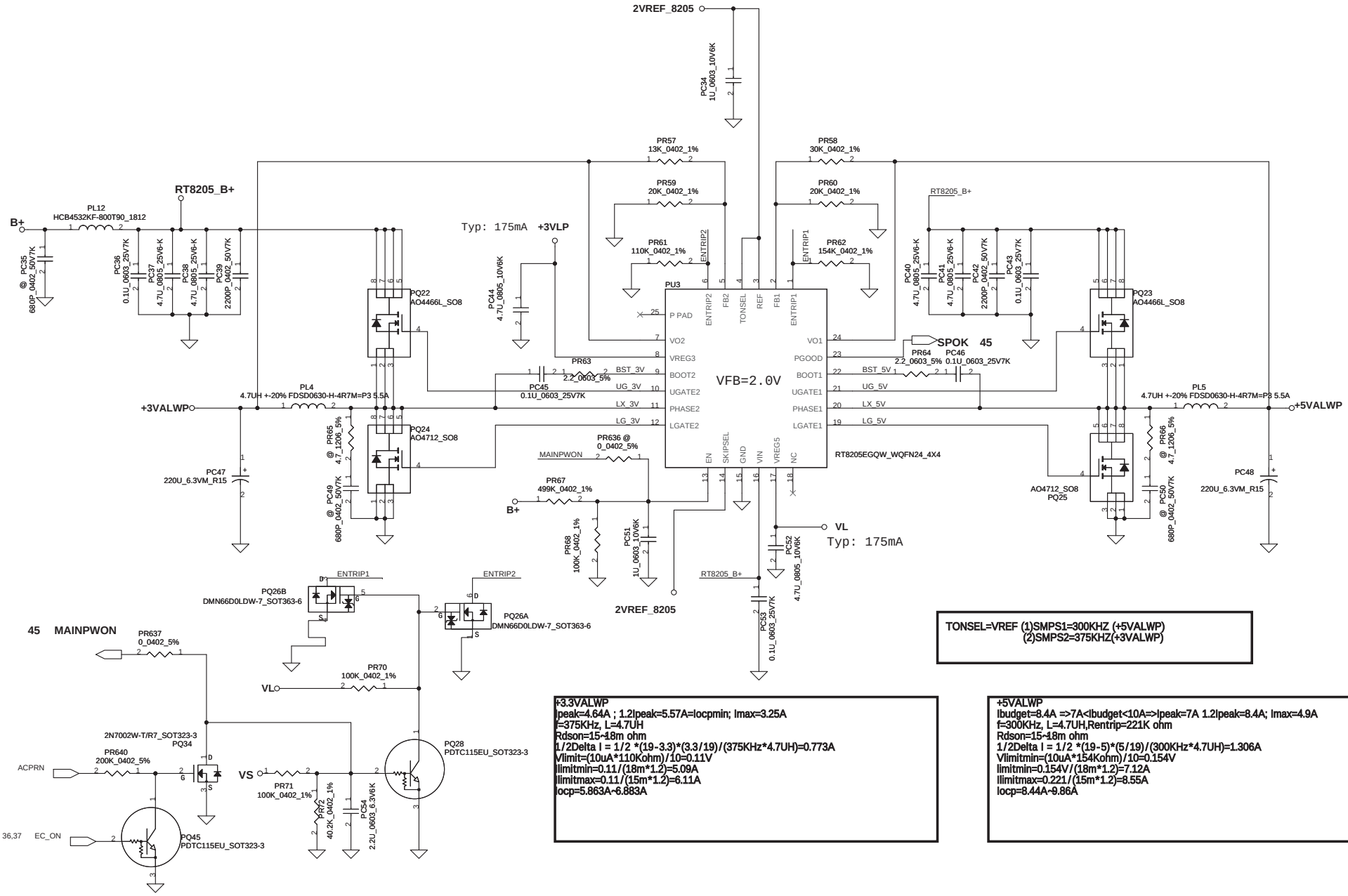
Compal Electronics, Inc.	
Title	SCHEMATIC,MB A6911
Size: Custom	Document Number: 4019A9
Rev	B
Date: Tuesday, November 09, 2010	Sheet 43 of 60



TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)
(2)SMPS2=375KHZ(+3VALWP)

+3.3VALWP
Ipeak=4.64A ; 1.2Ipeak=5.57A=Iocpmin; Imax=3.25A
f=375KHz, L=4.7UH
Rdson=15~18m ohm
1/2Delta I = 1/2 *(19-3.3)*(3.3/19)/(375KHz*4.7UH)=0.773A
Vlimit=(10uA*110Kohm)/10=0.11V
Ilimitmin=0.11/(18m*1.2)=5.09A
Ilimitmax=0.11/(15m*1.2)=6.11A
Iocp=5.863A~6.883A

+5VALWP
Ibudget=8.4A =>7A<Ibudget<10A=>Ipeak=7A 1.2Ipeak=8.4A; Imax=4.9A
f=300KHz, L=4.7UH,Rentrip=221K ohm
Rdson=15~18m ohm
1/2Delta I = 1/2 *(19-5)*(5/19)/(300KHz*4.7UH)=1.306A
Vlimitmin=(10uA*154Kohm)/10=0.154V
Ilimitmin=0.154V/(18m*1.2)=7.12A
Ilimitmax=0.221/(15m*1.2)=8.55A
Iocp=8.44A~9.86A

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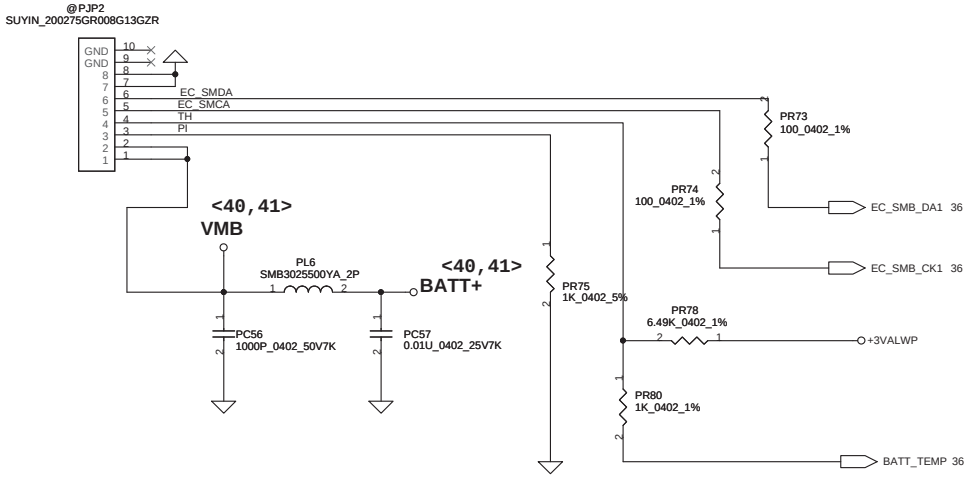
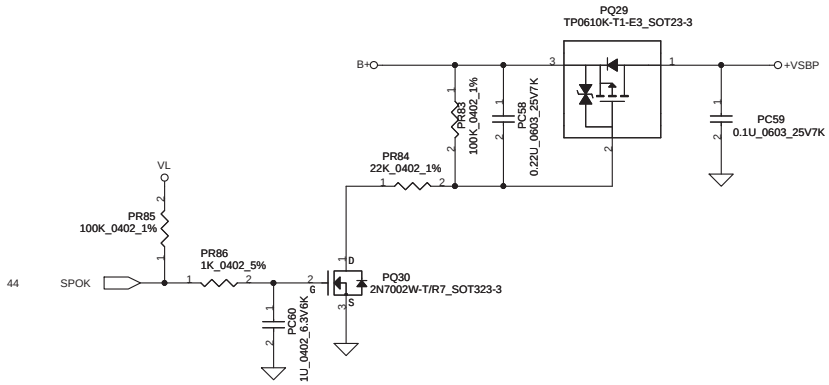
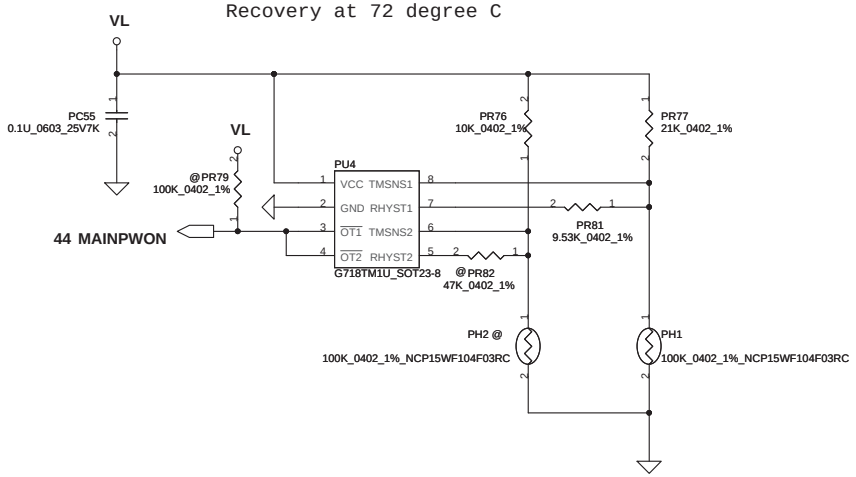
Size	Document Number	Rev
Custom	4019A9	B

Date: Tuesday, November 09, 2010 | Sheet 44 of 60

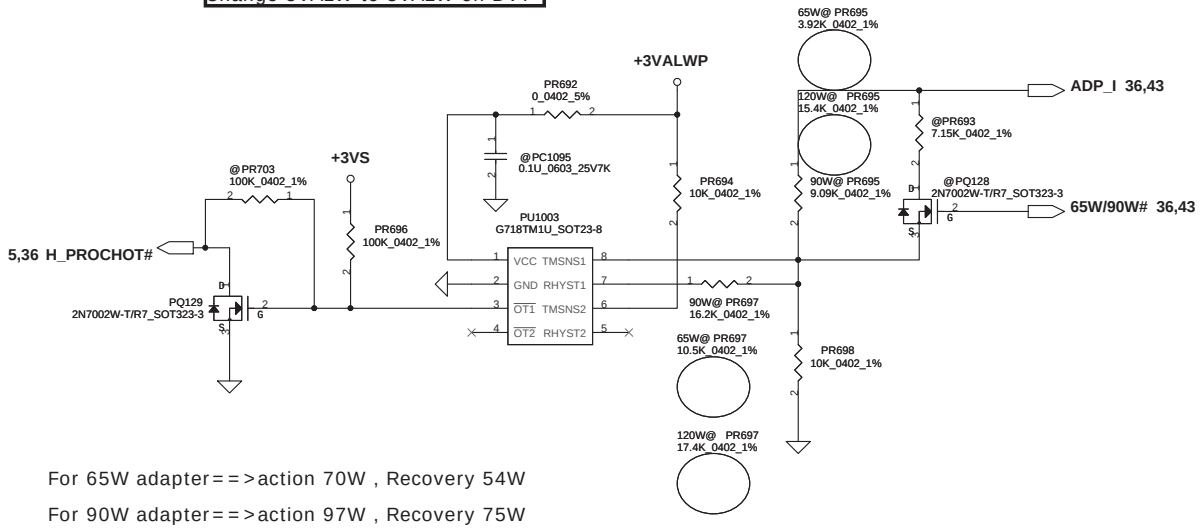




PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 72 degree C



Change 5VALW to 3VALW on DVT



For 65W adapter==>action 70W , Recovery 54W

For 90W adapter==>action 97W , Recovery 75W

For 120W adapter==>action 135W , Recovery 100W

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Issued Date	2010/07/12	Deciphered Date	2012/07/12

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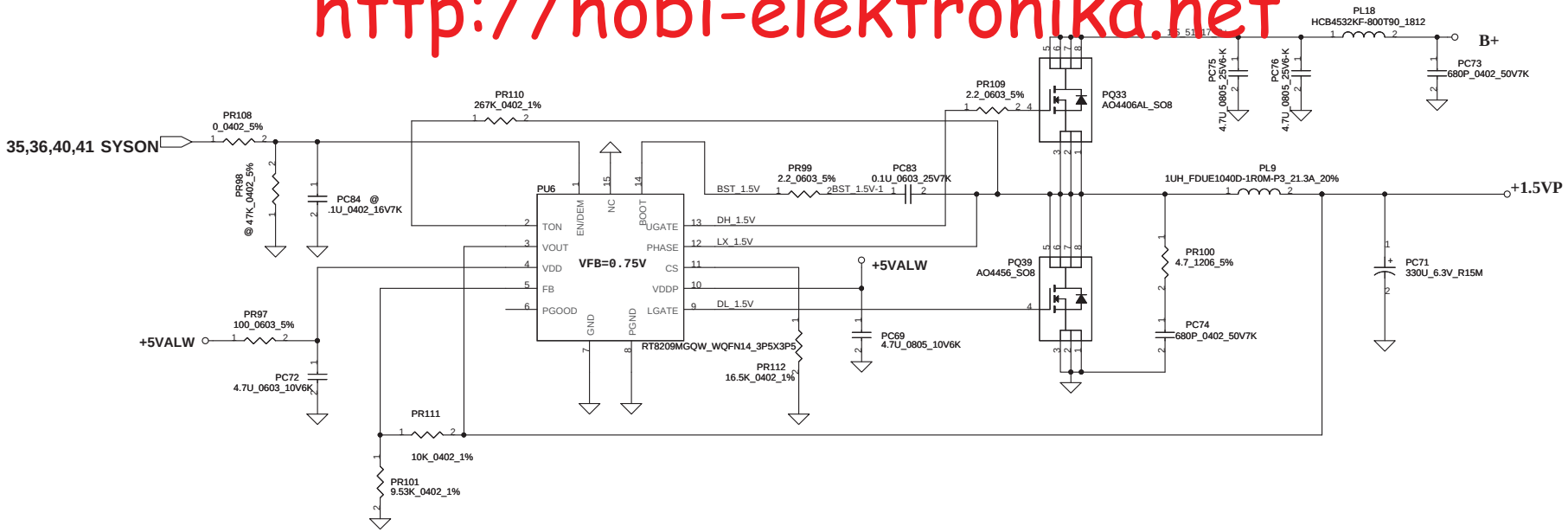
Title: SCHEMATIC,MB A6911

Size	Document Number	Rev
Custom	4019A9	B

Date: Tuesday, November 09, 2010 | Sheet 45 of 60




```
+1.5VP
Ipeak=21.56A;1.2Ipeak=25.87A ;Imax=15.09A
Rton=267K, Fsw=298KHz ,Rdson=4.5~5.6mohm
Rtrip=16.5K
Iocp=25.97A~42.41A
```

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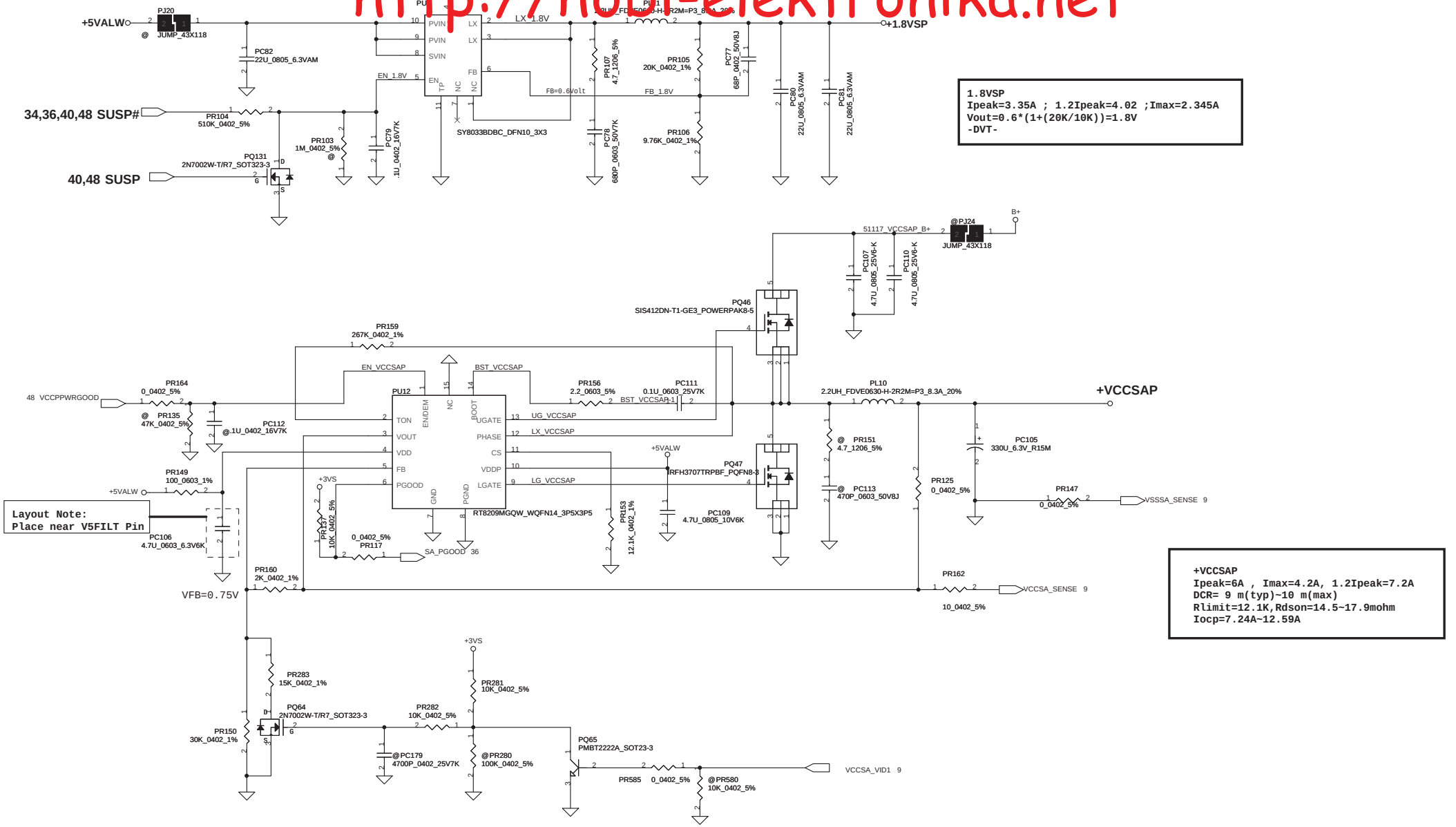
Title: SCHEMATIC,MB A6911

Size	Document Number	Rev
Custom	4019A9	B

Date: Tuesday, November 09, 2010 | Sheet 46 of 60



VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.75V	No/Yes
1	1	0.65V	No/Yes

Note:Use VCCSA_SEL to switch High & Low Level for VID[1]

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Issued Date	2010/07/12	Deciphered Date	2012/07/12

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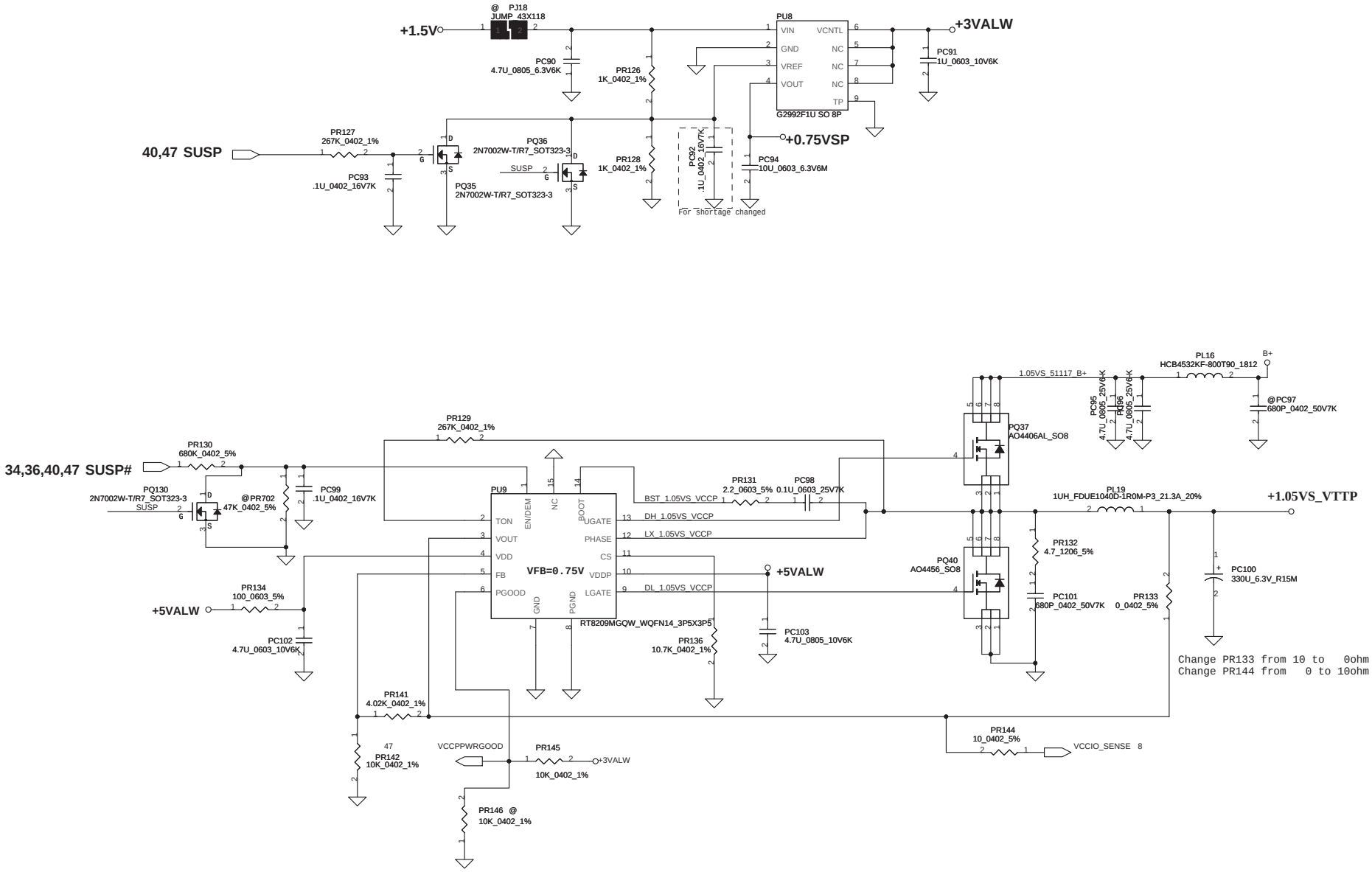
Title: SCHEMATIC,MB A6911

Size	Document Number	Rev
Custom	4019A9	B

Date: Tuesday, November 09, 2010 | Sheet 47 of 60



+1.05VS_VTTP:
Ipeak=14.05A;Imax=9.84A;1.2Ipeak=16.86A
Rdson=4.5~5.6m ohm ; Freq=298KHz
Rtrip=10.7Kohm,Vtrip<200mV
Iocp=16.99A~27.73A

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Issued Date	2010/07/12	Deciphered Date	2012/07/12

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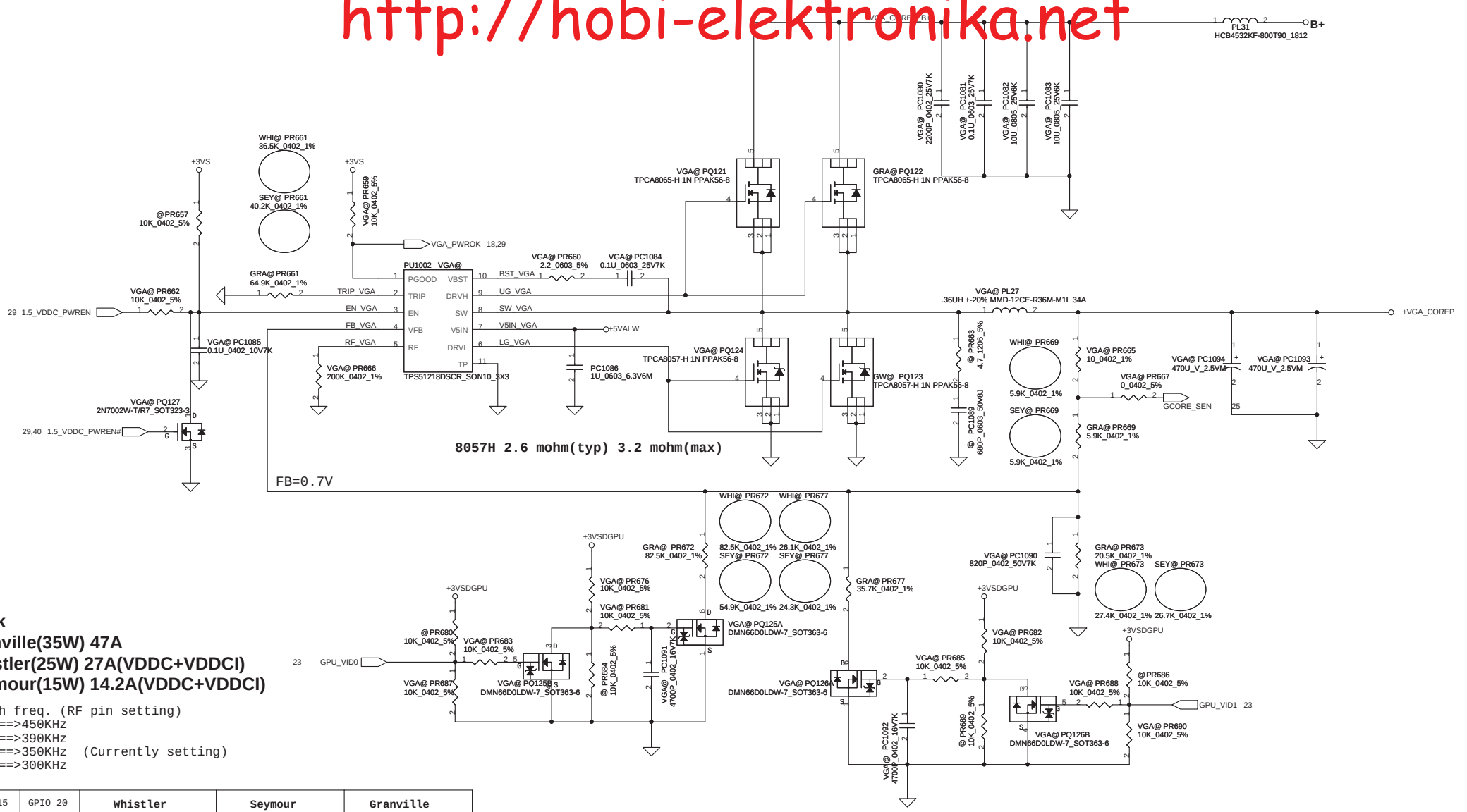
Title: SCHEMATIC,MB A6911

Size	Document Number	Rev
Custom	4019A9	B

Date: Tuesday, November 09, 2010 | Sheet 48 of 60



Ipeak
Granville(35W) 47A
Whistler(25W) 27A(VDDC+VDDCI)
Seymour(15W) 14.2A(VDDC+VDDCI)

Switch freq. (RF pin setting)
47K ==>450KHz
100K ==>390KHz
200K ==>350KHz (Currently setting)
470K ==>300KHz

GPIO 15	GPIO 20	Whistler	Seymour	Granville
GPU_VID0	GPU_VID1	Core Voltage Level	Core Voltage Level	Core Voltage Level
1	1	0.85V	0.85V(0.855V)	0.90V
0	1	0.9V	0.9V(0.930V)	0.95V
1	0	1.00V	1.00V(1.025V)	1.00V
0	0		1.1V(1.100V)	1.05V

For Granville
1/2Delta I=4.05A
Vtrip=Rtrip*Itrip=64.9K*10uA=0.649V
Iocpmin=(Vtrip/8*Rdson)+1/2Delta
=(0.649V/(8*1.6m ohm))+4.502A
=50.7A+4.05A=54.75A

For Seymour
1/2Delta I=4.31A
Vtrip=40.2K*10uA=0.402V
Iocp=0.402V/(8*3.2m)+1/2Delta I
=15.70A+4.31A=20.01A

For Whistler
1/2Delta I=4.05A
Vtrip=36.5K*10uA=0.365V
Iocpmin=0.365V/(8*1.6m)+1/2Delta I=28.51A+4.05A
=32.56A

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Issued Date	2010/07/12	Deciphered Date	2012/07/12

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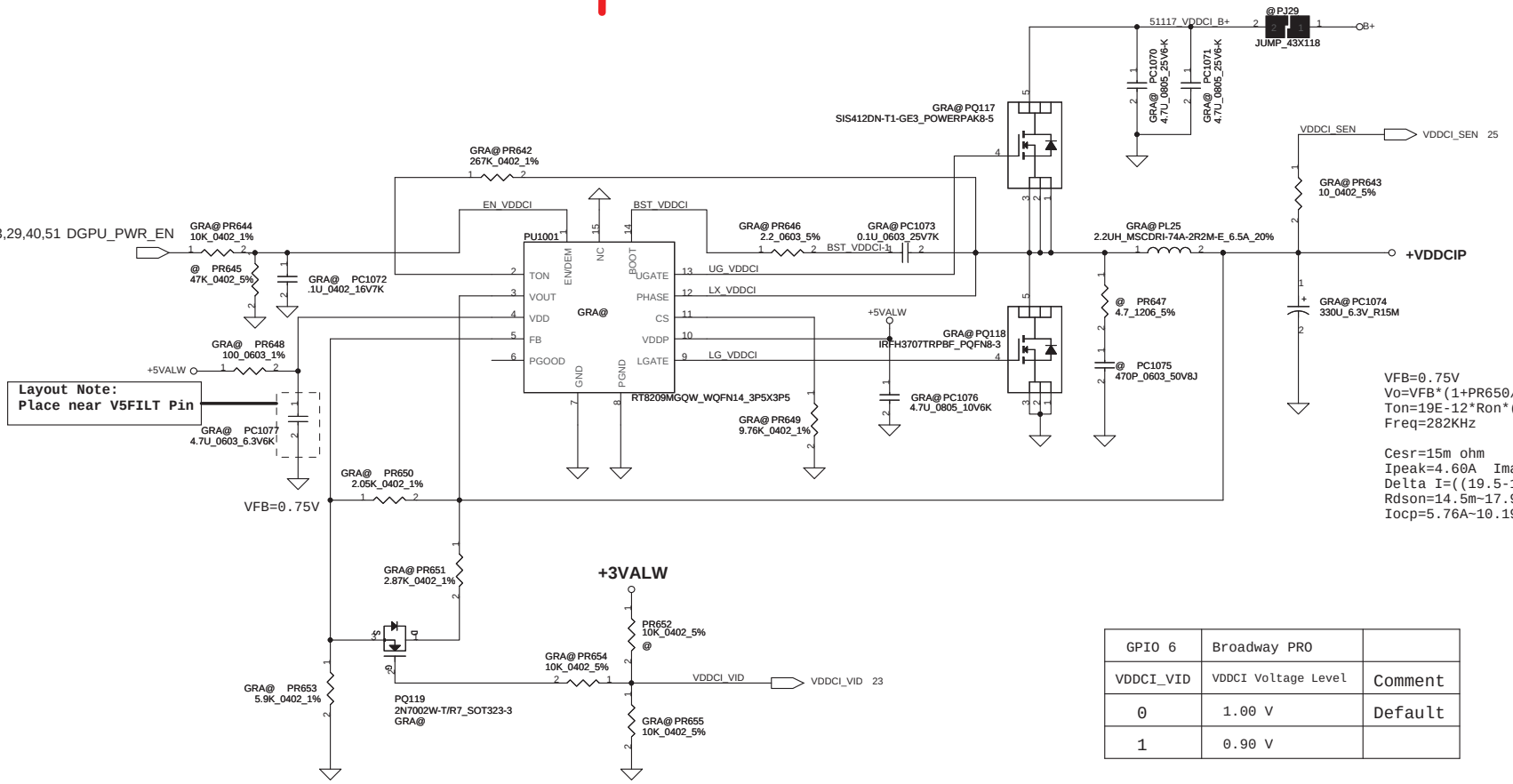
Title: SCHEMATIC,MB A6911

Size	Document Number	Rev
Custom	4019A9	B

Date: Tuesday, November 09, 2010 | Sheet 49 of 60



VFB=0.75V
Vo=VFB*(1+PR650/PR653)=1.01V
Ton=19E-12*Ron*(((2/3)*Vo+150mV)/Vin)+50ns=2.4E-7
Freq=282KHz

Cesr=15m ohm
Ipeak=4.60A Imax=2.70A 1.2Ipeak=5.52A
Delta I=((19.5-1.0)*(1.0/19.5))/(L*Freq)=1.48A
Rdson=14.5m~17.9m ohm
Iocp=5.76A~10.19A

GPIO 6	Broadway PRO	
VDDCI_VID	VDDCI Voltage Level	Comment
0	1.00 V	Default
1	0.90 V	

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

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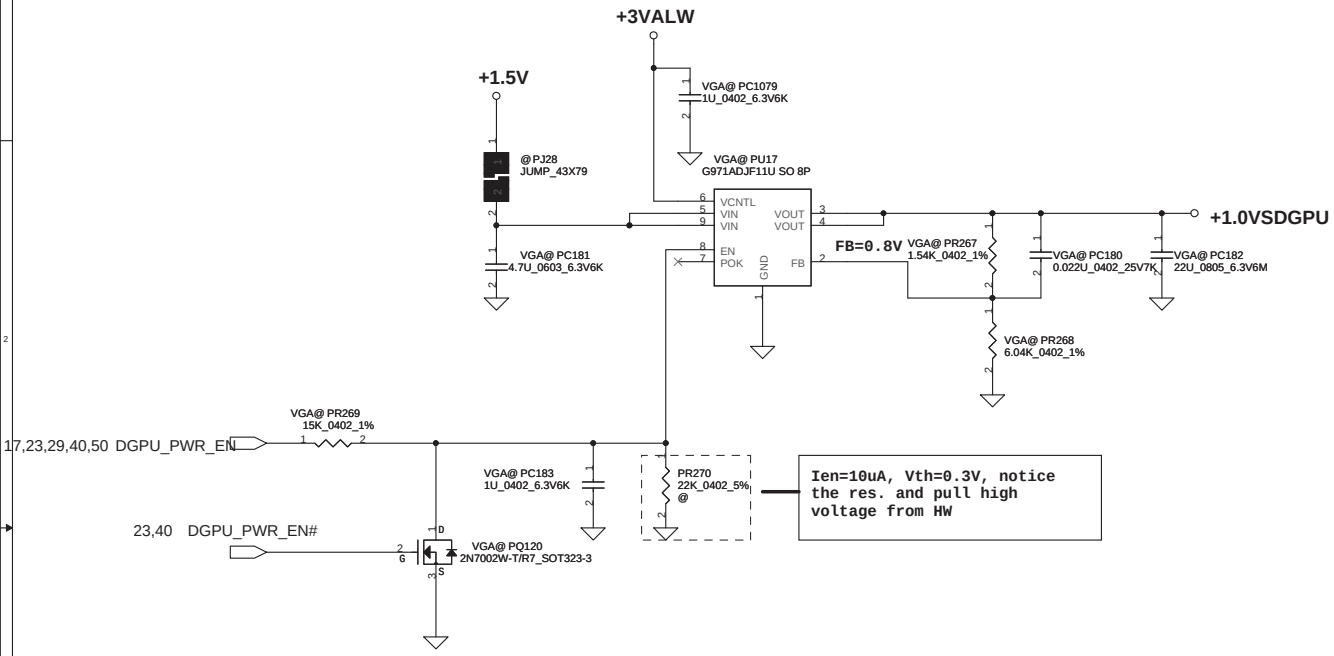
Title: SCHEMATIC,MB A6911

Size: Custom | Document Number: 4019A9 | Rev: B

Date: Tuesday, November 09, 2010 | Sheet 50 of 60



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: SCHEMATIC,MB A6911

Size	Document Number	Rev
Custom	4019A9	B

Date: Tuesday, November 09, 2010 | Sheet 51 of 60

Alert# PU resister need close CPU,
so the PU resister in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resister in POWER schematic.

DEL off page GFXVR_IMON

Parallel and tune length

change from 43P to 47P
for shortage problem
2010-03-15

ISL95831CRZ-T_TQFN48_6X6

PU1000

*Iccmax in Turbo Mode for SV (35W) is 53A

+CPU_CORE

Icc-max=53A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)10U_0805_4V *10
(2)22U_0805_6.3V *15
(3)470U_D2_2V *4(ESR=4.5m ohm)

*Dual Core OCP setting value=70A
*Qual Core OCP setting value=120A

+VGFX_COREP

Ipeak=26A , Imax=18.2A , 1.2Ipeak=31.2A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)22U_0805_6.3V *12
(2)470U_D2_2V *2(ESR=4.5m ohm)

*OCP setting value=40A

Rdroop is PR615
Ri is PR618

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Issued Date	2010/07/12	Deciphered Date	2012/07/12

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Title: SCHEMATIC,MB A6911

Size: Custom | Document Number: 4019A9 | Rev: B

Date: Tuesday, November 09, 2010 | Sheet 52 of 60

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	HW increase 1.8V voltage.	HW need to increase 1.8V voltage.	0.1	47	Change PR106 from SD034100280 to SD034976180.	2010/09/23	DVT
2	VGA Granville OVP issue.	Because VGA has happened OVP issue in Granville SKU, that is caused by outptut capacitor too small. change PC1094 to SGA00004200 to solve it. PC1088 must remove.	0.1	49	Add PC1094 to SGA00004200 and delete PC1088 SF000002O00.	2010/09/23	DVT
3	1.8V Power sequence adjust.	HW adjust 1.8V power sequence.	0.1	47	change PR104 from SD028100380 to SD028150380.	2010/09/23	DVT
4	0.75V Power sequence adjust.	HW adjust 0.75V power sequence.	0.1	48	Change PR127 from SD028150380 to SD034267380.	2010/09/23	DVT
5	adjust +1.05VS_VTT power sequence	HW adjust +1.05VS_VTT power sequence	0.1	48	Change PC99 from SE107475K80 to SE076104K80.	2010/09/23	DVT
6	adjust +VDDCI power sequence	HW adjust +VDDCI power sequence	0.1	50	Change PR644 from SD034301380 to SD034100280.	2010/09/23	DVT
7	HW request to delete PR103.	HW request to delete PR103.	0.2	47	Delete PR103 SD028100480.	2010/09/28	DVT
8	PR104 BOM error.	PR104 BOM error for power sequence.	0.2	47	Change PR104 from SD034150380 to SD034510380.	2010/09/28	DVT
9	PR669 BOM error for Seymour only.	PR669 BOM error for Seymour only.	0.2	49	Chnage PR669 from SD034681180 to SD034590180.	2010/09/28	DVT
10	To same as P5WE0 VCCSAP choke.	To same as P5WE0 VCCSAP choke.	0.2	47	Change PL10 from SH000009Q00 to SH00000M700.	2010/09/28	DVT
11	HW request to add PQ130 and PQ131 to speed up to 放電.	HW request to add PQ130 and PQ131 to speed up to 放電.	0.3	47 48	Add PQ130 and PQ131 SB000006800.	2010/10/05	DVT
12	Remove chargable RTC battery.	We reserve chargeable RTC battery to prevent over heat issue, Thermal team result is pass, so remove chargeable RTC battery.	0.3	42	Delete PR691 SD013000080 CHange PR6 from SD013560080 to SD013000080.	2010/10/05	DVT
13	Chnage PL4 and PL5 to TOKO new part.	Chnage PL4 and PL5 to TOKO new part.	0.3	44	Change PL4 and PL5 from SH000006J80 to SH00000MB00	2010/10/05	DVT
14	for ISN issue.	for ISN issue.	0.3	43	Add PL30 SH000009Q00. Delete PL28 SM010018210	2010/10/05	DVT
15	to same as P5WE0 choke.	to same as P5WE0 choke.	0.3	47	Change PL10 and PL11 from SH000009Q00 to SH00000F800	2010/10/05	DVT
16	for QC+25WGPU and QC+35W GPU change CP point.	Becasue Acer deine QC with 25W/35W GPU to be 120W SKU, change CP point to meet Acer request.	0.3	43	Delete PQ20 SB000006800. Delete PR48 SD034255180 Change PR22 from SD000001F00 to SD021100D80.	2010/10/05	DVT
17	for QC+25WGPU and QC+35W GPU change CP point.	Becasue Acer deine QC with 25W/35W GPU to be 120W SKU, change CP point to meet Acer request.	0.3	43	Change PR47 from SD034121280 to SD034100180 Change PR50 from SD034200280 to SD034511280	2010/10/05	DVT
18	Modify adapter throttling at turbo mode setting point.	Modify adapter throttling at turbo mode setting point.	0.3	45	Add PR695 SD034154280 Add PR697 SD034174280	2010/10/05	DVT
19	CPU Transient responds issue.	Change CPU transient reponds RC time constant.	0.4	52	Add PC1052 SE000003J80. Add PC1096 SE071471J80. Add PR700 SD034200180.	2010/10/07	DVT
20	for ISN issue.	for ISN issue.	0.4	43	Change PL30 from SH000009Q00 to SH00000M700.	2010/10/07	DVT
21	Make BOM same as P5WE0.	Make BOM same as P5WE0.	0.4	52	Change PL21,PL23,PL24 from SH000005680 to SH00000HK00.	2010/10/07	DVT
22	BOM loss.	Because BOM Config loss 65@ and 90W@, so miss PR695 and PR697.	0.5	45	Add PR695 SD034909180 9.09K_0402_1% ADD PR697 SD034162280 16.2K_0402_1%	2010/10/26	PVT
23	Modify CPU OCP.	Becuase original design is for 3 phase DC, now change to 2 phase DC, so modify OCP.	0.5	52	Chnage PR618 from SD034698080 to SD000009480	2010/10/26	PVT
24	Modify DC LL.	Because DC OCP was modified, must also update LL of DC.	0.5	52	Chnage PR615 from SD034215180 to SD034332180	2010/10/26	PVT

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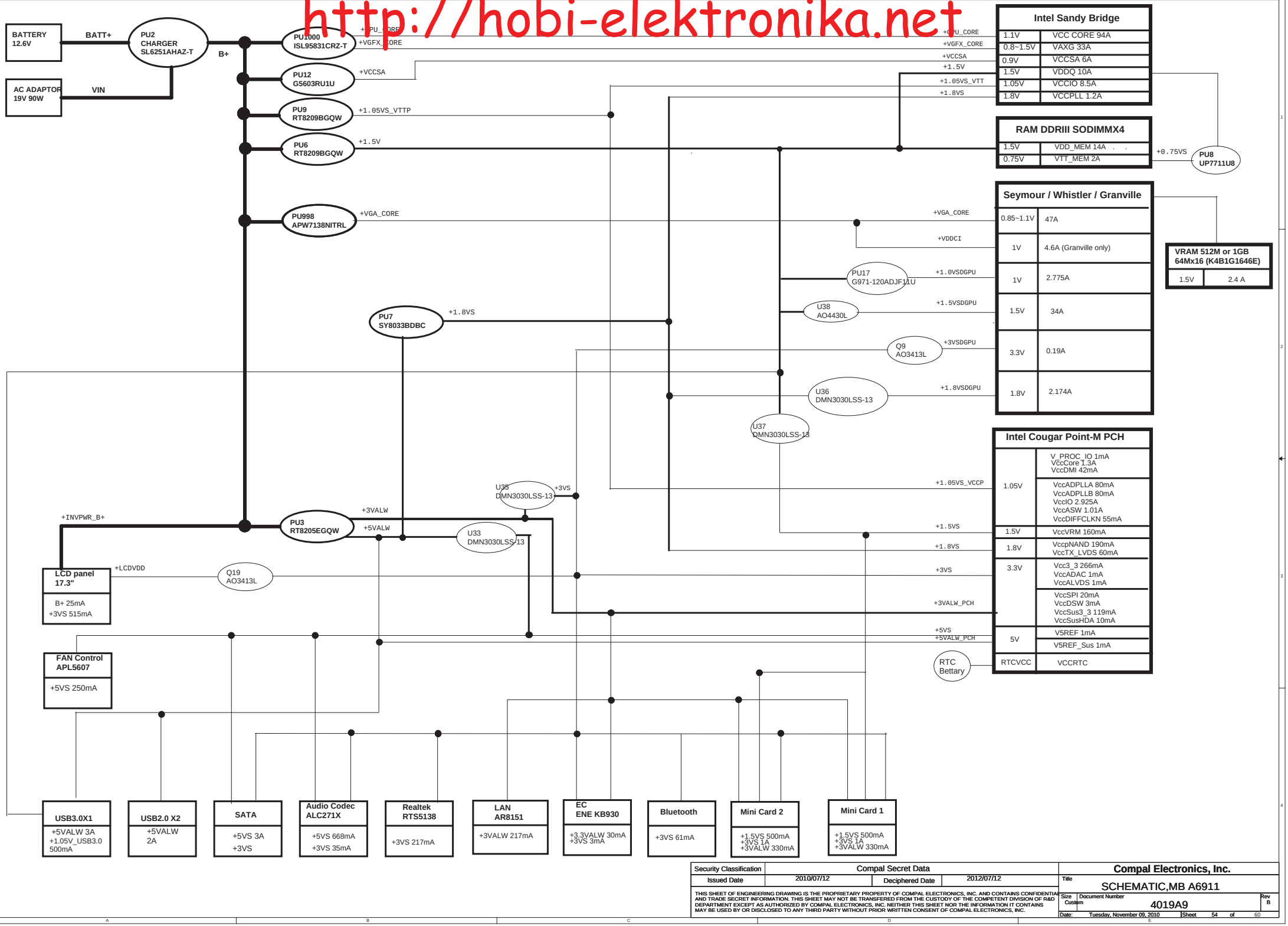
Title: SCHEMATIC,MB A6911			
Size: Custom	Document Number: 4019BE		Rev: B
Date: Tuesday, November 09, 2010	Sheet 53 of 60		



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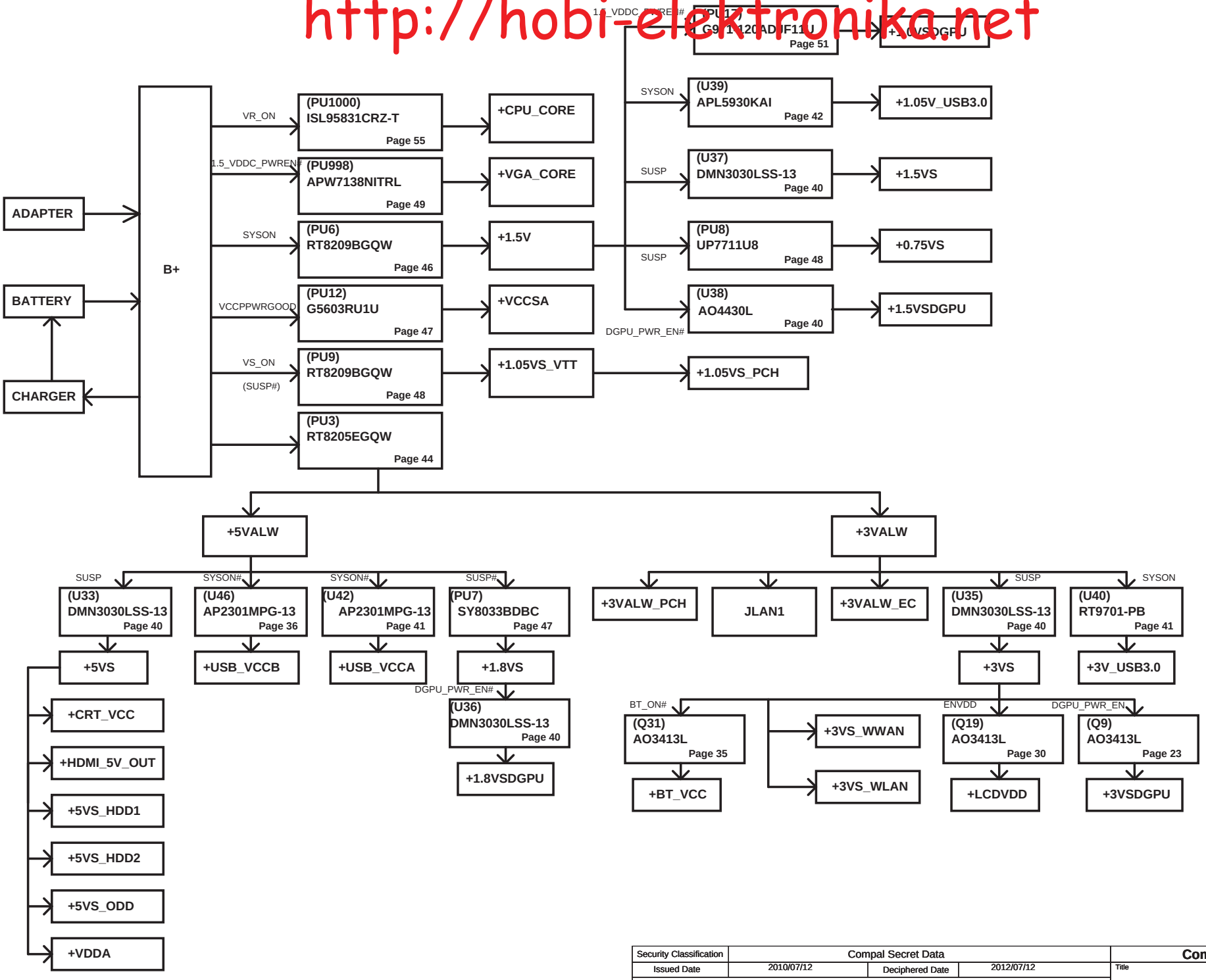
Title: SCHEMATIC,MB A6911

Size	Document Number	Rev
Custom	4019A9	B

Date: Tuesday, November 09, 2010 Sheet 54 of 60



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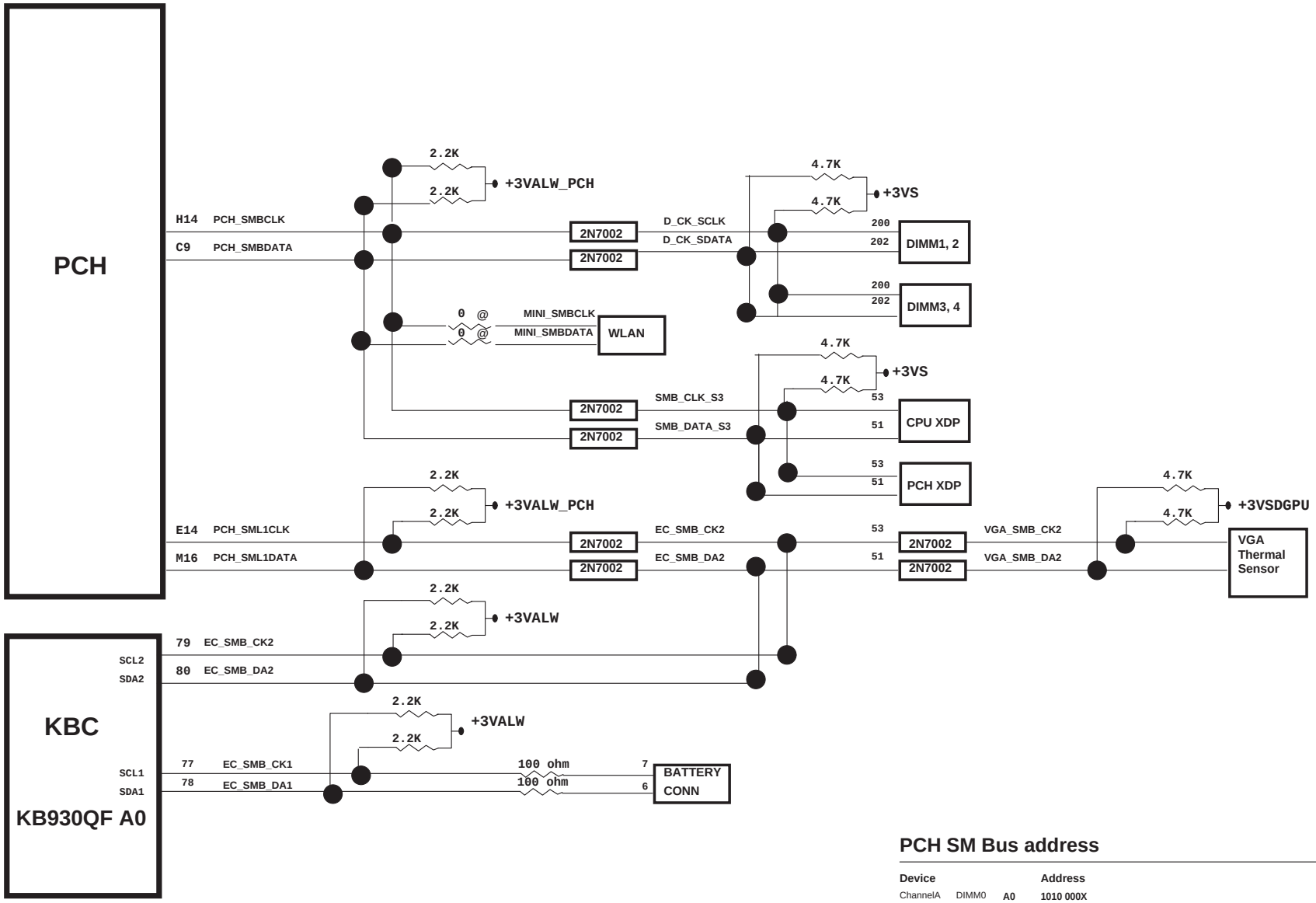
Title: SCHEMATIC,MB A6911

Size	Document Number	Rev
Custom	4019A9	B

Date: Tuesday, November 09, 2010 | Sheet 55 of 60



PCH SM Bus address

Device			Address
ChannelA	DIMM0	A0	1010 000X
	DIMM1	A2	1010 001X
ChannelB	DIMM0	A4	1010 010X
	DIMM1	A6	1010 011X

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

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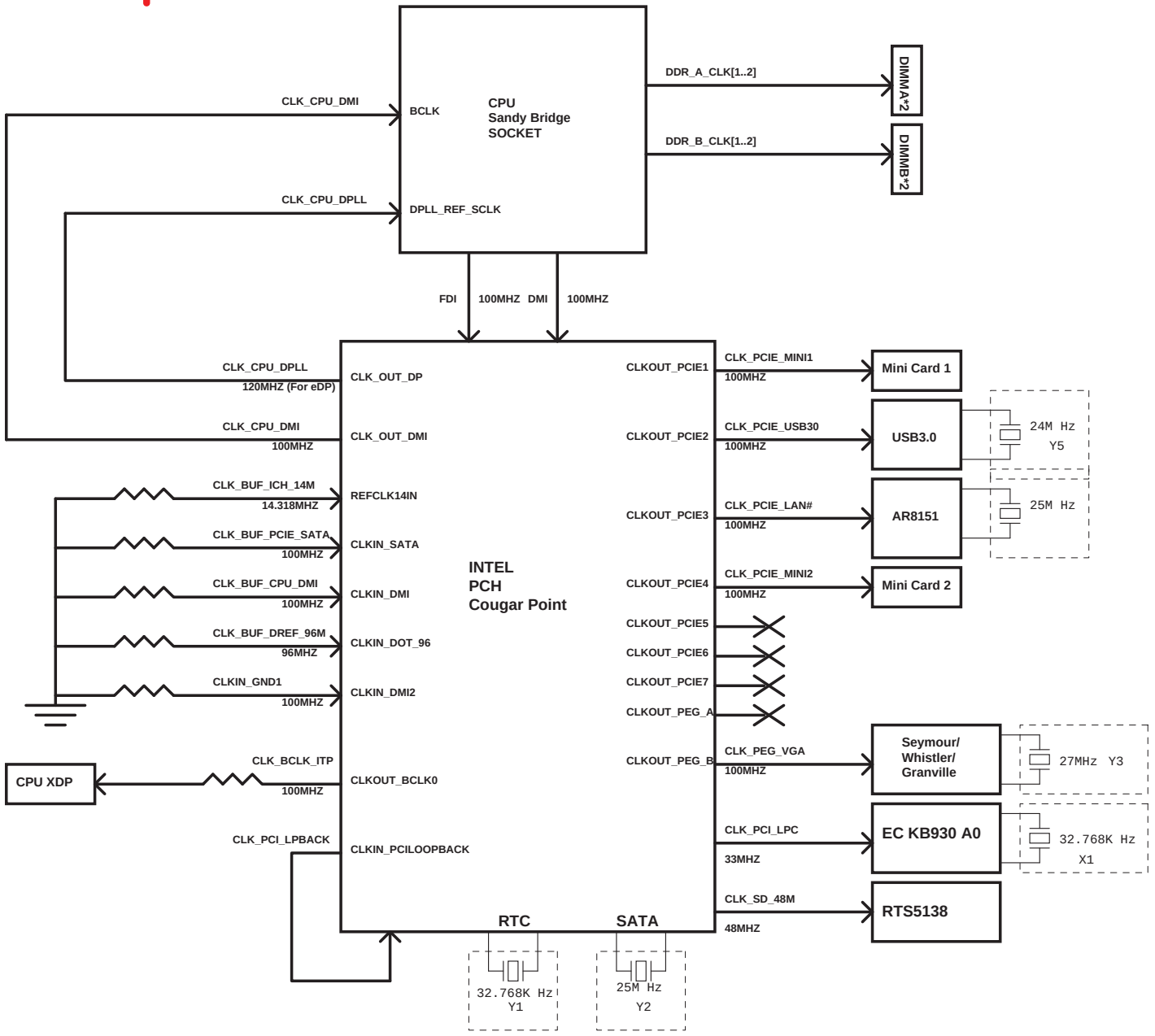
Title	SCHEMATIC,MB A6911	
Size: Custom	Document Number: 4019A9	Rev: B
Date: Tuesday, November 09, 2010	Sheet 56 of 60	



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

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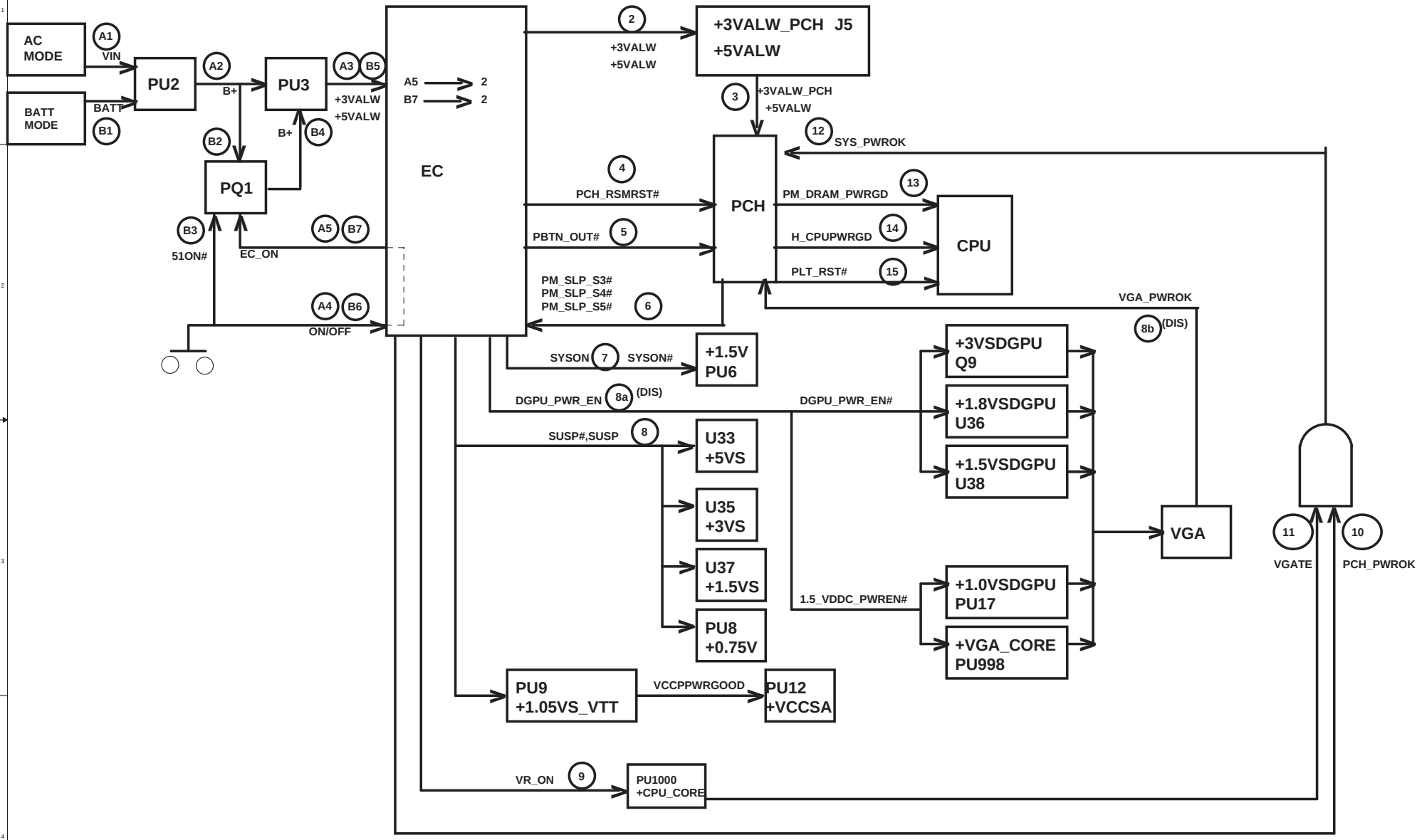
Title: SCHEMATIC,MB A6911

Size	Document Number	Rev
Custom	4019A9	B

Date: Tuesday, November 09, 2010 | Sheet 57 of 60



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Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: SCHEMATIC,MB A6911

Size	Document Number	Rev
Custom	4019A9	B

Date: Tuesday, November 09, 2010 | Sheet 58 of 60

PCB

ZZZ

LA-6911P MB Rev0: DA80000LC00
LA-6911P MB Rev1: DA80000LC10
LA-6911P MB with Small Board Rev1: DAZ

LA-69111P REV0 M/B

VGA

U30
GRAN@

Granville PRO M2 A12:
SA00004C820(S IC 216-0769024 A12 GRANVILLE PRO ABO!)

216-0769024 A12

U30
WHIS@

WHISTLER PRO M2 A11:
SA00004C720(S IC 216-0810005 A11 WHISTLER PRO FCBGA 962P ABO !)

216-0810005 A11

X76

ZZZ X76264BOL01
X761@
X76264BOL01

X76264BOL01 VRAM 512M SAM P7YE0
Samsung : SA000035720 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)
64Mx16x4 Seymour

ZZZ X76264BOL02
X762@
X76264BOL02

X76264BOL02 VRAM 512M HYN P7YE0
Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO!)
64Mx16x4 Seymour

ZZZ X76264BOL03
X763@
X76264BOL03

X76264BOL03 VRAM 1G SAM P7YE0
Samsung : SA000035720 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)
64Mx16x8 Whistler/Granville

ZZZ X76264BOL04
X764@
X76264BOL04

X76264BOL04 VRAM 1G HYN P7YE0
Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO!)
64Mx16x8 Whistler/Granville

ZZZ X76264BOL05
X765@
X76264BOL05

X76264BOL05 VRAM 2G HYN P7YE0
Hynix : SA00003VS10 (S IC D3 128M16 H5TQ2G63BFR-12C FBGA ABO!)
128Mx16x8 Whistler/Granville

ZZZ X76264BOL06
X766@
X76264BOL06

X76264BOL06 VRAM 2G SAM P7YE0
Samsung : SA00003MQ60 (S IC D3 128M16 K4W2G1646C-HC12 FBGA ABO!)
128Mx16x8 Whistler/Granville

ZZZ X76264BOL07
X767@
X76264BOL07

X76264BOL07 VRAM 1G SAM P7YE0
Samsung : SA00003MQ60 (S IC D3 128M16 K4W2G1646C-HC12 FBGA ABO!)
128Mx16x4 Seymour

ZZZ X76264BOL08
X768@
X76264BOL08

X76264BOL08 VRAM 1G HYN P7YE0
Hynix : SA00003VS10 (S IC D3 128M16 H5TQ2G63BFR-12C FBGA ABO!)
128Mx16x4 Seymour

CRT Option Components

C622 C605 C598
DISO@ DISO@ DISO@
15P_0402_50V8J
15P_0402_50V8J 15P_0402_50V8J

C623 C614 C600
DISO@ DISO@ DISO@
12P_0402_50V8J
12P_0402_50V8J 12P_0402_50V8J

15P_0402_50V8J: SE071150J80
12P_0402_50V8J: SE071120J80

L42 DISO@ 0_0805_5%
L38 DISO@ 0_0805_5%
L35 DISO@ 0_0805_5%

0_0805_5%: SD002000080

R307 DISO@ 1K_0402_5%

DIS only PCH DAC_IREF
can use 1K_0402_5% PD to GND

DIS EDP Option Components

R23 DEDP@ .1U_0402_16V7K TXOUT_2P = DP0P
R17 DEDP@ .1U_0402_16V7K TXOUT_2N = DP0N

R24 DEDP@ .1U_0402_16V7K TXOUT_1P = DP1P
R22 DEDP@ .1U_0402_16V7K TXOUT_1N = DP1N

R9 DEDP@ .1U_0402_16V7K I2CC_SCL = AUXP
R7 DEDP@ .1U_0402_16V7K I2CC_SDA = AUXN

Granville VGA_CORE CAP Option

C591 GRAN@ 470U_X_2VY_R9M
C604 GRAN@ 470U_X_2VY_R9M

SGA00003N00
S POLY C 470U 2V Y X
LESR9M S H1.9

EC susclk/crystal Option Components

C504
100K_0402_5%

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Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: SCHEMATIC,MB A6911

Size	Document Number	Rev
Custom	4019A9	B

Date: Tuesday, November 09, 2010 Sheet 60 of 60

0923:
rework
ADD Q8 DMN66D0LDW-7(SB00000DH00) & change BOM structure to DIS@(DIS@ Granville can't power on issue)
R72 100K_0402_5%(SD028100380)change BOM structure to DIS@(DIS@ Granville can't power on issue)
R674 4.7K PH change BOM structure to @(+3VS GPIO19 leakage)
D31 change BOM structure to @(EC debug CLK leakage)
R531,R530 change BOM structure to DISO@(HSYN:VSYNC 11: Audio for both DisplayPort and HDMI)
ADD C591 C604 BOM option
(Seymour/Whistler option NOGRAN@ SGA20331E10 S POLY C 330U 2V 9mohm H1.9)
(Granville option GRAN@ SGA00004200 S POLY C 470U 2V M D2 LESR4.5M SX H1.9)
C746,C750 change from SF000001500 to SF000001580

Power sequence:
1. BOT (adjust +5VS power sequence)
  R698 change from 200K to 100K_0402_5% (SD028100380)
2. BOT (adjust +1.8VS power sequence)
  PR104 change from 100K to 510K_0402_5%(SD028510380)
  remove PR103 1M_0402_5%
3. TOP (adjust +1.5VS power sequence)
  R67   change from 510K_0402_5% to 750K_0402_5%(SD028750380)
4. TOP (adjust +0.75VS power sequence)
  PR127 change from 150K_0402_5% to 267K_0402_1%(SD034267380)
5. TOP (adjust +1.05VS_VTT power sequence)
  PC99 change from 4.7U to .1U_0402_16V7K (SE076104K80)
6. TOP (adjust +1.5VSDGPU power sequence)
R113 510K change to 100K_0402_1% (SD034100380)
7. BOT (adjust +VDDCI power sequence)
PR644 301K change to 10K_0402_1% (SD034100280)

Power:
PR101 change from 10K to 9.53K (adjust +1.5V power)
PR106 change from 10K to 9.76K (adjust +1.8VS power)
Layout:
D21 channge to SC600000B00 (for sourcer 2nd source)
DEL C590,C603 (DEL colay Cap)
L24,25,27,30,31 change from SM010004010 to SM010015410
BATT Blue light place at front side
H1 change H3P0 to H4P6
DEL LED1,LED2,LED3,LED4

0924:
Q37,Q39,Q40,Q41, change from SB00000FG00 to SB00000FG10
U7 change from SB000007O00 to SB000007O10
USB3.0 schmetic change to unpop
XDP change to unpop
U19 A10,N10,P10,B12 connect to GND

0925:
R249 change from U15.2 to U15.1(footprint issue)
R105 change form 10K to 10_0402_5%(SD028100A80)
R422 change BOM structure to @(crystal issue debug port1.2)
R422 change +3VS to +3VALW_PCH (GPIO28)
R674 change BOM structure to @(leakage issue debug port1.2)
R674 change +3VALW_PCH to +3VS (GPIO19)
ADD LED11 pop WLAN_LED#(SC500007700),LED12 @ MEDIA_LED#(SC591NB5A30)
LED10 WLAN_LED#(SC500007700) change BOM structure to @
DEL D9,D10 USB3.0 old ESD diode
ADD D32 new USB3.0 ESD diode (SC300001D00)
DEL R238,R250,C401 USB3.0 conn PD resister & CAP
EMI request:
R595,R596 change to @ L47 change to POP(USB2.0 common mode choke)

0927:
Audio vender suggest:
C913 change BOM structure to @
ADD C702 22K_0402_5%(SD028220280)
change USB conn to USB2.0(SUYIN_020133GB004M25MZL_4P-T)
modify Debug port note(GPIO19 PH +3VS GPIO28 PH +3VALW_PCH)
R667,R666 change BOM structure to @(XDP CLK source)
change SW4,SW5 BOM structure to @ (debug PWRBTN)
change R432,R435,R437 from 1K_0402_5% to 300_0402_5%(orange LED resister)
change USB3.0 schmetic BOM structure back to USB3@
C746,C750 change from SF000001500 to SF000001580
D4,D5 change from SCSH491D010(S SCH DIO CH491DPT SOT-23) to SCS00002000(S SCH DIO RB491D SOT-23 PANJIT)
Q29,Q33,Q36 change from SB934130020(S TR AO3413L 1P SOT23-3) to SB000006R10(S TR AO3419L 1P SOT23-3)

0928:
DEL R468
JMINI1.24 change power source from +3VS to +3VS_WLAN
DEL R613
JMINI2.24change power source from +3VS to +3VS_WWAN
DEL R352
change power source from +XDPWR_SDPWR_MSPWR to +CARDPWR
Q21 change from SB324110080(2SC2411K) to SB039040020(MMBT3904)
Change JUSB2 footprint to "SUYIN_020173GB004M25MZL_4P"
ADD R613 1M PD to GND(HDA_SYNC_PCH_R)
ADD SLP_A#   at U37.G10 test point(for DFT request)
ADD JTAG_TDI at U30.AN23 test point(for DFT request)
ADD JTAG_TDO at U30.AM24 test point(for DFT request)
JREAD1 change conn from TAITW_R013-P12-HM_44P_NR to TAITW_R013-P17-HM_40P_NR

0930:
DEL Rechargerable RTC Schmatic R47,R427,C561
0930:
R534,R540 change from 100_0402_1% to 1K_0402_5%(SD028100180)(DG1.5 change save cost)
C744,C745 change from 18P_0402_50V8J to 27P_0402_50V8J(SE071270J80)(25Mhz Crystal modify)
R357,R358,R330,R331,R345,R346,R387,R393,R292 change BOM structure to @ (10K_0402_5%)PD to GND(DG1.5 unuse CLK NC)
R666,R667 change BOM structure to @(XDP unuse)
R573,R575,R571,R572,R562,R566,R567,R570 DEL option 499_0402_1% leave 680_0402_5%
R318,R332 change from 0ohm to 22_0402_5%(SD028220A80)
C448,C483 change to 4.7P_0402_50V8J(SE07147AC80)
L47 change to 67ohm common mode choke CHENG HANN WCM2012F2SF-670T04(SM070000S80)

1025:
R370,R413 change from SD028100380(100K_0402_5%) to SD028200380(200K_0402_5%)
PCH_GPIO1 change net to WL_EN#
LVDS
Add +5VS (Pin34) & USB20_N4/P4 (Pin35, 36)
change EDP_HPD to Pin18
PCH side add USB20_N4/P4 (Pin35, 36)

For eDP interface AUX channel, please request Layout routing as differential signal to follow eDP Layout Guide.
(VGA_LCD_CLK & VGA_LCD_DATA / I2CC_SCL & I2CC_SDA)

DEL DDR DM
R50,R58,R59,R48,R56,R51,R60,R49 DIMMA
R39,R52,R44,R43,R46,R38,R45,R40 DIMMA
R77,R73,R109,R112,R180,R181,R192,R206 DIMMB
R64,R83,R108,R115,R179,R183,R189,R208 DIMMB

1026:
C604,C591 change from SGA00004200(470 4.5mohm)to SGA00003N00(470 9mohm)
Pop R257(SD028100380 100K_0402_5%),R622(SD028820180 8.2K_0402_5%) Board ID
R443 change from 100K_0402_5% to 10K_0402_5% (SD028100280)

remove R471,R622(JMINI1,JMINI2 Pin42 0ohm series resister)
J1,J2 change location to J6,J7
remove R222 0ohm_0402 (H_CPUPWRGD_R)
remove R423,0ohm_0402 (MINI1_CLKREQ#_R)
remove R392 0ohm_0402 (LAN_CLKREQ#_R)
remove R685 0ohm_0402 (MINI2_CLKREQ#_R)
remove R655 0ohm_0402 (WAKE#)
remove R636 0ohm_0402 (PCH_RSMRST#)
remove R377 0ohm_0402 (SUS_PWR_DN_ACK)
remove R339 0ohm_0402 (PBTN_OUT#)
remove R359 0ohm_0402 (DGPU_HOLD_RST#)
remove R16 0ohm_0402 (BKOFF#)
remove R448 0ohm_0402 (VGA_EDP_DET)
remove R533 0ohm_0402 (VGA_HDMI_DET)
remove R627 0ohm_0603 (+SPI_VCC)

ADD R39 0ohm_0402 LOCAL_DIM
ADD R38 0ohm_0402 COLOR_ENG_EN

C242,C653,C332,C354,C678 change footprint to C_X(2pin)

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Title	SCHEMATIC,MB A6911	
Size: Custom	Document Number: 4019A9	Rev: B
Date: Tuesday, November 09, 2010	Sheet 59 of 60	