

Compal confidential

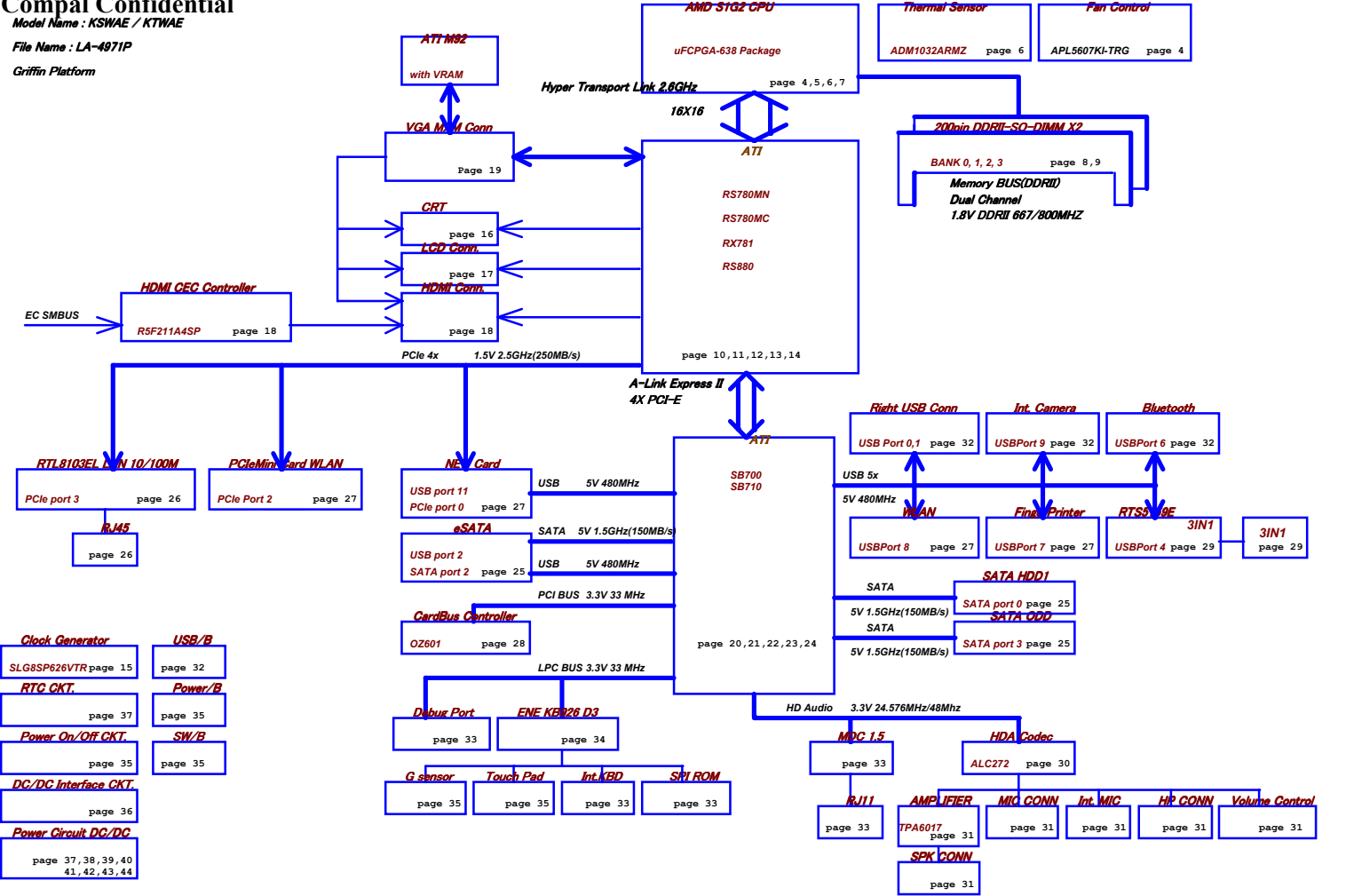
Liverpool 10AR/10ARG

KSWAE LA-4971P Schematics Document

Mobile AMD S1G2 S1G3/
RS780MN & RS780MC & RX781 & RS880 /
SB700 & SB710

2009-04-22 Rev. 1.0

Security Classification	Compal Secret Data		Title	
Issued Date	2008-09-25	Deciphered Date	2009-09-25	<i>Compal Electronics, Inc.</i> <i>Cover Sheet</i>
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				Document Number <i>LA-4971P</i>
				Rev 1.0
				Date: Wednesday, April 22, 2009
				Sheet 1 of 45



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power plane

State

+B

+3VL

+5VL

+RTCVCC

+5VALW

+3VALW

+1.2VALW

+3V_LAN

+1.8V

+0.9V

+0.9V

+5VS

+3VS

+2.5VS

+1.8VS

+1.5VS

+1.1VS

+VGA_CORE

+1.2V_HT

+CPU_CORE_NB

+CPU_CORE_0

+CPU_CORE_1

S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: Digital Ground

: Analog Ground

@ : just reserve , no build

DEBUG@ : reserve for debug.

Layout Notes

UMA@: means for RS780M.

Platform	Item	CPU	NB	VGA	SB	Comment
PUMA@	GM@	S1G2	RS780MC	NA	SB700	
	GM@	S1G2	RS780MN	NA	SB700	
	PM@+GPM@	S1G2	RS780MN	MXM	SB700	
	PM@+PM1@	S1G2	RX781	MXM	SB700	

Platform	Item	CPU	NB	VGA	SB	Comment
TIGRIS@	GM@	S1G3	RS880MC	NA	SB710	
	GM@	S1G3	RS880M	NA	SB710	
	PM@+GPM@	S1G3	RS880M	MXM	SB710	
	PM@+PM1@	S1G3	RX881	MXM	SB710	

Function	Express card / PCMCIA	BLUE TOOTH	RJ11	SSD	SATA ODD		WIFI		G- sensor		3 in 1 card reader
Description	(E / A)	(B)	(R)	(S)			(H)				
Explain					16"	17"	Half - size		First	Second	RTS5159
BTO	EXPCARD@ / PCMCIA@	BT@	MDC@	SSD@	16inch@	17inch@	WLAN@	WIMAX@	G@ + G_1st@	G@ + G_2nd@	CARD@

Function	FingerPrinter	CAMERA & MIC	HDMI		LVDS wireset	DC-IN	CHIPSET				
Description	(F)	(X)	(Y)								
Explain		CAMERA MIC	AMD(UMA)	ATI VGA/B	COMMON	Cost down					
BTO	FP@	CAM@	MIC@	IHDMI@	HDMI@	H@	LVDSSET@	16inch_45@	17inch_45@	PUMA@	TIGRIS@

SBMUS Control Table

	SOURCE	INVERTER	BATT	HDMI CEC	CPU THERMAL SENSOR	SODIMM I / II	CLK GEN	WLAN	LCD DDC ROM	HDMI DDC ROM	NEW CARD	MXM Thermal Sensor
EC_SMB_CK1	KB926		V	V								
EC_SMB_DA1												
EC_SMB_CK2	KB926				V							V
EC_SMB_DA2												
I2C_CLK	RS780M								V			
I2C_DATA												
DDC_CLK0	RS780M									V		
DDC_DATA0												
DDC_CLK1	RS780M											
DDC_DATA1												
SCL0	SB700					V	V				V	
SDA0												
SCL1	SB700							V				
SDA1												
SCL2	SB700											
SDA2												
SCL3	SB700											
SDA3												

EC SM Bus1 address

Device	HEX	Address
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

EC SM Bus2 address

Device	HEX	Address
ADH1032-1 CPU	98H	1001 010X b
ADH1032-2 VGA	9AH	1001 101X b
EC KB926D2		
Ext. VGA/B		
CS/B		

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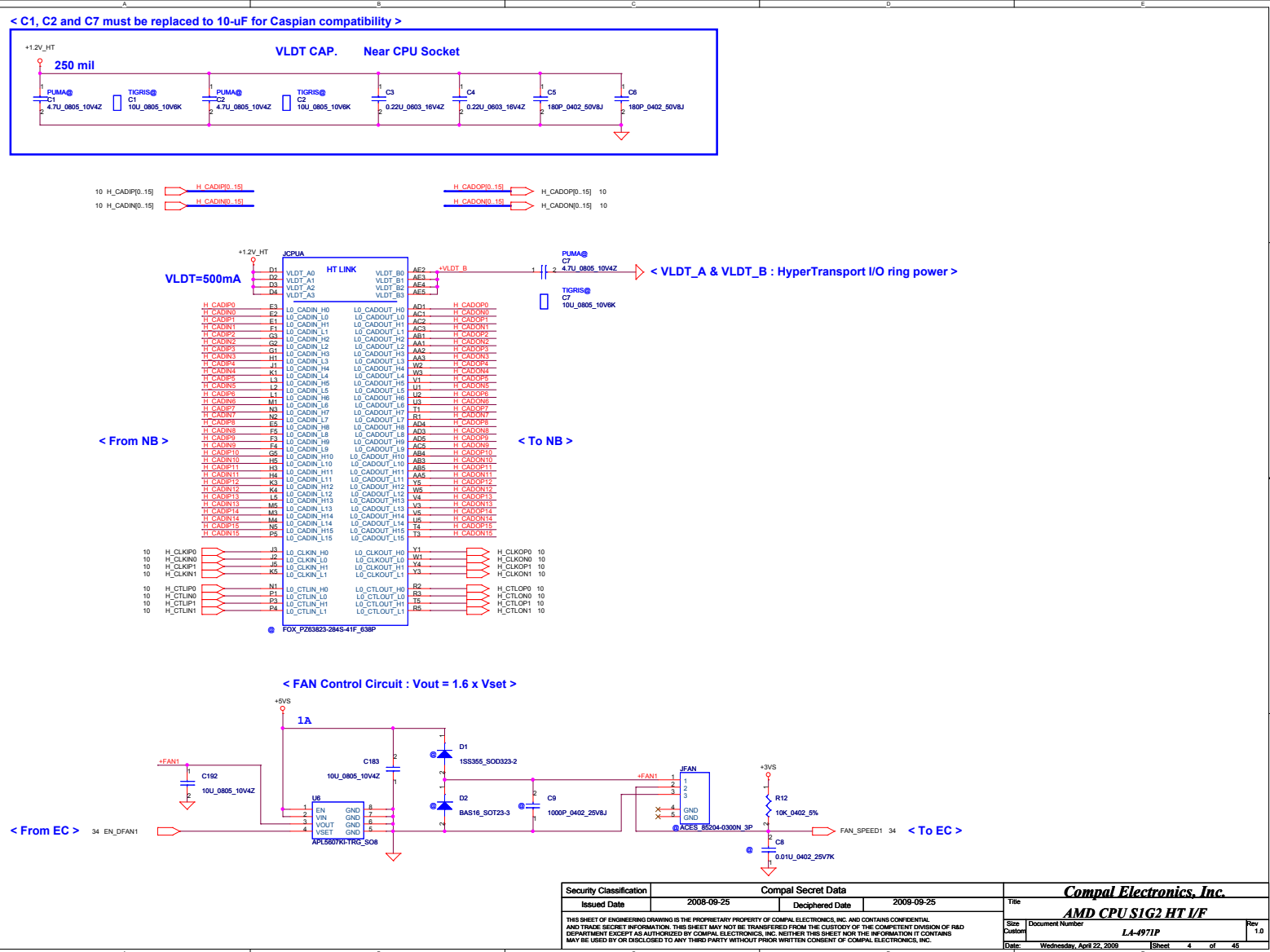
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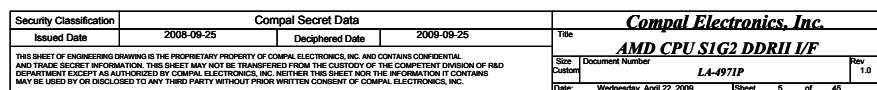
TitleCompal Electronics, Inc.

Notes List

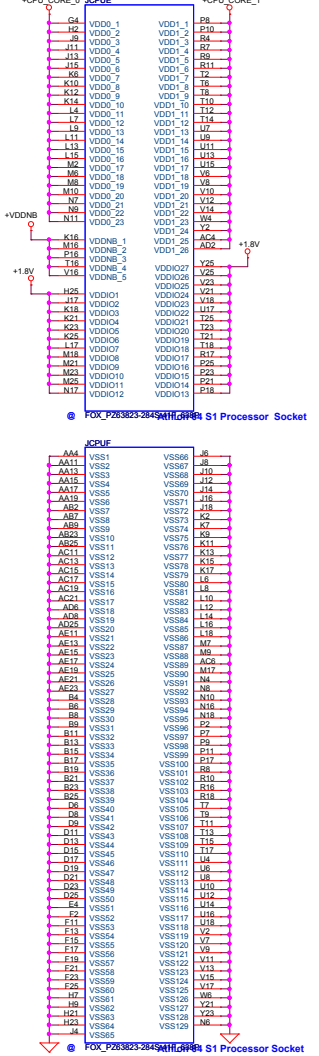
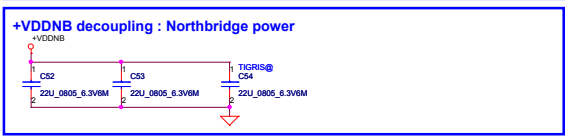
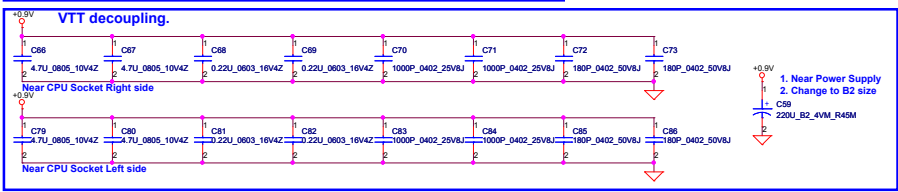
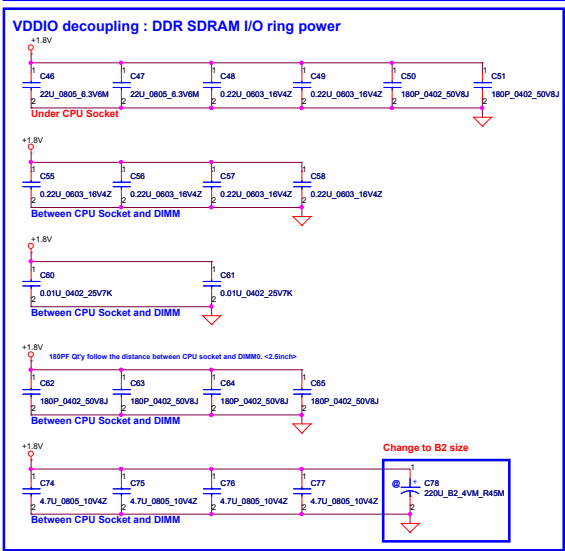
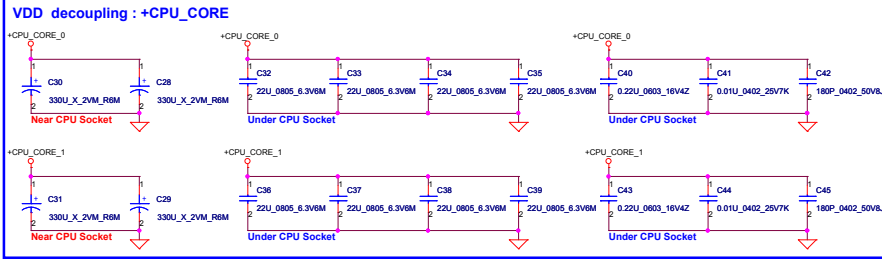
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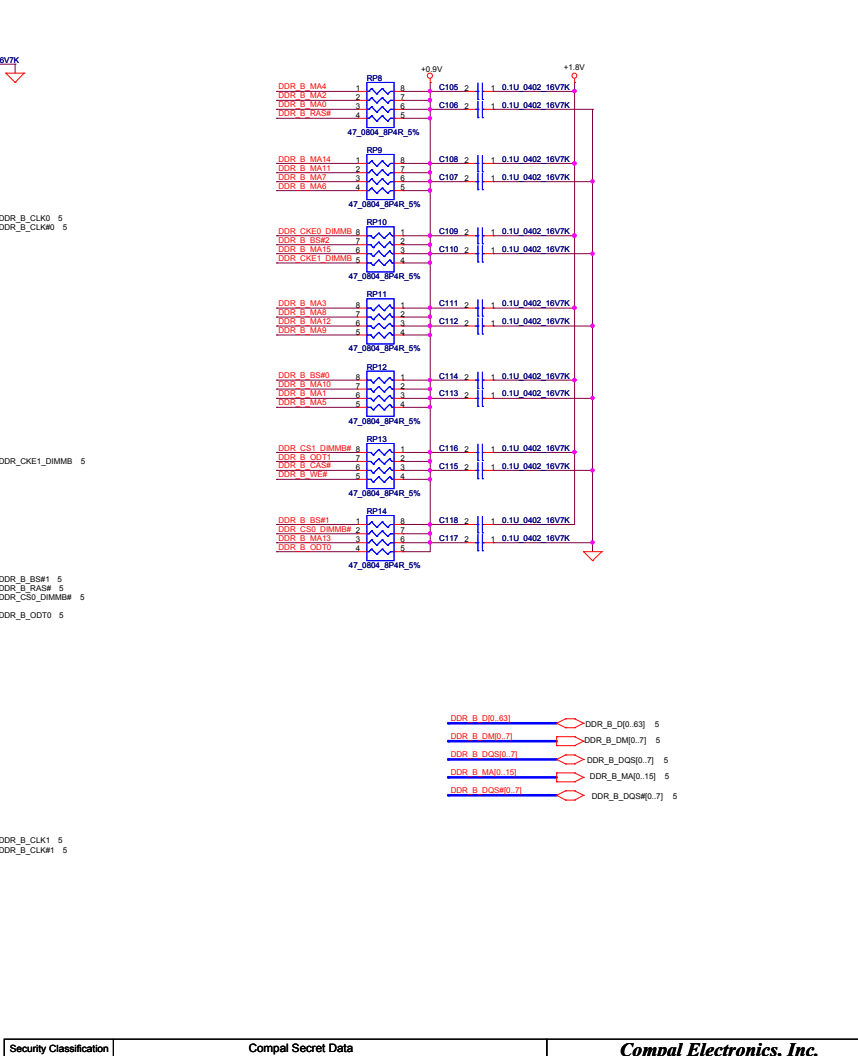
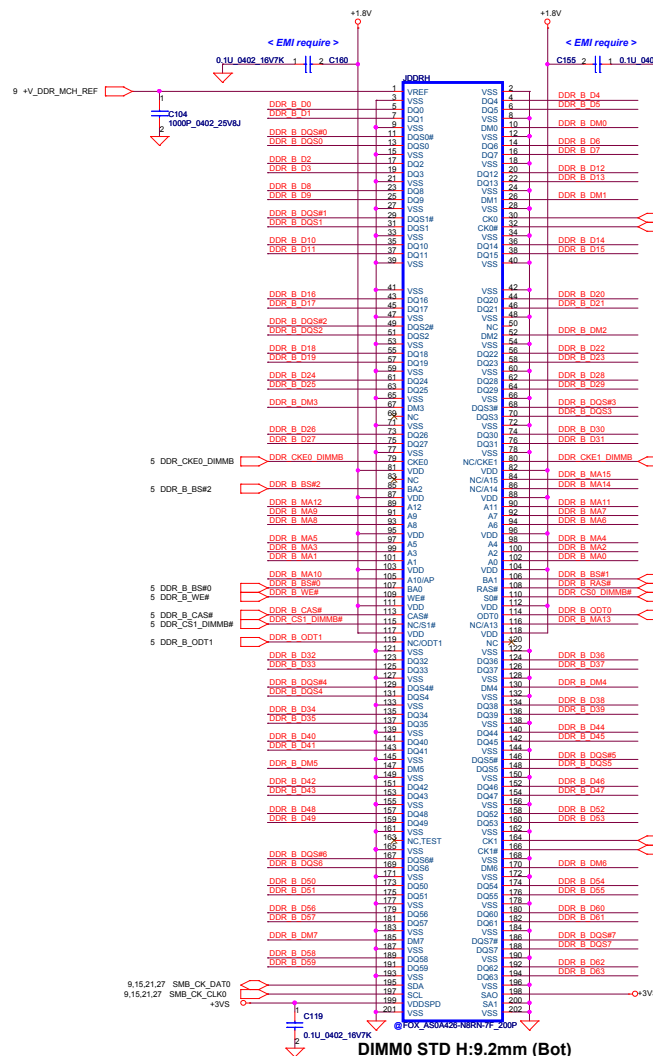




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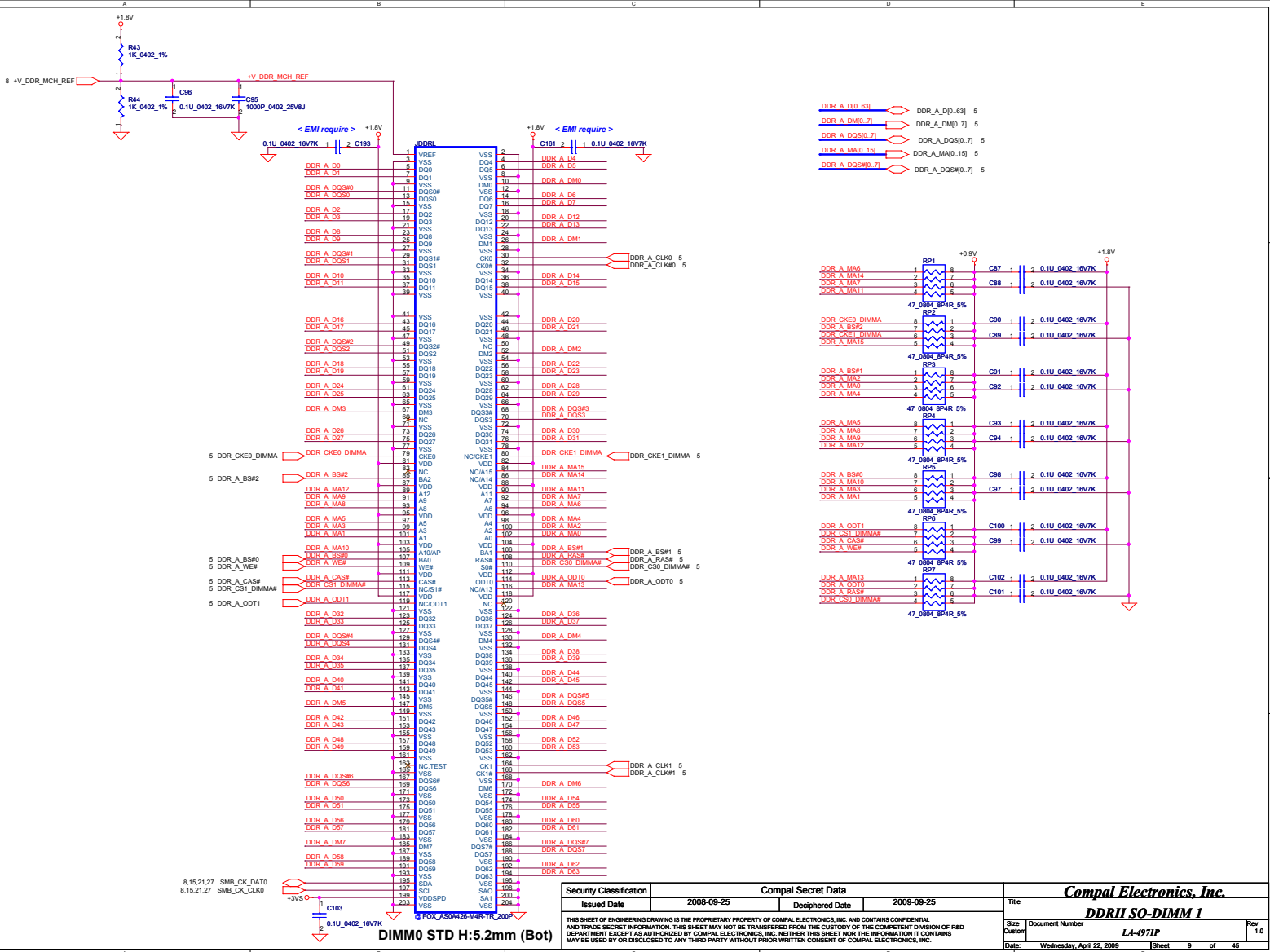


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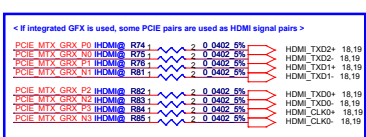


DIMM0 STD H:9.2mm (Bot)

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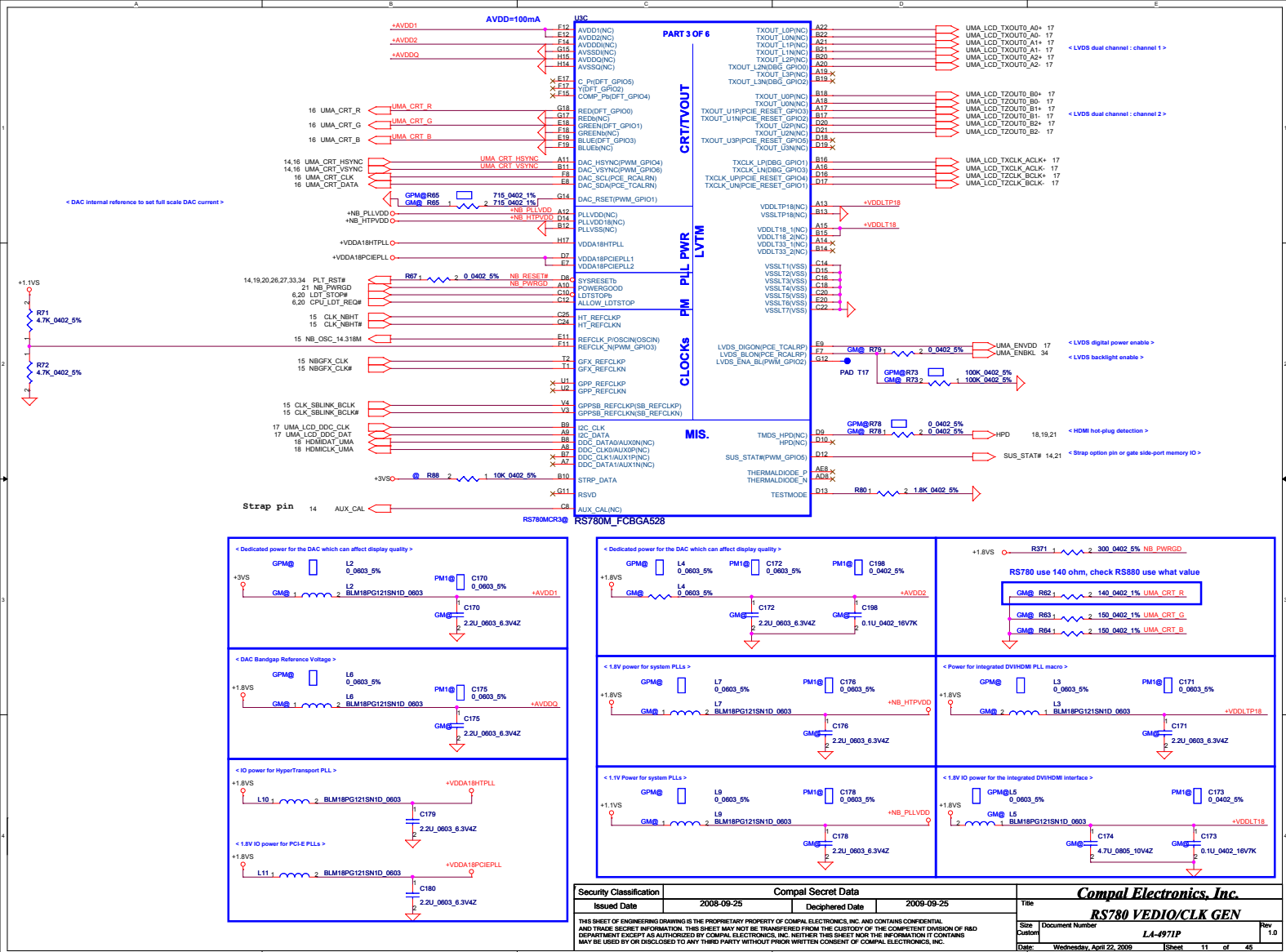


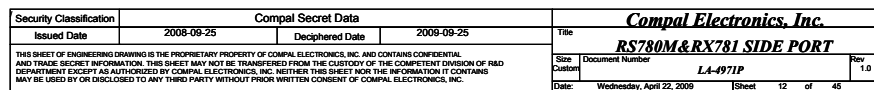
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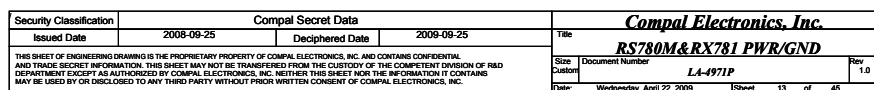


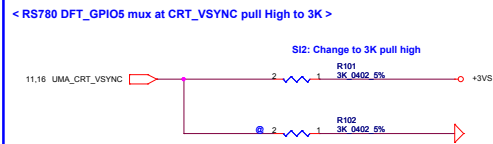
DP0	GFX_TX0, TX1, TX2 and TX3	AUX0 and HPD0
DP1	GFX_TX4, TX5, TX6 and TX7	AUX1 and HPD1

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< DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb >

Enables the Test Debug Bus using GPIO.

1 : Enable (RX780, RS780)
0 : Disable (RX780, RS780)

PIN: RS740-->RS780_AUX_CAL; RX780-->NB_TV_C; RS780--> VSYNC#

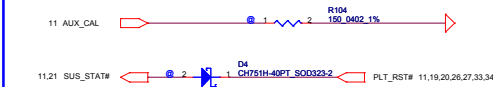
< RS780 use register to control PCI-E configure >

< DFT_GPIO[4:2] : STRAP_PCIE_GPP_CFG[2:0] >

These pin straps are used to configure PCI-E GPP mode.

000 : 00001
001 : 00010
010 : 01011
011 : 00100
100 : 01010
101 : 01100
111 : 01011

< RS780 DFT_GPIO1 >



< DFT_GPIO1 : LOAD_EEPROM_STRAPS >

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS740/RX780: DFT_GPIO1 RS780:SUS_STAT

< RS780 use HSYNC to enable SIDE PORT (internal pull high) >



< DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb >

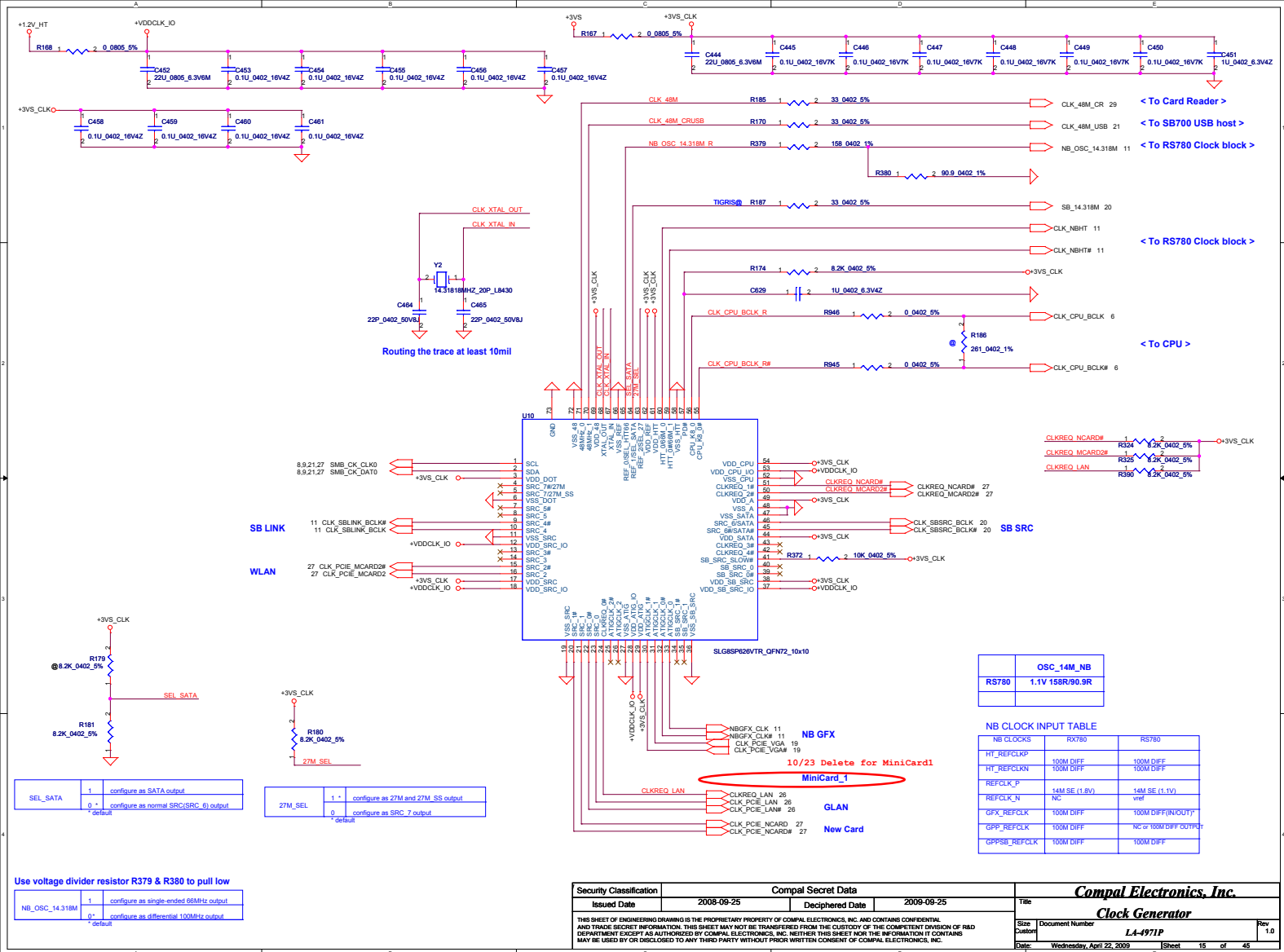
RX780: Enables the Test Debug Bus using PCIE bus

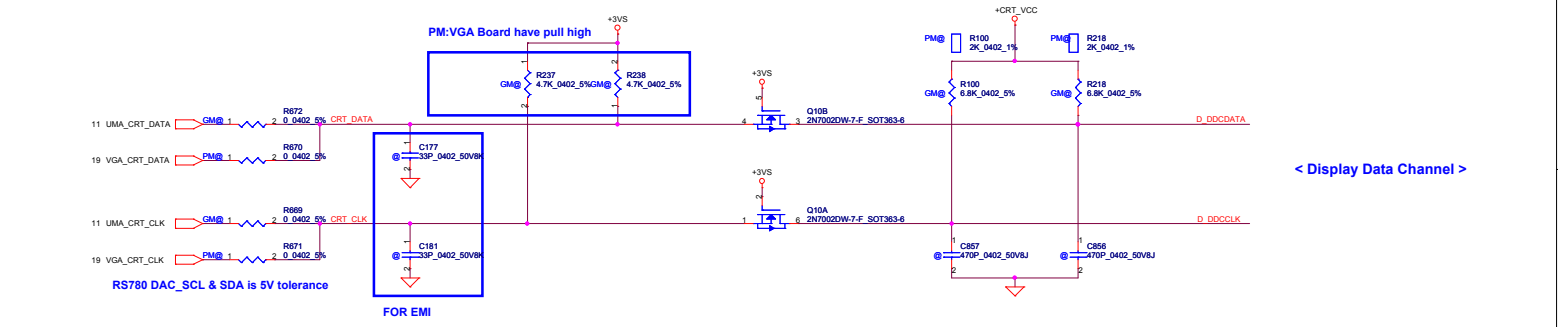
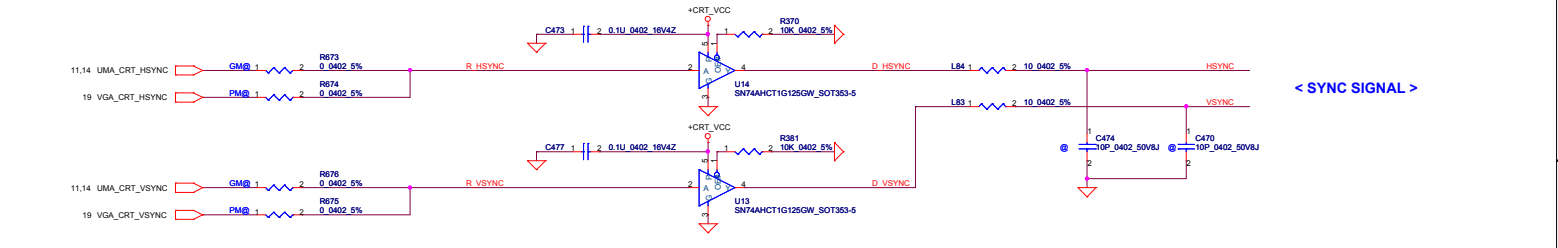
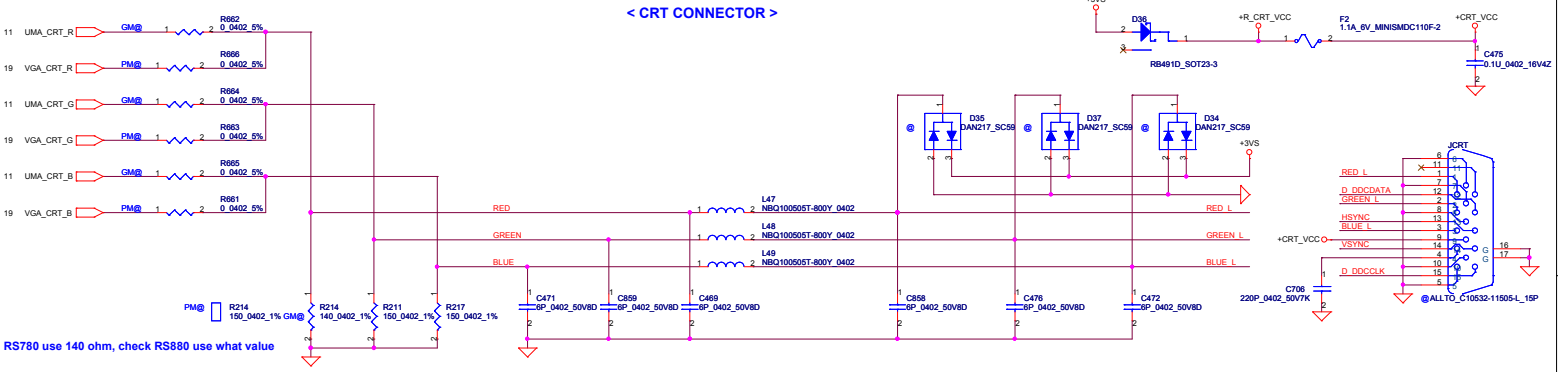
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

RS780: Enables Side port memory (RS780 use HSYNC#)

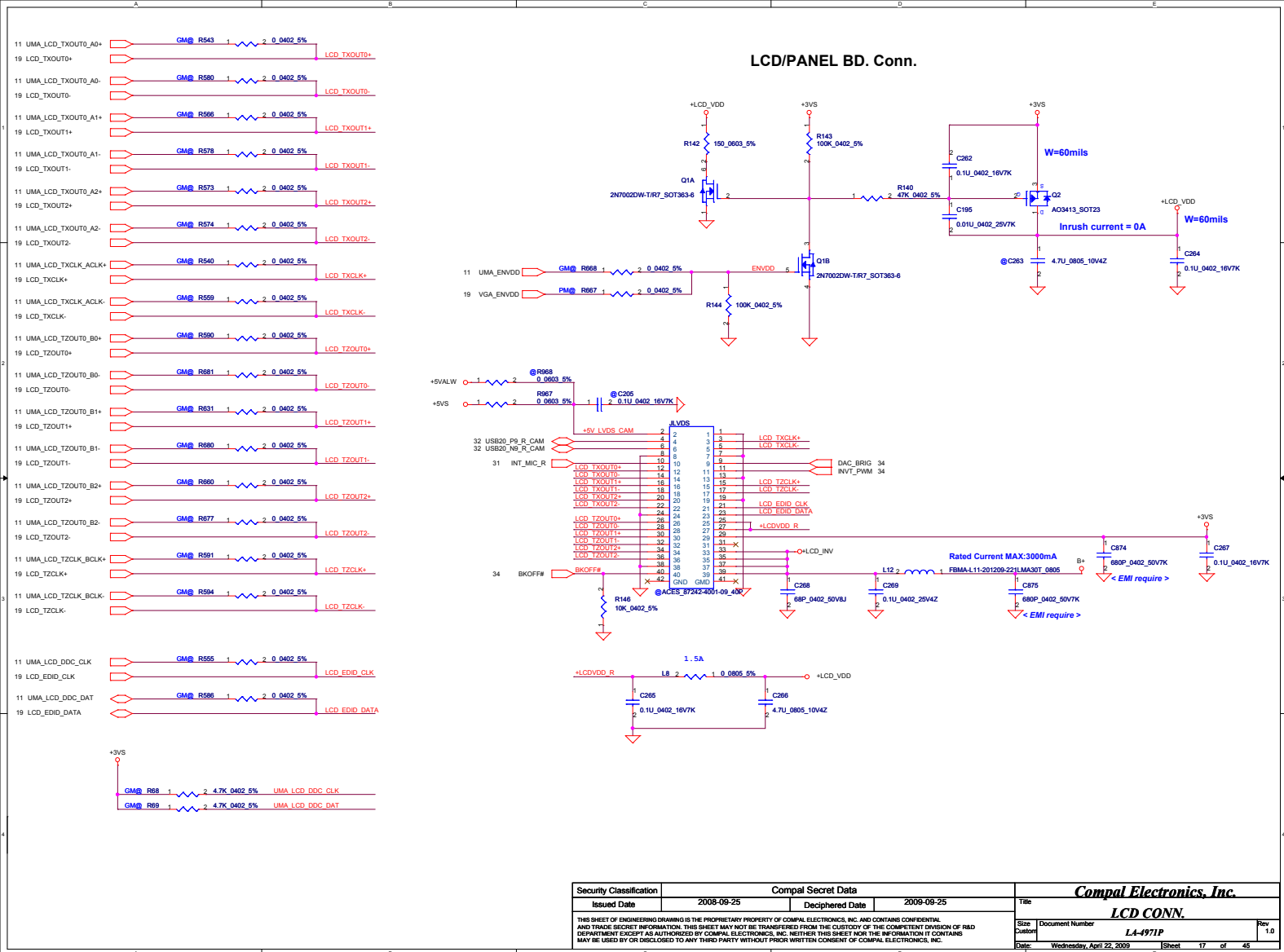
1. Disable (RS780)
0 : Enable (RS780)

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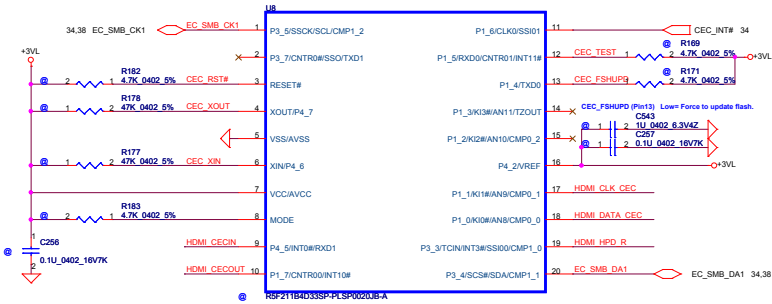




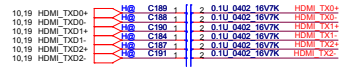
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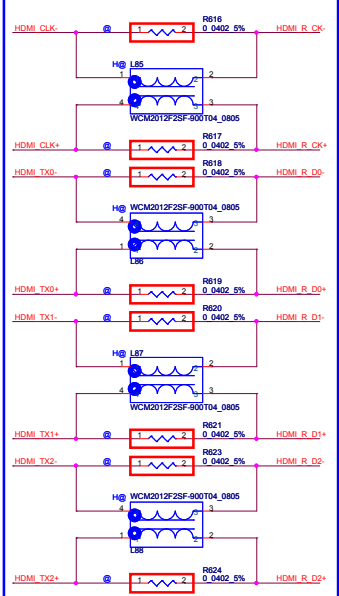
< HDMI CEC Controller >



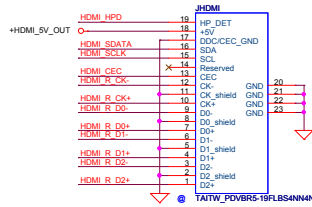
SI-Add R616-R624 for EMI request



< EMI solution >



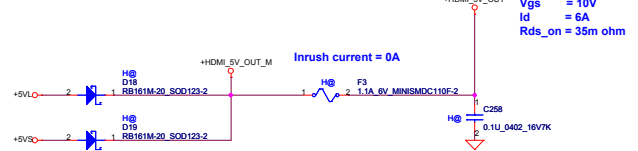
< HDMI Connector >



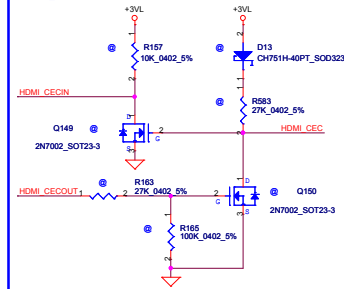
< Termination resistor >



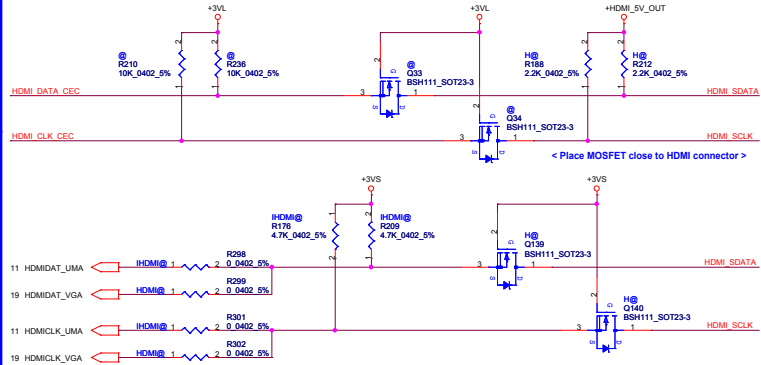
< Power, reset and crystal >



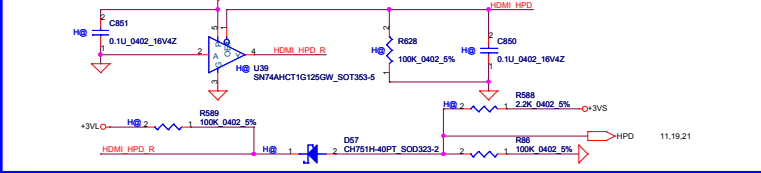
< HDMI_CEC level shift > < Place MOSFET close to HDMI connector >



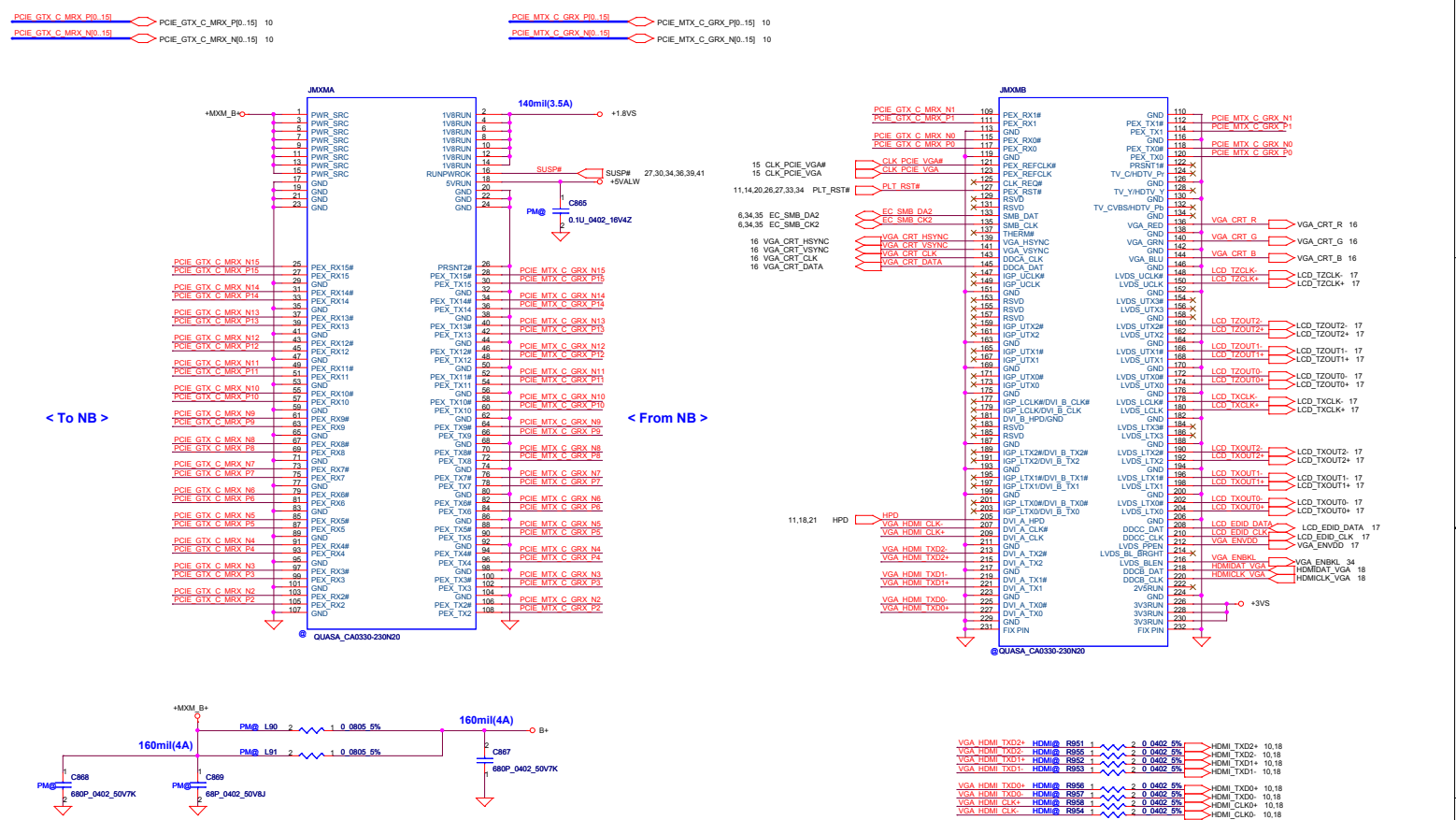
< HDMI DDC channel to device >



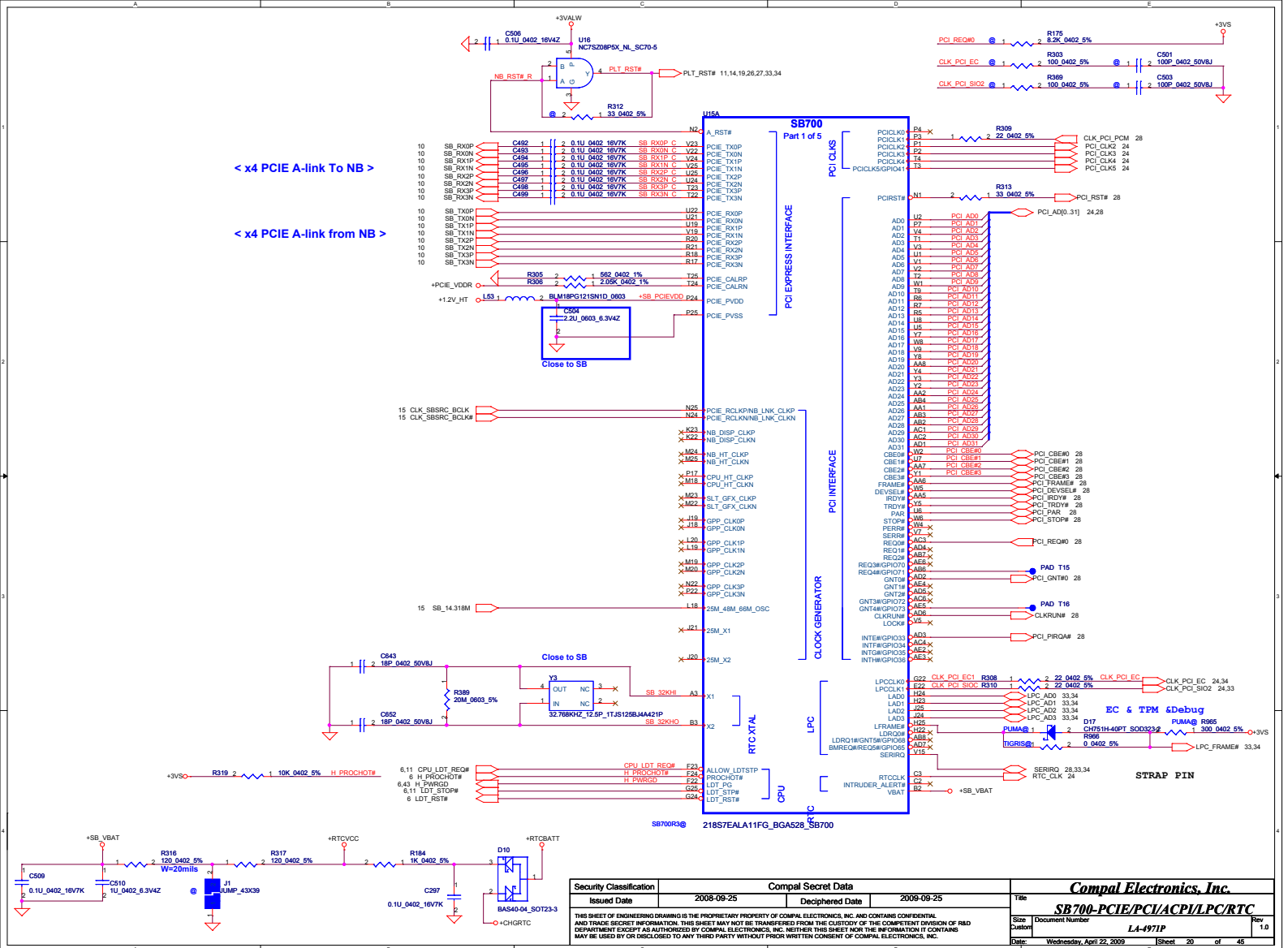
< Hot-plug detection & level shift >



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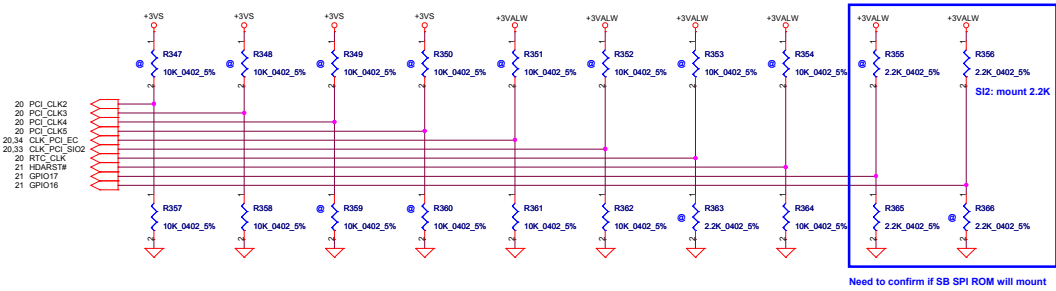
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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

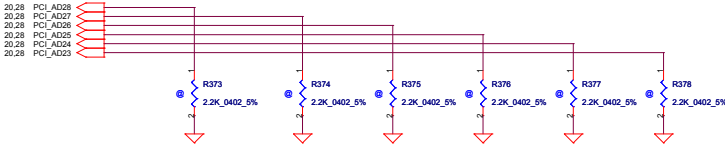
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		



DEBUG STRAPS

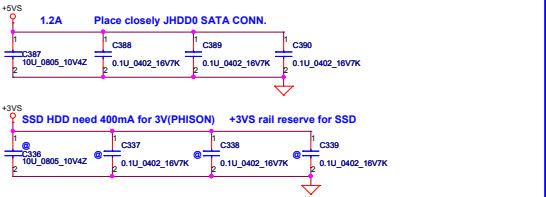
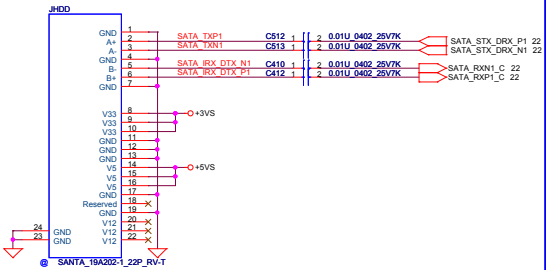
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

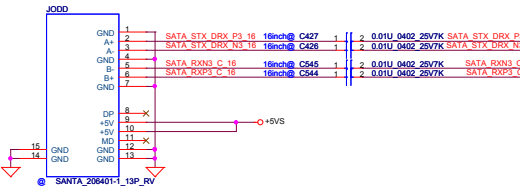


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				Document Number LA-4971P
				Rev 1.0
				Date: Wednesday, April 22, 2009
				Sheet 24 of 45

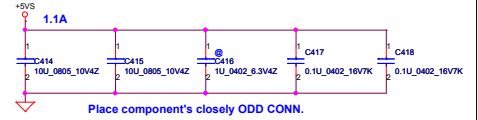
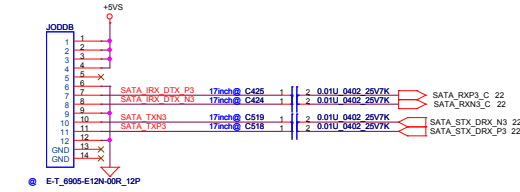
< SATA HDD1 Conn >



< 16" SATA ODD Conn >

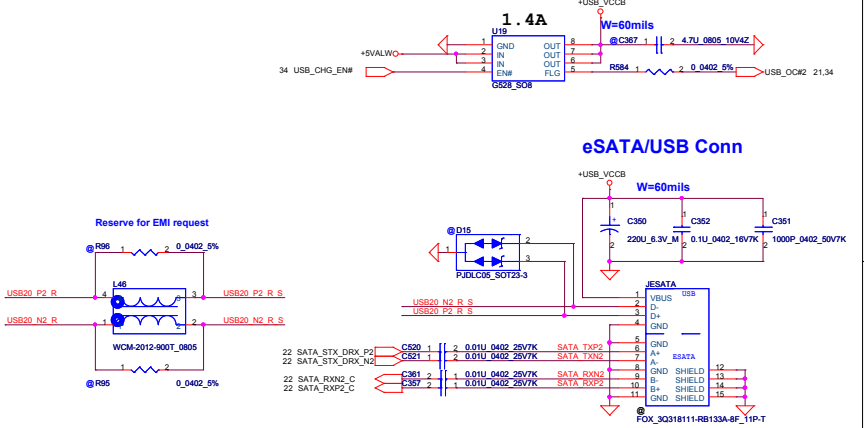
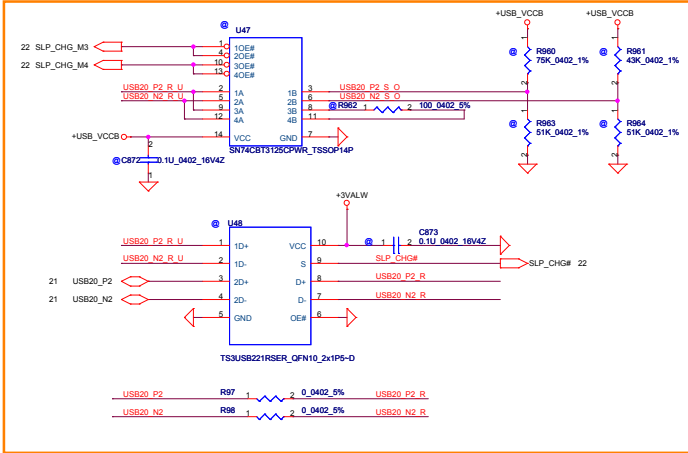


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< eSATA/USB >

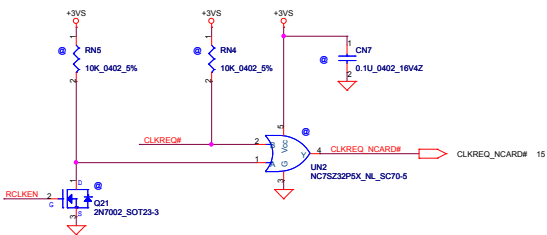
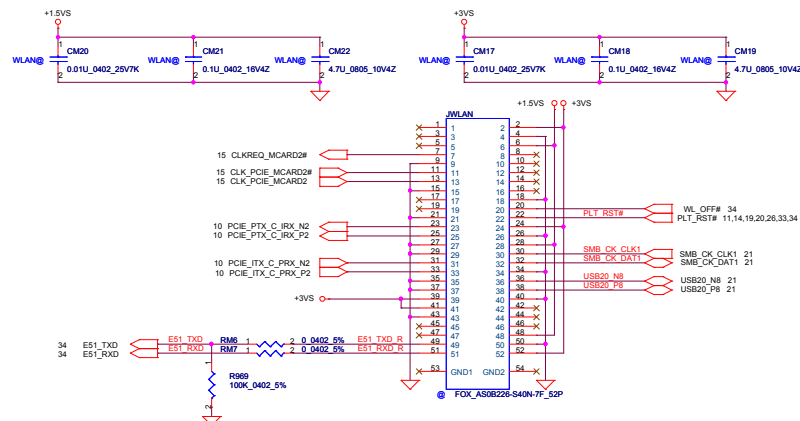
10/22 Add for USB Sleep & Charge M3/M4



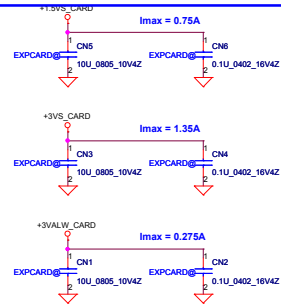
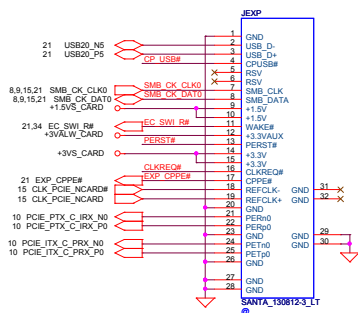
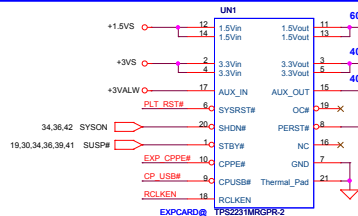
SLP_CHG_M3	SLP_CHG_M4	SLP_CHG#	FUNCTION
Mode 3	HIGH	LOW	D=1D
Mode 4	LOW	HIGH	D=2D

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Date: Wednesday, April 22, 2009		Sheet 26 of 45

< PCIe Mini Card for WLAN >

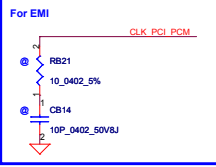
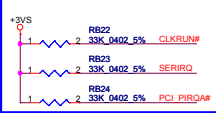


< Reserve for test >



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				Date	Wednesday, April 22, 2009
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22K TO 47K PULL-UPS MUST BE PLACED ON INTA#, PME#, SERIRQ# & CLKRUN#.



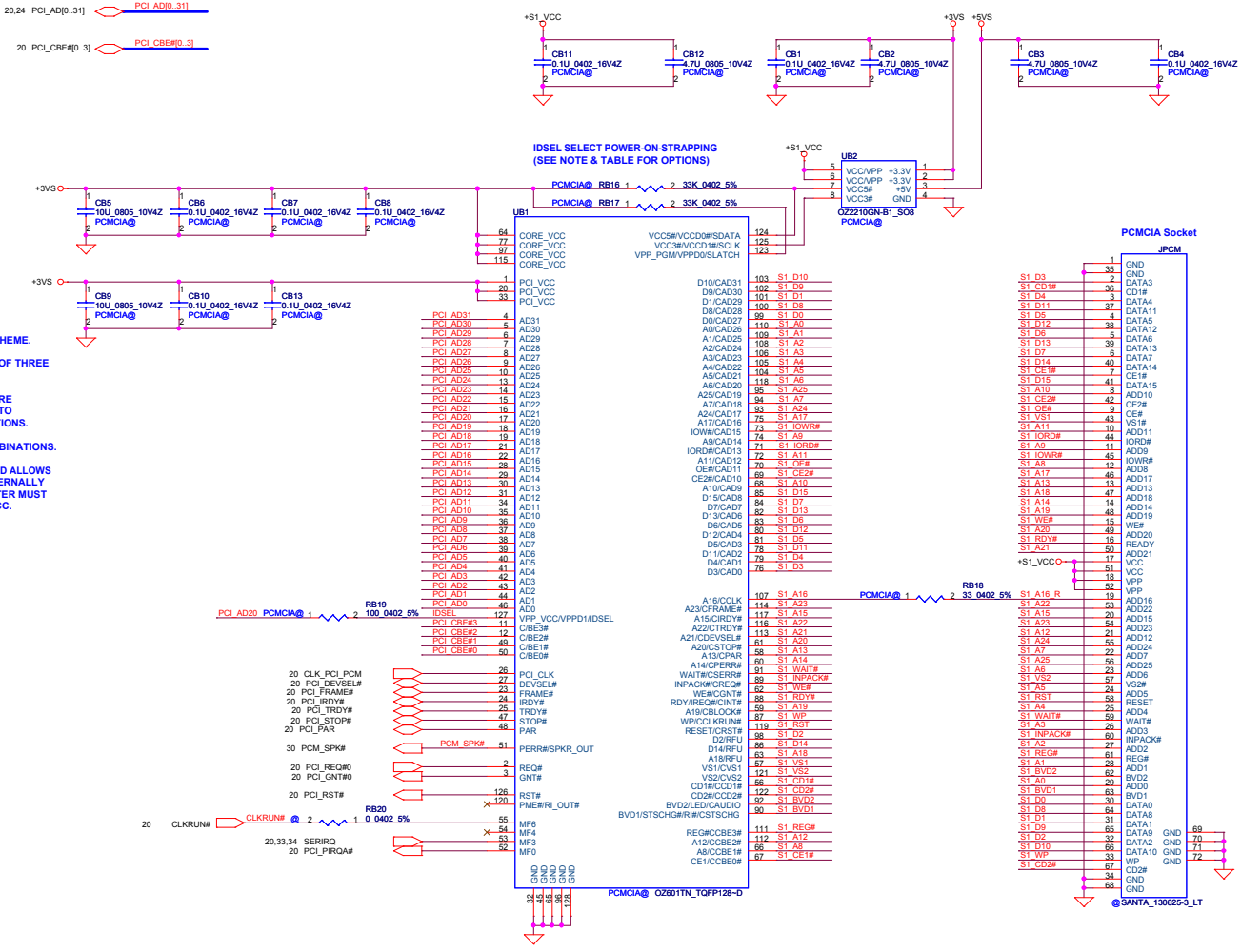
NOTE: IDSEL SELECTION!
THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME.

IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE PCI AD LINES OR EXTERNAL IDSEL SIGNAL.
22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS.

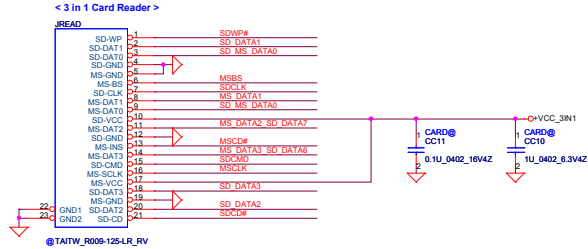
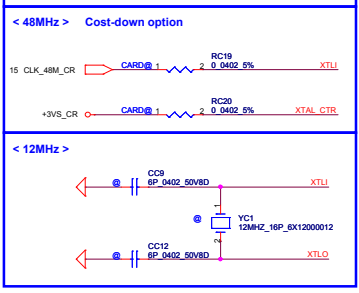
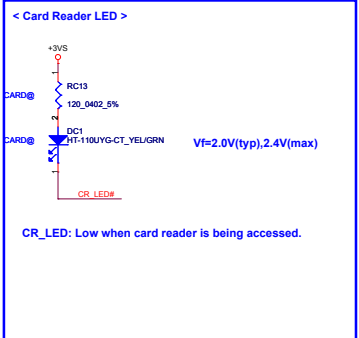
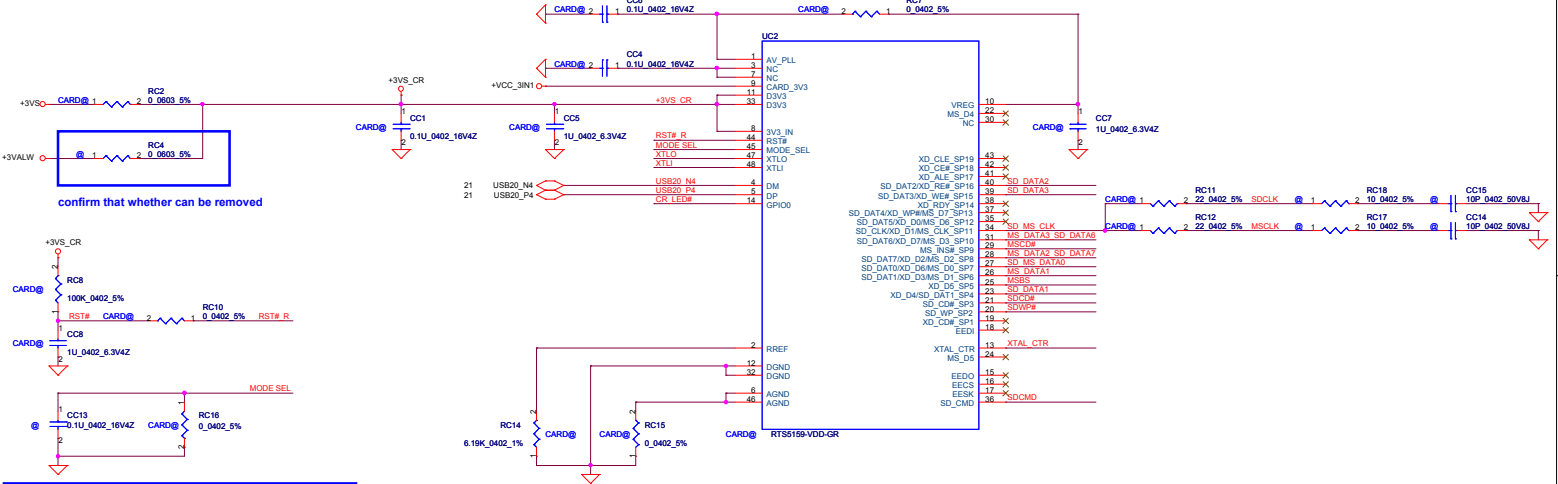
THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.
CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

VCC5# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN 127 ball F4

must check IDSEL, PCI_PIRQ#,

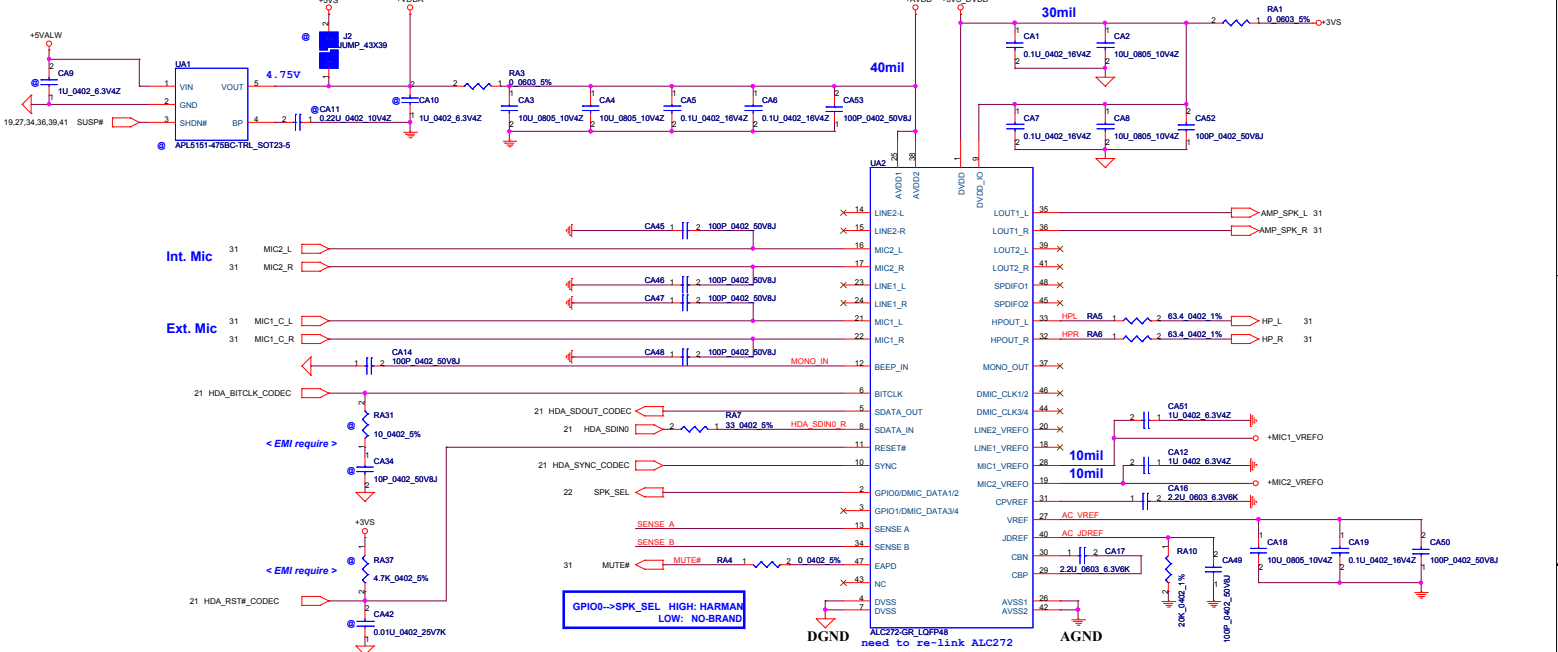


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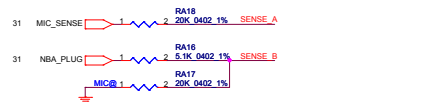


R	C	USB AUTO DE-LINK	MS FORMATTER	Description
0	NC	YES		Recommended
NC	47P	YES	YES	
NC	NC			Compatible with RTSS5158E
NC	680P	YES		LED ON
10K	180P			LED ON
10K	680P		YES	

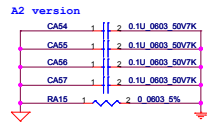
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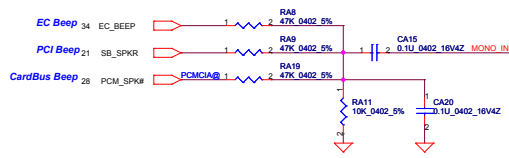
< SENSE_A & SENSE_B, place close to chip >



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	Ext. MIC
	20K	PORT-B (PIN 21, 22)	
	10K	PORT-C (PIN 23, 24)	
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	Int. MIC
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out



< MONO_IN SOURCE >



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Issued Date	2008-09-25	Deciphered Date	2009-09-25	HD Audio ALC272 Codec	
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				Date: Wednesday, April 22, 2009	Sheet 30 of 45

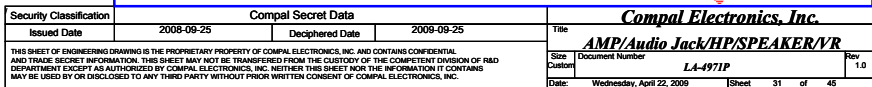
Compal Electronics, Inc.

HD Audio ALC272 Codec

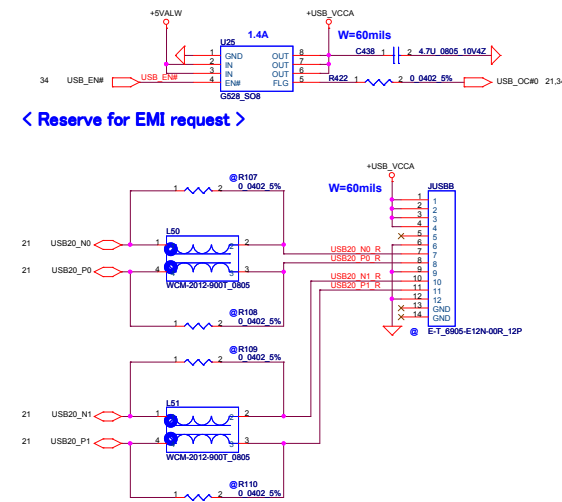
LA-4971P

Rev 1.0

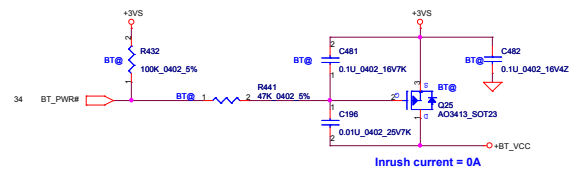
GAIN0	GAIN1	Av (db)	Rin (ohm)
0	0	6	90K
0	1	10	70K
1	0	15.6	45K
1	1	21.6	25K



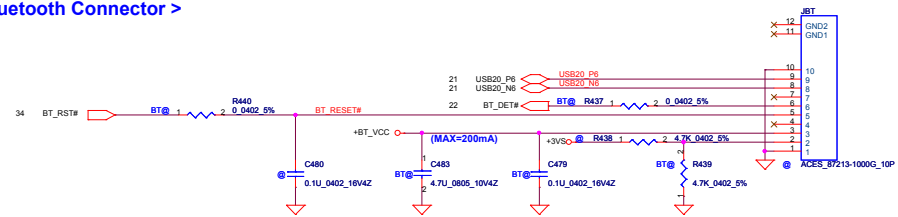
< USB Right-side Board, USB port 0,1 >



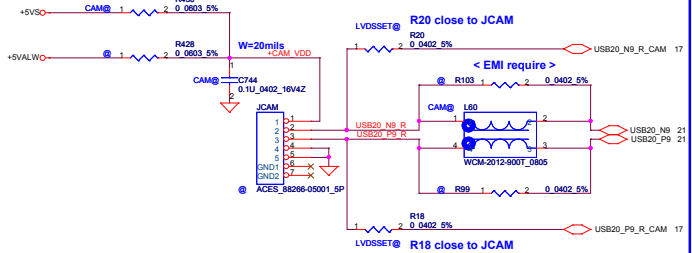
< BlueTooth Interface, USB port6 >



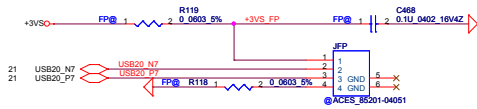
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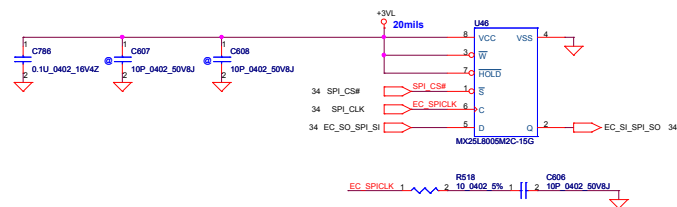
< Int. Camera, USB port 9 >



< Finger Printer, USB port 7 >

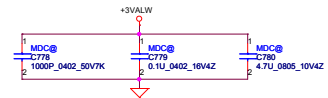
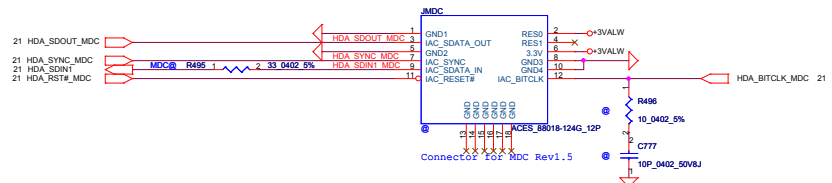
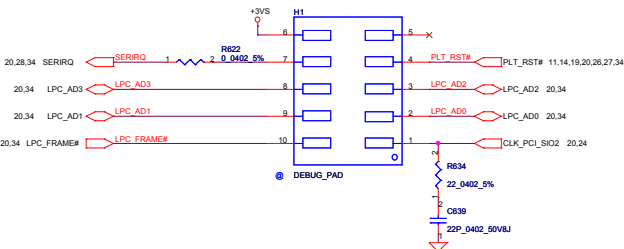


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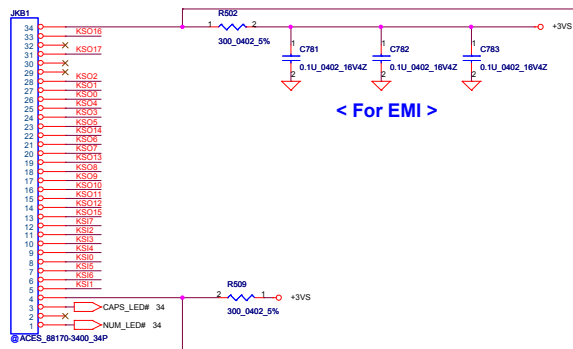


< LPC Debug Port >

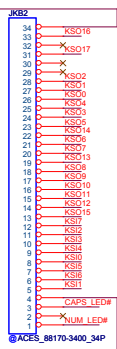
Please place the PAD under DDR DIMM.



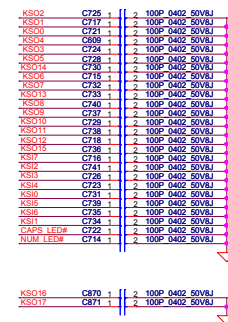
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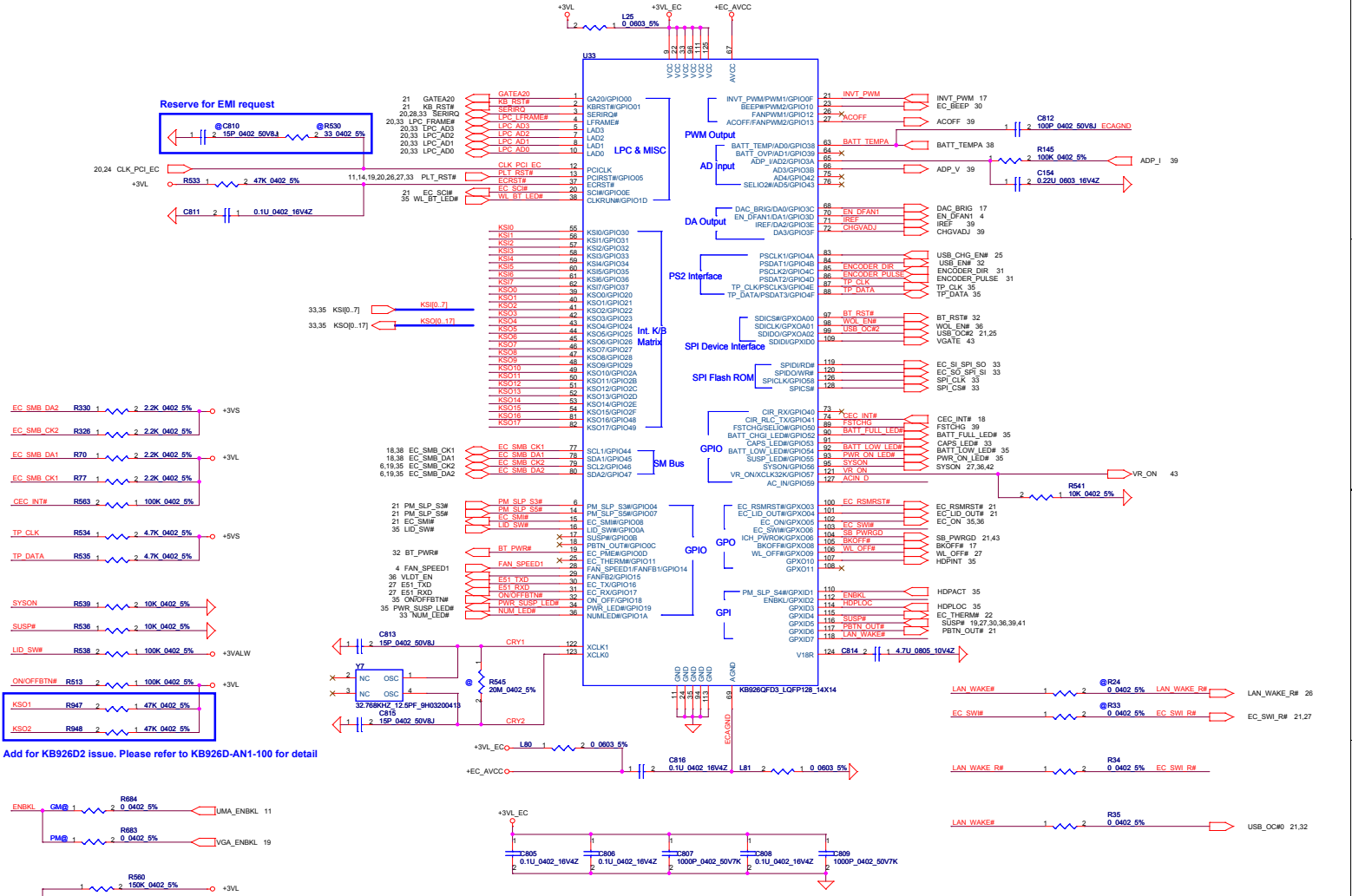
< KEYBOARD CONN 17" >



< For EMI >

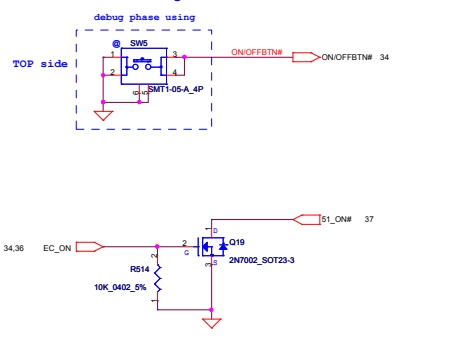


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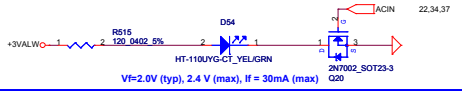


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				Custom	LA-4971P
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< Power Button for Debug >

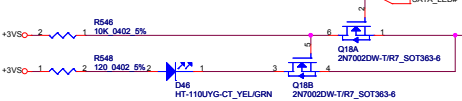


< DC-IN LED >



Remove WIMAX LED control circuit

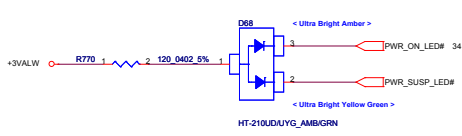
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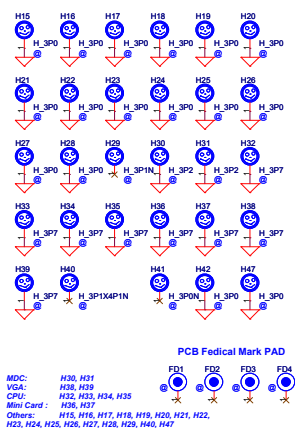
< WL&BT LED >



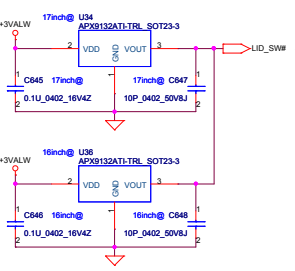
< POWER-ON & SUSPEND LED >



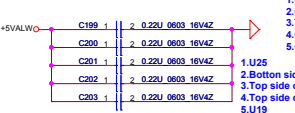
< Screw Hole >



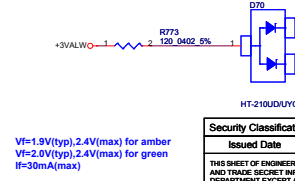
< LID Switch >



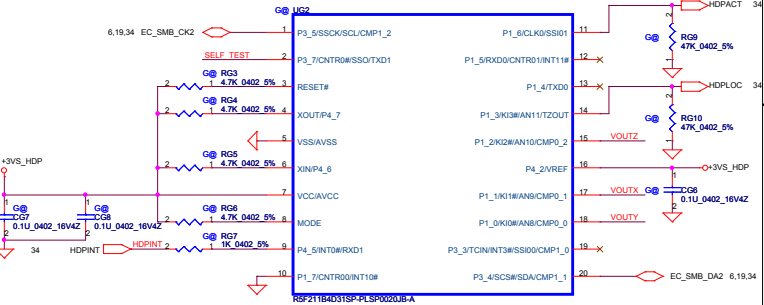
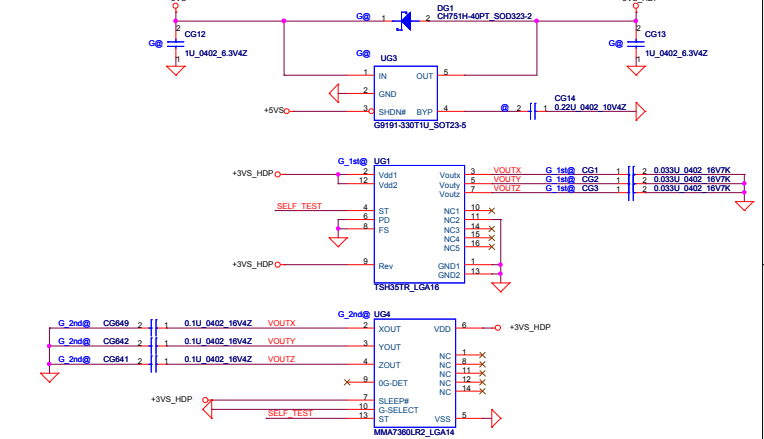
< EMI reserve >



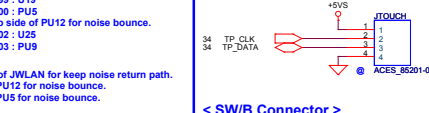
< BATT CHARGE/FULL LED >



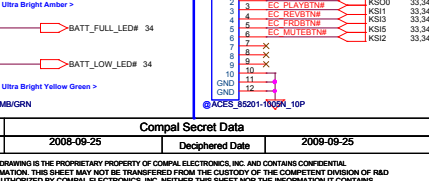
< G - Sensor >



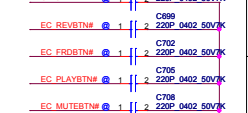
< Touch/B Connector >



< SW/B Connector >



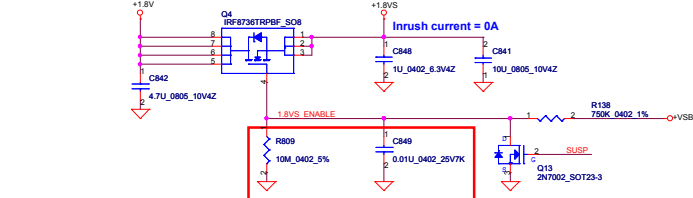
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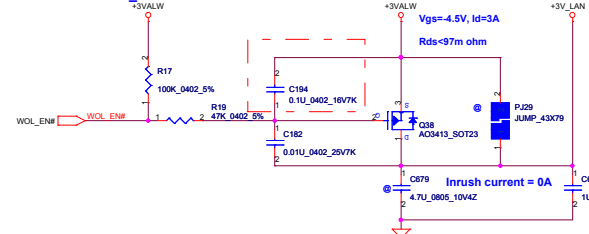
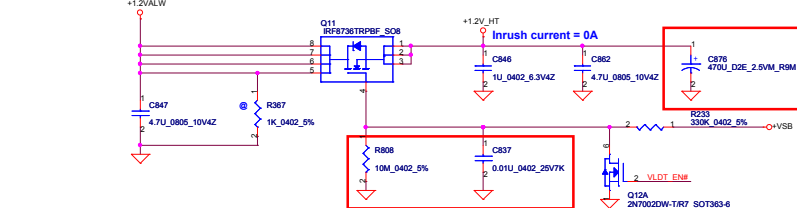
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Compal Electronics, Inc.
LED/LID/PB/FB/SCREW HOLE
LA-497IP

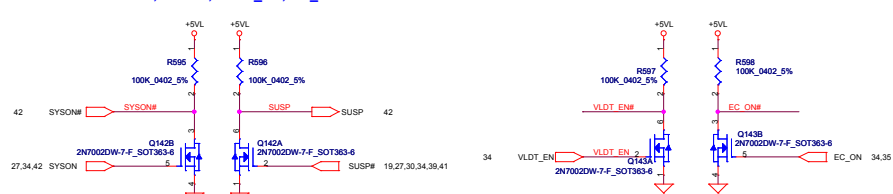
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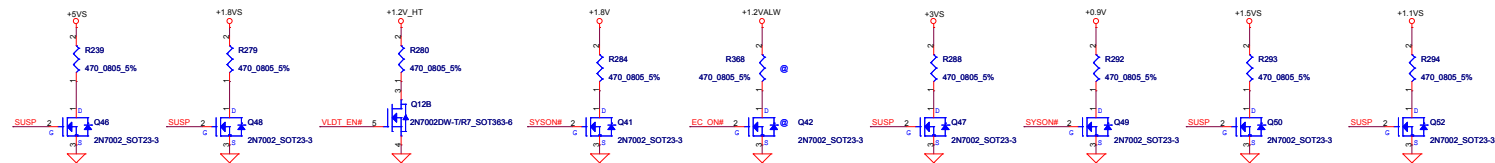
< close to PQ20, must EMI confirm >



< Inversion of SYSON, SUSP#, VLDT_EN, EC_ON >

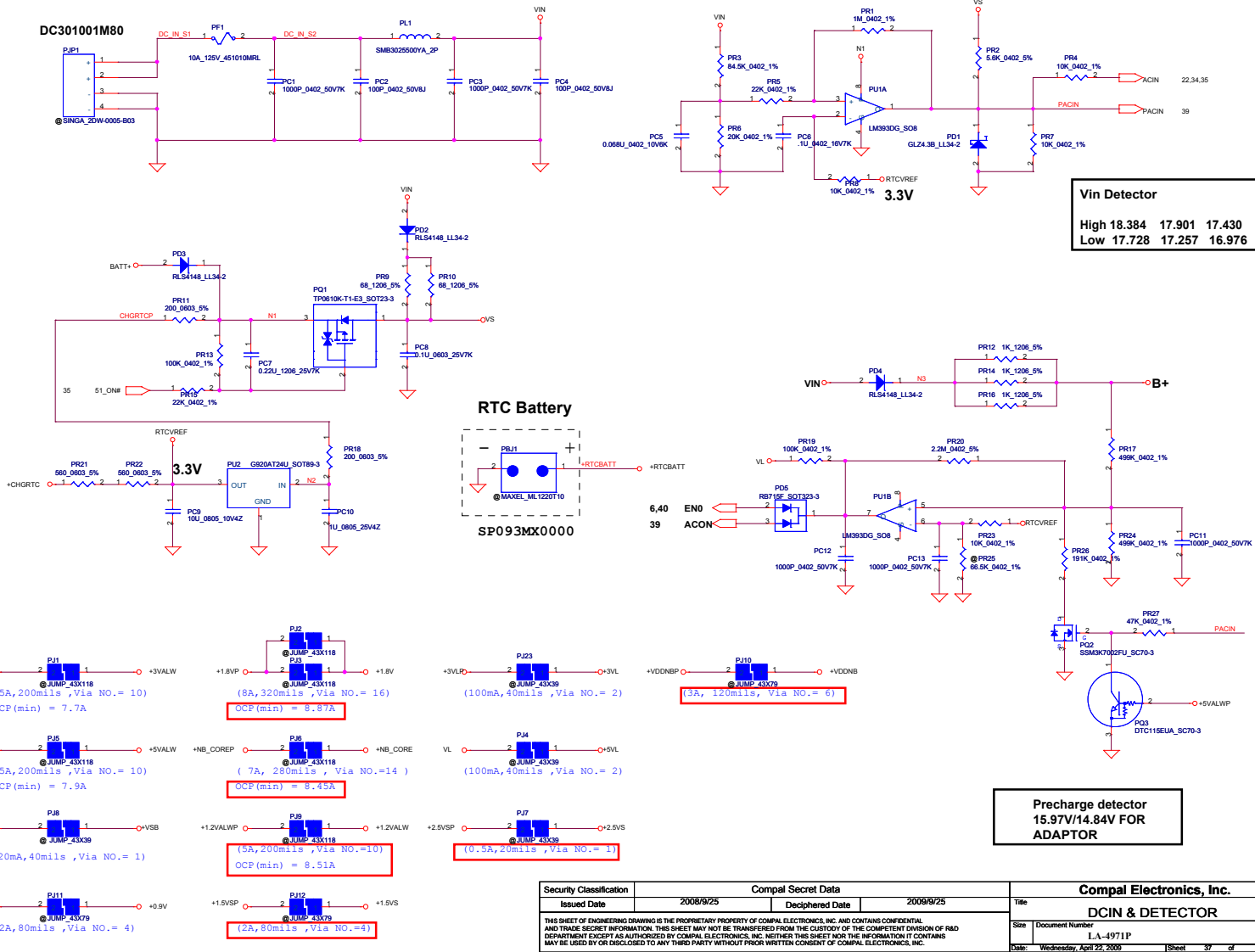


< Discharge circuit >

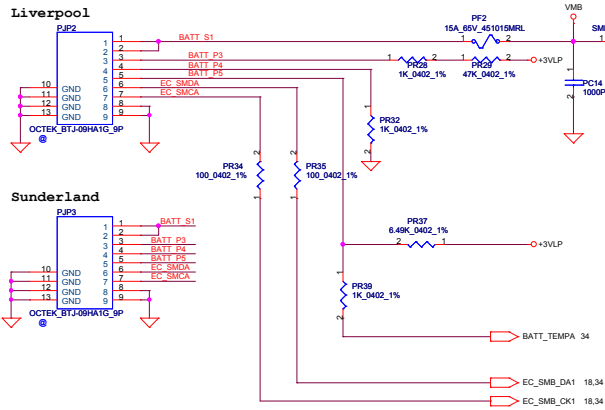


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Date	Document Number			14-4971P	1.0
Printed: Wednesday, April 22, 2009				Sheet	58 of 65

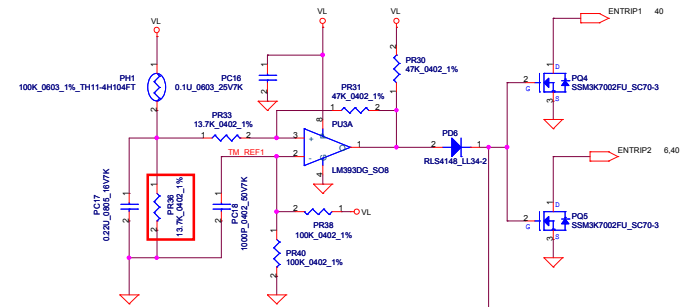
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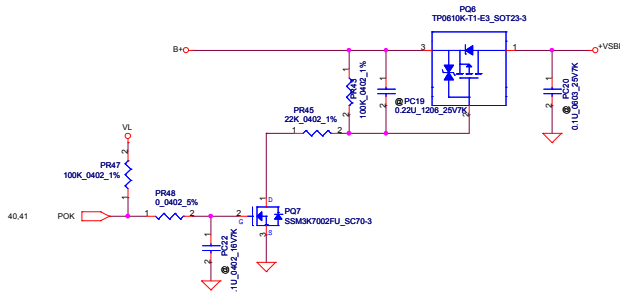
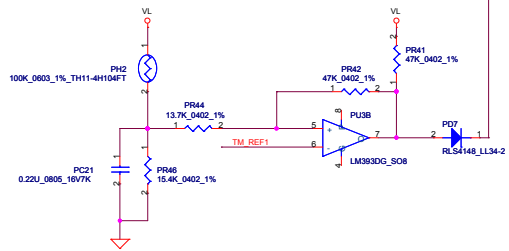
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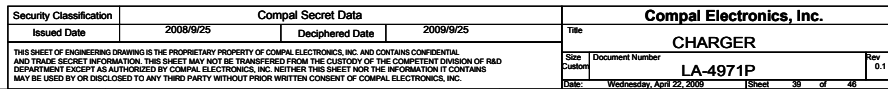
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 92 degree C
Recovery at 56 degree C



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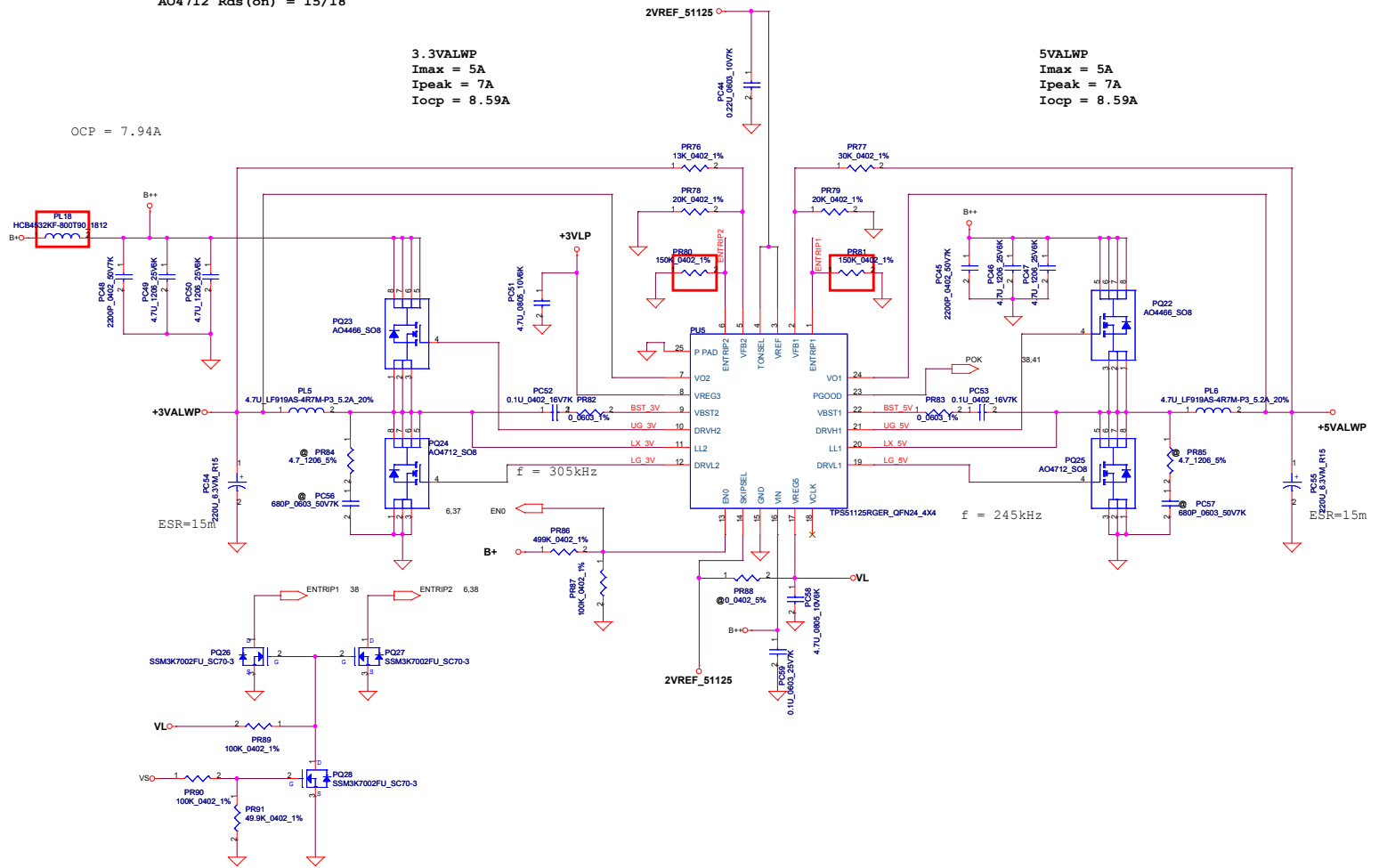


AO4712 Rds(on) = 15/18

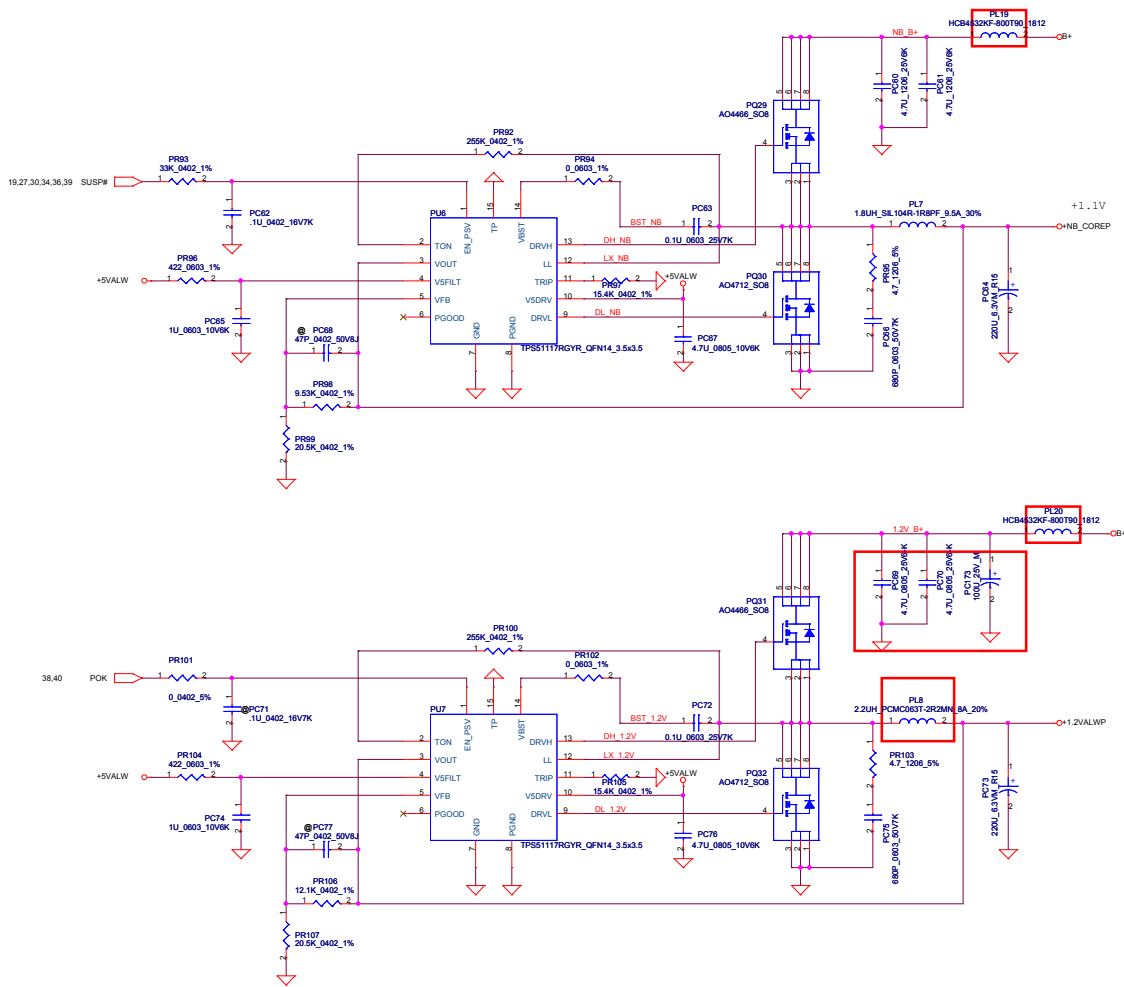
3.3VALWP
Imax = 5A
Ipeak = 7A
Iocp = 8.59A

5VALWP
Imax = 5A
Ipeak = 7A
Iocp = 8.59A

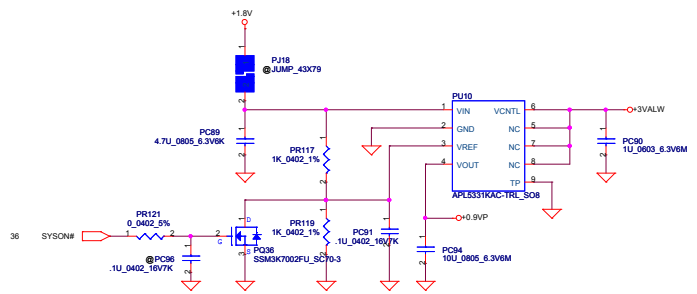
OCP = 7.94A



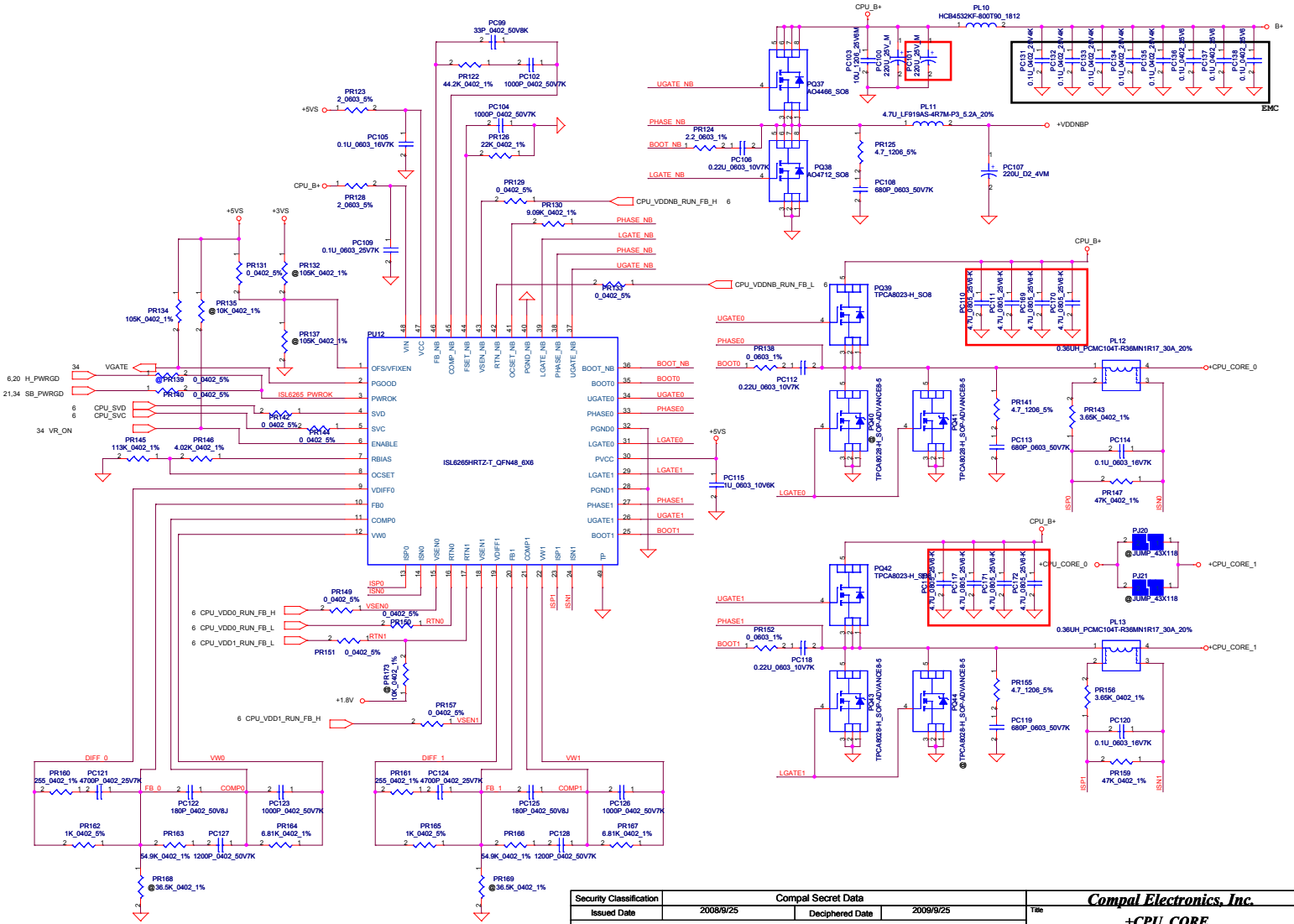
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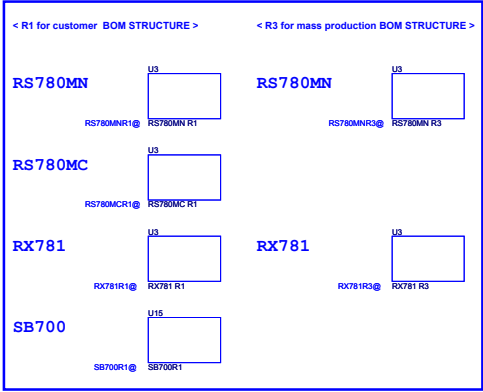
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Version Change List (P. I. R. List) for Circuit

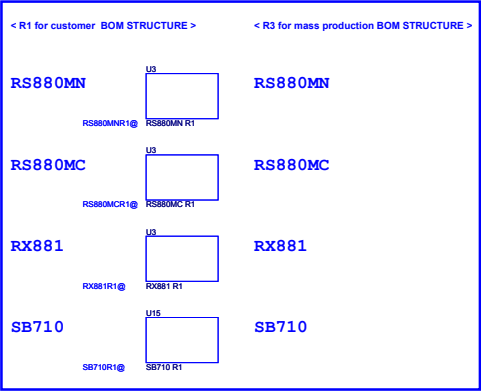
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1.	2009/02/23	--> change R70, R77 from 4.7K to 2.2K					
2.	2009/02/23	--> change R178 from 4.7K to 47K					
3.	2009/02/26	--> change SPI ROM from SST to MXIC					
4.	2009/02/26	--> change D36 from ROHM to PANJI					
5.	2009/02/27	--> change the footprint of T9, T10, T11, T12, T19, T20 from TPC12 to TPC24					
6.	2009/02/27	--> change 5V power of LCD connector					
7.	2009/03/02	--> unmount R556					
8.	2009/03/04	--> change RA16 from 5% to 1%					
9.	2009/03/10	--> change R146 from 100k ohm to 10k ohm					
10.	2009/03/10	--> change Y2 from SJ114P3M730 to SJ114P3MG00					
11.	2009/03/11	--> change C686, C699, C702, C705, C706, C708, CA27 from SE074221K00SE to SE074221K80 for Green part					
12.	2009/03/11	--> change LAN_WAKE# & EC_SWI#					
13.	2009/03/11	--> unmount USB sleep & charge, add R97 & R98					
14.	2009/03/11	--> unmount HDMI CEC controller and related components.					
15.	2009/03/11	--> connect USB_OC#0 to LAN_WAKE# through 0 ohm					
16.	2009/03/12	--> change H42 from NPH to PH					
17.	2009/03/12	--> add PR203 10Ohm					
18.	2009/03/24	--> change F2 footprint to F_MINISMDC110F-2					
19.	2009/03/24	--> Add R370 & R381					
20.	2009/03/24	--> change R557's BOM structure from H@ to @					
21.	2009/03/24	--> change R440 from 0 ohm to 100k ohm					
22.	2009/03/31	--> Replace PJ13, PJ30, PJ14, PJ15, PJ16 by PL17, PL18, PL19, PL20, PL21					
23.	2009/04/02	--> Add R969 on E51_TXD					
24.	2009/04/02	--> Modify +HDMI_5V_OUT Circuit Remove Q159, R160, Q26, R557, C876 and add D19					
25.	2009/04/02	--> Change R440 from 100k to 0 for Askey BT Reset					
26.	2009/04/02	--> Change C480's BOM Stuuucture from BT@ to @					
27.	2009/04/06	--> Change SW5's BOM Stuuucture to @ for MP					
28.	2009/04/06	--> Add C876 for Power noise issue					
29.	2009/04/06	--> Add D20 for Power issue					
30.	2009/04/17	--> Change D12's BOM Stuuucture to @					
31.	2009/04/22	--> Change C876 & C234 from 330u to 470u (SGA00001U00) for Power noise issue					
							</

HW4 Product Improvement Record (P.I.R.)

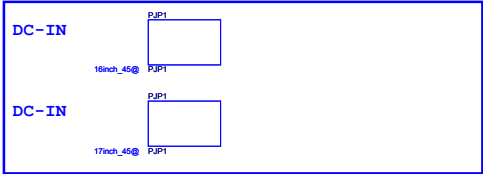
< Liverpool & Sunderland >



< Tigris >



< DC Jack >



Use MEMO : change UG1 R5F211B4D31SP (SA000037Y60) to R5F211B4D34SP (SA00003A600)

< PCB >



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