KTKAA

Los Angeles 10/10G

LA-4571P REV 2.0 Schematic

Intel Penryn/ Cantiga/ ICH9M

2008-09-19 Rev. 2.0

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/09/19	Deciphered Date	2009/09/19
Title	SCHEMATIC MB A4571		
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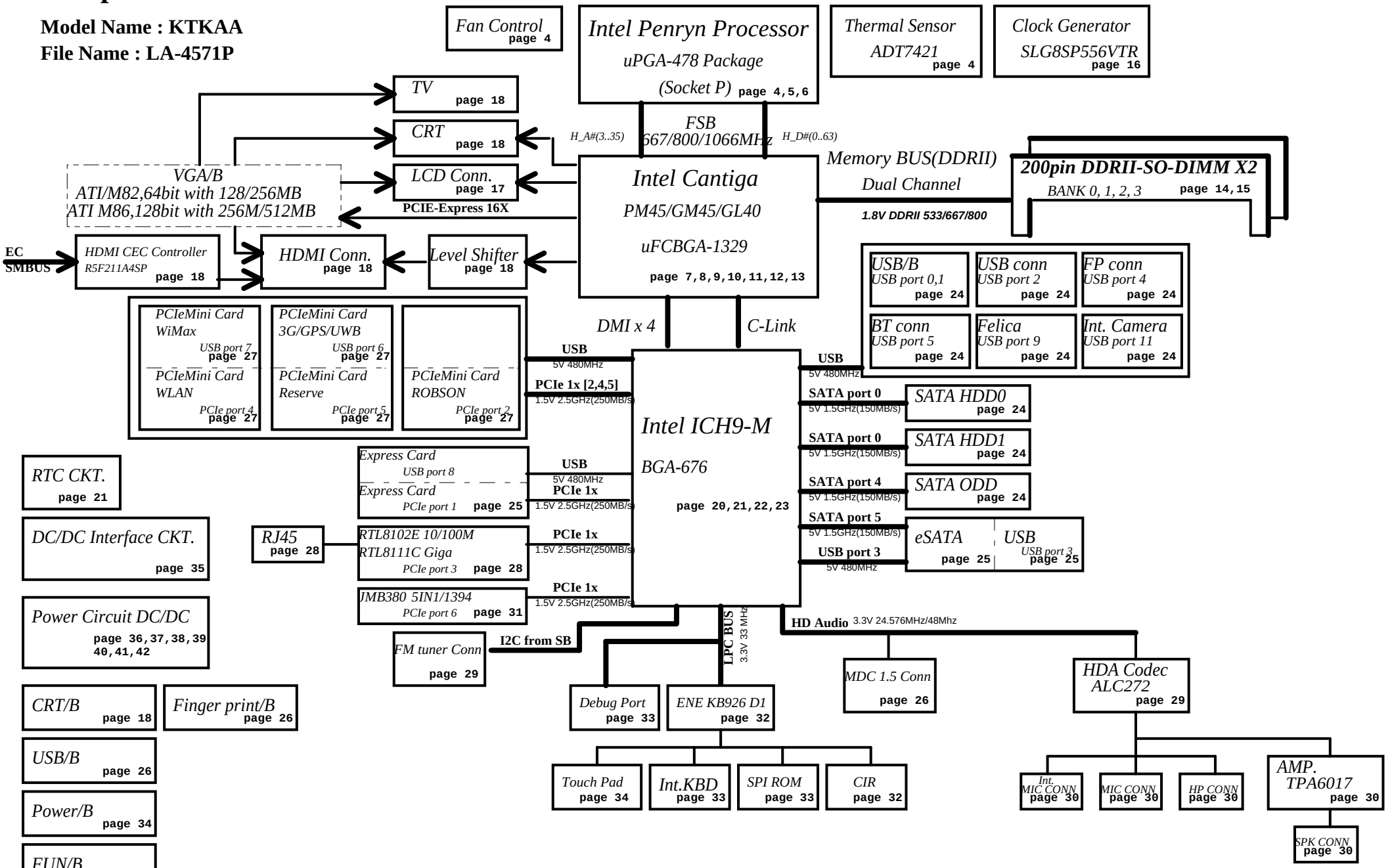
Compal Confidential

Model Name : KTKAA
File Name : LA-4571P



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Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3VL	3.3V always on power rail	ON	ON	ON	ON
+3V_SB	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5VL	5V always on power rail	ON	ON	ON	ON
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON
+CPU_CORE	Core voltage for VGA chip	ON	ON	OFF	OFF
+VGA_PCIE_1.1VS	1.1V switched power rail for VGA PCIE	ON	ON	OFF	OFF
+1.8VS	1.8V power rail for VRAM	ON	ON	OFF	OFF

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#		
Full ON	HIGH	HIGH	HIGH	HIGH		
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH		
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH		
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH		
S5 (Soft OFF)	LOW	LOW	LOW	LOW		
G3	LOW	LOW	LOW	LOW		

BTO Option Table

Function	2nd HDD	LAN		Mini card			RJ11/FM tuner		3G SIM slot
description	(2H)	(E)	(C)	(D2)		(D3)	(R)	(M)	(G)
explain		10/100M	Giga	Two Crads		three Crads	RJ11	FM	
BTO	2HDD@	8102E@	8111C@	WLAN@	GPS@	NAND@	MDC@	FM@	3G@

Function	HDMI			TV-out	CIR	CAMERA & MIC		Finger printer
description	(Y)			(S)	(I)	(X)		(F)
explain	Intel(UMA)	ATI VGA/B	COMMON			CAMERA	MIC	
BTO	IHDMI@	NIHDMI@	HDMI@	H@	TVOUT@	CIR@	CAM@	MIC@	FP@

Function	Felica	BLUE TOOTH	
description	(J)	(B)	
explain			
BTO	FLICA@	BT@	

External PCI Devices

EC SM Bus1 address

Power	Device	Address
+5VL	EC KB926 C0	
+5VL	Smart Battery	0001 011X b
+5VL	HDMI-CEC	0011 010x b
+5VL	FUN/B (CAP Sensor)	

EC SM Bus2 address

Power	Device	Address
+3VS	EC KB926 C0	
+3VS	CPU THM Sen SMSC SMC1402	0100 110x b
+3VS	VGA THM Sen ADM1032ARMZ	1001 110Xb
	VGA on die thermal sensor	1001 111Xb

need to confirm

ICH9M SM Bus address

Power	Device	Address
+3V_SB	ICH9M	
+3VS	Clock Generator (SLG8SP556V)	1101 001Xb
+3VS	DDR DIMM0	1001 000Xb
+3VS	DDR DIMM1	1001 010Xb
+3VS	Express	
+3VS	FM Module	

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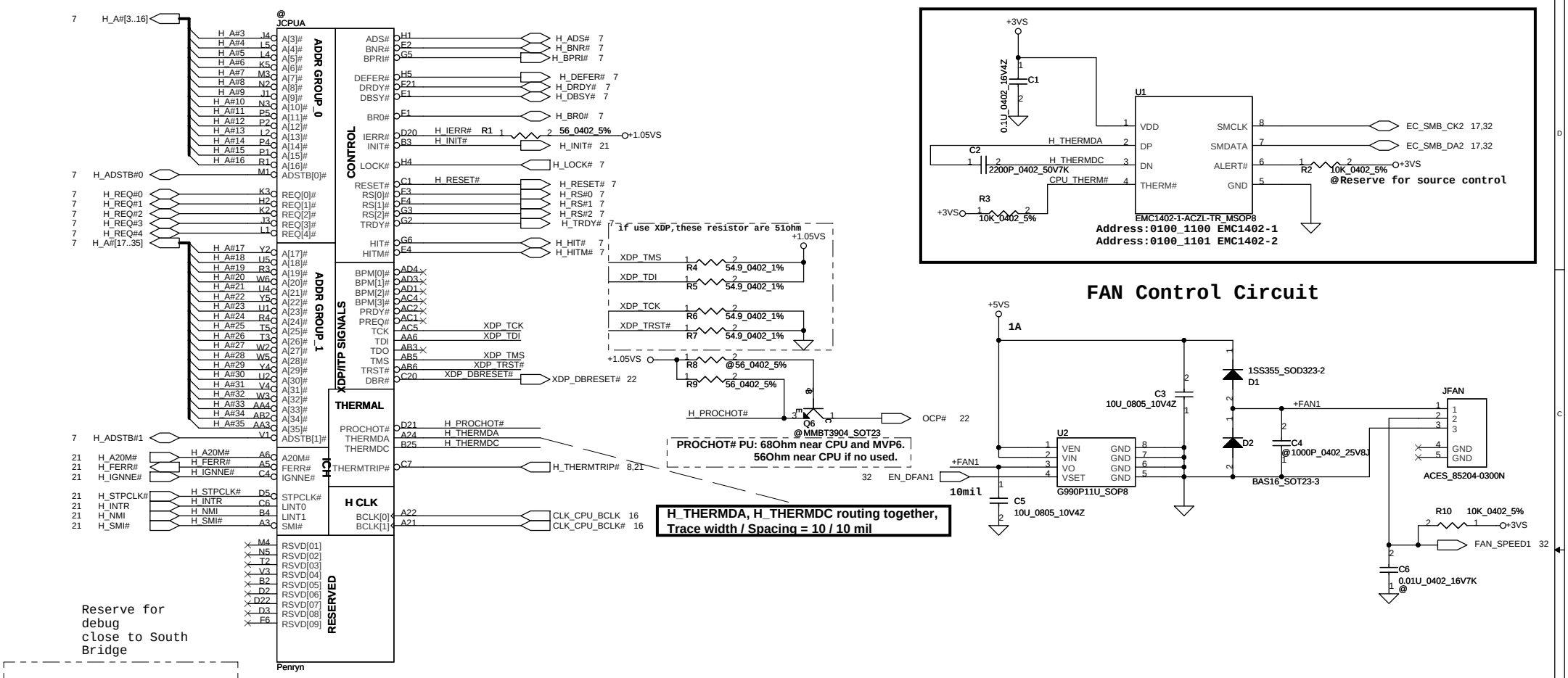

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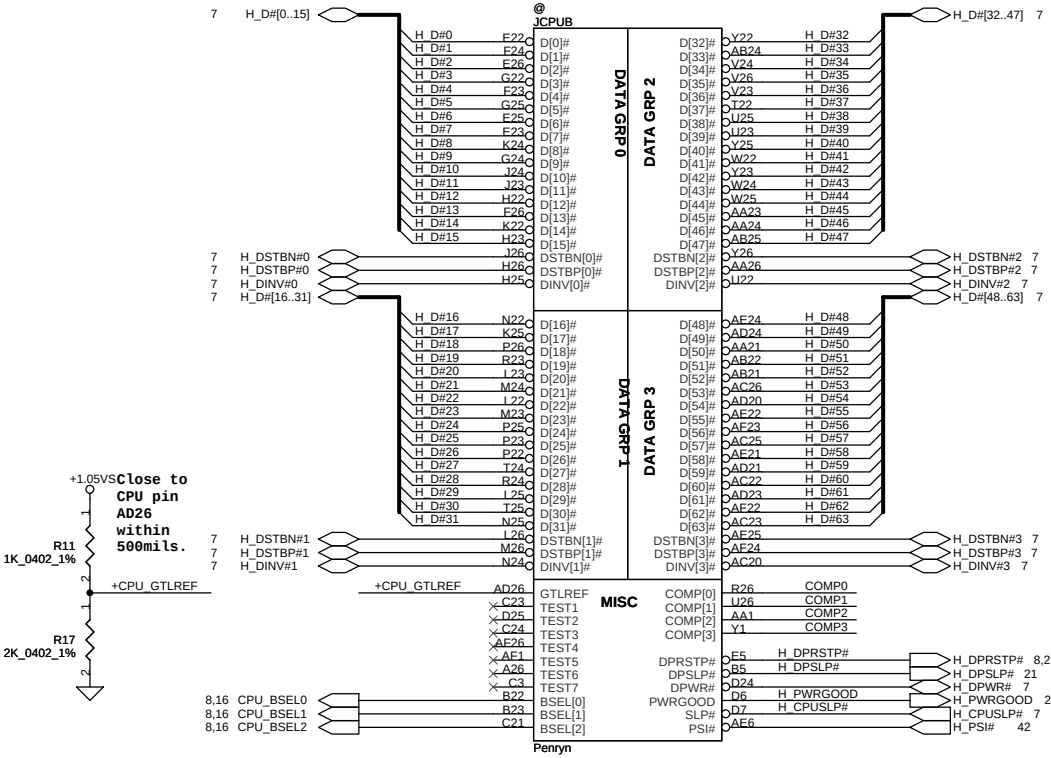
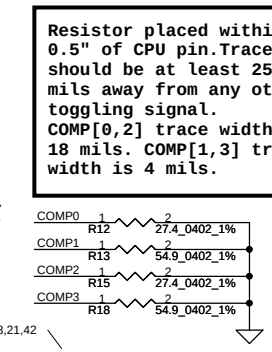


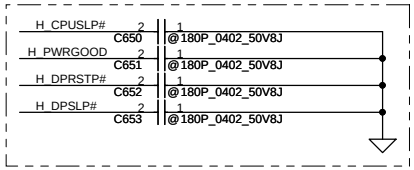


Resistor placed within 0.5" of CPU pin.Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

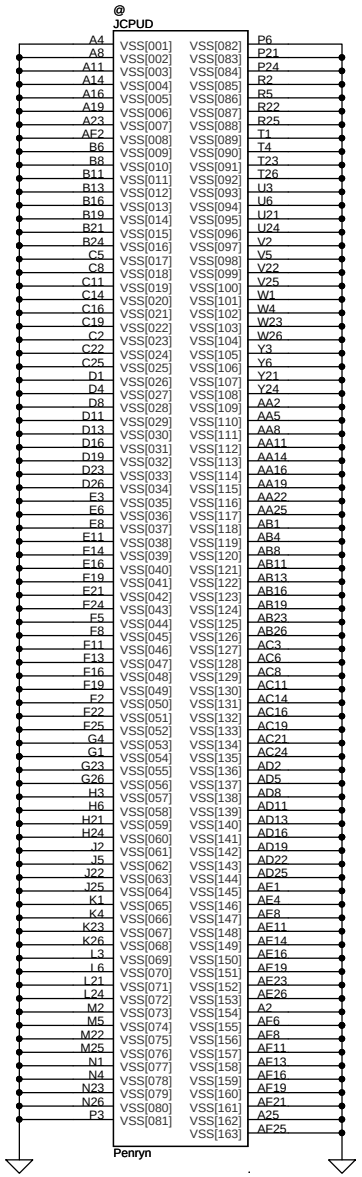
layout note: Please use "Daisy Chain" to layout and the signal (H_DPRSTP#) is routed from ICH9 to power IC, then to NB and CPU

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0



Reserve for debug close to CPU



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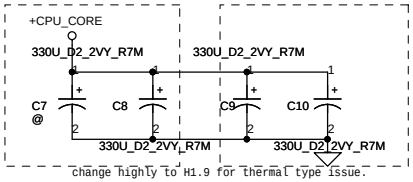
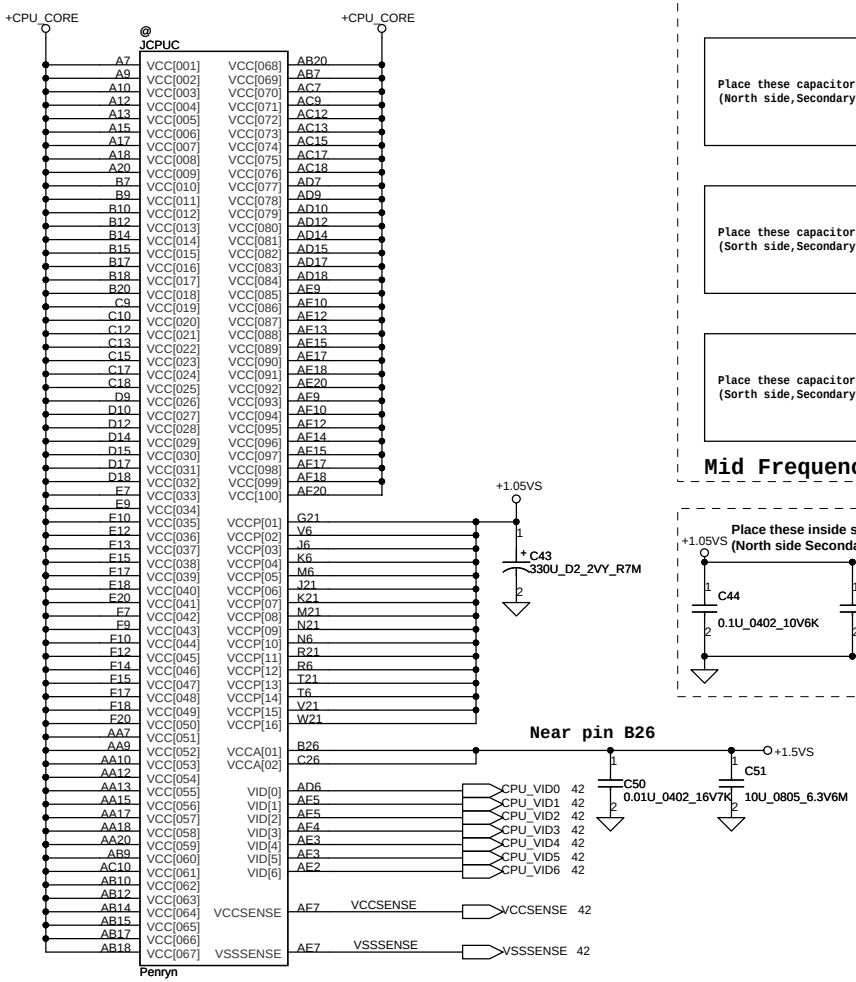
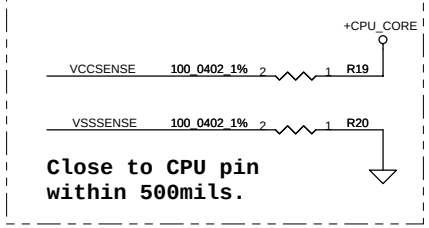
Near CPU CORE regulator

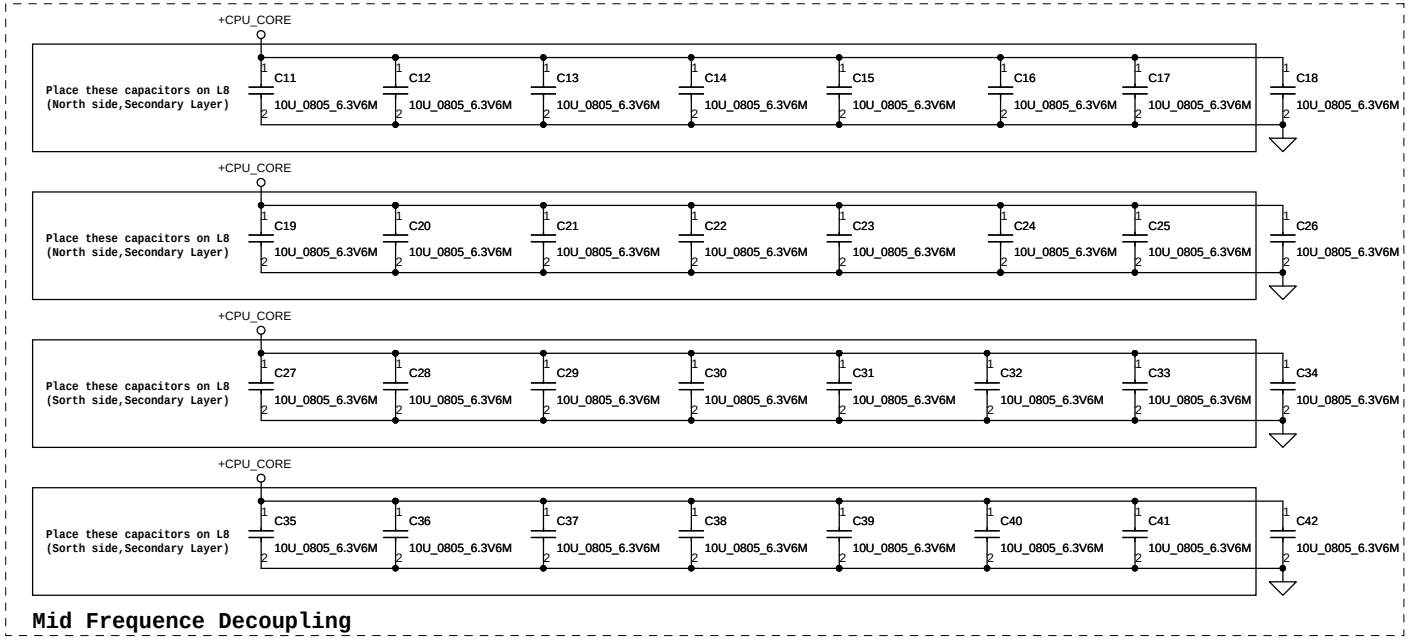
ESR <= 1.5m ohm
Capacitor > 1980uF

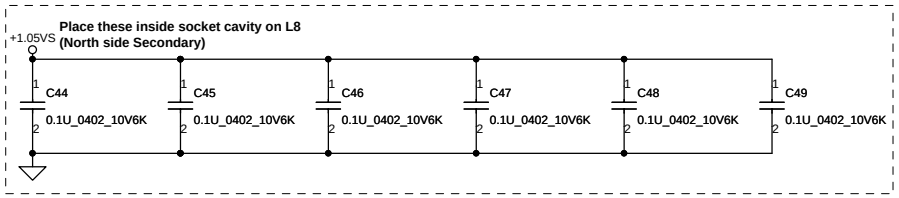






Length match within 25 mils.
The trace width/space/other is 14/7/25.





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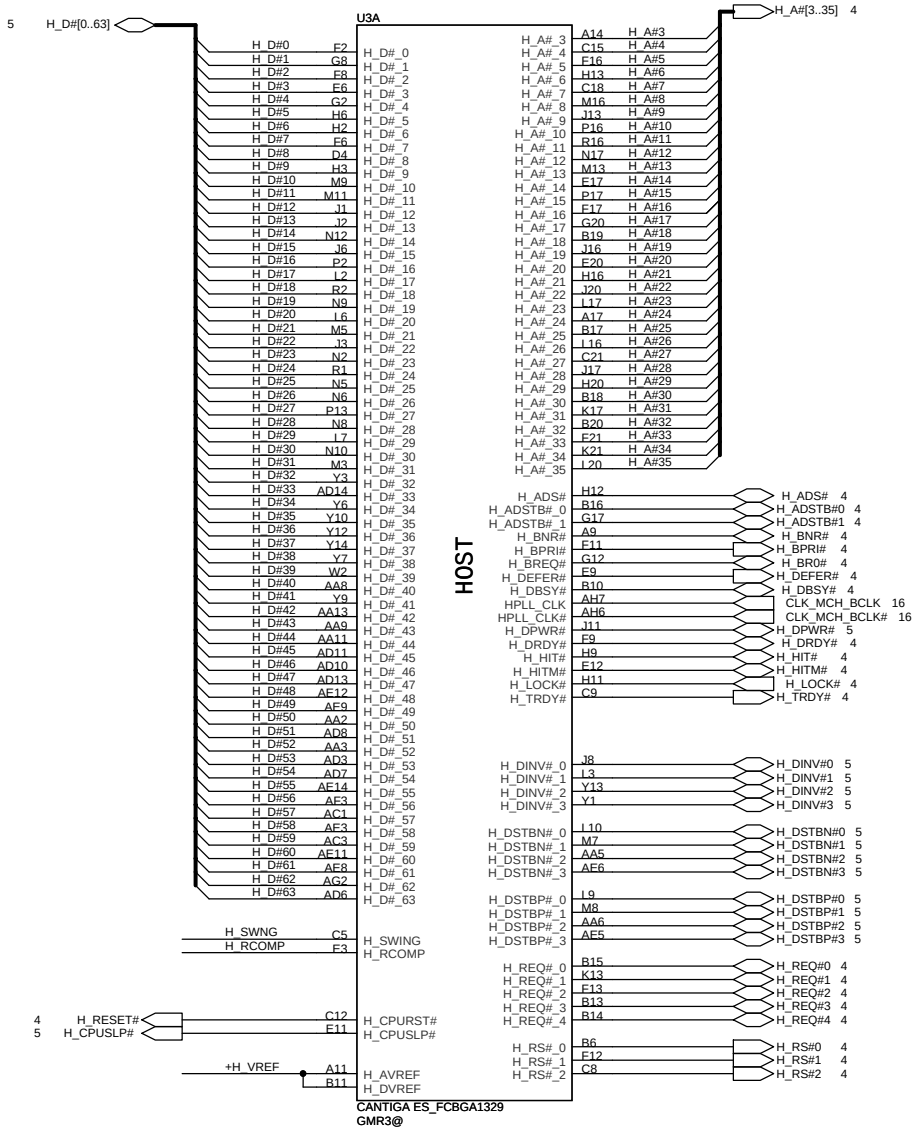
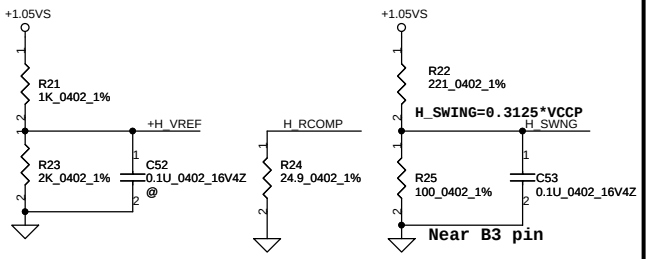


Layout Note:
H_RCOMP / +H_VREF / H_SWNG
trace width and spacing is 10/20
within 100 mils from NB



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Strap Pin Table

CFG[2:0]		011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	Internal pull-up	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG6	Internal pull-up	0 = iTPM Host Interface is enabled can support disble by SW. 1 = iTPM Host Interface is Disabled *(Default)
CFG7	Internal pull-up	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality *(Default)
CFG9	Internal pull-up	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG10	Internal pull-up	0 = PCIe Loopback Enable 1 = Disable*(Default)
CFG[13:12]	Internal pull-up	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation*(Default)
CFG16	Internal pull-up	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG19	Internal pull-down	0 = Normal Operation 1 = DMI Lane Reversal Enable *(Default)
CFG20 (PCIE/SDVO select)	Internal pull-down	0 = Only PCIE or [SDVO/DP/HDMI] is operational. * (Default) 1 = PCIE/[SDVO/DP/HDMI] are operating simu.

U3B

RSVD: RSVD1 RSVD2 RSVD3 RSVD4 RSVD5 RSVD6 RSVD7 RSVD8 RSVD9 RSVD10 RSVD11 RSVD12 RSVD13 RSVD14 RSVD15 RSVD16 RSVD17 RSVD20 RSVD22 RSVD23 RSVD24 RSVD25

DDR CLK/ CONTROL/ COMPENSATION: SA_CK_0 SA_CK_1 SB_CK_0 SB_CK_1 SA_CK#_0 SA_CK#_1 SB_CK#_0 SB_CK#_1 SA_CKE_0 SA_CKE_1 SB_CKE_0 SB_CKE_1 SA_CS#_0 SA_CS#_1 SB_CS#_0 SB_CS#_1 SA_ODT_0 SA_ODT_1 SB_ODT_O SB_ODT_1 SM_RCOMP SM_RCOMP# SM_RCOMP_VOH SM_RCOMP_VOL SM_VREF SM_PWROK SM_REXT SM_DRAMRST#

CLK: DPLL_REF_CLK DPLL_REF_CLK# DPLL_REF_SSCLK DPLL_REF_SSCLK# PEG_CLK PEG_CLK#

DMI: DMI_RXN_0 DMI_RXN_1 DMI_RXN_2 DMI_RXN_3 DMI_RXP_0 DMI_RXP_1 DMI_RXP_2 DMI_RXP_3 DMI_TXN_0 DMI_TXN_1 DMI_TXN_2 DMI_TXN_3 DMI_TXP_0 DMI_TXP_1 DMI_TXP_2 DMI_TXP_3

GRAPHICS VID: GFX_VID_0 GFX_VID_1 GFX_VID_2 GFX_VID_3 GFX_VID_4 GFX_VR_EN

ME: CL_CLK CL_DATA CL_PWROK CL_RST# CL_VREF

MISC: DDPC_CTRLCLK DDPC_CTRLDATA SDVO_CTRLCLK SDVO_CTRLDATA ICH_SYNC# TSATN#

HDA: HDA_BCLK HDA_RST# HDA_SDI HDA_SDO HDA_SYNC

CFG: CFG_0 CFG_1 CFG_2 CFG_3 CFG_4 CFG_5 CFG_6 CFG_7 CFG_8 CFG_9 CFG_10 CFG_11 CFG_12 CFG_13 CFG_14 CFG_15 CFG_16 CFG_17 CFG_18 CFG_19 CFG_20

PM: PM_SYNC# PM_DPRSTP# PM_EXT_TS#_0 PM_EXT_TS#_1 PWROK RSTIN# THERMTRIP# DPRSLPVR

NC: NC_1 NC_2 NC_3 NC_4 NC_5 NC_6 NC_7 NC_8 NC_9 NC_10 NC_11 NC_12 NC_13 NC_14 NC_15 NC_16 NC_17 NC_18 NC_19 NC_20 NC_21 NC_22 NC_23 NC_24 NC_25 NC_26

CANTIGA ES_FCBGA1329

GMR3@

SM_DRAMRST# would be needed for DDR3 only

For Cantiga 80 Ohm

20mil

Please place these resistors close to related balls

Lane reversal

Use VGATE for GMCH_PWROK

Strap Pin Table

SDVO_CTRLDATA (Internal pull-down)	0 = SDVO interface disabled *(Default) 1 = SDVO interface enabled
DDPC_CTRLDATA (Internal pull-down)	0 = Digital display (iHDMI/DP) interface disabled 1 = Digital display (iHDMI/DP) interface enabled *(Default)

CL_VREF should be 0.35 V

+CL_VREF=0.355V

Width:Spacing 12mil:12mil

the strap pin will impact no IHDMI SKU if mount R62

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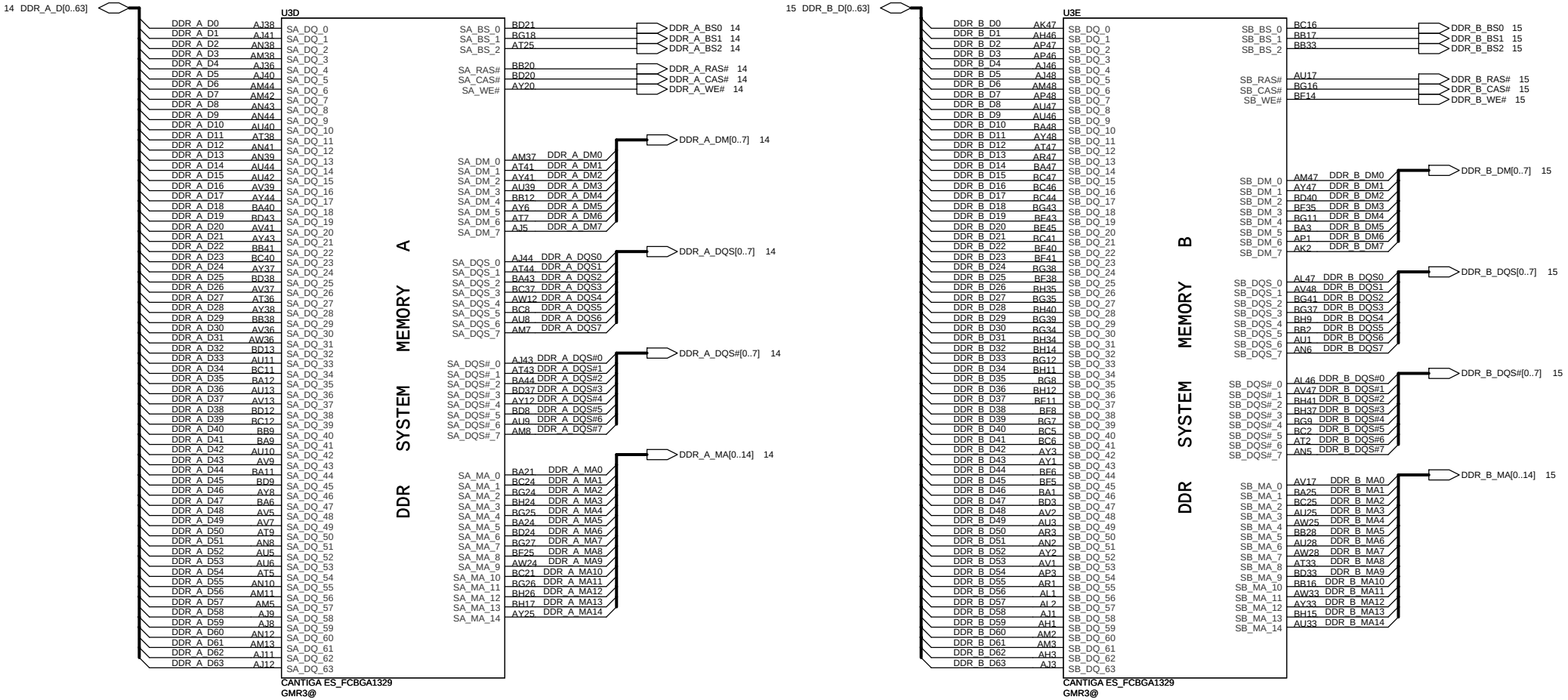

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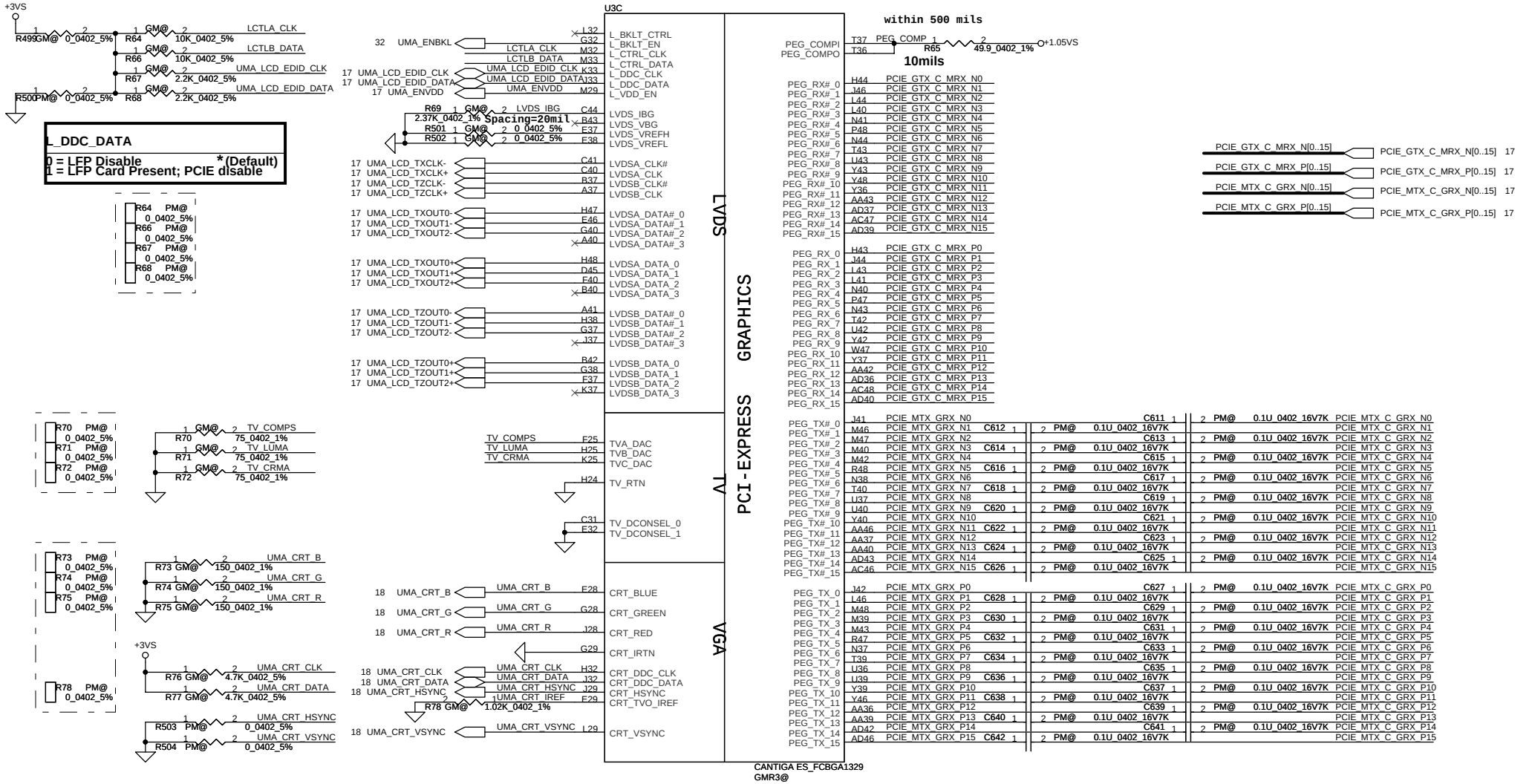

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U3F

DDR2,667MHz,2600mA
DDR2,800MHz,3000mA

+1.8V

DDR PWR

10U_0805_10V4Z

C78 220U_6.3V_M

C68 220U_D2_4VM_R15 @

C69

C70

C71

10U_0805_10V4Z

0.1U_0402_16V4Z

reserve for test

VCC_SM_1 AP33
VCC_SM_2 AN33
VCC_SM_3 BH32
VCC_SM_4 BG32
VCC_SM_5 BF32
VCC_SM_6 BD32
VCC_SM_7 BC32
VCC_SM_8 BB32
VCC_SM_9 BA32
VCC_SM_10 AV32
VCC_SM_11 AW32
VCC_SM_12 AV32
VCC_SM_13 AU32
VCC_SM_14 AT32
VCC_SM_15 AR32
VCC_SM_16 AP32
VCC_SM_17 AN32
VCC_SM_18 BH31
VCC_SM_19 BG31
VCC_SM_20 BE31
VCC_SM_21 BG30
VCC_SM_22 BH29
VCC_SM_23 BG29
VCC_SM_24 BF29
VCC_SM_25 BD29
VCC_SM_26 BC29
VCC_SM_27 BB29
VCC_SM_28 BA29
VCC_SM_29 AY29
VCC_SM_30 AW29
VCC_SM_31 AV29
VCC_SM_32 AU29
VCC_SM_33 AT29
VCC_SM_34 AR29
VCC_SM_35 AP29

VCC SM

Could be NC for DDR2 Board

VCC_SM_36/NC BA36
VCC_SM_37/NC BB24
VCC_SM_38/NC BD16
VCC_SM_39/NC BB21
VCC_SM_40/NC AW16
VCC_SM_41/NC AW13
VCC_SM_42/NC AT13

VCC GFX NCTF

8700mA

POWER

+NB_VCCAXG

Int. Graphic

Extnal Graphic: 1210.34mA
integrated Graphic: 1930.4mA
Intel Management Engine Link:508.12mA

VCC_AXG_NTCF_1 W28
VCC_AXG_NCTF_2 V28
VCC_AXG_NCTF_3 W26
VCC_AXG_NCTF_4 V26
VCC_AXG_NCTF_5 W25
VCC_AXG_NCTF_6 V25
VCC_AXG_NCTF_7 W24
VCC_AXG_NCTF_8 V24
VCC_AXG_NCTF_9 W23
VCC_AXG_NCTF_10 V23
VCC_AXG_NCTF_11 AM21
VCC_AXG_NCTF_12 AL21
VCC_AXG_NCTF_13 AK21
VCC_AXG_NCTF_14 W21
VCC_AXG_NCTF_15 V21
VCC_AXG_NCTF_16 U21
VCC_AXG_NCTF_17 AM20
VCC_AXG_NCTF_18 AK20
VCC_AXG_NCTF_19 W20
VCC_AXG_NCTF_20 U20
VCC_AXG_NCTF_21 AM19
VCC_AXG_NCTF_22 AL19
VCC_AXG_NCTF_23 AK19
VCC_AXG_NCTF_24 AJ19
VCC_AXG_NCTF_25 AH19
VCC_AXG_NCTF_26 AG19
VCC_AXG_NCTF_27 AF19
VCC_AXG_NCTF_28 AF19
VCC_AXG_NCTF_29 AB19
VCC_AXG_NCTF_30 AA19
VCC_AXG_NCTF_31 Y19
VCC_AXG_NCTF_32 W19
VCC_AXG_NCTF_33 V19
VCC_AXG_NCTF_34 U19
VCC_AXG_NCTF_35 AM17
VCC_AXG_NCTF_36 AK17
VCC_AXG_NCTF_37 AH17
VCC_AXG_NCTF_38 AG17
VCC_AXG_NCTF_39 AF17
VCC_AXG_NCTF_40 AE17
VCC_AXG_NCTF_41 AC17
VCC_AXG_NCTF_42 AB17
VCC_AXG_NCTF_43 Y17
VCC_AXG_NCTF_44 W17
VCC_AXG_NCTF_45 V17
VCC_AXG_NCTF_46 AM16
VCC_AXG_NCTF_47 AL16
VCC_AXG_NCTF_48 AK16
VCC_AXG_NCTF_49 AJ16
VCC_AXG_NCTF_50 AH16
VCC_AXG_NCTF_51 AG16
VCC_AXG_NCTF_52 AF16
VCC_AXG_NCTF_53 AE16
VCC_AXG_NCTF_54 AC16
VCC_AXG_NCTF_55 AB16
VCC_AXG_NCTF_56 AA16
VCC_AXG_NCTF_57 Y16
VCC_AXG_NCTF_58 W16
VCC_AXG_NCTF_59 V16
VCC_AXG_NCTF_60 U16

VCC GFX

For layout placement un-mound C123 and mound C84

Int. Graphic

+1.05VS

220U_D2_4VM_R15

C83 GM@

C84 @

220U_D2_4VM_R15

+NB_VCCAXG

10U_0805_10V4Z

C85 GM@

C86 GM@

C87 GM@

0.47U_0603_10V7K

C88 GM@

C89 GM@

0.1U_0402_16V4Z

C90 GM@

10U_0805_10V4Z

1U_0402_6.3V4Z

0.1U_0402_16V4Z

Intel:AXG and AXG_NCTF -- 220U*2, ESR 15mOhm

For layout issue to separate 220u*2 to +1.05VS

C86 PM@
0_0805_5%

VCC_AXG_1 Y26
VCC_AXG_2 AE25
VCC_AXG_3 AB25
VCC_AXG_4 AA25
VCC_AXG_5 AE24
VCC_AXG_6 AC24
VCC_AXG_7 AA24
VCC_AXG_8 Y24
VCC_AXG_9 AE23
VCC_AXG_10 AC23
VCC_AXG_11 AB23
VCC_AXG_12 AA23
VCC_AXG_13 AJ21
VCC_AXG_14 AG21
VCC_AXG_15 AE21
VCC_AXG_16 AC21
VCC_AXG_17 AA21
VCC_AXG_18 V21
VCC_AXG_19 AH20
VCC_AXG_20 AE20
VCC_AXG_21 AE20
VCC_AXG_22 AC20
VCC_AXG_23 AB20
VCC_AXG_24 AA20
VCC_AXG_25 T17
VCC_AXG_26 T16
VCC_AXG_27 AM15
VCC_AXG_28 AL15
VCC_AXG_29 AE15
VCC_AXG_30 AJ15
VCC_AXG_31 AH15
VCC_AXG_32 AG15
VCC_AXG_33 AE15
VCC_AXG_34 AB15
VCC_AXG_35 AA15
VCC_AXG_36 Y15
VCC_AXG_37 V15
VCC_AXG_38 U15
VCC_AXG_39 AN14
VCC_AXG_40 AM14
VCC_AXG_41 U14
VCC_AXG_42 T14

PAD T3 AJ14 VCC_AXG_SENSE
PAD T4 AH14 VSS_AXG_SENSE

+1.05VS

+NB_VCCAXG

PJ27 JUMP_43X39 @
PJ28 JUMP_43X39 @
PJ29 JUMP_43X39 @
PJ30 JUMP_43X39 @
PJ31 JUMP_43X39 @
PJ32 JUMP_43X39 @

CANTIGA ES_FCBGA1329
GMR3@

+1.05VS

NB Core,Intel Management Engine Link

220U_6.3V_M

0.22U_0402_10V4Z

0.1U_0402_16V4Z

C72 GM@

C73

C74

C75

C76

C77

220U_6.3V_M

10U_0805_10V4Z

0.22U_0402_10V4Z

Intel: VCC -- 220U*2, ESR 12mOhm

U3G

VCC_1 AG34
VCC_2 AC34
VCC_3 AB34
VCC_4 AA34
VCC_5 Y34
VCC_6 V34
VCC_7 U34
VCC_8 AM33
VCC_9 AK33
VCC_10 AJ33
VCC_11 AG33
VCC_12 AE33
VCC_13 AE33
VCC_14 AC33
VCC_15 AA33
VCC_16 Y33
VCC_17 W33
VCC_18 V33
VCC_19 U33
VCC_20 AH28
VCC_21 AF28
VCC_22 AC28
VCC_23 AA28
VCC_24 AJ26
VCC_25 AG26
VCC_26 AF26
VCC_27 AC26
VCC_28 AH25
VCC_29 AG25
VCC_30 AF25
VCC_31 AG24
VCC_32 AJ23
VCC_33 AH23
VCC_34 AF23
VCC_35 T32

VCC CORE POWER

CANTIGA ES_FCBGA1329
GMR3@

+1.05VS

VCC_NCTF_1 AM32
VCC_NCTF_2 AL32
VCC_NCTF_3 AK32
VCC_NCTF_4 AJ32
VCC_NCTF_5 AH32
VCC_NCTF_6 AG32
VCC_NCTF_7 AE32
VCC_NCTF_8 AC32
VCC_NCTF_9 AA32
VCC_NCTF_10 Y32
VCC_NCTF_11 W32
VCC_NCTF_12 U32
VCC_NCTF_13 AM30
VCC_NCTF_14 AL30
VCC_NCTF_15 AK30
VCC_NCTF_16 AH30
VCC_NCTF_17 AG30
VCC_NCTF_18 AE30
VCC_NCTF_19 AE30
VCC_NCTF_20 AC30
VCC_NCTF_21 AB30
VCC_NCTF_22 AA30
VCC_NCTF_23 Y30
VCC_NCTF_24 W30
VCC_NCTF_25 V30
VCC_NCTF_26 U30
VCC_NCTF_27 AL29
VCC_NCTF_28 AK29
VCC_NCTF_29 AJ29
VCC_NCTF_30 AH29
VCC_NCTF_31 AG29
VCC_NCTF_32 AE29
VCC_NCTF_33 AC29
VCC_NCTF_34 AA29
VCC_NCTF_35 Y29
VCC_NCTF_36 W29
VCC_NCTF_37 V29
VCC_NCTF_38 AL28
VCC_NCTF_39 AK28
VCC_NCTF_40 AL26
VCC_NCTF_41 AK26
VCC_NCTF_42 AK25
VCC_NCTF_43 AK24
VCC_NCTF_44 AK23

VCC NCTF

VCC SM LF

VCC_SM_LF1 AV44 VCCSM_LF1
VCC_SM_LF2 BA37 VCCSM_LF2
VCC_SM_LF3 AM40 VCCSM_LF3
VCC_SM_LF4 AV21 VCCSM_LF4
VCC_SM_LF5 AY5 VCCSM_LF5
VCC_SM_LF6 AM10 VCCSM_LF6
VCC_SM_LF7 BB13 VCCSM_LF7

C91 0.1U_0402_16V4Z

C92 0.1U_0402_16V4Z

C93 0.22U_0603_10V7K

C94 0.22U_0603_10V7K

C95 0.47U_0603_10V7K

C96 1U_0402_6.3V4Z

C97 1U_0402_6.3V4Z

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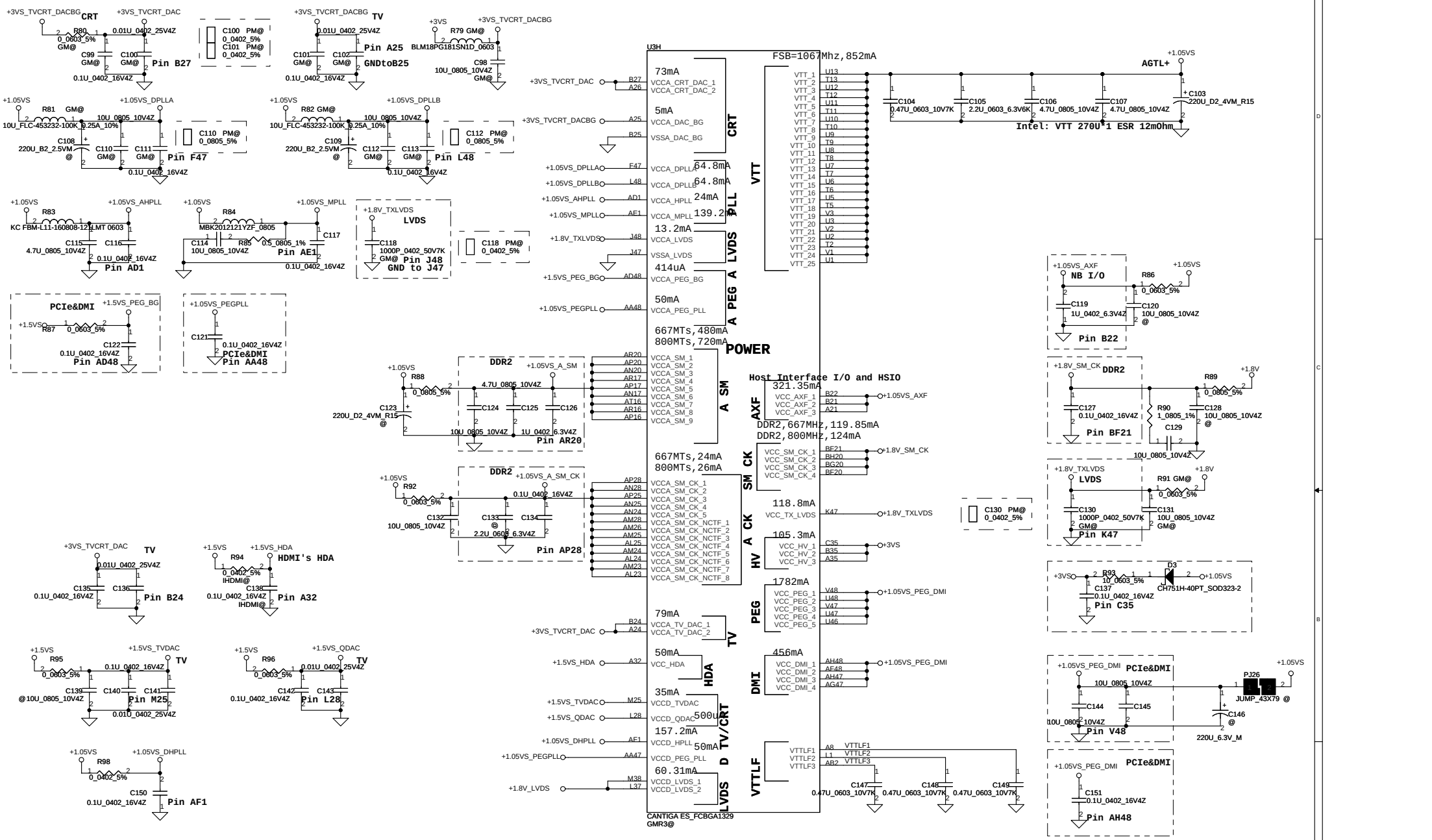

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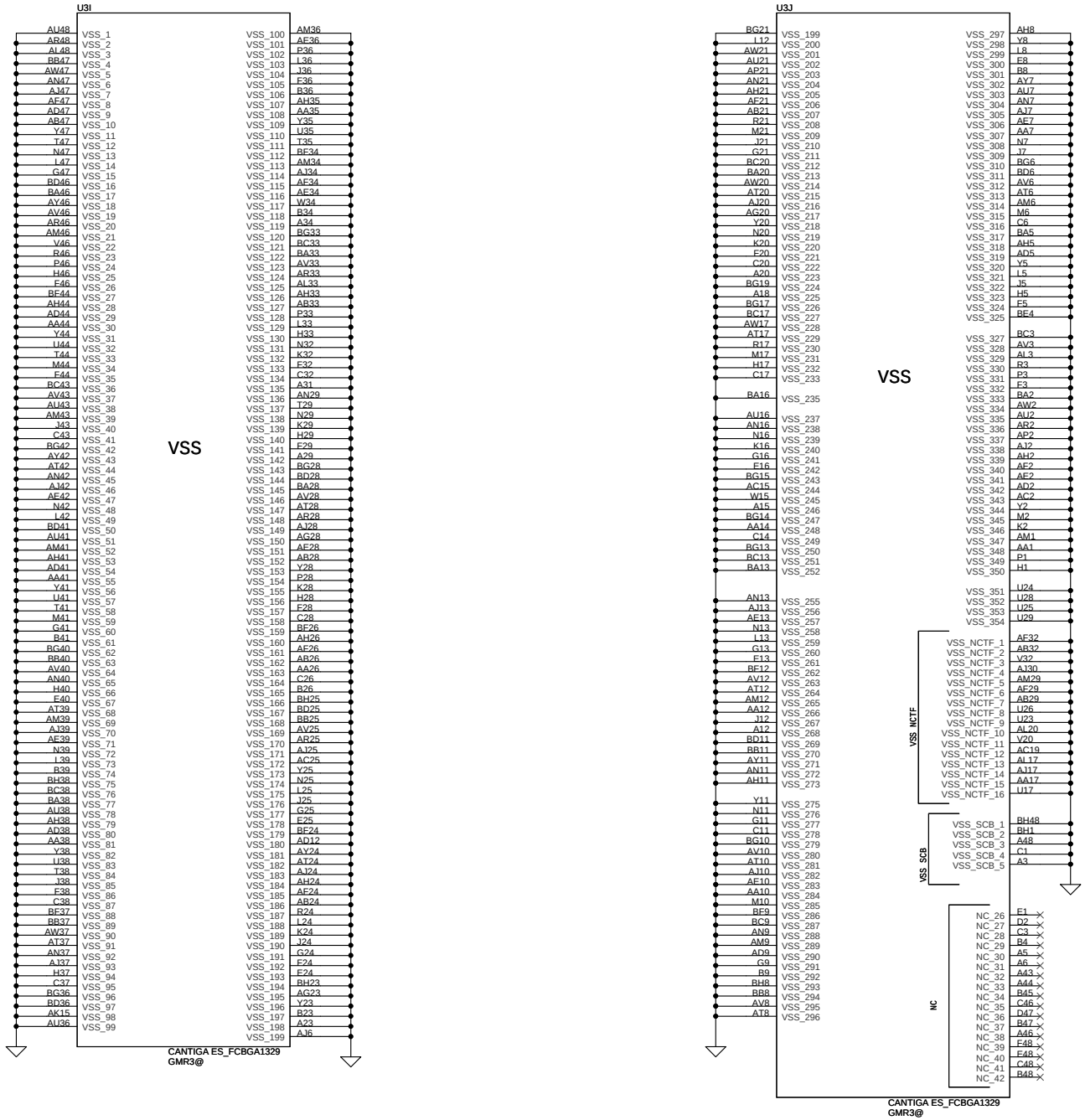

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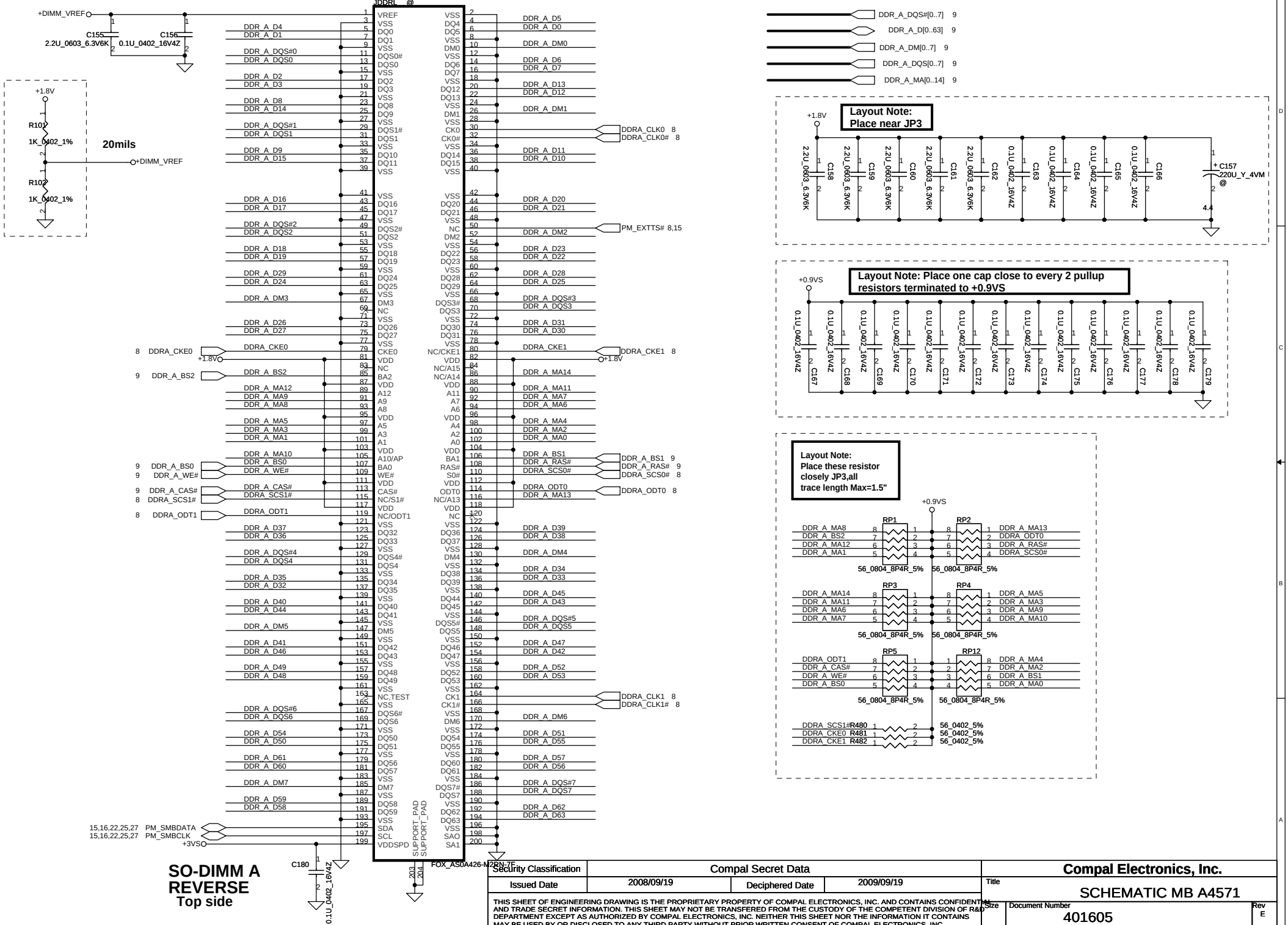

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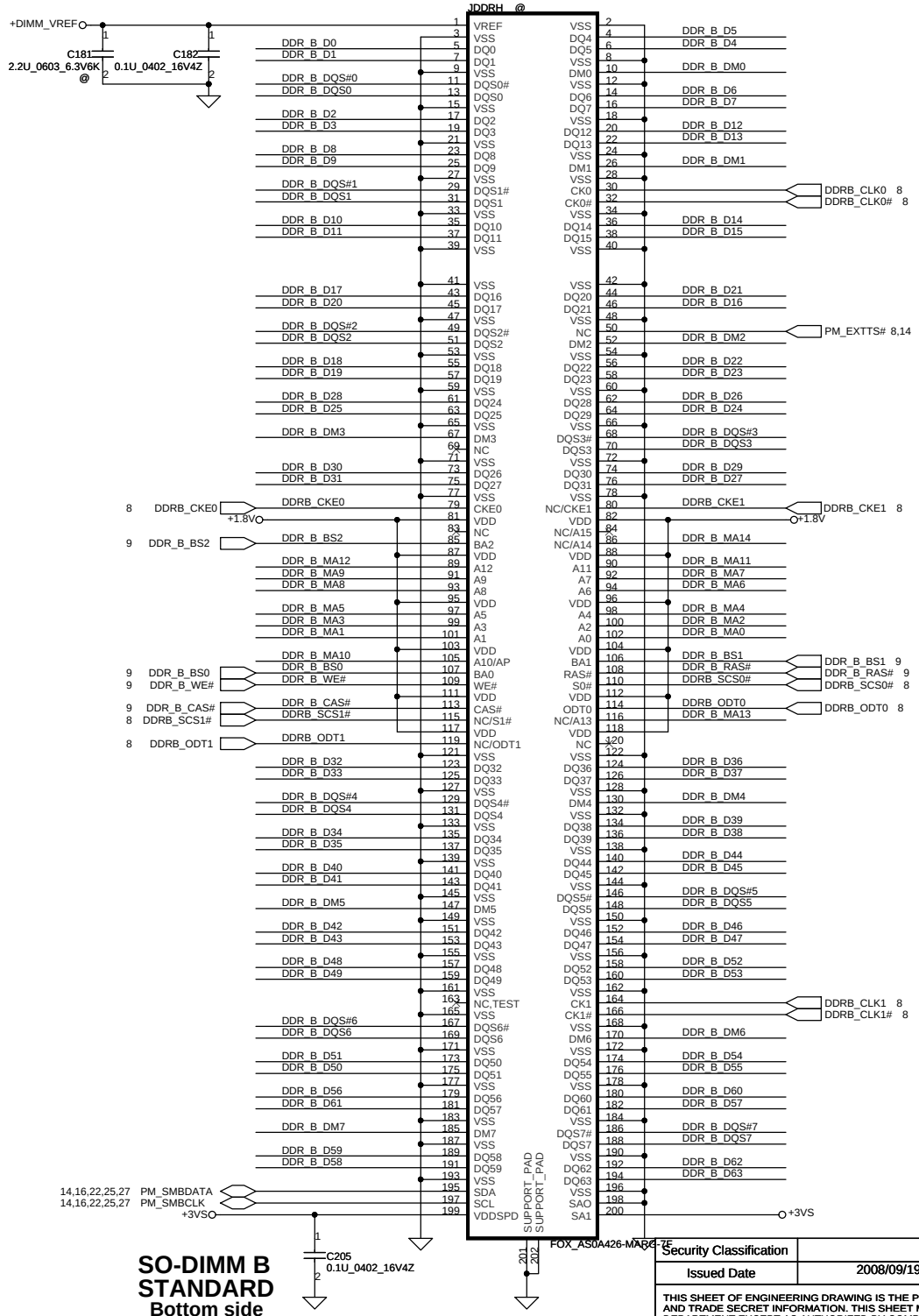
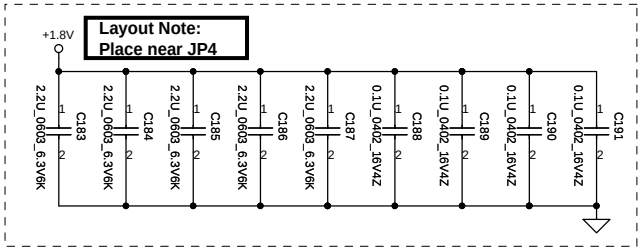
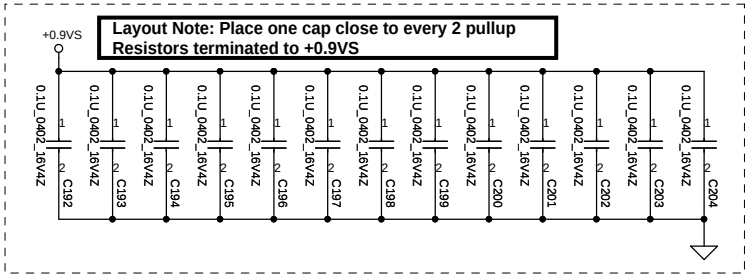


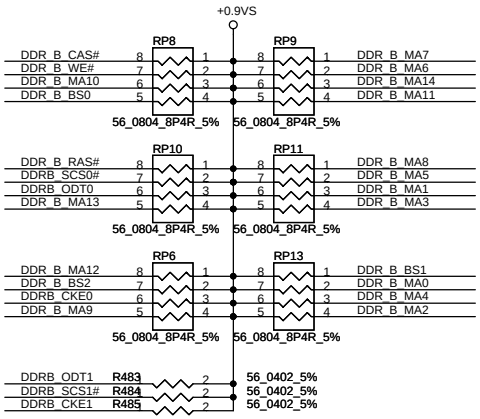
SO-DIMM B
STANDARD
Bottom side

DDR_B_DQS#[0..7] 9
DDR_B_D[0..63] 9
DDR_B_DM[0..7] 9
DDR_B_DQS[0..7] 9
DDR_B_MA[0..14] 9





Layout Note:
Place these resistor closely JP4,all trace length Max=1.5"



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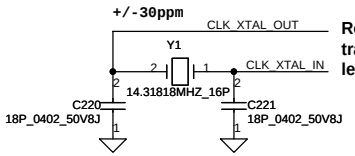
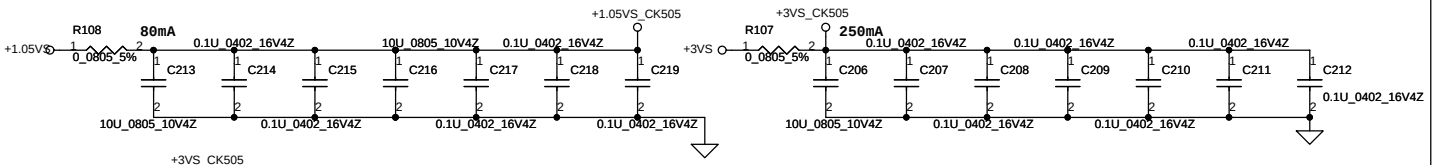
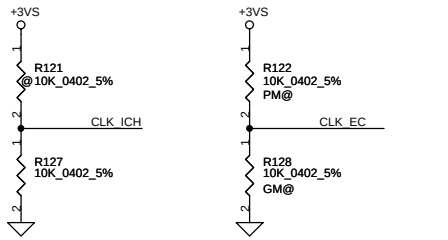
FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



Routing the trace at least 10mil



CLK_ICH	0 = SRC8/SRC8# (100MHz) 1 = ITP/ITP# (266MHz)
CLK_EC	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)



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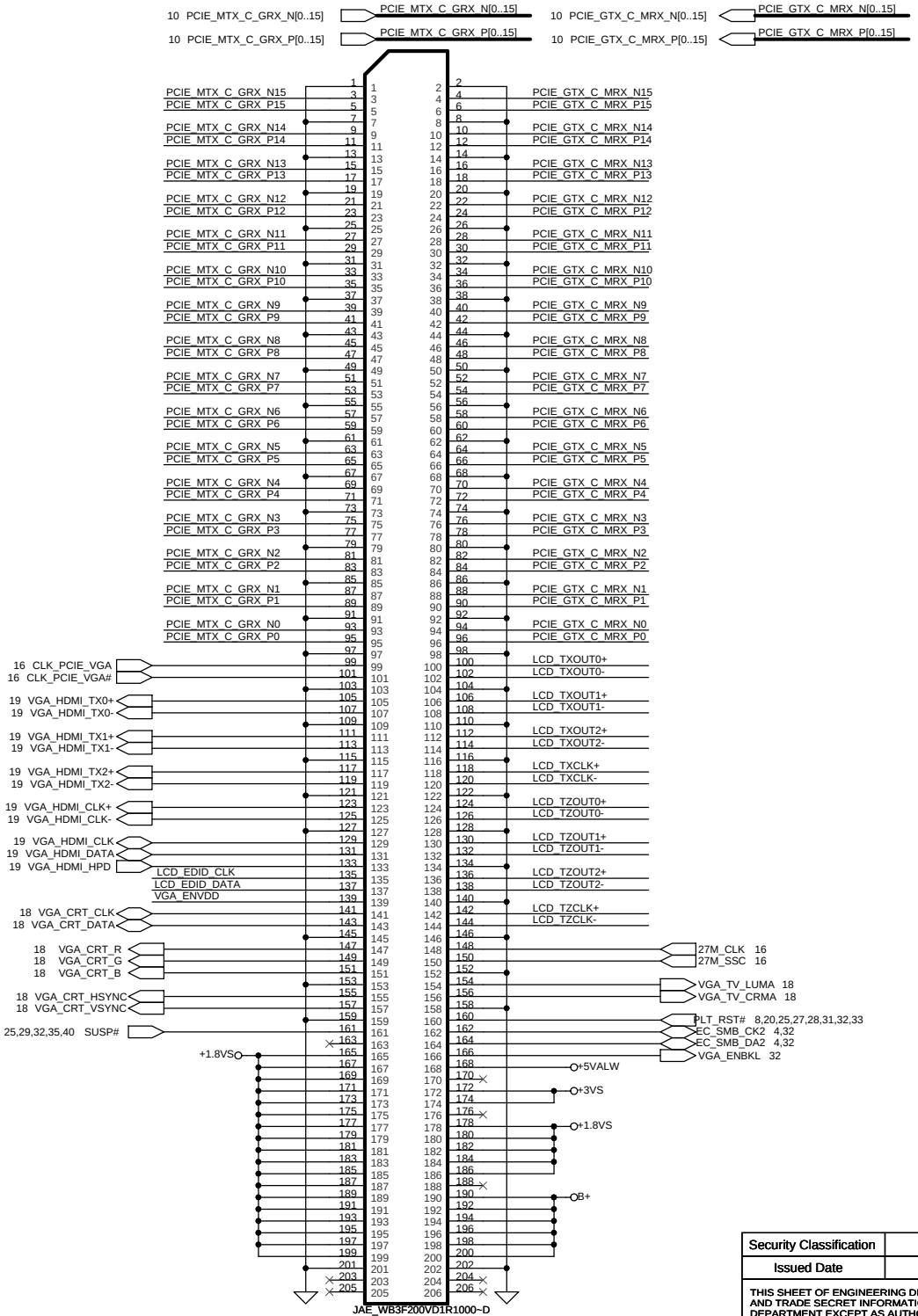
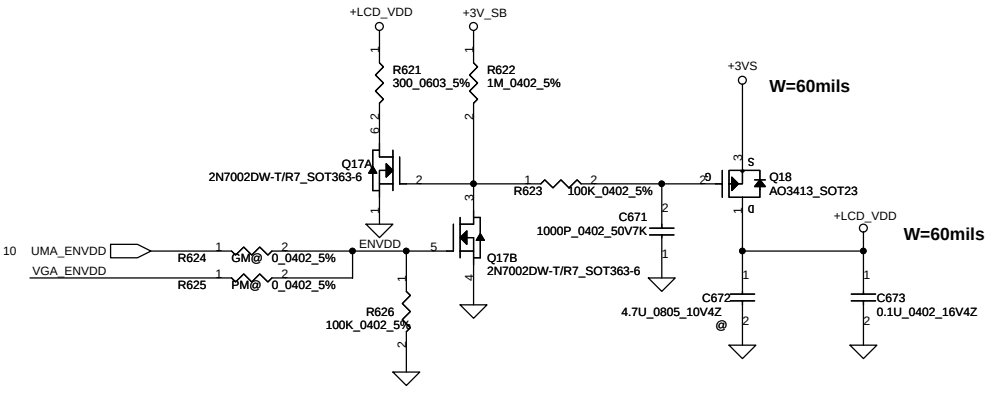
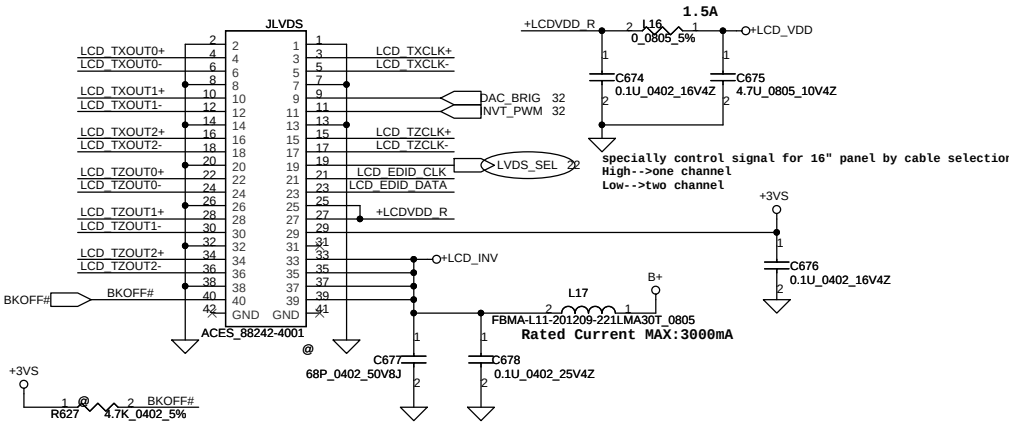
LCD/PANEL BD. Conn.







VGA side

please link to VGA Conn. then link to LVDS Conn.

LVDS conn. **NB side**

LCD_TXOUT0+	0_0402_5%	GM@	R629	UMA_LCD_TXOUT0+ 10
LCD_TXOUT0-	0_0402_5%	GM@	R631	UMA_LCD_TXOUT0- 10
LCD_TXOUT1+	0_0402_5%	GM@	R633	UMA_LCD_TXOUT1+ 10
LCD_TXOUT1-	0_0402_5%	GM@	R635	UMA_LCD_TXOUT1- 10
LCD_TXOUT2+	0_0402_5%	GM@	R637	UMA_LCD_TXOUT2+ 10
LCD_TXOUT2-	0_0402_5%	GM@	R639	UMA_LCD_TXOUT2- 10
LCD_TXCLK+	0_0402_5%	GM@	R641	UMA_LCD_TXCLK+ 10
LCD_TXCLK-	0_0402_5%	GM@	R643	UMA_LCD_TXCLK- 10
LCD_TZOUT0+	0_0402_5%	GM@	R645	UMA_LCD_TZOUT0+ 10
LCD_TZOUT0-	0_0402_5%	GM@	R647	UMA_LCD_TZOUT0- 10
LCD_TZOUT1+	0_0402_5%	GM@	R649	UMA_LCD_TZOUT1+ 10
LCD_TZOUT1-	0_0402_5%	GM@	R651	UMA_LCD_TZOUT1- 10
LCD_TZOUT2+	0_0402_5%	GM@	R653	UMA_LCD_TZOUT2+ 10
LCD_TZOUT2-	0_0402_5%	GM@	R655	UMA_LCD_TZOUT2- 10
LCD_TZCLK+	0_0402_5%	GM@	R657	UMA_LCD_TZCLK+ 10
LCD_TZCLK-	0_0402_5%	GM@	R659	UMA_LCD_TZCLK- 10
LCD_EDID_CLK	0_0402_5%	GM@	R661	UMA_LCD_EDID_CLK 10
LCD_EDID_DATA	0_0402_5%	GM@	R663	UMA_LCD_EDID_DATA 10

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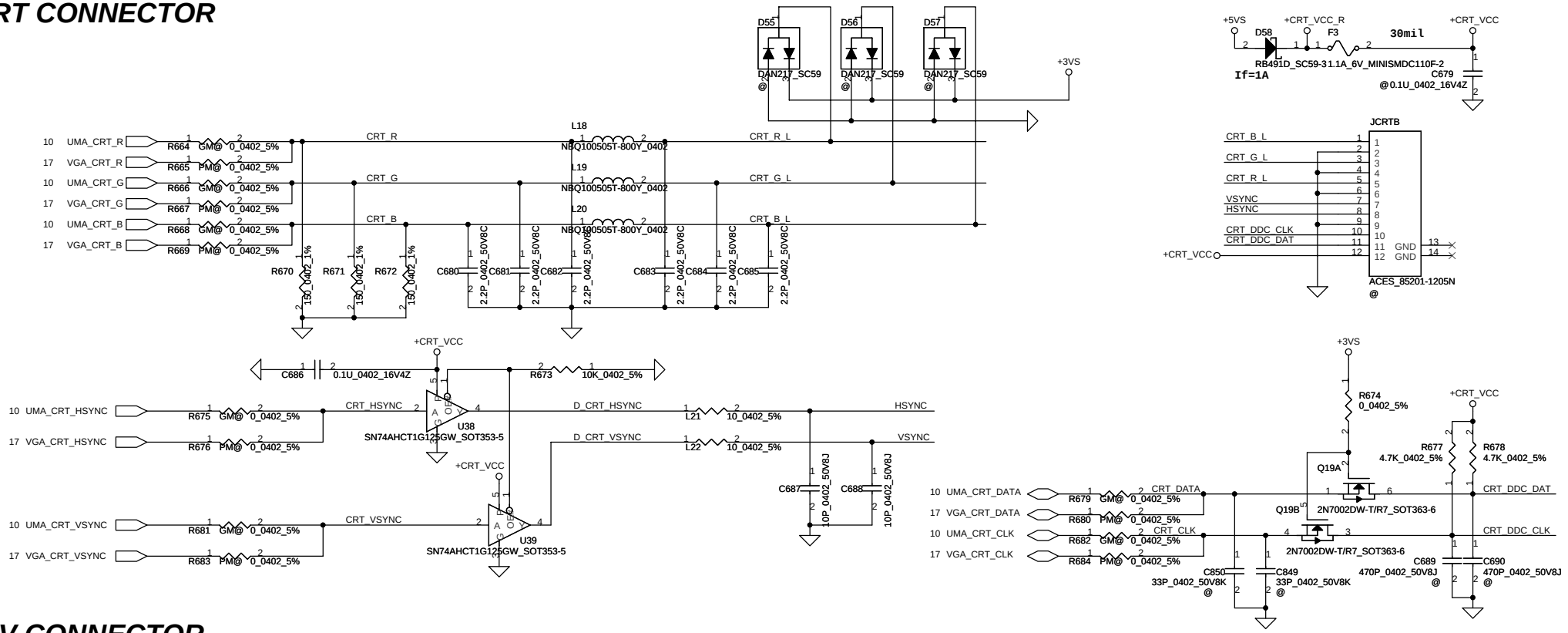
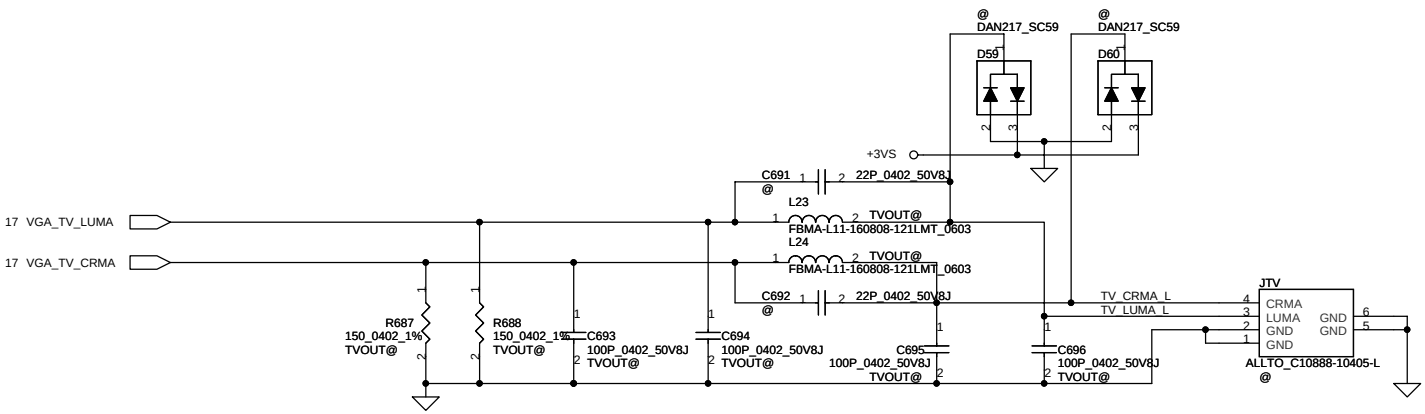
CRT CONNECTOR



TV CONNECTOR



TV-OUT Conn.

1. Y ground
2. C ground
3. Y (luminance+sync)
4. C (crominance)

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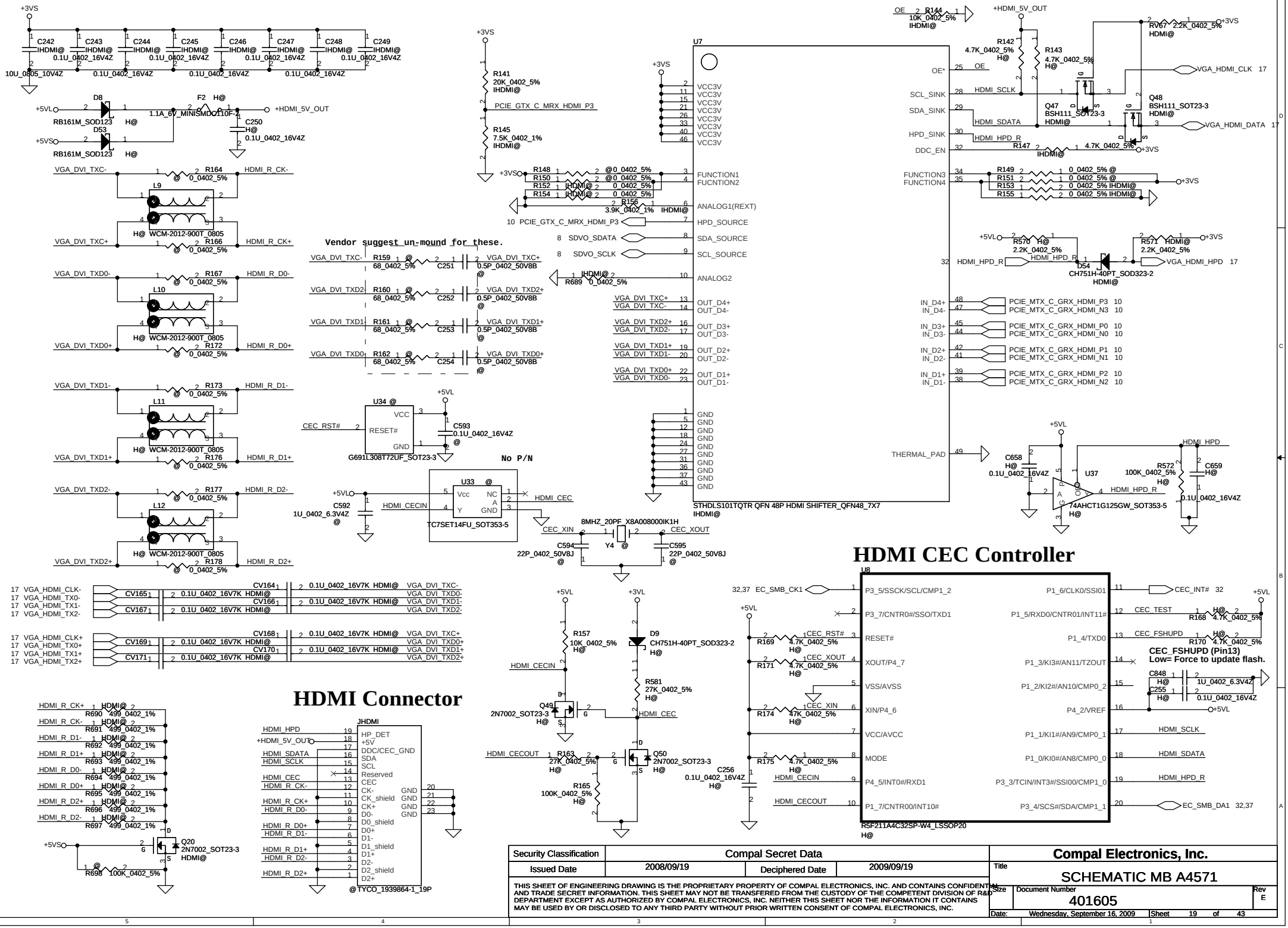

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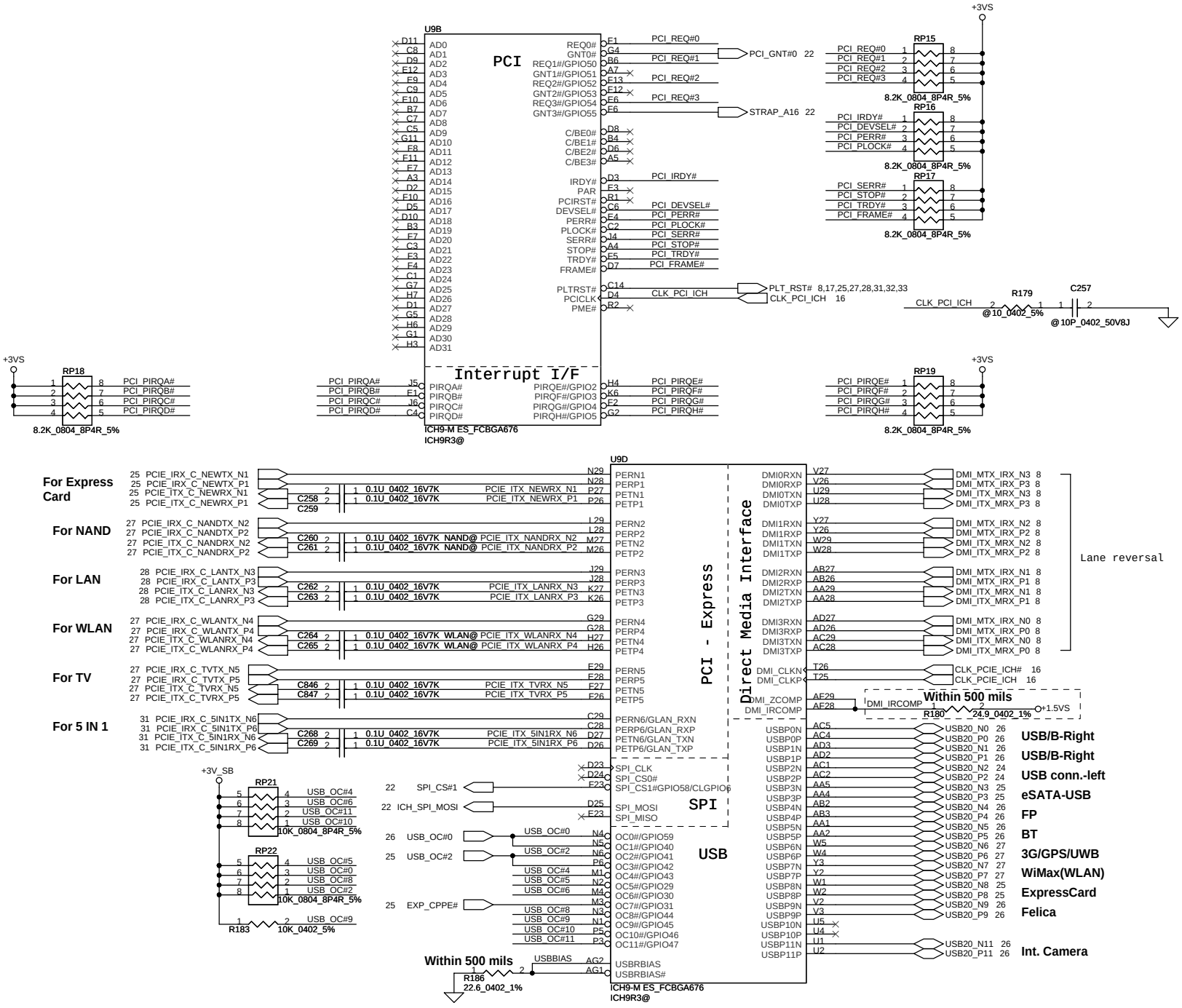

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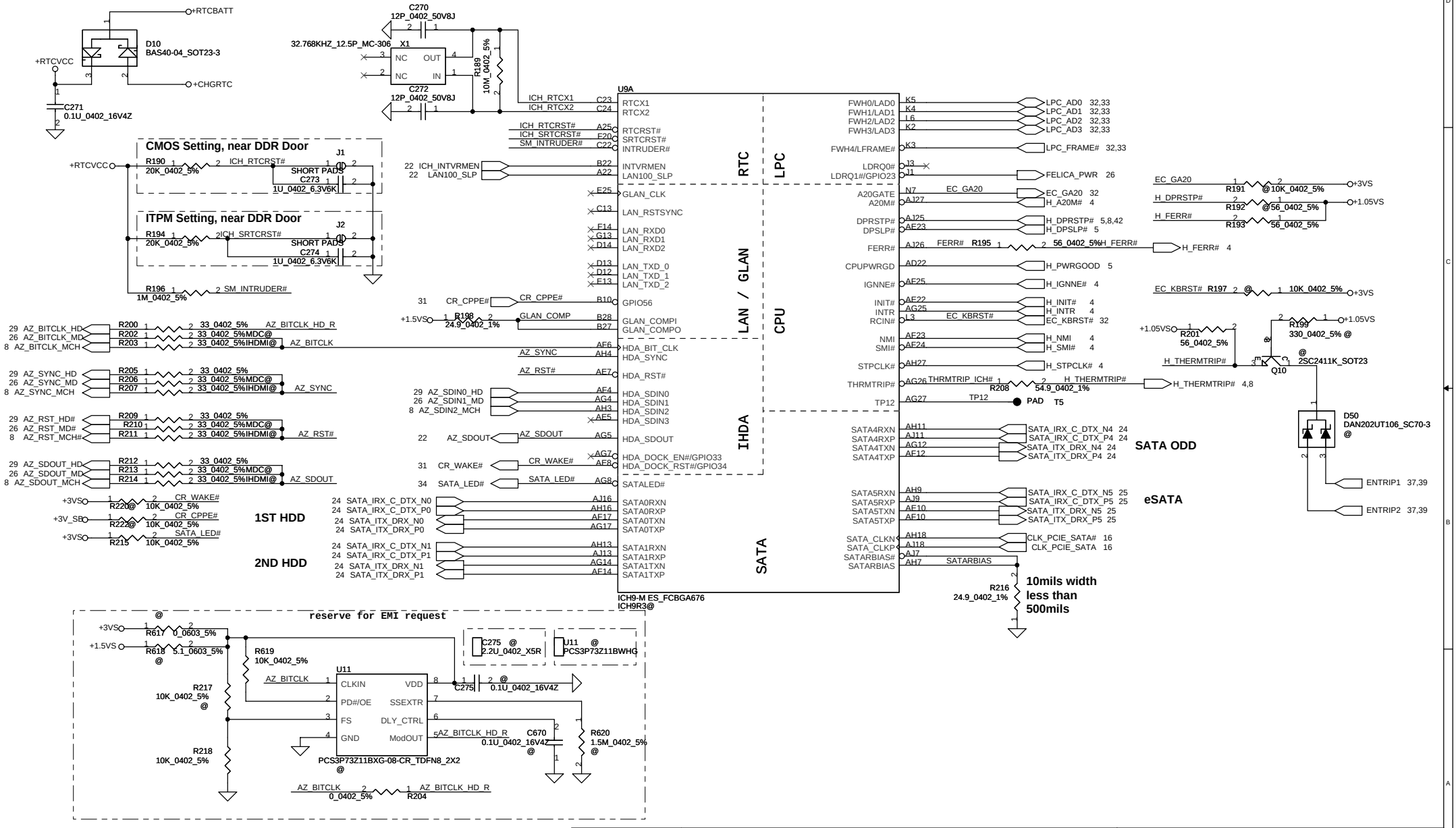

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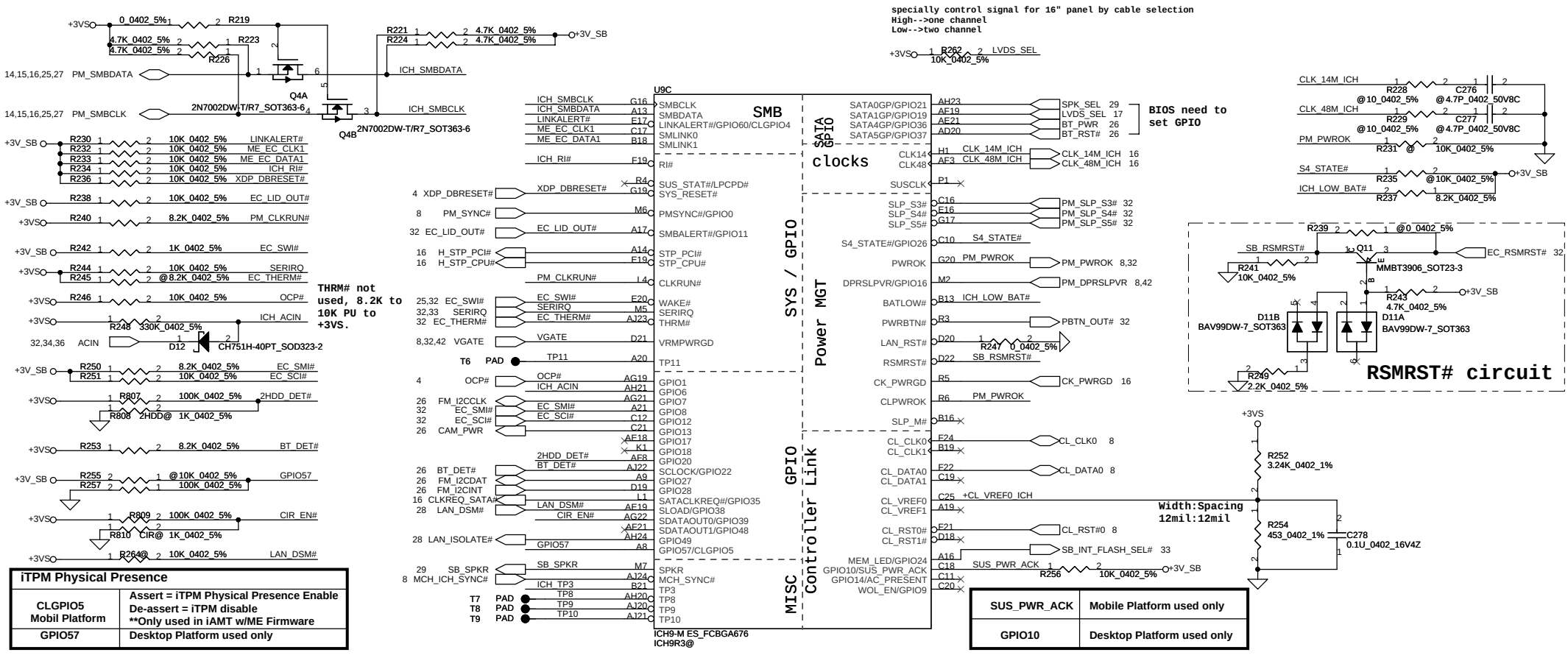

ICH9M Strap Pin

Internal TPM Strap(Internal pull-down)

SPI_MOSI	Low= Disable High= iTPM enable by MCH strap*

No Reboot Strap (Internal pull-up)

SB_SPKR	Low= *Default High= "No Reboot"

Boot BIOS Strap (Internal pull-up)

PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	0	RESERVED
0	1	SPI
1	0	PCI
1	1	LPC* (Default)

A16 Swap Override Strap

PCI_GNT#3	Low= A16 swap override Enable High= Default* (Internal pull-up)

Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)

ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

Flash Descriptor Security Override Strap

GPIO33	Low= Descriptor Security override High= Default* (Internal pull-up)

DMI Termination Voltage

GPIO49	Low= Desktop used High= Mobile* (Internal pull-up)

XOR Chain Entrance Strap

ICH_TP3 (Internal pull-up)	HDA_SDOUT (Internal pull-down)	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

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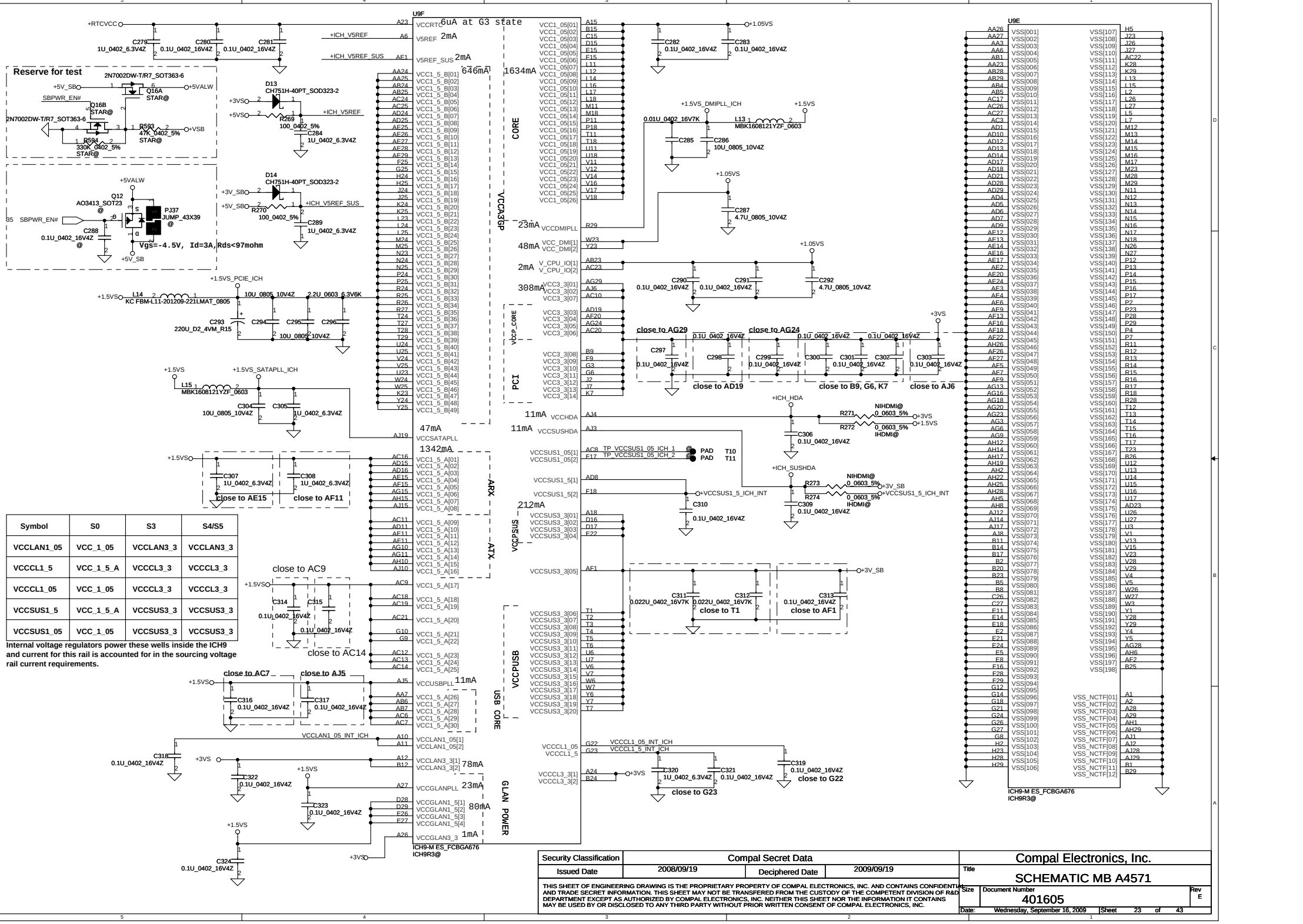

Symbol	S0	S3	S4/S5
VCCLAN1_05	VCC_1_05	VCCLAN3_3	VCCLAN3_3
VCCCL1_5	VCC_1_5_A	VCCCL3_3	VCCCL3_3
VCCCL1_05	VCC_1_05	VCCCL3_3	VCCCL3_3
VCCSUS1_5	VCC_1_5_A	VCCSUS3_3	VCCSUS3_3
VCCSUS1_05	VCC_1_05	VCCSUS3_3	VCCSUS3_3

Internal voltage regulators power these wells inside the ICH9 and current for this rail is accounted for in the sourcing voltage rail current requirements.

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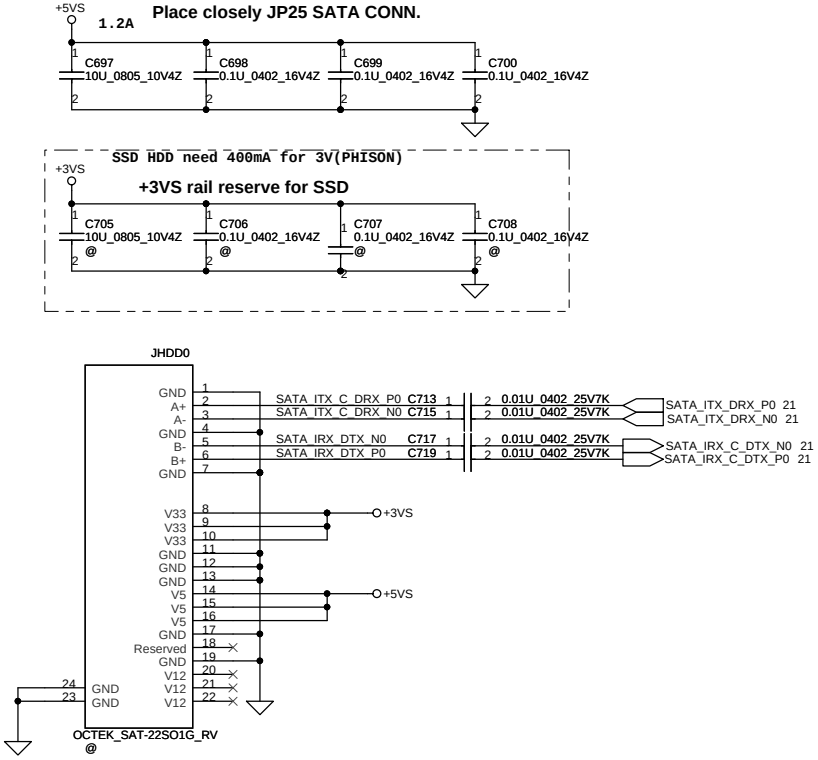
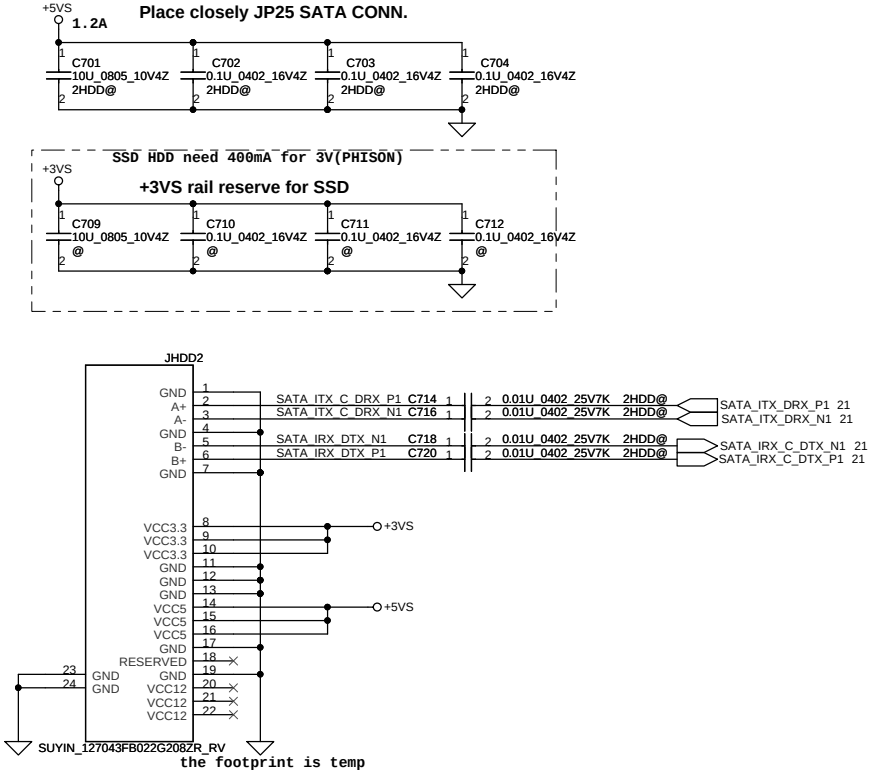
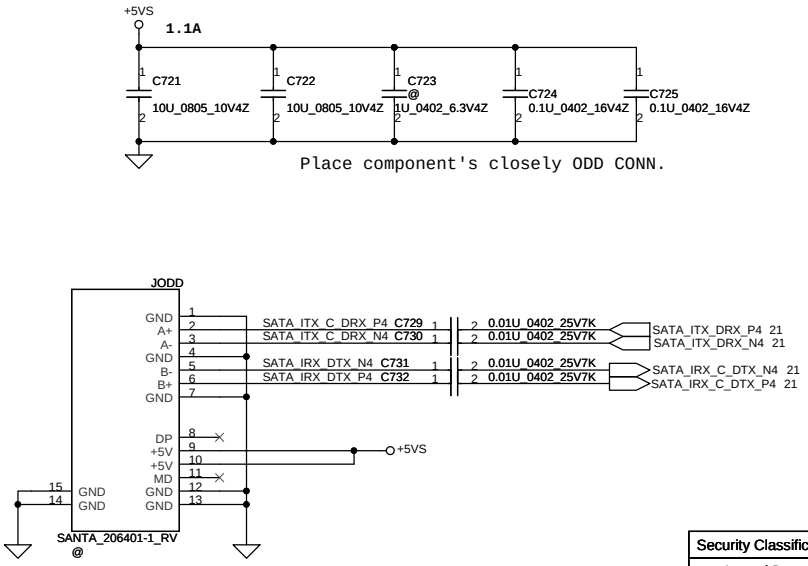
SATA HDD1 Conn.



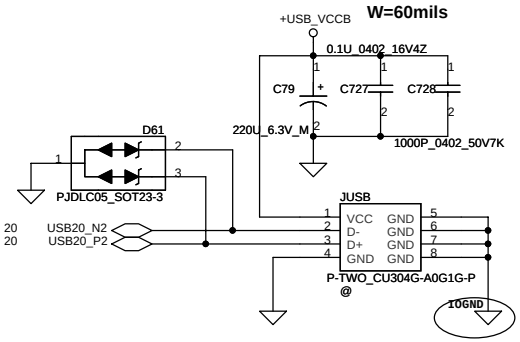
SATA HDD2 Conn.



SATA ODD Conn



USB Conn.



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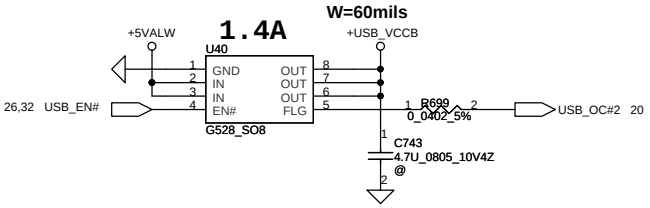
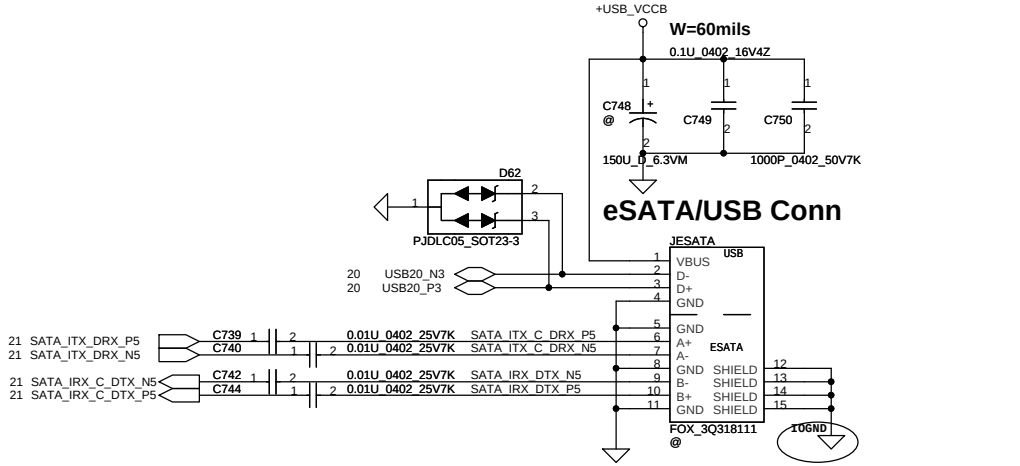
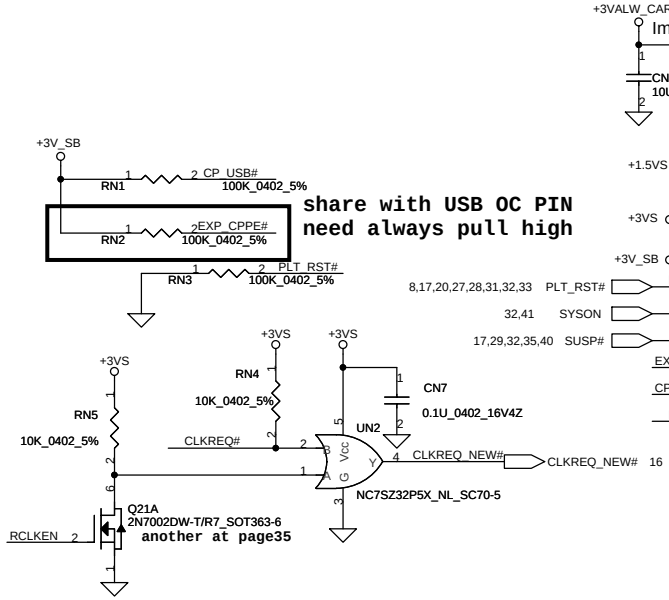
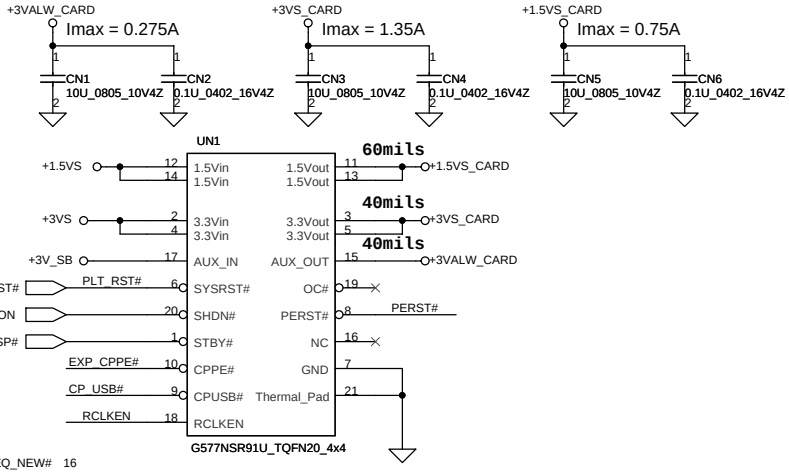
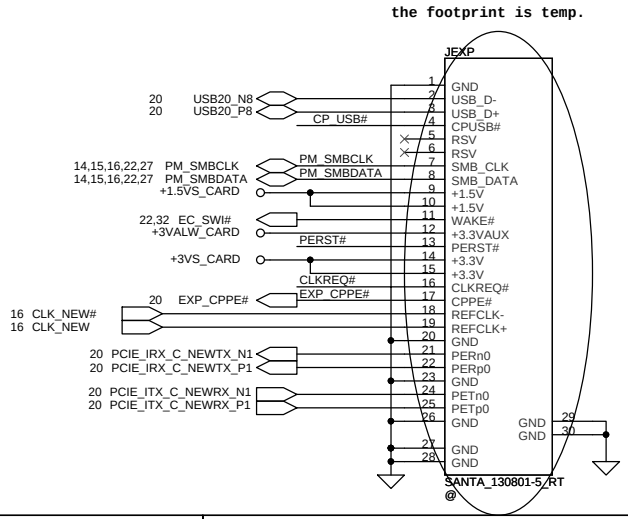
eSATA/USB











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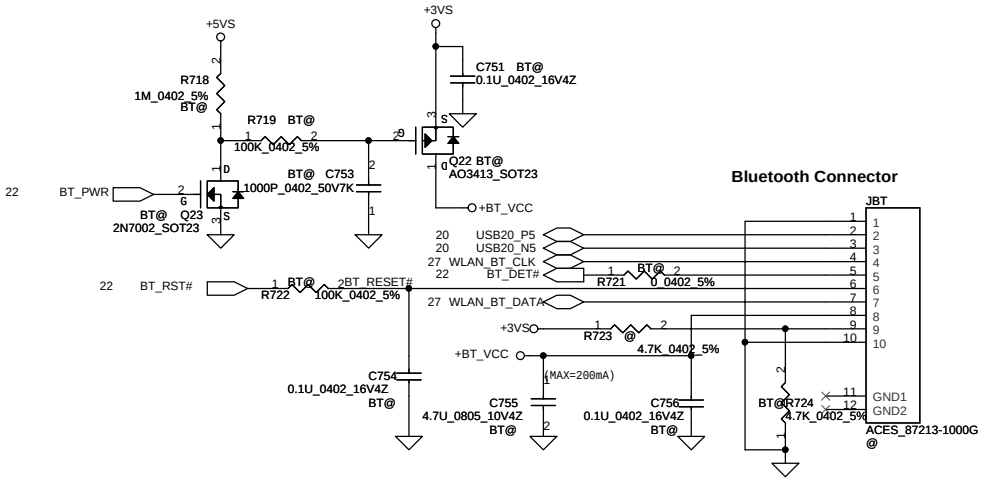
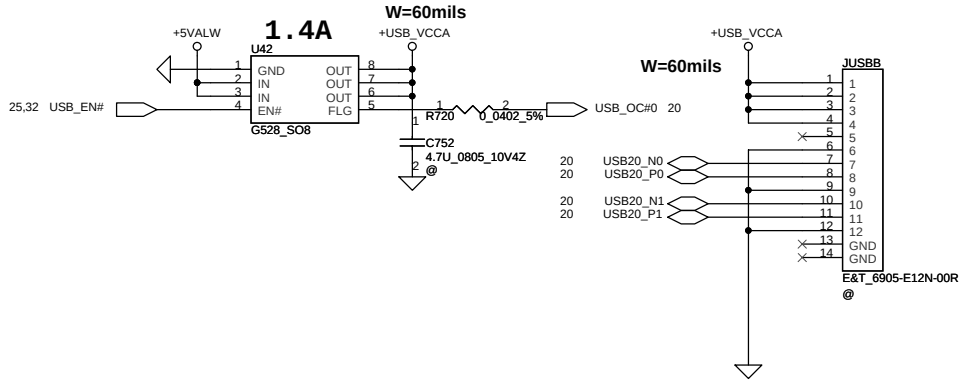
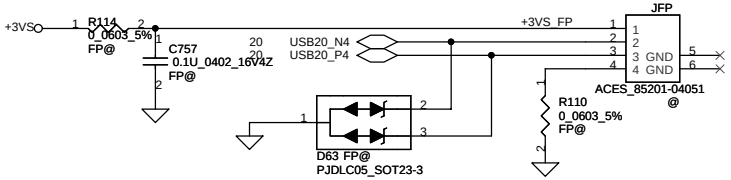
BlueTooth Interface



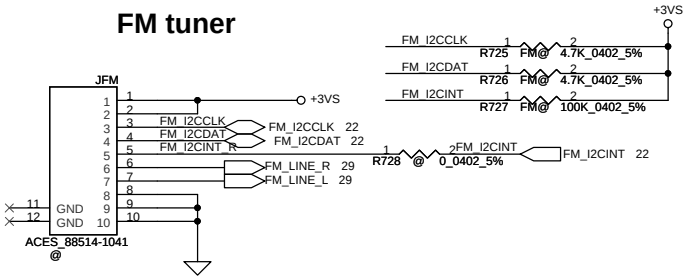
USB Board



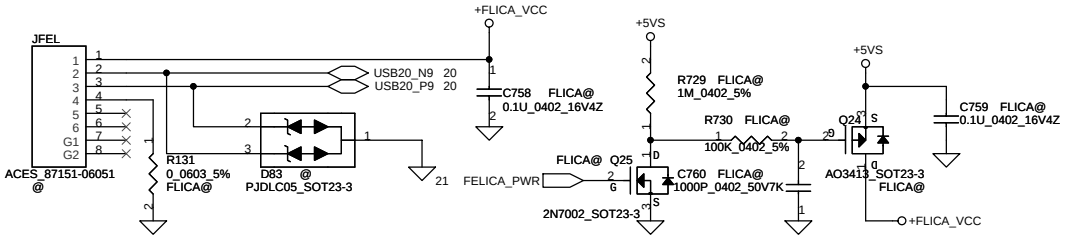
Finger printer



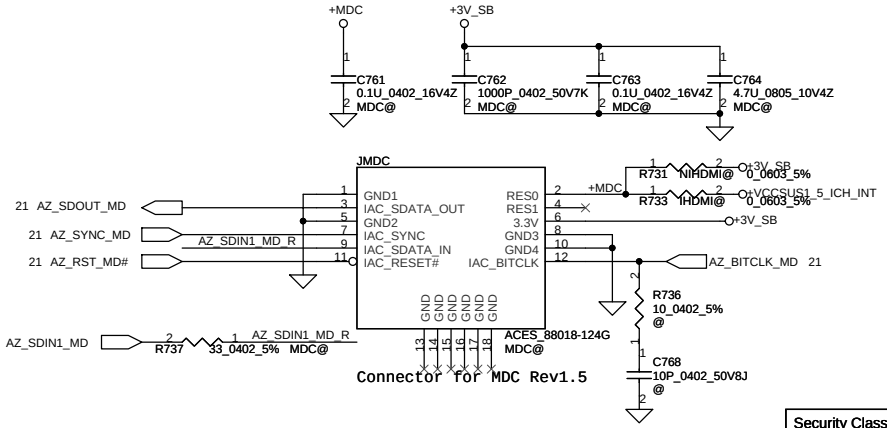
FM tuner



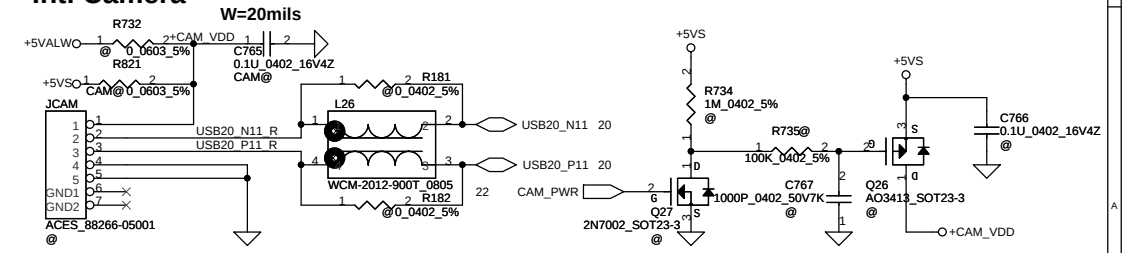
Felica



MDC 1.5 Conn.



Int. Camera



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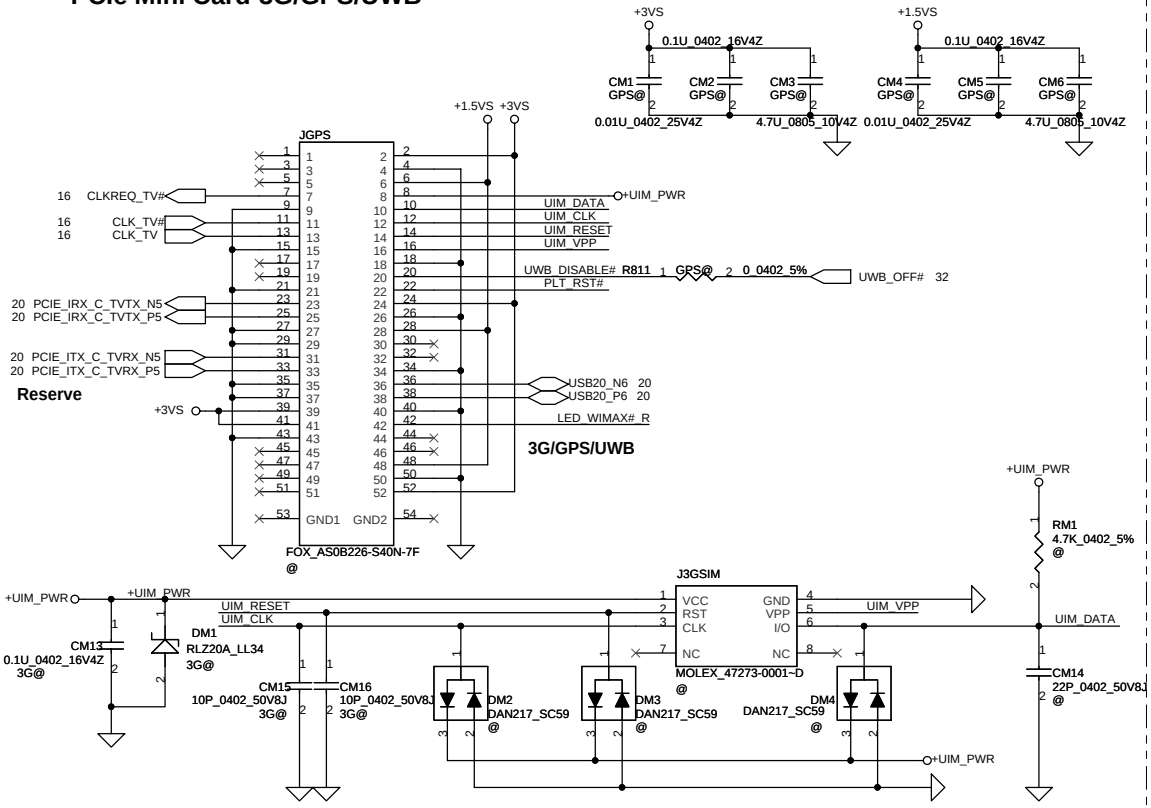
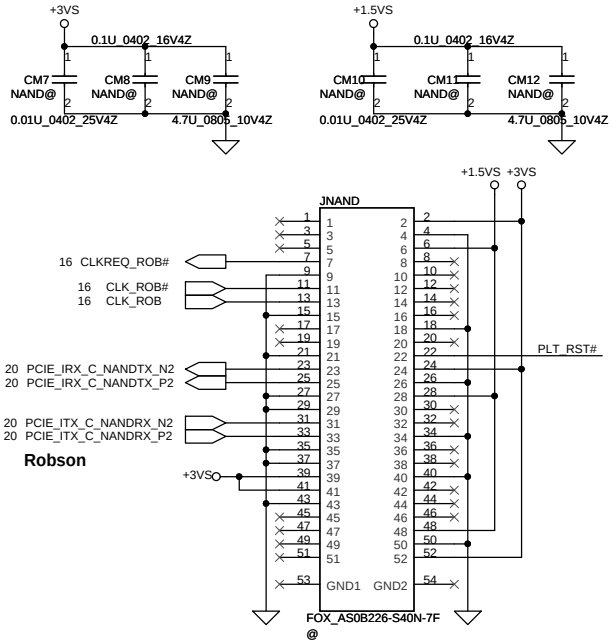
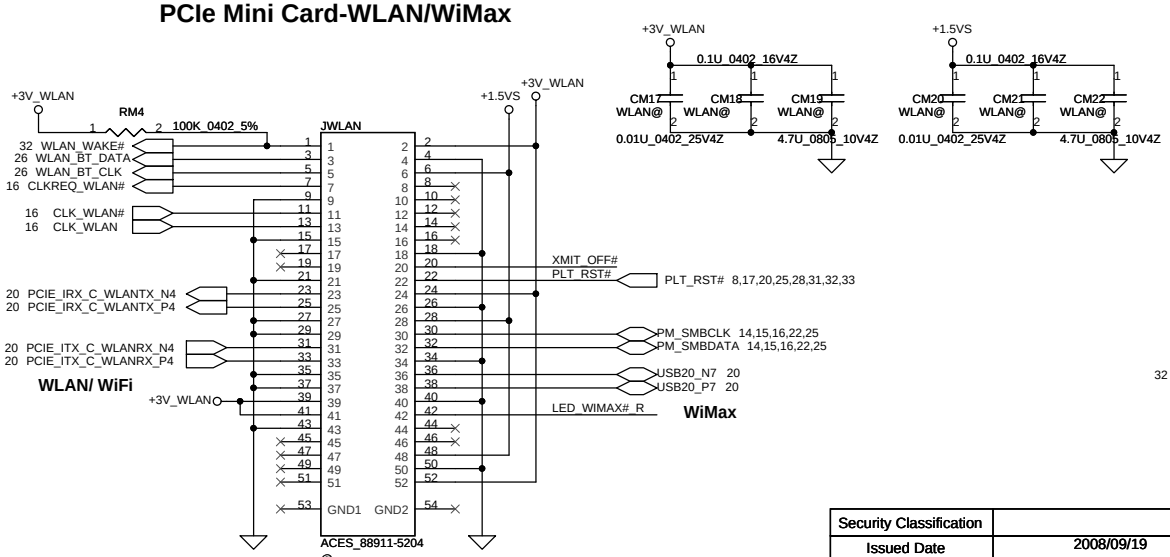
PCIe Mini Card-3G/GPS/UWB



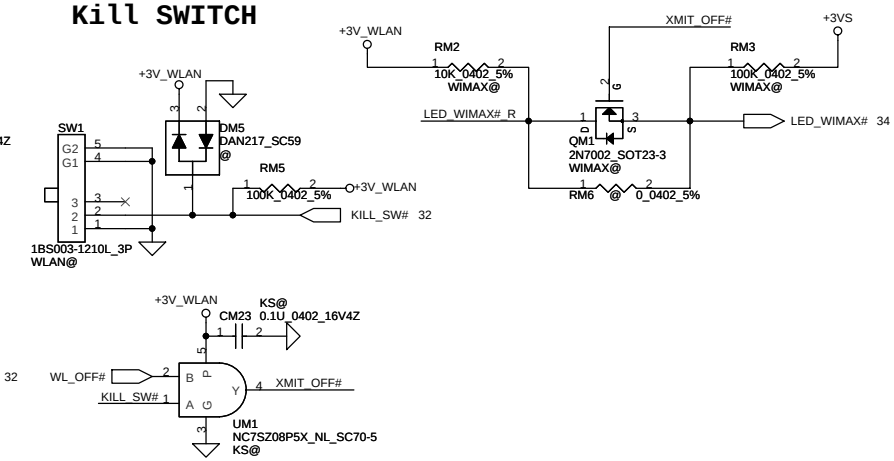
PCIe Mini Card-Robson



PCIe Mini Card-WLAN/WiMax



Kill SWITCH



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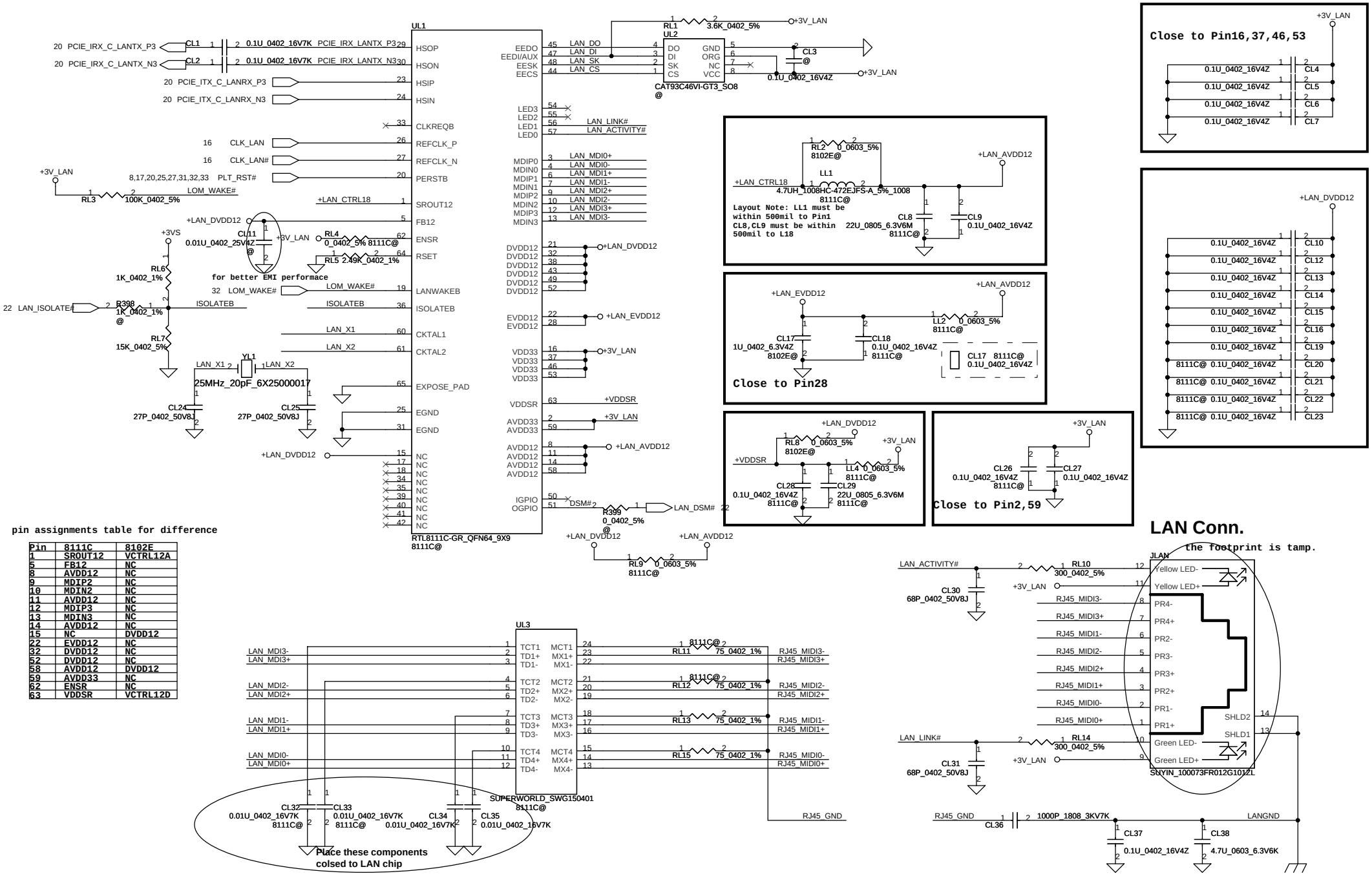

pin assignments table for difference

Pin	8111C	8102E
1	SROUT12	VCTRL12A
5	FB12	NC
8	AVDD12	NC
9	MDIP2	NC
10	MDIN2	NC
11	AVDD12	NC
12	MDIP3	NC
13	MDIN3	NC
14	AVDD12	NC
15	NC	DVDD12
22	EVDD12	NC
32	DVDD12	NC
52	DVDD12	NC
58	AVDD12	DVDD12
59	AVDD33	NC
62	ENSR	NC
63	VDDSR	VCTRL12D

LAN Conn.

the footprint is tamp.

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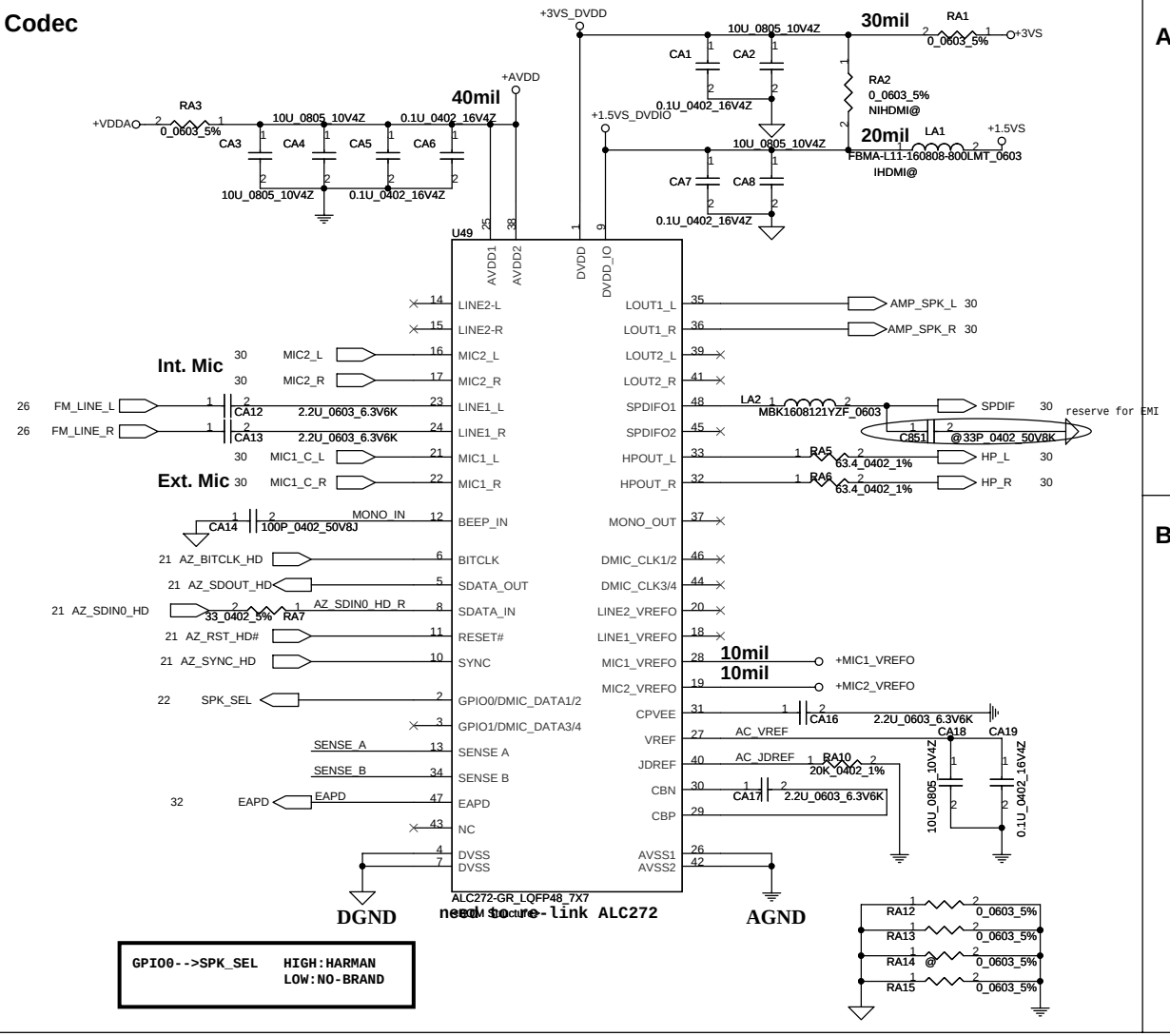
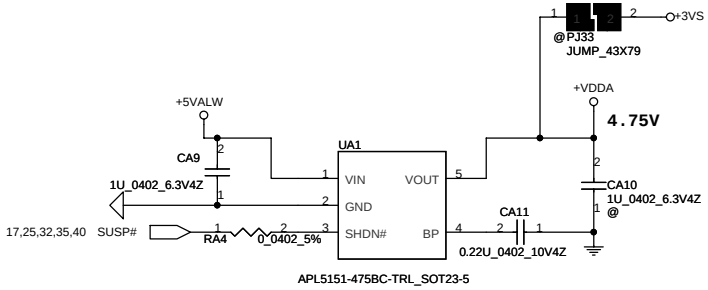
Codec



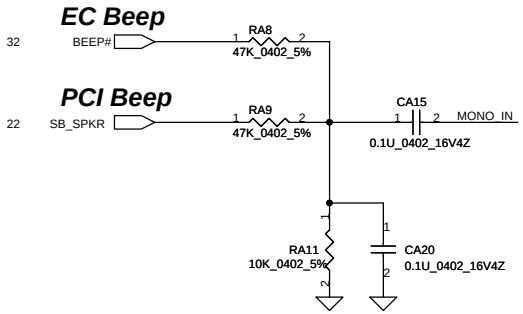
need to re-link ALC272

GPIO0-->SPK_SEL HIGH:HARMAN
LOW:NO-BRAND

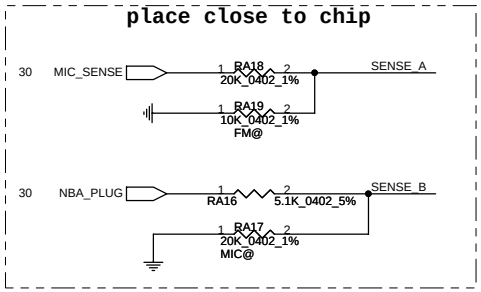
Audio regulator



Beep sound



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	FM tuner
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out



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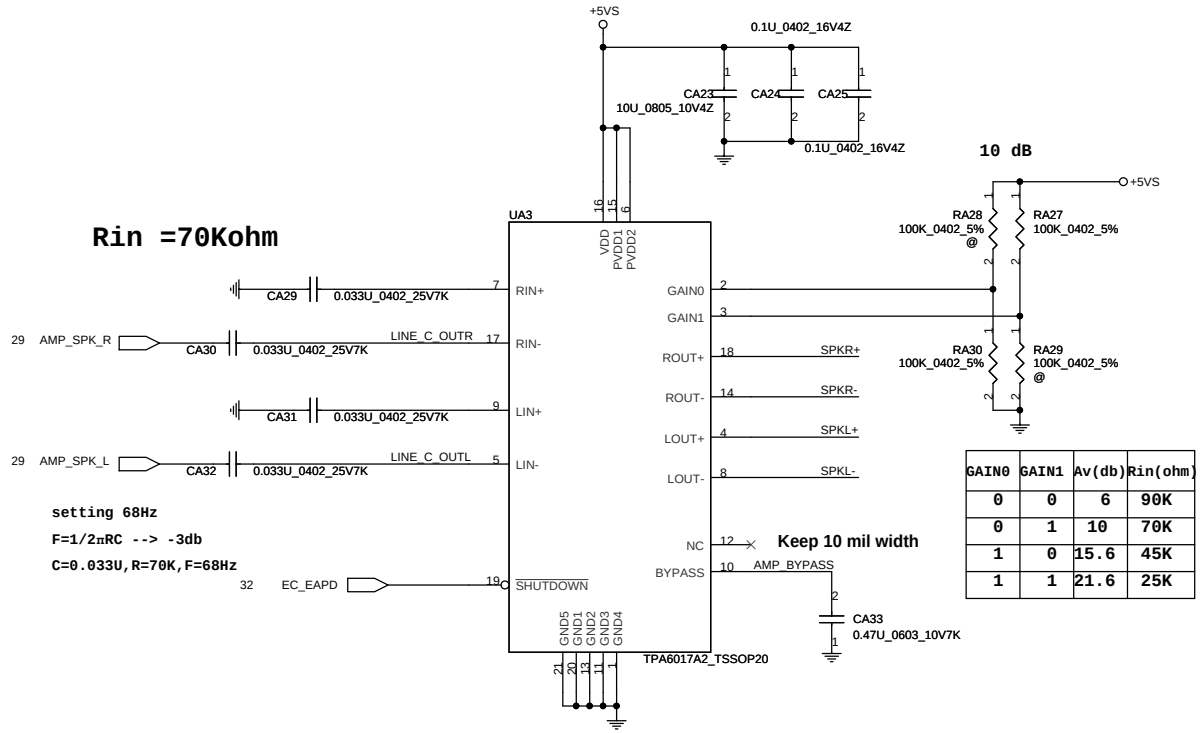
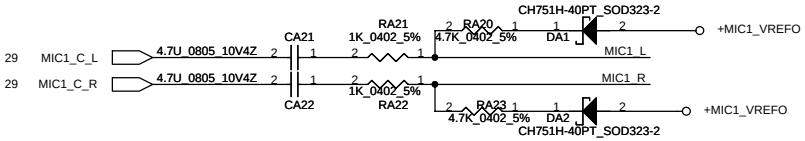
TPA6017 Medium Range Amplifier

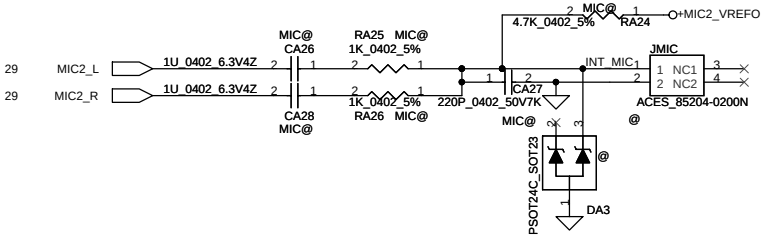


GAIN0	GAIN1	Av(db)	Rin(ohm)
0	0	6	90K
0	1	10	70K
1	0	15.6	45K
1	1	21.6	25K

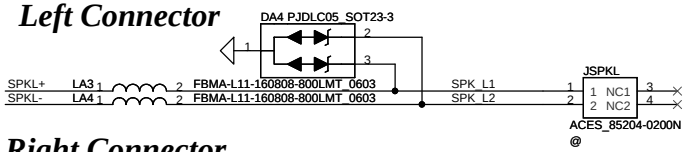
Ext. Mic



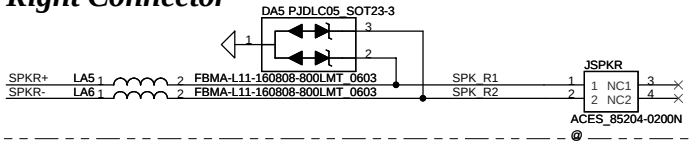
Int. Mic



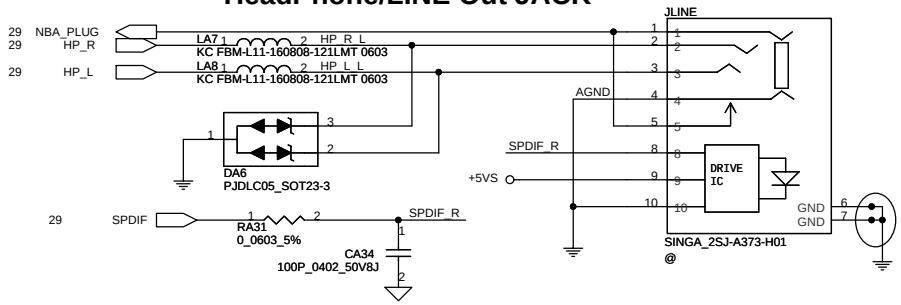
Left Connector



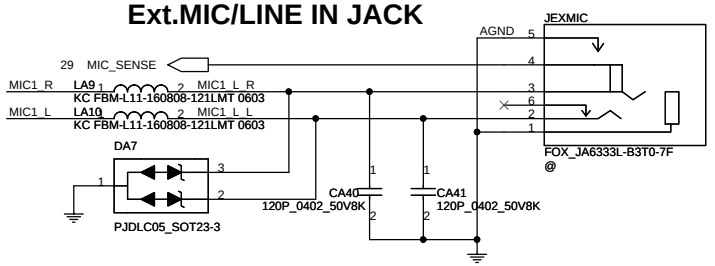
Right Connector



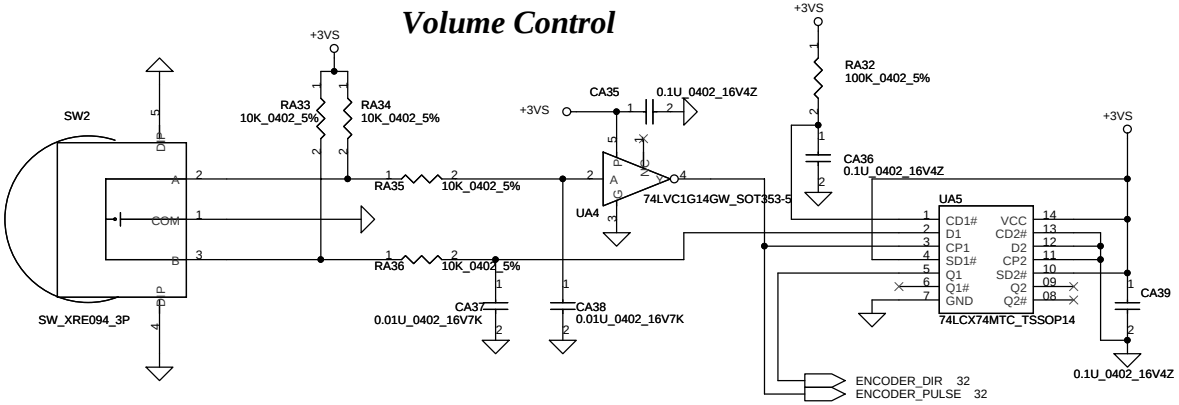
HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK



Volume Control



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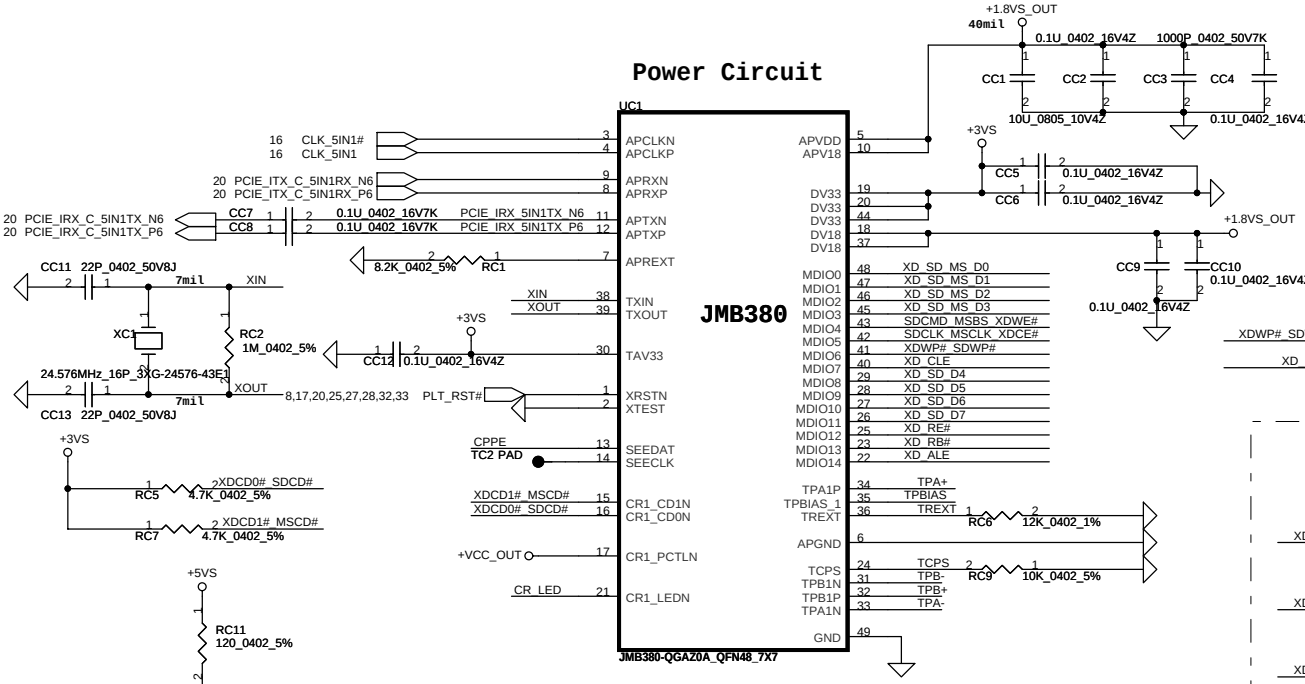
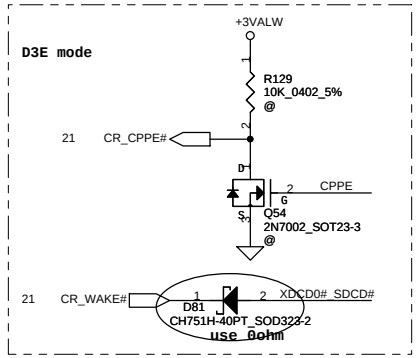
Power Circuit



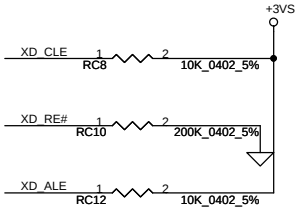
D3E mode

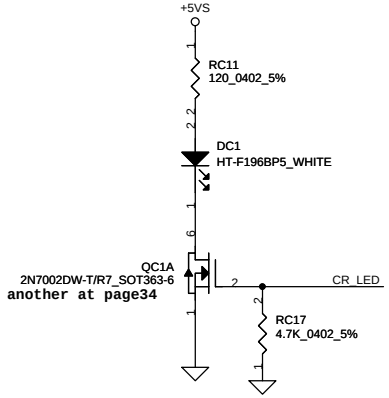


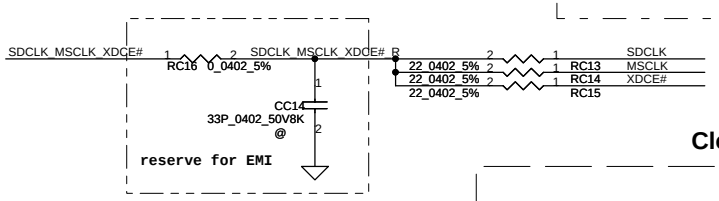
Strapping setting

Pin name	Description	
	High	low
MDIO7	on-board★	add-in card
MDIO12	+VCC_OUT high active	+VCC_OUT low active★
MDIO14	CR_LED high active★	CR_LED low active

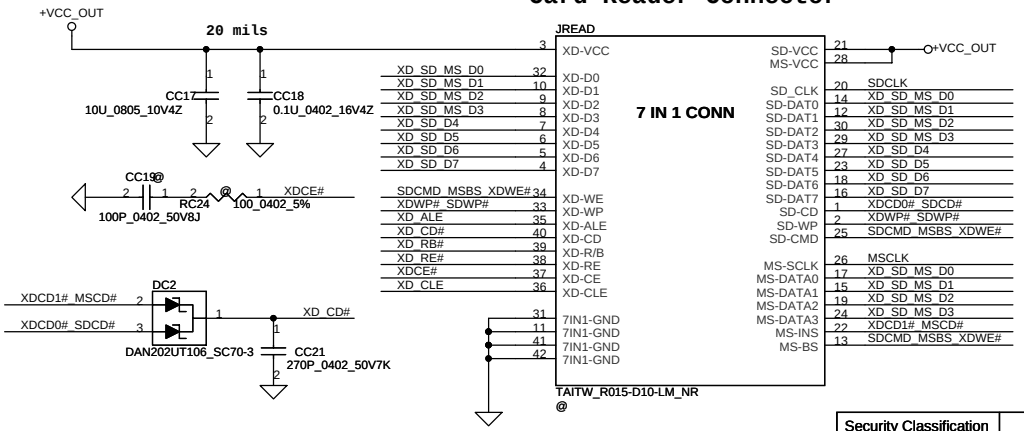
P.S CR1_PCTLN aslo can out 3V with 250mA for 5IN1 using.(MDIO12 can't be seted after MP IC)



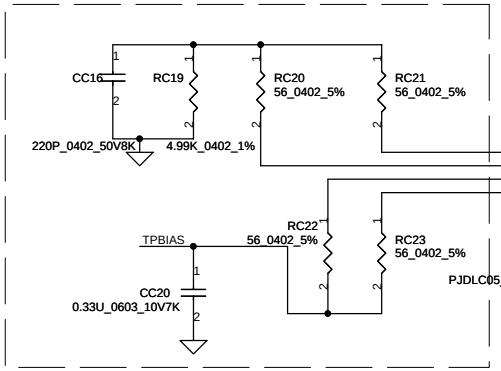




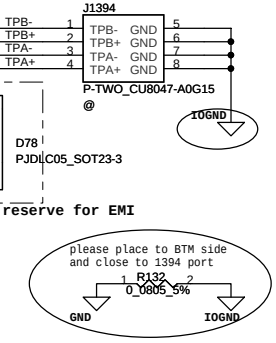
Card Reader Connector



Close to Chip



1394 Port



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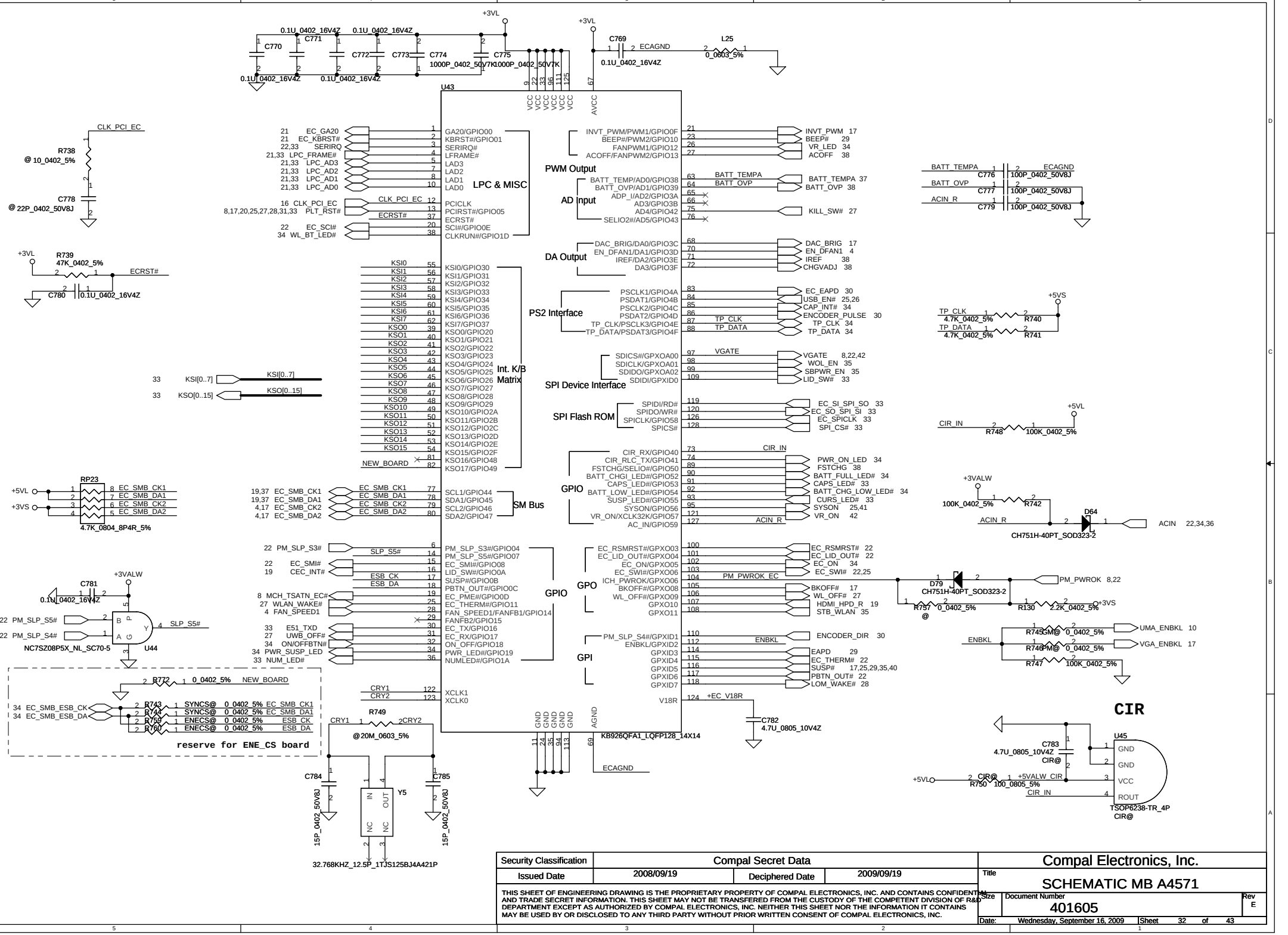
U43
KB926QFA1_LQFP128_14X14
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
reserve for ENE_CS board
CIR
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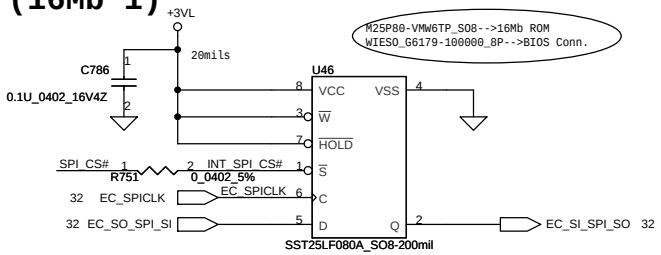
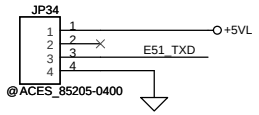
SPI Flash (16Mb*1)

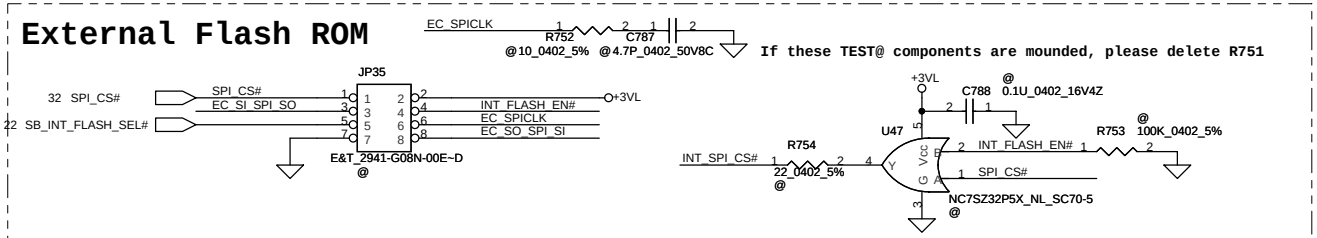


Please place the connector under DDR door

For EC

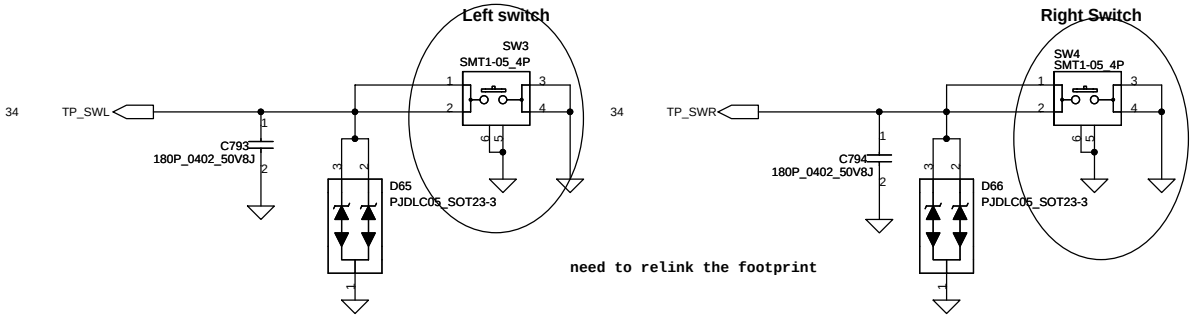


External Flash ROM

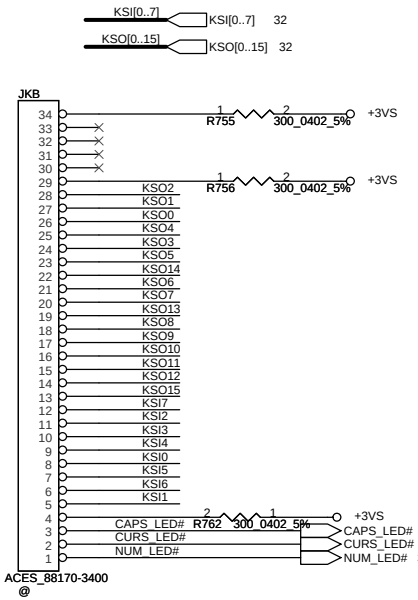


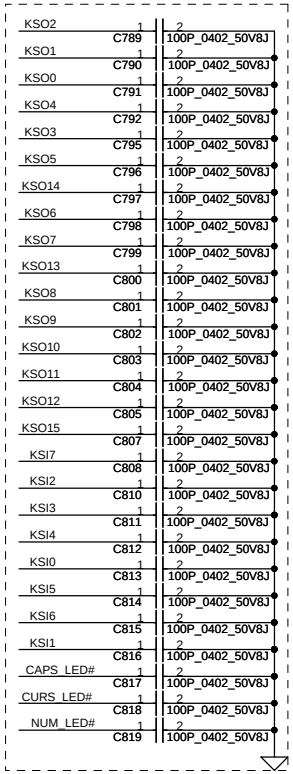
SB_INT_FLASH_SEL	H	L	L
SPI#	L	L	H
EXT_CS#	H	L	H
External Flash ROM	STOP	RUN	STOP

SB_INT_FLASH_SEL	H	L	L
INT_FLASH_EN#	L	H	H
SPI#	L	L	H
INT_SPI_CS#	L	H	H
External Flash ROM	RUN	STOP	STOP



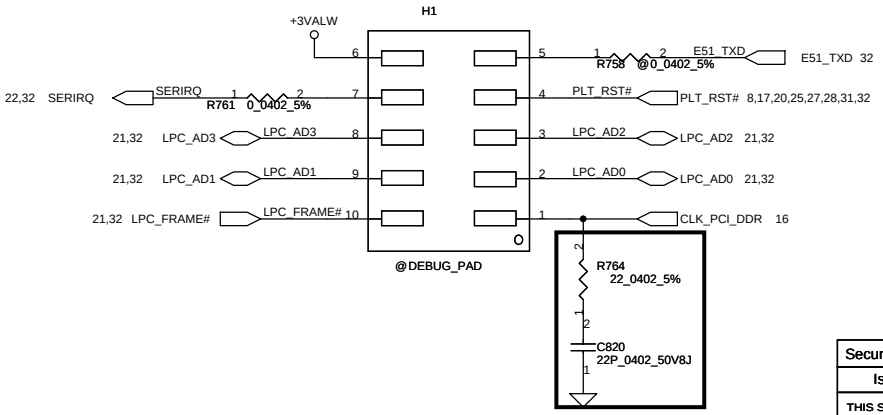
KEYBOARD CONN.



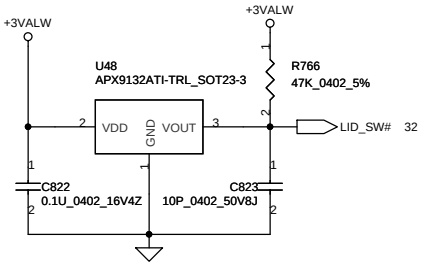


LPC Debug Port

Please place the PAD under DDR DIMM.



Lid SW



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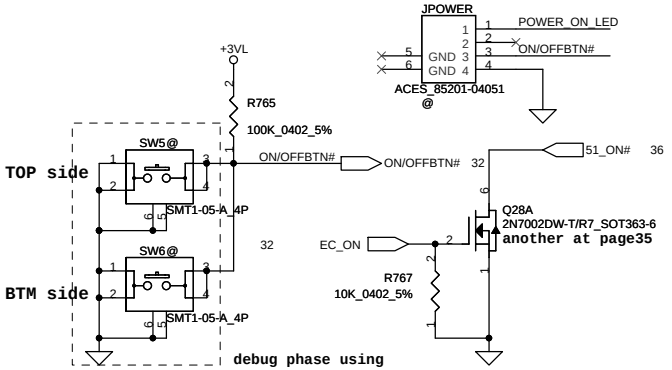
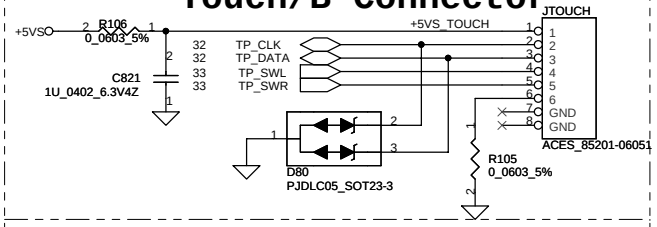
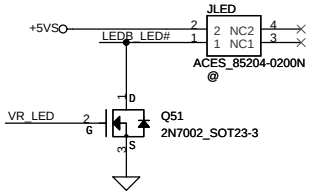
Power Button/ PWR/B



Touch/B Connector



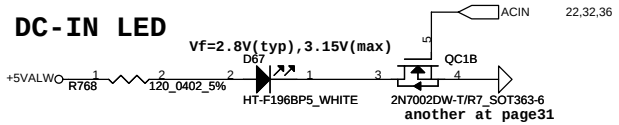
LED/B Connector



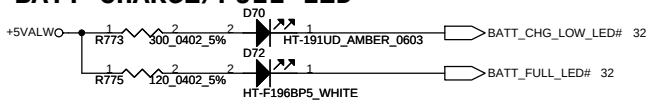
ISPD

PCB	ZZZ PCB ZKU LA-4571P REV4	LAN	UL1 8102E 8102E@		
NB_GL_R1	U3 CANTIGA GL40 A1 GMLR1@	NB_PM	U3 CANTIGA PM PMR3@	DC-IN	PJP1 PJP1 45@
NB_GL_R1	U9 ICH9-M ES ICH9R1@	NB_PM_R1	U3 CANTIGA PM PMR1@	NB_GL	U3 CANTIGA GL40 A1 GMLR3@
		NB_GM_R1	U3 CANTIGA GM45 GMR1@	Trans former	UL3 10/100M transformer 8102E@

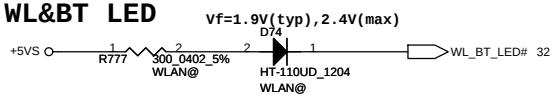
DC-IN LED



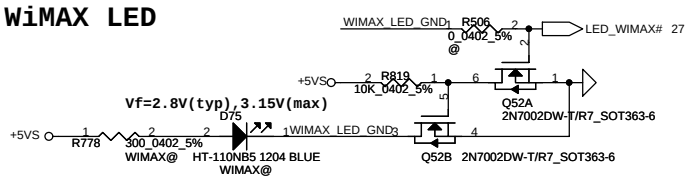
BATT CHARGE/FULL LED



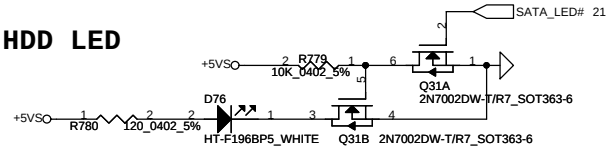
WL&BT LED



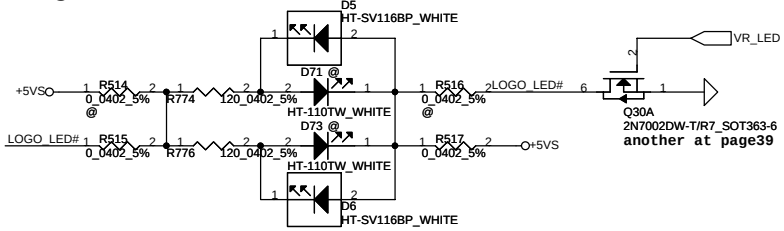
WiMAX LED



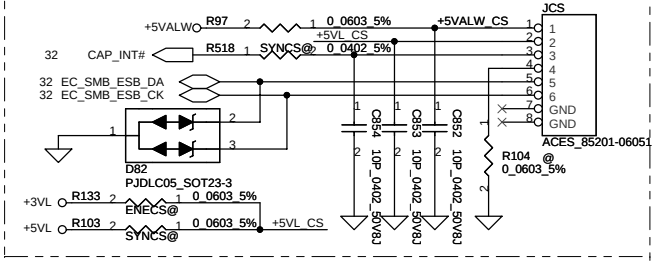
HDD LED



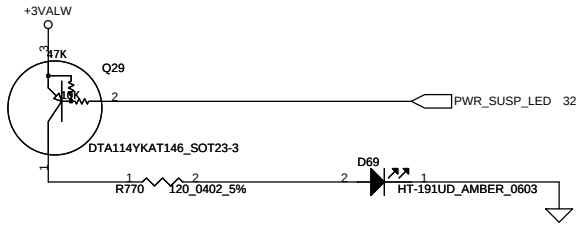
Logo LED



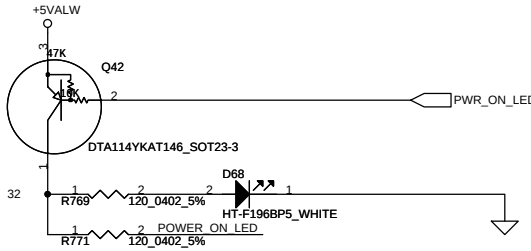
FUN/B Connector



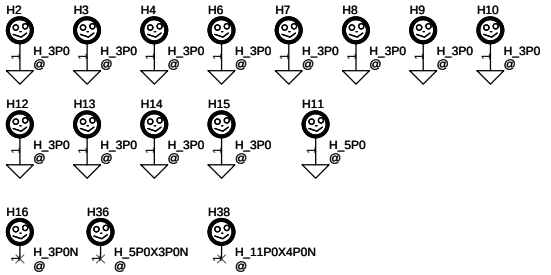
SUSPEND LED



POWER LED

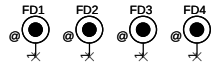


Screw Hole



MINI CARD-1	H32 H_3P8 H34 H_3P8	CPU	H20 H_3P7 H22 H_3P8 H19 H_3P8X4P8 H21 H_3P8X4P8		
MINI CARD-2	H28 H_3P8 H31 H_3P8	VGA	H25 H_4P0 H26 H_4P0 H30 H_4P0		
MINI CARD-3	H29 H_3P8 H24 H_3P8	MDC	H27 H_1P2 H33 H_1P2		

PCB Fedical Mark PAD



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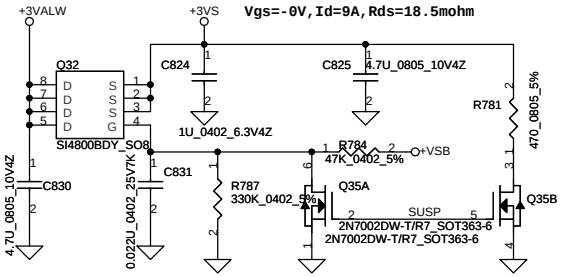
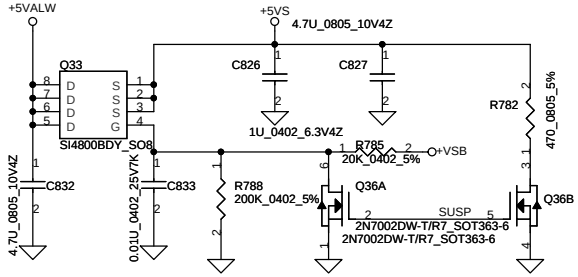
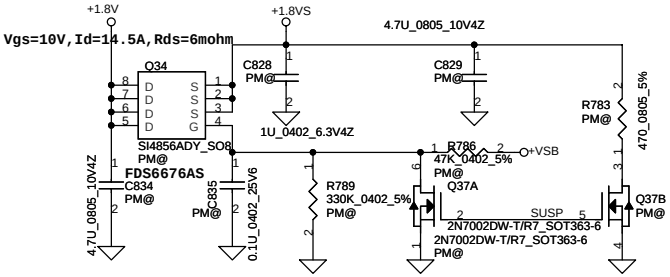
+3VALW TO +3VS



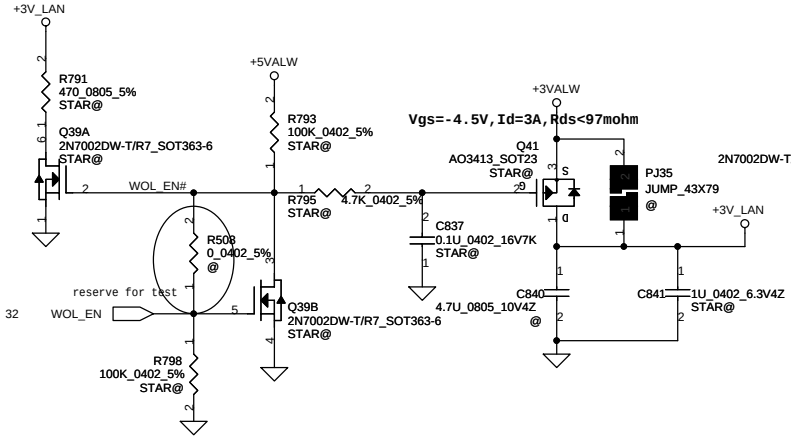
+5VALW TO +5VS



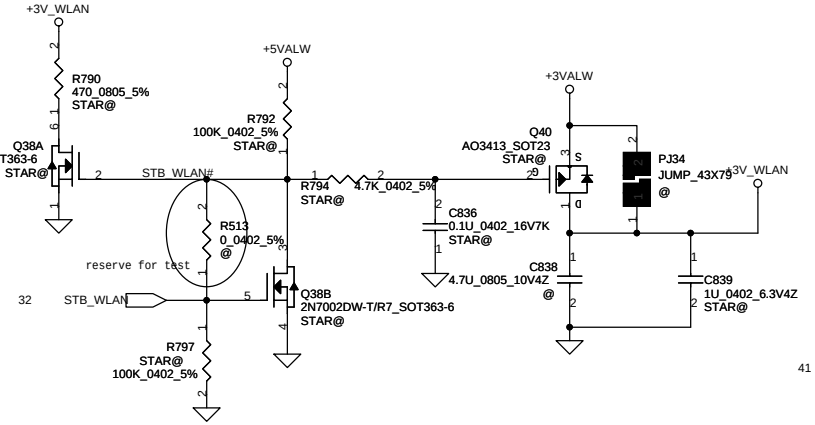
+1.8V to +1.8VS

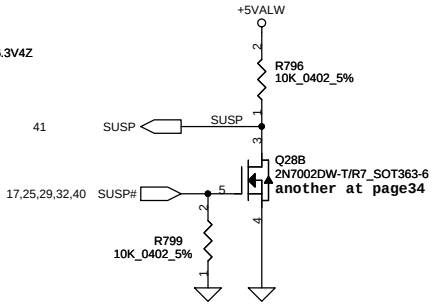


+3VALW TO +3V_LAN

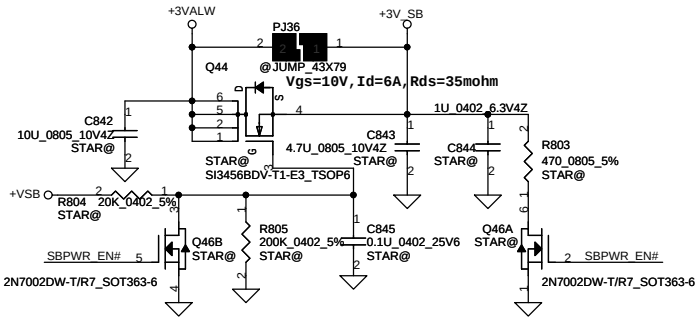


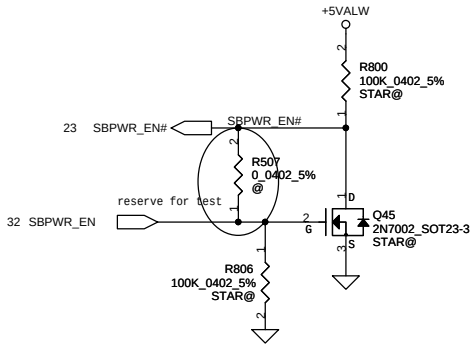
+3VALW TO +3V_WLAN

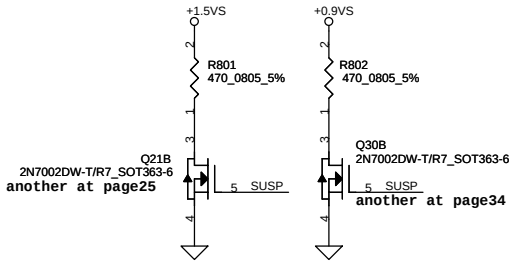




+3VALW TO +3V_SB







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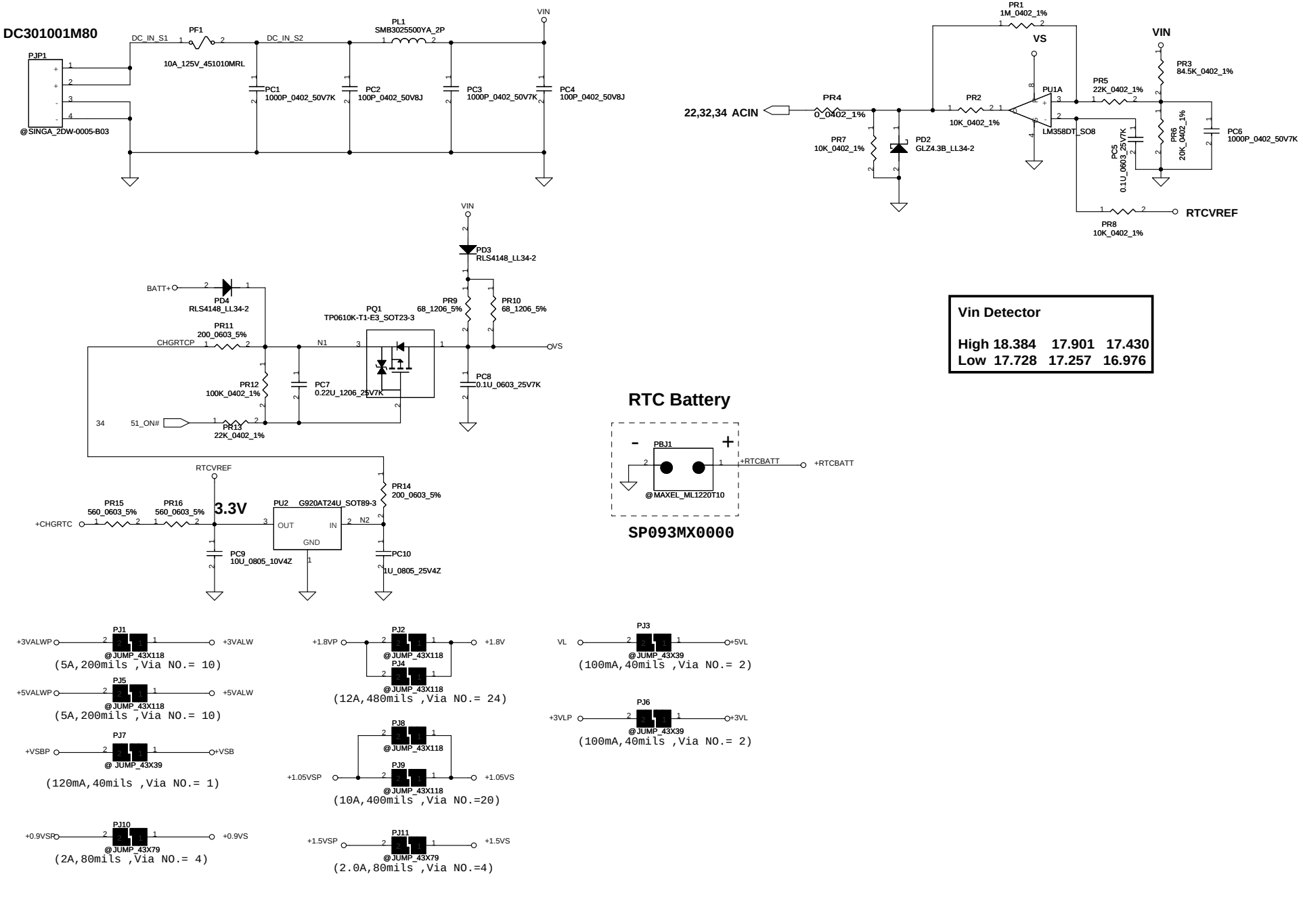

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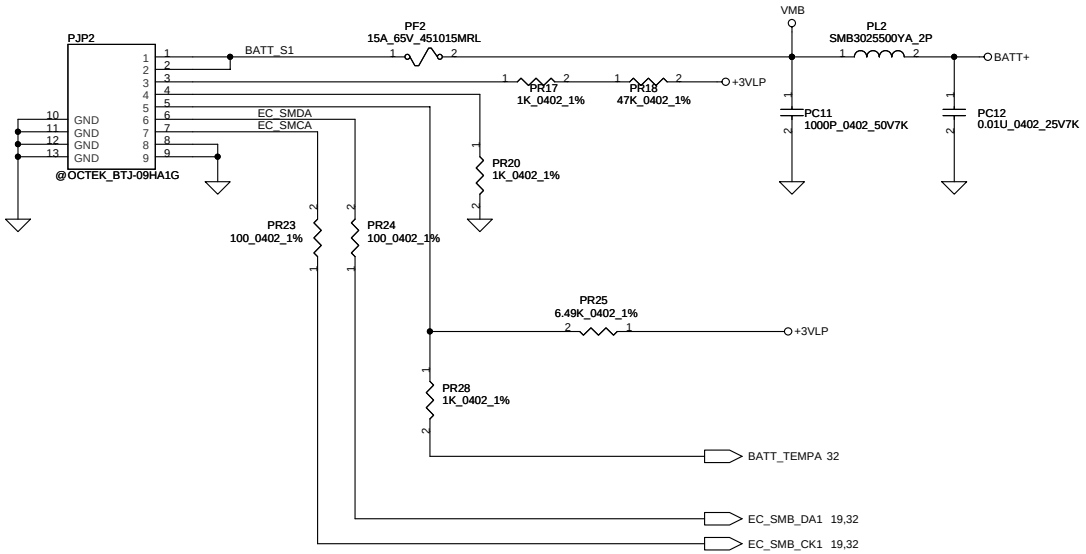
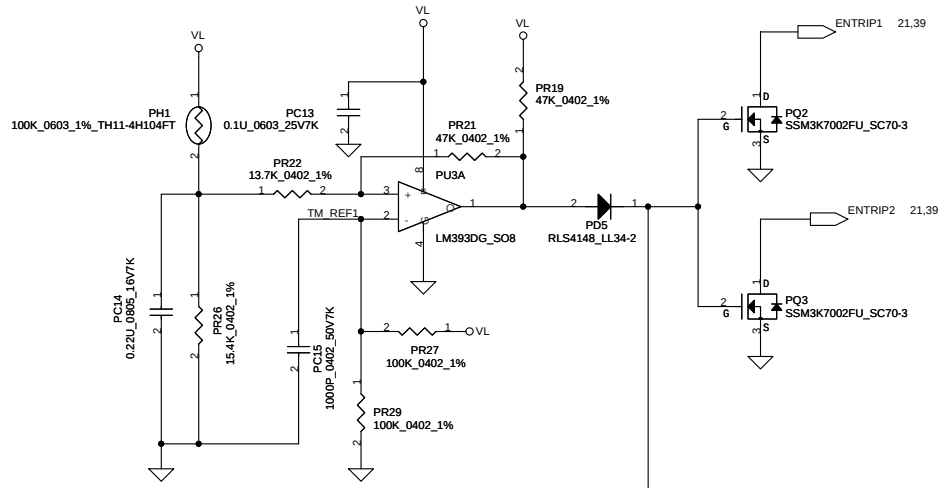
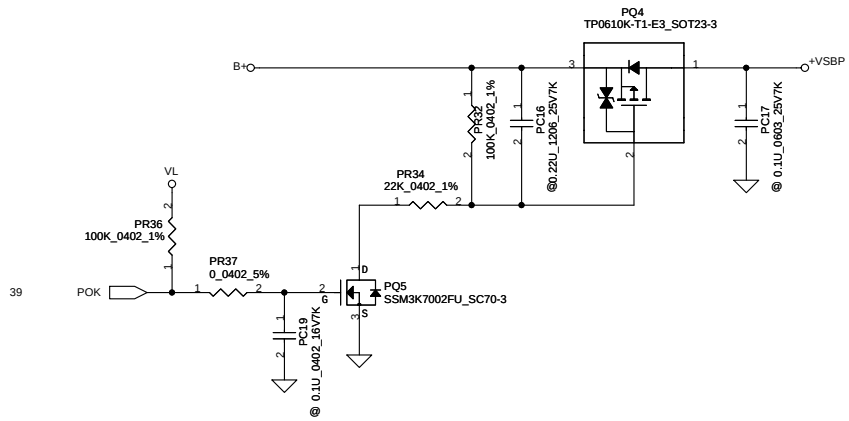
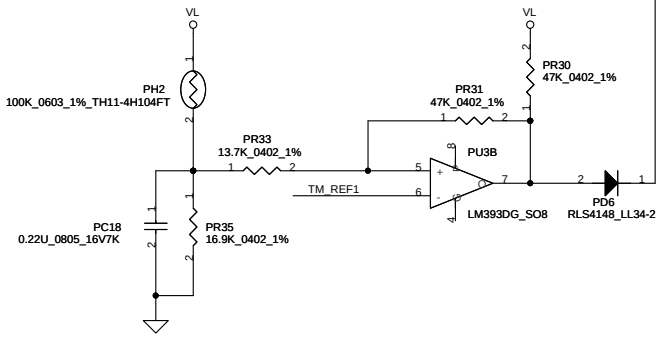
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C





PH2 near main Battery CONN :
BAT. thermal protection at 90 degree C
Recovery at 53 degree C





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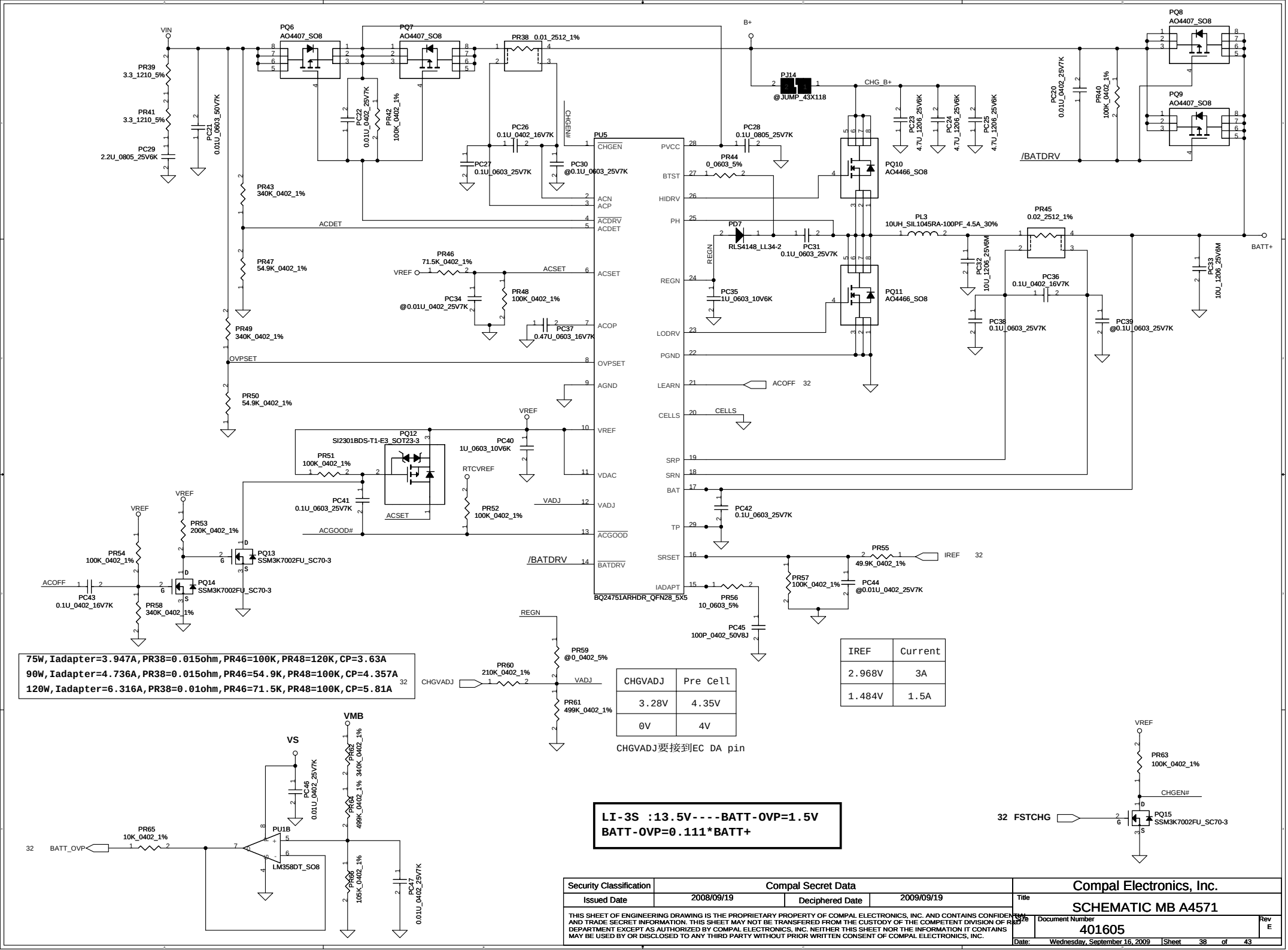

IREF	Current
2.968V	3A
1.484V	1.5A

CHGVADJ	Pre Cell
3.28V	4.35V
0V	4V

CHGVADJ要接到EC DA pin

75W,Iadapter=3.947A,PR38=0.015ohm,PR46=100K,PR48=120K,CP=3.63A
90W,Iadapter=4.736A,PR38=0.015ohm,PR46=54.9K,PR48=100K,CP=4.357A
120W,Iadapter=6.316A,PR38=0.01ohm,PR46=71.5K,PR48=100K,CP=5.81A

LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.111*BATT+

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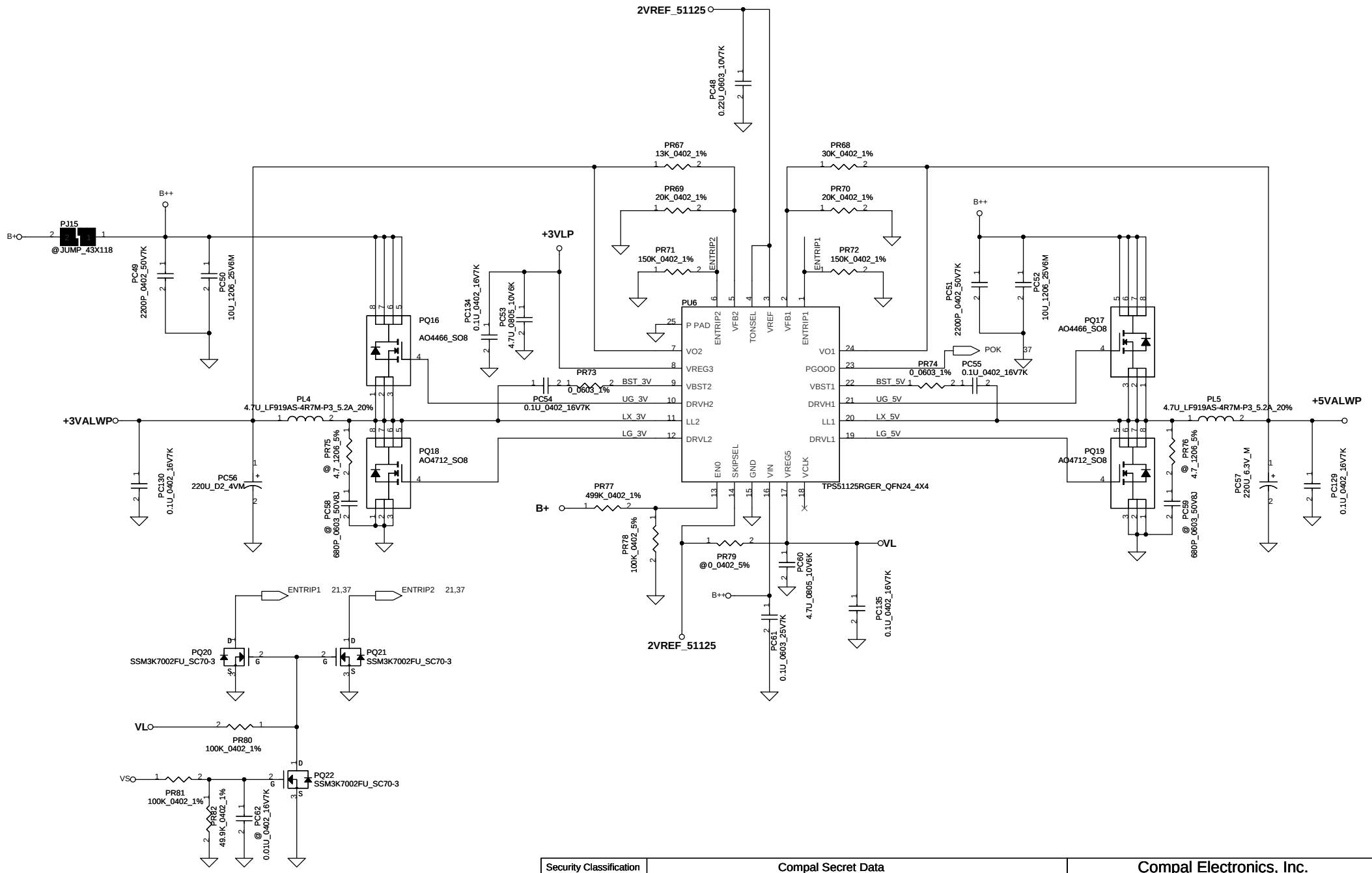

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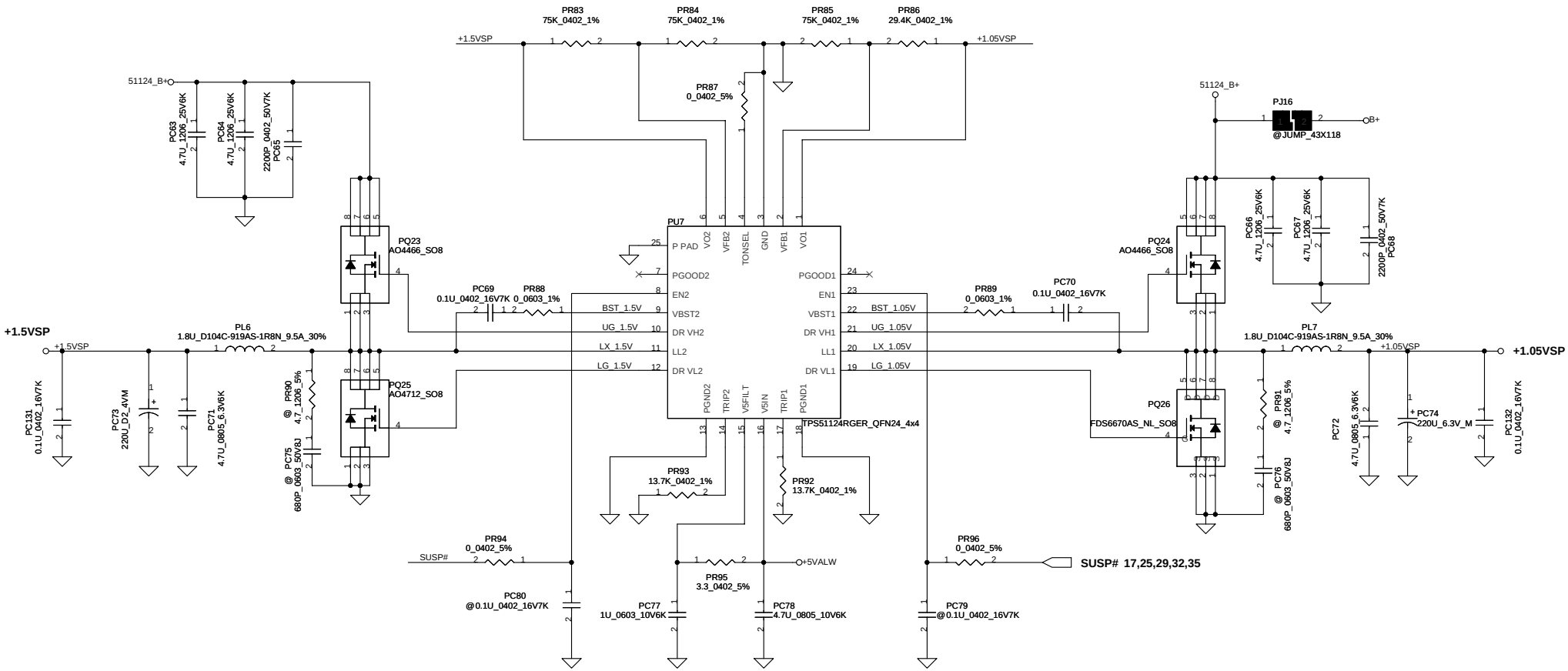

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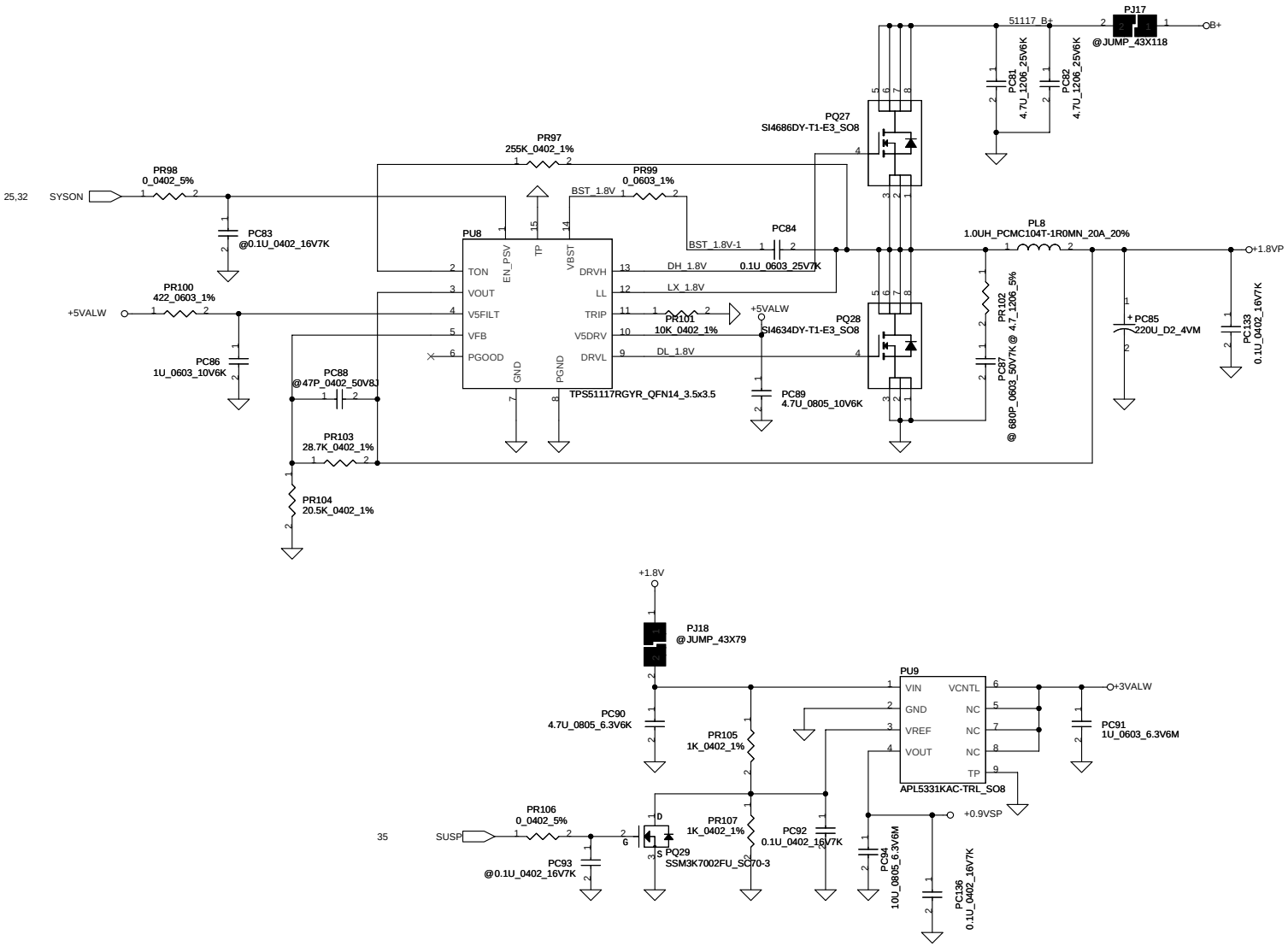

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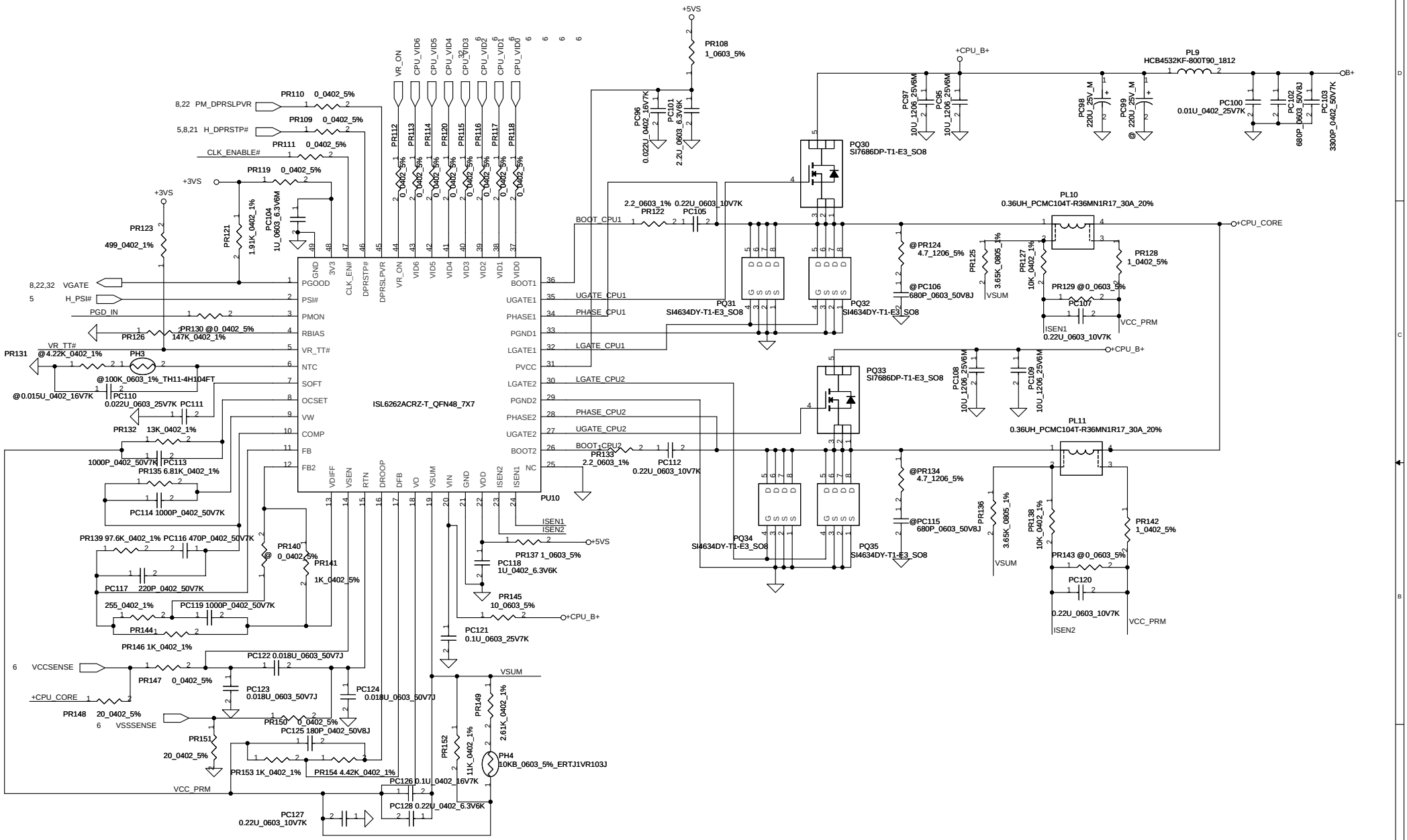

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PIR (Product Improve Record)

KTKAA LA-4571P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	6/18	34	change Q29.3 to pull up with +3VALW and R770, R720 to 120ohm	to solve suspend led issue.
2	6/18	27	exchange J3GSIM pin2 and pin3	link to error pin definition.
3	6/18	27	change CM15,CM16 to 10P and un-mount RM1 and Cm14.	for customer request.
4	6/24	18	add C849, C850 for EMI request.	for EMI request.
5	6/24	11	add 220u to +1.8V with C78.	reserve for test.
6	6/24	24	add 220u to +USB_VCCB with C79.	reserve for test.
7	6/24	29	add C851 to SPDIF.	for EMI request.
8	6/24	27	link JNAND.39,41 to +3VS,and 39,43 pin link to GND	this is standard pin define
9	6/25	19	change U37 power from +HDMI_5V_OUT to +5VL	for customer request and follow Toshiba design guide with CEC.
10	6/25	27	reserve some circuit for change Mini card 1 and 2	reserve for GPS issue
11	6/26	30	change CA29~CA32 from 0.47u to 0.033u	set high pass frequency to 68Hz

REVISION CHANGE: 0.2 TO 0.3

1	7/19	34	add R506 and Q52 for Wimax LED control	reserve Wimax LED control to avoid MINI card module damage.
2	7/19	35	change R788,R805 from 330K to 200K	reduce the voltage on the Vgs of MOS as AC mode.
3	7/19	35	mount R507 and un-mount Q45,R800,R806	use another control for +5V_SB
4	7/19	23	mount Q16,R593,R594 and un-mount Q12	use another control for +5V_SB
5	7/22	35	add R508,R513	reserve for tset
5	7/22	31	add D77,D78 on 1394 port	reserve for EMI request
6	7/22	26	exchange JFEL all pin	to solve the cable reverse issue
7	7/24	3	delete XDP conn and related compoments	to improve ESD issue
8	7/24	34	add Q42 and link to EC U43.72	to solve the power on LED need 2.1S will be light after press power button
9	7/24	31	add Q54,R129,R220,R222,D81 and link to U9.B10,U9.AE8	reserve D3E mode as JMB380
10	7/24	28	add R398,R399,R264 for LAN and link to U9.AH24,U9.C21	reserve LAN saving mode
11	7/24	32	add R757,R130,D79	to avoid glitch issue when KB926 power on
12	7/24	34	add D80	reserve for ESD request
13	7/24	26	add L26,R181,R182 on camera conn.	reserve for EMI request
14	7/24	34	add R514~R517,D5,D6	reserve for LED type option
15	7/25	34	add R97,R103,R518,C852~C854,D82 on CS/B conn	reserve for ESD request
16	7/25	34	add R105,R106 on Touch/B conn	reserve for ESD request
17	7/25	26	add R110,R114 on Finger/B conn	reserve for ESD request
18	7/25	26	add R131,D83 on Felica conn	reserve for ESD request
19	7/25	28	change LAN footprint to "TYCO_2068888-1_12P-T"	for ME team request
20	7/25	31	add R132 and separate support pin of 1394,USB,eSATA to IOGND	for ESD request
21	7/25	18	change C680~C685 to 2.2pF	for customer request
22	7/25	26	change R722 form 0ohm to 100Kohm	it's to let the power on first then reset# will be high later to meet spec
23	7/25	34	mount D5,D6,R515,R517 and un-mount D71,D73,R514,R516	change logo LED to high illumination

REVISION CHANGE: 0.3 TO 1.0

1	8/10	27	exchange QM1 Pin2,3	
2	8/10	27	add R820 and link to both JGPS.16 and J3GSIM.5	reserve 3G SMI card VPP function.
3	8/10	27	link JGPS.24 to +3V_WLAN,link JNAND.24 to +3VS	add more power pin for standard definition
4	8/10	19	change D8,D53 from RB491D to RB161M	reduce the forward voltage for HDMI logo Spec.
5	8/10	30	change CA29~CA32 form 0603 type to 0402	no 0603 type part in Compal Hub and improve the audio perfermance
6	8/10	34	change H19,H21 from 4P8X3P8 to 3P8X4P8	for Layout team request
7	8/10	26	add R821 and link +5VS to +CAM_VDD	change camera power to +5VS for energy star
8	8/11	11	change C72,C73,C78,C79,C146 Footprint to C_PXC6P3VC220MF60	for DFX request to easy check when SMT
9	8/11	34	delete R772	2008 no amber LED on power button
10	8/18	4	change R4~R7 from 49.9ohm to 54.9ohm	follow Intel design guide when no XDP schematic
11	8/18	19	Change RV67 from 10K to 2.2Kohm	to solve measure HDMI logo can't be detected with test implement
12	8/18	19	use common choke(L9~L12) to replace 0ohm	solve EMI issue
13	8/18	18	change L18~L20 to high speed bead	to solve the word is blurred when CRT mode
14	8/18	21	mount EMI SSIC and related conpomemts for Bit_CLK	solve EMI issue
15	8/18	33	mount C793,C794	for EMI request
16	8/18	34	change C831 from 0.01u to 0.022u	to solve VGA/B external thermal sensor can't normal work when VGA chip is very high temp.
17	8/31	31	change D81 to 0805_0	enable D3E mode
18	8/31	32	change R130 form 10K to 2.2K	expand PM_PWROK voltage from 2.4V to 3.05V
19	9/5	30	mount CA40 and CA41 to 120P	for EMI request
20	9/5	8	change R62 BOM config from GM@ to IHDMI@	set right strap pin when no IHDMI SKU
21	9/8	18	change R674 from 10K to 0ohm	solve some CRT device will appear most resolution when CRT only mode

REVISION CHANGE: 1.0 TO 2.0

1	9/19	27	change JGPS power from +3V_WLAN to +3VS	Solve GPS disappear when link 850Mhz only
2.	9/19	N/A	change PCB from 6 layer to 8 layer	imporve EMI and slove assembly procedure not easy issue

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