

Compal Confidential

JAQ10 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRIII + ICH9M

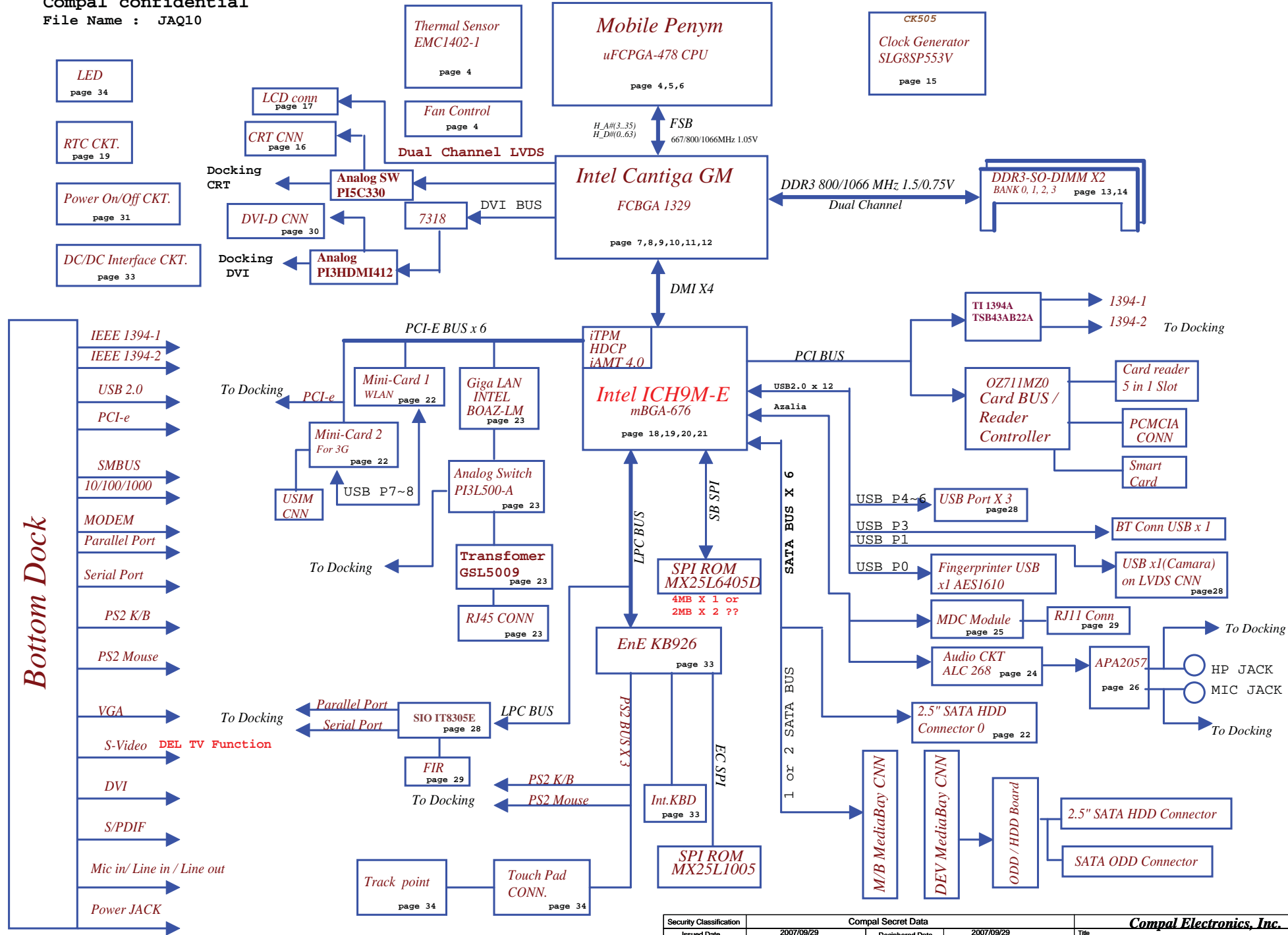
2008-04-21

REV:1.0

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				Date:	Friday, July 04, 2008	Sheet 1 of 44

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Date:	Friday, July 04, 2008	Sheet	2	of 44

Voltage Rails

Power Plane	Description	S1	S3/M1	S5/M1
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75VS power rail for DDR3 terminator	ON	OFF/ON	OFF/ON
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.05VM	1.05VM switched power rail	ON	OFF/ON	OFF/ON
+1.5V	1.5V power rail for HDA	ON	ON	OFF/ON
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	OFF/ON	OFF/ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
1394 TI	AD21	3	PIRQ-F
PCMCIA + Card Reader + Small Card	AD22	2	PIRQ-E

External PCI-e Devices

Device	PORT NO.	Interrupts
MINI CARD1 WLAN	P1	??
MINI CARD2 3G	P2	??
DOCKING PCI-E	P5	??
INTEL GIGA LAN	P6	??

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADM1032	1001 100X b
		GMT G781-1	1001 101X b

EC SM Bus2 address

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS365)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
HDMI Analog S/W	1100 000Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

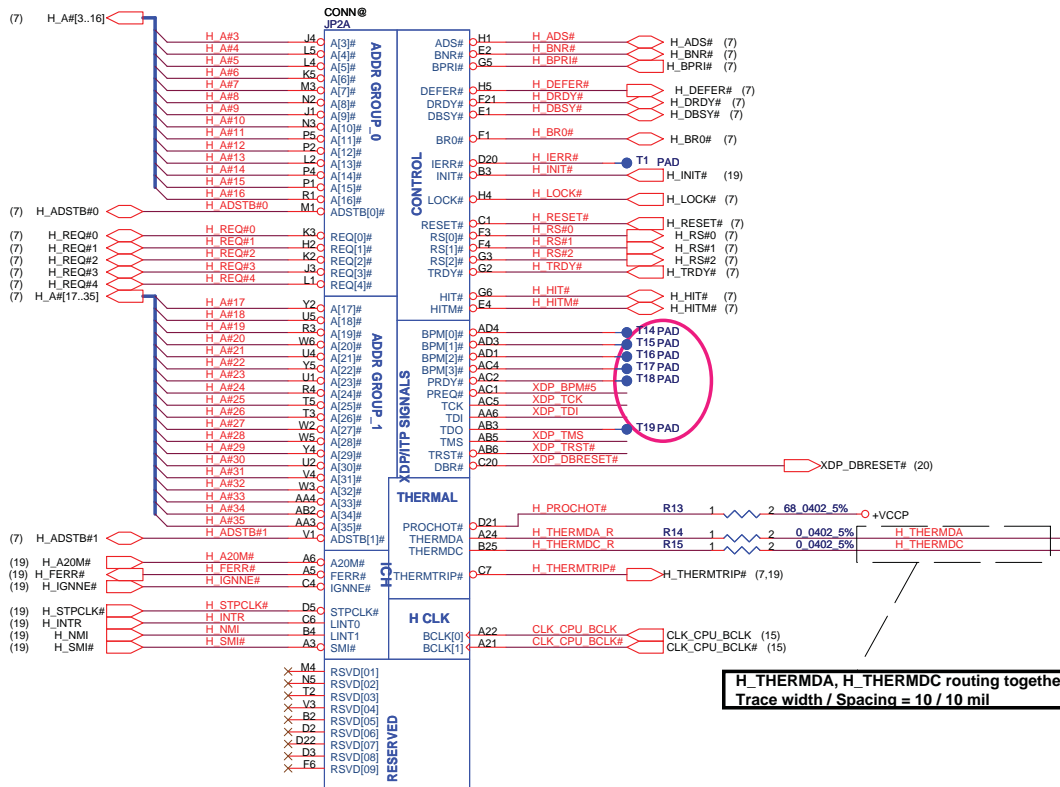
BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

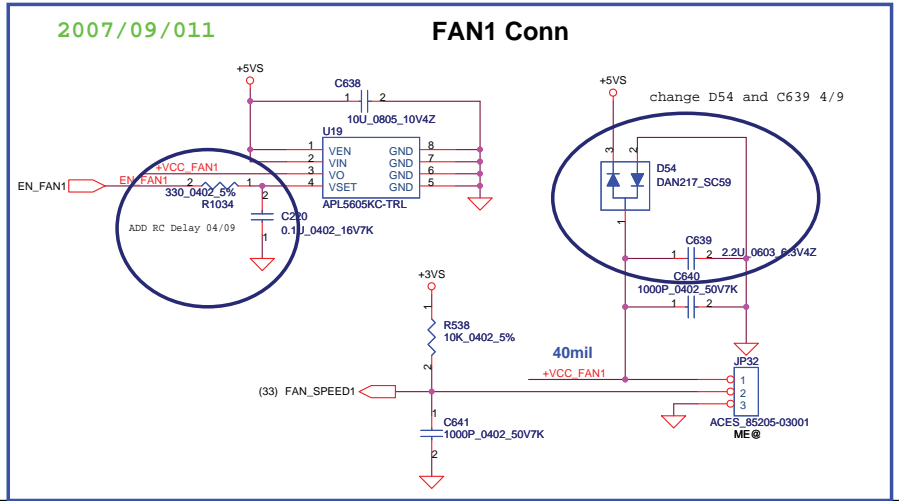
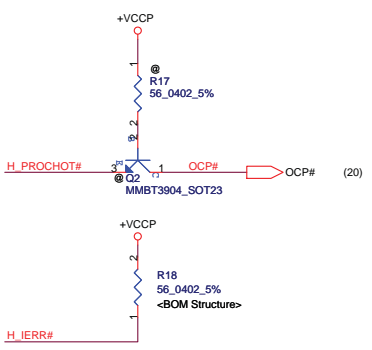
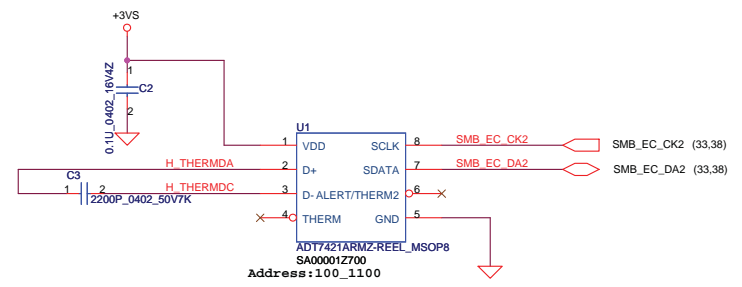
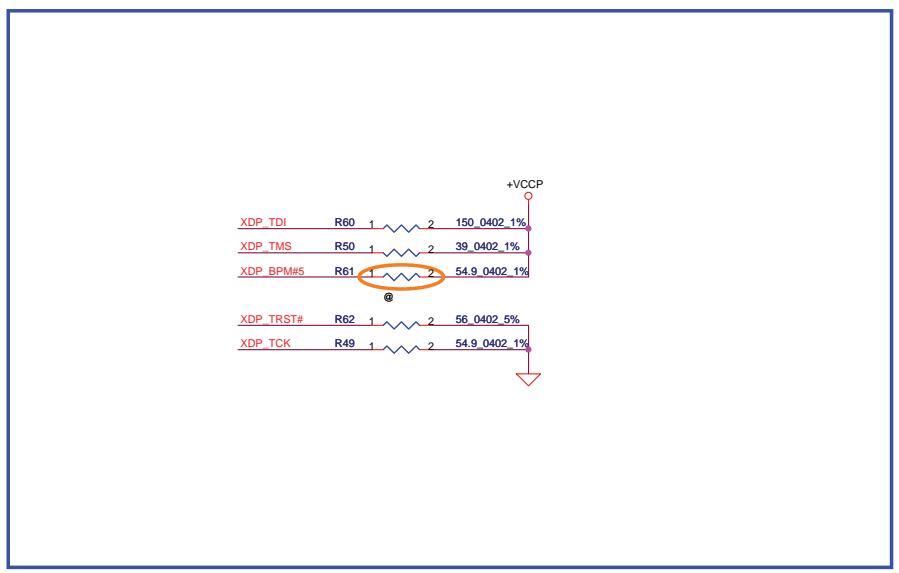
BTO Option Table

BTO Item	BOM Structure
Discrete	PM@
UMA	GM@
CIR	CIR@
8111C	8111C@
8102E	8102E@
ALC888VC	888VC@
ALC888VB	888VB@
ALC268	268@

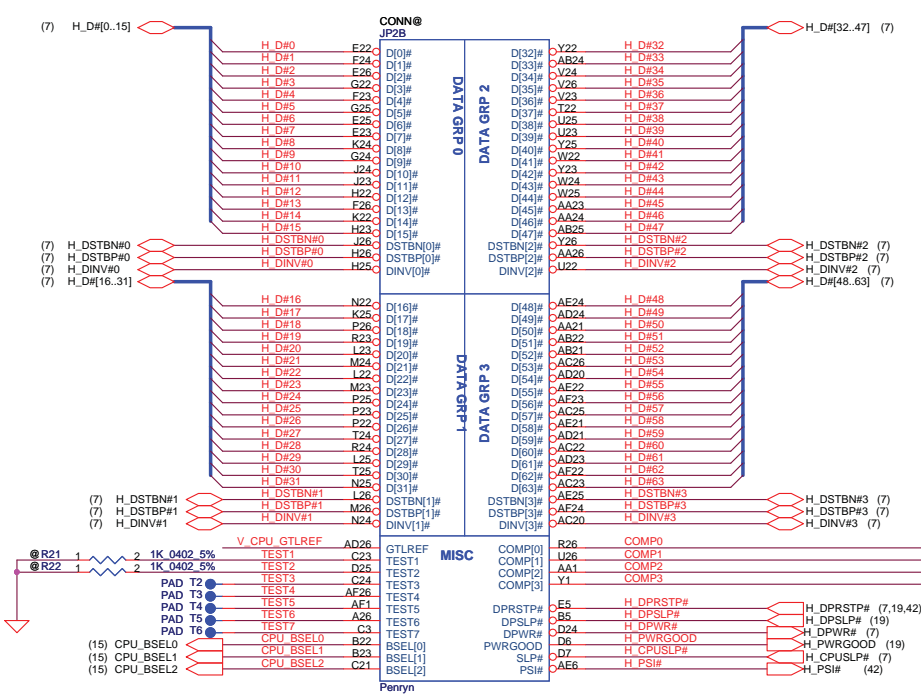
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Size B	Document Number	Rev B	Date:	Friday, July 04, 2008
	401559		Sheet 3 of 44	



H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

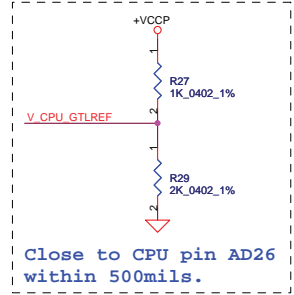


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						401559	401559	B
						Date:	Friday, July 04, 2008	Sheet 4 of 44

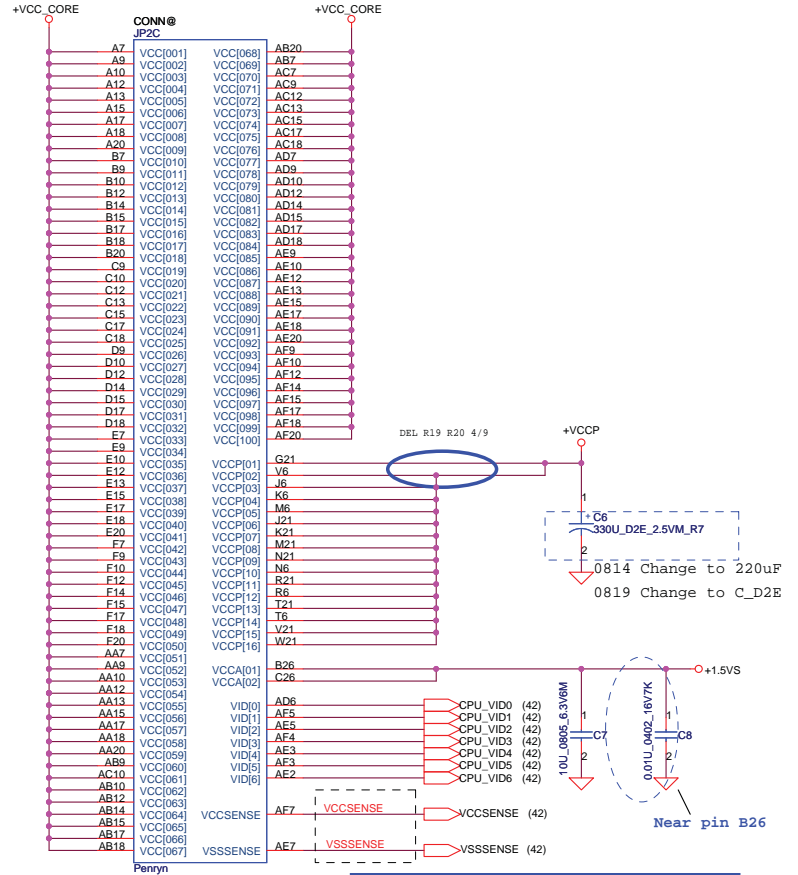


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

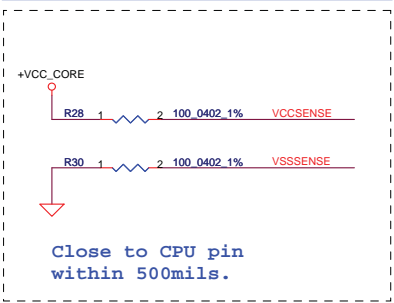
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0



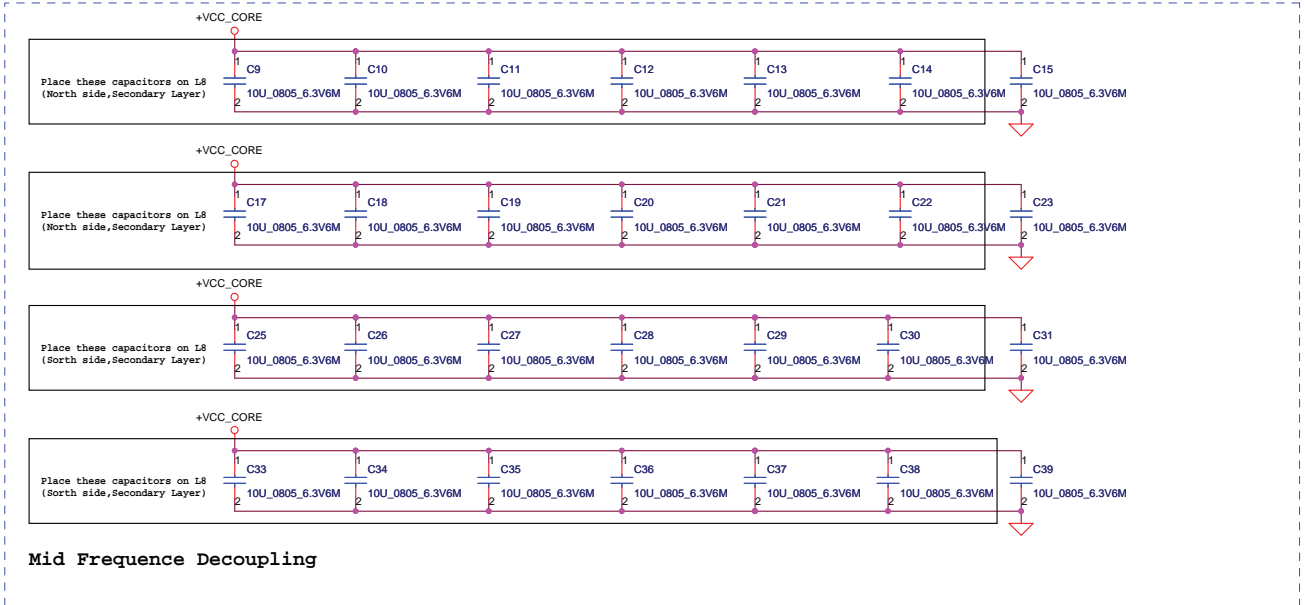
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Length match within 25 mils. The trace width/space/other is 20/7/25.

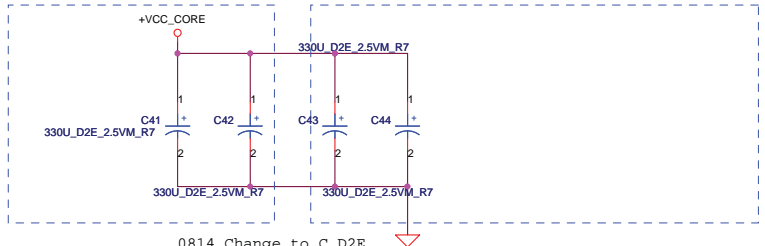


CONN@ JP2D		
A4	VSS[001]	VSS[082]
A8	VSS[002]	VSS[083]
A11	VSS[003]	VSS[084]
A14	VSS[004]	VSS[085]
A16	VSS[005]	VSS[086]
A19	VSS[006]	VSS[087]
A23	VSS[007]	VSS[088]
AF2	VSS[008]	VSS[089]
B6	VSS[009]	VSS[090]
B8	VSS[010]	VSS[091]
B11	VSS[011]	VSS[092]
B13	VSS[012]	VSS[093]
B16	VSS[013]	VSS[094]
B19	VSS[014]	VSS[095]
B21	VSS[015]	VSS[096]
B24	VSS[016]	VSS[097]
C5	VSS[017]	VSS[098]
C8	VSS[018]	VSS[099]
C11	VSS[019]	VSS[100]
C14	VSS[020]	VSS[101]
C16	VSS[021]	VSS[102]
C2	VSS[022]	VSS[103]
C22	VSS[024]	VSS[105]
C25	VSS[025]	VSS[106]
D1	VSS[026]	VSS[107]
D4	VSS[027]	VSS[108]
D8	VSS[028]	VSS[109]
D11	VSS[029]	VSS[110]
D13	VSS[030]	VSS[111]
D16	VSS[031]	VSS[112]
D19	VSS[032]	VSS[113]
D23	VSS[033]	VSS[114]
D26	VSS[034]	VSS[115]
E3	VSS[035]	VSS[116]
E6	VSS[036]	VSS[117]
E8	VSS[037]	VSS[118]
E11	VSS[038]	VSS[119]
E14	VSS[039]	VSS[120]
E16	VSS[040]	VSS[121]
E19	VSS[041]	VSS[122]
E21	VSS[042]	VSS[123]
E24	VSS[043]	VSS[124]
F5	VSS[044]	VSS[125]
F8	VSS[045]	VSS[126]
F11	VSS[046]	VSS[127]
F13	VSS[047]	VSS[128]
F16	VSS[048]	VSS[129]
F19	VSS[049]	VSS[130]
F2	VSS[050]	VSS[131]
F25	VSS[051]	VSS[132]
G23	VSS[052]	VSS[133]
G4	VSS[053]	VSS[134]
G1	VSS[054]	VSS[135]
G23	VSS[055]	VSS[136]
G26	VSS[056]	VSS[137]
H3	VSS[057]	VSS[138]
H6	VSS[058]	VSS[139]
H21	VSS[059]	VSS[140]
H24	VSS[060]	VSS[141]
J2	VSS[061]	VSS[142]
J5	VSS[062]	VSS[143]
J22	VSS[063]	VSS[144]
J25	VSS[064]	VSS[145]
K1	VSS[065]	VSS[146]
K4	VSS[066]	VSS[147]
K23	VSS[067]	VSS[148]
K26	VSS[068]	VSS[149]
L3	VSS[069]	VSS[150]
L6	VSS[070]	VSS[151]
L21	VSS[071]	VSS[152]
L24	VSS[072]	VSS[153]
M2	VSS[073]	VSS[154]
M5	VSS[074]	VSS[155]
M22	VSS[075]	VSS[156]
M25	VSS[076]	VSS[157]
N1	VSS[077]	VSS[158]
N4	VSS[078]	VSS[159]
N23	VSS[079]	VSS[160]
N26	VSS[080]	VSS[161]
P3	VSS[081]	VSS[162]
	VSS[163]	

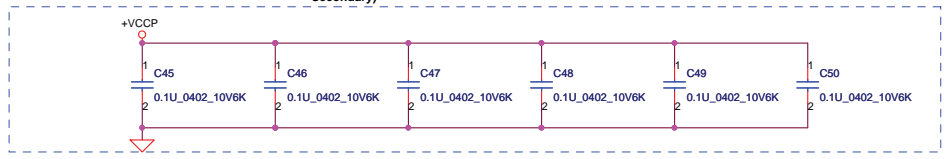


Near CPU CORE regulator

ESR <= 1.5m ohm
Capacitor > 1980uF

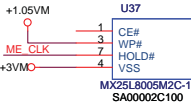
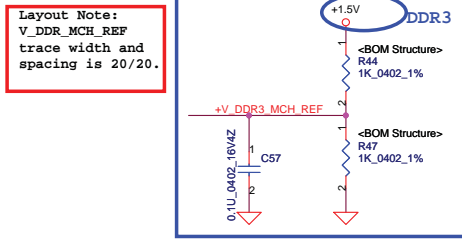
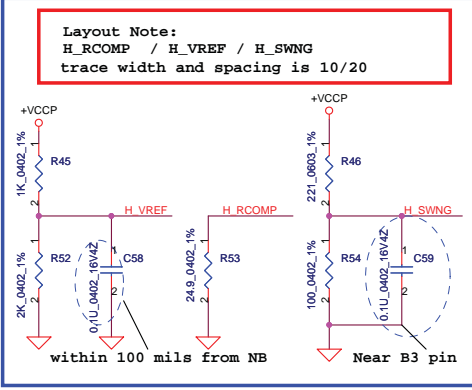
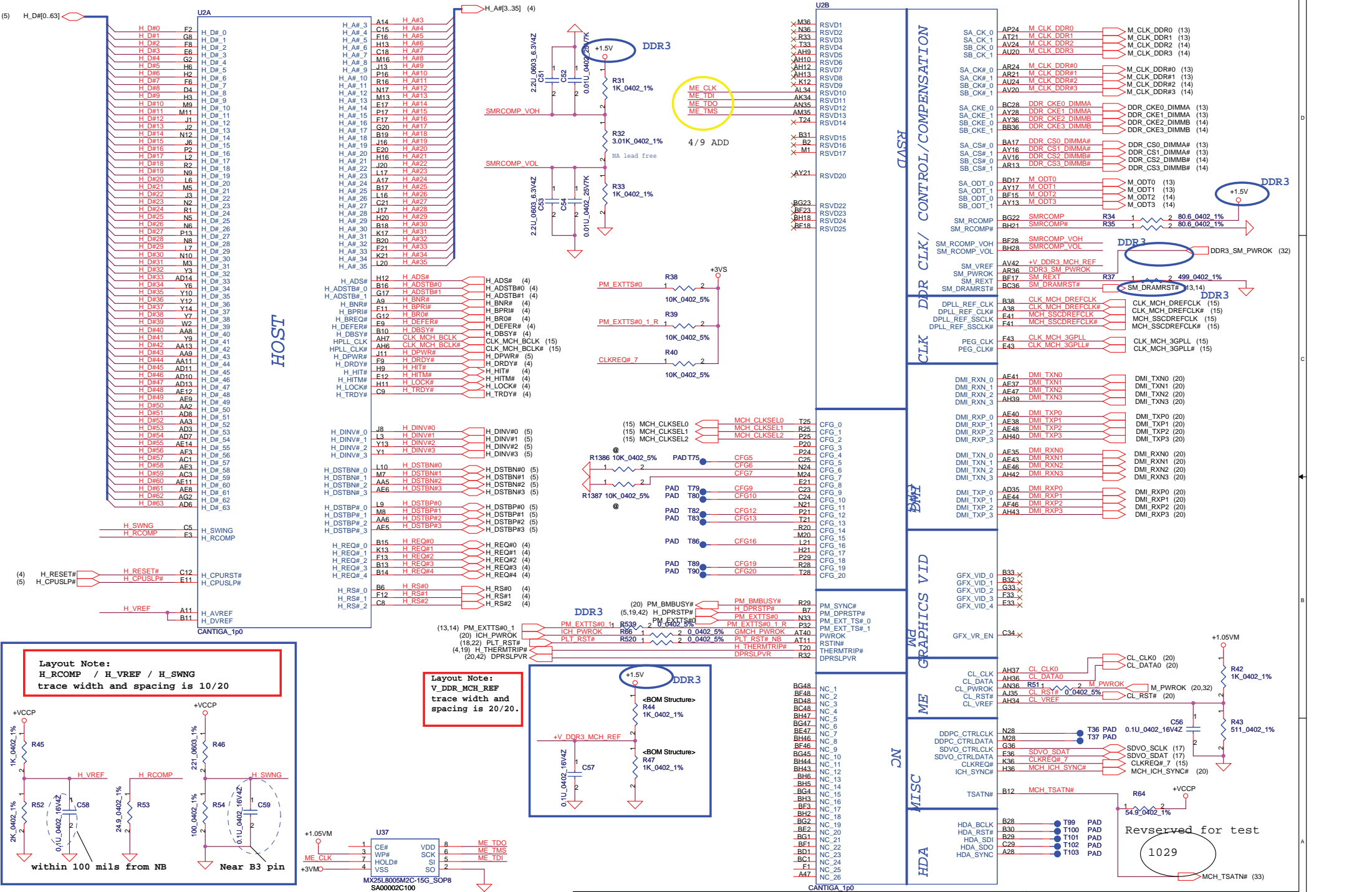


Place these inside socket cavity on L8 (North side Secondary)

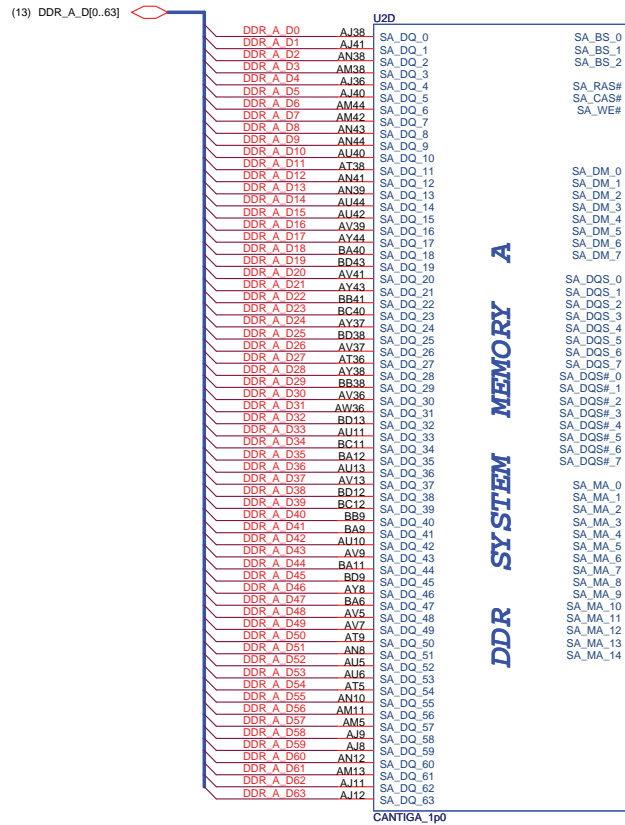


DEL 330U 1017

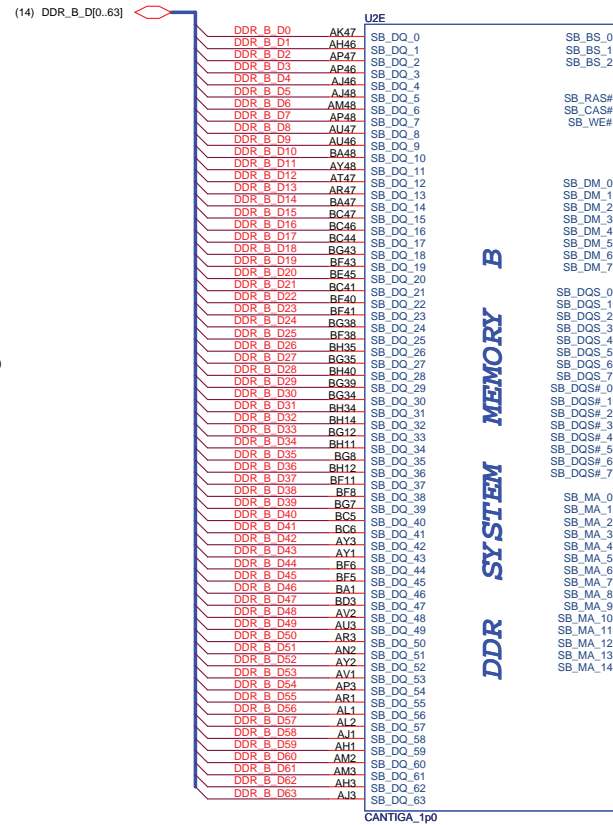
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				Custom	401539	B
				Date:	Friday, July 04, 2008	Sheet 6 of 44



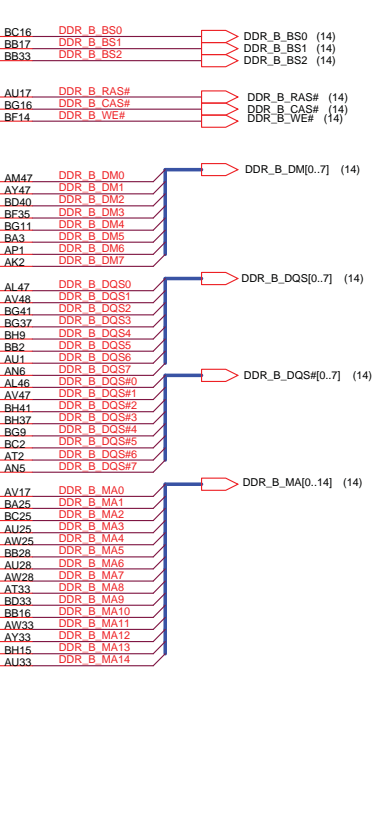
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Custom	401559	Friday, July 04, 2008		B
Sheet 7 of 44				



DDR SYSTEM MEMORY A



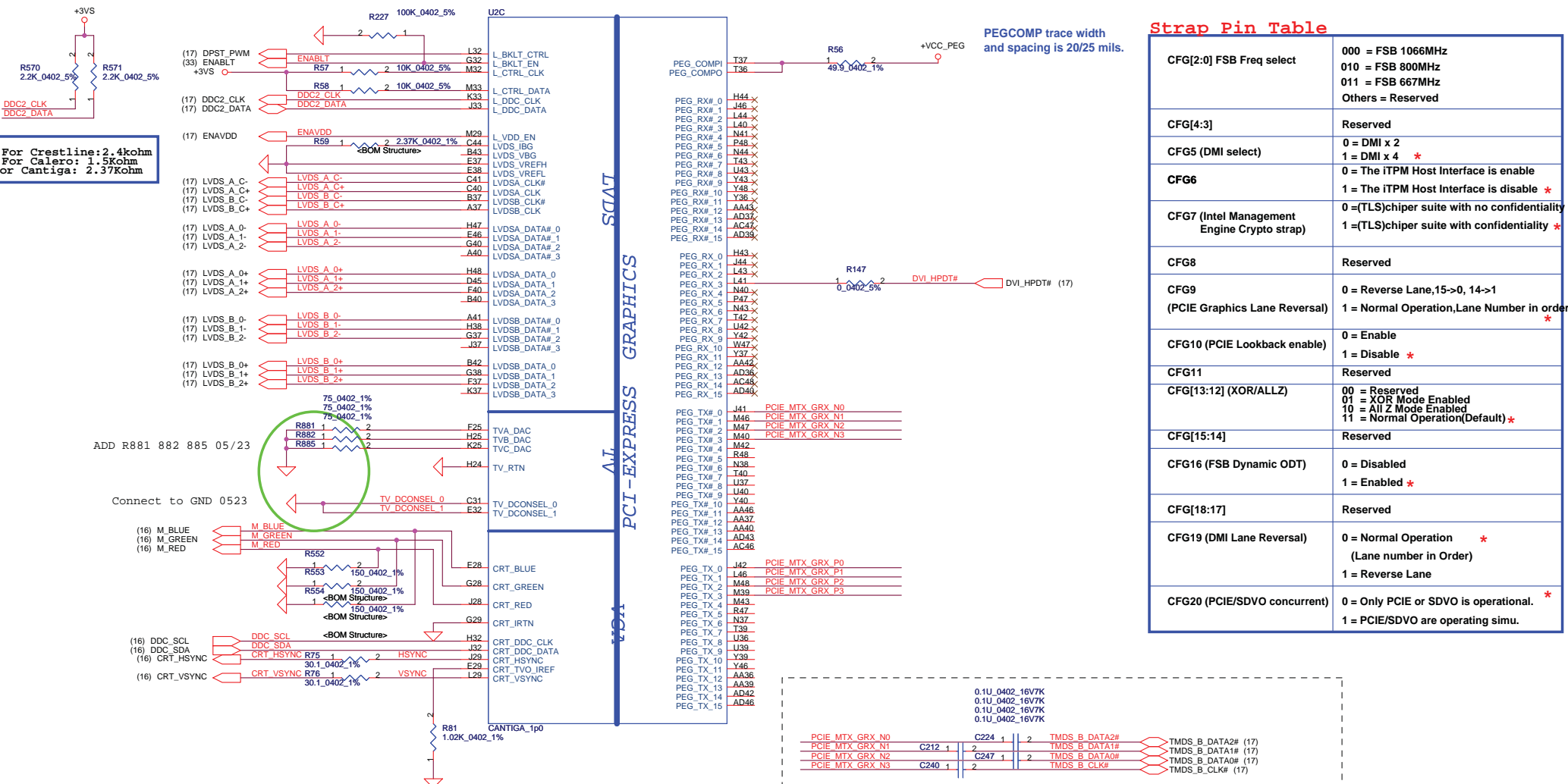
DDR SYSTEM MEMORY B



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Date:	Friday, July 04, 2008	Sheet 8 of 44

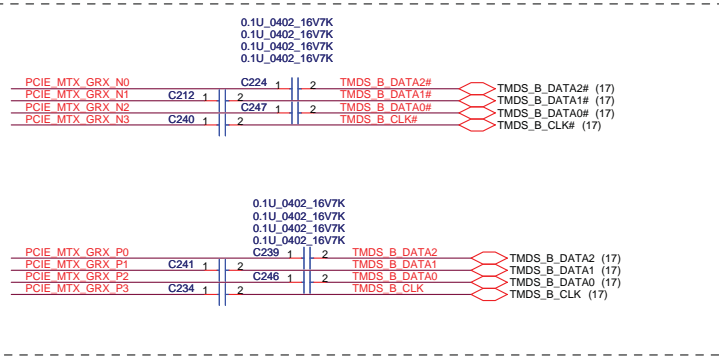


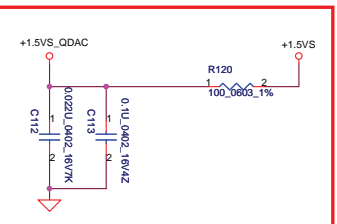
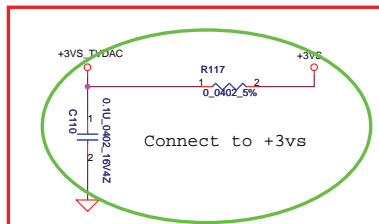
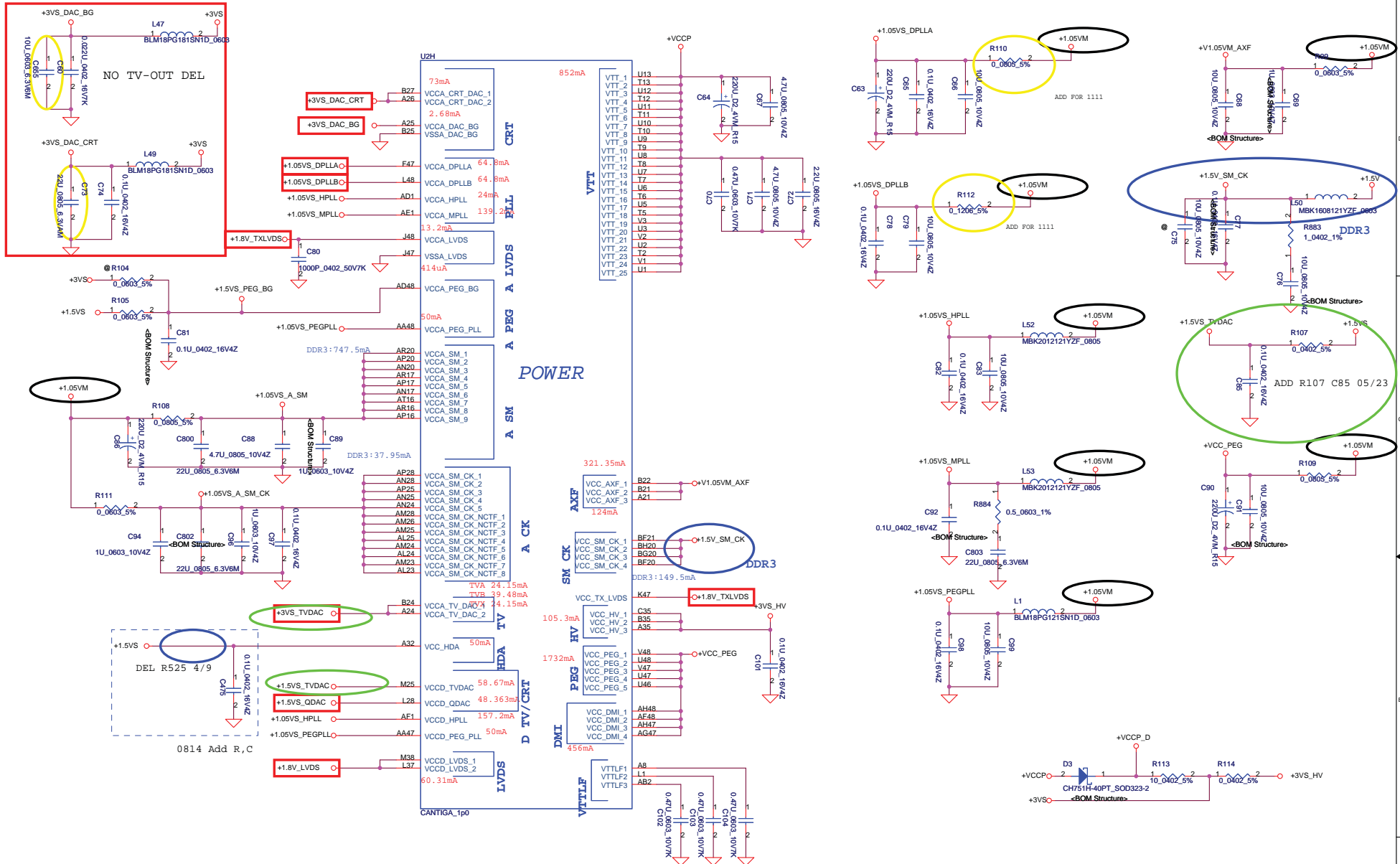
For Crestline: 2.4kohm
 For Calero: 1.5kohm
 For Cantiga: 2.37kohm

PEGCOMP trace width and spacing is 20/25 mils.

Strap Pin Table

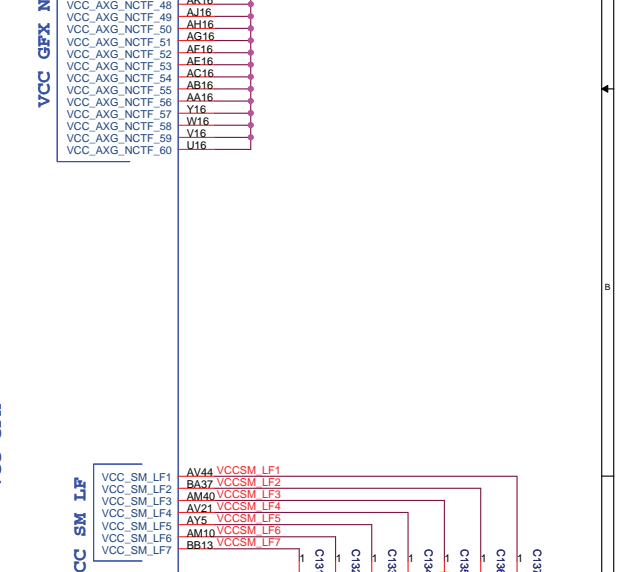
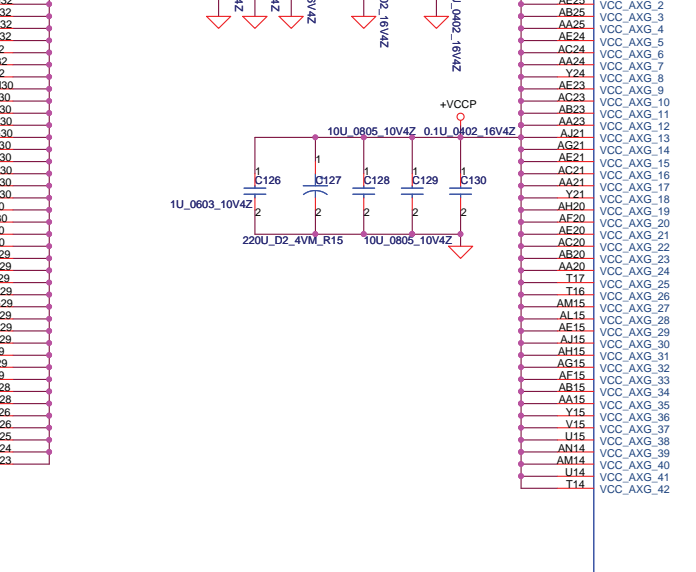
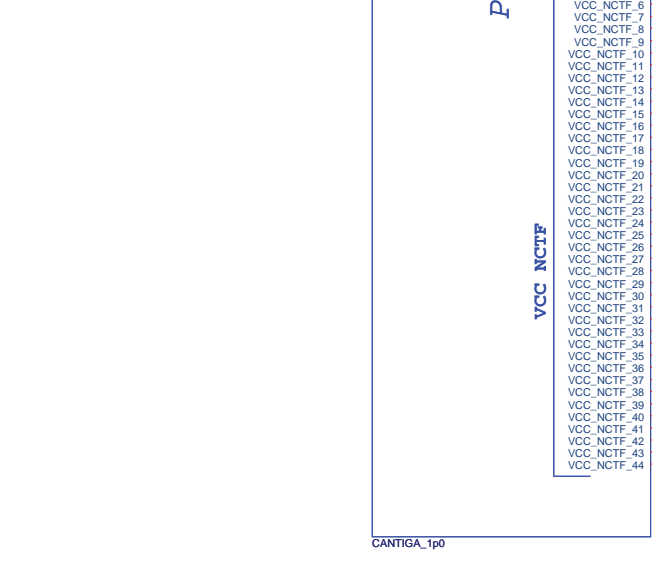
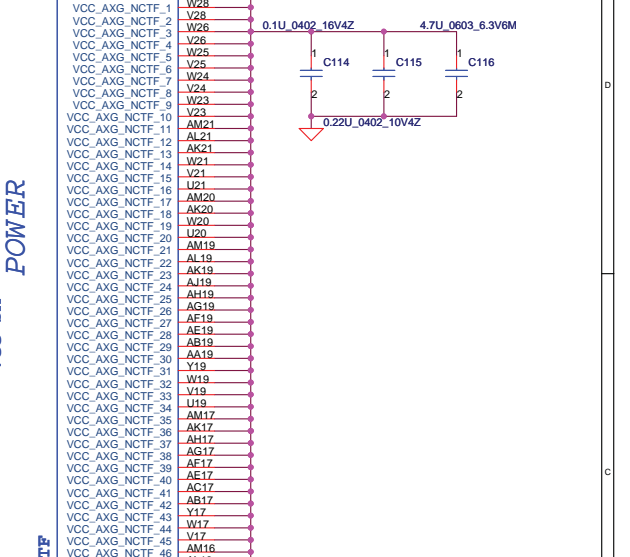
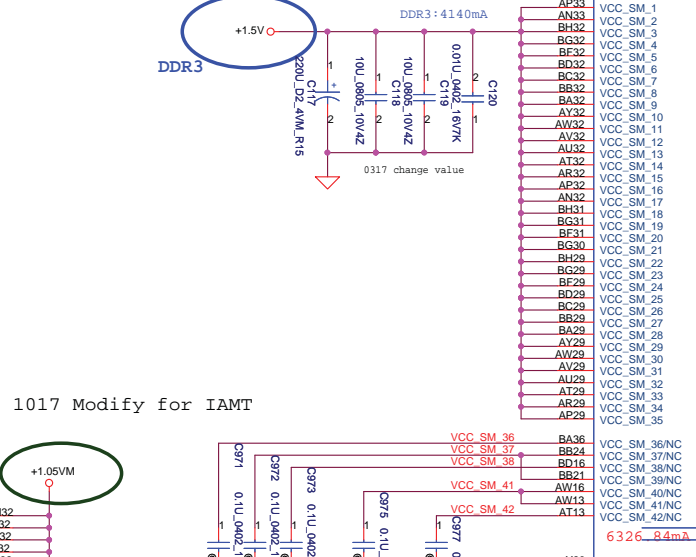
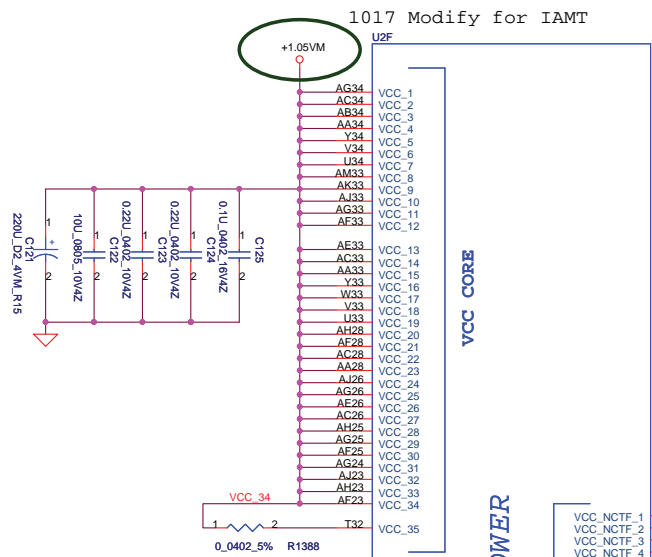
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0=(TLS)chiper suite with no confidentiality 1=(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane, 15->0, 14->1 1 = Normal Operation, Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All 2 Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.





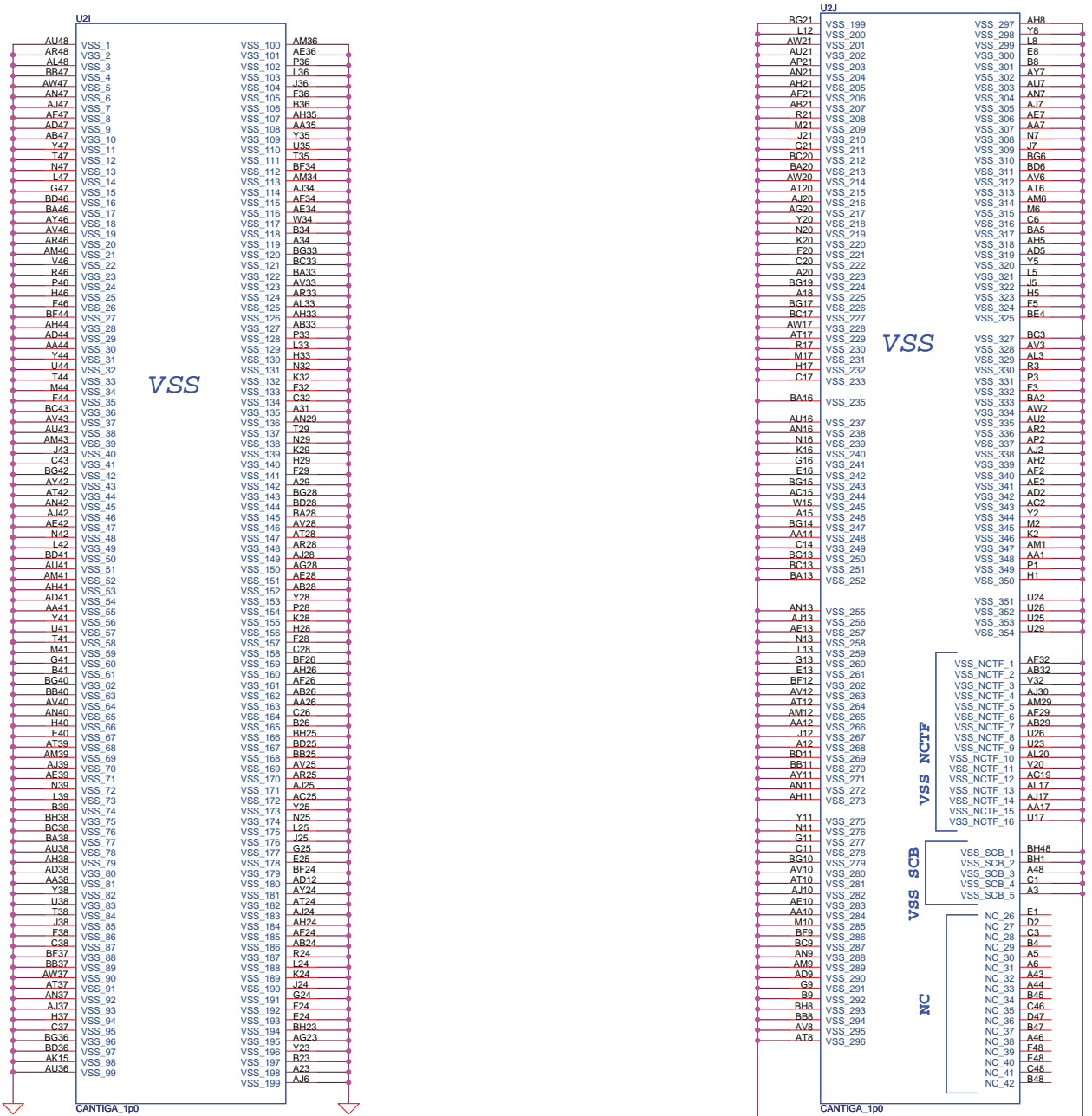
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Date	Friday, July 04, 2008	Sheet	10	of	44

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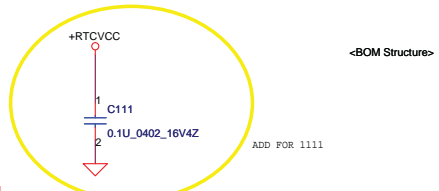
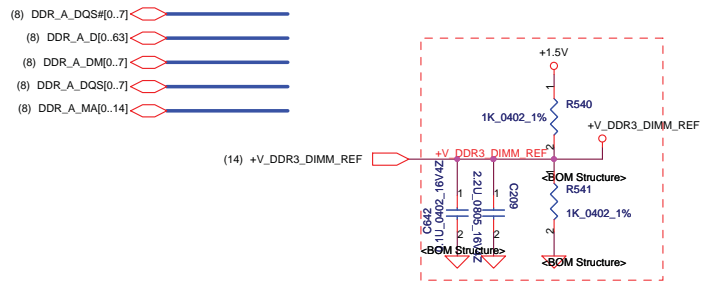


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Size	Document Number	Date:	Rev
Custom	401559	Friday, July 04, 2008	B
Sheet		11 of 44	

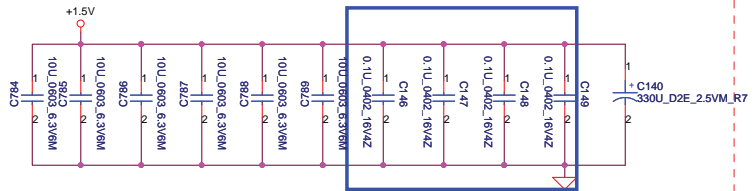


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Size	Document Number	Rev		B	
Custort	401559				
Date:	Friday, July 04, 2008	Sheet	12	of	44

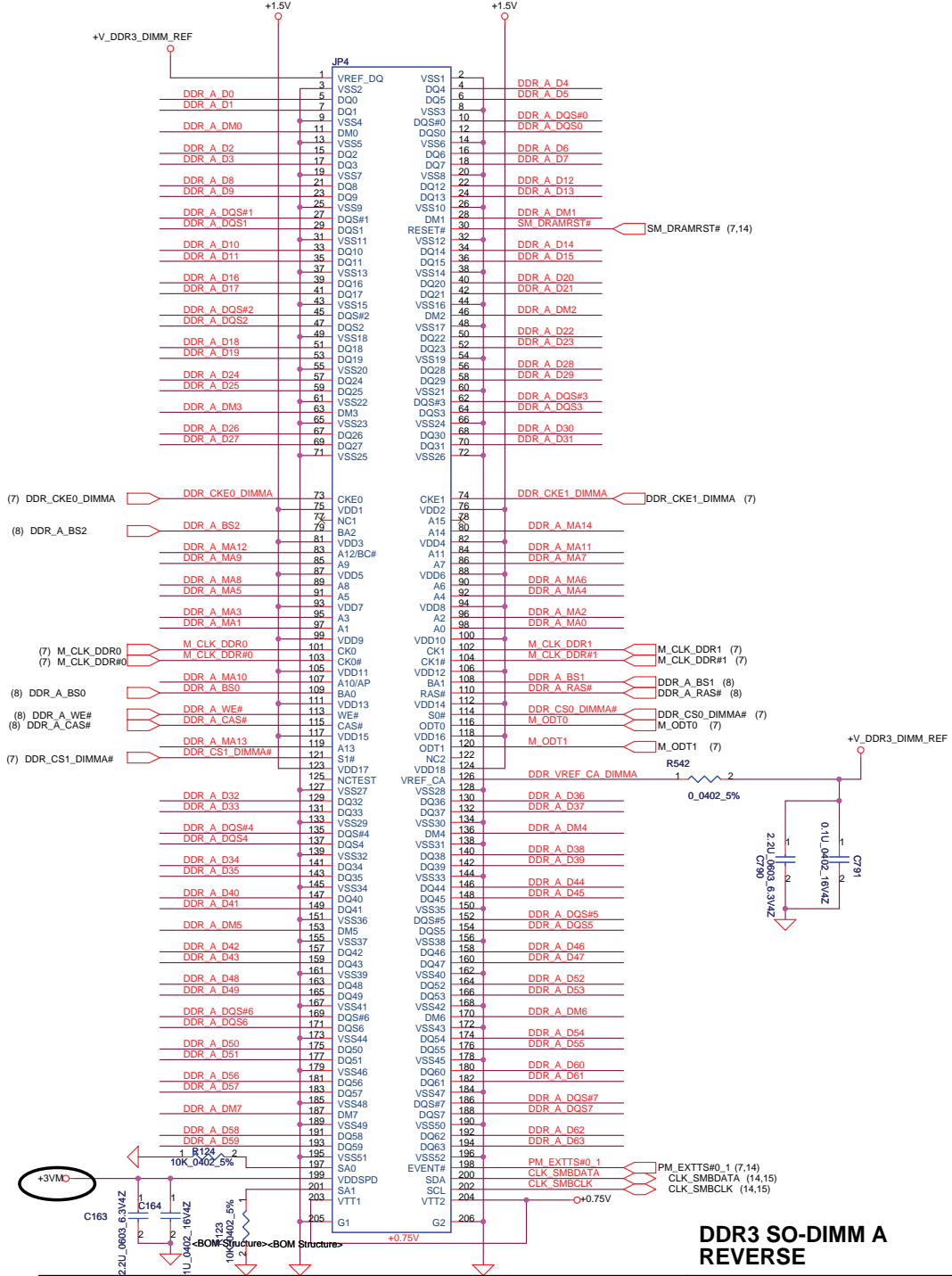
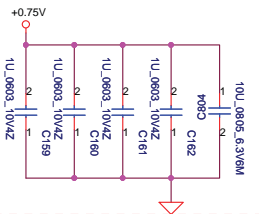


Layout Note:
Place near JP4

Layout Note: Place these 4 Caps near Command and Control-signals-of-DIMM

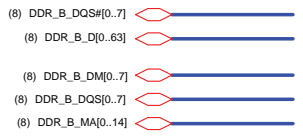


Layout Note:
Place near JP4.203 & JP4.204



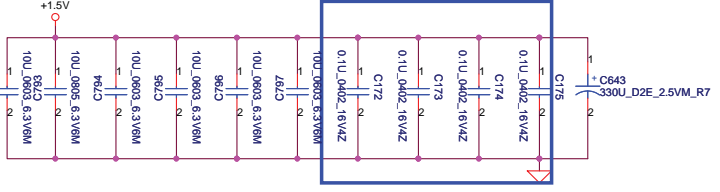
DDR3 SO-DIMM A REVERSE

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				401559	Rev B
Date:	Friday, July 04, 2008	Sheet	13	of 44	

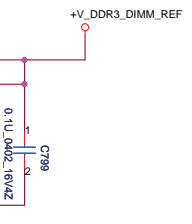
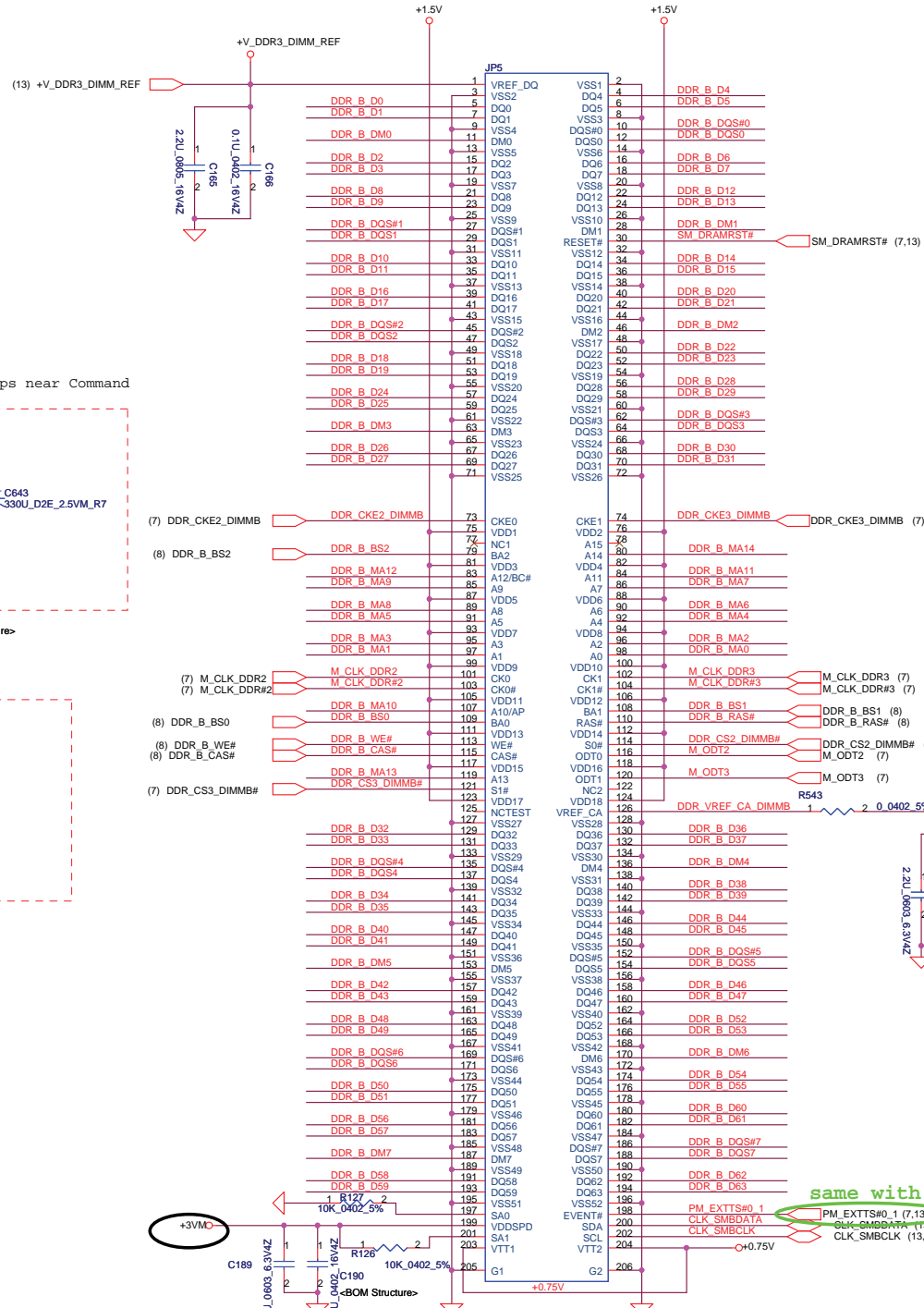
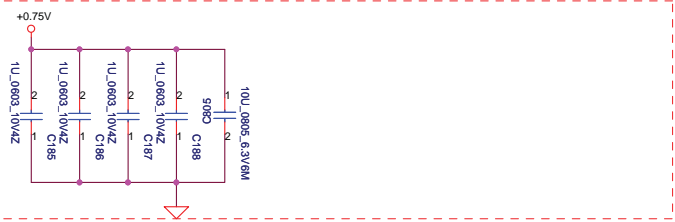


Layout Note:
Place near JP5

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



Layout Note:
Place near JP5.203 & JP5.204



same with intel DDR3 CRB connection

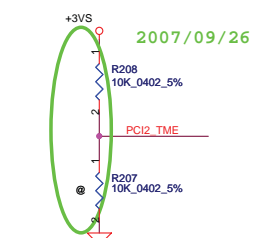
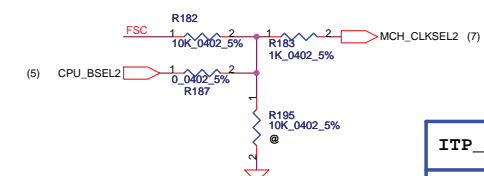
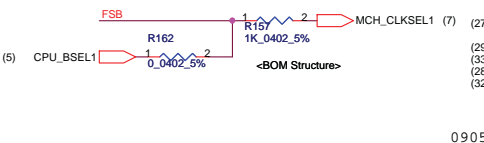
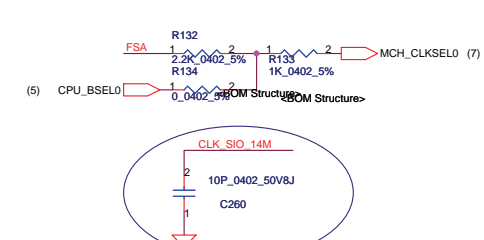
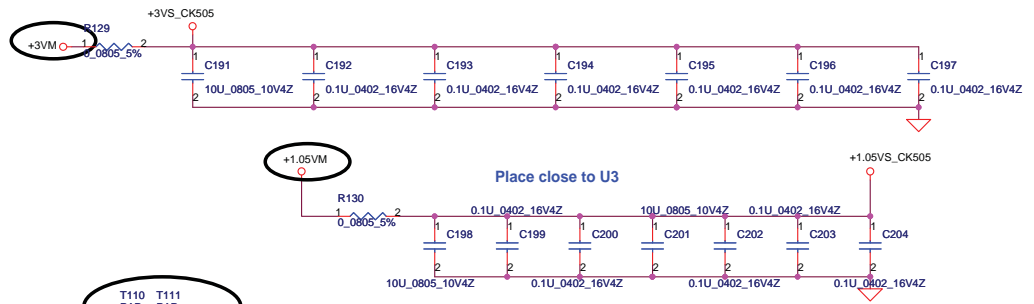
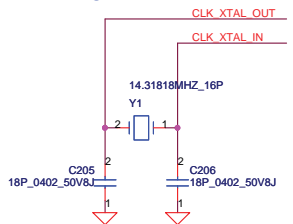
DDR3 SO-DIMM B
REVERSE

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Compal Electronics, Inc.			
SCHEMATIC, M/B A4311			
Size	Document Number		Rev
	401559		B
Date:	Friday, July 04, 2008	Sheet	14 of 44

FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB	
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz	
0	0	0	266	100	33.3	14.318	96.0	48.0	
0	0	1	133	100	33.3	14.318	96.0	48.0	
0	1	0	200	100	33.3	14.318	96.0	48.0	
0	1	1	166	100	33.3	14.318	96.0	48.0	
1	0	0	333	100	33.3	14.318	96.0	48.0	
1	0	1	100	100	33.3	14.318	96.0	48.0	
1	1	0	400	100	33.3	14.318	96.0	48.0	
1	1	1	Reserved						

Routing the trace at least 10mil



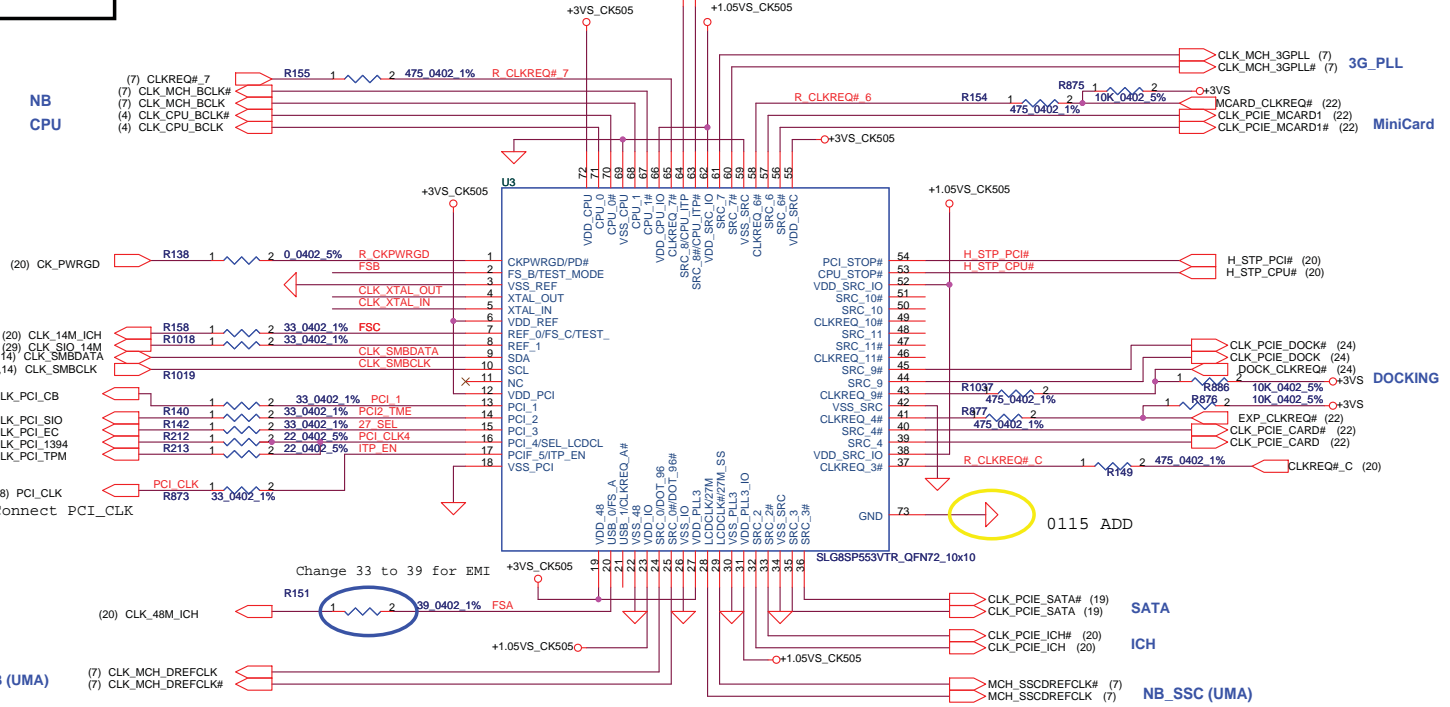
for ICS Overclocking setting
 0=Overclocking of CPU and SRC allowed
 1=Overclocking of CPU and SRC NOT allowed

NB CPU

NB (UMA)

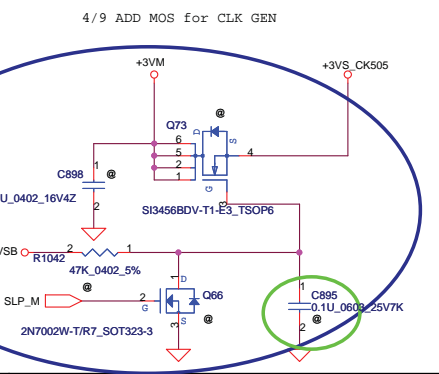
ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
PCI_CLK3	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)

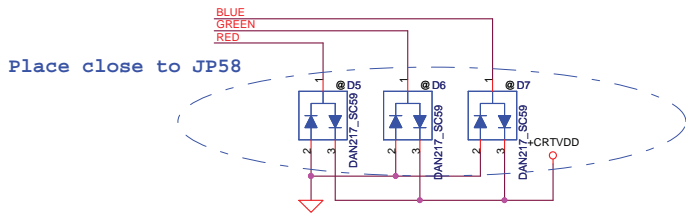
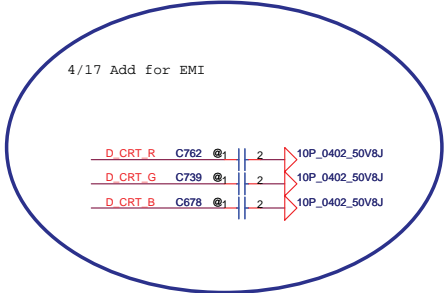
M: ICS P/N:
S: Silego



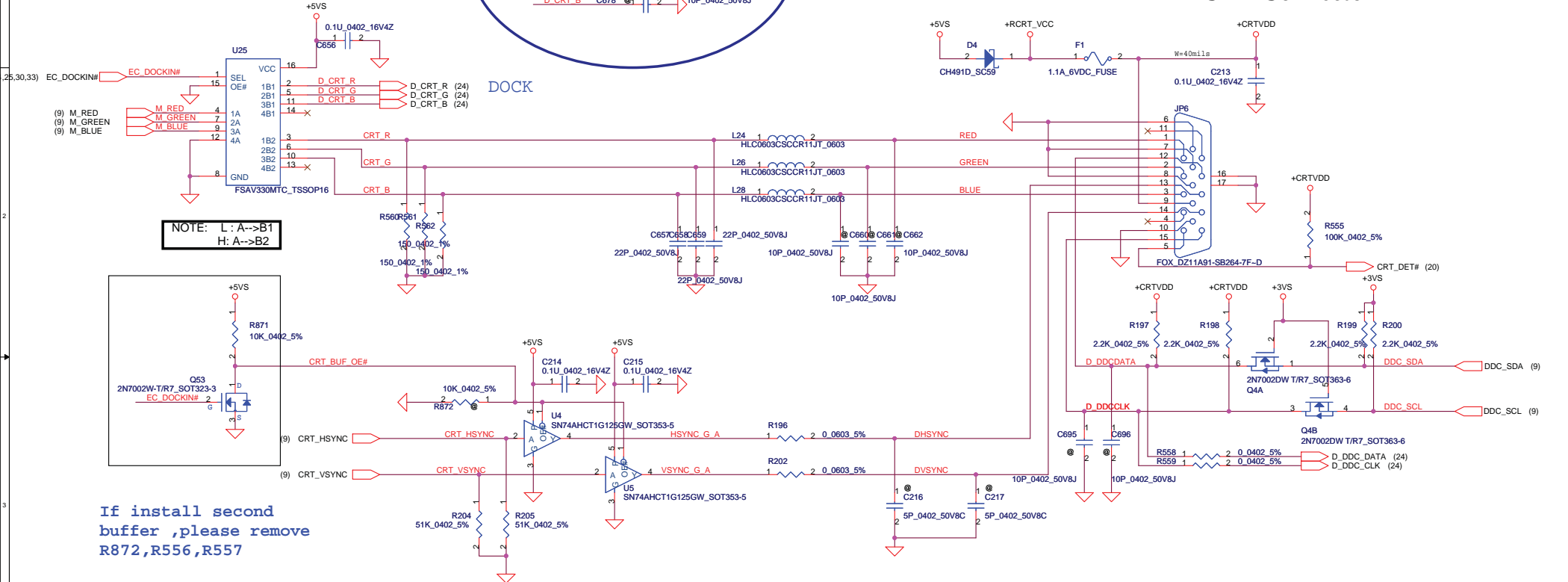
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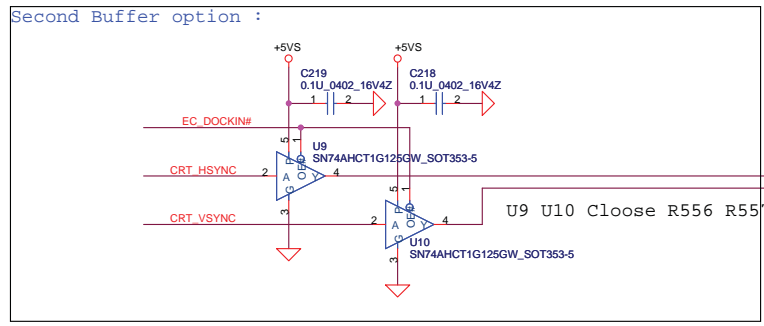




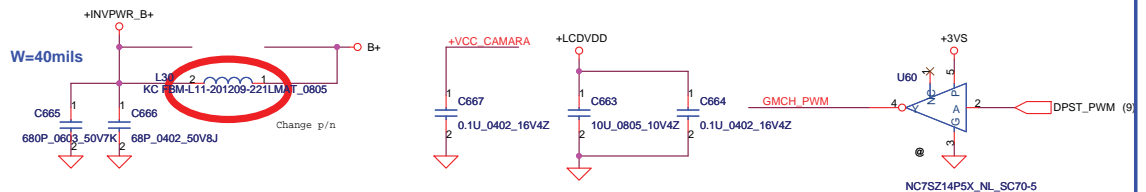
CRT Connector



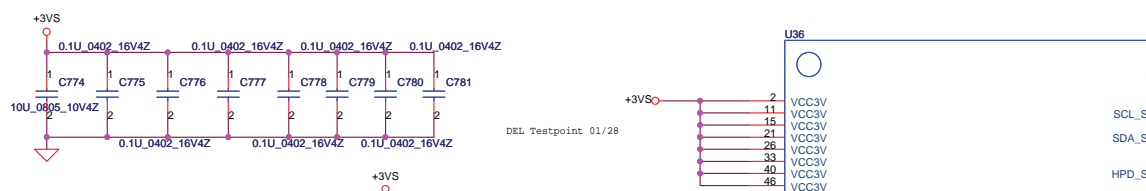
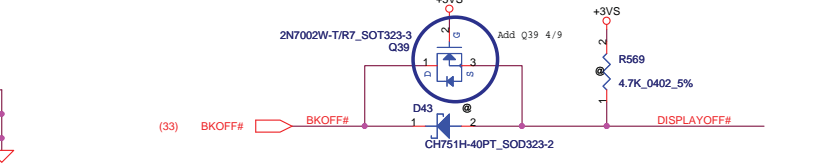
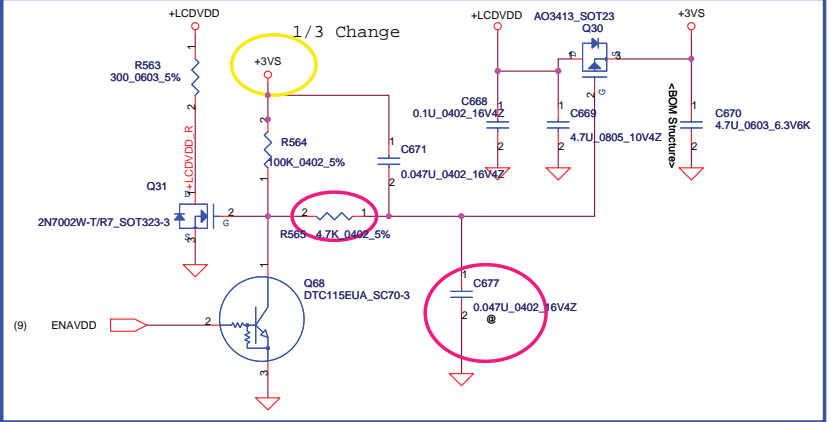
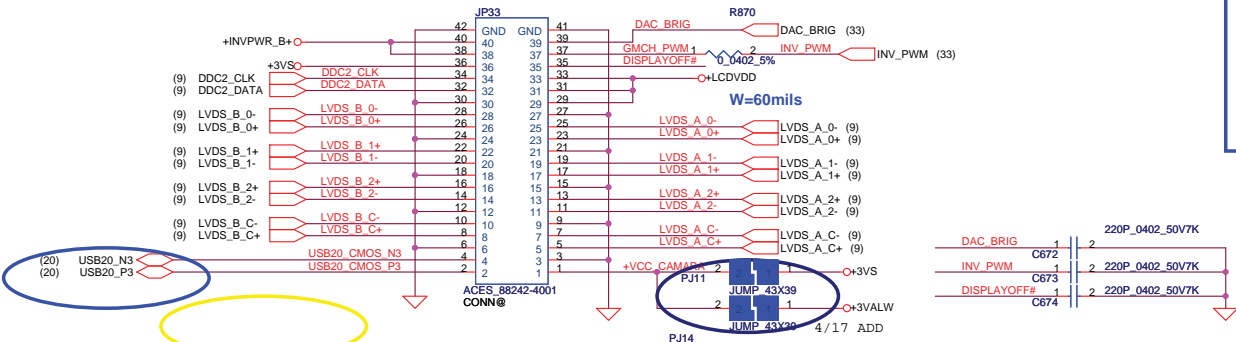
If install second buffer ,please remove R872,R556,R557



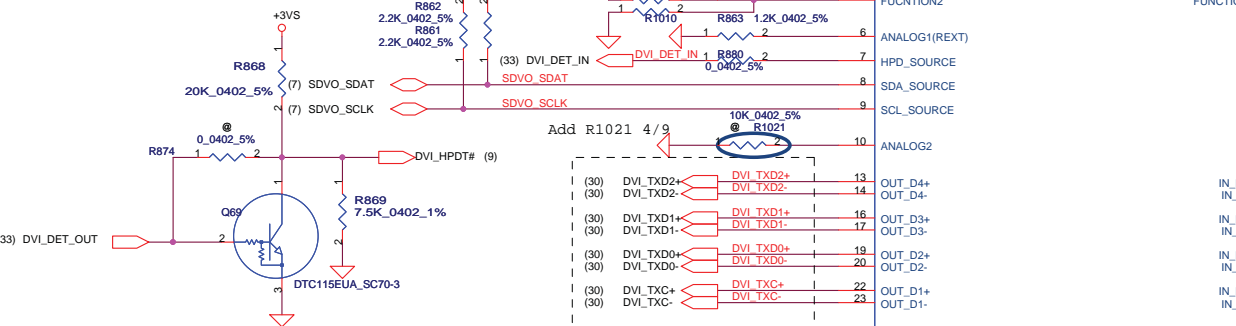
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Size		Document Number	Rev	
		401539	B	
Date:	Friday, July 04, 2008	Sheet	16	of 44



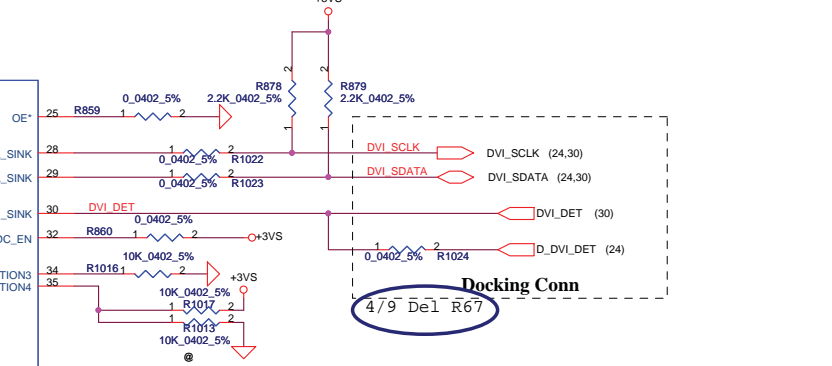
LVDS and USB CAM connector



Docking Conn



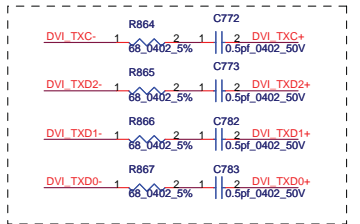
inverting level shift for NB



Docking Conn

4/9 Del R67

pin 4	0 = disable inverting output 1 = enable inverting output
pin 35	0 = Default value 1 = output driver current increased 10%

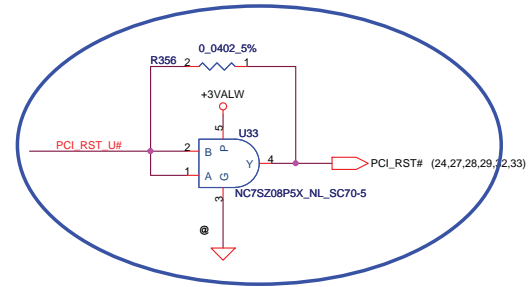
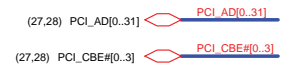
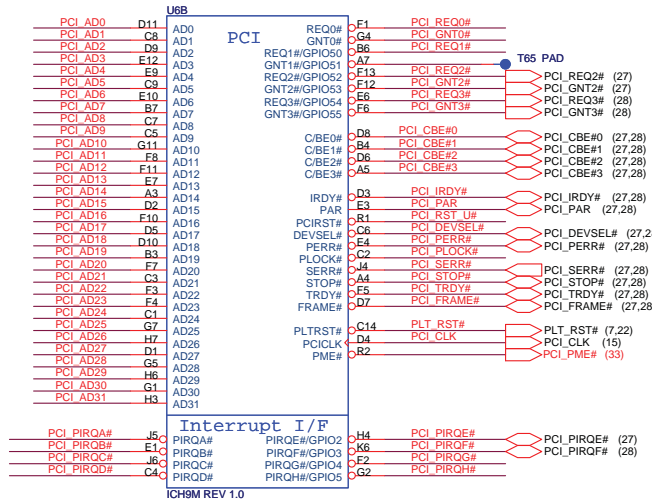
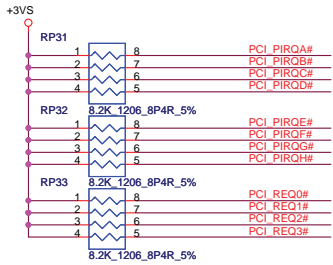
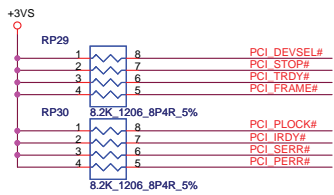


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Date:	Friday, July 04, 2008	Sheet	17	of	44
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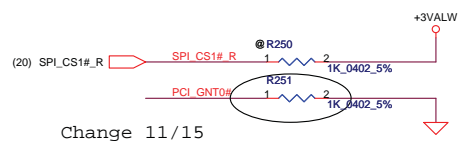


ADD Buffer for 4/9

A16 swap override Strap
 Low= A16 swap override Enable
 High= Default *

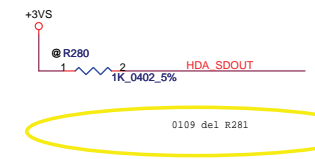
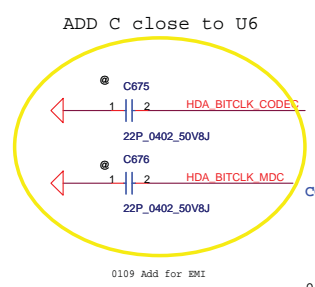
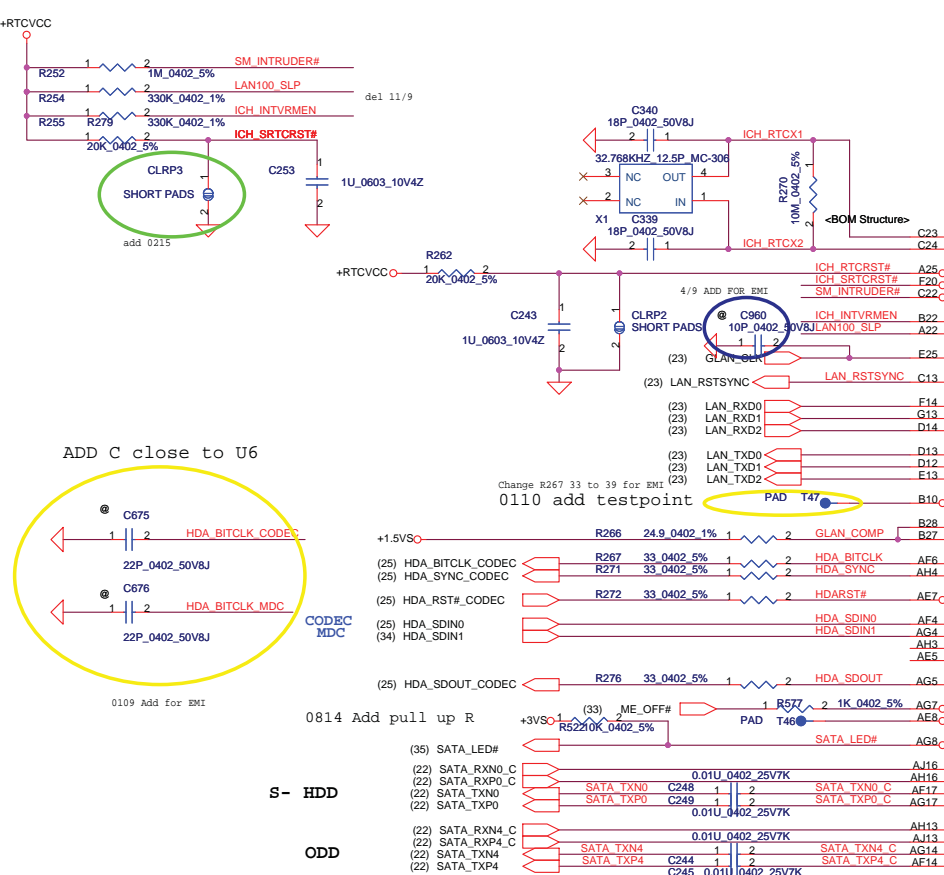


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

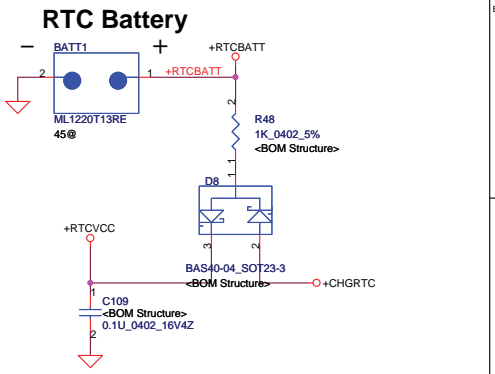
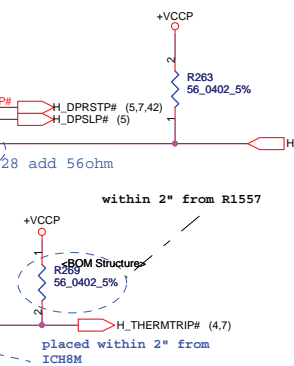
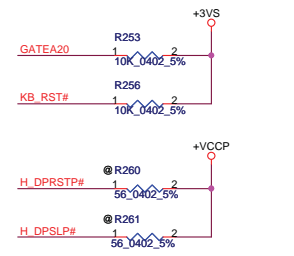
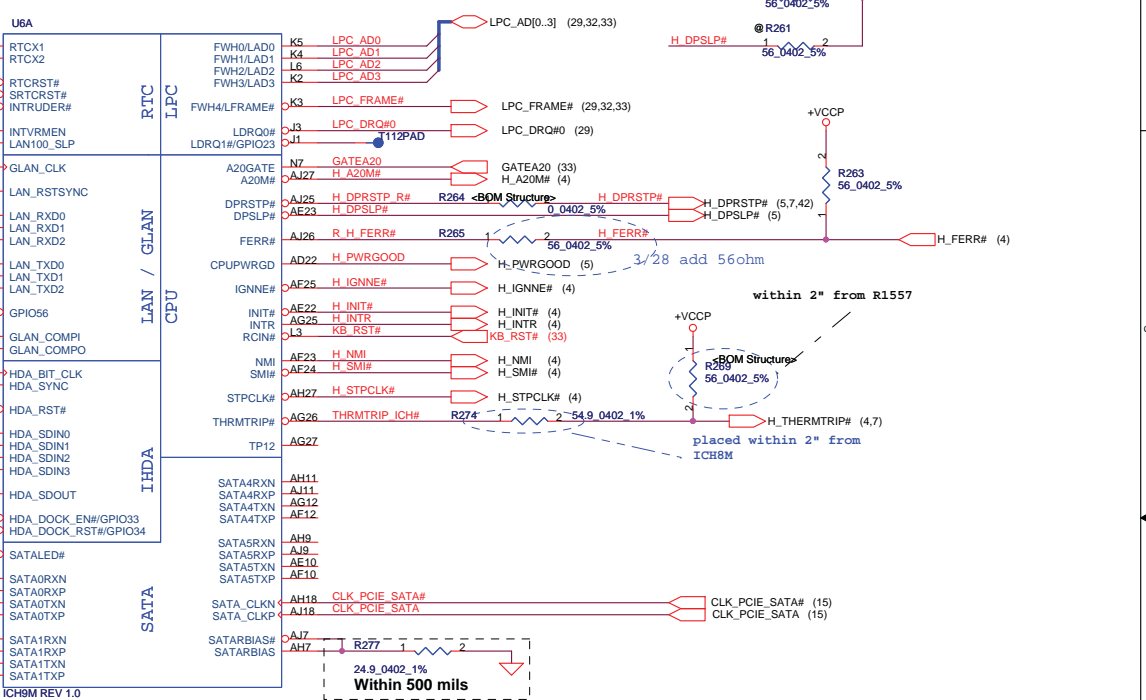


Change 11/15

ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

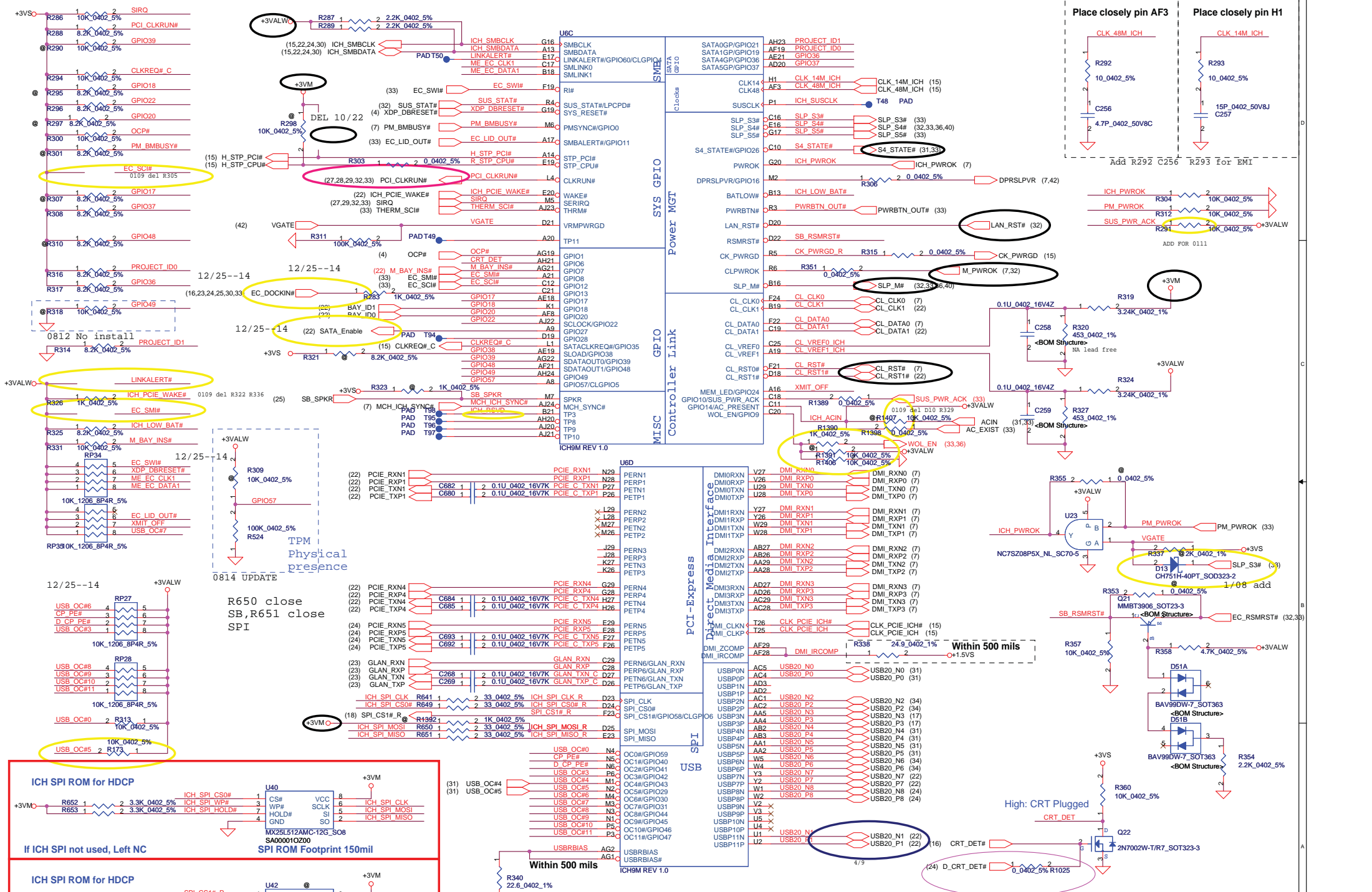


ICH_RSVD	HDA_SDOUIT_CODECC
0	0
0	1
1	0
1	1



Change BATT1 P/N : SP093PA0200 (Panasonic)
SP093MX0000 (MAXELL)

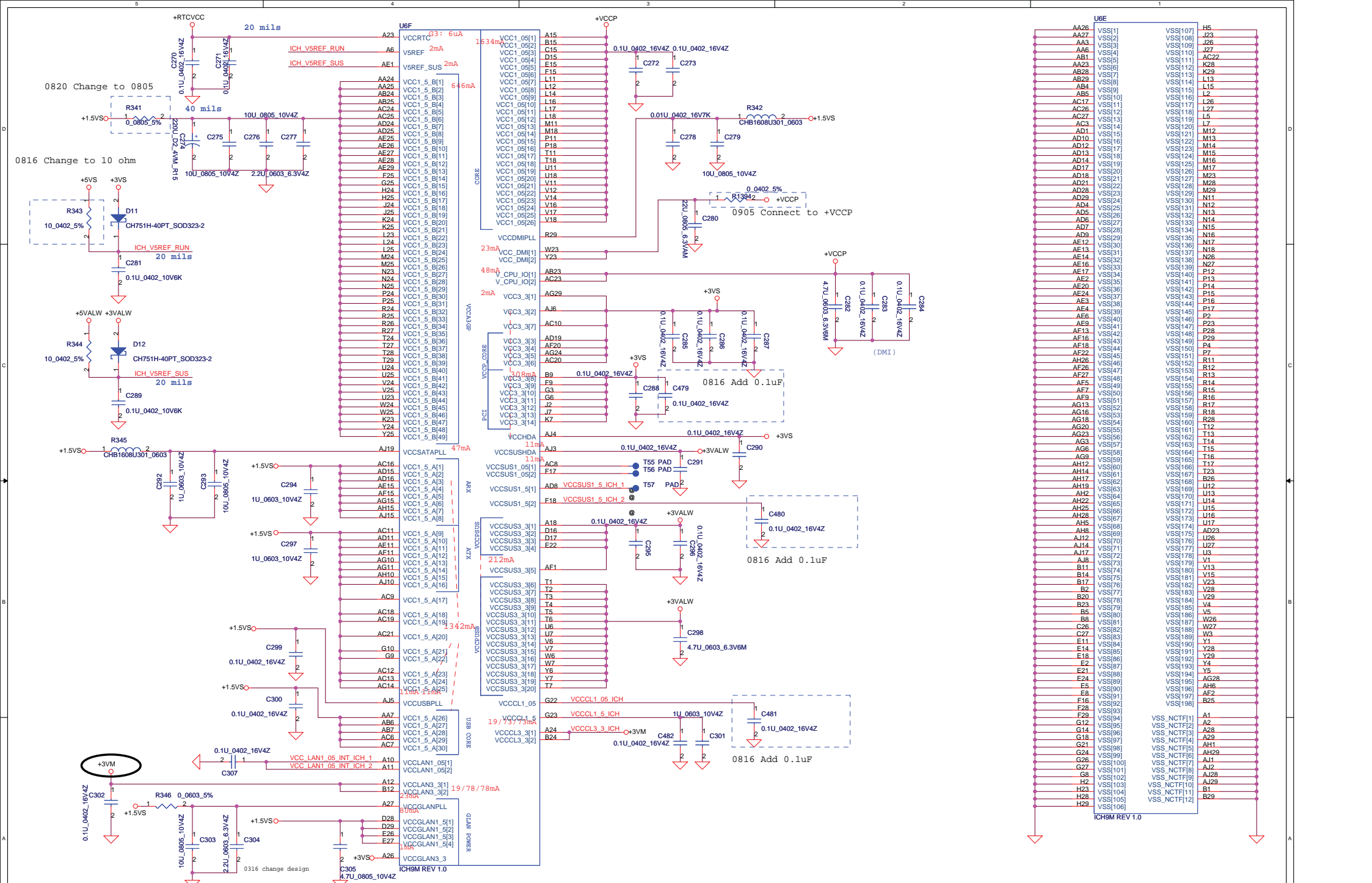
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Date:	Friday, July 04, 2008	Sheet	19	of	44



Security Classification	Compal Secret Data	
Issued Date	2007/09/29	Deciphered Date
		2007/09/29

Compal Electronics, Inc.		
SCHEMATIC, M/B A4311		
Title	Document Number	Rev
	401559	B
Date:	Friday, July 04, 2008	Sheet 20 of 44

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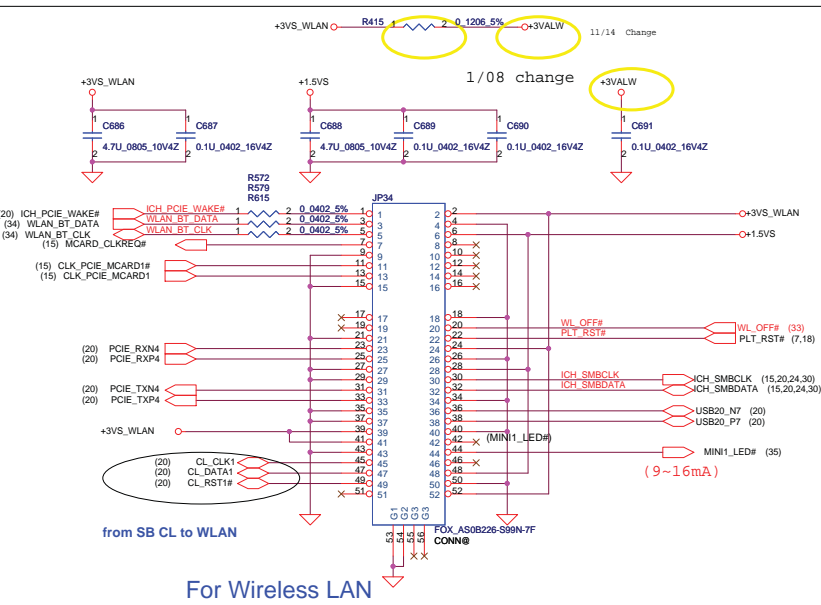
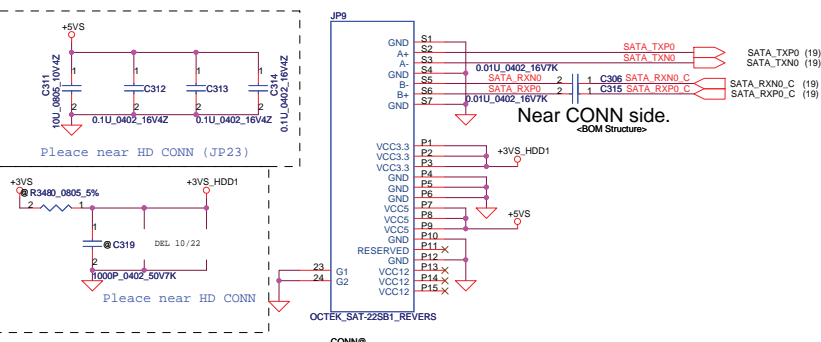


IC9M REV 1.0		
AA26	VSS[1]	H5
AA27	VSS[2]	J23
AA3	VSS[3]	J26
AA6	VSS[4]	J27
AB1	VSS[5]	AC22
AA23	VSS[6]	K28
AB28	VSS[7]	K29
AB23	VSS[8]	L15
AB4	VSS[9]	L2
AB5	VSS[10]	L12
AC17	VSS[11]	L26
AC26	VSS[12]	L27
AC27	VSS[13]	L5
AC3	VSS[14]	L7
AD1	VSS[15]	M12
AD10	VSS[16]	M13
AD12	VSS[17]	M14
AD13	VSS[18]	M15
AD14	VSS[19]	M16
AD17	VSS[20]	M17
AD18	VSS[21]	M23
AD21	VSS[22]	M28
AD28	VSS[23]	M29
AD29	VSS[24]	N11
ADA	VSS[25]	N12
AD5	VSS[26]	N13
AD6	VSS[27]	N14
AD7	VSS[28]	N15
AD9	VSS[29]	N16
AE12	VSS[30]	N17
AE13	VSS[31]	N18
AE14	VSS[32]	N26
AE16	VSS[33]	N27
AE2	VSS[34]	P13
AE20	VSS[35]	P14
AE24	VSS[36]	P15
AE4	VSS[37]	P16
AE6	VSS[38]	P2
AE9	VSS[39]	P23
AE10	VSS[40]	P28
AE18	VSS[41]	P4
AF22	VSS[42]	P7
AH26	VSS[43]	R11
AH28	VSS[44]	R12
AF27	VSS[45]	R13
AF5	VSS[46]	R14
AF7	VSS[47]	R15
AG3	VSS[48]	R16
AG13	VSS[49]	R17
AG16	VSS[50]	R18
AG18	VSS[51]	R28
AG20	VSS[52]	T12
AG23	VSS[53]	T13
AG3	VSS[54]	T14
AG6	VSS[55]	T15
AG8	VSS[56]	T16
AH2	VSS[57]	T17
AH14	VSS[58]	T23
AH17	VSS[59]	B26
AH13	VSS[60]	B27
AH2	VSS[61]	A13
AH22	VSS[62]	U14
AH25	VSS[63]	U15
AH28	VSS[64]	U16
AH5	VSS[65]	U17
AH8	VSS[66]	AD23
AJ12	VSS[67]	U26
AJ14	VSS[68]	U27
AJ17	VSS[69]	U3
AJ8	VSS[70]	V1
B11	VSS[71]	V13
B14	VSS[72]	V15
B17	VSS[73]	V23
B2	VSS[74]	V28
B20	VSS[75]	V29
B23	VSS[76]	V4
B5	VSS[77]	V5
B8	VSS[78]	W26
C26	VSS[79]	W27
C27	VSS[80]	W3
E14	VSS[81]	Y1
E18	VSS[82]	Y28
E2	VSS[83]	Y4
E21	VSS[84]	Y5
E24	VSS[85]	AG28
E5	VSS[86]	AH6
E8	VSS[87]	AF2
F19	VSS[88]	B25
F28	VSS[89]	
F29	VSS[90]	
G12	VSS[91]	VSS_NCTF[1]
G14	VSS[92]	VSS_NCTF[2]
G18	VSS[93]	VSS_NCTF[3]
G21	VSS[94]	VSS_NCTF[4]
G24	VSS[95]	VSS_NCTF[5]
G26	VSS[96]	VSS_NCTF[6]
G27	VSS[97]	VSS_NCTF[7]
G5	VSS[98]	VSS_NCTF[8]
H2	VSS[99]	VSS_NCTF[9]
H23	VSS[100]	VSS_NCTF[10]
H28	VSS[101]	VSS_NCTF[11]
H29	VSS[102]	VSS_NCTF[12]

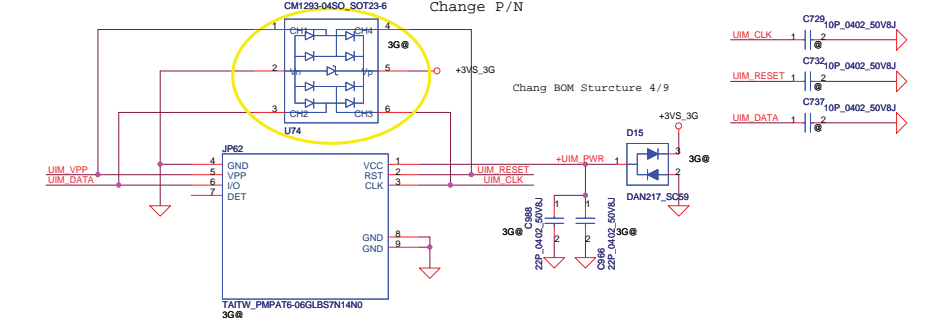
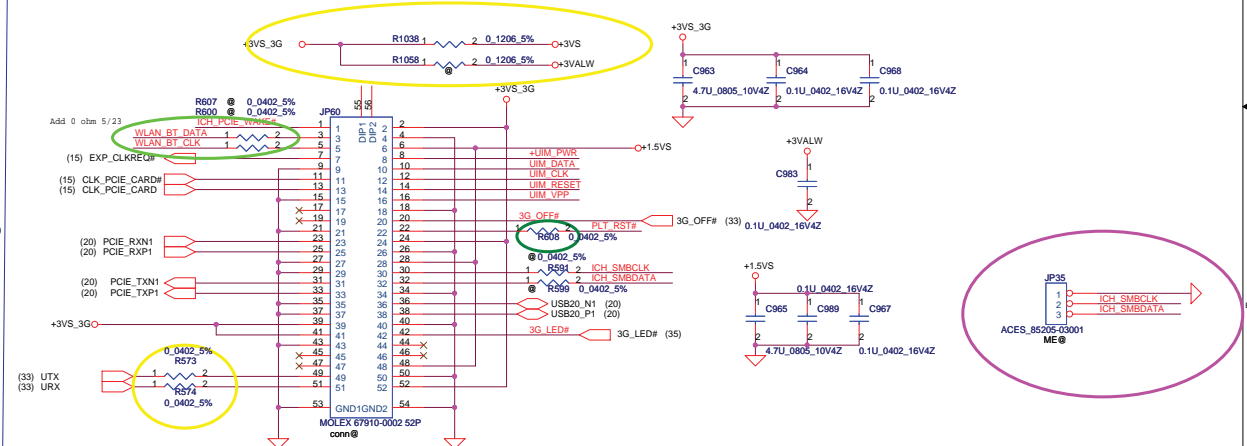
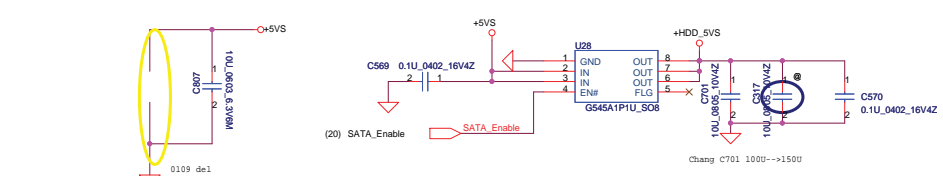
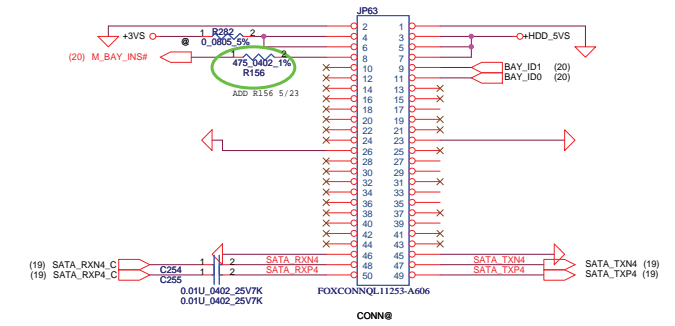
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Issued Date	2007/09/29	Deciphered Date
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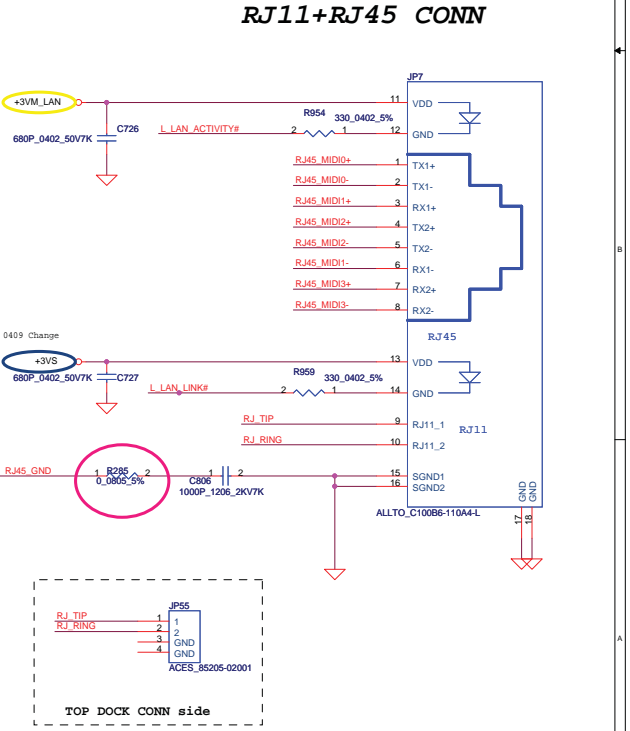
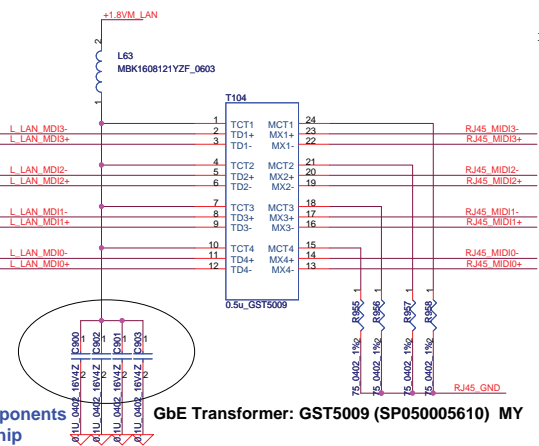
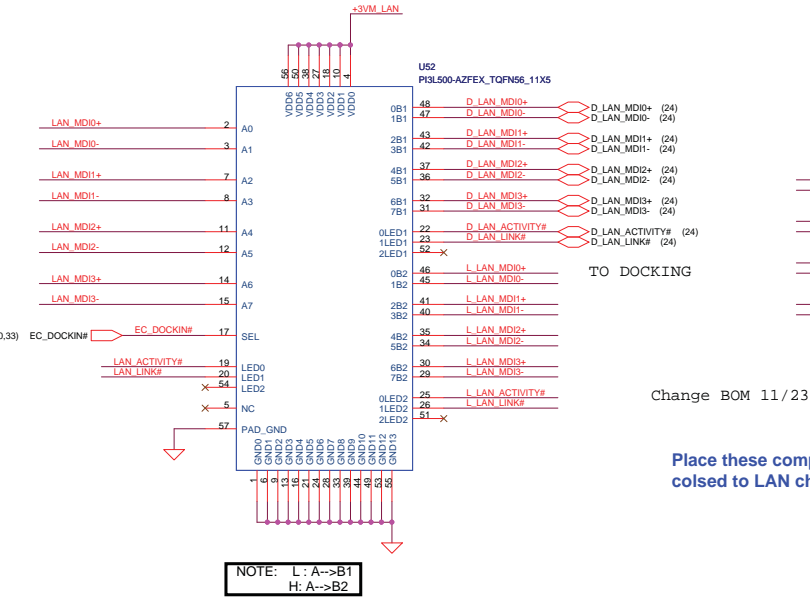
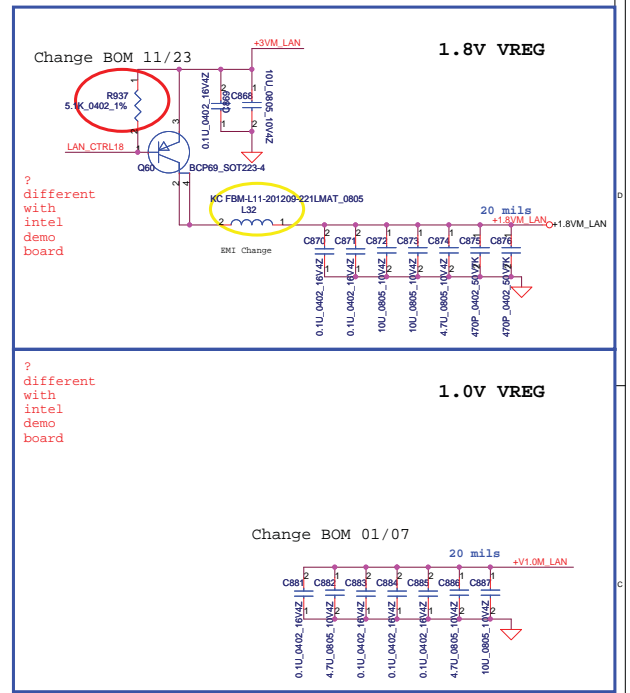
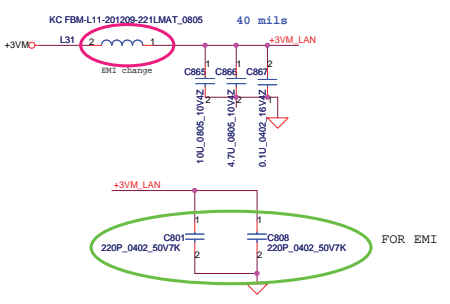
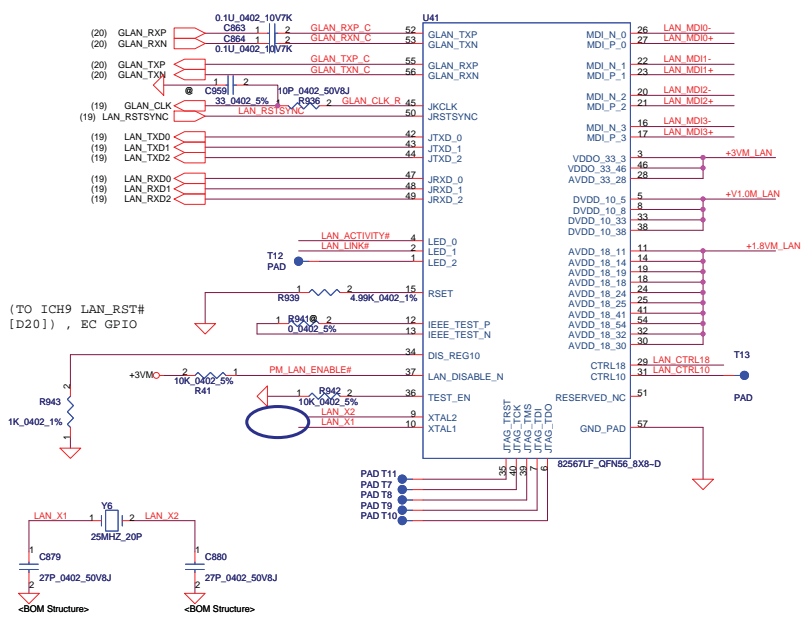
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SCHEMATIC, M/B A4311		
Title	Document Number	Rev
	401559	B
Date:	Friday, July 04, 2008	Sheet
		21 of 44

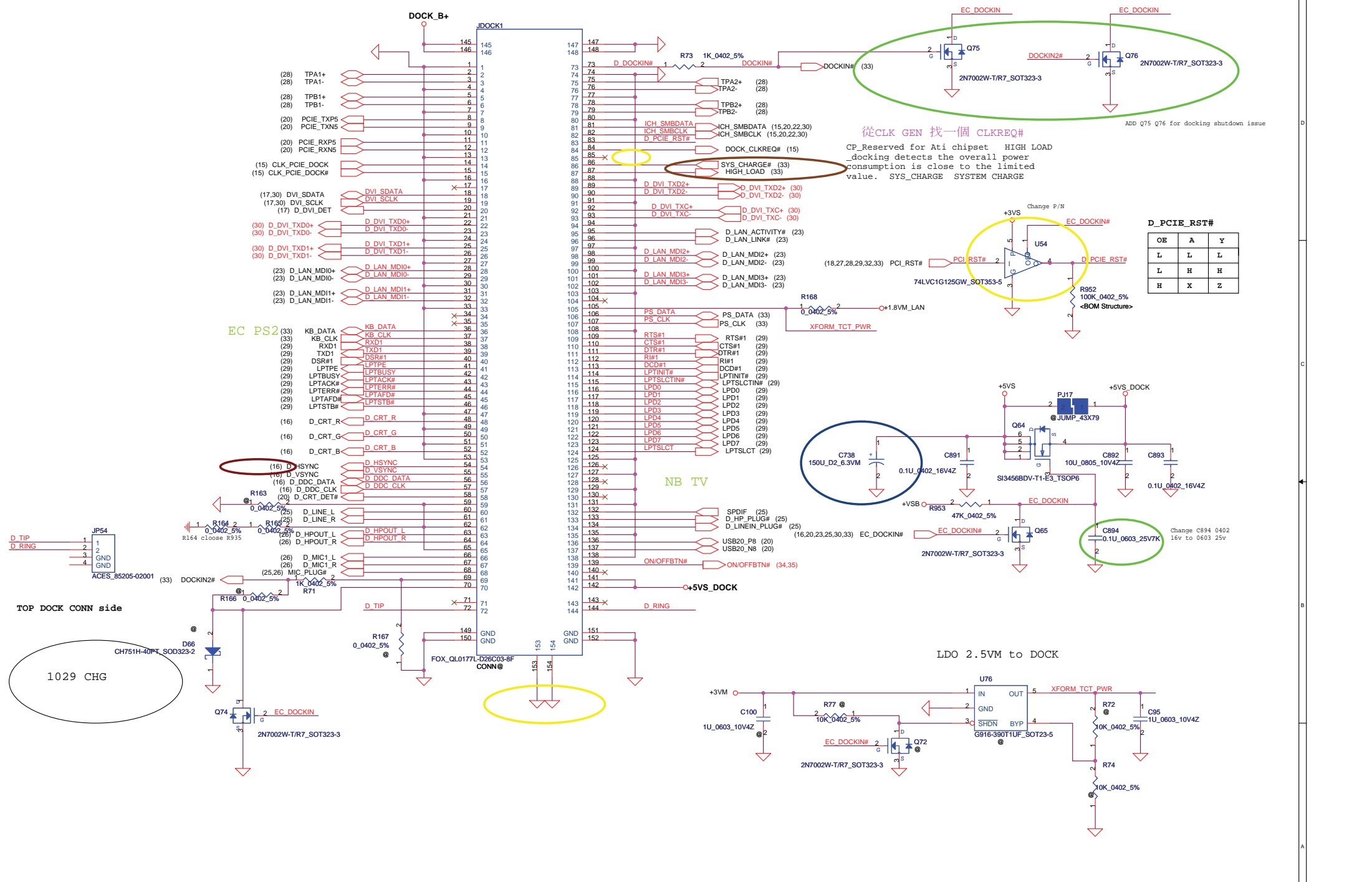
HDD Connector



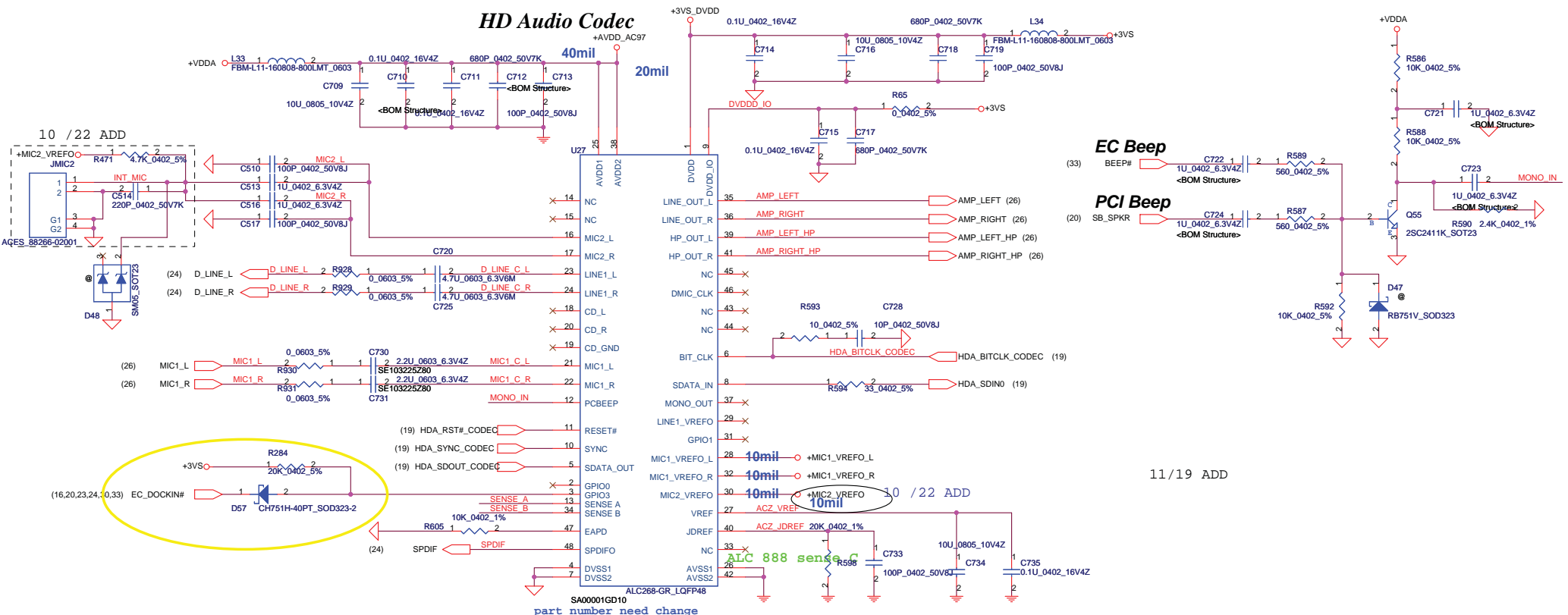
Media BAY for 2ND HDD BATT



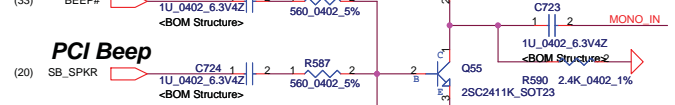




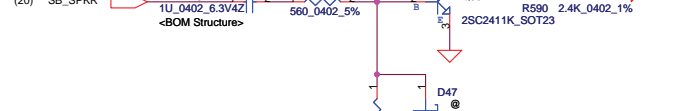
HD Audio Codec



EC Beep



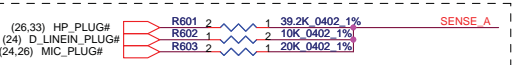
PCI Beep



10 / 22 ADD

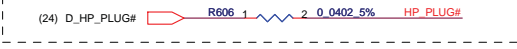
11/19 ADD

268 did not have sense C ! How can I know SPDIF IN OR HP IN ??



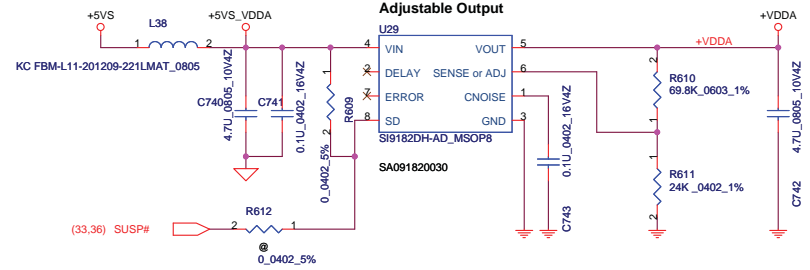
10 / 22 ADD

From Docking



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
SENSE B	5.1K	PORT-D (PIN 35, 36)
	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
SENSE C	5.1K	PORT-H (PIN 45, 46)
	39.2K	CD
	20K	1st S/PDIF Out
	10K	2nd S/PDIF Out
	5.1K	S/PDIF-IN

Regulator for CODEC



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Issued Date	2007/09/29	Deciphered Date
		2007/09/29

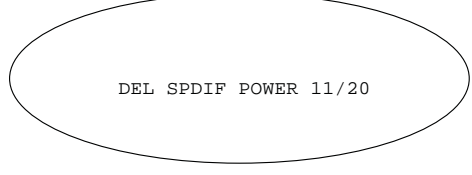
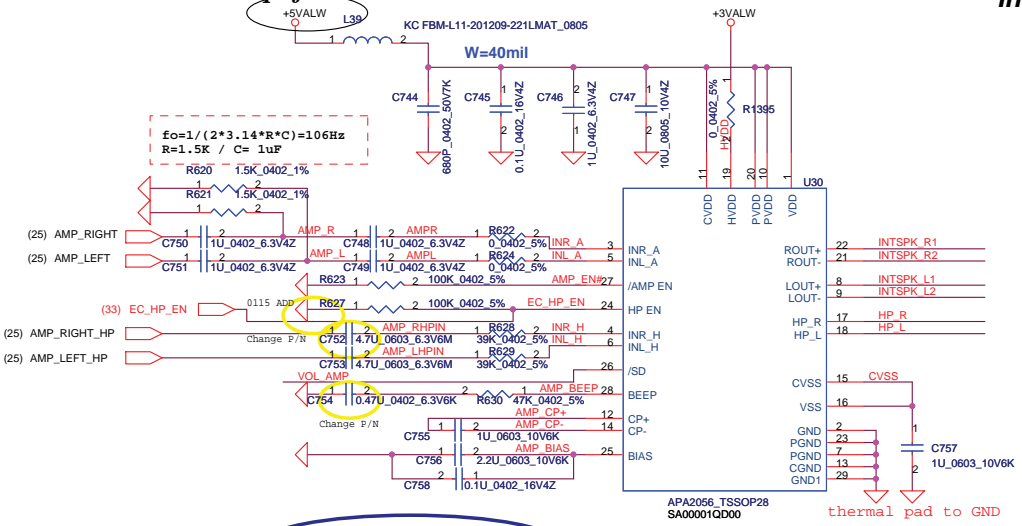
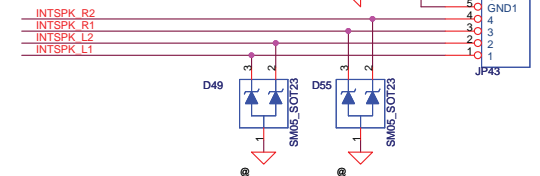
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Title		
SCHEMATIC, M/B A4311		
Size	Document Number	Rev
Custor	401559	B
Date:	Friday, July 04, 2008	Sheet 25 of 44

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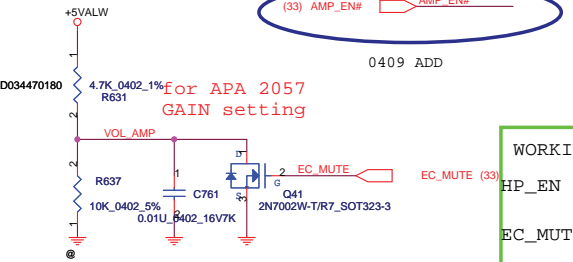
APA2056 SPK/HP Amplifier

Int. Speaker Conn.

20mil



LINE Out/Headphone Out S/PDIF Out JACK

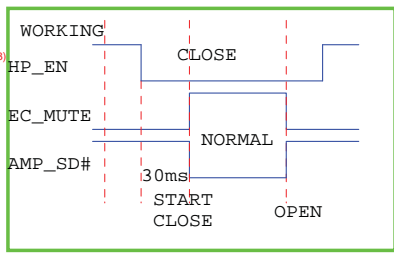


IN_A Gain = 10dB (Internal Speaker)
IN_H Gain = 0dB (Headphone)

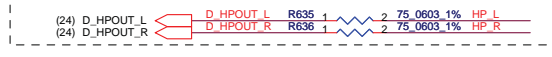
APA2057 gain setting table

gain (dB)	V	V(low)	V(high)
8		3.21	3.27
9		3.33	3.39
10		3.45	3.51

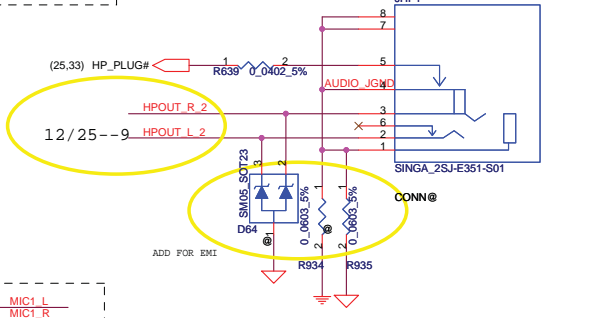
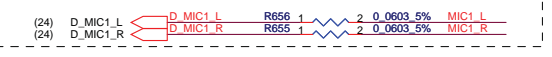
← current setting (3.48V)



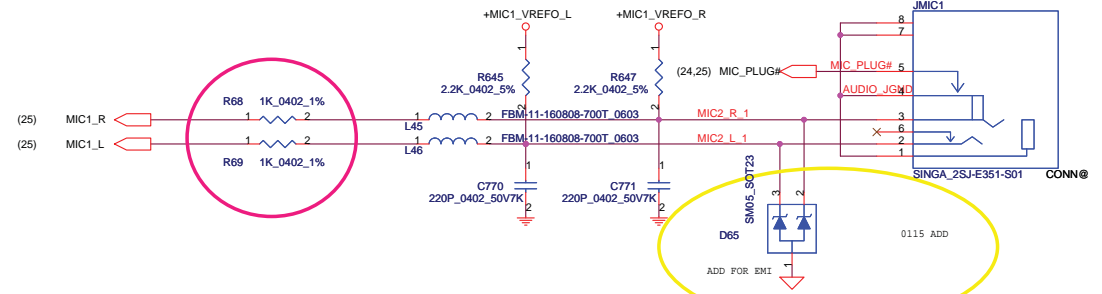
Docking Conn



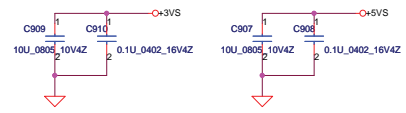
Docking Conn



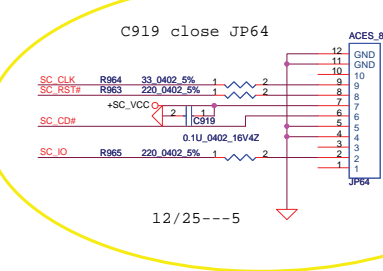
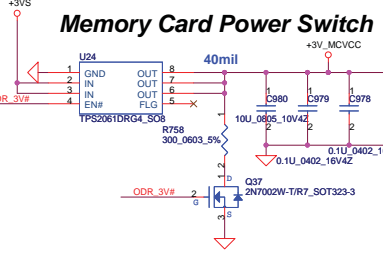
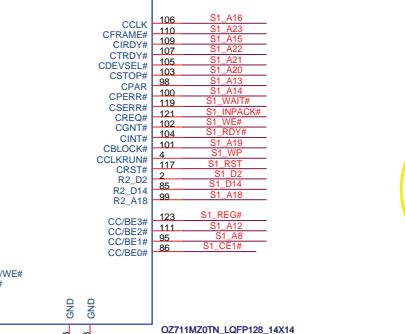
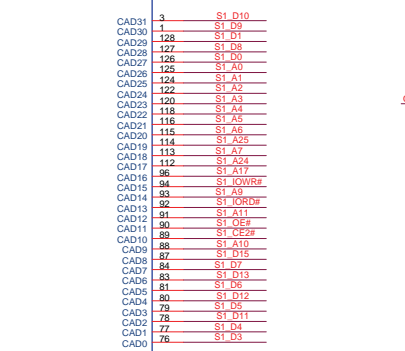
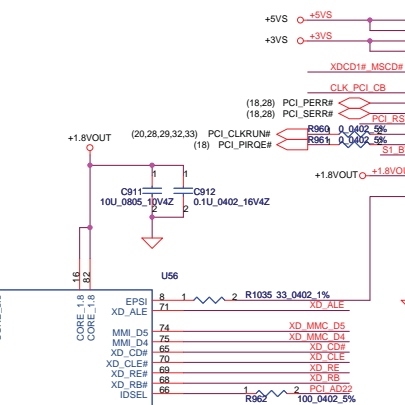
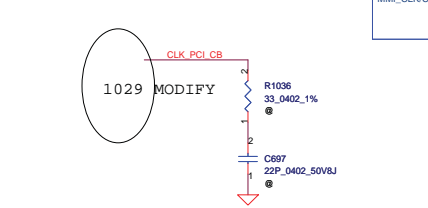
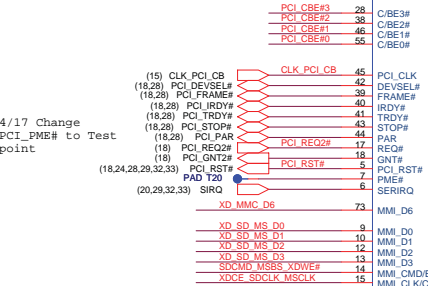
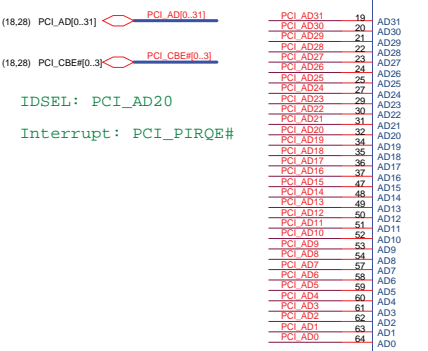
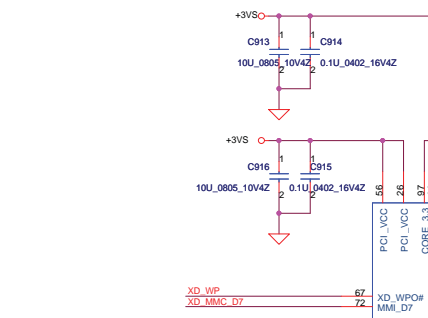
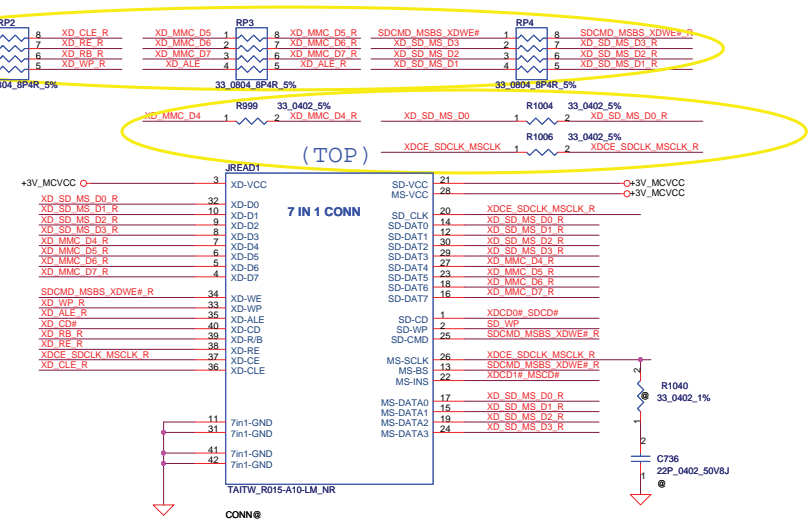
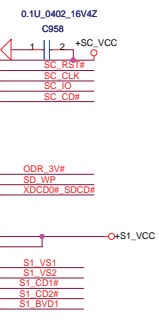
MIC JACK



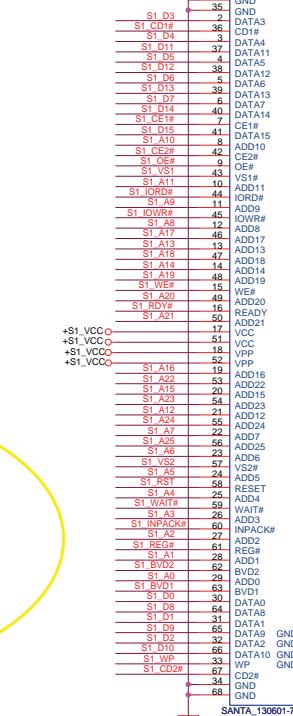
Change library U55/U56



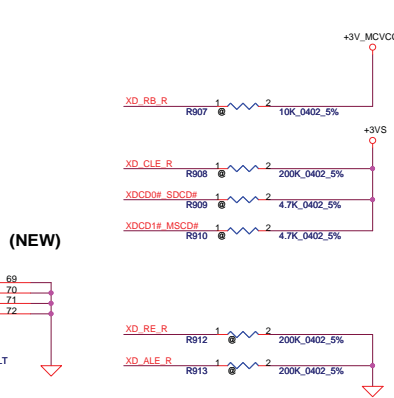
C958 close U55



PCMCIA Socket



MDIO PULL HIGH/LOW ?

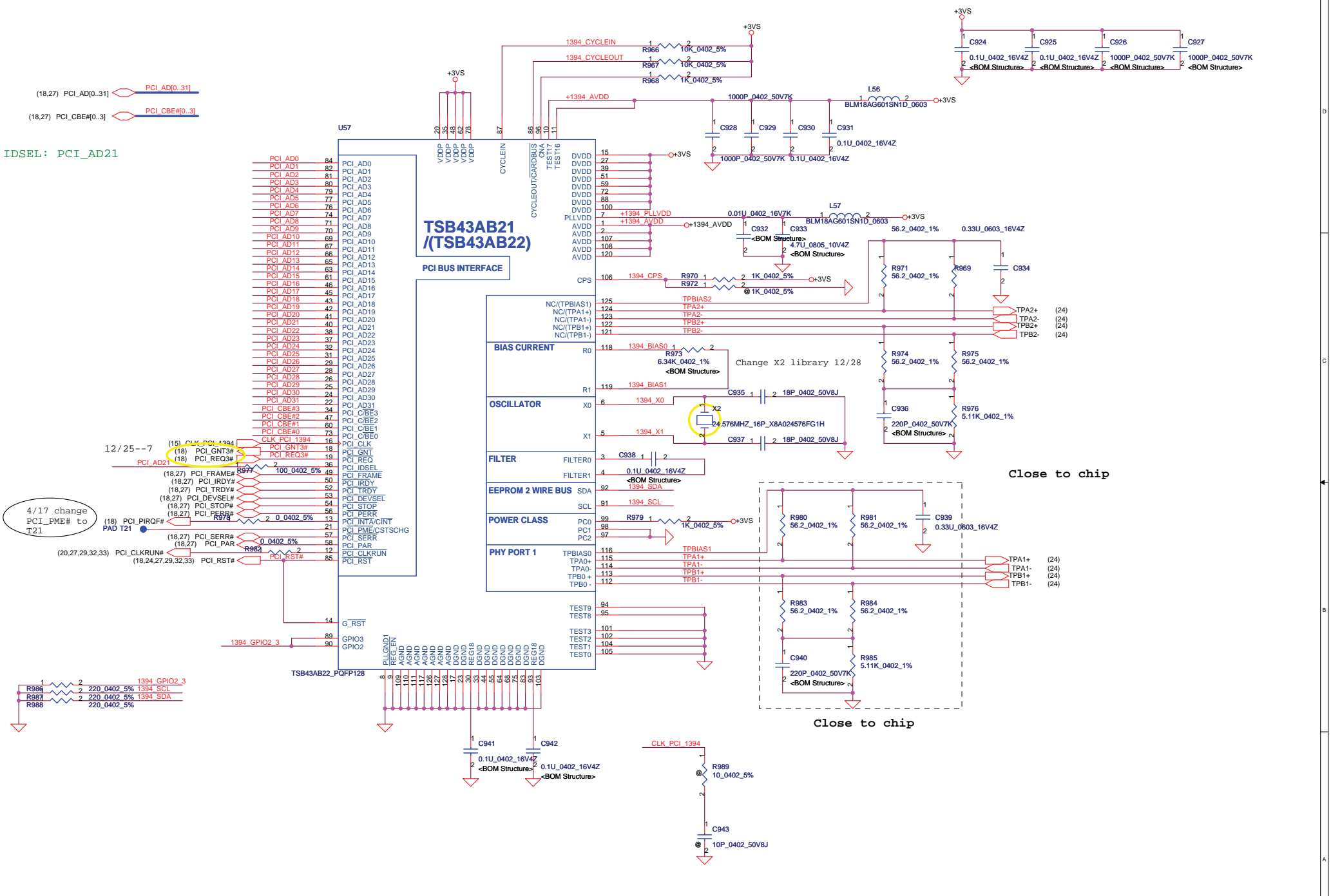


(NEW)

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Size	Document Number	401559		Rev
Date:	Friday, July 04, 2008	Sheet	27	of 44

IDSEL: PCI_AD21

(18.27) PCI_AD[0..31] PCI_AD0..31
(18.27) PCI_CBE#[0..3] PCI_CBE0..3



4/17 change PCI_PME# to T21

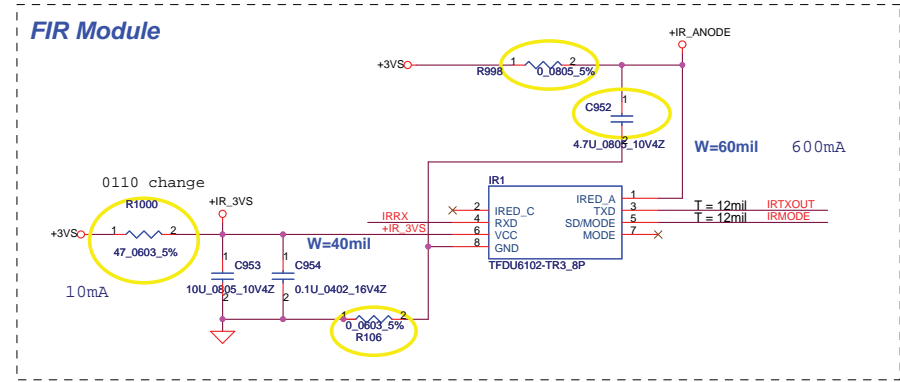
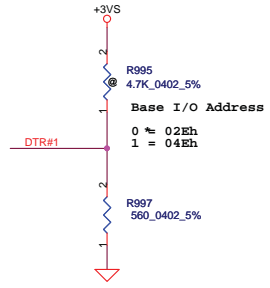
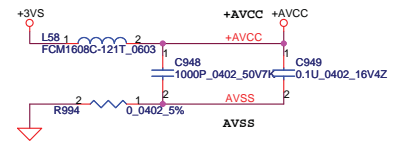
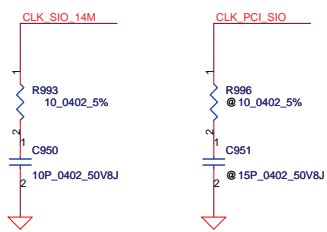
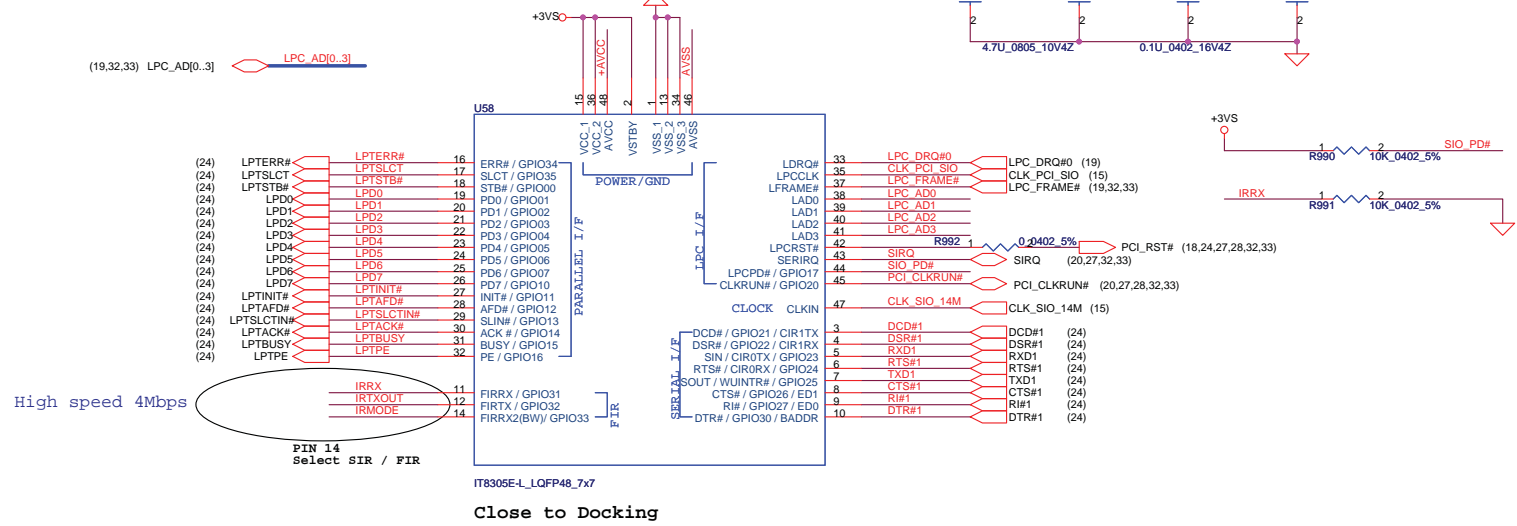
<http://hobi-elektronika.net>

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				401559	Rev B
Date:	Friday, July 04, 2008	Sheet	28	of 44	

SUPER I/O ITE IT8305E

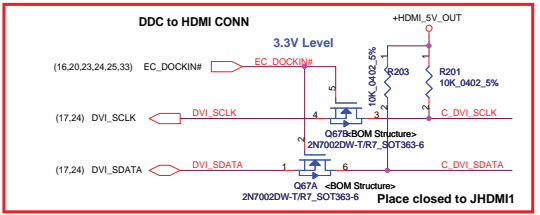
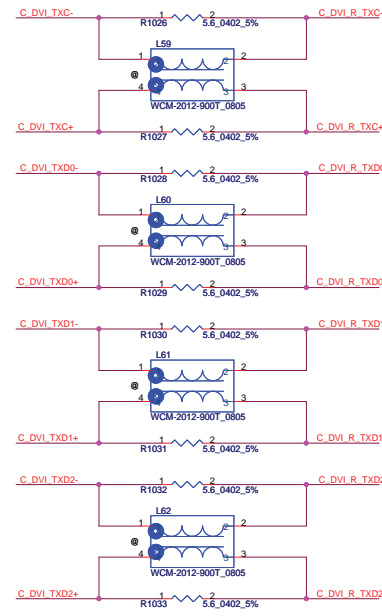
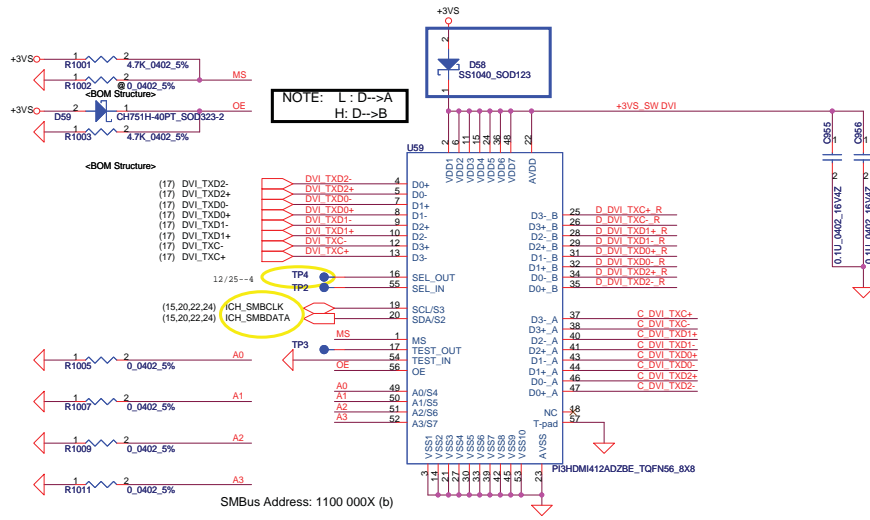
Note for pin 2:
 If needs to support power on from IT8305 CIR, please connect pin2 for "VSTBY".
 If don't need to support power on from IT8305 CIR, please connect pin2 for "V33".

From External CLK for 14.318MHz(default) or 48MHz

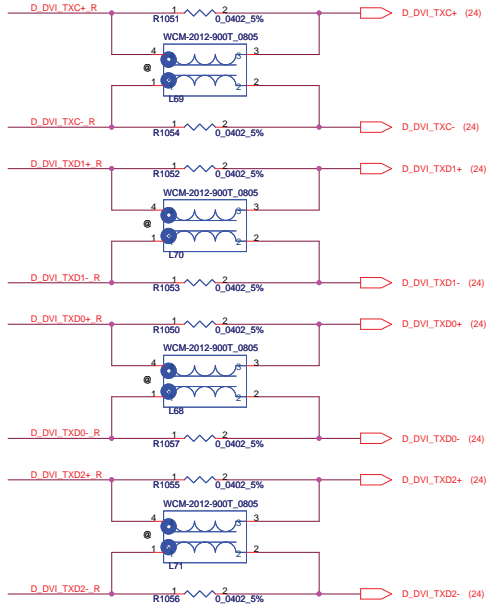
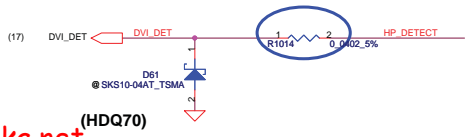
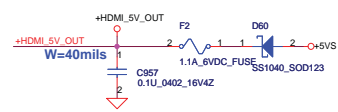
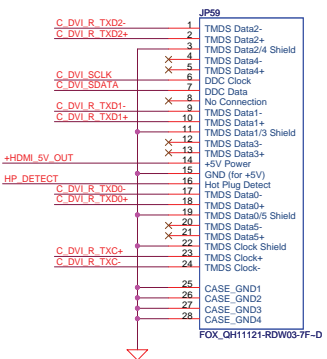


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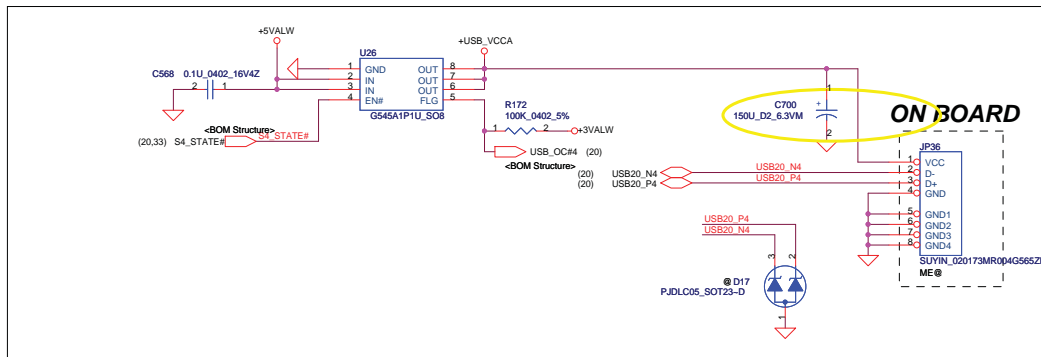
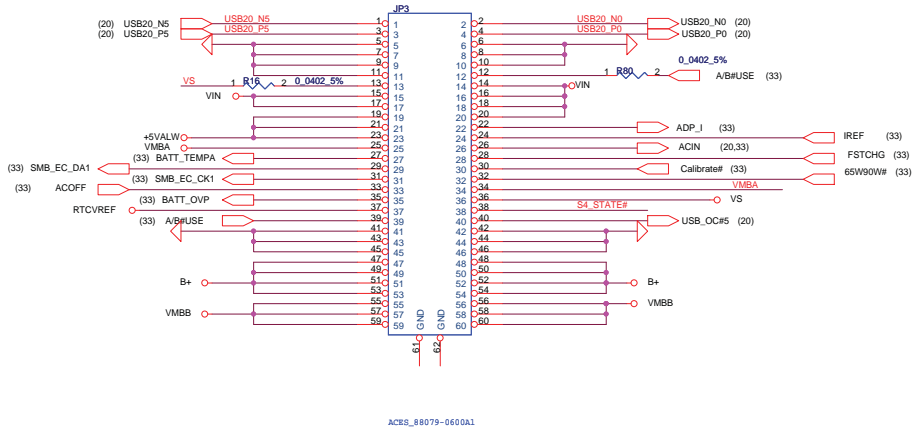
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Size	Document Number	Rev
Custort	401539	B
Date:	Friday, July 04, 2008	Sheet 29 of 44



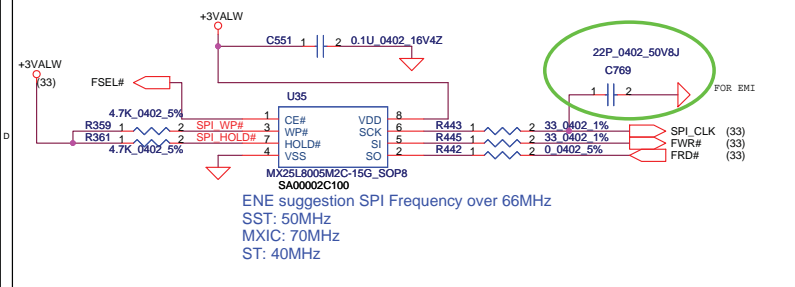
DVI-D Connector



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Size	C	Document Number	401559	Rev	B
Date:	Friday, July 04, 2008	Sheet	30	of	44



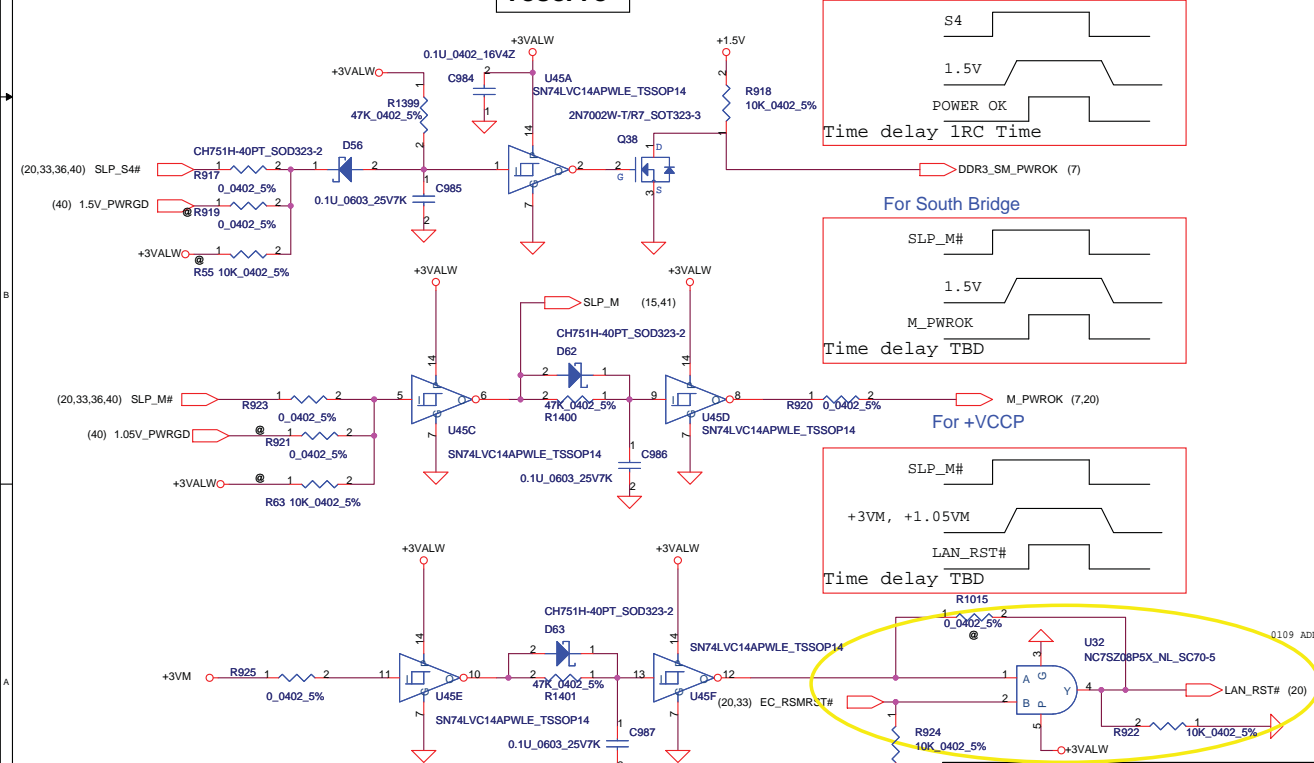
BIOS



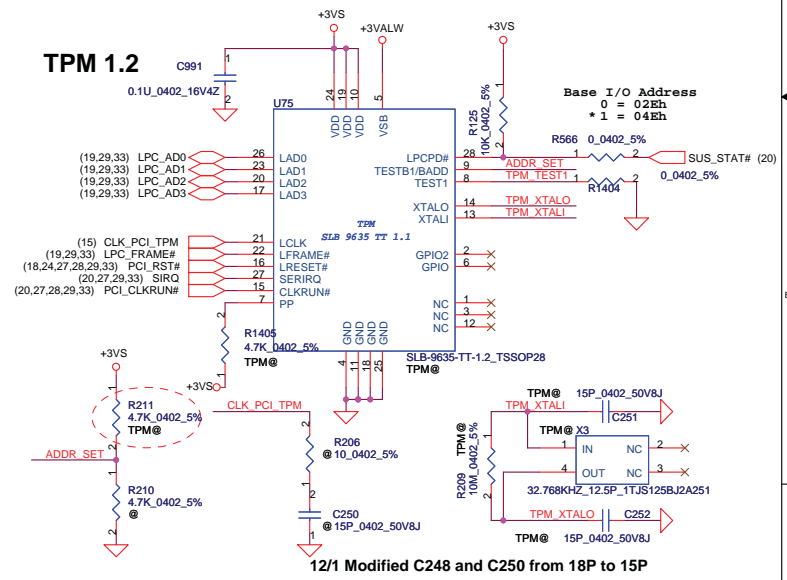
0115 DEL

Power ON Circuit

reserve

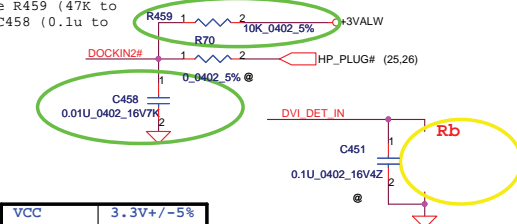
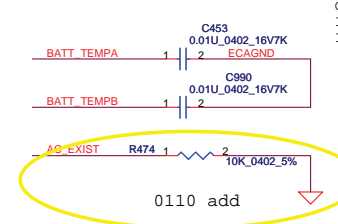
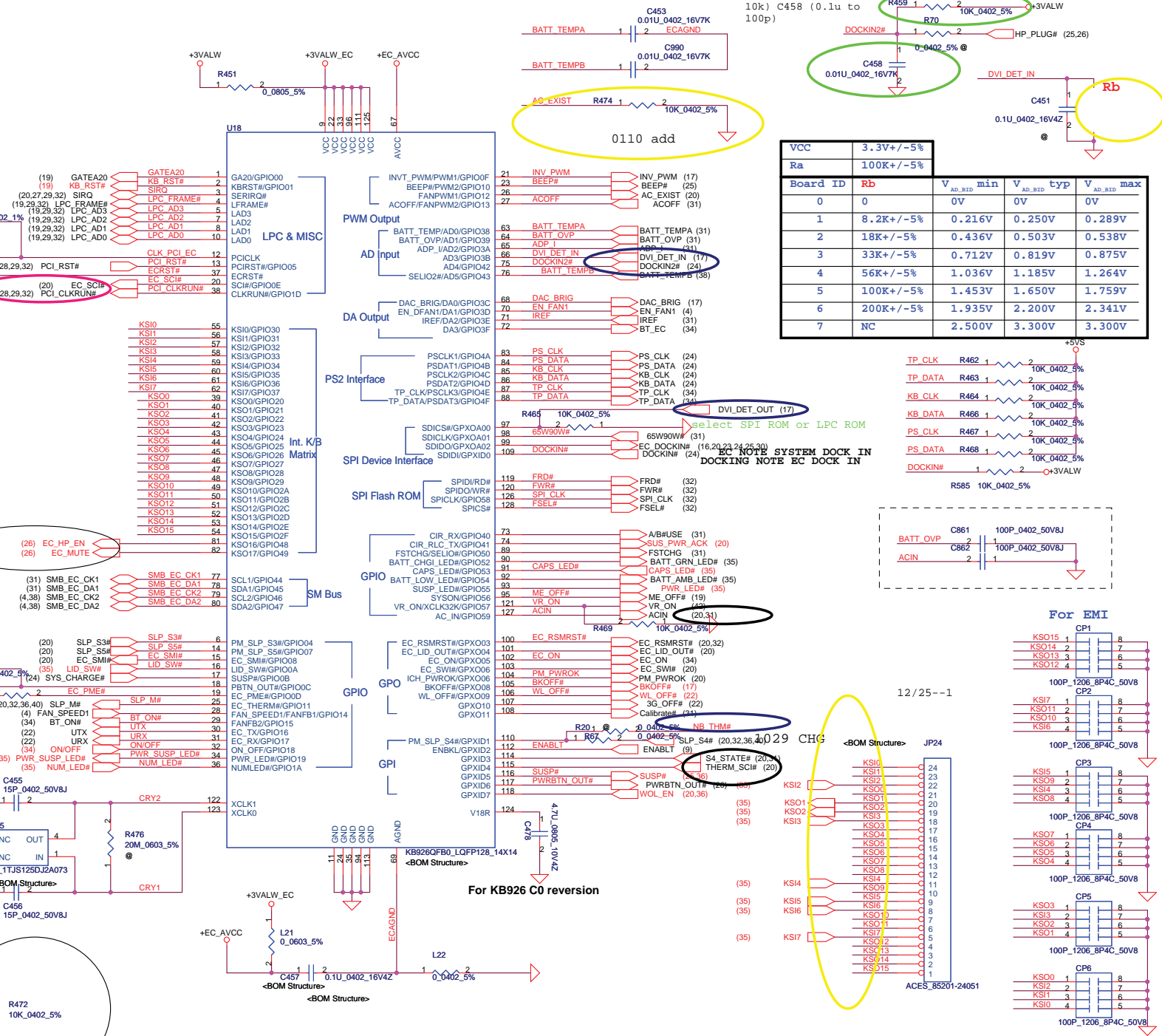
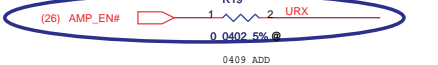
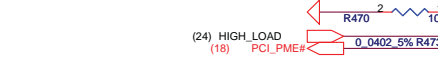
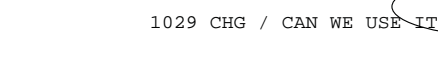
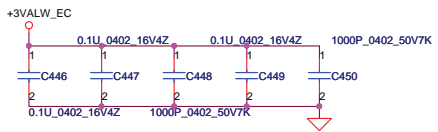


TPM 1.2

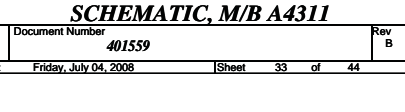
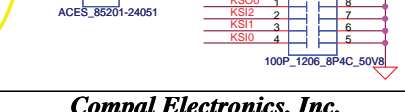
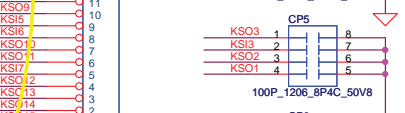
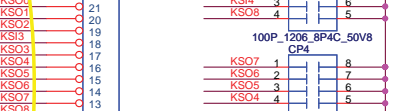
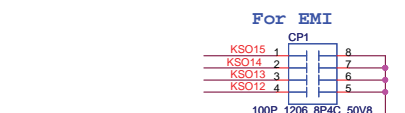
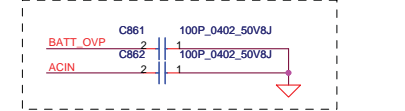
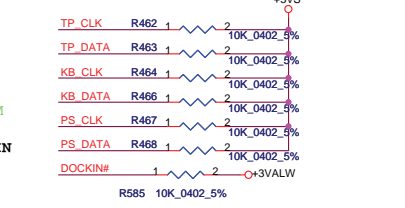


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SCHEMATIC, M/B A4311			
Size	Document Number	Rev	
	401559	B	
Date:	Friday, July 04, 2008	Sheet	32 of 44



VCC	3.3V+/-5%			
Ra	100K+/-5%			
Board ID	Rb	V _{AD_BTD} min	V _{AD_BTD} typ	V _{AD_BTD} max
0	0	0V	0V	0V
1	8.2K+/-5%	0.216V	0.250V	0.289V
2	18K+/-5%	0.436V	0.503V	0.538V
3	33K+/-5%	0.712V	0.819V	0.875V
4	56K+/-5%	1.036V	1.185V	1.264V
5	100K+/-5%	1.453V	1.650V	1.759V
6	200K+/-5%	1.935V	2.200V	2.341V
7	NC	2.500V	3.300V	3.300V

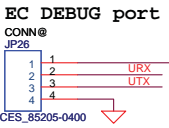


1029 CHG / CAN WE USE IT ?

12/25--1

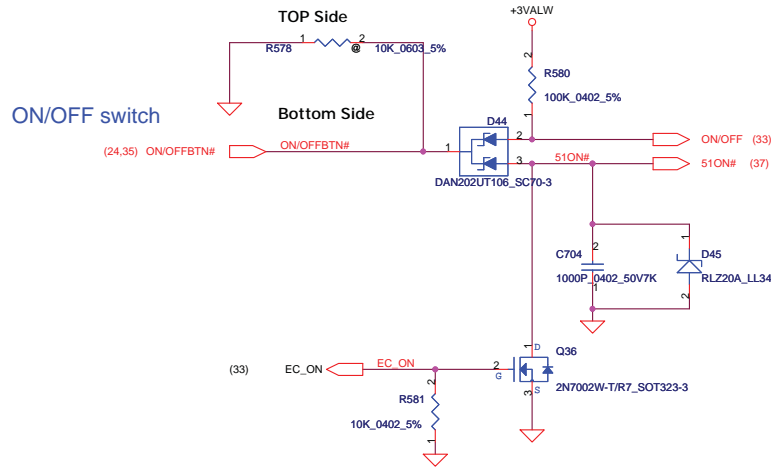
CHG

For KB926 C0 reversion

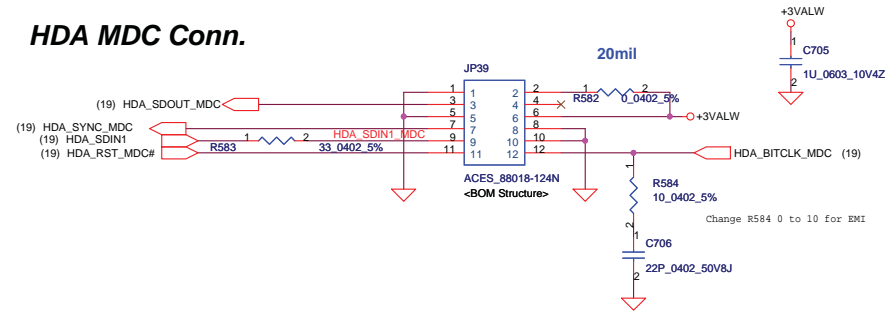


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Size	Document Number	Date	Sheet	Rev
	401559	Friday, July 04, 2008	33	B

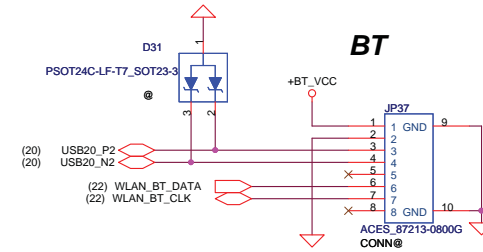
Power Button



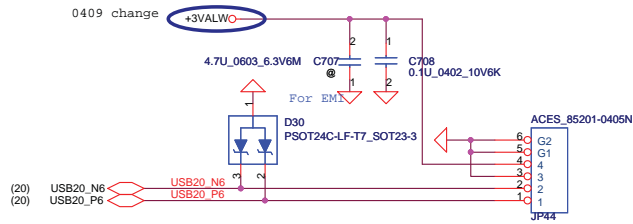
HDA MDC Conn.



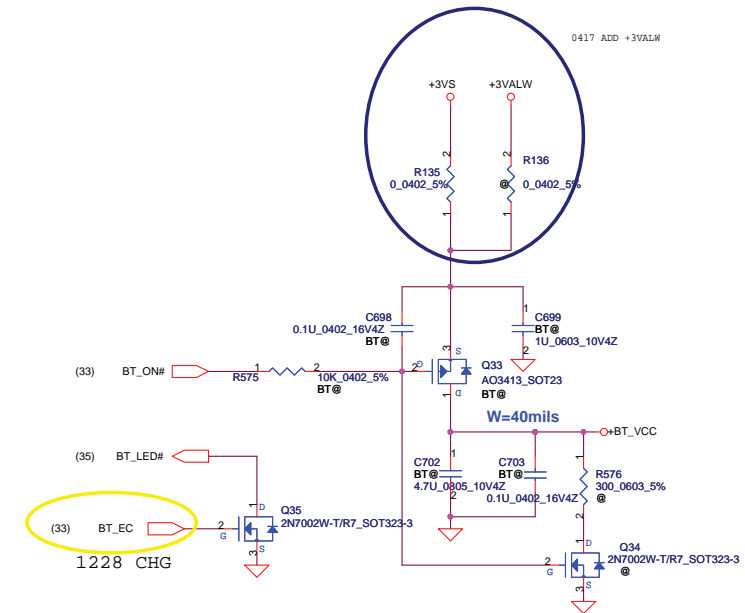
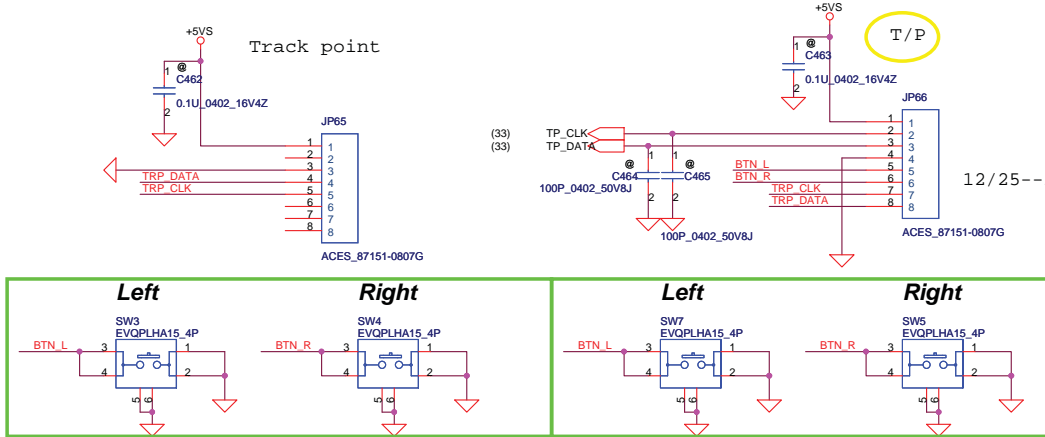
BT



Finger Print Conn

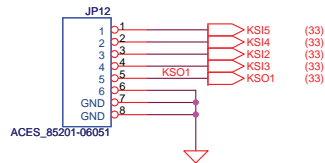


CHECK CONN

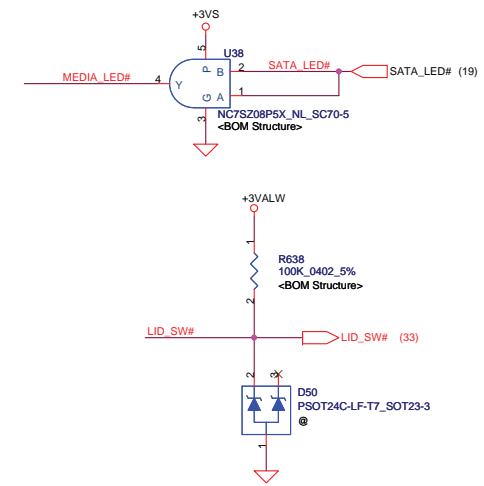
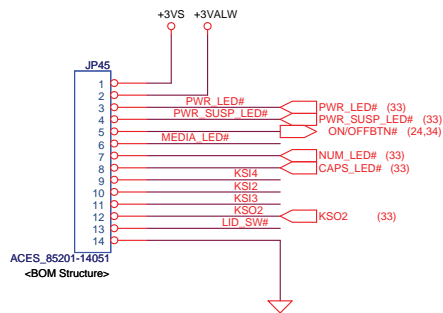


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Size		Document Number		Rev	
		401559		B	
Date:		Friday, July 04, 2008		Sheet 34 of 44	

TO S/W B



TO POWER BTN/B

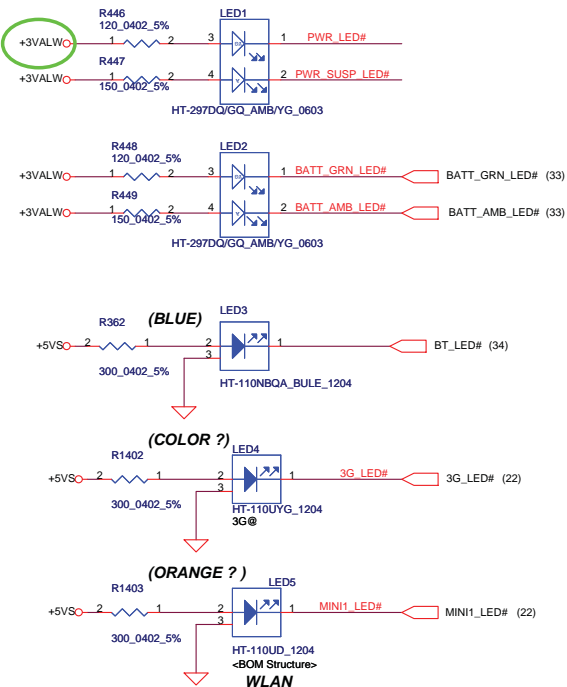
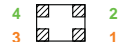


	KSO1	KSO2
KSI2	SYNC_BTN#	EMAIL_BTN#
KSI3	BRIEF_BTN#	PROGRAM_BTN#
KSI4	LOCK_BTN#	IE_BTN#
KSI5	E-KEY_BTN#	
KSI6		3G ON#
KSI7	WL ON#	BT ON#

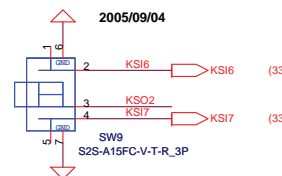
0103 Change1

Change +3vs to +3valw

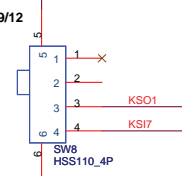
Compal Footprint



BT_SW & 3G_SW



WL_SW

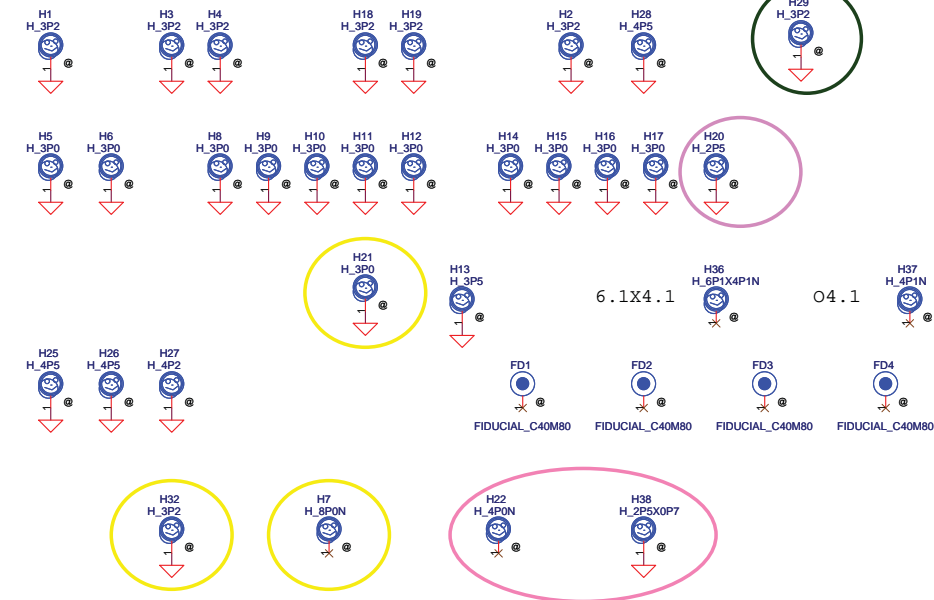


06 03.2

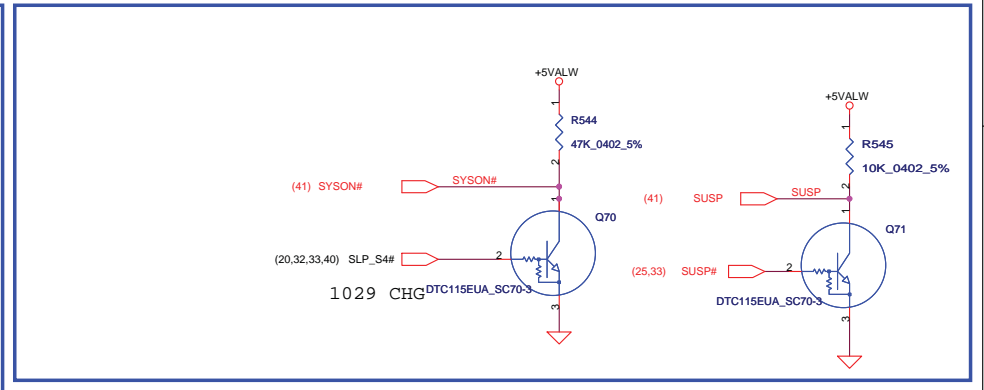
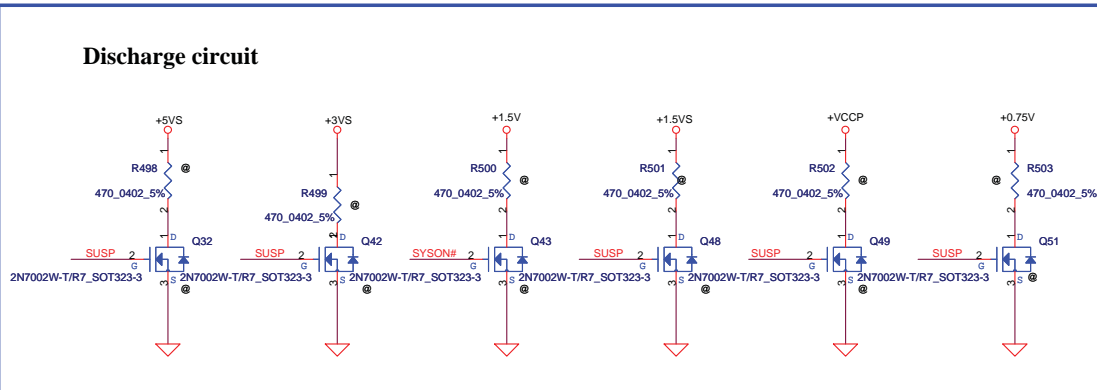
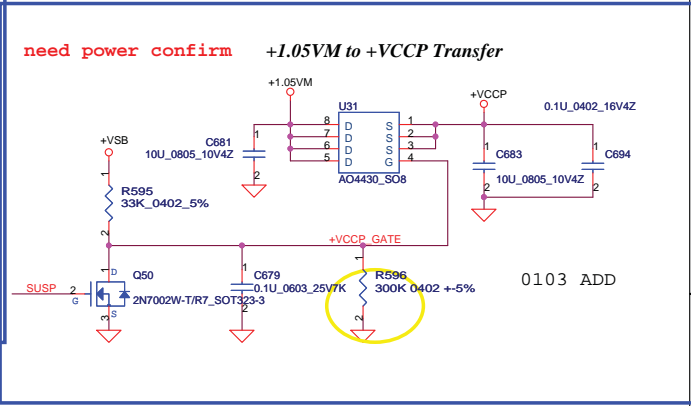
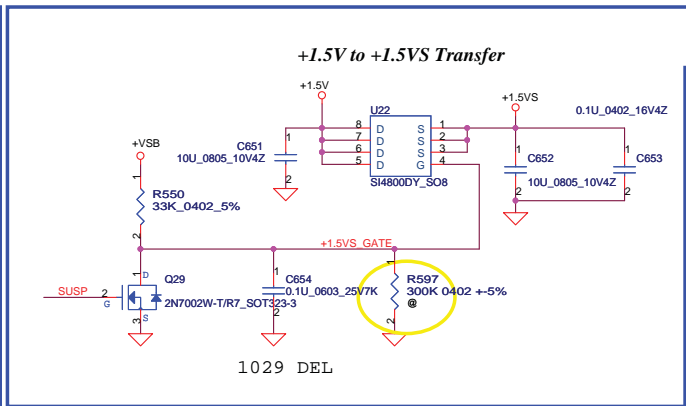
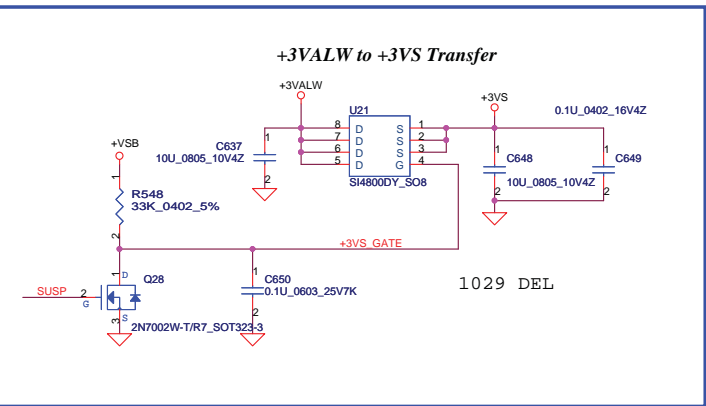
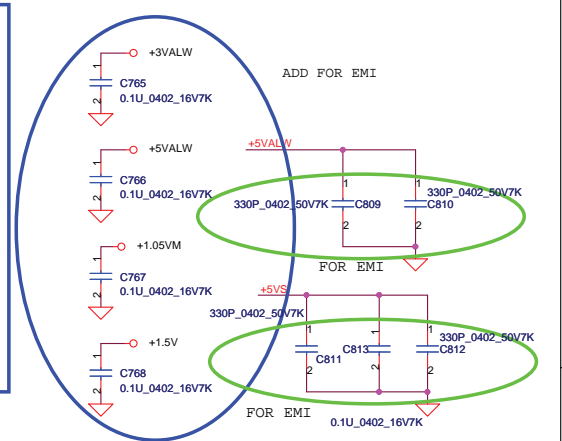
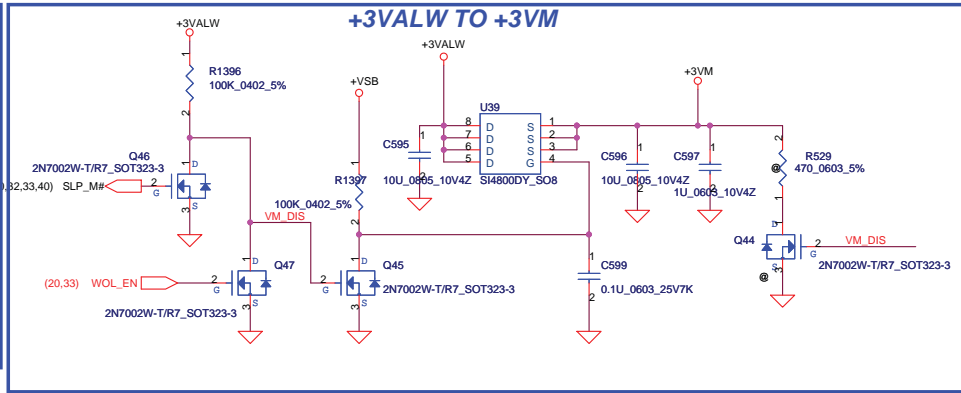
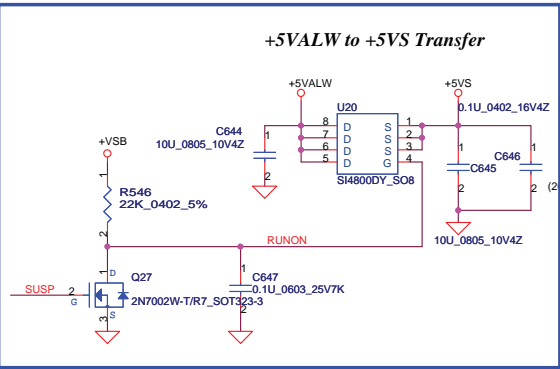
9 X 9 03

04.2

02.5



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Size	Document Number	401559	Rev	B	
Date:	Friday, July 04, 2008	Sheet	35	of 44	

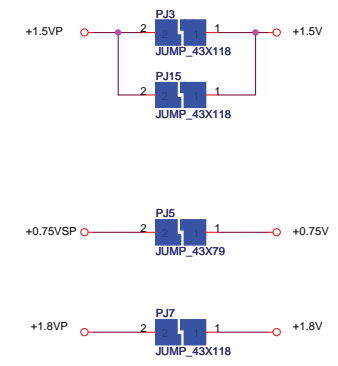
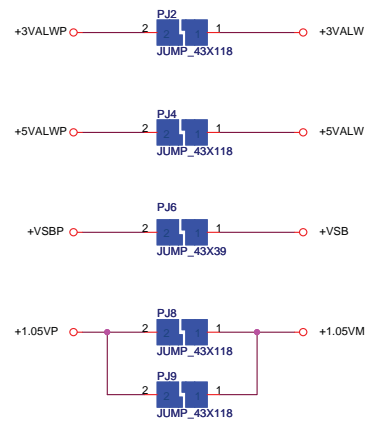
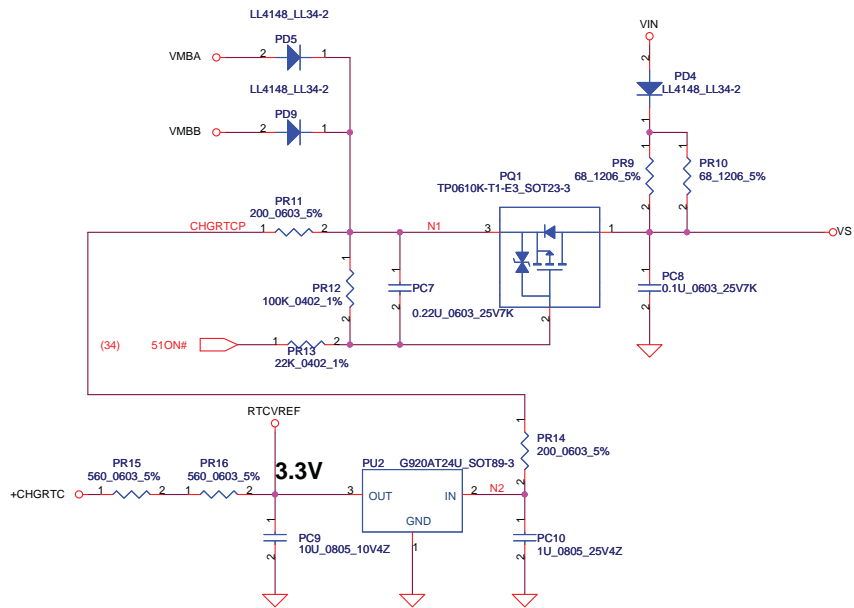
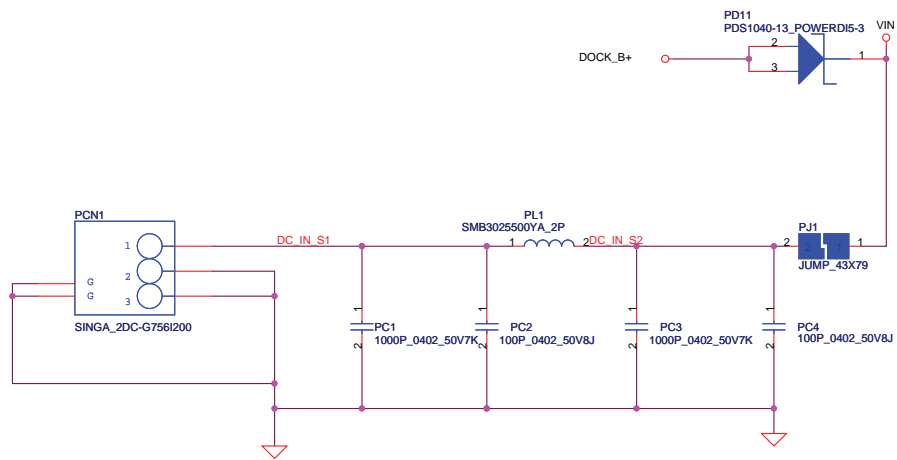


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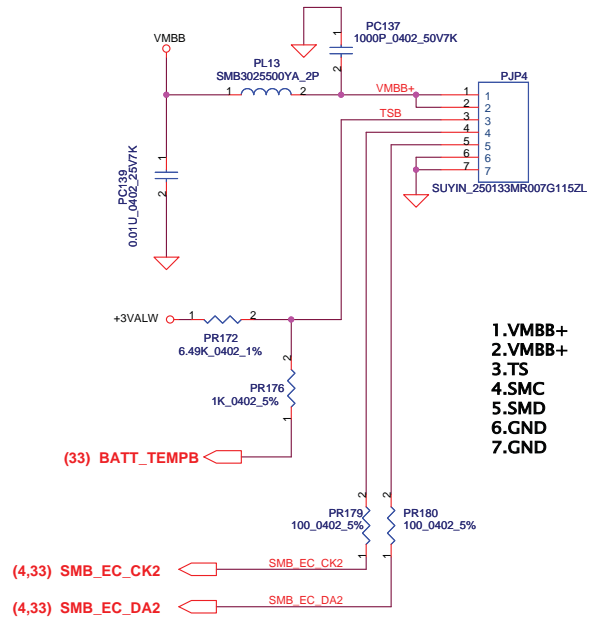
Size	Document Number	Rev
	401559	B
Date:	Friday, July 04, 2008	Sheet 36 of 44



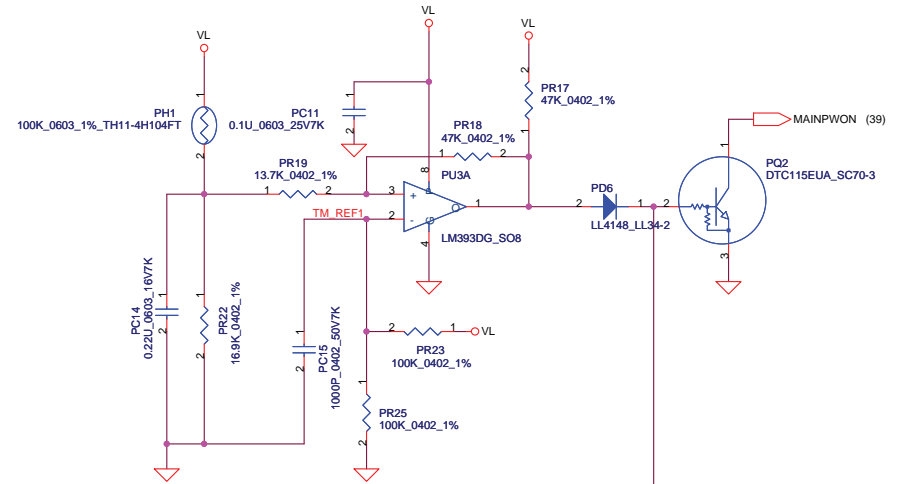
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					401559	B
				Date:	Friday, July 04, 2008	Sheet 37 of 44

PH1 under CPU botten side :

CPU thermal protection at 86 degree C
Recovery at 56 degree C

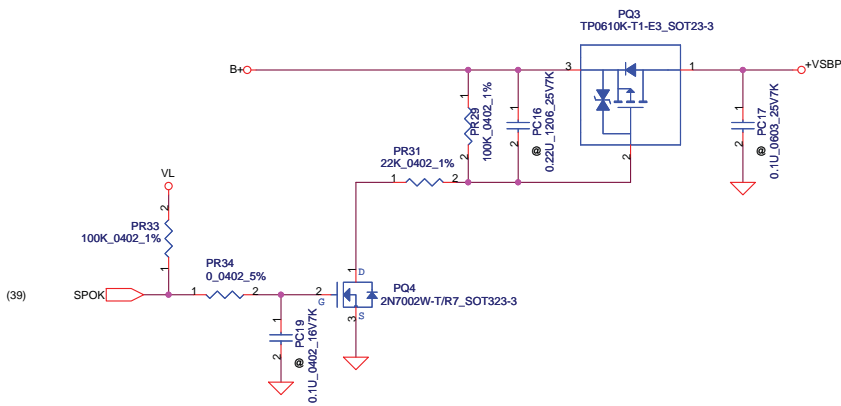
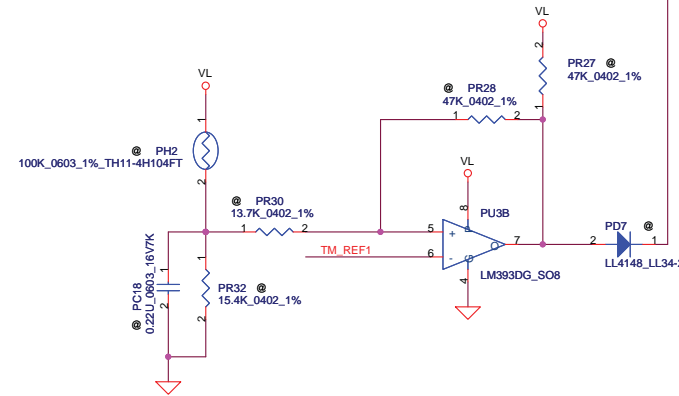


- 1.VMBB+
- 2.VMBB+
- 3.TS
- 4.SMC
- 5.SMD
- 6.GND
- 7.GND

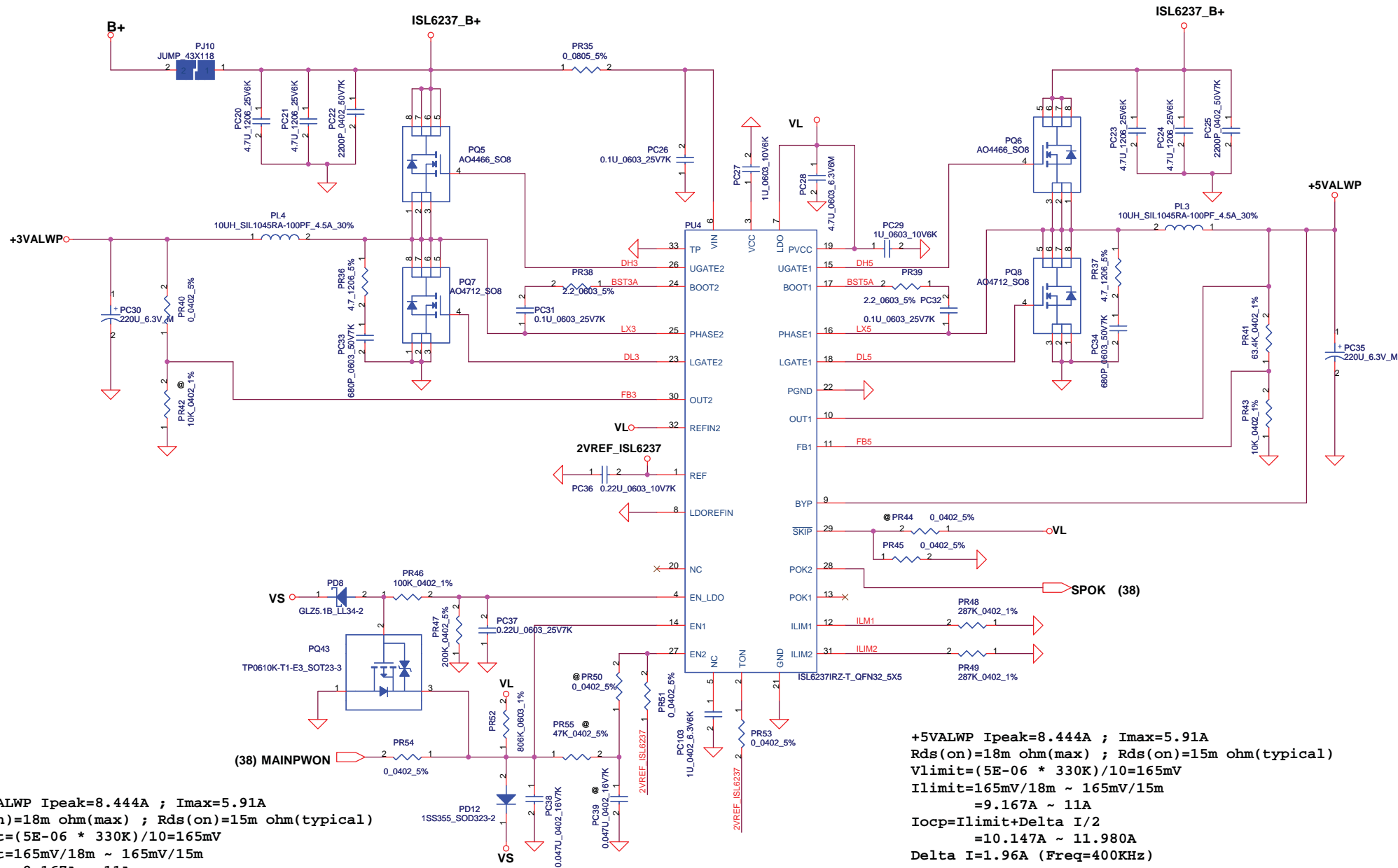


PH2 near main Battery CONN :

BAT. thermal protection at 92 degree C
Recovery at 56 degree C



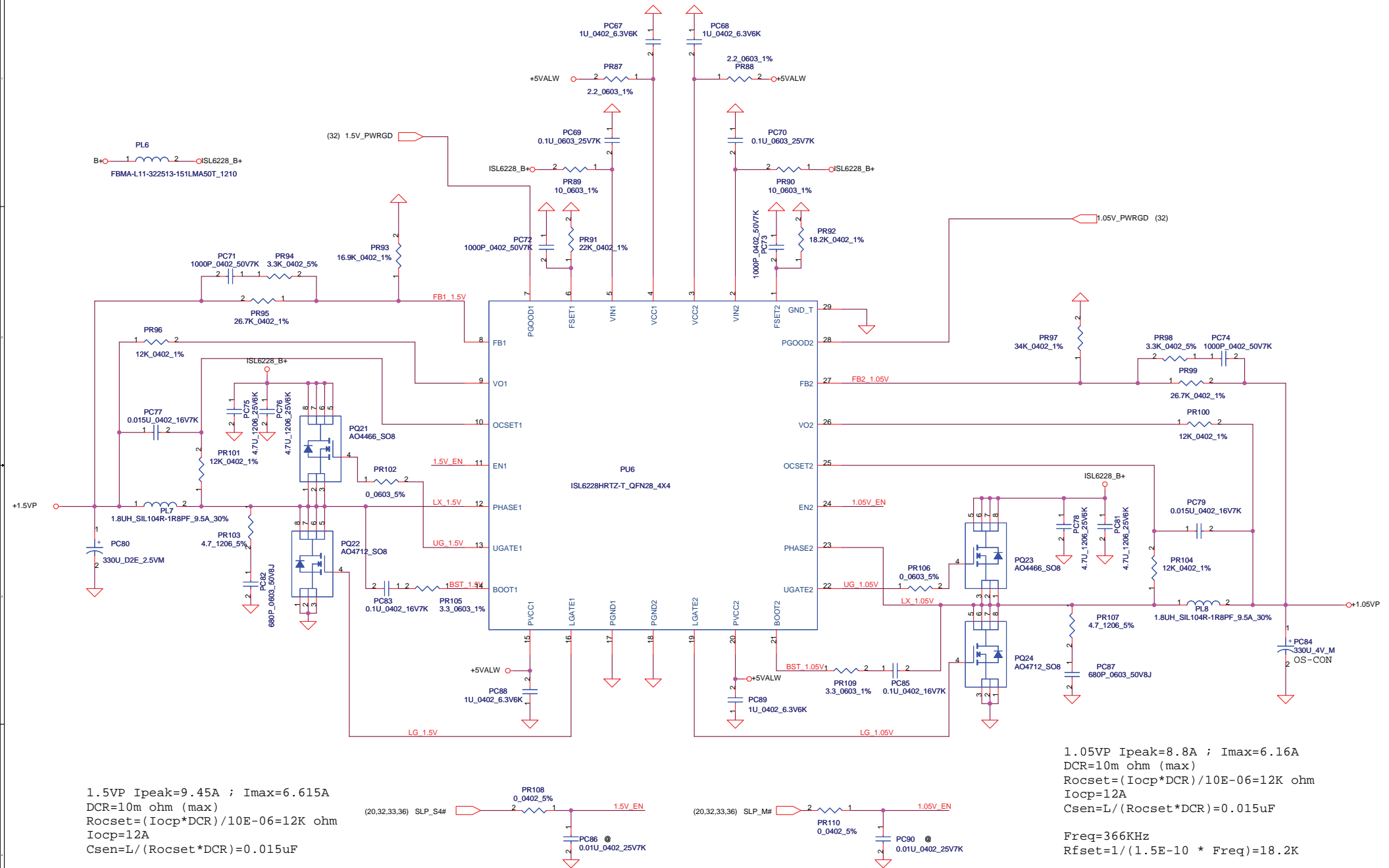
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Size	Document Number	401559		Rev	B
Date:	Friday, July 04, 2008	Sheet	38	of	44



+3.3VALWP Ipeak=8.444A ; Imax=5.91A
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(5E-06 * 330K)/10=165mV
 Ilimit=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A
 Iocp=Ilimit+Delta I/2
 =10.134A ~ 11.967A
 Delta I=1.934A (Freq=300KHz)

+5VALWP Ipeak=8.444A ; Imax=5.91A
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(5E-06 * 330K)/10=165mV
 Ilimit=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A
 Iocp=Ilimit+Delta I/2
 =10.147A ~ 11.980A
 Delta I=1.96A (Freq=400KHz)

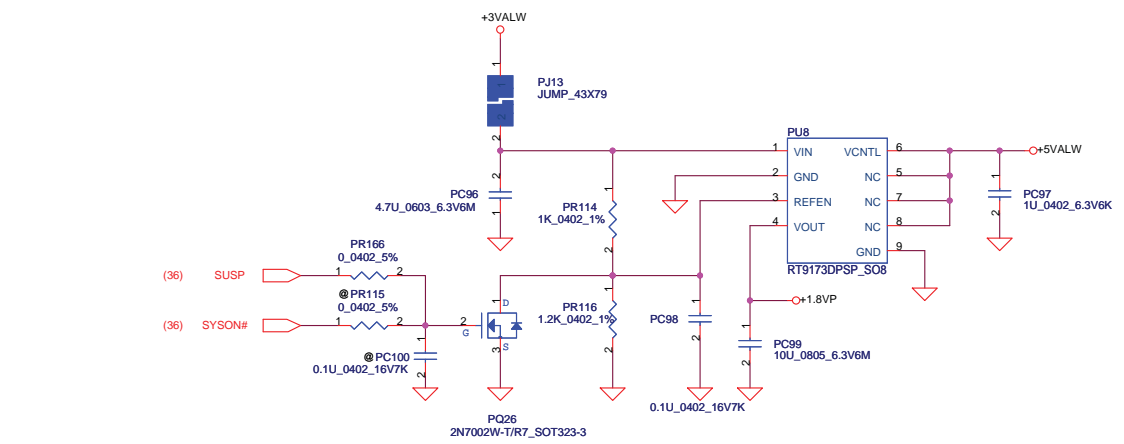
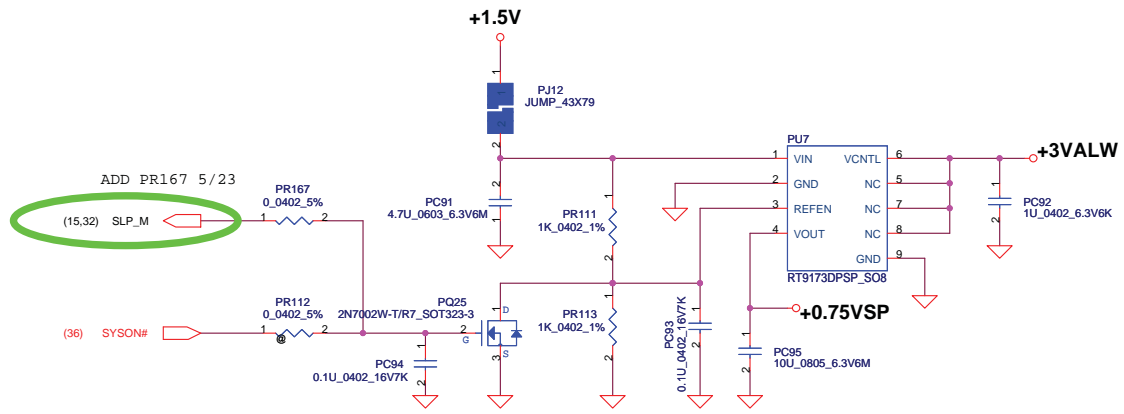
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Size	Document Number	Rev		B	
Custpm	401559				
Date:	Friday, July 04, 2008	Sheet	39	of	44



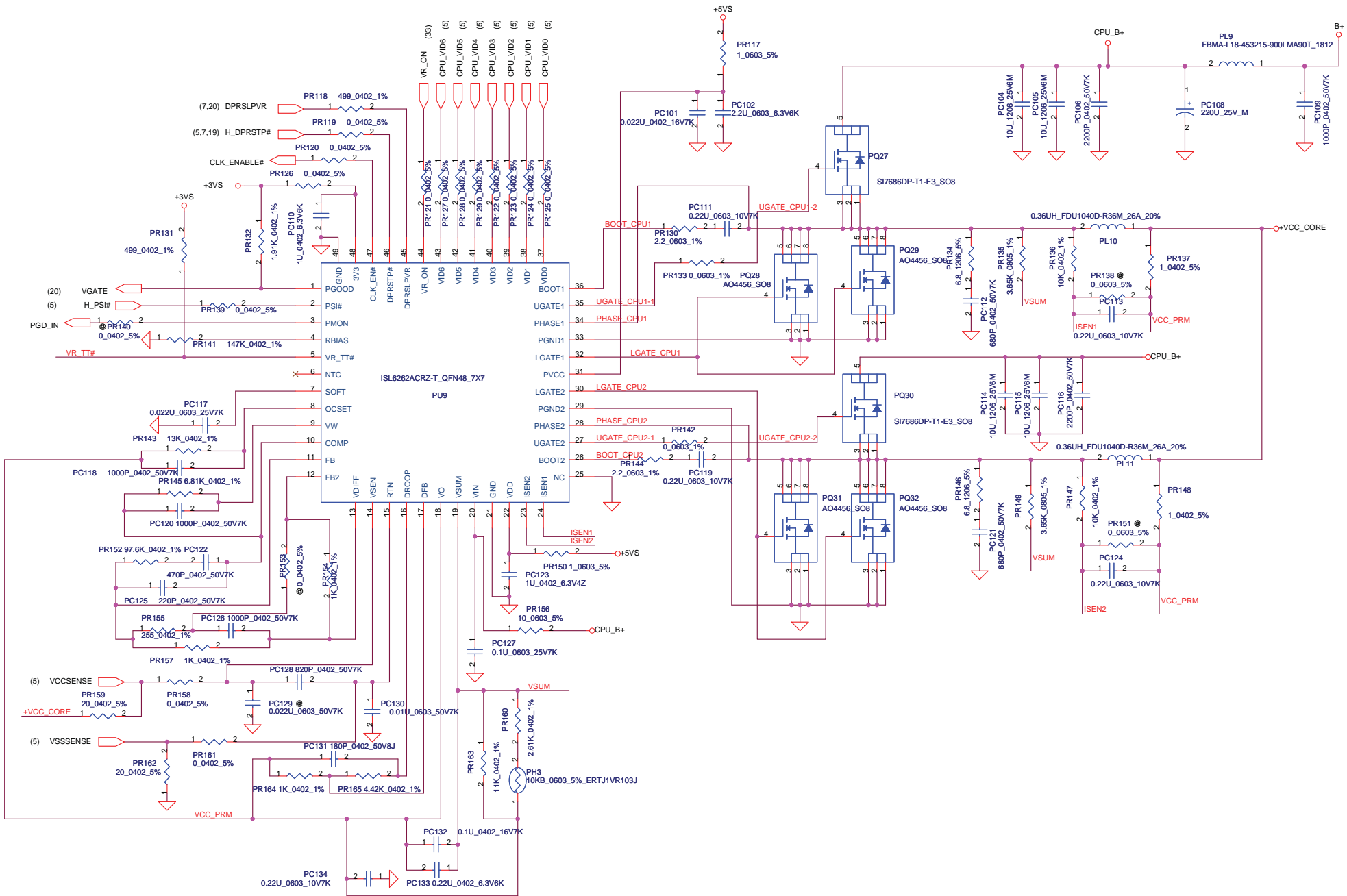
1.5VP Ipeak=9.45A ; Imax=6.615A
 DCR=10m ohm (max)
 $Rocset = (Iocp * DCR) / 10E-06 = 12K \text{ ohm}$
 $Iocp = 12A$
 $Csen = L / (Rocset * DCR) = 0.015uF$
 Freq=303KHz
 $Rfset = 1 / (1.5E-10 * Freq) = 22K$

1.05VP Ipeak=8.8A ; Imax=6.16A
 DCR=10m ohm (max)
 $Rocset = (Iocp * DCR) / 10E-06 = 12K \text{ ohm}$
 $Iocp = 12A$
 $Csen = L / (Rocset * DCR) = 0.015uF$
 Freq=366KHz
 $Rfset = 1 / (1.5E-10 * Freq) = 18.2K$

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Size	Document Number	401559		Rev	B
Date:	Friday, July 04, 2008	Sheet	40	of	44



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Size	Document Number			Rev	B
	401559				
Date:	Friday, July 04, 2008	Sheet	41	of	44



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Issued Date	2007/09/29	Deciphered Date	2007/09/29	Title	
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Size	Document Number	Rev		B	
	401559				
Date:	Friday, July 04, 2008	Sheet	42	of	44

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For 2nd source of ISL6237		39	Add PC103 SE000000K80(S CER CAP 1U 6.3V K X5R 0402) on Pin5 of PU4 to GND	2007 12/26	EVT
2		For EN function of PU4		39	Add PD12 SC100001K00(S DIO 1SS355 SOD323 T/R-5K)on pin 3 of PQ43 to VS	2007 12/26	EVT
3		Down size		39	Change PC38 from 0603 to 0402(SE076473K80)	2007 12/26	EVT
4		Down size		39	Change PC28 from 0805 to 0603(SE107475M80)	2007 12/26	EVT
5		Down size		37	Change PC7 from 1206 to 0603(SE0000005Z80)	2007 12/26	EVT
6		For more current		37	Change PD11 in SCS00002F00(S SCH DIO PDS1040-13 POWERDI5)	2007 12/26	EVT
7		For more current		37	Change PD1 in SCS00002F00(S SCH DIO PDS1040-13 POWERDI5)	2007 12/26	EVT
8		Down size		41	Change PC91 from 0805 to 0603(SE107475M80)	2007 12/26	EVT
9		Down size		41	Change PC96 from 0805 to 0603(SE107475M80)	2007 12/26	EVT
10		Down size		41	Change PC92 from 0603 to 0402(SE000000K80)	2007 12/26	EVT
11		Down size		41	Change PC97 from 0603 to 0402(SE000000K80)	2007 12/26	EVT
12		Down size		42	Change PC110 from 0603 to 0402(SE000000K80)	2007 12/26	EVT
13		Down size		42	Change PC112 from 0603 to 0402(SE074681K80)	2007 12/26	EVT
14		Down size		42	Change PC121 from 0603 to 0402(SE074681K80)	2007 12/26	EVT
15		Down size		42	Change PC128 from 0603 to 0402(SE0000003W00)	2007 12/26	EVT
16		Down size		38	Change PC14 from 0805 to 0603(SE026224K80)	2007 12/26	EVT
17		Down size		38	Change PC18 from 0805 to 0603(SE026224K80)	2007 12/26	EVT
18		Sourcer request		40	Change PC71 \ PC74 from NPO to X7R (SE074102K80)	2008 01/14	EVT
19		DFX		37	Delete PD1	2008 01/14	EVT
20		OCP adjust		39	Change PL3 \ PL4 from 4.7uH to 10uH (SH000002L80)	2008 01/14	EVT
21		OCP adjust		39	Change PR48 \ PR49 from 330K to 287K (SD000005D80)	2008 01/14	EVT
22	HW request	Set 1.5V==>1.54V, 1.05V==>1.07V		40	Change PR95 \ PR99 from 25.5K to 26.7K (SD034267280)	2008 01/14	EVT
23	HW request	Set 5V==>5.138V		39	Change PR41 from 61.9K to 63.4K (SD03463K280)	2008 04/17	DVT

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Title			
SCHEMATIC, M/B A4311			
Size	Document Number	401559	Rev B
Date:	Friday, July 04, 2008	Sheet	43 of 44

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24	Thermal request	Change protect point from 92 to 86 degree C		38	Change PR22 from 15.4K to 16.9K (SD034169280)	2008 04/17	DVT
25		3G EMI request			Delete PR36 \ PR37 \ PR103 \ PR107 \ PC33 \ PC34 \ PC82 \ PC87 "@" mark	2008 04/22	DVT
26					Change PR105 \ PR109 \ PR130 \ PR144 from 0 to 2.2		
27		3G EMI request		40	Change PR105 \ PR109 from 2.2 to 3.3	2008 05/21	PVT
28	EPA power	HW request		41	Add PR167, mark "@" PR112	2008 05/27	PVT
29		EMI request		37	Delete PJ4, add PL12 (SM010020720)	2008 05/27	PVT
30		3G EMI request		39	Change PR38 \ PR39 from 0 to 2.2	2008 05/29	PVT
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Size	Document Number	401559	Rev B
Date:	Friday, July 04, 2008		Sheet 44 of 44