

Compal Confidential

Schematics Document

AMD S1/ ATI RS690MC / SB600

2007 / 1 / 10 Rev:0.3

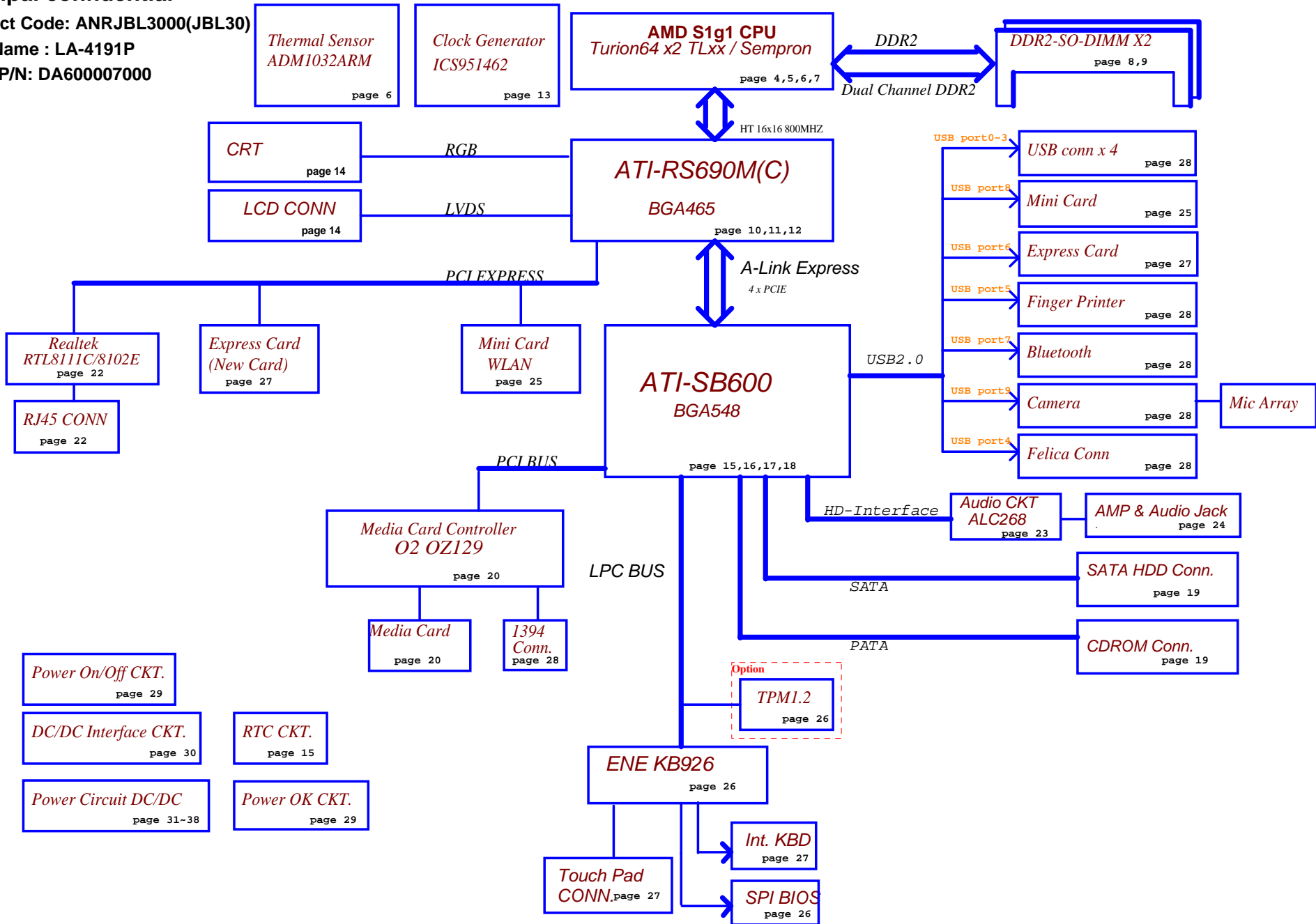
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Project Code: ANRJBL3000(JBL30)

File Name : LA-4191P

PCB P/N: DA600007000



Security Classification	Compal Secret Data			Title	Block Diagrams	
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Voltage Rails

Power Plane	Description	S1	S3	S4/ S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.2VALW	1.2V always on power rail	ON	ON	ON
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra / Rc	100K +/- 5%			
Board ID	Rb / Rd	V _{AD_BID min}	V _{AD_BID typ}	V _{AD_BID max}
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
OZ129	AD21	0	PIRQG

BOARD ID Table

Board ID	PCB Revision
0	0.1 0.2
1	0.3
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b?	ADM1032	1001 110X b?
EEPROM(24C16/02)	1010 000X b?		
(24C04)	1011 000Xb?		

EC SM Bus2 address

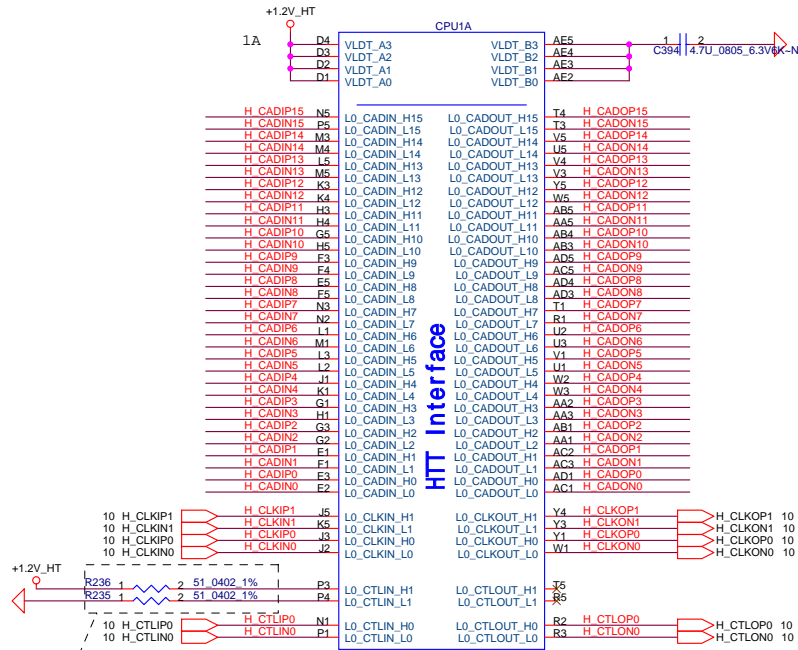
SB600 SM Bus address

Device	Address
Clock Generator (ICS 95146ZAGT)	1101 001Xb?
DDRII DIMM0	1001 000Xb?
DDRII DIMM2	1001 010Xb?



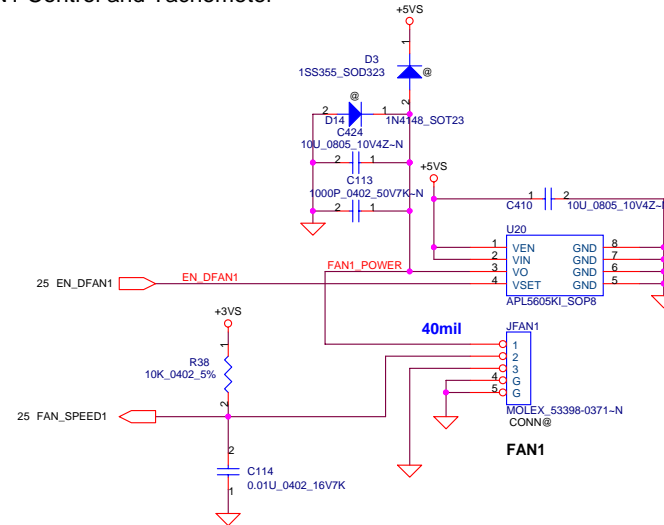
PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



HT Interface

FAN1 Control and Tachometer



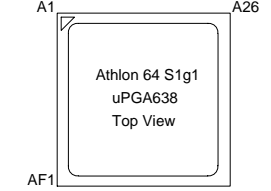
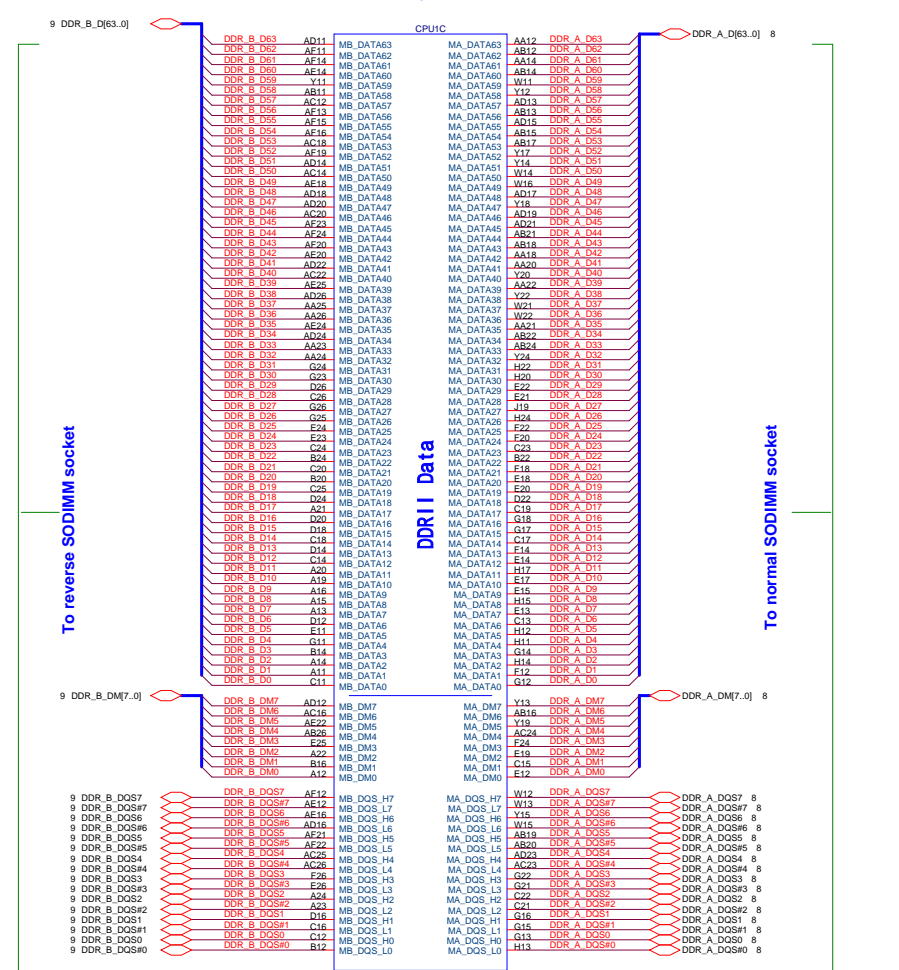
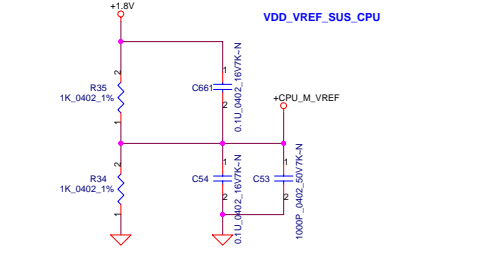
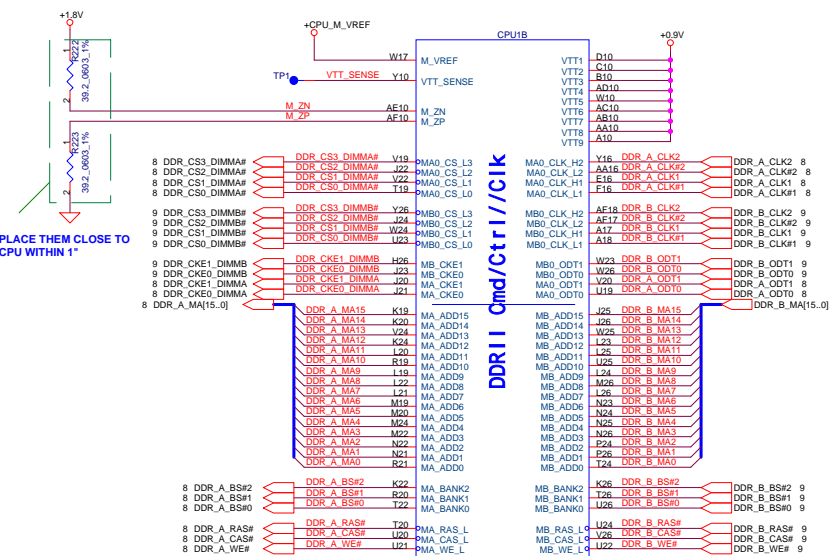
LAYOUT: Place bypass cap near CPU socket

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS PLACE CLOSE TO VLDT0 POWER PINS

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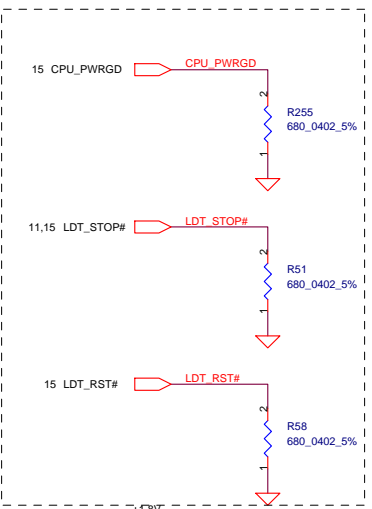
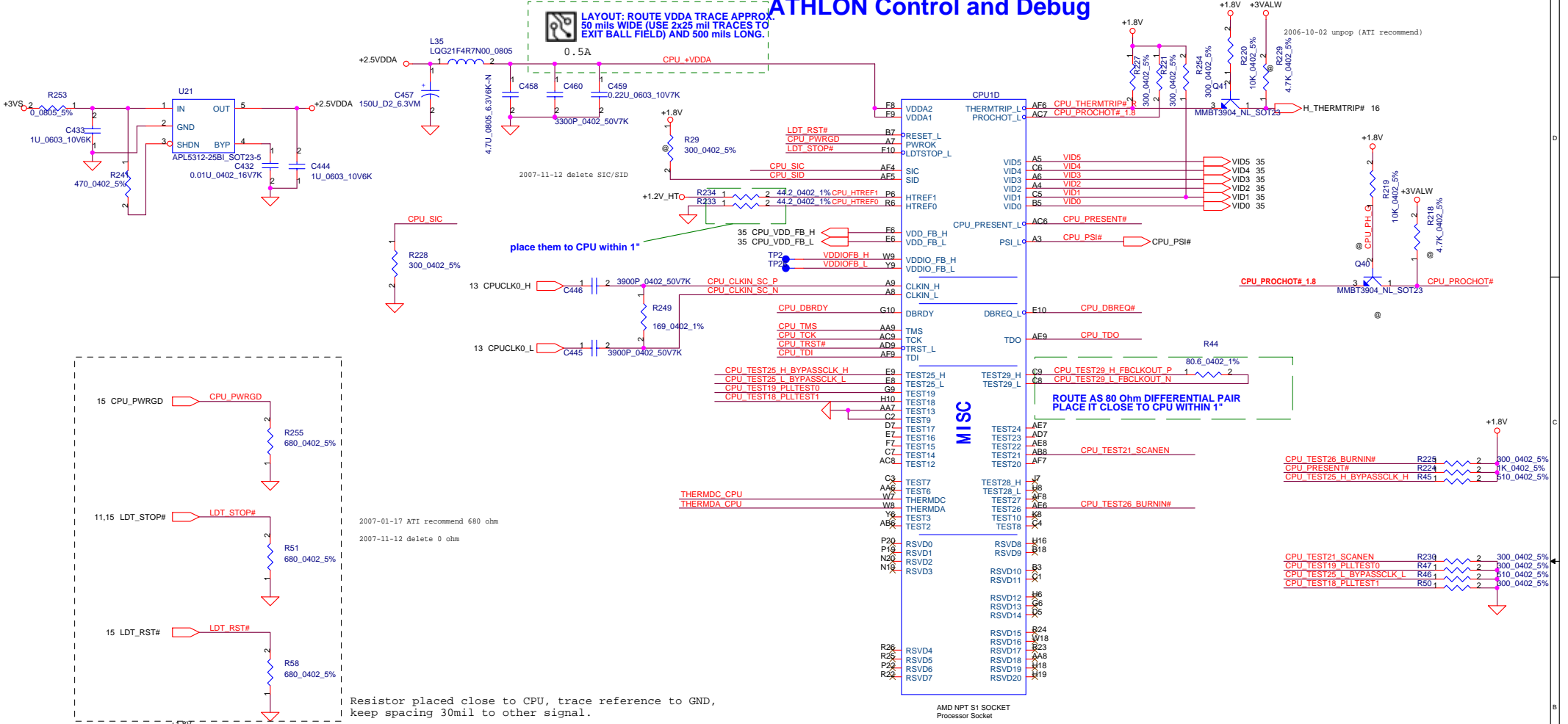
Processor DDR2 Memory Interface

VDD VTT SUS_CPU IS CONNECTED TO THE VDD VTT SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

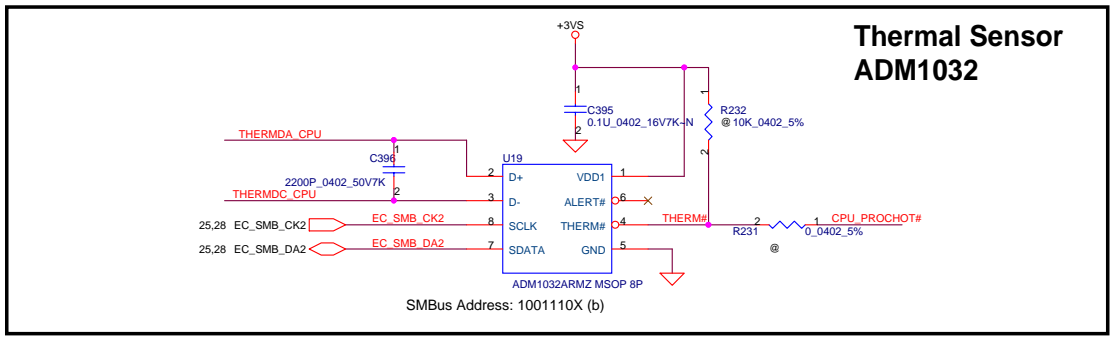
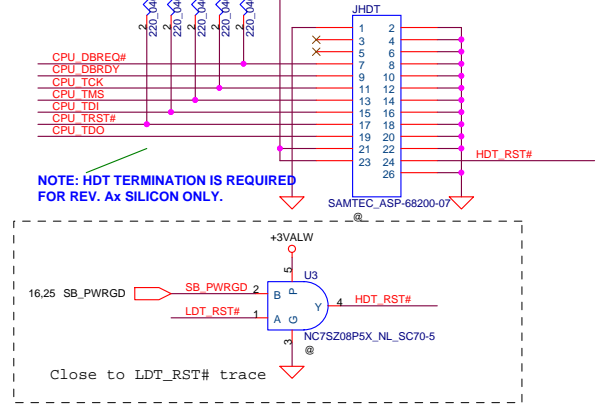


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ATHLON Control and Debug

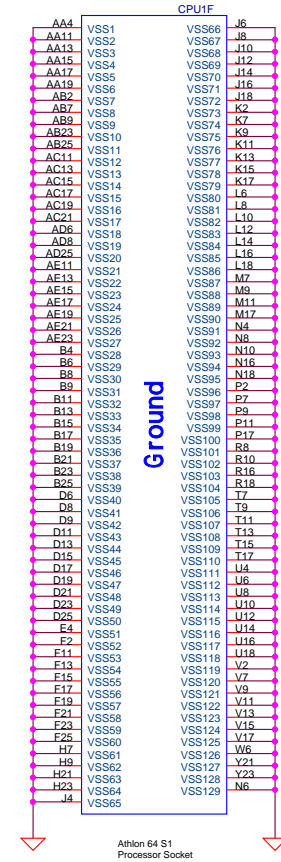
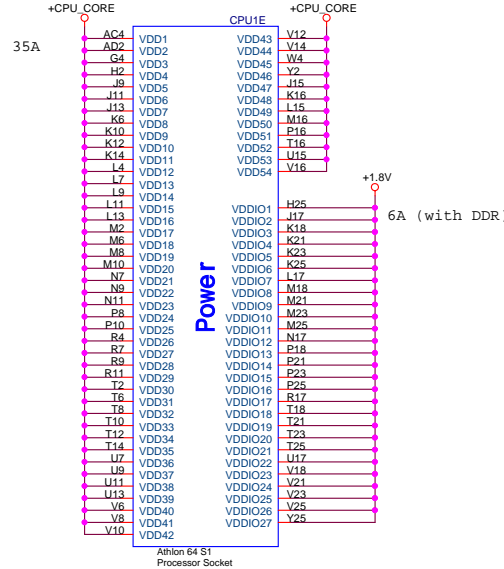
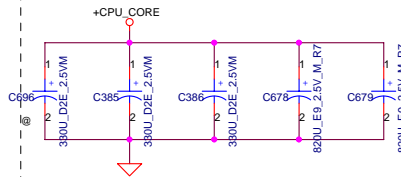
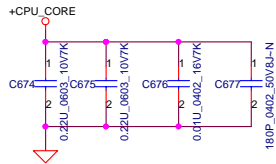
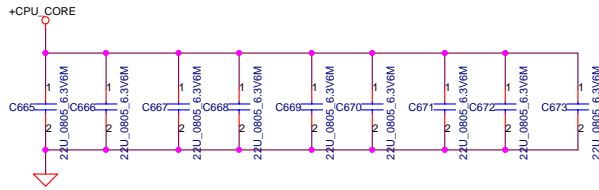
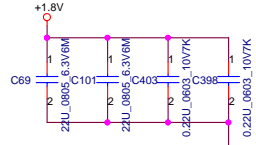


HDT Connector

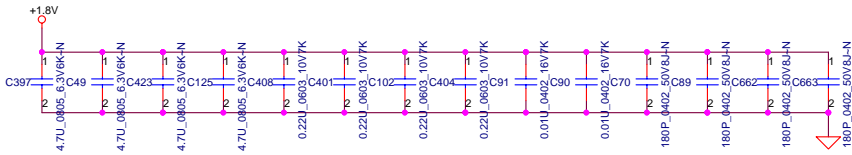


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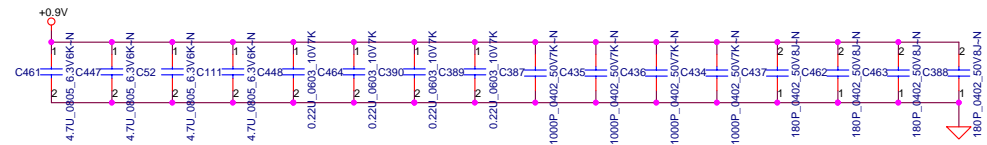
CPU BOTTOMSIDE DECOUPLING



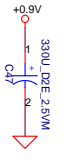
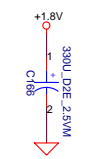
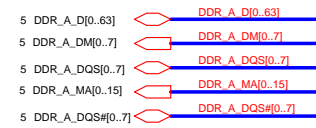
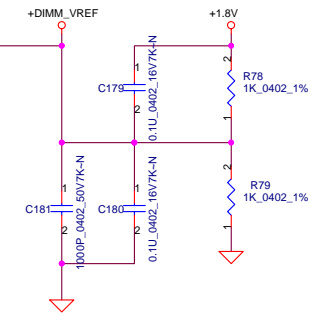
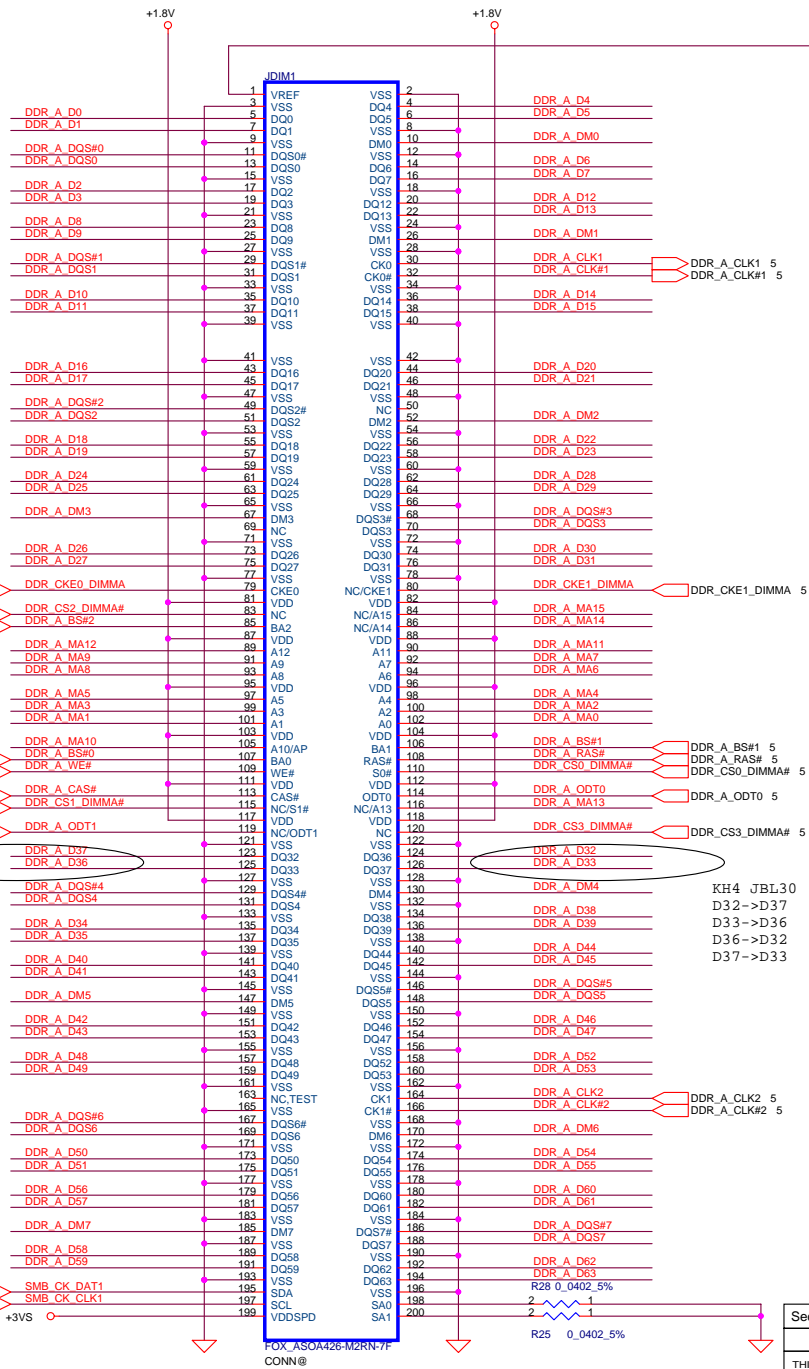
DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE



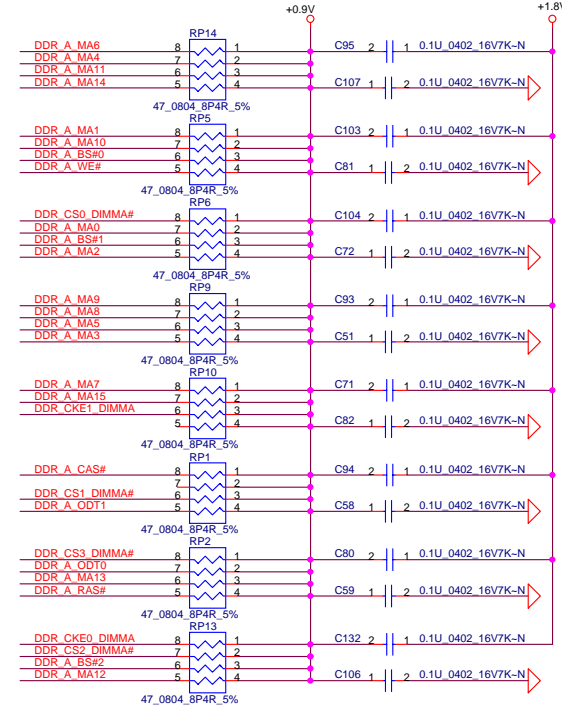
DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE



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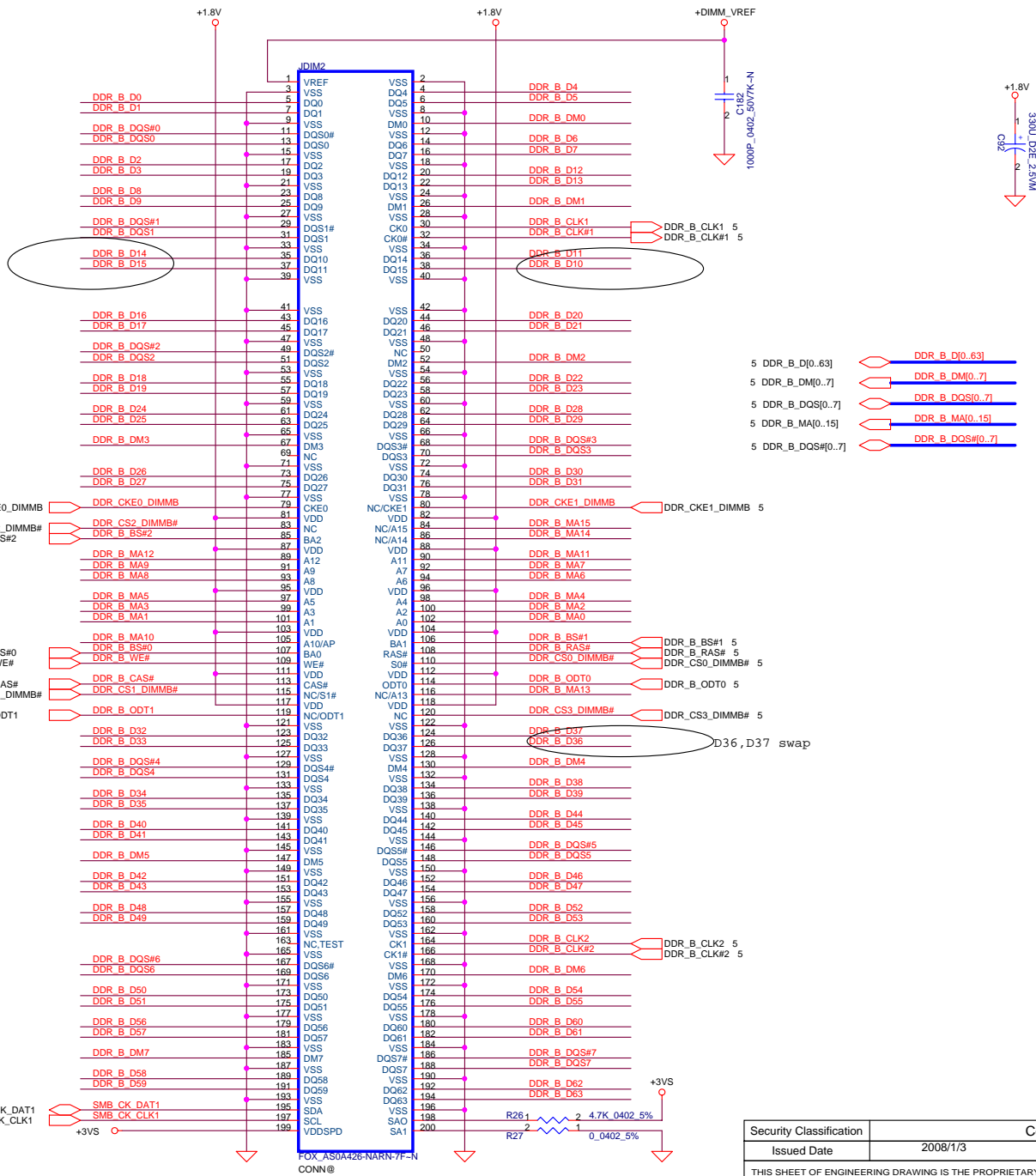
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



9.13.16.26 SMB_CK_DAT1
9.13.16.26 SMB_CK_CLK1

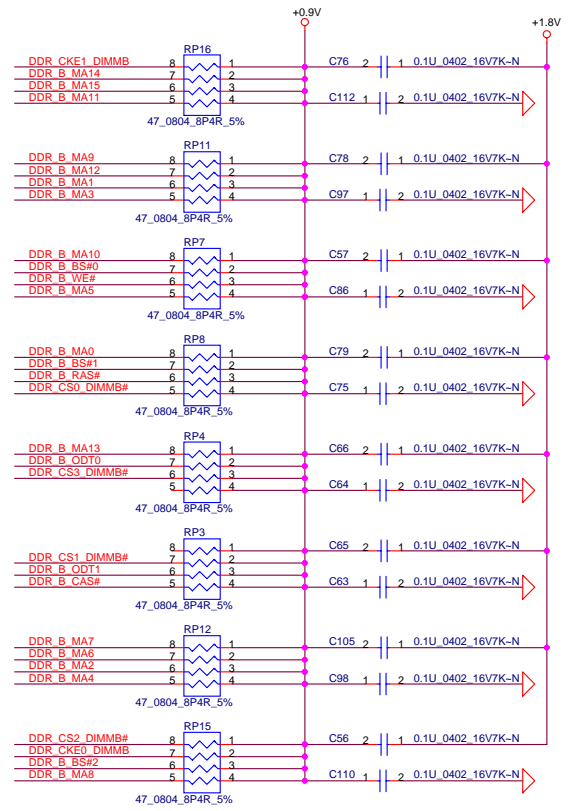
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KH4 JBL30
 D10-->D14
 D11-->D15
 D14-->D11
 D15-->D10

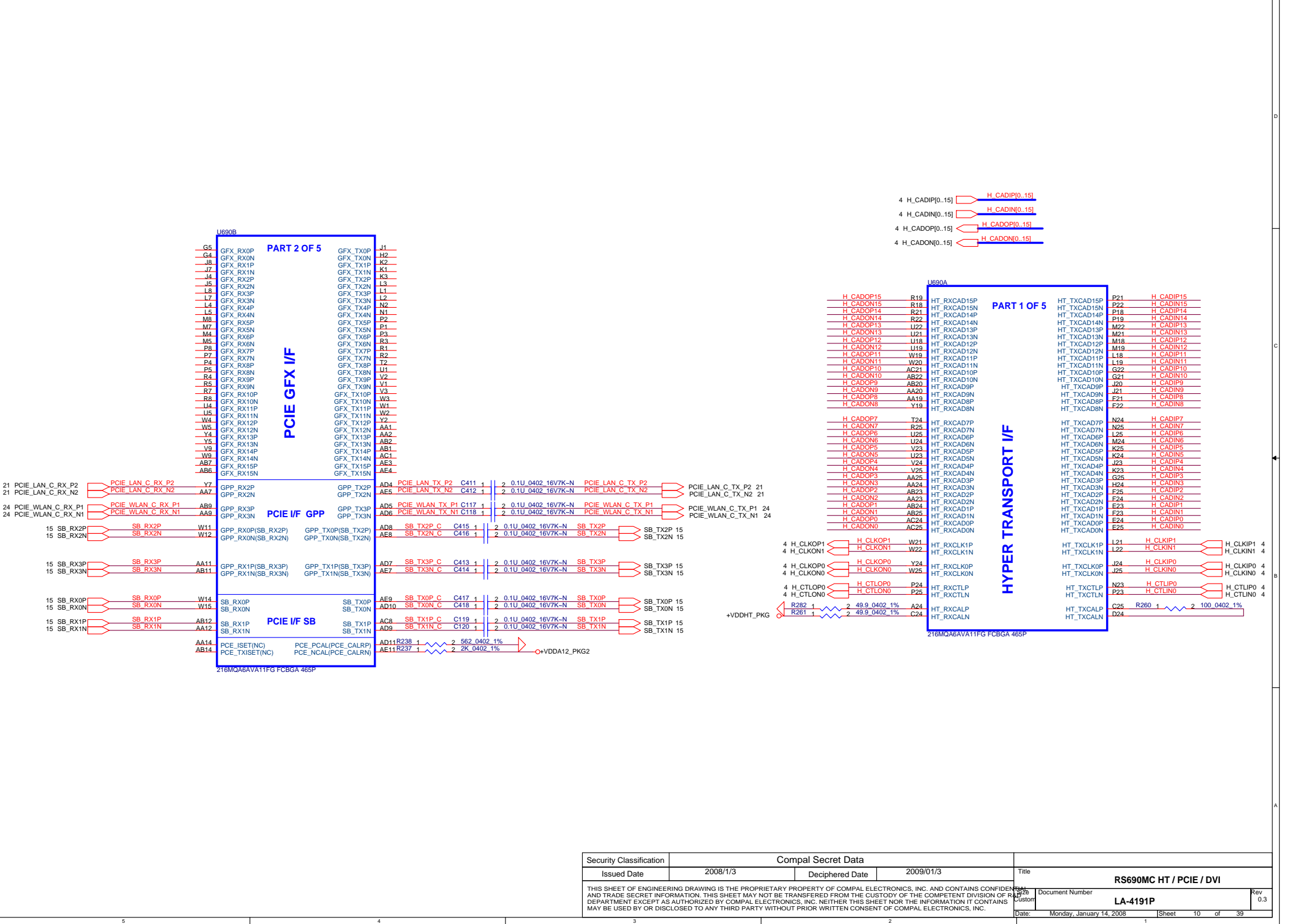


- 5 DDR_B_D[0..63] ← DDR_B_D[0..63]
- 5 DDR_B_DM[0..7] ← DDR_B_DM[0..7]
- 5 DDR_B_DQS[0..7] ← DDR_B_DQS[0..7]
- 5 DDR_B_MA[0..15] ← DDR_B_MA[0..15]
- 5 DDR_B_DQS#[0..7] ← DDR_B_DQS#[0..7]

Layout Note:
 Place one cap close to every 2 pullup resistors terminated to +0.9V



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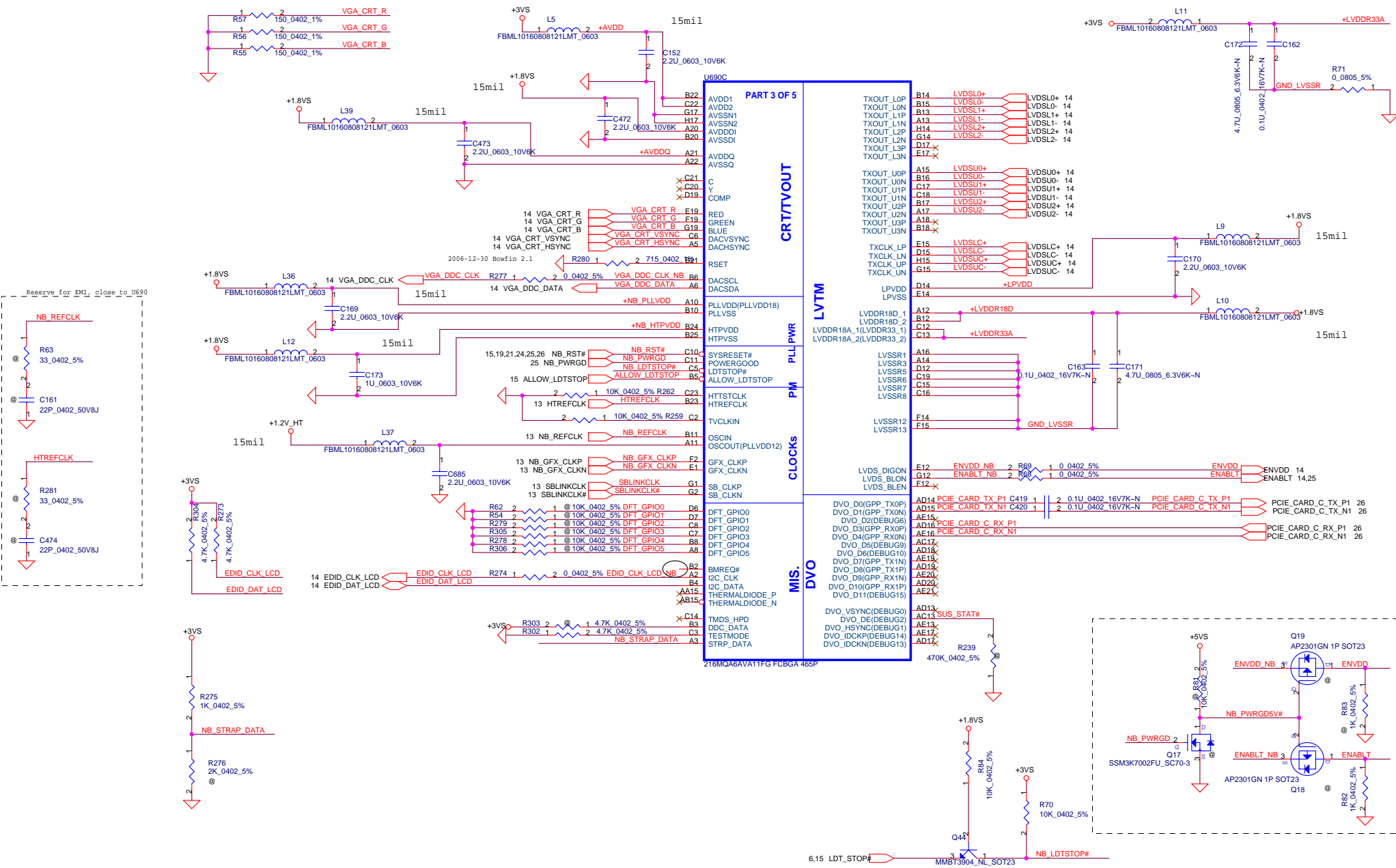


4 H_CADIP[0..15] H_CADIP[0..15]
 4 H_CADIN[0..15] H_CADIN[0..15]
 4 H_CADOP[0..15] H_CADOP[0..15]
 4 H_CADON[0..15] H_CADON[0..15]

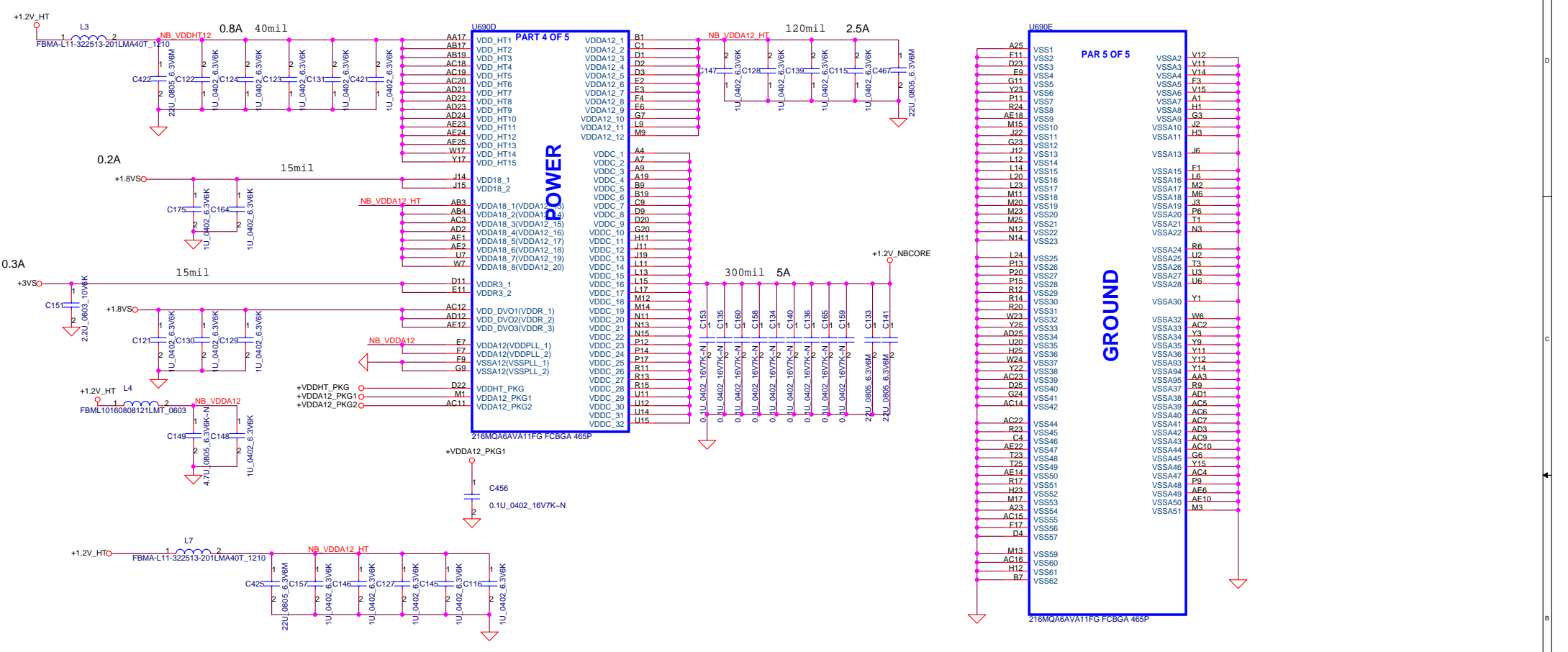
HYPER TRANSPORT I/F

H_CADOP15	R19	HT_RXCAD15P	P21	H_CADIP15		
H_CADON15	R18	HT_RXCAD15N	P22	H_CADIN15		
H_CADOP14	R21	HT_RXCAD14P	P18	H_CADIP14		
H_CADON14	R22	HT_RXCAD14N	P19	H_CADIN14		
H_CADOP13	U22	HT_RXCAD13P	M22	H_CADIP13		
H_CADON13	U21	HT_RXCAD13N	M21	H_CADIN13		
H_CADOP12	U18	HT_RXCAD12P	M18	H_CADIP12		
H_CADON12	U19	HT_RXCAD12N	M19	H_CADIN12		
H_CADOP11	W19	HT_RXCAD11P	L18	H_CADIP11		
H_CADON11	W20	HT_RXCAD11N	L19	H_CADIN11		
H_CADOP10	AC21	HT_RXCAD10P	G22	H_CADIP10		
H_CADON10	AB22	HT_RXCAD10N	G21	H_CADIN10		
H_CADOP9	AB20	HT_RXCAD9P	J20	H_CADIP9		
H_CADON9	AA20	HT_RXCAD9N	J21	H_CADIN9		
H_CADOP8	AA19	HT_RXCAD8P	F21	H_CADIP8		
H_CADON8	Y19	HT_RXCAD8N	F22	H_CADIN8		
H_CADOP7	T24	HT_RXCAD7P	N24	H_CADIP7		
H_CADON7	R25	HT_RXCAD7N	N25	H_CADIN7		
H_CADOP6	U25	HT_RXCAD6P	L25	H_CADIP6		
H_CADON6	U24	HT_RXCAD6N	M24	H_CADIN6		
H_CADOP5	V23	HT_RXCAD5P	K25	H_CADIP5		
H_CADON5	U23	HT_RXCAD5N	K24	H_CADIN5		
H_CADOP4	V24	HT_RXCAD4P	J23	H_CADIP4		
H_CADON4	V25	HT_RXCAD4N	K23	H_CADIN4		
H_CADOP3	AA25	HT_RXCAD3P	G25	H_CADIP3		
H_CADON3	AA24	HT_RXCAD3N	H24	H_CADIN3		
H_CADOP2	AB23	HT_RXCAD2P	F25	H_CADIP2		
H_CADON2	AA23	HT_RXCAD2N	F24	H_CADIN2		
H_CADOP1	AB24	HT_RXCAD1P	E23	H_CADIP1		
H_CADON1	AB25	HT_RXCAD1N	E23	H_CADIN1		
H_CADOP0	AC24	HT_RXCAD0P	E24	H_CADIP0		
H_CADON0	AC25	HT_RXCAD0N	E25	H_CADIN0		
H_CLKOP1	W21	HT_RXCLK1P	L21	H_CLKIP1		
H_CLKON1	W22	HT_RXCLK1N	L22	H_CLKIN1		
H_CLKOPO	Y24	HT_RXCLK0P	J24	H_CLKIPO		
H_CLKONO	W25	HT_RXCLK0N	J25	H_CLKINO		
H_CTLOPO	P24	HT_RXCTLP	N23	H_CTLIPO		
H_CTLONO	P25	HT_RXCTLN	P23	H_CTLINO		
R282	2 49.9 0402 1%	A24	HT_RXCALP	C25	R260	2 100 0402 1%
R261	2 49.9 0402 1%	C24	HT_RXCALN	D24		

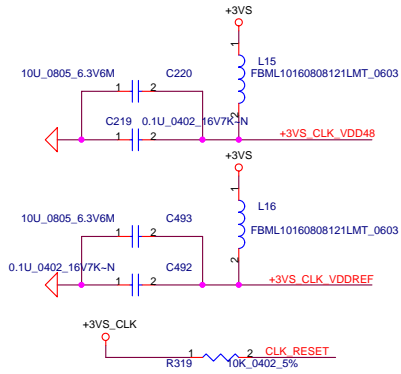
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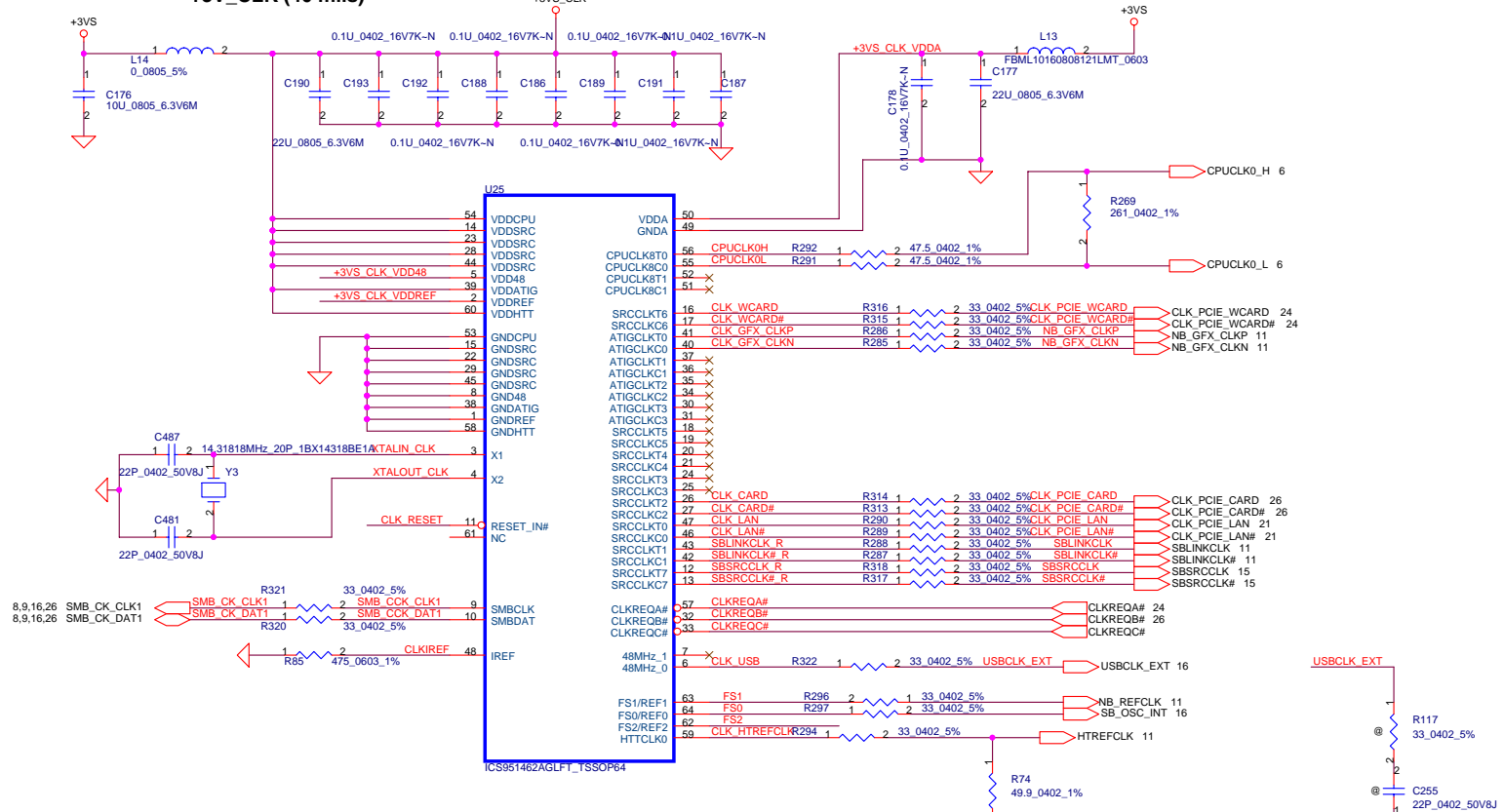
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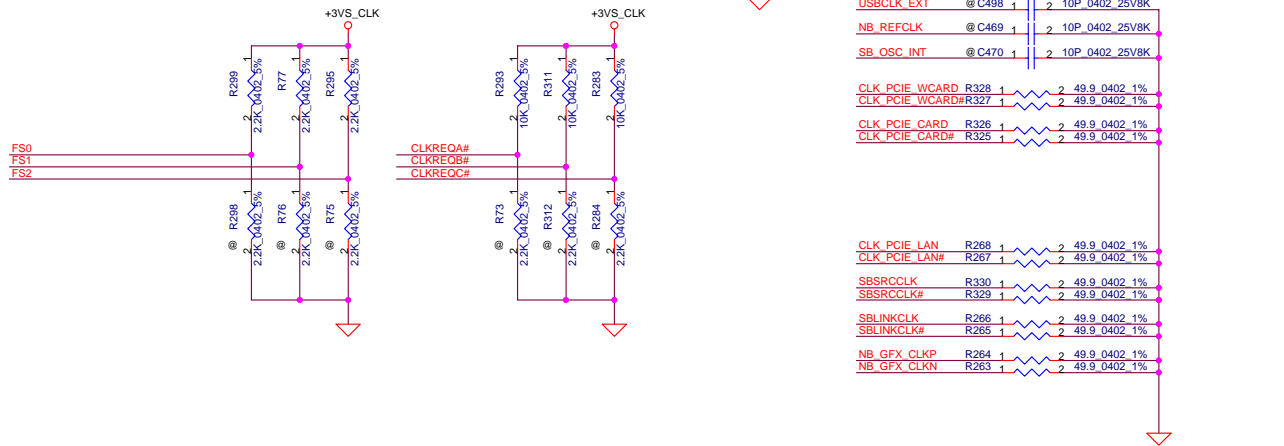


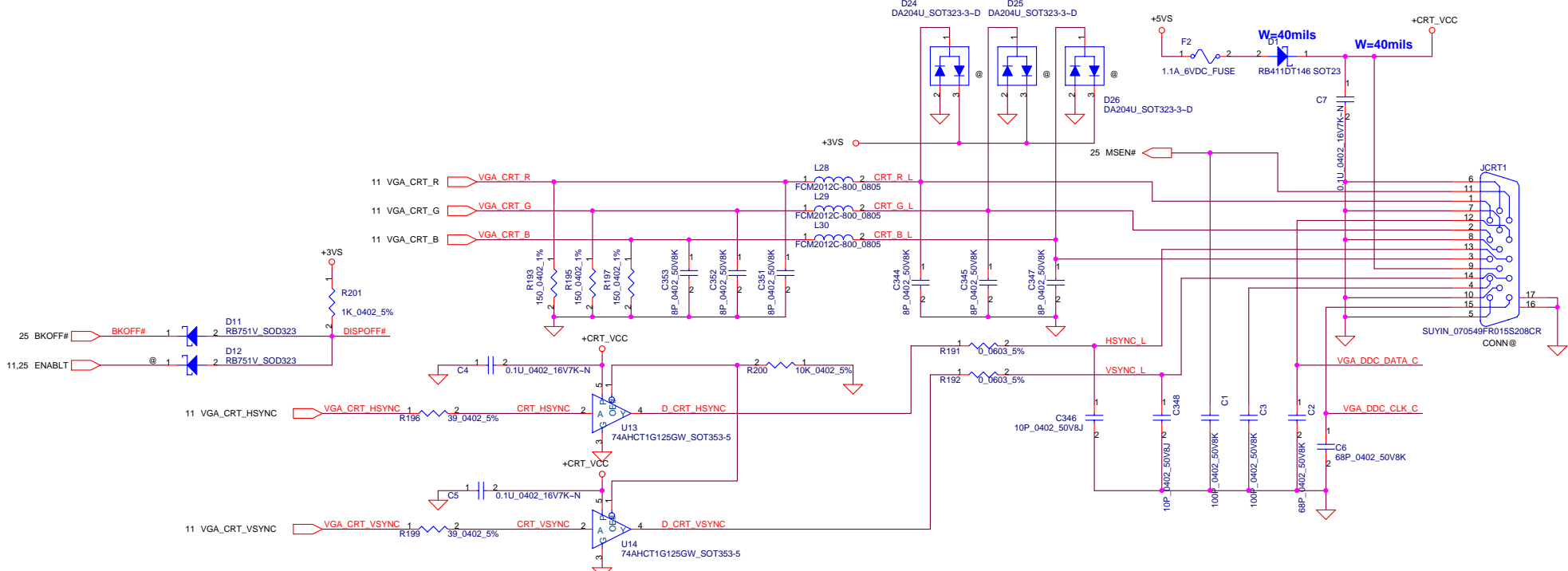
+3VS_CLK (40 mils)



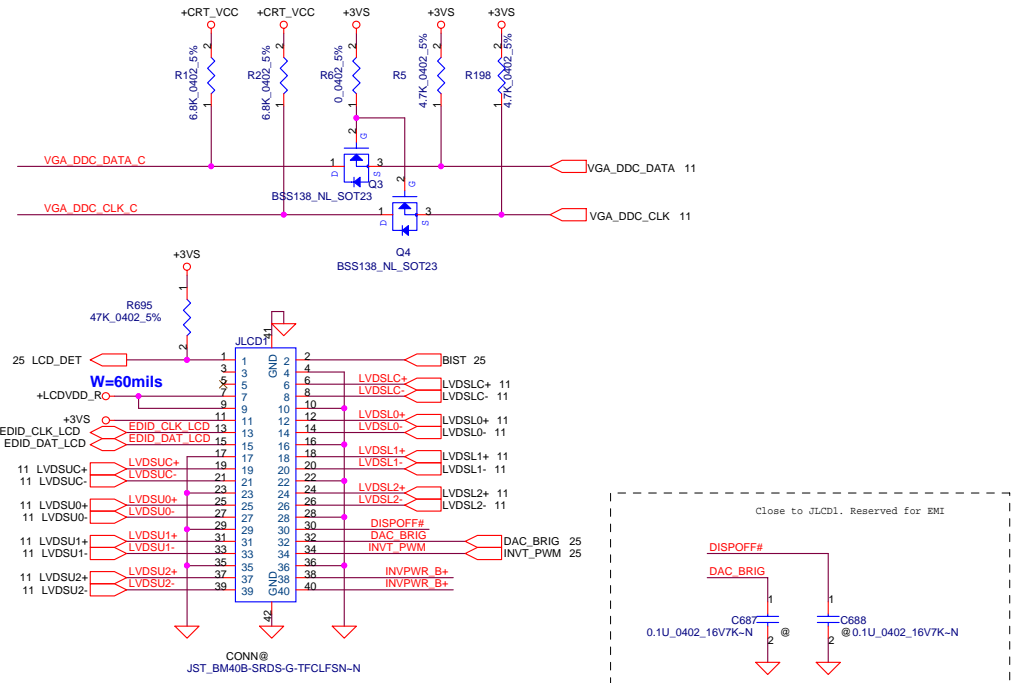
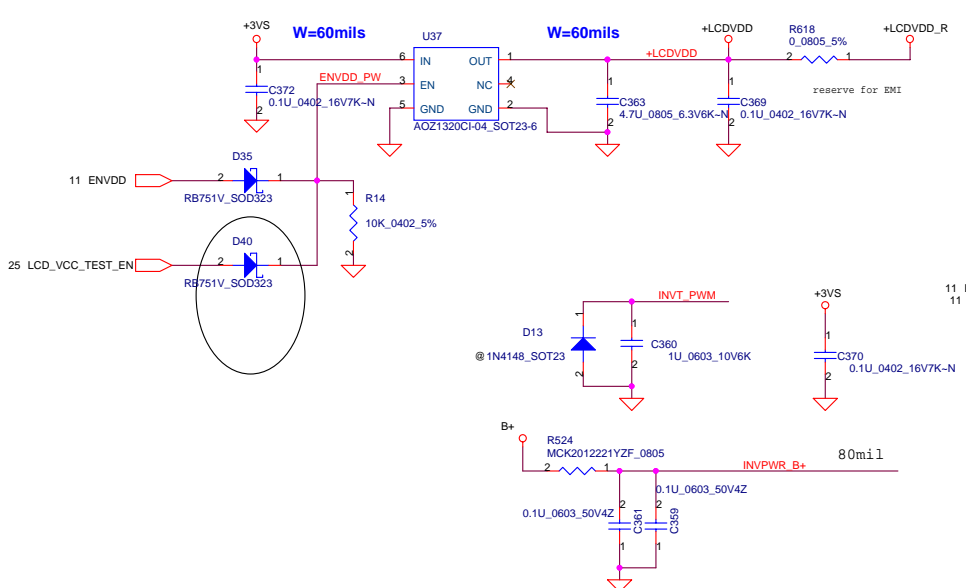
EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

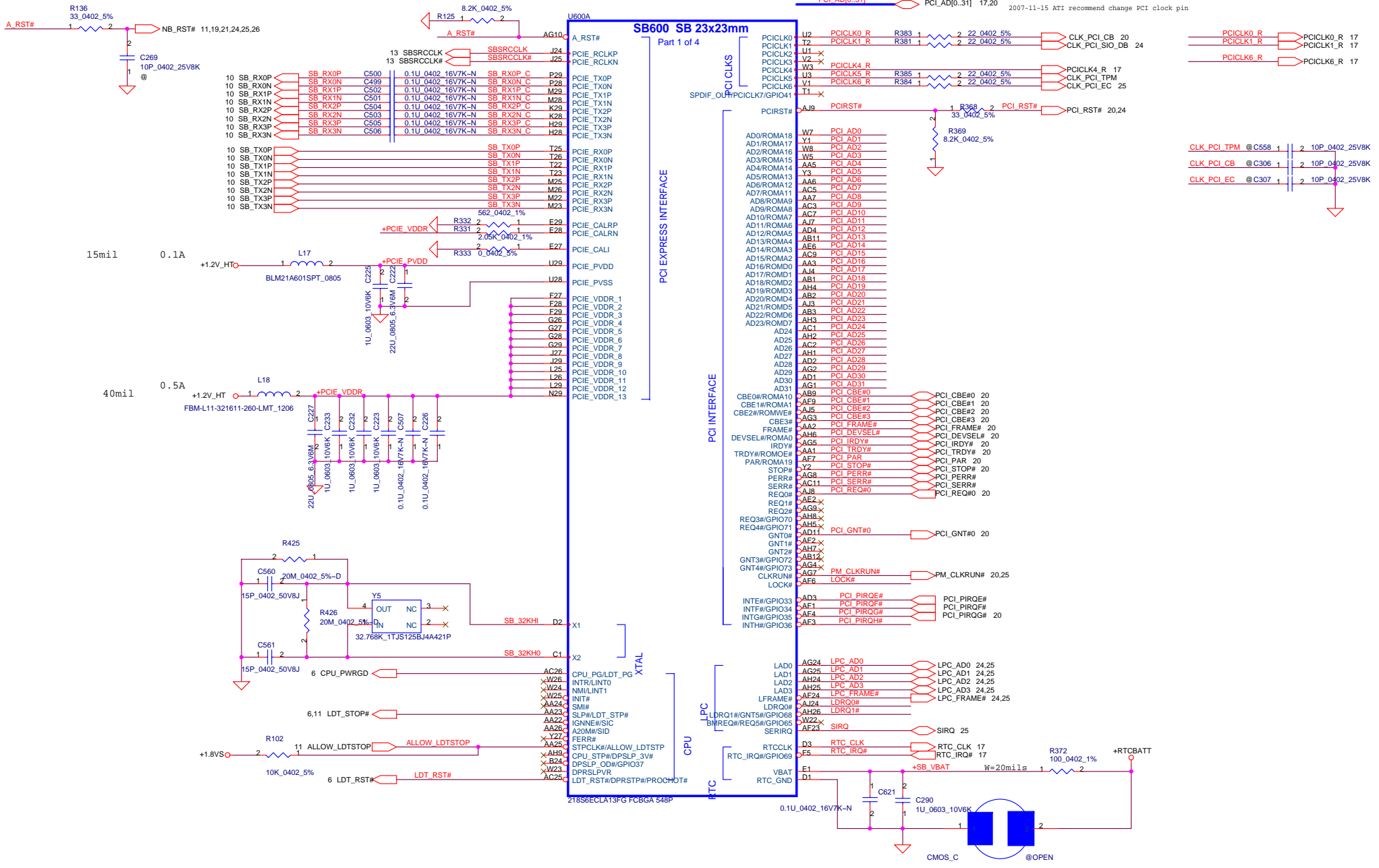




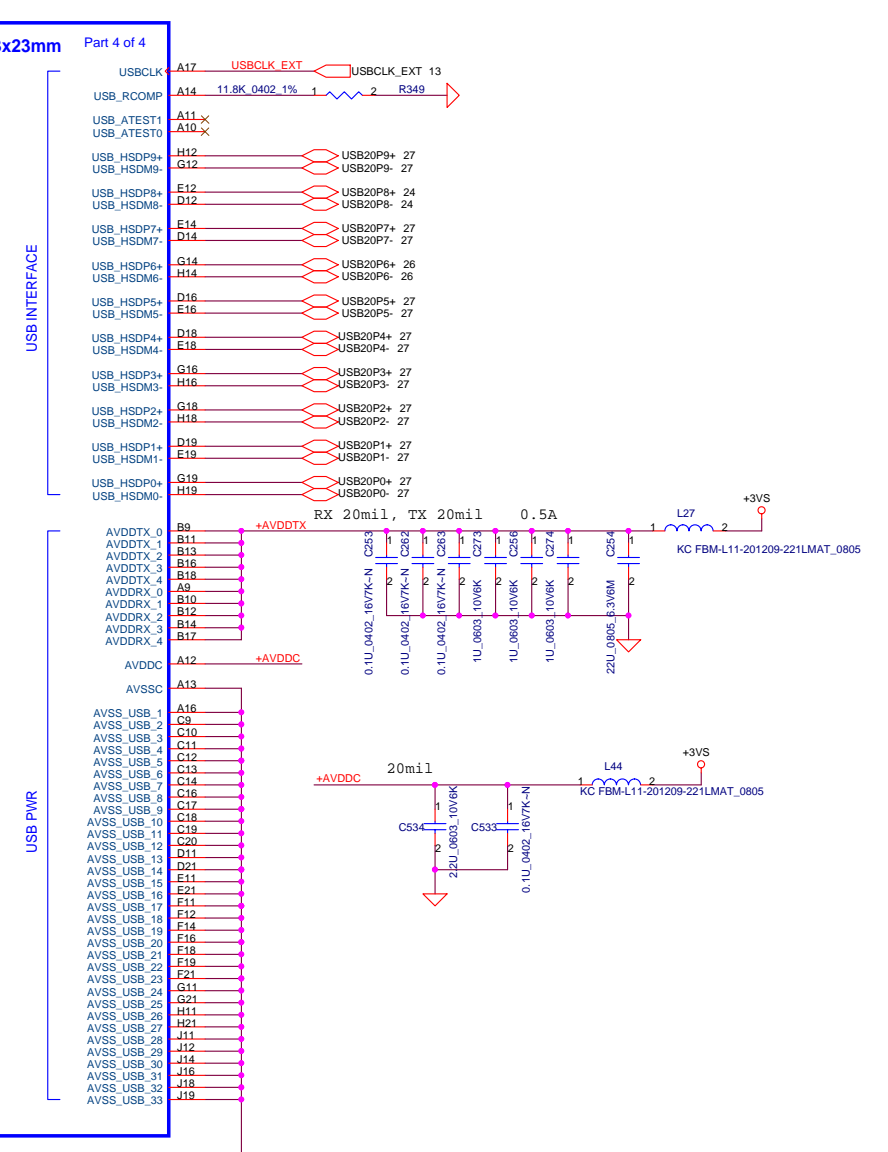
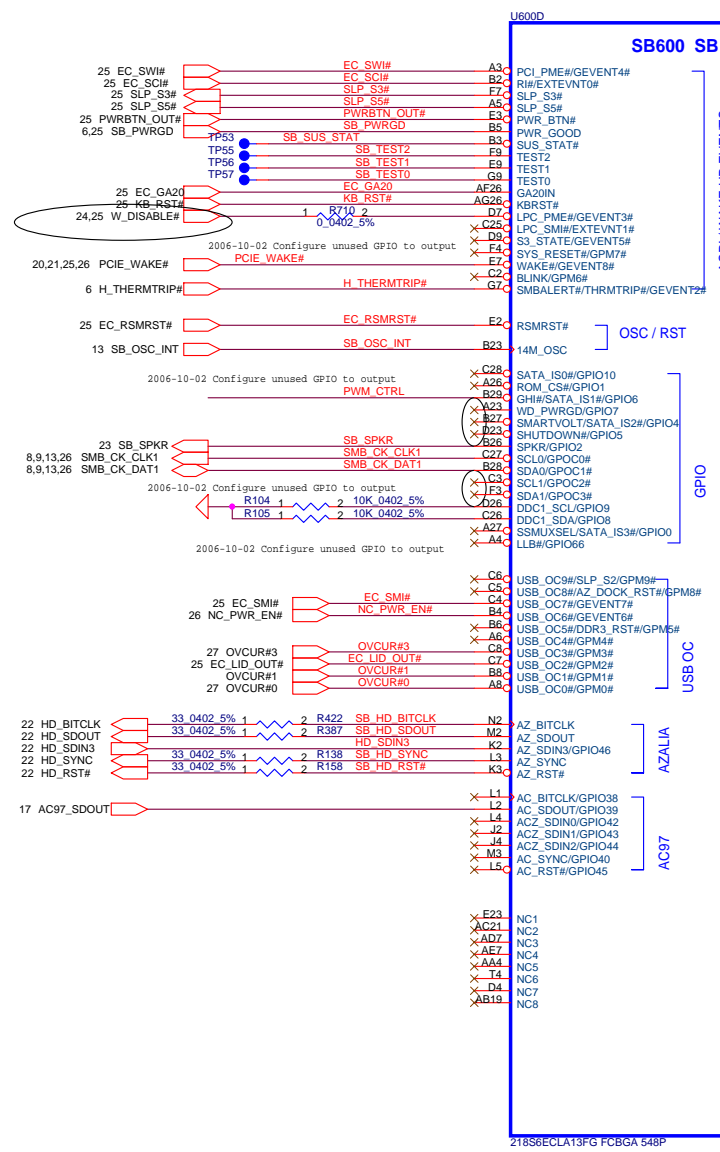
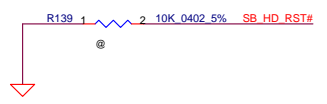
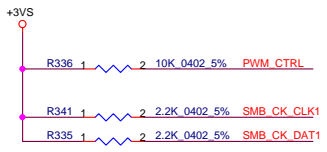
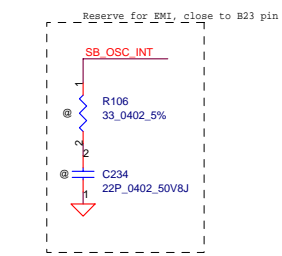
LCD POWER CIRCUIT



Security Classification	Compal Secret Data			Title	CRT Conn.& LCD Conn.	
Issued Date	2008/1/3	Deciphered Date	2009/01/3	Revision	Document Number	Rev
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				Customer	LA-4191P	0.3



Security Classification		Compal Secret Data		Title	
Issued Date	2008/1/3	Deciphered Date	2009/01/3	SB600-PCI_EXP/PCI/LPC/RTC	
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Date:	Monday, January 14, 2008	Sheet	15	of 39	



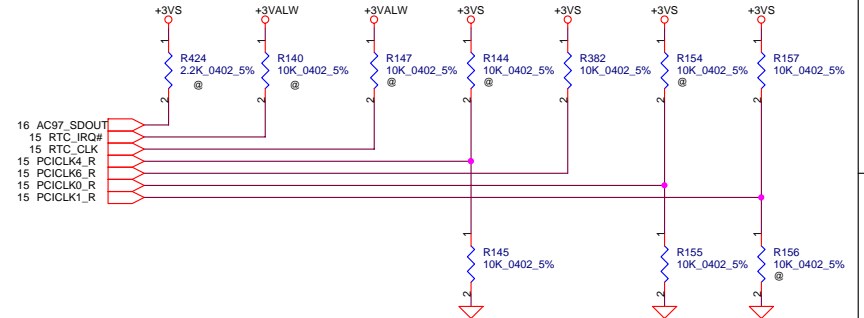
21856ECL1A13FG F0BGA 548P

Security Classification	Compal Secret Data		Title	SB600 USB/ACPI/AC97/GPIO	
Issued Date	2008/1/3	Deciphered Date	2009/01/3	Document Number	LA-4191P
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REQUIRED STRAPS

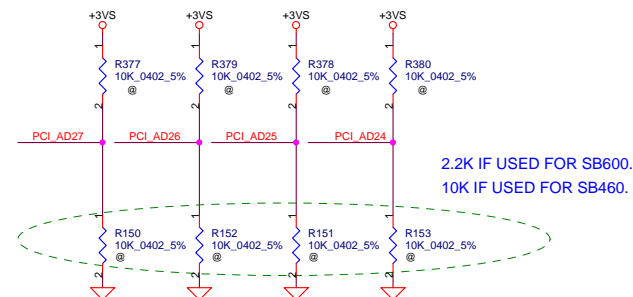
SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT, 15K PU FOR RTC_CLK, EXTERNAL PU/PD IS NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE REQUIRED



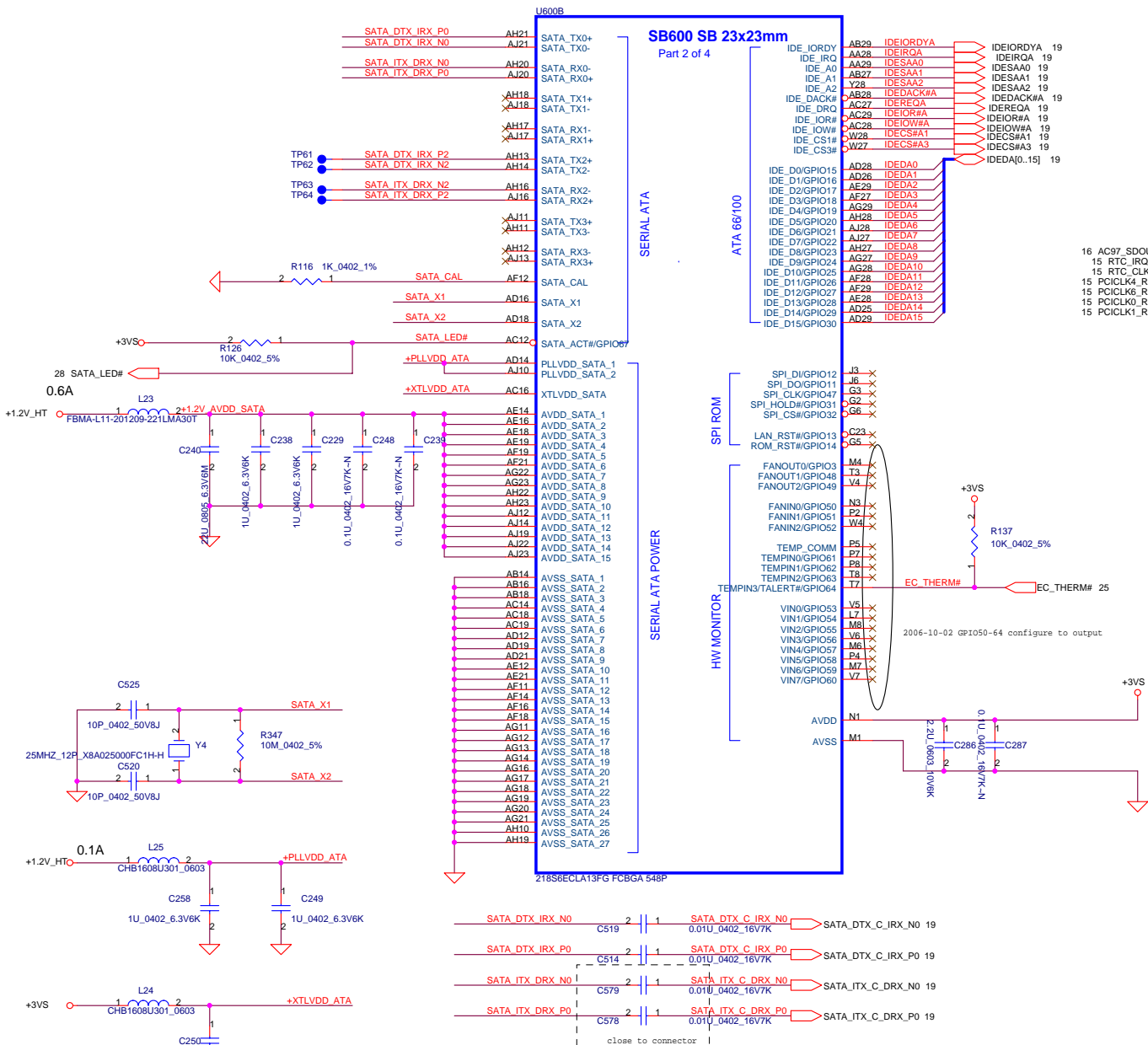
	AC97_SDOUT	RTC_CLK	PCICLK4_R	PCICLK6_R	PCICLK1_R	PCICLK0_R
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM L, L = LPC I ROM L, L = FWH ROM	
PULL LOW	IGNORE DEBUG STRAPS	EXTERNAL RTC	USE EXT. 48MHZ	CPU IF=P4	NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK1[0]	

DEBUG STRAPS

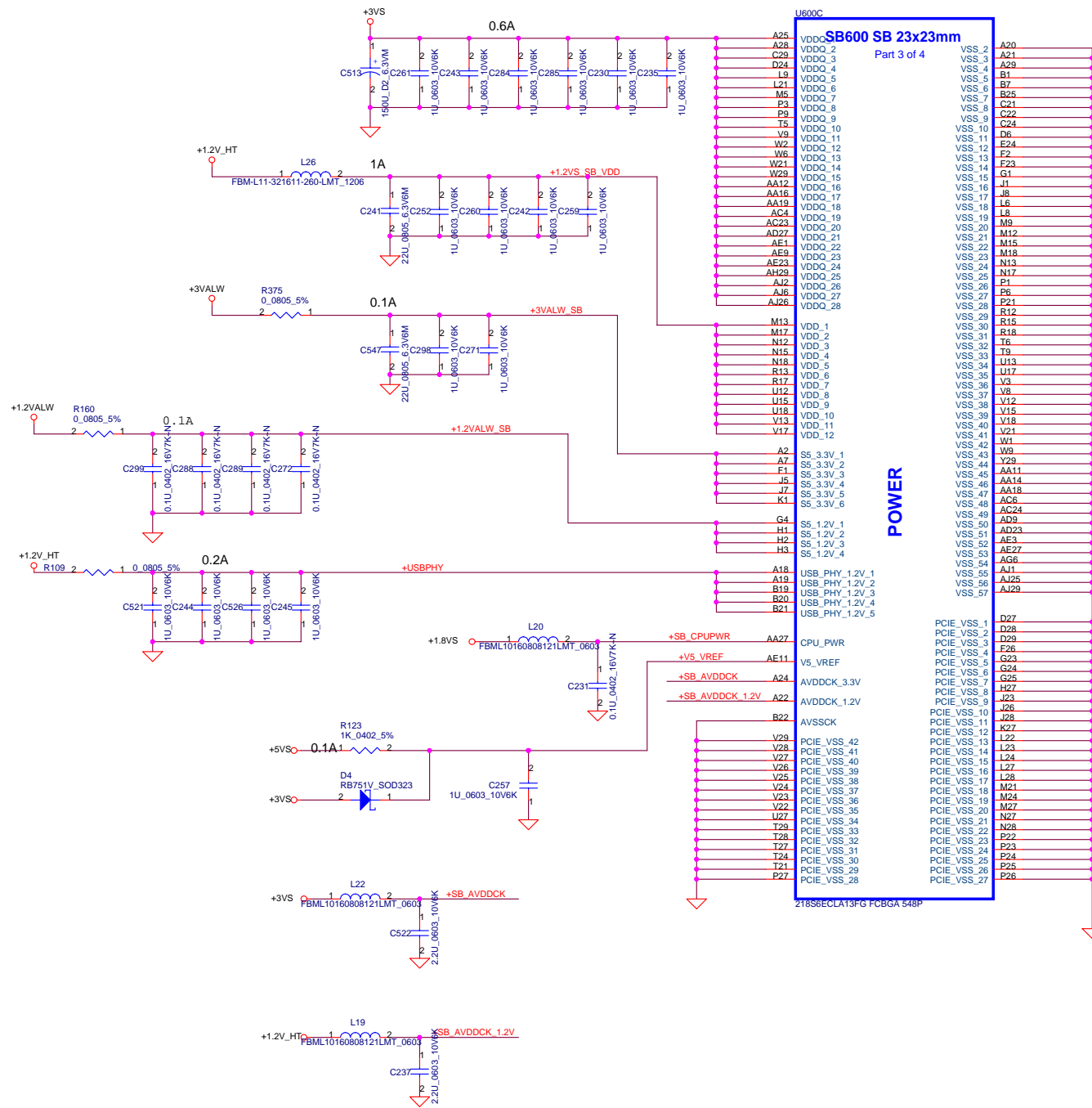
SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24
PULL HIGH	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS
PULL LOW	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS

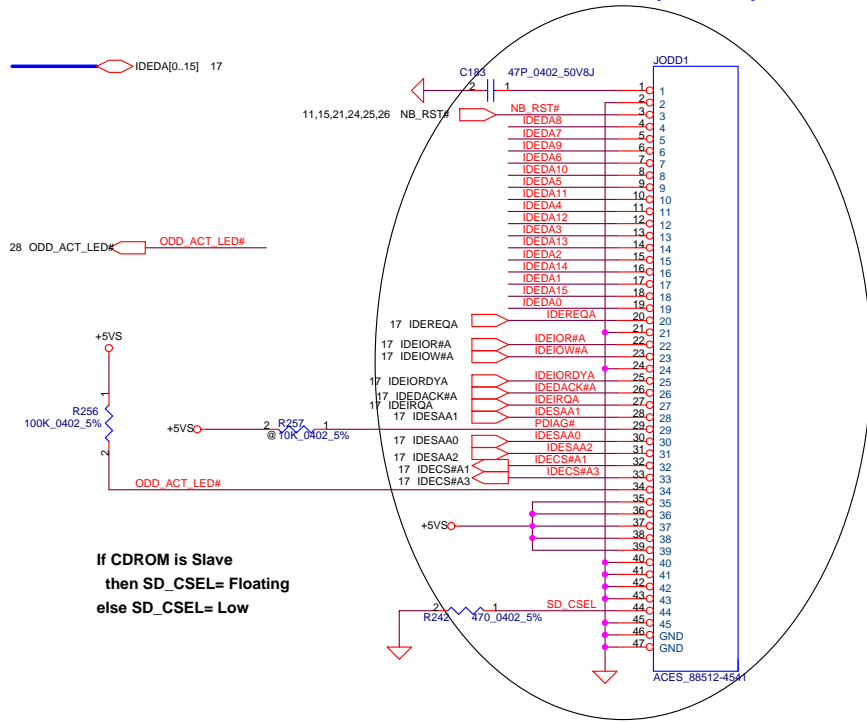


SATA_DTX_IRX_N0	2	1	SATA_DTX_C_IRX_N0	SATA_DTX_C_IRX_N0	19
SATA_DTX_IRX_P0	2	1	SATA_DTX_C_IRX_P0	SATA_DTX_C_IRX_P0	19
SATA_ITX_DRX_N0	2	1	SATA_ITX_C_DRX_N0	SATA_ITX_C_DRX_N0	19
SATA_ITX_DRX_P0	2	1	SATA_ITX_C_DRX_P0	SATA_ITX_C_DRX_P0	19

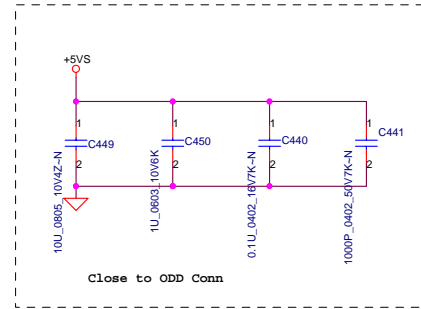


Security Classification	Compal Secret Data			Title	SB600 Power/GND	
Issued Date	2008/1/3	Deciphered Date	2009/01/3	Part Number	Document Number	Rev
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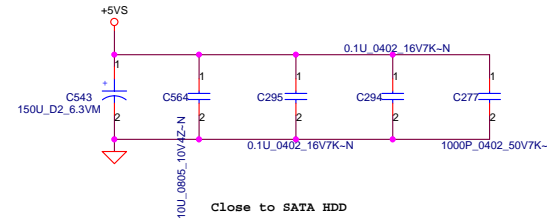
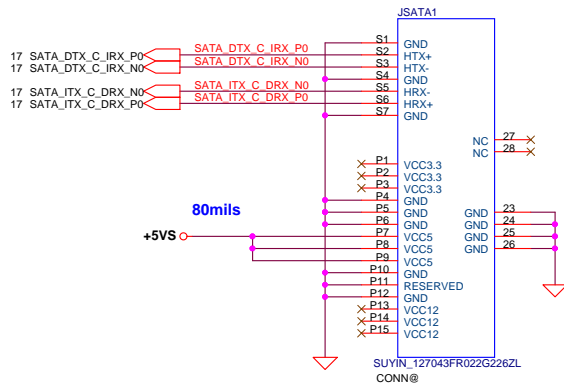
CDROM CONN(to FPC)



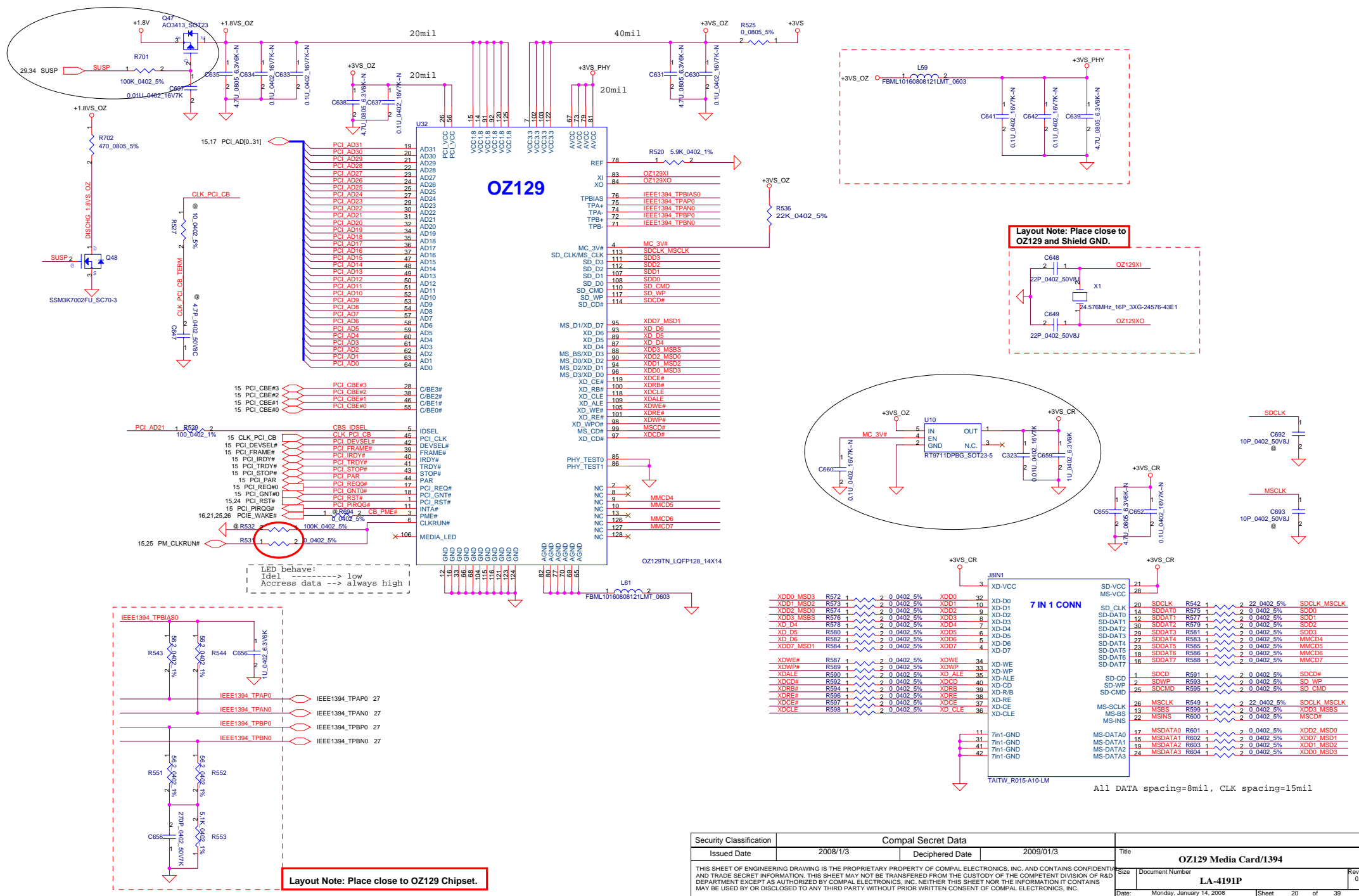
If CDROM is Slave
then SD_CSEL= Floating
else SD_CSEL= Low



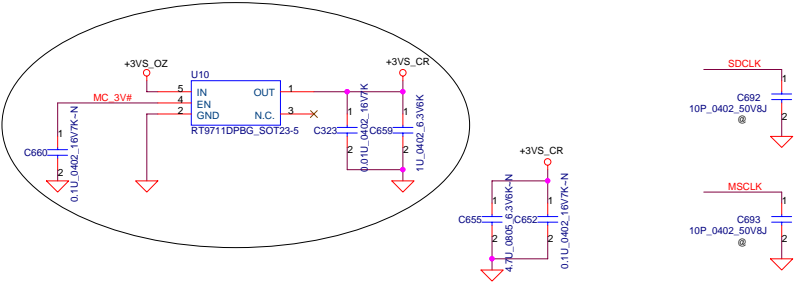
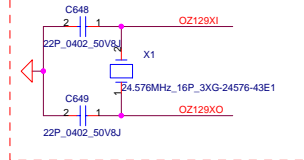
SATA HDD CONN



Security Classification	Compal Secret Data			Title	HDD/CDROM	
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Layout Note: Place close to OZ129 and Shield GND.



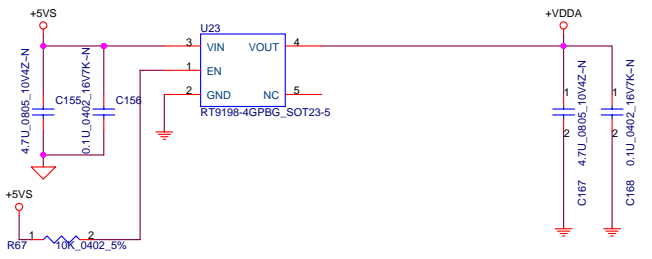
XDD0 MSD3		R572		XDD0		XD-D0	
XDD1 MSD2	R573	XDD1	10	XD-D1			
XDD2 MSD0	R574	XDD2	9	XD-D2			
XDD3 MSB5	R575	XDD3	8	XD-D3			
XD D4	R576	XDD4	7	XD-D4			
XD D5	R580	XDD5	6	XD-D5			
XD D6	R582	XDD6	5	XD-D6			
XDD7 MSD1	R584	XDD7	4	XD-D7			
XDWIE#	R587	XDWIE	34	XD-WP			
XDWPF#	R588	XDWPF	33	XD-WP			
XDALE	R590	XDALE	38	XD-ALE			
XDCD#	R592	XDCD	40	XD-CD			
XDRB#	R594	XDRB	39	XD-R/B			
XDRE#	R596	XDRE	38	XD-RE			
XDCIE#	R597	XDCIE	37	XD-CE			
XDCLE	R598	XD-CLE	36	XD-CLE			

7 IN 1 CONN

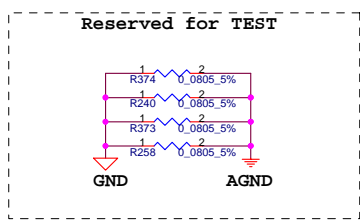
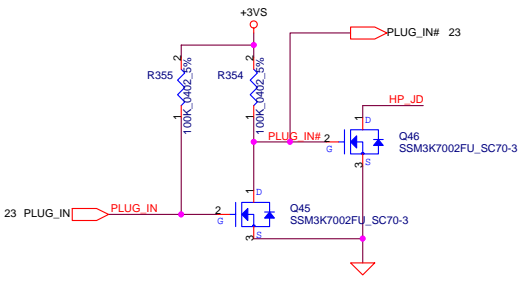
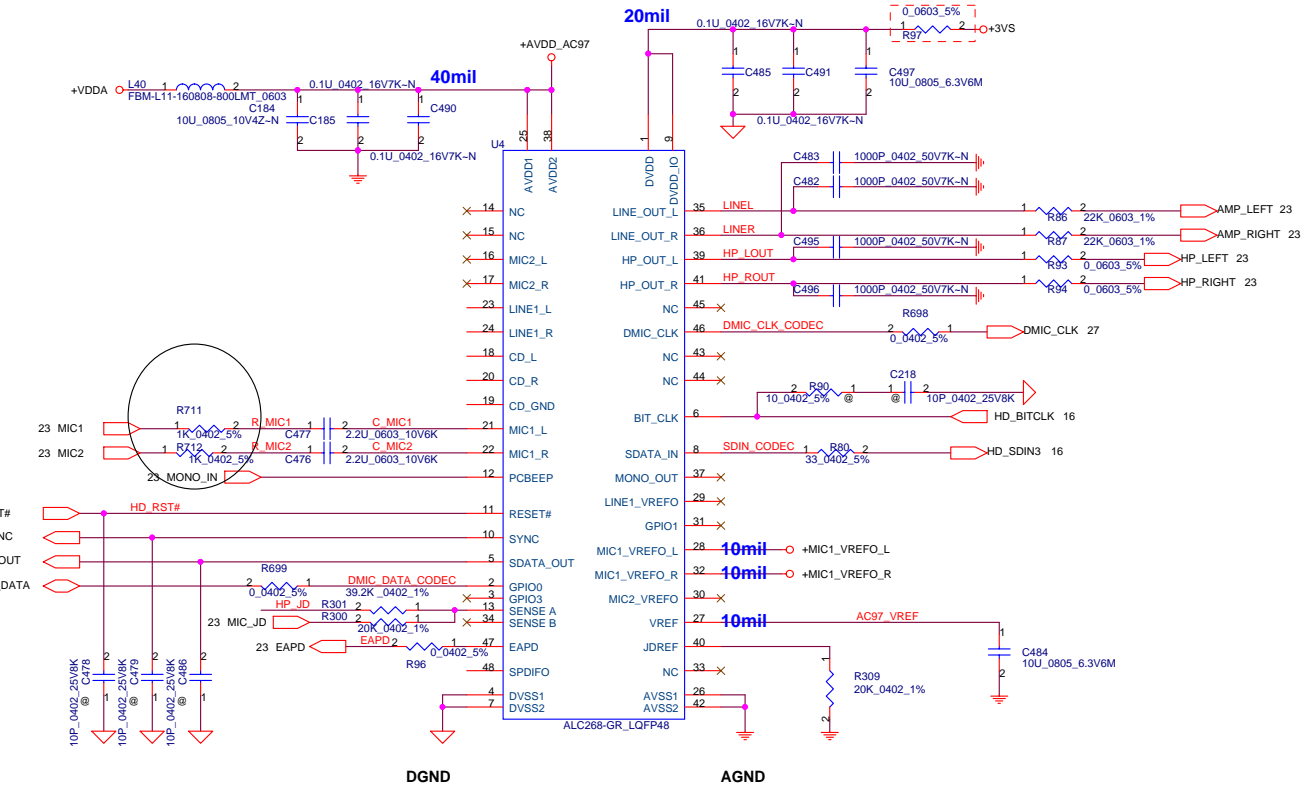
All DATA spacing=8mil, CLK spacing=15mil

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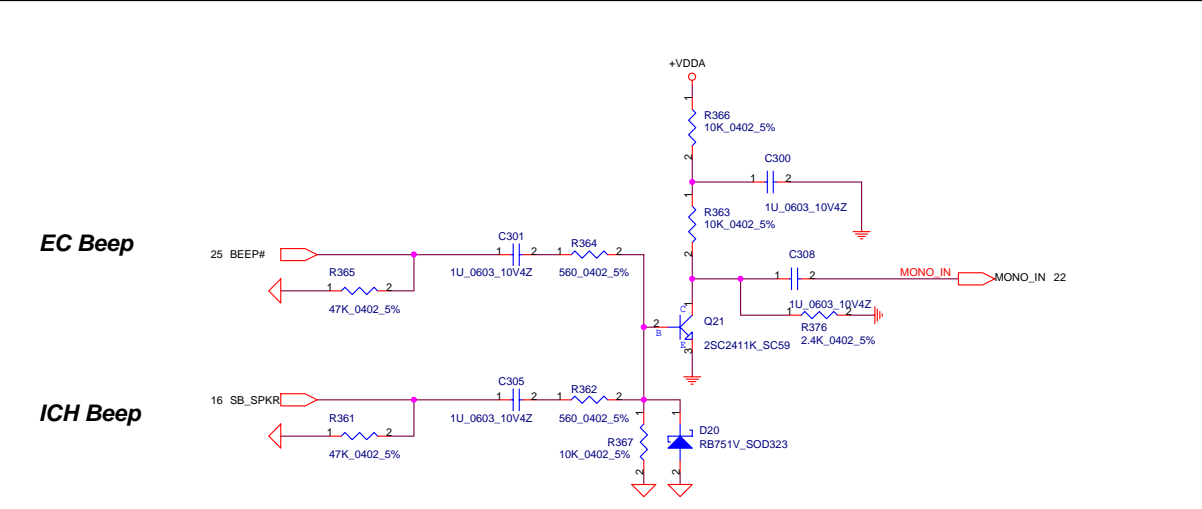
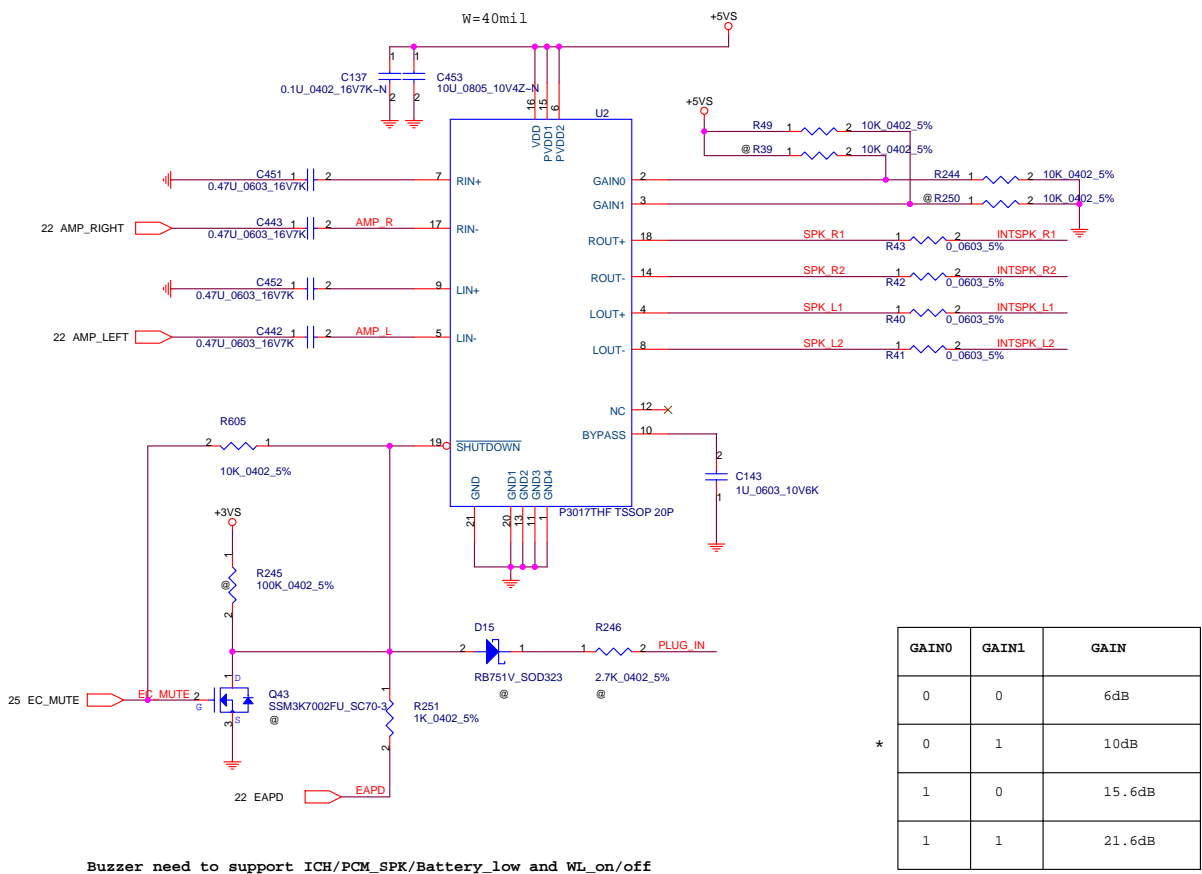
Layout Note: Place close to OZ129 Chipset.



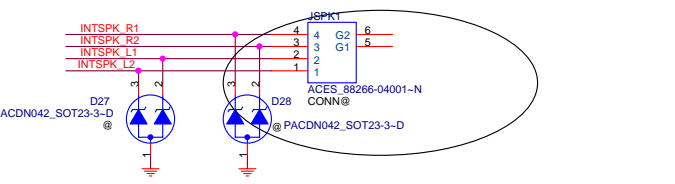
HD Audio Codec



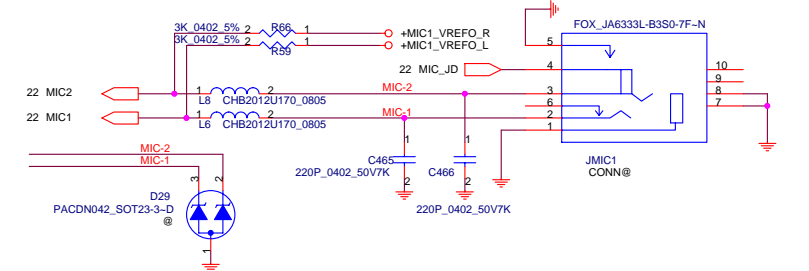
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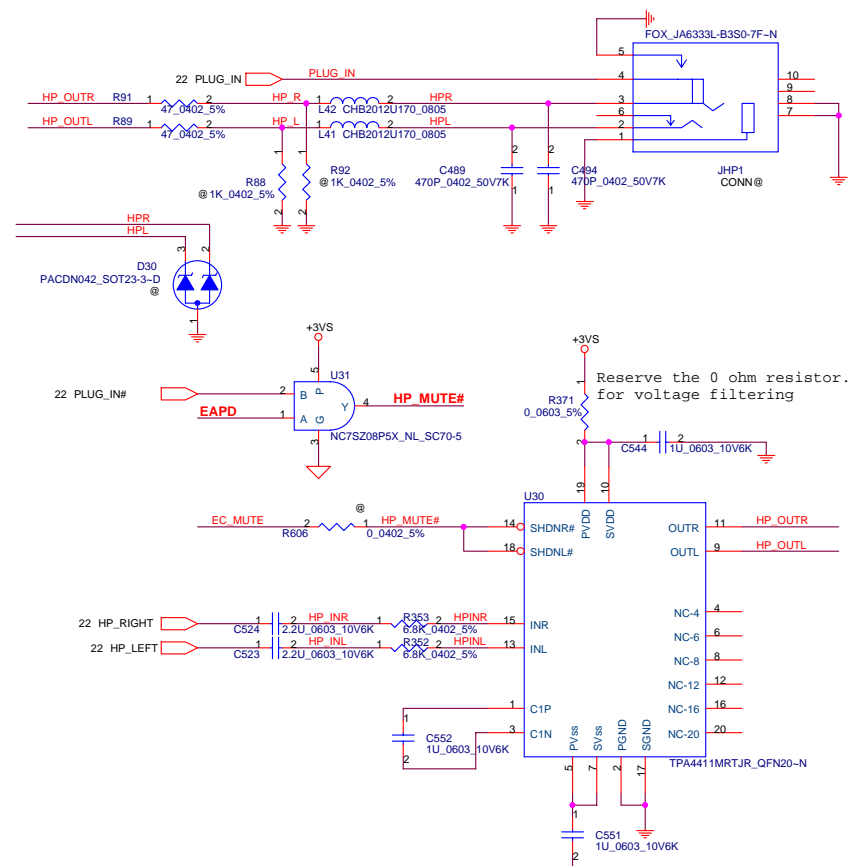
Speaker Connector

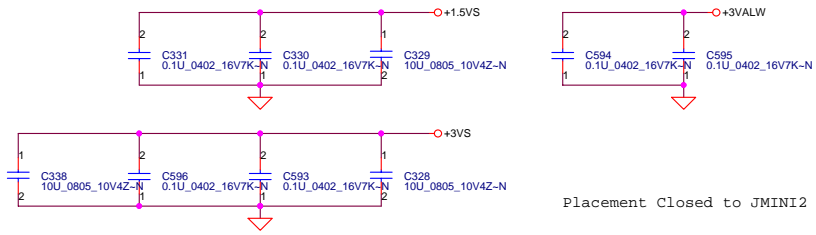


MICROPHONE IN JACK

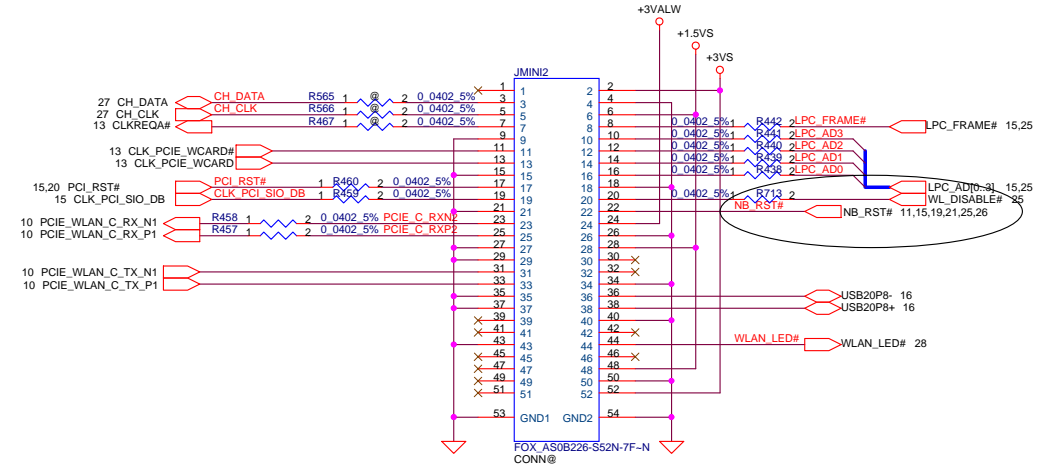


HEADPHONE OUT JACK



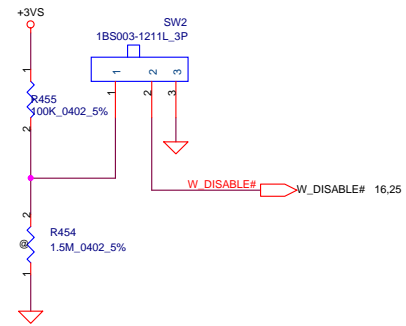


Mini-Express Card (WLAN)

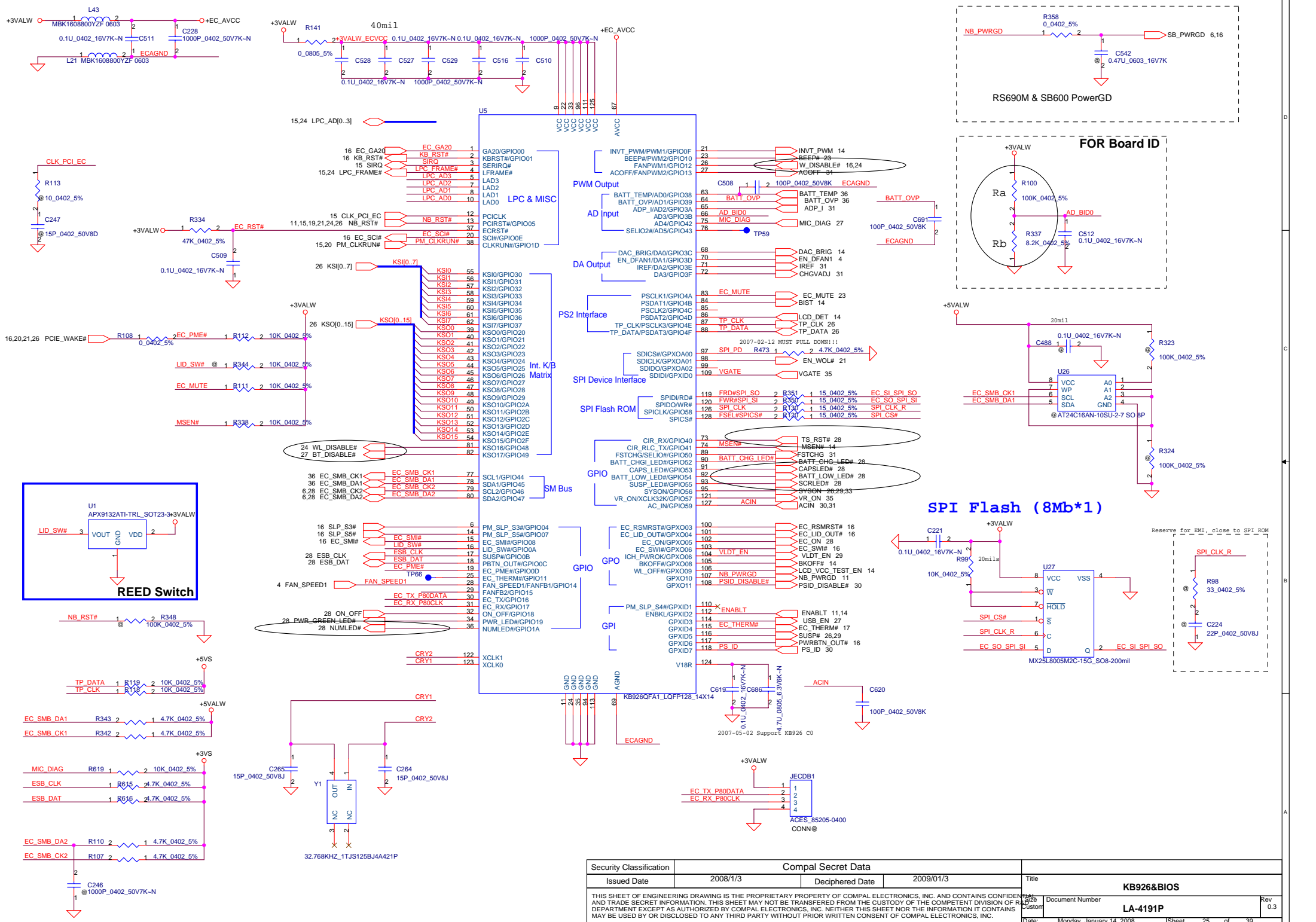


Wireless_BTN

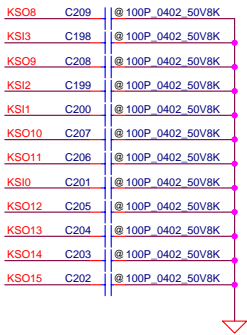
Killer switch



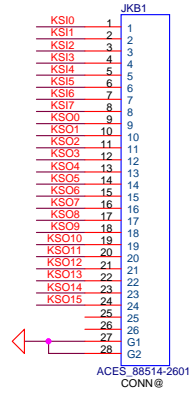
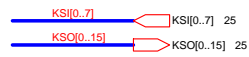
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Title	KB926&BIOS		
Document Number	LA-4191P		
Date	Monday, January 14, 2008	Sheet	25 of 39

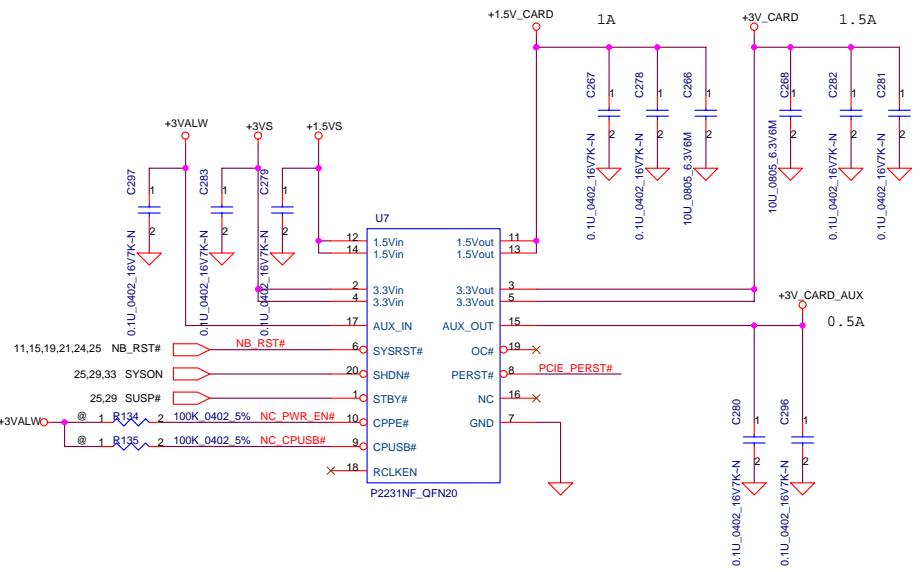
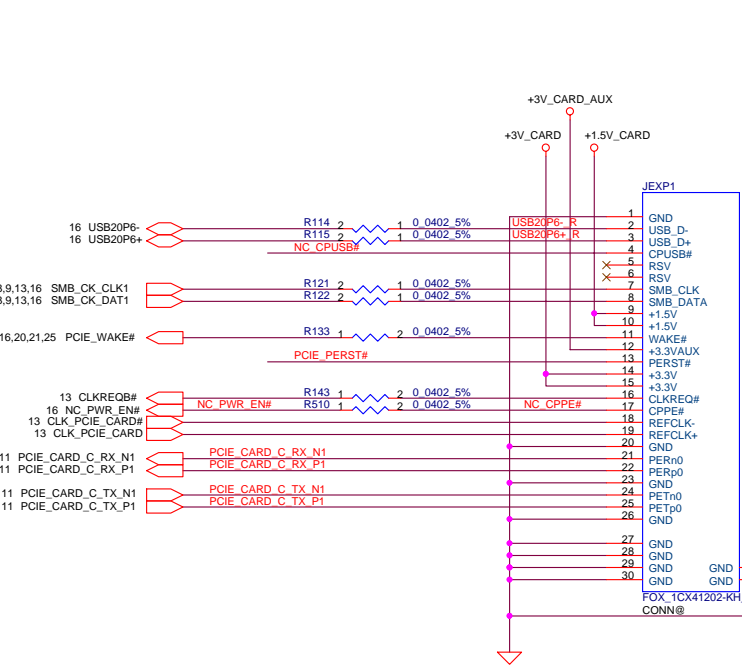
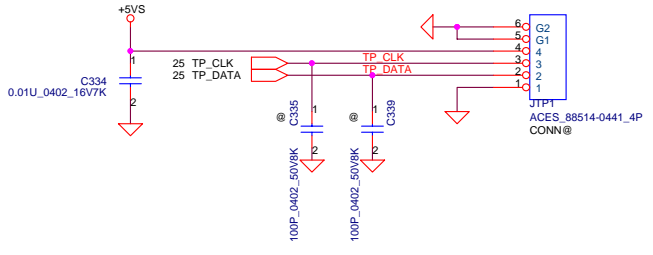


INT_KBD CONN.

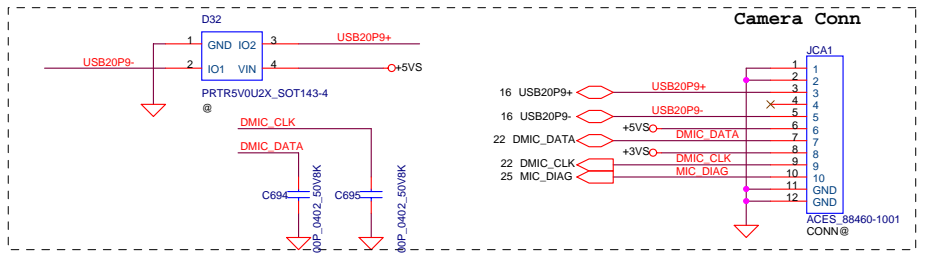
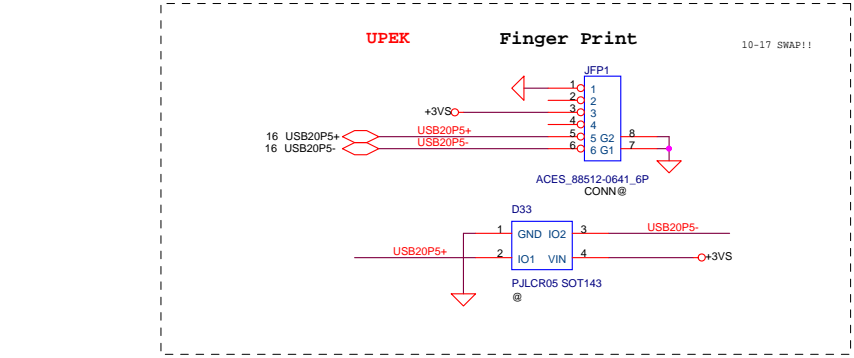
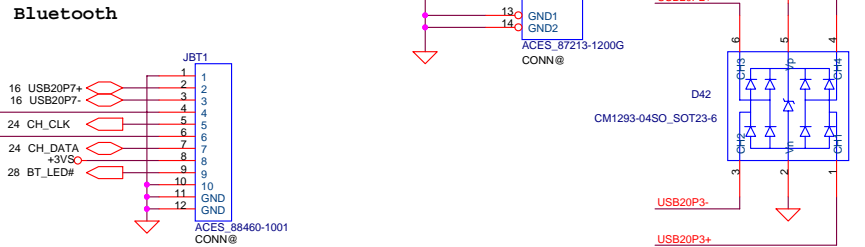
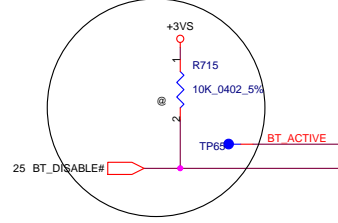
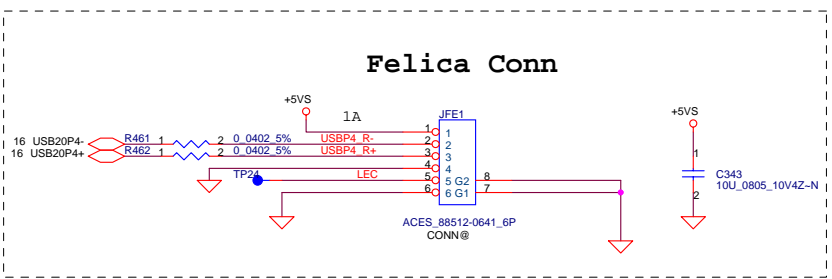
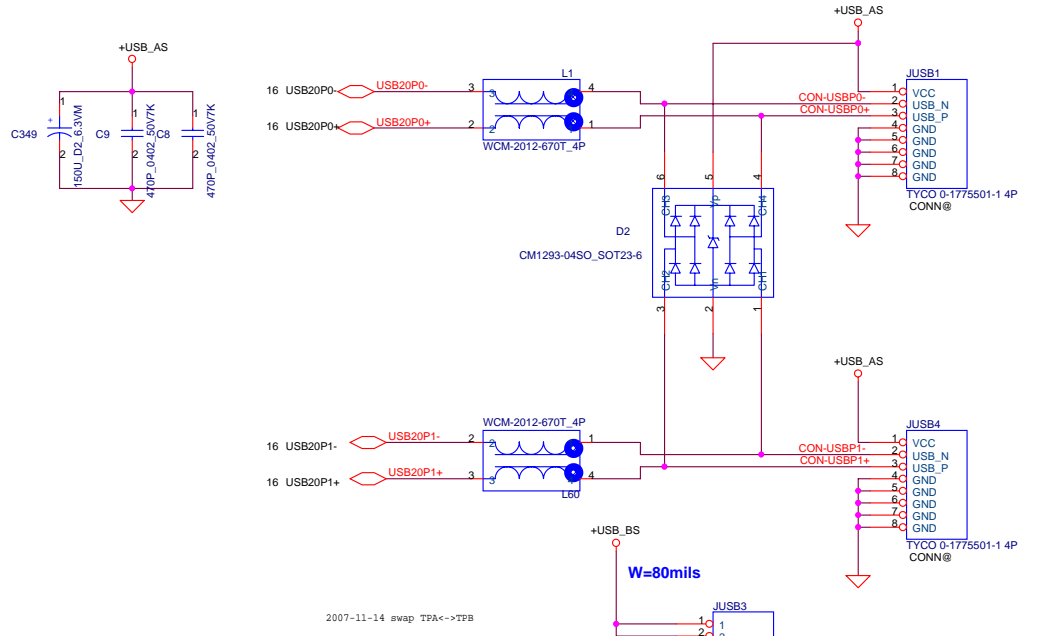
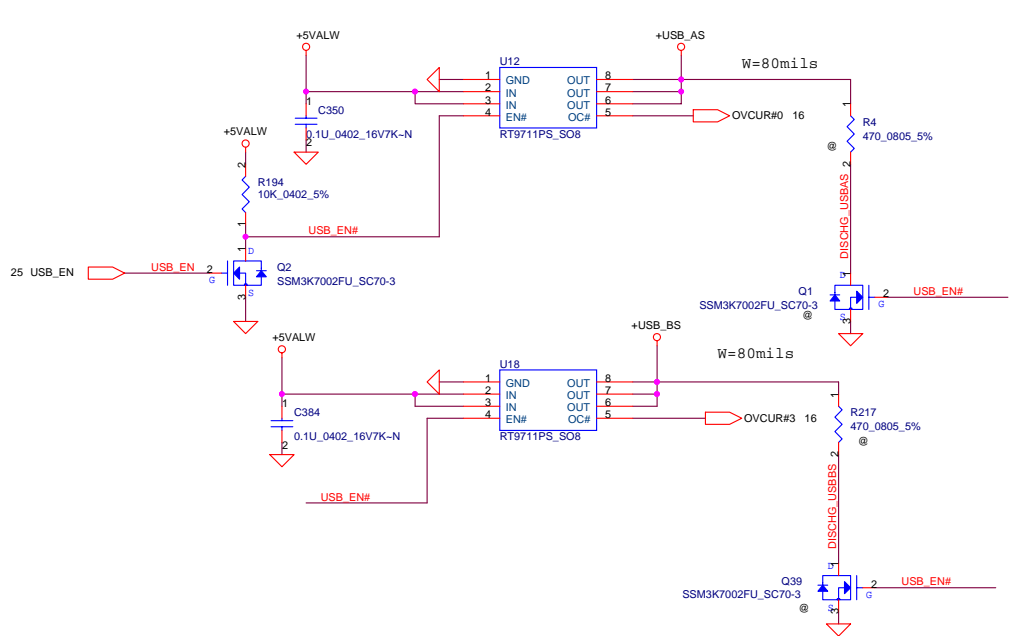


2007-11-15 update to 26pin

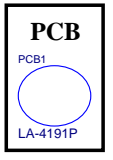
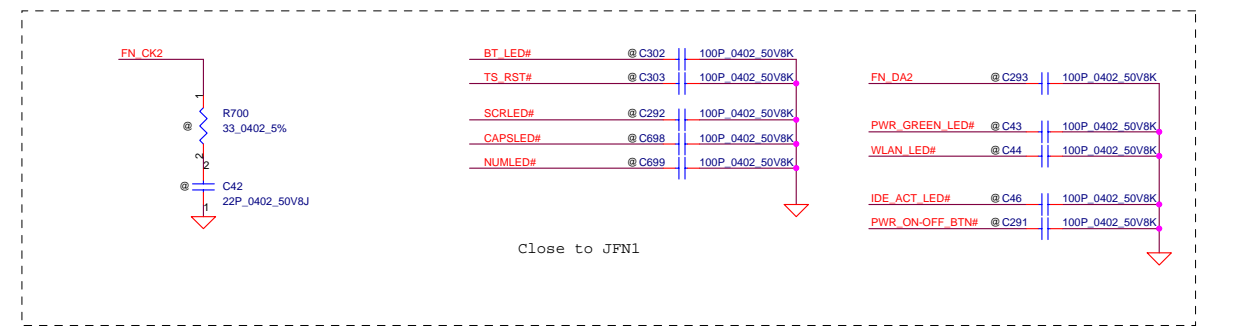
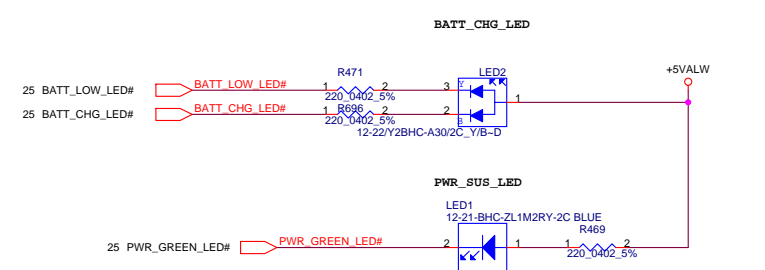
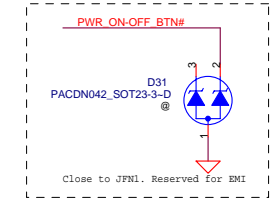
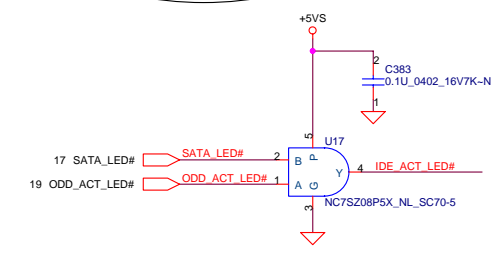
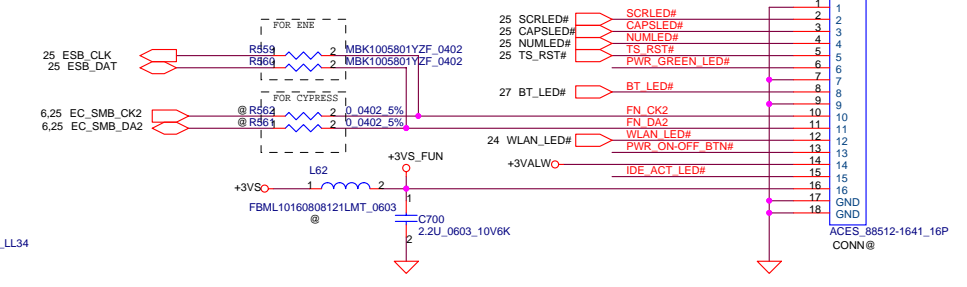
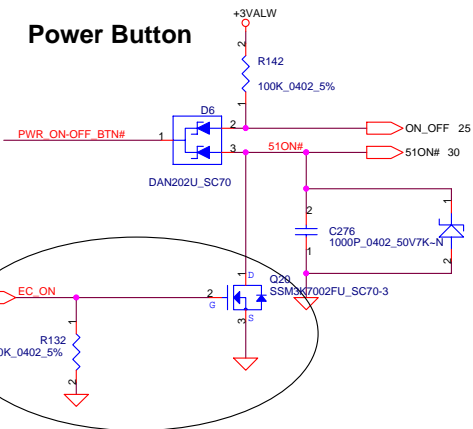
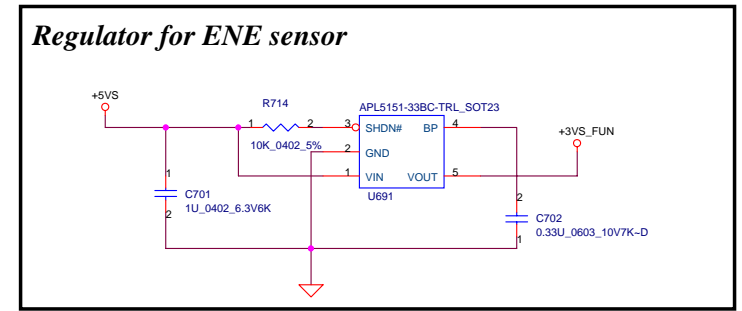
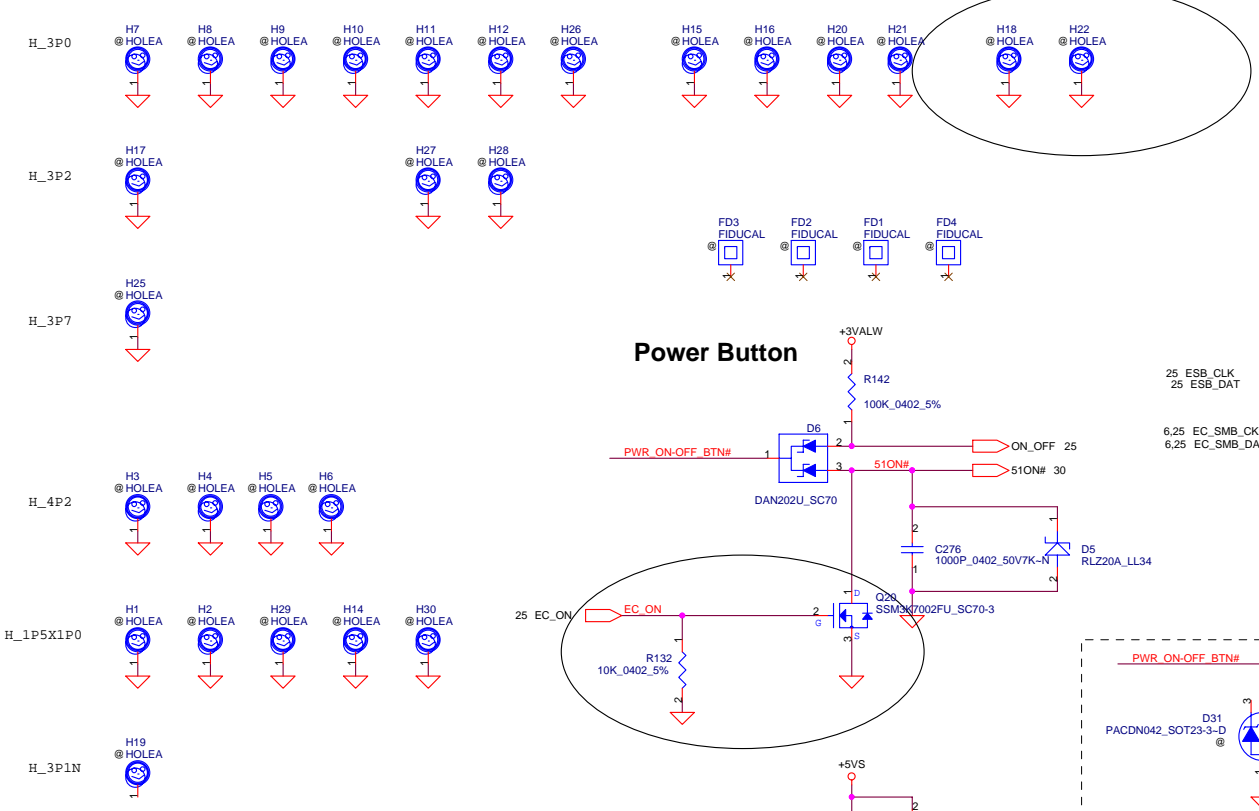
TouchPad TP/B TO M/B



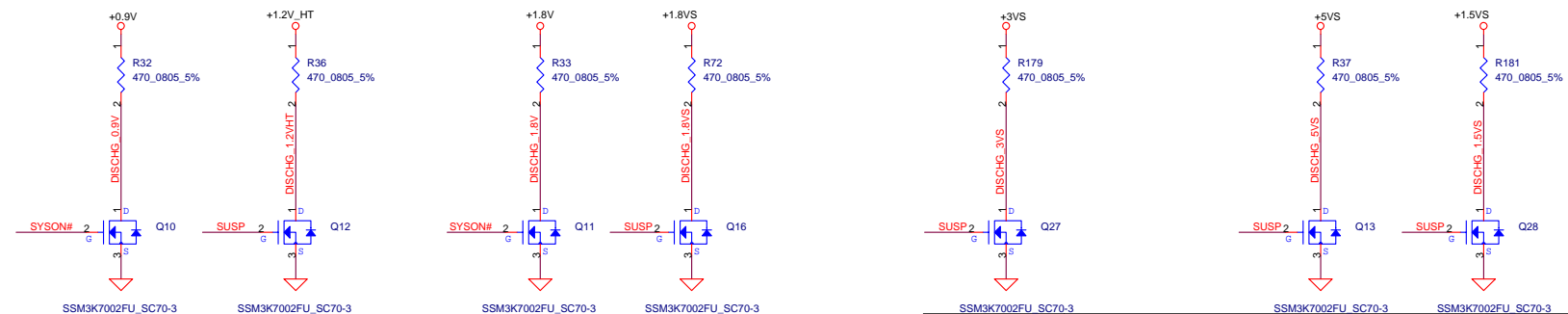
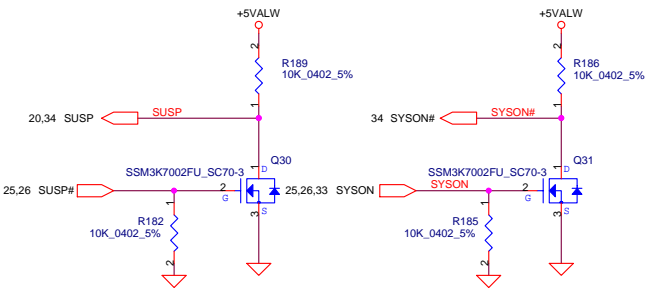
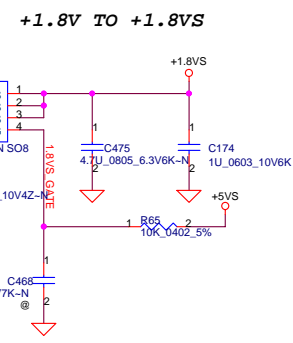
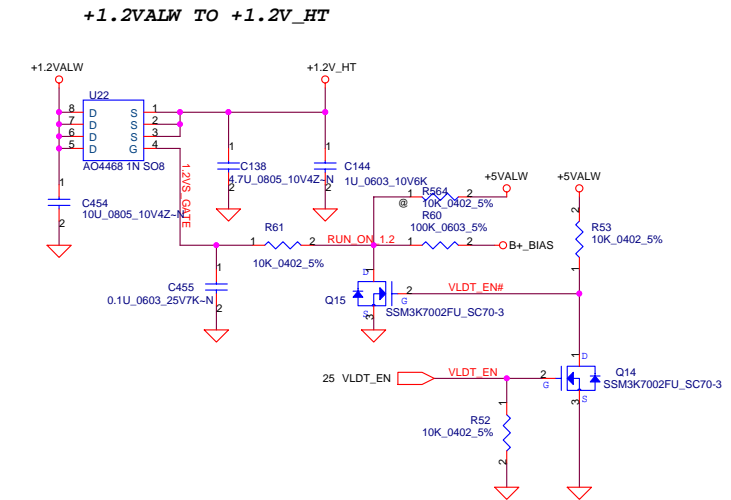
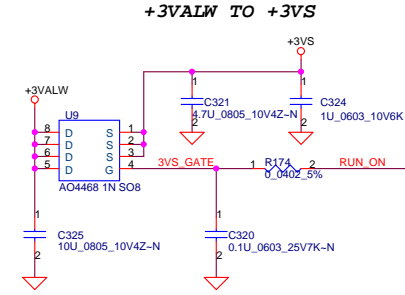
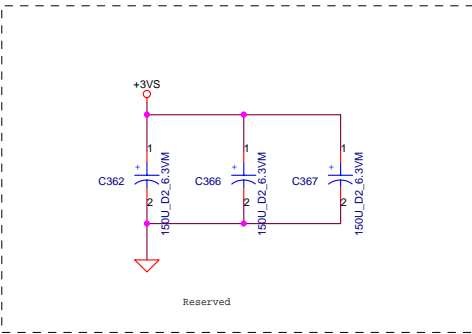
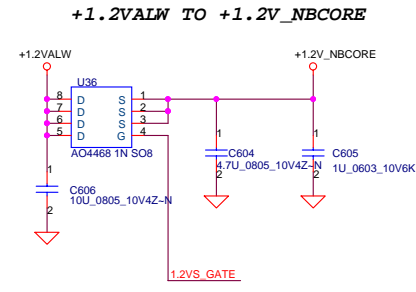
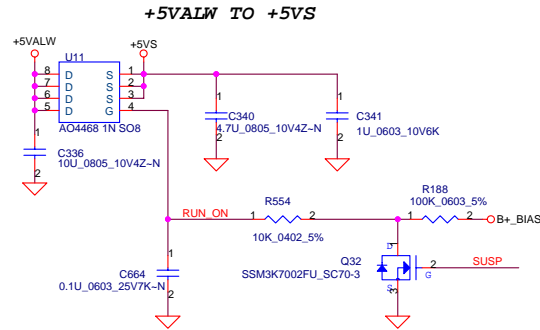
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Issued Date	2008/1/3	Deciphered Date	2009/01/3	Document Number	LA-4191P
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Date:	Monday, January 14, 2008	Sheet	26	of	39



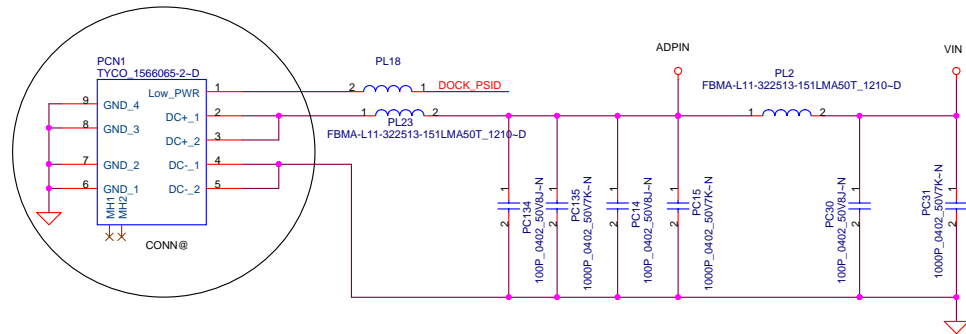
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/1/3	Deciphered Date	2009/01/3	Title
				USB Port
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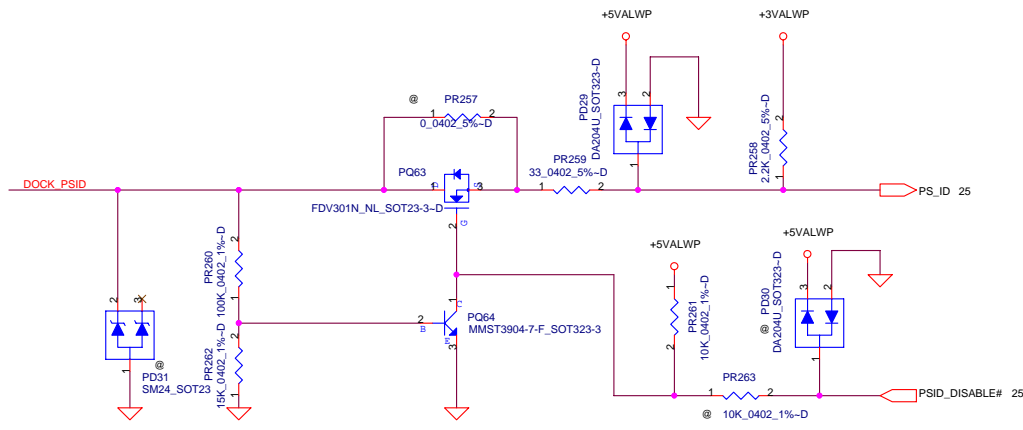
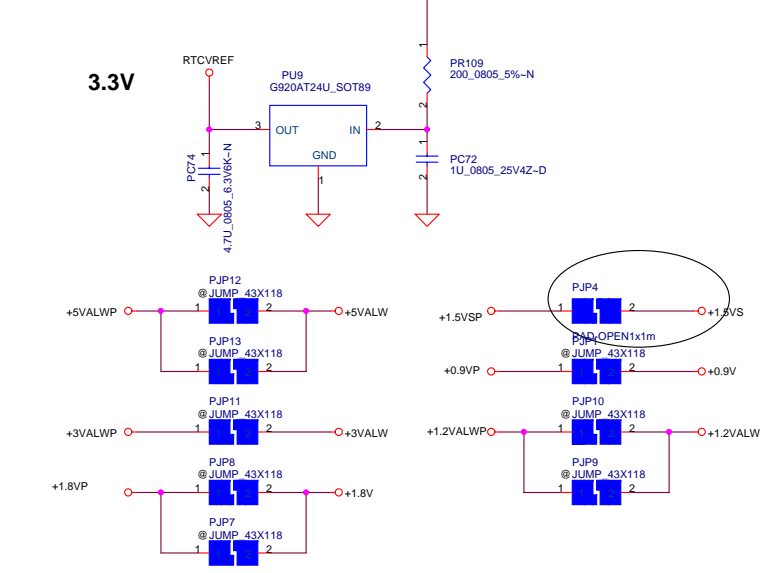
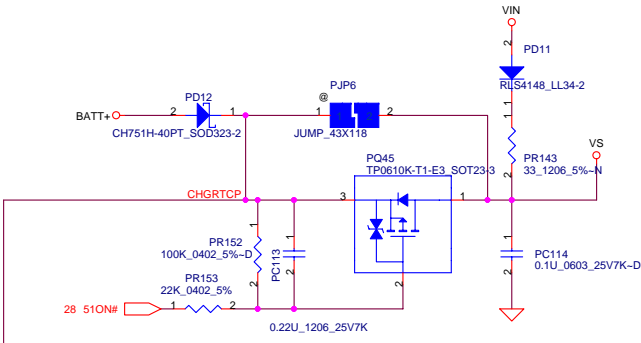
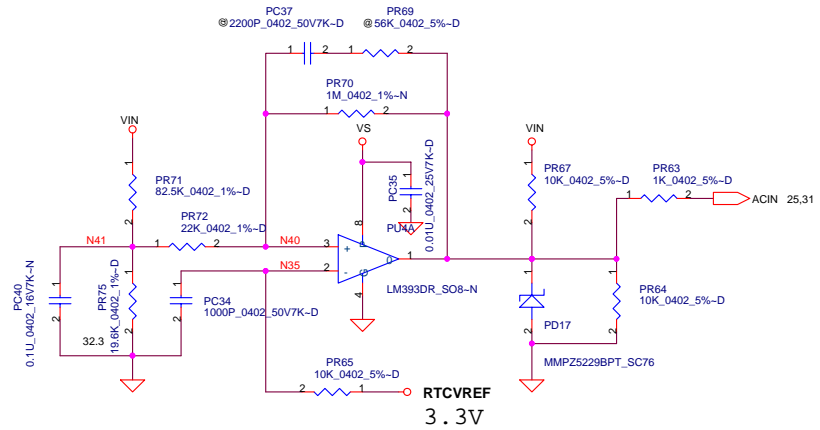
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Date:	Monday, January 14, 2008	Sheet	28	of	39



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Issued Date	2008/1/3	Deciphered Date	2009/01/3	Revision	0.3	Document Number
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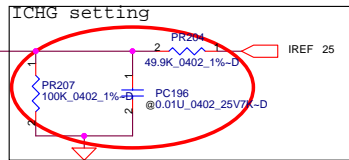
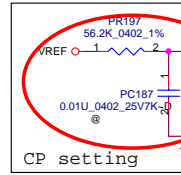
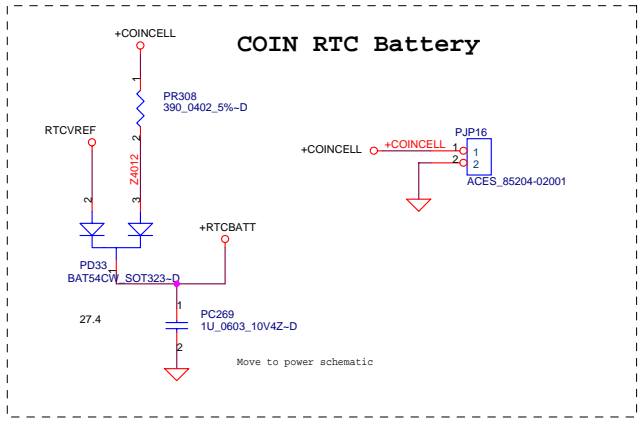
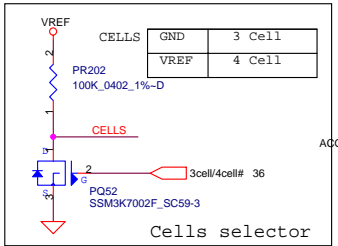


Vin Detector			
	Max.	typ.	Min.
H-->L	18.234	17.841	17.449
L-->H	17.597	17.210	16.813

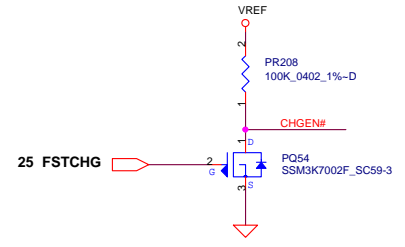
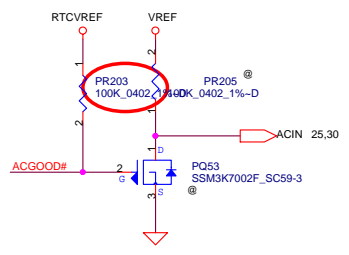
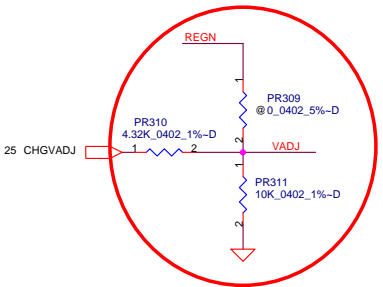


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Date:	Monday, January 14, 2008	Sheet	30 of 39

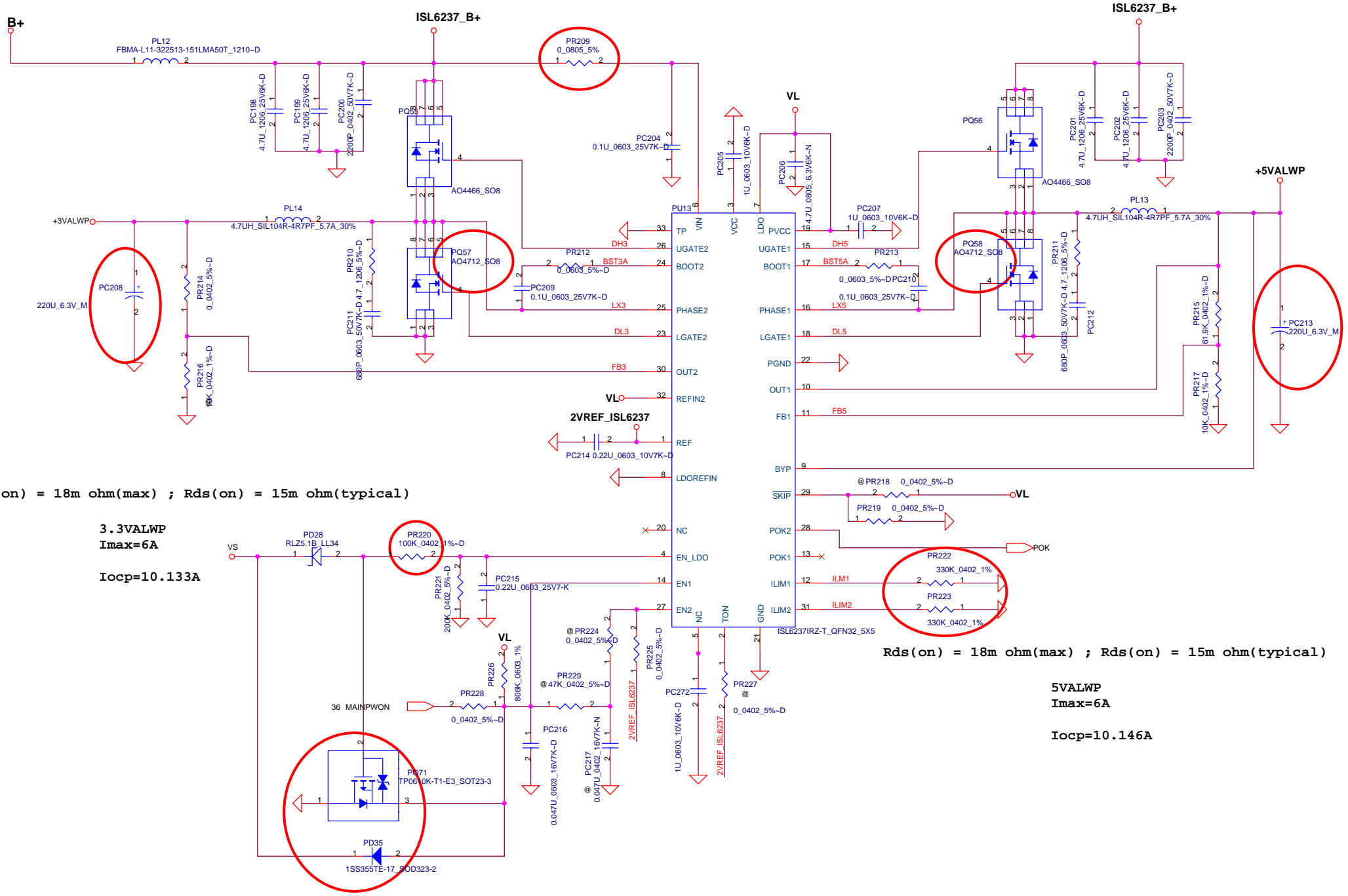
90W adapter
 $I_{charge} = (V_{rsset} / V_{vdac}) * (0.1 / PR195) = 3.3A$
 $I_{adapater} = (V_{acset} / V_{vdac}) * (0.1 / PR188) = 4.26A$
 Input OVP : 22.3V
 Input UVP : 17.26V
 Fsw : 300KHz



IREF	Current
3.265V	3.3A
0.49V	0.5A



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				Rev	0.3
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Rds(on) = 18m ohm(max) ; Rds(on) = 15m ohm(typical)

3.3VALWP
I_{max}=6A
I_{ocp}=10.133A

Rds(on) = 18m ohm(max) ; Rds(on) = 15m ohm(typical)

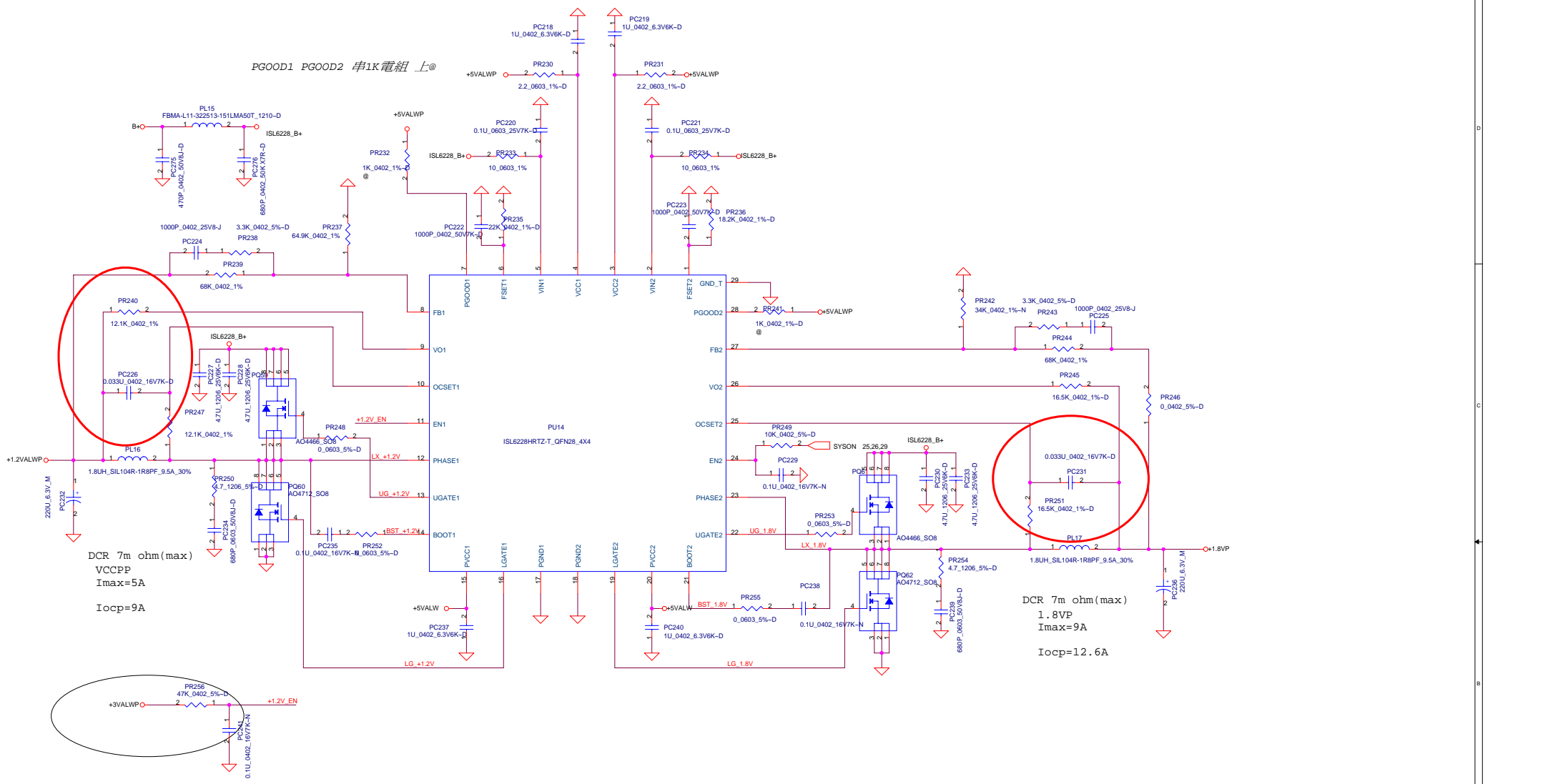
+5VALWP
I_{max}=6A
I_{ocp}=10.146A

Security Classification		Compal Secret Data		Title	
Issued Date	2008/1/3	Deciphered Date	2009/01/3	+3VALWP, +5VALWP	
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Compal Electronics, Inc.

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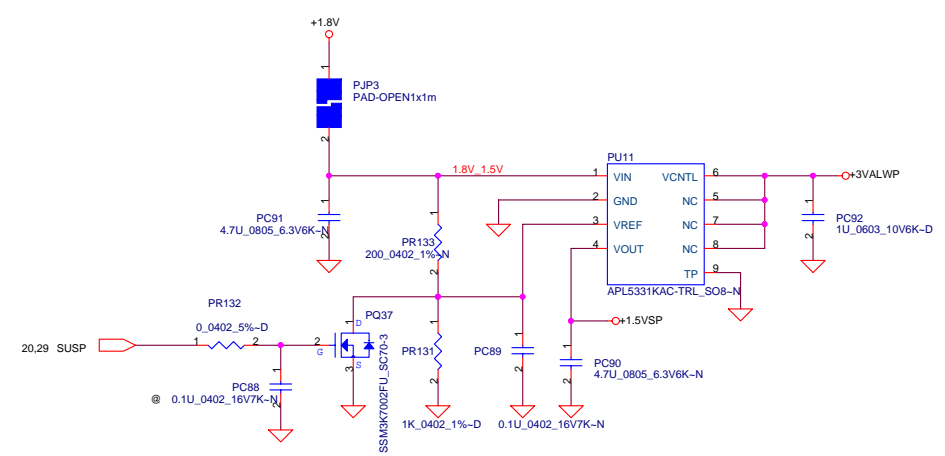
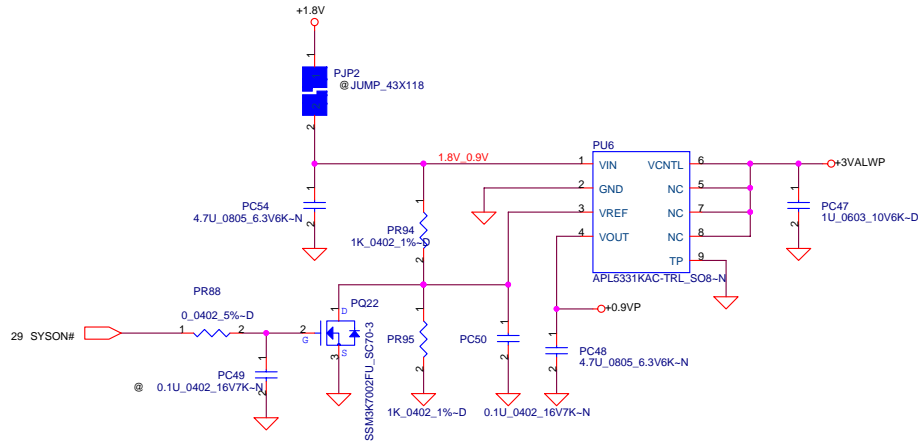


DCR 7m ohm(max)
VCCPP
Imax=5A
Iocp=9A

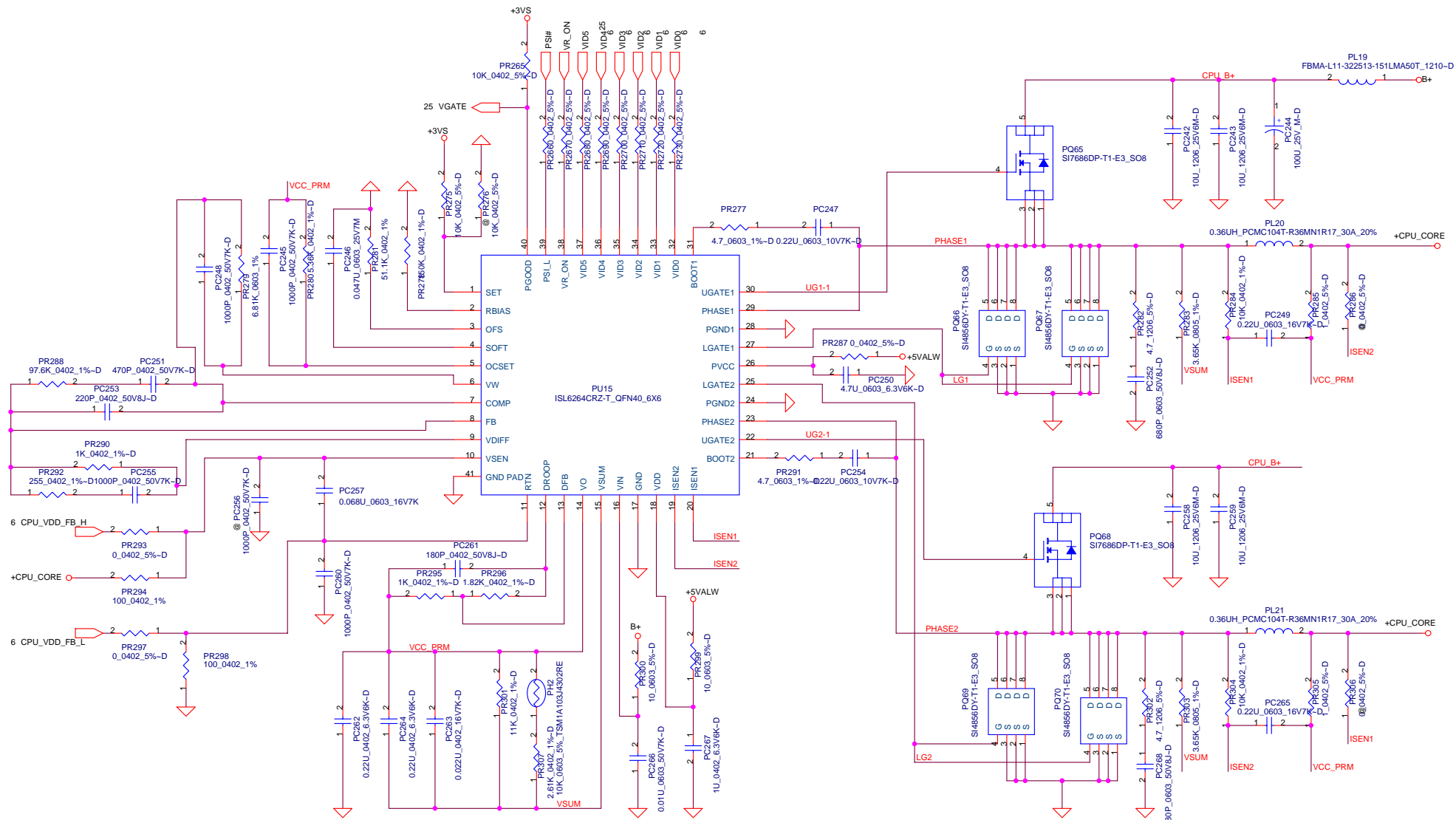
DCR 7m ohm(max)
1.8VP
Imax=9A
Iocp=12.6A

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Issued Date	2008/1/3	Deciphered Date	2009/01/3
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Size	Document Number JBL30	Rev 0.3	Date: Monday, January 14, 2008 Sheet 33 of 39

+1.5VSP/+0.9VSP

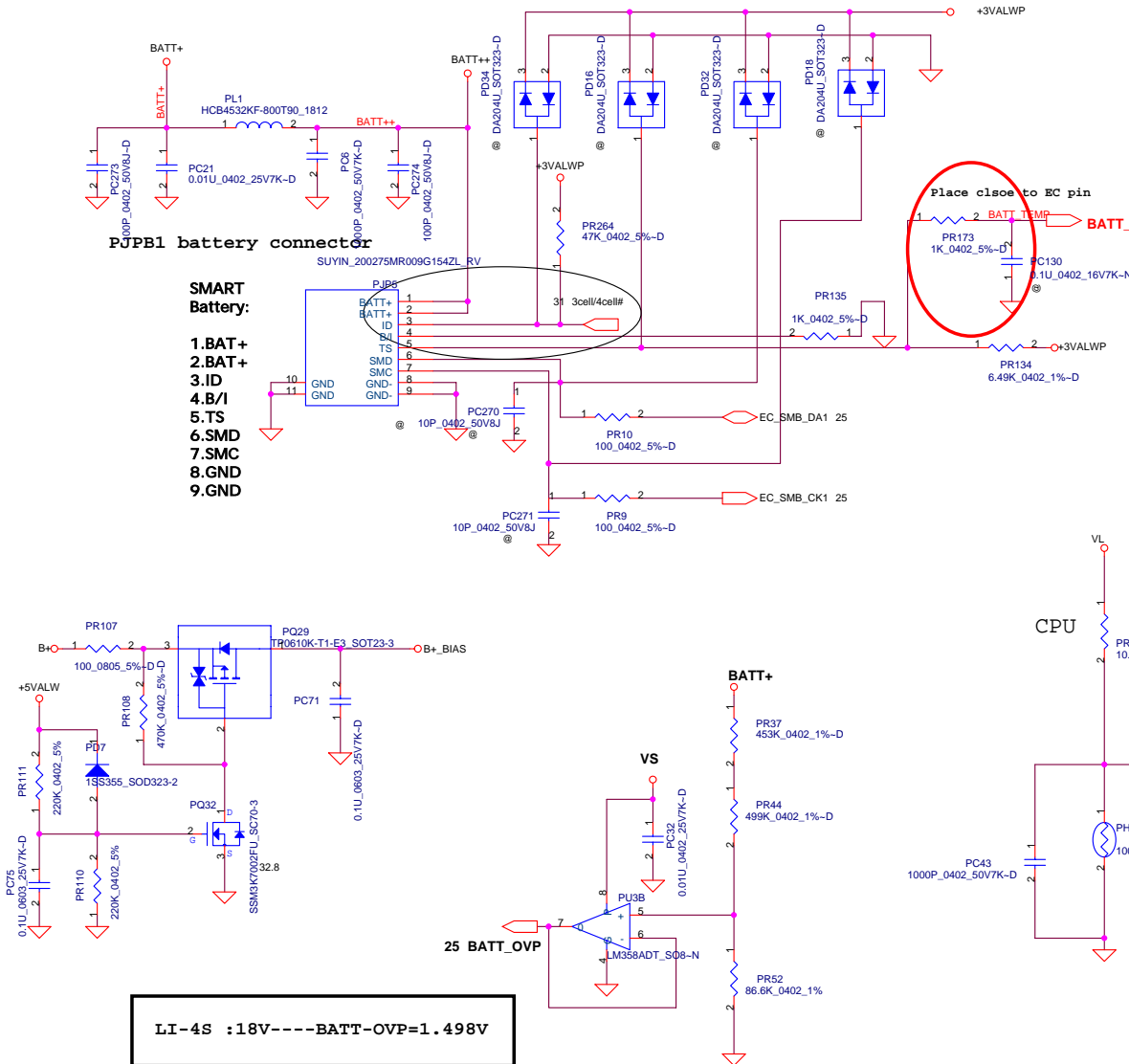


Security Classification	Compal Secret Data			Title	+1.5VSP/+0.9VSP	
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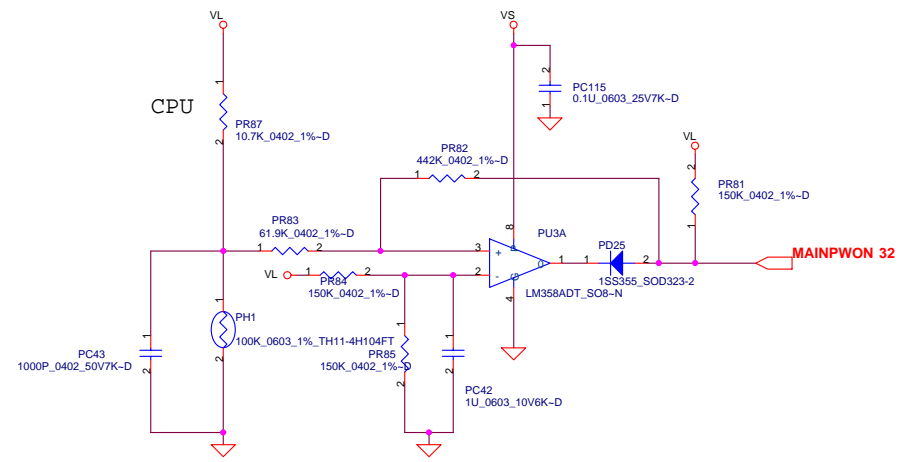
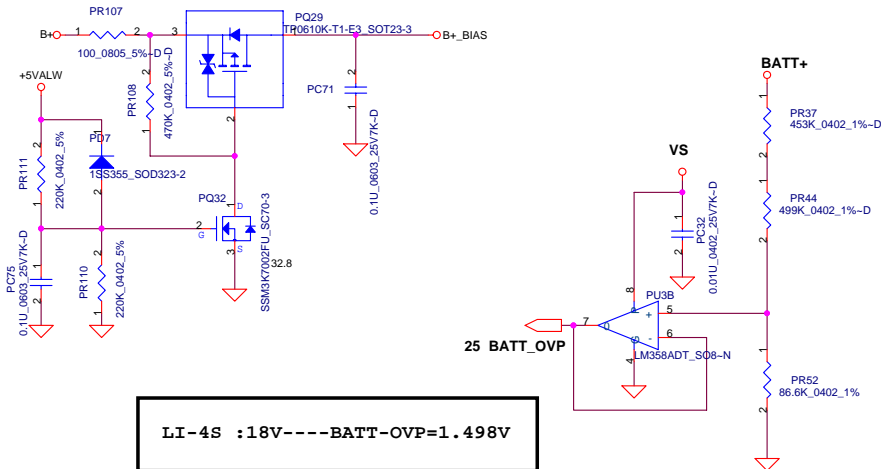
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Issued Date	2008/1/3	Deciphered Date	2009/01/3	+CPU_CORE
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Battery Connect/OTP



CPU

PH1 under CPU bottom side :
 CPU thermal protection at 90 degree C
 Recovery at 50 degree C



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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	31	Charge	08/01/04	COMPAL	adjust battery charge voltage set	CHANGE PR310 from 15K to 4.3K	
2	31	Charge	08/01/04	COMPAL	VIN Detector has the same function	DEL PR205 PQ53	
3	32	+3VALWP/+5VALWP	08/01/04	COMPAL	When in the DC-mode , shut down the system ,5valwp output not turn off	ADD PD35 to turn off 5VALWP wehn shut down the system in the DC-mode	

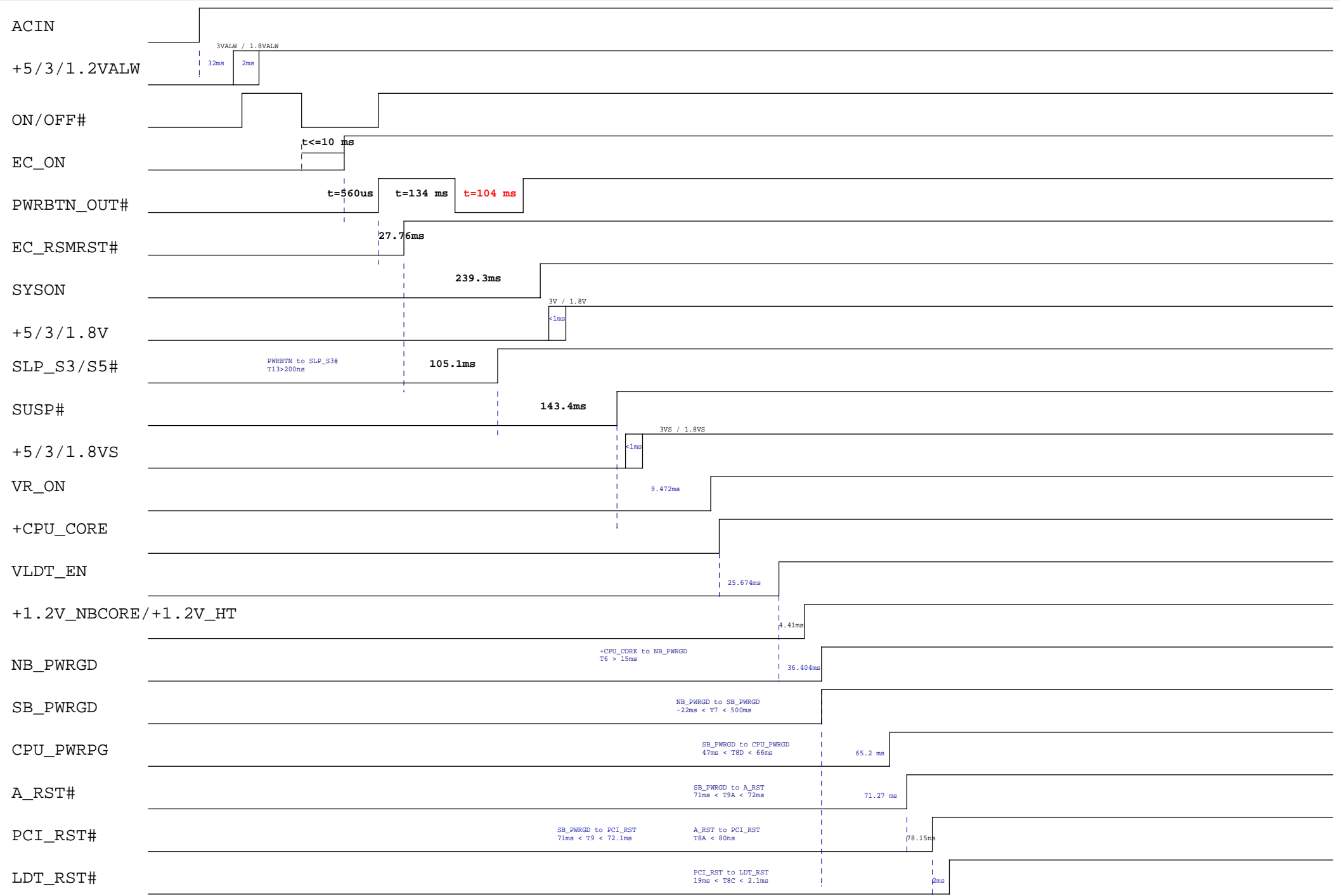
Next: PR238, PC202, PQ56, PD42, PJP21

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Compal Electronics, Inc.	
Title	EE-PIR
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List
1	Fine-tune CPU_PWRGD,LDT_STOP#,LDT_RST#	Fine-tune CPU_PWRGD,LDT_STOP#,LDT_RST#	0.2	6	Delete CPU testpad
2		Reserve LCD enable from EC for test panel function	0.2	14	Add BIST and LCD_DET and LCD_VCC_TEST_EN from EC
3		Change RTC battery to cable type, also change to PWR portion	0.2	15	
4		Change CLK_PCI_TPM and CLK_PCI_EC to PCICLK5 and 6 (ATI recommend)	0.2	15	
5		Modify Media card circuit to OZ129	0.2	20	Modify Media card circuit to OZ129
6		Change Audio codec LDO to RT9198-4GPBG	0.2	22	Change Audio codec LDO to RT9198-4GPBG
7		USB port power control by EC	0.2	27	USB_EN(High=Enable)
8		CAPS,NUM,SCR LED control change from touch sensor to EC	0.3	28	
9		RTL8102E ver.B have E-fuse to flash MAC address.	0.3	21	U16 change to DNI (@)
10		Change RJ45 connector to include LED type.	0.3	21	
11					
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Issued Date	2008/1/3	Deciphered Date	2009/01/3	PIR (HW)	
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Issued Date	2008/1/3	Deciphered Date	2009/01/3	Title	Power Sequence
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				LA-4191P	
				Date	Monday, January 14, 2008
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				Rev	0.3