

Compal confidential

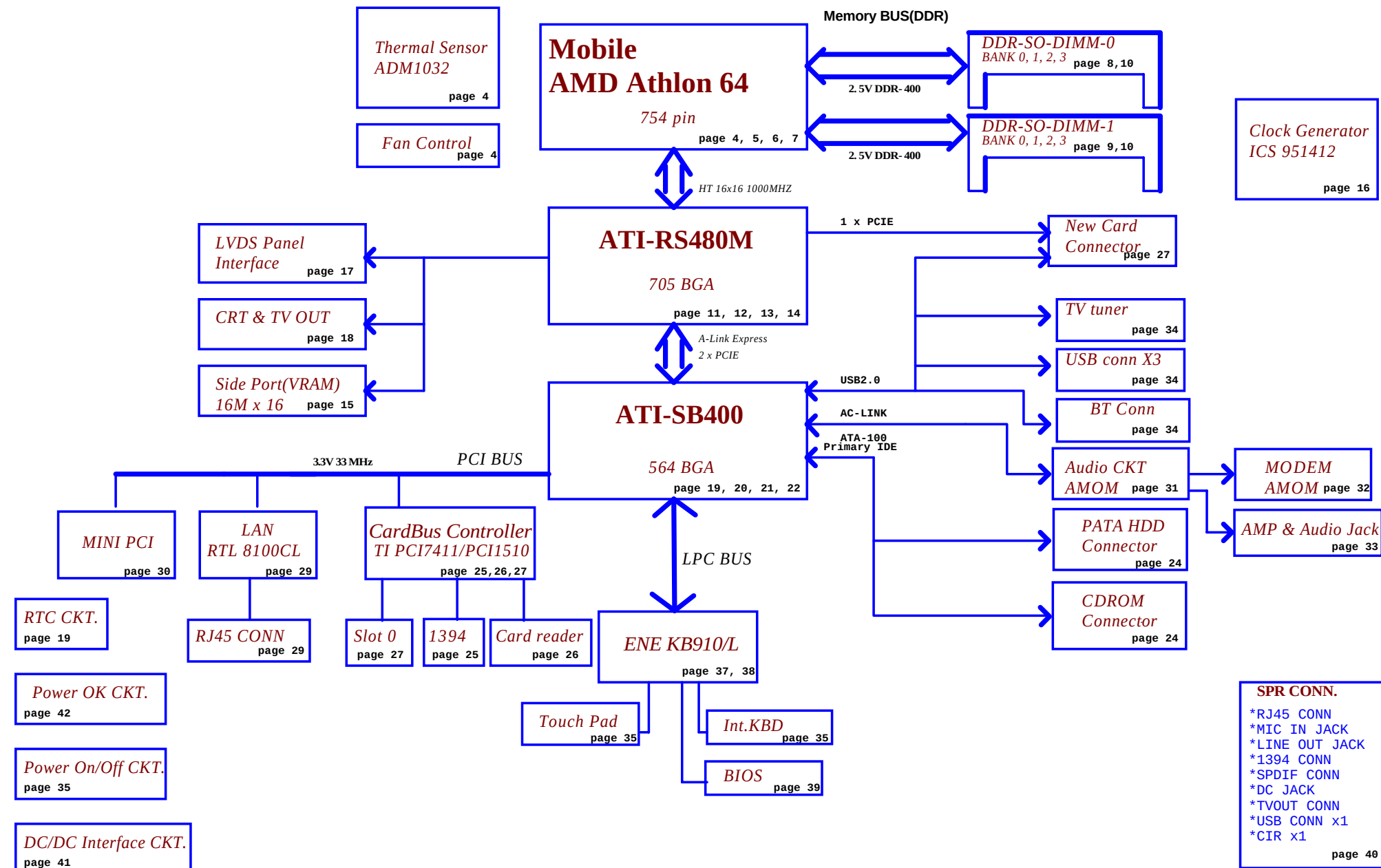
Schematics Document

AMD K8 with
ATI RS480M+ATI SB400

2006 - 03 - 06
REV:1.0



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Voltage Rails

power plane State	+12VALW +5VALW +3VALW +1.8VALW	+5V +2.5V +1.25V	+5VS +3VS +2.5VS +1.8VS +1.5VS +2.5VDDA +CPU_CORE +1.2V_HT
S0	0	0	0
S1	0	0	0
S3	0	0	X
S5 S4/AC	0	X	X
S5 S4/AC don't exist	X	X	X

0 MEANS ON

X MEANS OFF

PCI Devices

INTERNAL DEVICE	IDSEL #	REQ/GNT #	PIRQ
SMBUS			
IDE			A
LPC I/F			
PCI to PCI			
AC97 AUDIO			B
AC97 MODEM			B
OHCI#1 USB			D
OHCI#1 USB			D
EHCI USB			D
SATA#1			A
SATA#2			A
EXTERNAL			
Wireless LAN	AD18	3	F
LAN	AD22	1	G
CARD BUS & 1394	AD20	2	E,H

BOM STATUS :

VRAM@ ,VRAMIC@, SAMSUNG@, HYNIX@, 2HDD@ ,7411@ ,EXP@ ,17_EXP@ ,15_EXO@,CIR@ ,D@, C@, 15.4@, DOCK@, WL_LED@

45@ (for 45 level RTC battery)

HAL10 17" VRAM@ , SAMSUNG@, HYNIX@, 2HDD@ ,7411@ ,EXP@ ,17_EXP@ ,CIR@ ,D@ ,DOCK@,WL_LED@

HAL20 FF 15.4" VRAM@ , SAMSUNG@, HYNIX@, 2HDD@ ,7411@ ,EXP@ ,15_EXP@ ,CIR@ ,C@ ,DOCK@,WL_LED@, 15.4@(LED)

HAL20 DF 15.4" EXP@, C@ ,DOCK@ ,15.4@(LED), CIR@, WLAN@, 15_EXP@

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22Z1
LA-3181P Rev0

<11> H_CADIP[0..15] H_CADIP[0..15]
<11> H_CADIN[0..15] H_CADIN[0..15]

H_CADOP[0..15] H_CADOP[0..15] <11>
H_CADON[0..15] H_CADON[0..15] <11>

Claw Hammer-DTR

HTT Interface

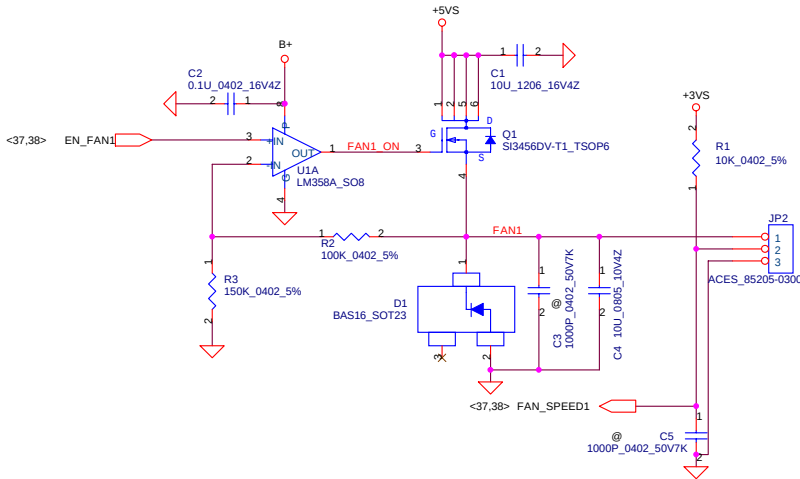
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H_CADIP14 U27 L0_CADIN_H14
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H_CADIP13 V25 L0_CADIN_H13
H_CADIN13 U25 L0_CADIN_L13
H_CADIP12 W27 L0_CADIN_H12
H_CADIN12 W26 L0_CADIN_L12
H_CADIP11 AA27 L0_CADIN_H11
H_CADIN11 AA26 L0_CADIN_L11
H_CADIP10 AB25 L0_CADIN_H10
H_CADIN10 AA25 L0_CADIN_H9
H_CADIP9 AC27 L0_CADIN_L9
H_CADIN9 AC26 L0_CADIN_H8
H_CADIP8 AD25 L0_CADIN_L8
H_CADIN8 AC25 L0_CADIN_H7
H_CADIP7 T27 L0_CADIN_L7
H_CADIN7 T28 L0_CADIN_H6
H_CADIP6 V29 L0_CADIN_L6
H_CADIN6 U29 L0_CADIN_H5
H_CADIP5 V27 L0_CADIN_L5
H_CADIN5 V28 L0_CADIN_H4
H_CADIP4 Y29 L0_CADIN_L4
H_CADIN4 W29 L0_CADIN_H3
H_CADIP3 AB29 L0_CADIN_L3
H_CADIN3 AA29 L0_CADIN_H2
H_CADIP2 AB27 L0_CADIN_L2
H_CADIN2 AB28 L0_CADIN_H1
H_CADIP1 AD29 L0_CADIN_L1
H_CADIN1 AC29 L0_CADIN_H0
H_CADIP0 AD27 L0_CADIN_L0
H_CADIN0 AD28 L0_CADIN_L0

N26 H_CADOP15
N27 H_CADON15
L25 H_CADOP14
M25 H_CADON14
L26 H_CADOP13
L27 H_CADON13
J25 H_CADOP12
K25 H_CADON12
G25 H_CADOP11
H25 H_CADON11
G26 H_CADOP10
G27 H_CADON10
E25 H_CADOP9
F25 H_CADON9
E26 H_CADOP8
E27 H_CADON8
N29 H_CADOP7
P29 H_CADON7
M28 H_CADOP6
M27 H_CADON6
L29 H_CADOP5
K28 H_CADON5
K27 H_CADON4
H28 H_CADOP3
H27 H_CADON3
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H29 H_CADON2
F28 H_CADOP1
F27 H_CADON1
E29 H_CADOP0
E29 H_CADON0

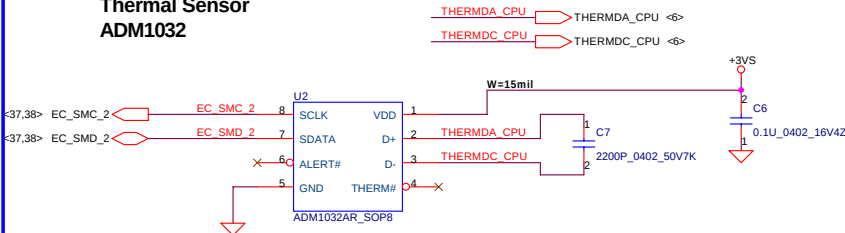
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L0_CLKOUT_H0 J29 H_CLKOP0 H_CLKON1 <11>
L0_CLKOUT_L0 K29 H_CLKON0 H_CLKON0 <11>
N25 X P25 X
P28 H_CTLOP0 H_CTLOP0 <11>
P27 H_CTLOP0 H_CTLOP0 <11>
A27 LDTSTOP# LDTSTOP# <13,19>
R8 680_0402_5% +2.5VS

FOX_P275403-2941-42

Fan Control Circuit

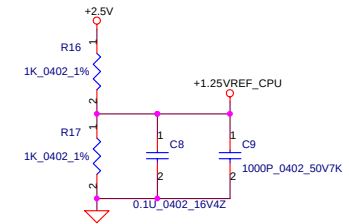
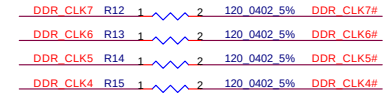
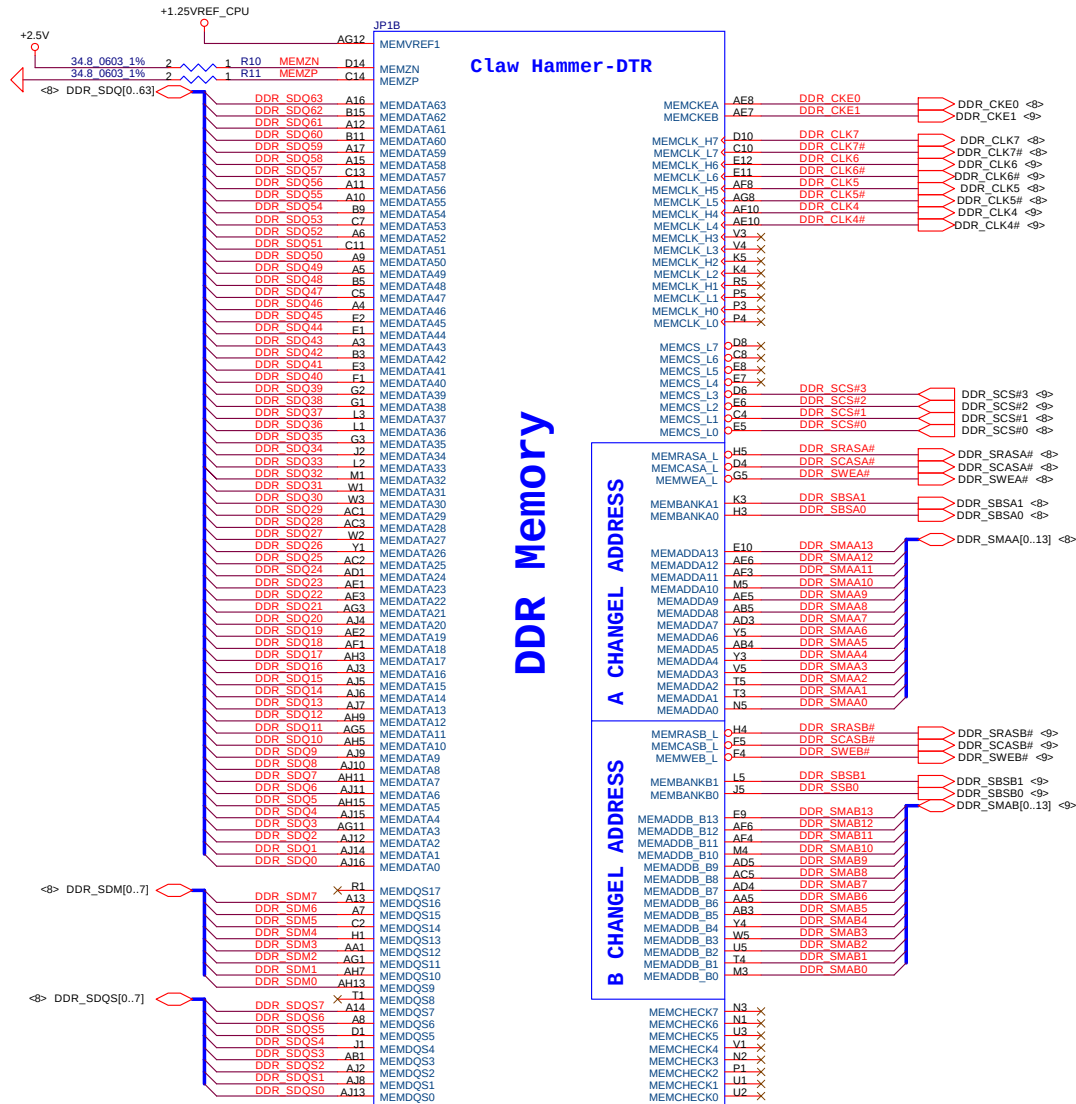


Thermal Sensor ADM1032



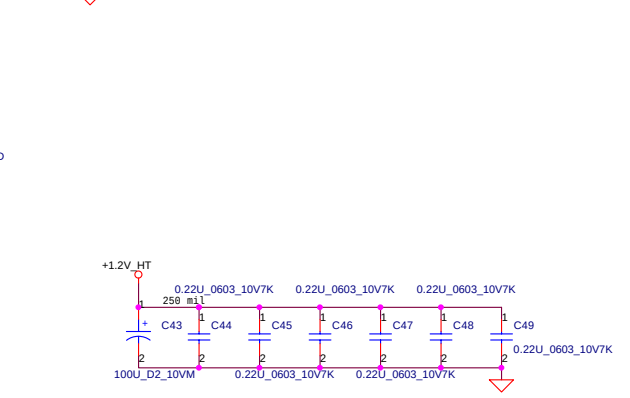
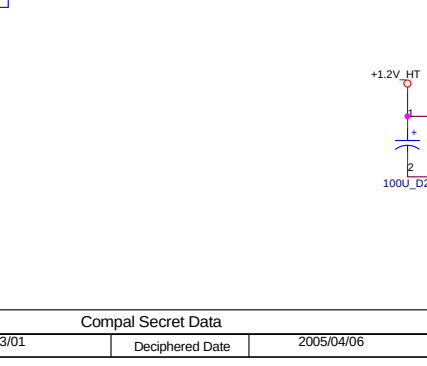
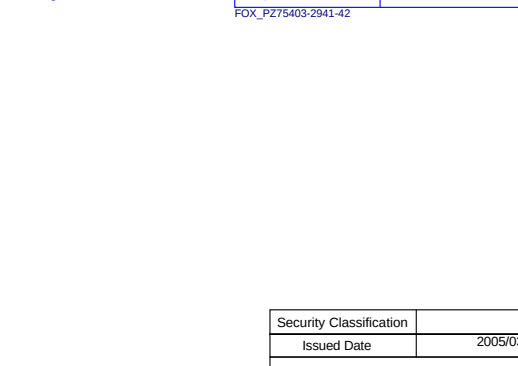
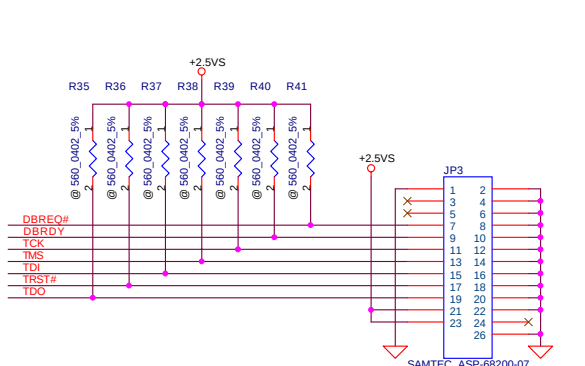
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50 mil width/20 mil space

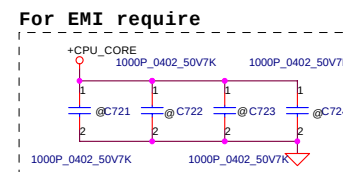
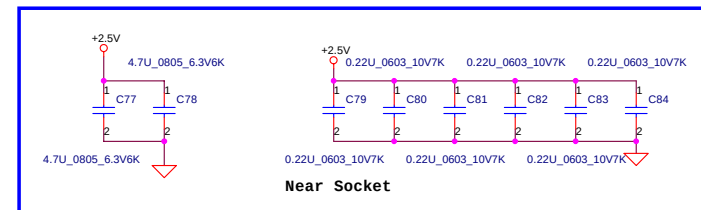
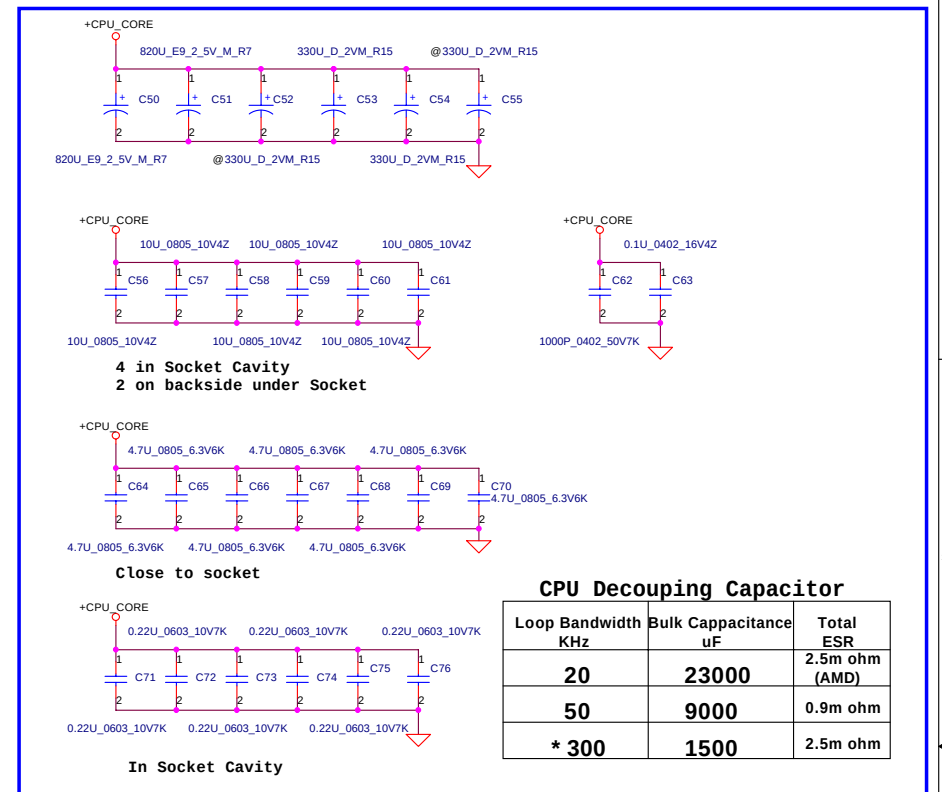
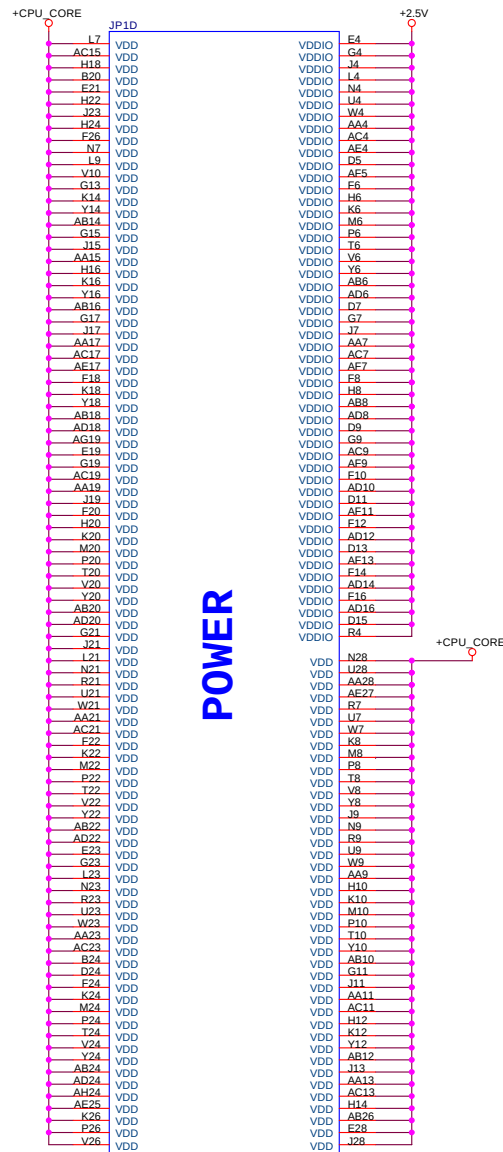
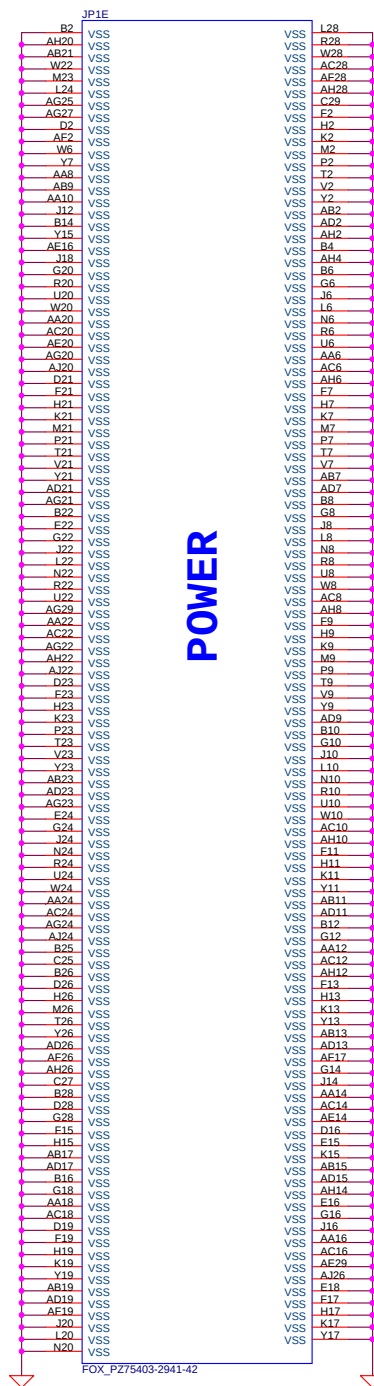


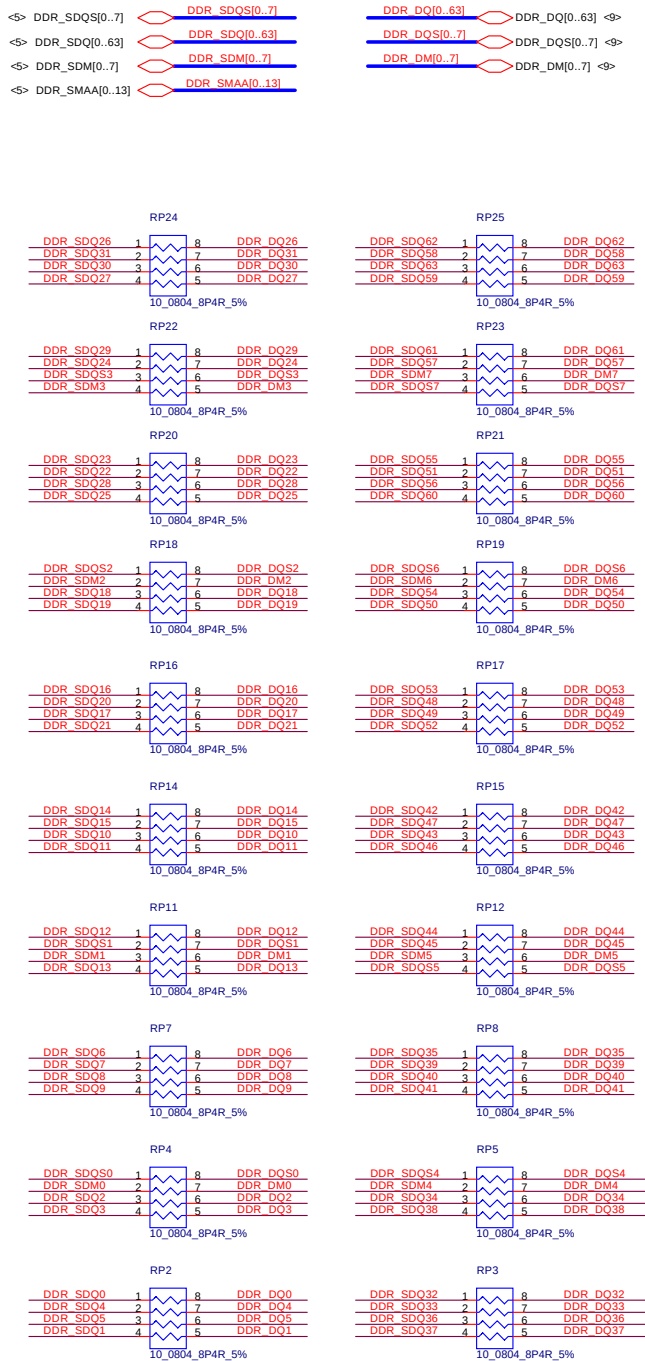
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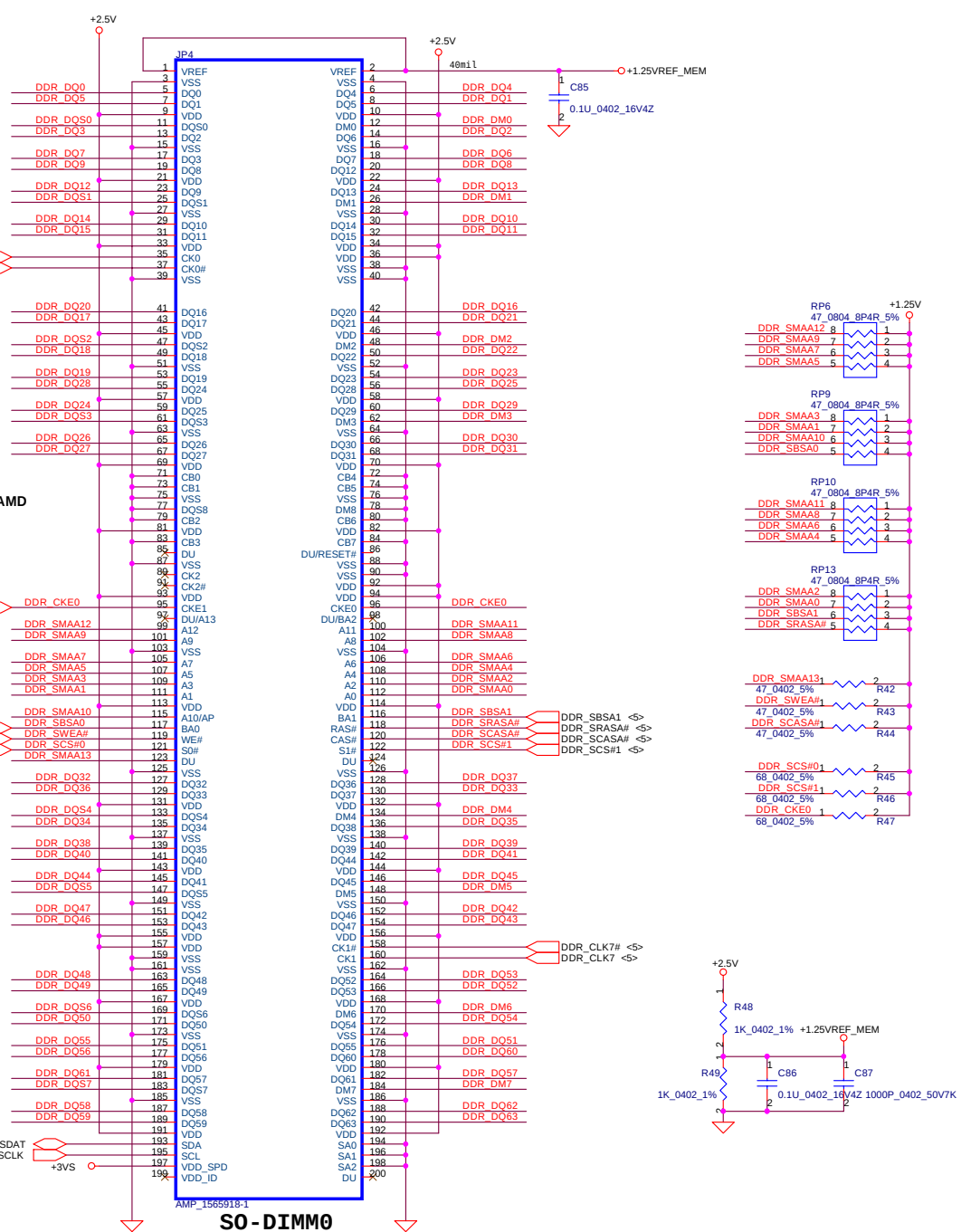




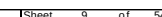
Note:
DDR_SMAA13 Recommend for AMD

Layout note

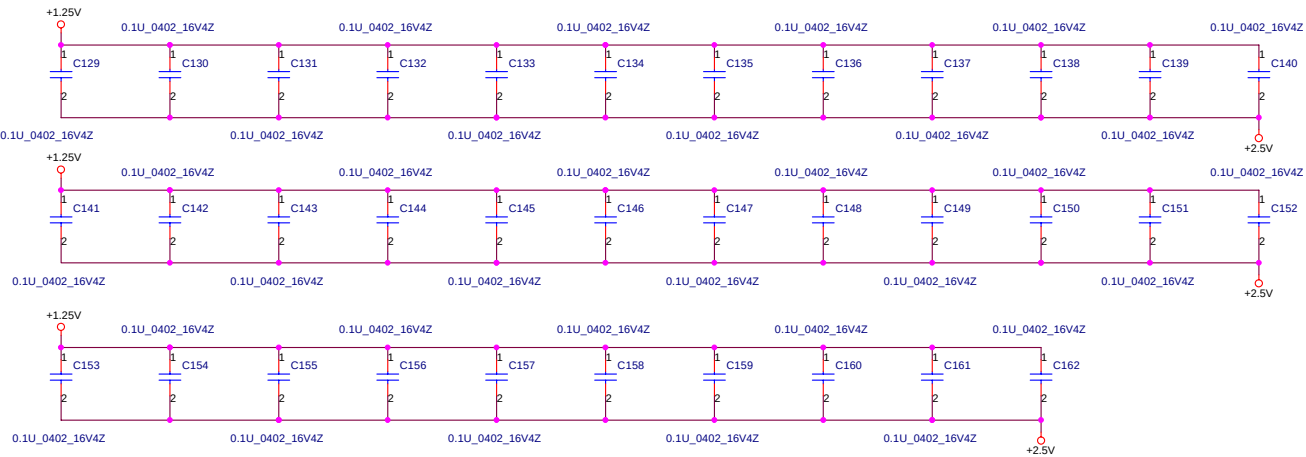
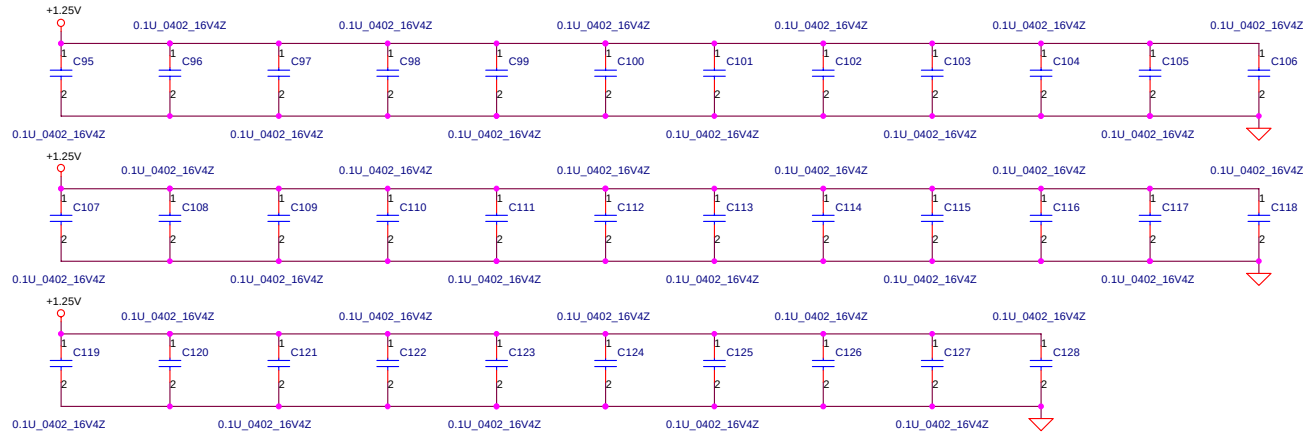
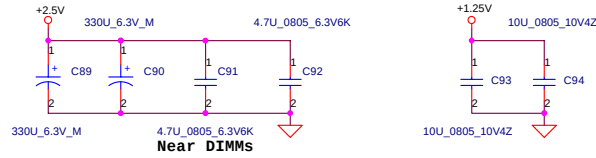
Place these resistors
close to DIMM0,
all trace length<500 mil



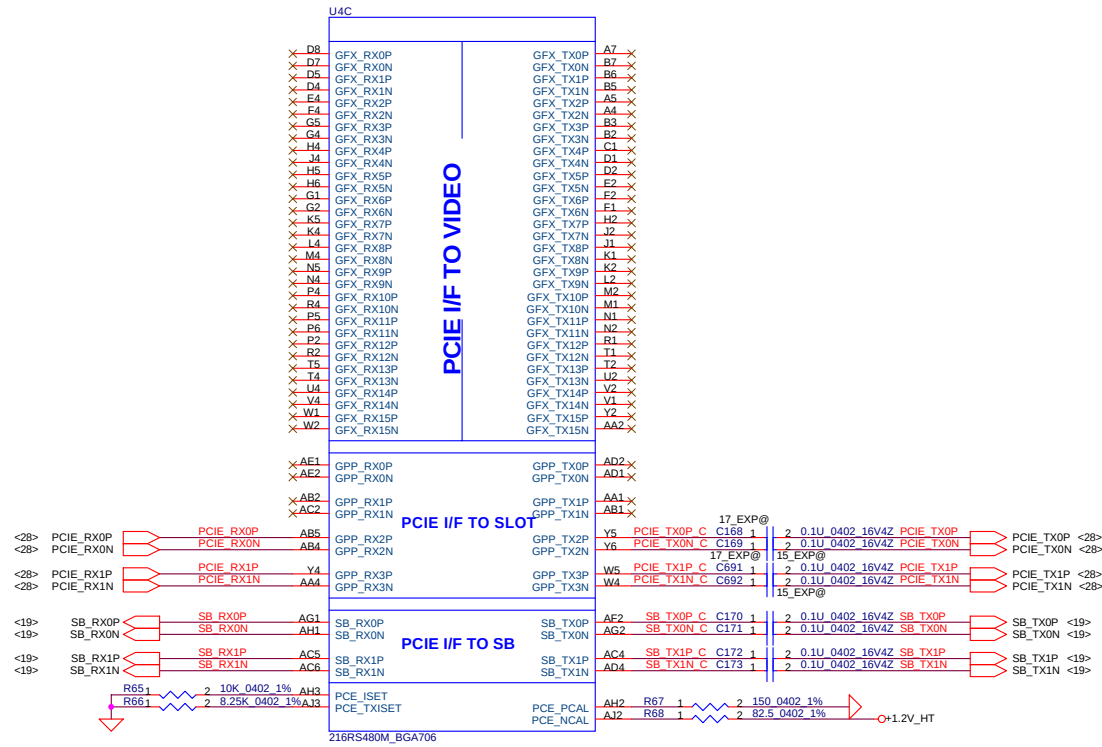
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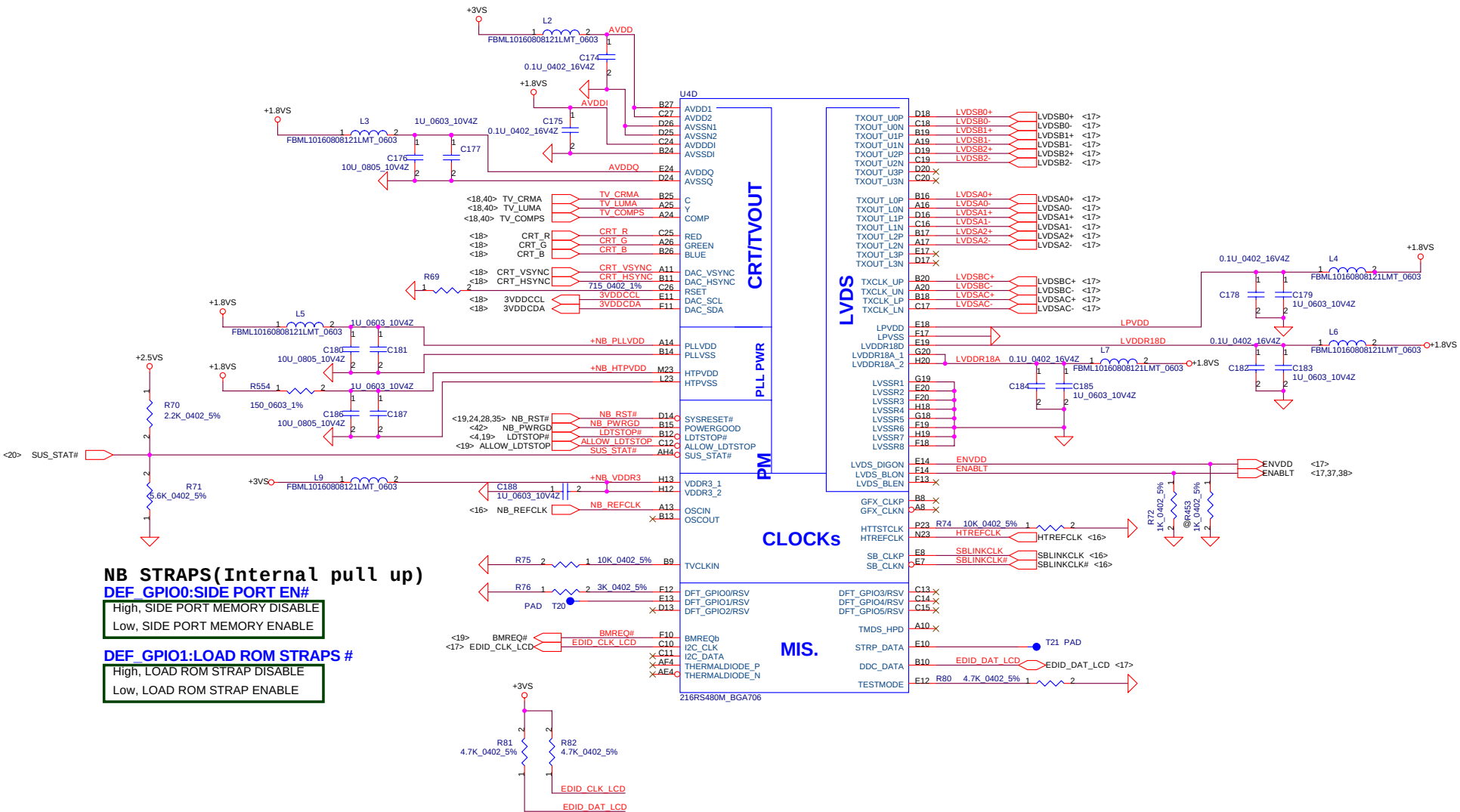
Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25V



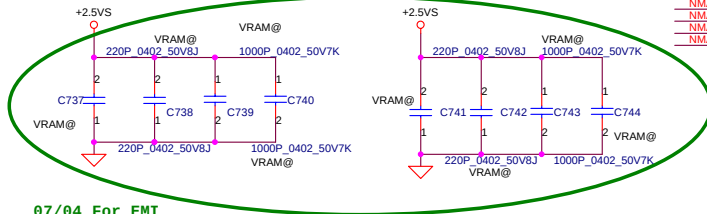
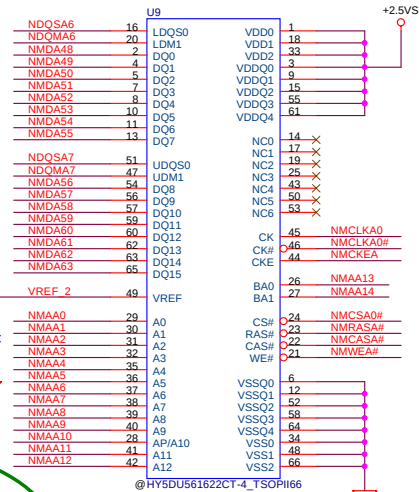
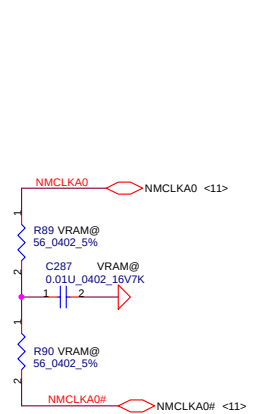
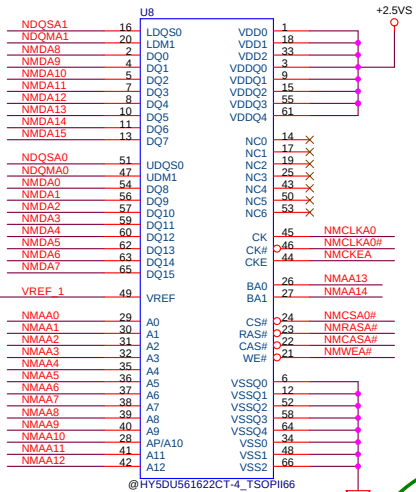
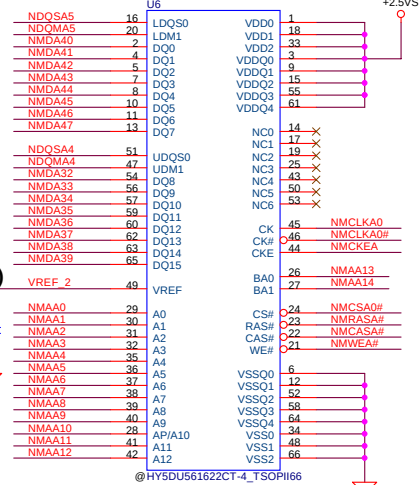
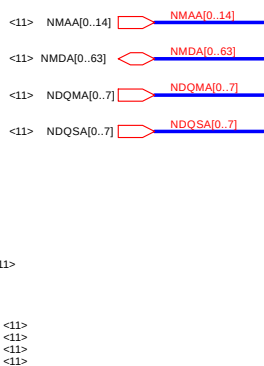
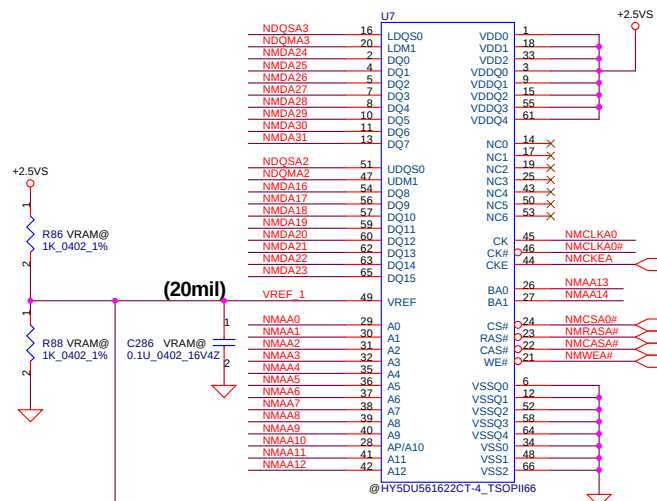
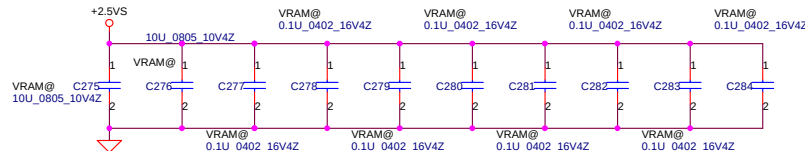
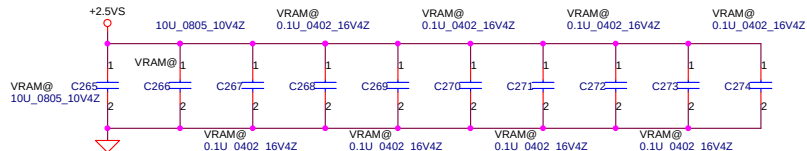
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AVDD , AVDDI , AVDDQ , +NB_PLLVDD , +NB_HTPVDD
+NB_VDDR3 , LPVDD , LVDDR18D , LVDDR18A (20mils)



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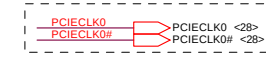
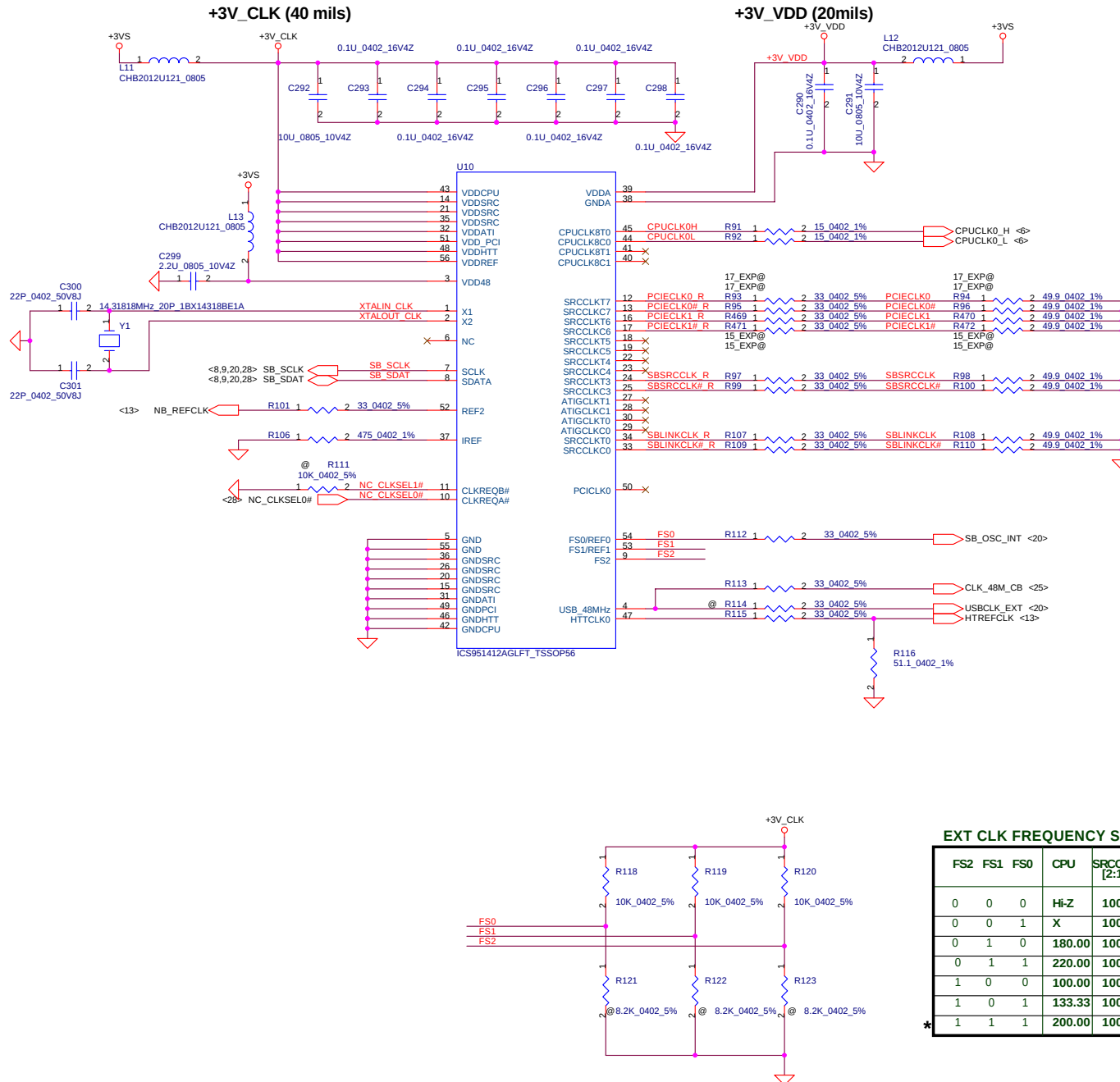


07/04 For EMI

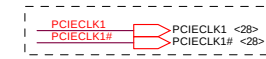
ZZZ
X76 VRAM
SAMSUNG@ SAMSUNG X76 VRAM

ZZZ
X76 VRAM
HYNIX@ HYNIX X76 VRAM

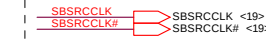
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Express Card(17)



Express Card(15.4)



A link Express

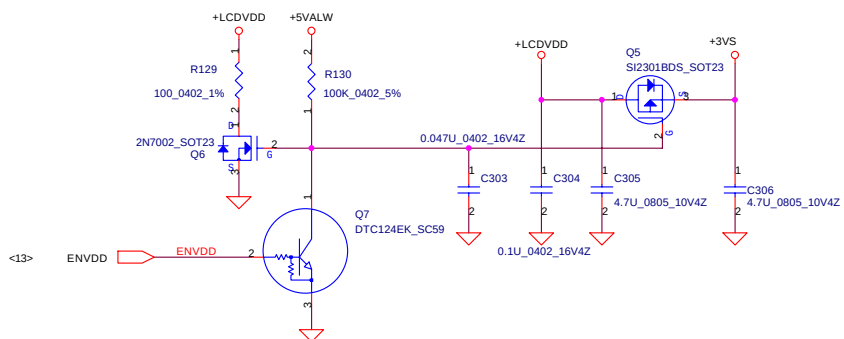
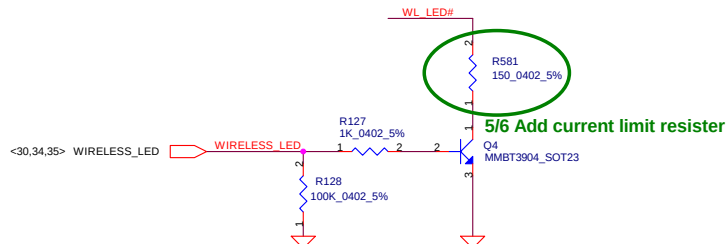
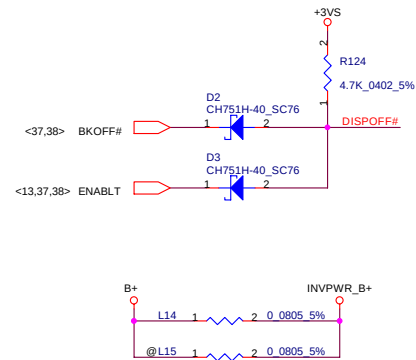
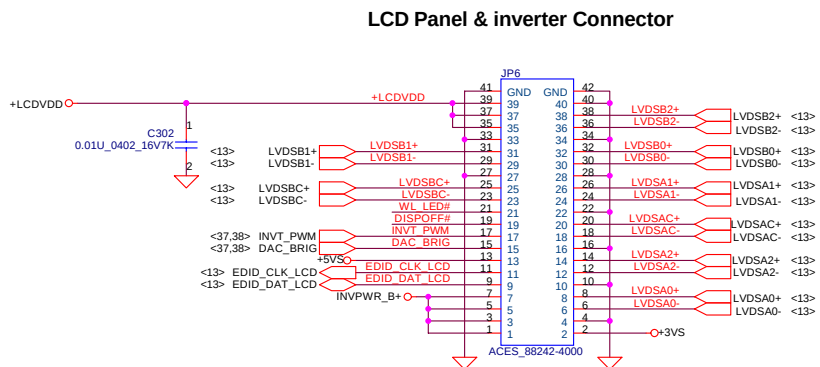


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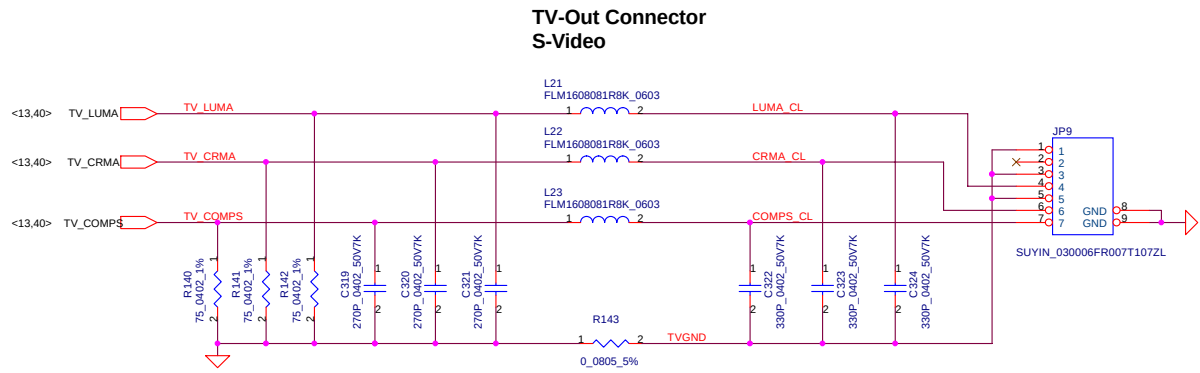
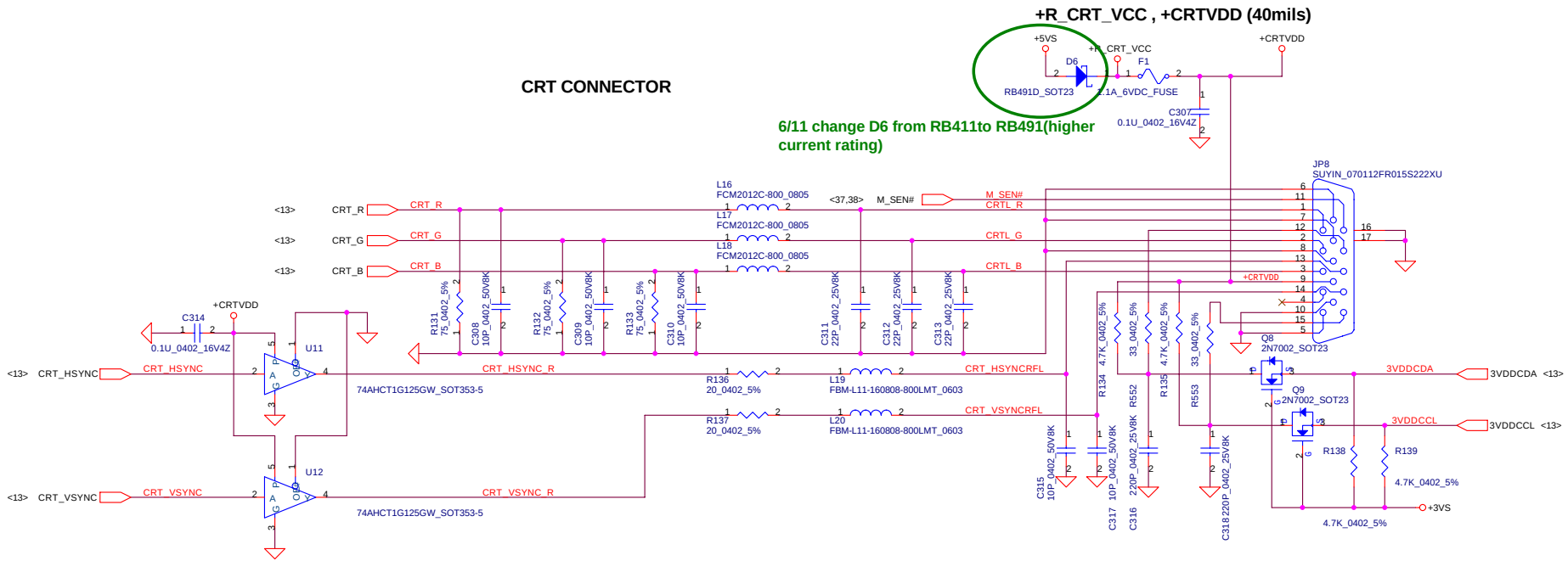
EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation

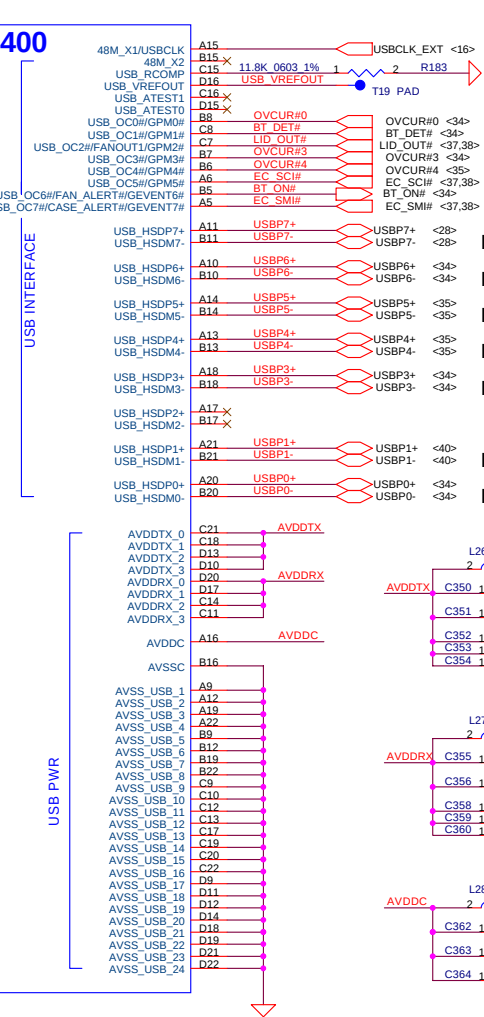
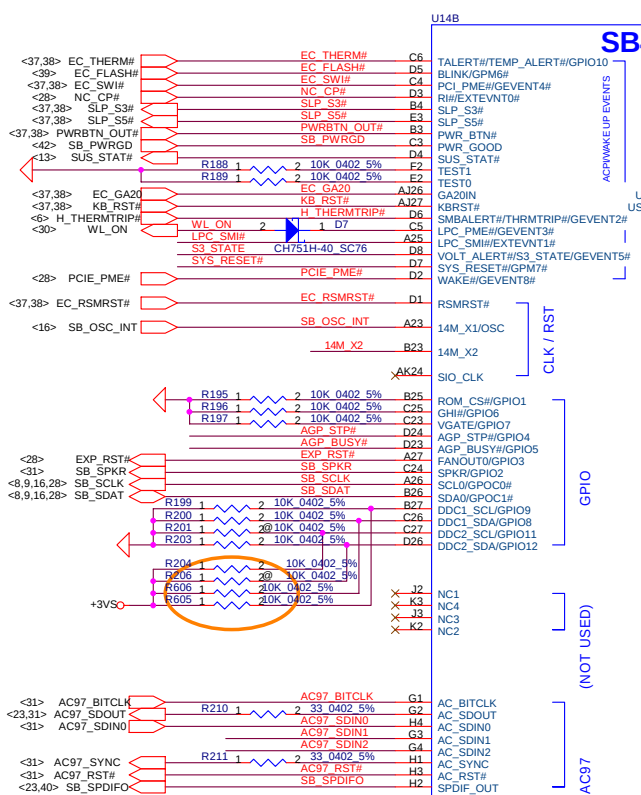
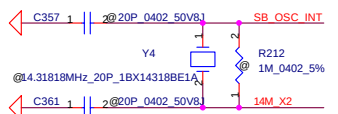
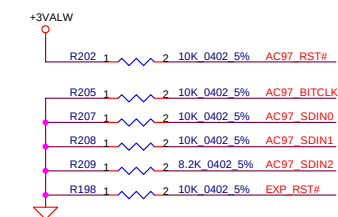
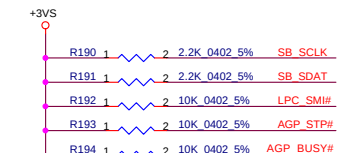
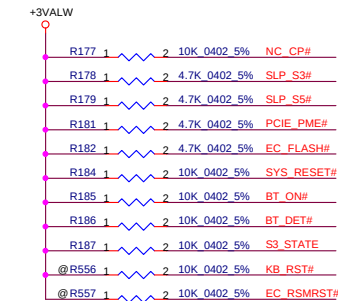
LCD Panel & inverter Connector



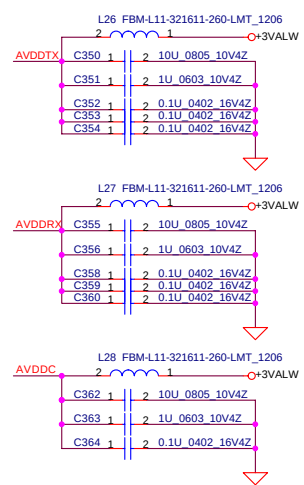
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								Size	Document Number	Rev
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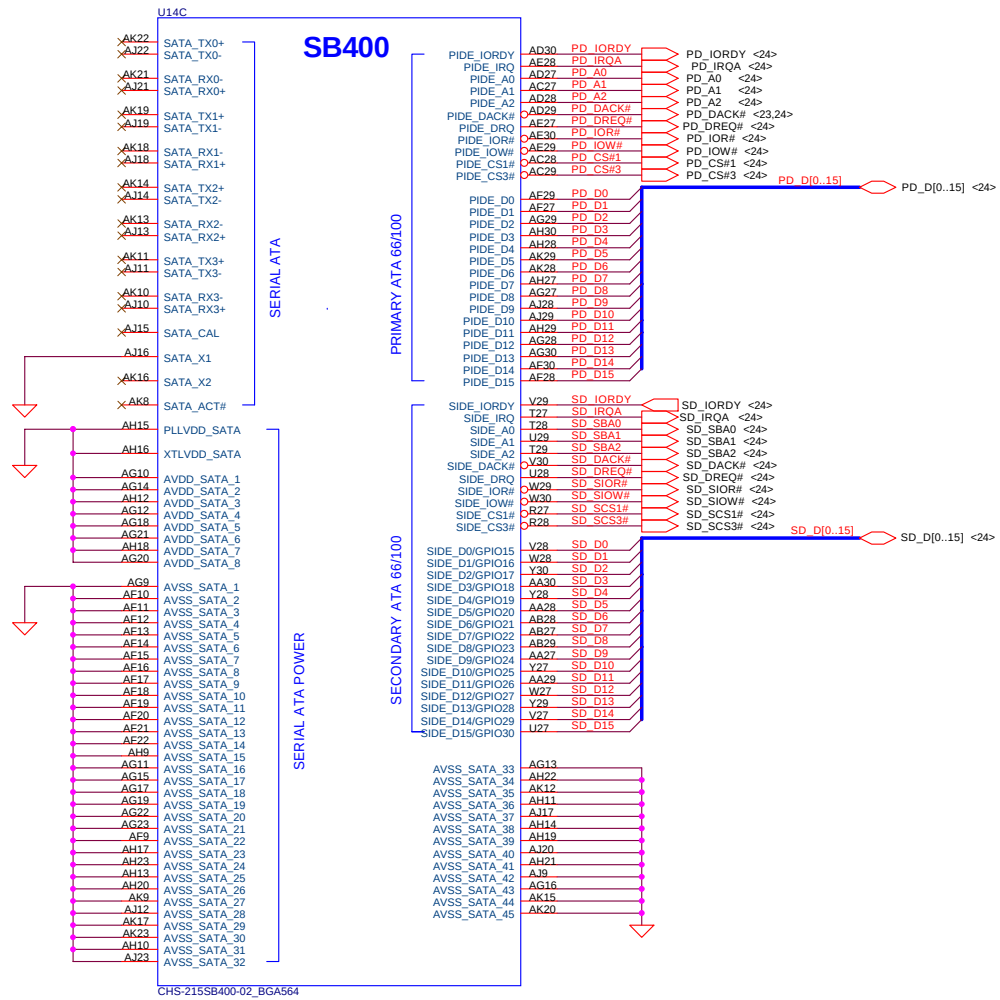


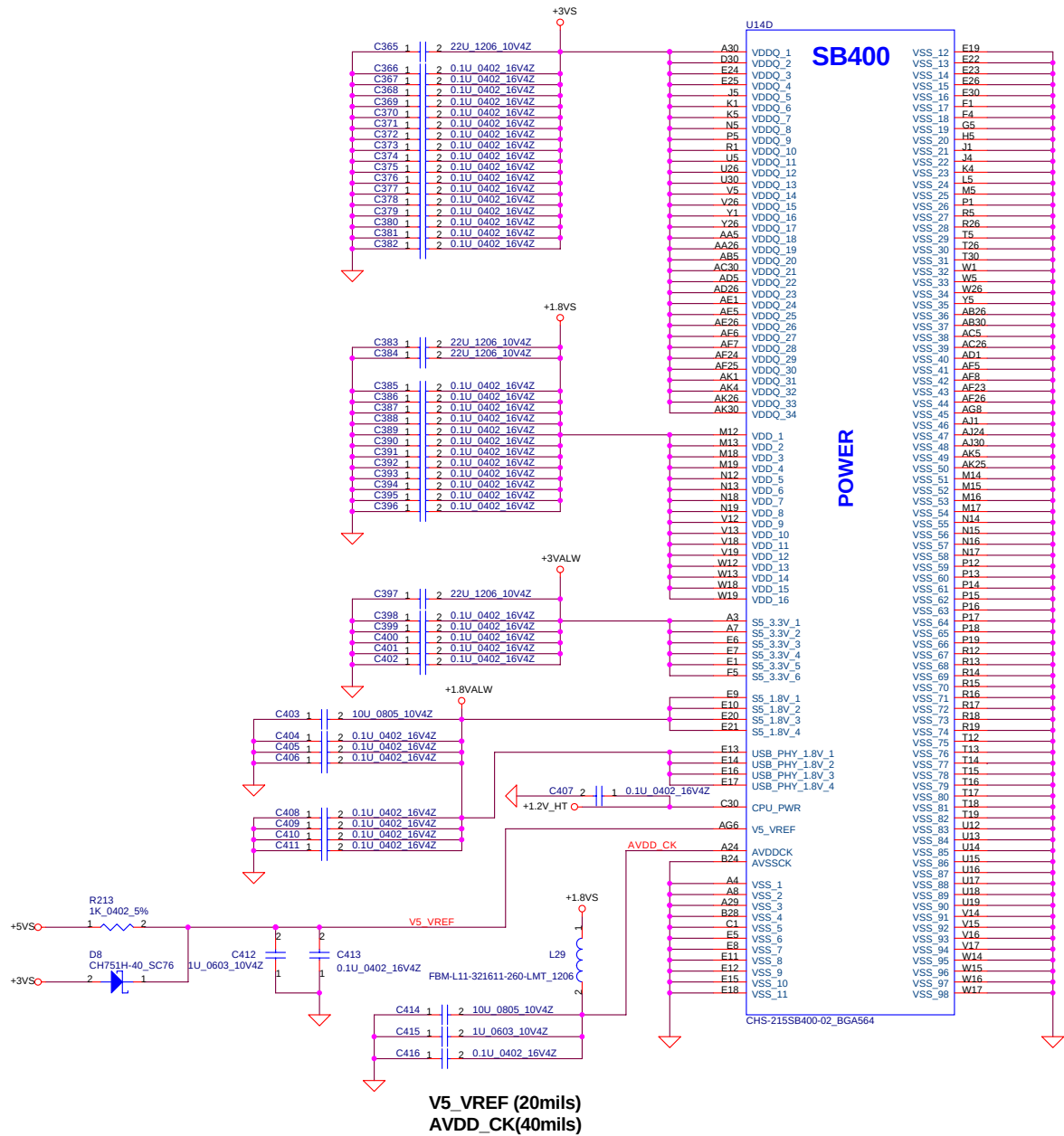
Express Card 15.4
Bluetooth
Right side USB
Right side USB
Left side USB
Docking
Left side USB



	GPI012	GPI011
* HYNIX 128MB	0	1
SAMSUNG 128MB	1	1
No VRAM	0	0
Reserved	1	0

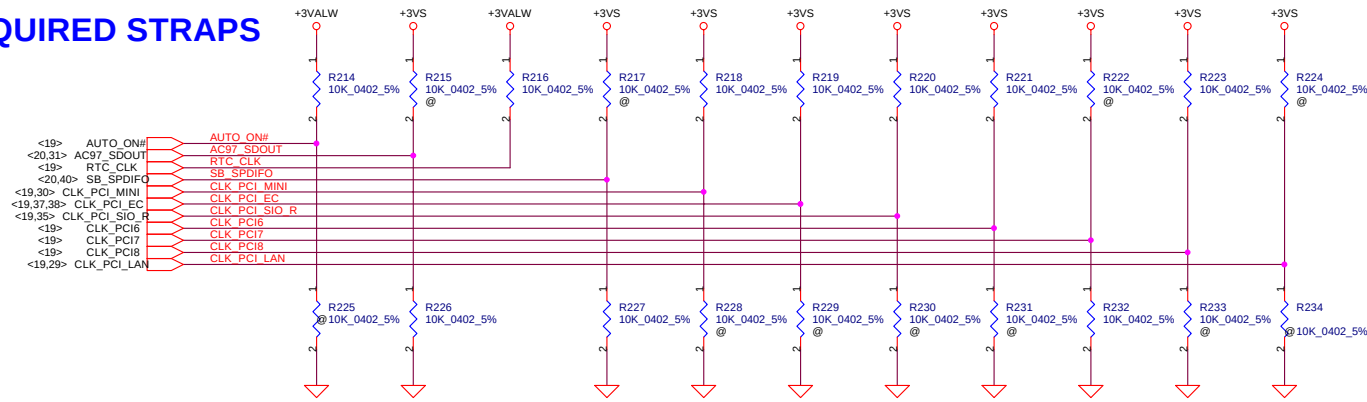
GPI08	0	Original Hynix VRAM
GPI08	1	New Hynix VRAM
GPI08	0	Original Samsung VRAM
GPI08	1	New Samsung VRAM





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				Size	Document Number	401417		Rev B	
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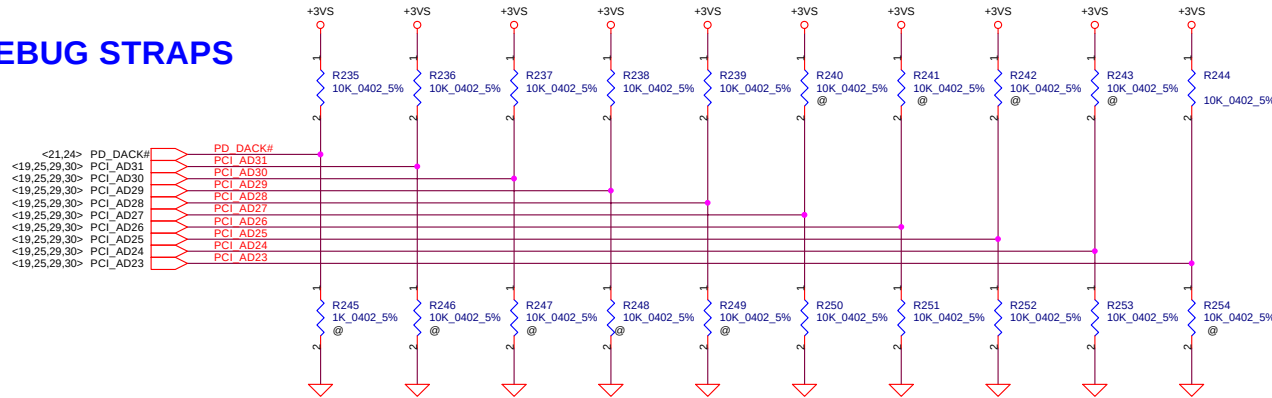
REQUIRED STRAPS



ACPWON

	AUTO_ON#	AC97_SDOOUT	RTC_CLK	SB_SPDIFO	CLK_PCI_LAN	CLK_PCI_MINI	CLK_PCI_EC	CLK_PCI_SIO	CLK_PCI6	CLK_PCI7	CLK_PCI8
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHz OSC MODE	USB PHY PWRDOWN DISABLE DEFAULT	INTERNAL 48MHz DEFAULT	PCIE_CM_SET LOW DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = PMC LPC ROM	
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	48MHz XTAL MODE	USB PHY PWRDOWN ENABLE	EXTERNAL 48MHz	PCIE_CM_SET High	CPU I/F = P4	L,H = NORMAL LPC ROM L,L = FWH ROM DEFAULT	

DEBUG STRAPS



	PD_DACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK DEFAULT	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	RESERVED
PULL LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

The figure consists of two schematic diagrams showing pin connections for an evaluation board.

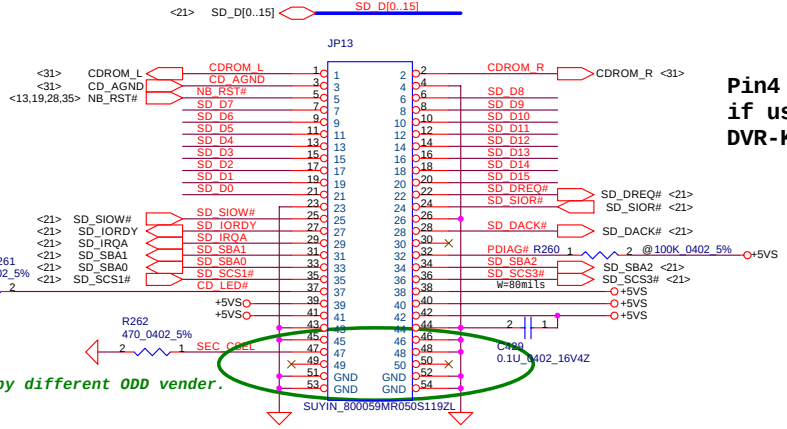
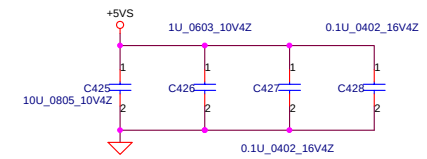
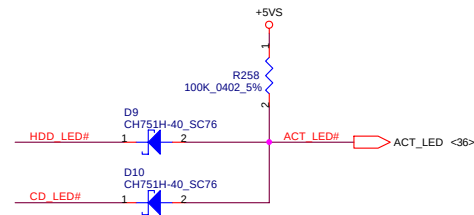
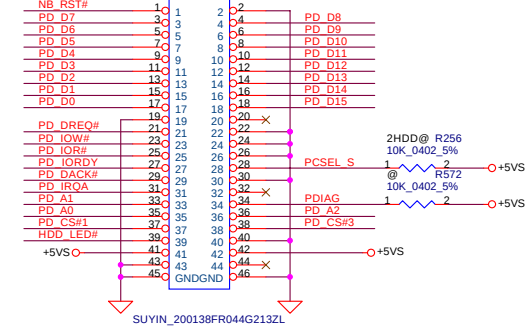
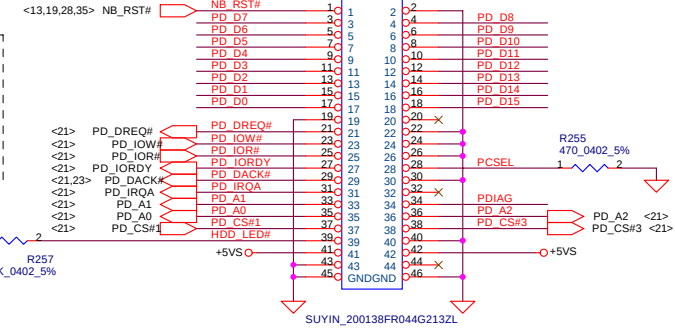
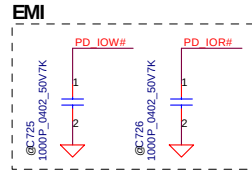
Top Diagram: Power Supply Connections

- +5V5** is connected to pin 1 of a header.
- 2HDD@ 10U_0805_10V4Z** is connected to pin 2 of a header.
- 2HDD@ 0.1U_0402_16V4Z** is connected to pin 1 of a header.
- 100U_C_4VM** is connected to pin 2 of a header.

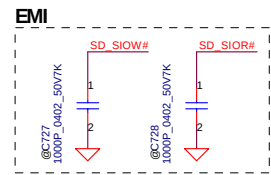
Bottom Diagram: JP12 Header Connections

The JP12 header has 46 pins. The connections are as follows:

- Pin 1:** NB_RST#
- Pin 2:** PD D7
- Pin 3:** PD D6
- Pin 4:** PD D5
- Pin 5:** PD D4
- Pin 6:** PD D3
- Pin 7:** PD D2
- Pin 8:** PD D1
- Pin 9:** PD D0
- Pin 10:** PD DREQ#
- Pin 11:** PD IOW#
- Pin 12:** PD IR#
- Pin 13:** PD IORDY
- Pin 14:** PD DACK#
- Pin 15:** PD IRQA
- Pin 16:** PD A1
- Pin 17:** PD A0
- Pin 18:** PD CS#1
- Pin 19:** HDD_LED#
- Pin 20:** +5V5
- Pin 21:** GNDGND
- Pin 22:** PD D8
- Pin 23:** PD D9
- Pin 24:** PD D10
- Pin 25:** PD D11
- Pin 26:** PD D12
- Pin 27:** PD D13
- Pin 28:** PD D14
- Pin 29:** PD D15
- Pin 30:** PCSEL_S
- Pin 31:** PDIAAG
- Pin 32:** PD A2
- Pin 33:** PD_CS#3
- Pin 34:** +5V5
- Pin 35:** GNDGND
- Pin 36:** +5V5
- Pin 37:** GNDGND
- Pin 38:** +5V5
- Pin 39:** GNDGND
- Pin 40:** +5V5
- Pin 41:** GNDGND
- Pin 42:** +5V5
- Pin 43:** GNDGND
- Pin 44:** +5V5
- Pin 45:** GNDGND
- Pin 46:** +5V5

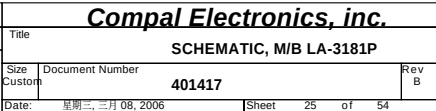


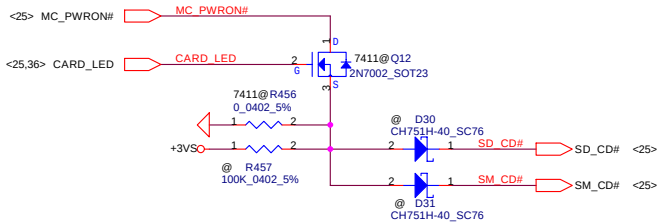
Pin4 of CD_ROM connector is NC
if use Pioneer ODD(DVD Dual
DVR-K12TBC/DVR-K13TBC)



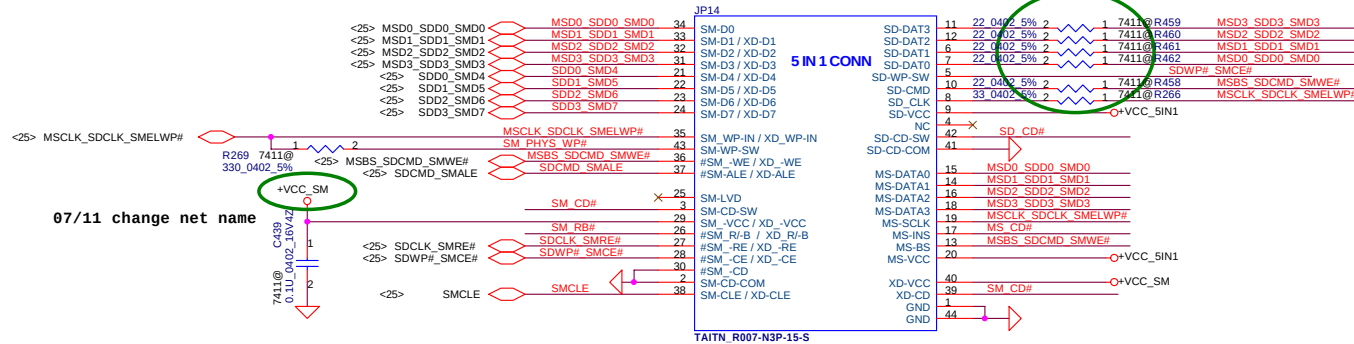
07/11 for defined by different ODD vender.

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				Custody	401417	B
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3		2		1		

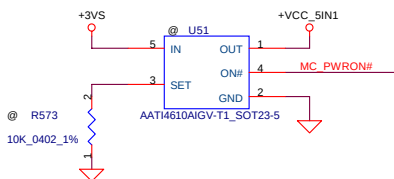




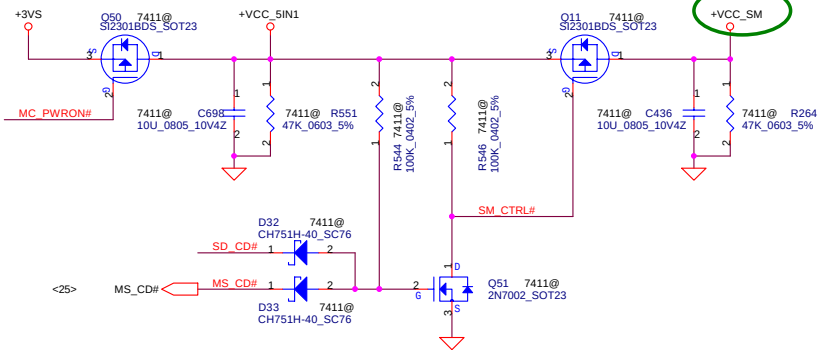
8/23 Relocate Damping resistor to solve Sandisk Card issue



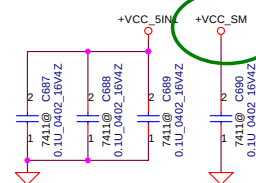
07/11 change net name



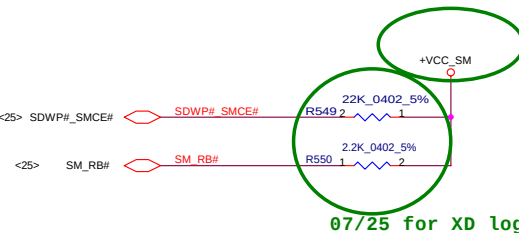
07/11 change net name



07/11 change net name

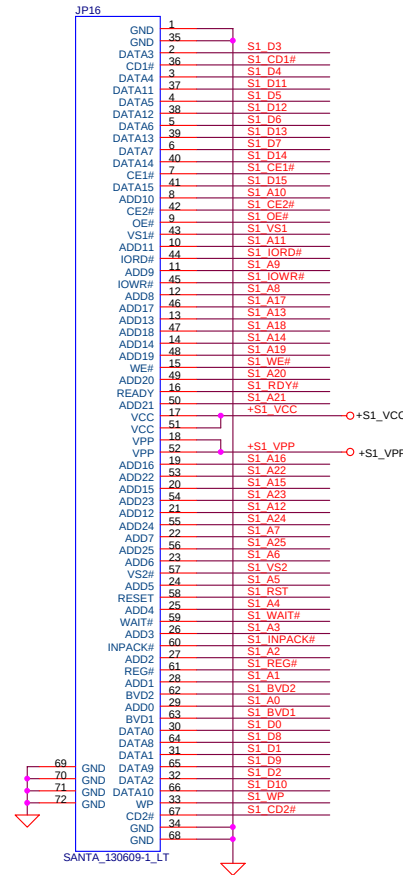
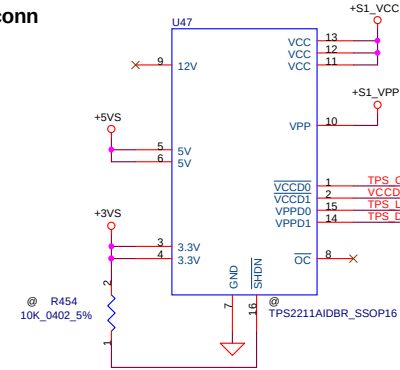
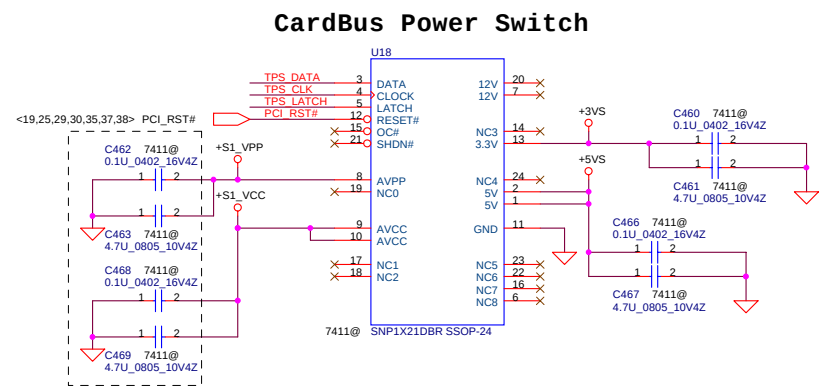


07/11 change net name



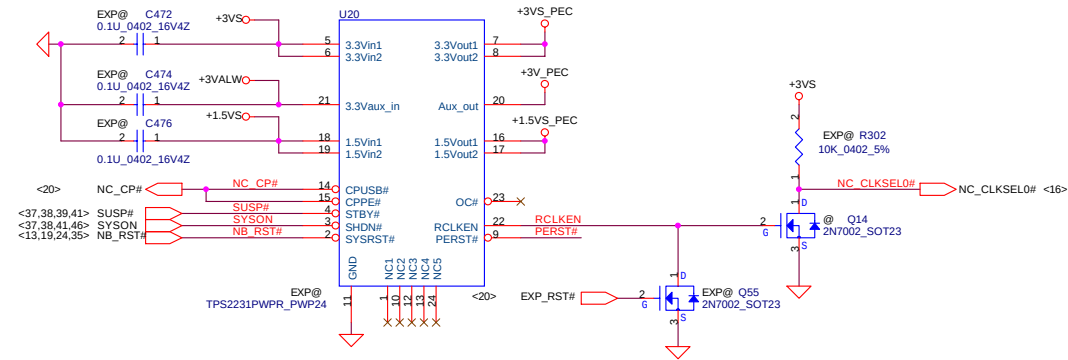
07/25 for XD log

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Custom		Document Number		401417		Rev B
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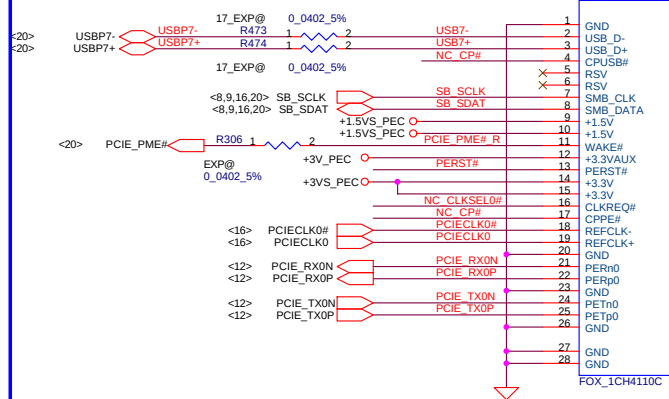


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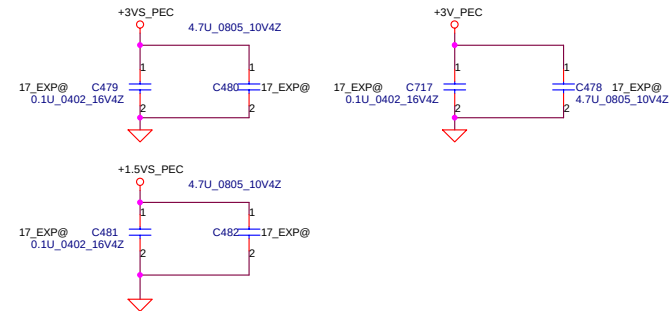
Express Card Power Switch



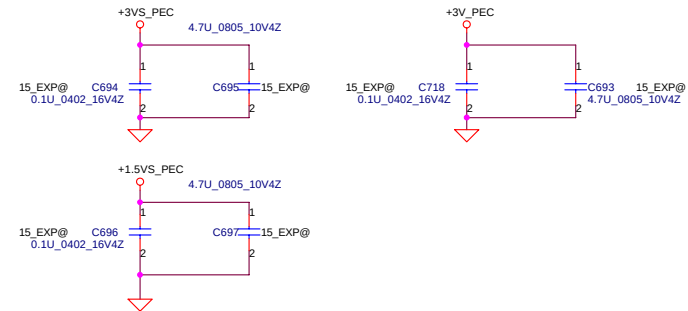
close to JP36



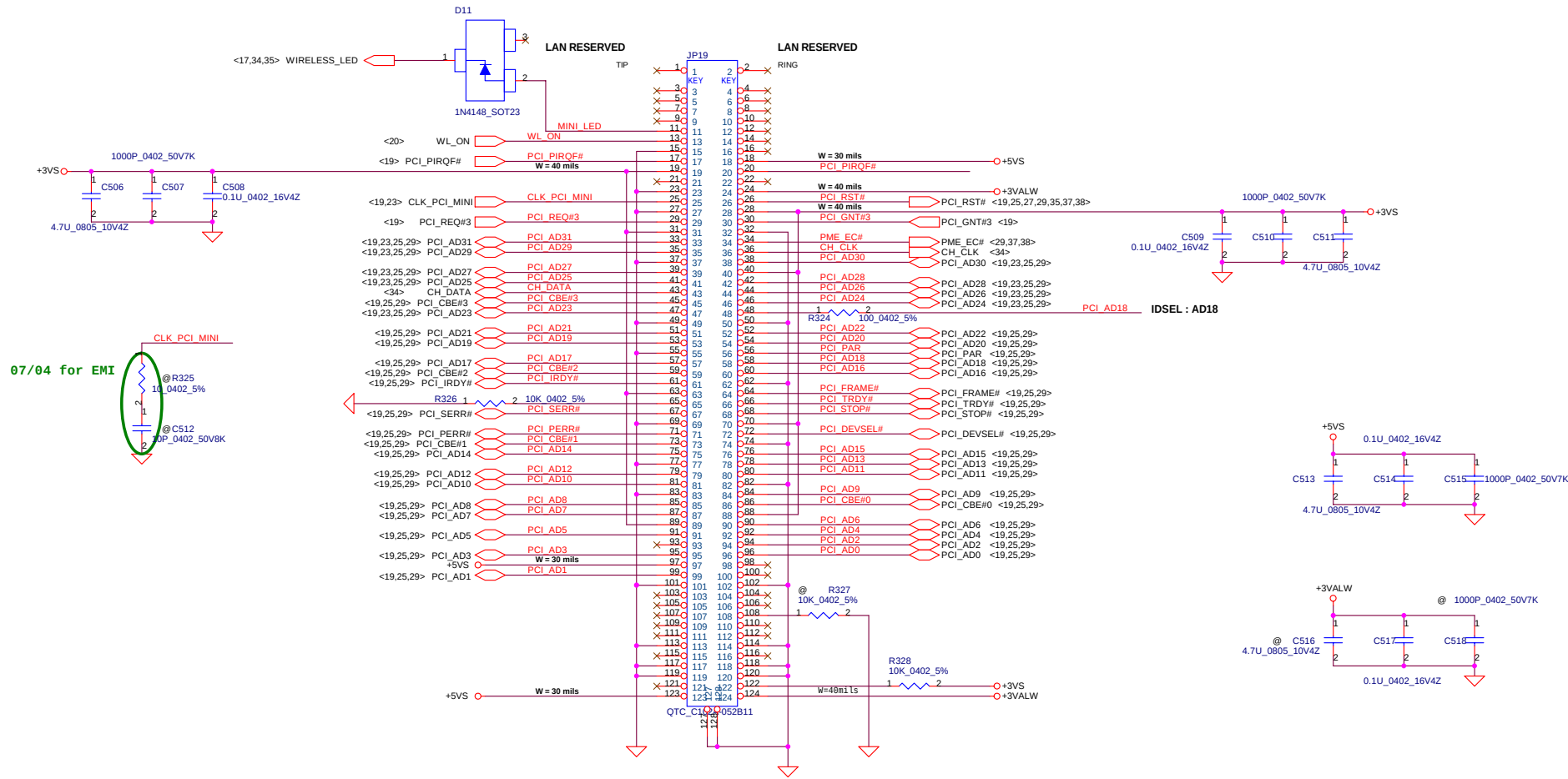
Near to Express Card slot. 17



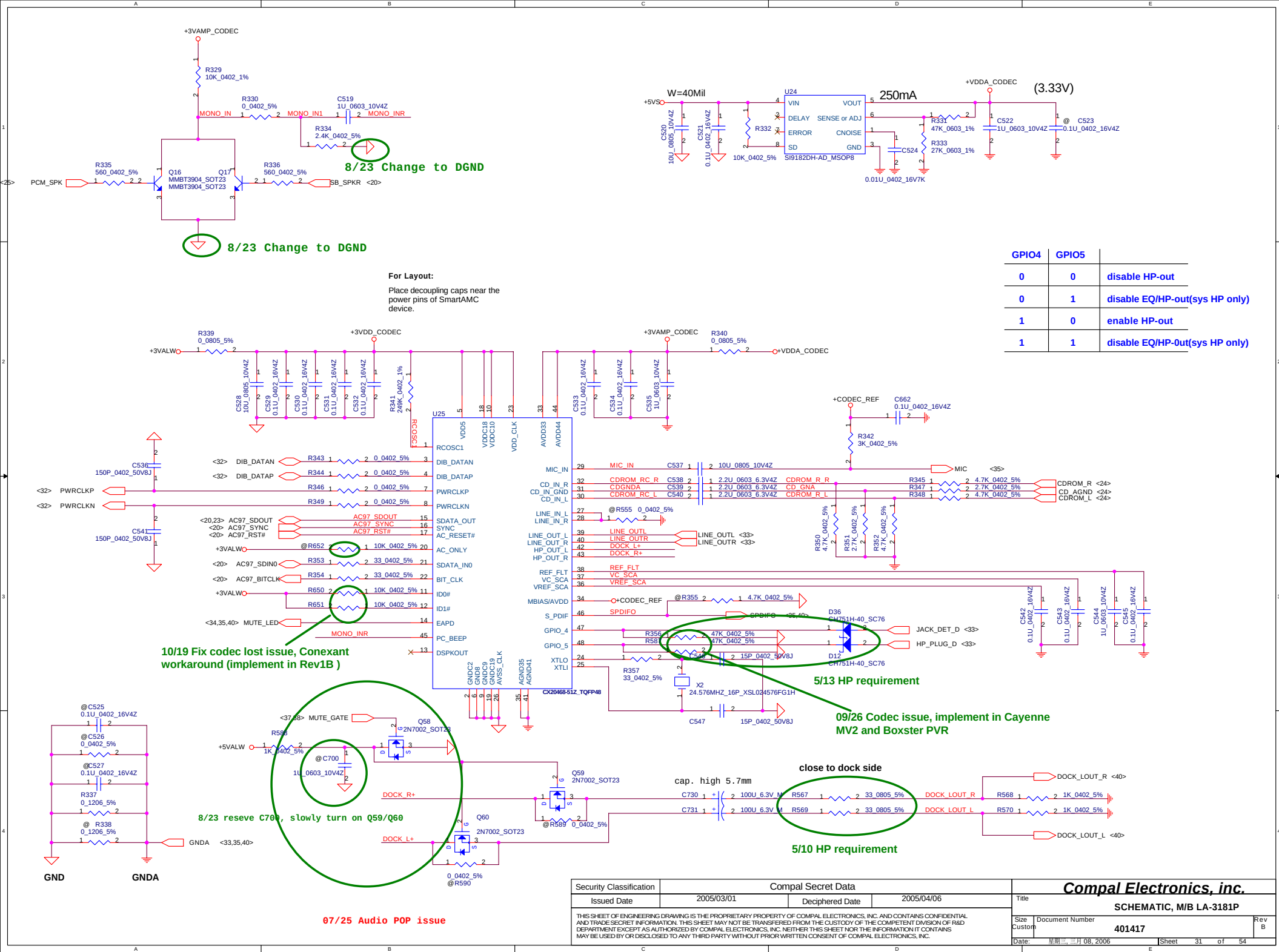
Near to Express Card slot. 15.4



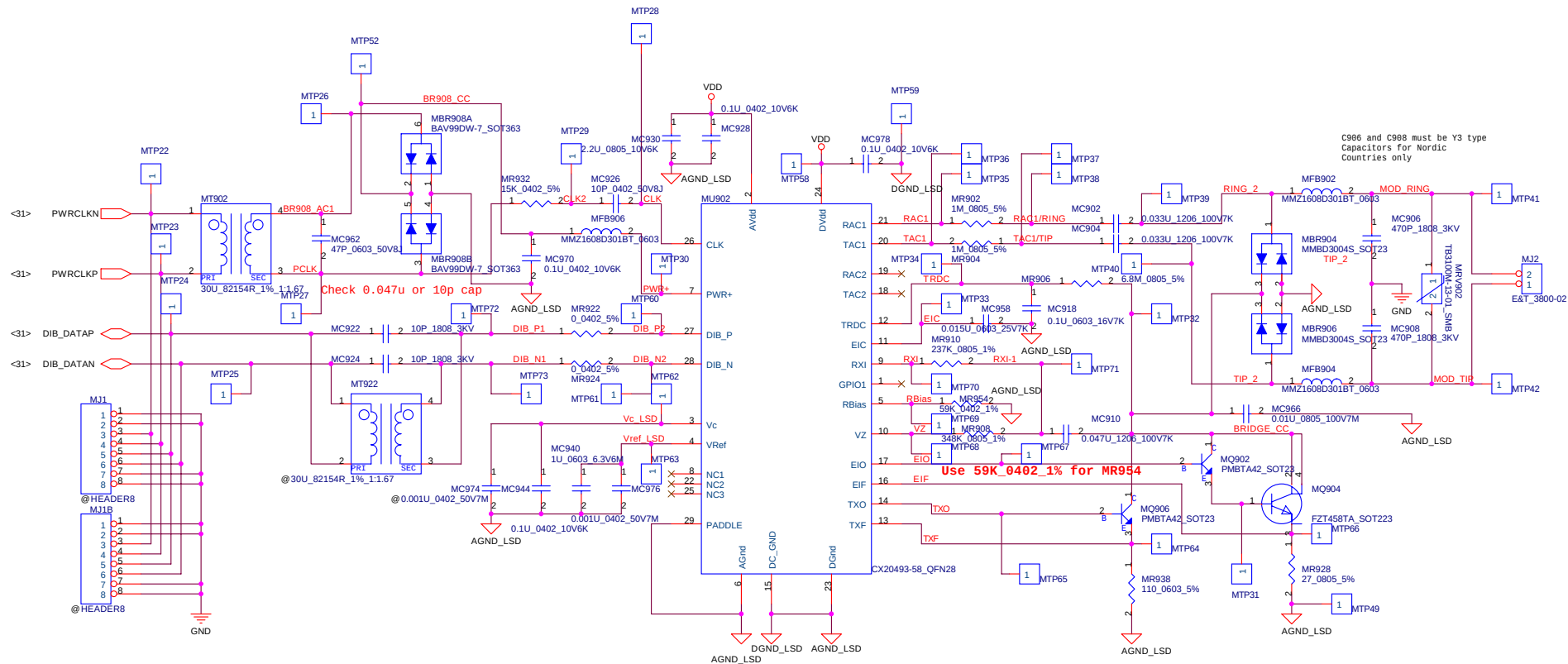
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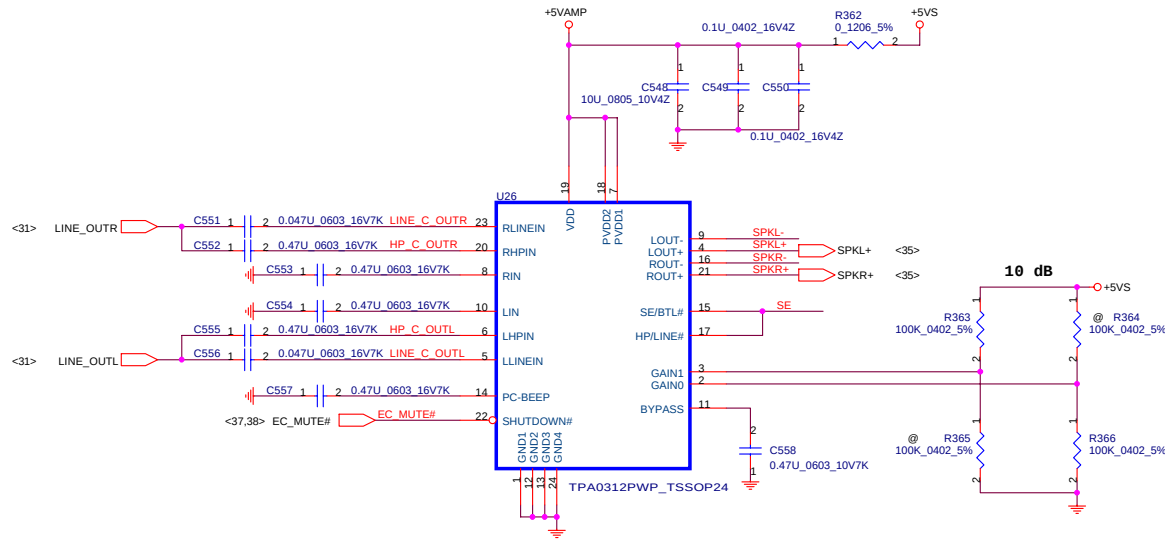
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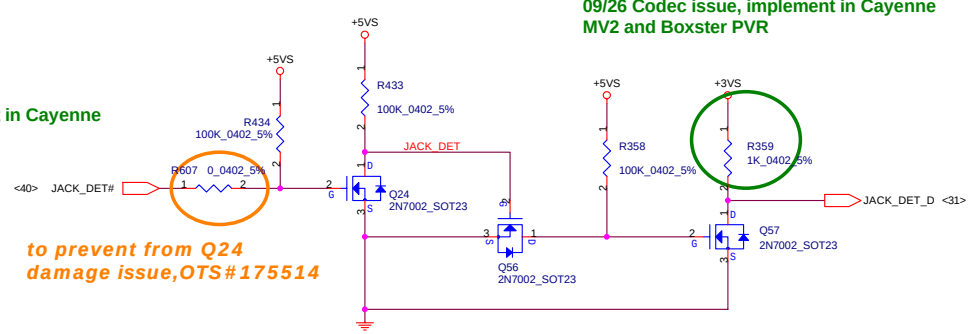
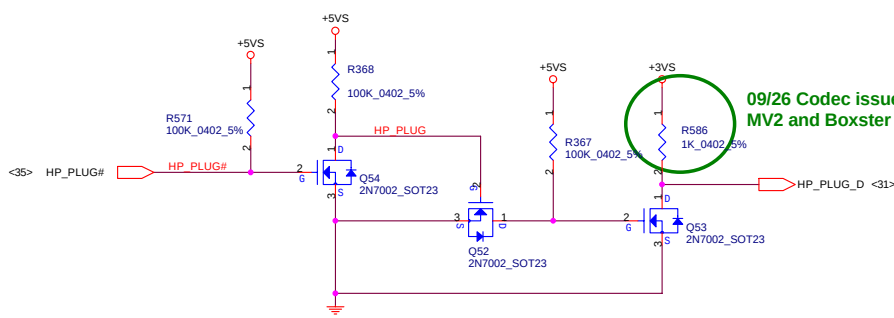
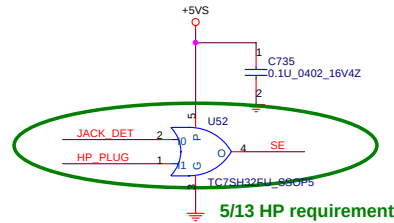
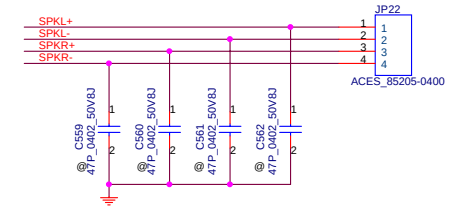
GPIO4	GPIO5	
0	0	disable HP-out
0	1	disable EQ/HP-out(sys HP only)
1	0	enable HP-out
1	1	disable EQ/HP-Out(sys HP only)



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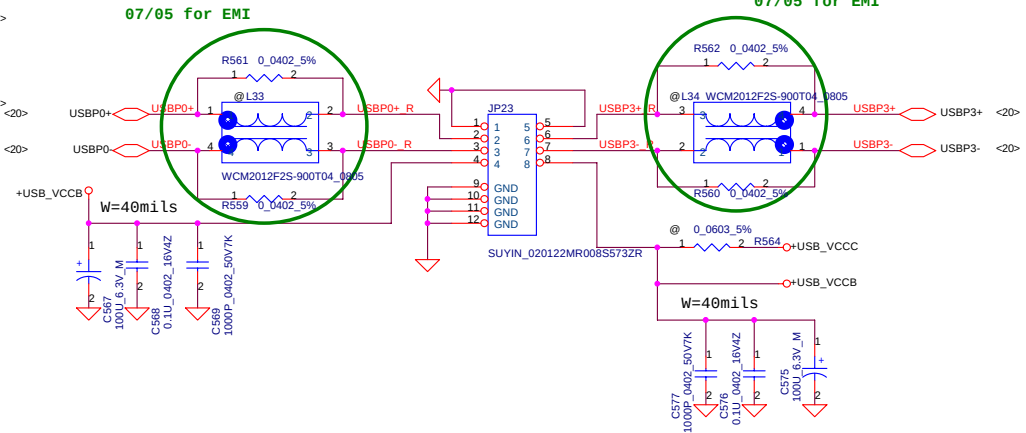
HEADPHONE OUT/LINE OUT			
Gain Settings			
GAIN0	GAIN1	SE/BTL#	Av(inv)
0	0	0	6 dB
0	1	0	* 10 dB
1	0	0	15.6 dB
1	1	0	21.6 dB
X	X	1	4.1 dB



USB CONNECTOR 0/3 (Left side)

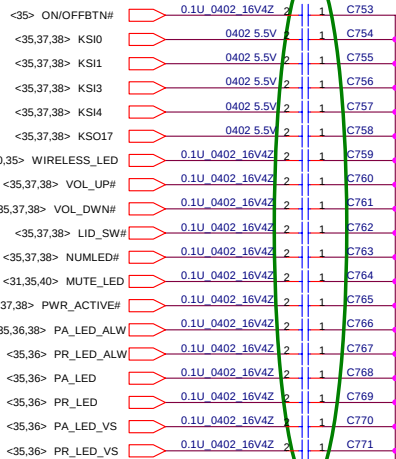
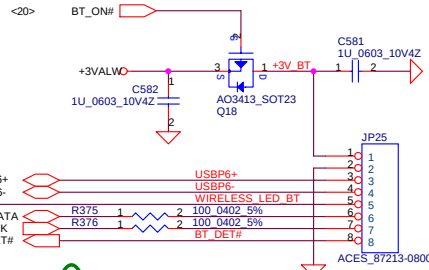
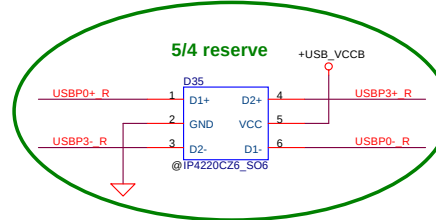
07/05 for EMI

07/05 for EMI



BT CONNECTOR

5/4 reserve



Add Varistor on C756, C757, C758 and Add Caps on C760, C761, C762, C763, C765 (9/5 Cayenne MV) for EMI requirement

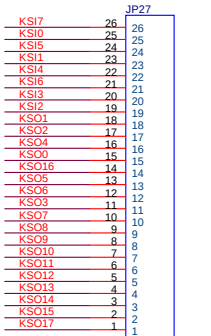
9/26 Add all components for Cayenne MV2 and Boxster PVR

2005.08.11 for EMI solution

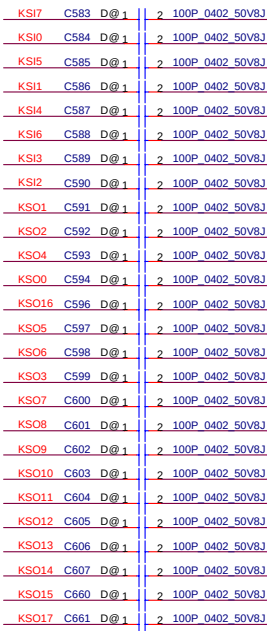
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INT_KBD CONN.(TYPE "D" KB)

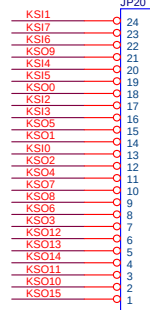
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KSO[0..17] <34,37,38>



ACES_85201-2605

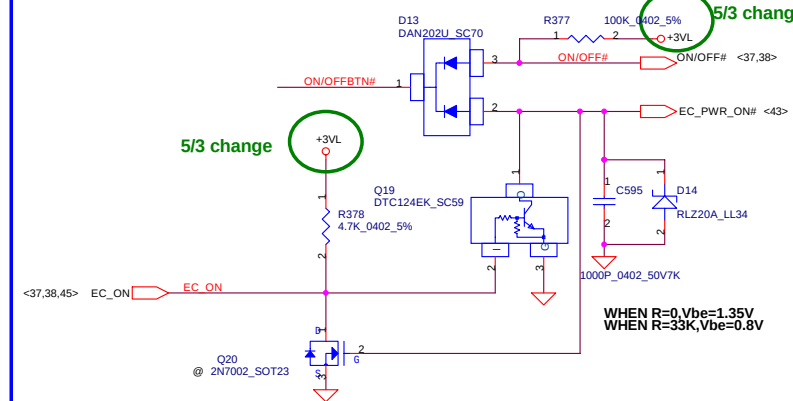


15.4 (TYPE "C" KB)

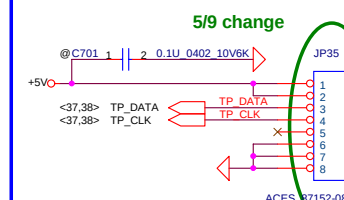


ACES_85201-2405

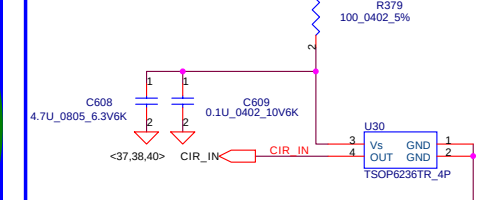
Power BTN



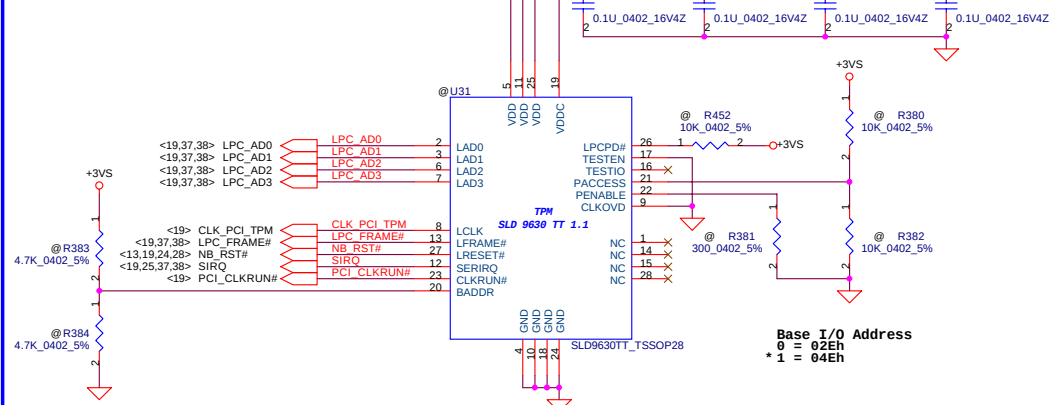
TP to MB CONN



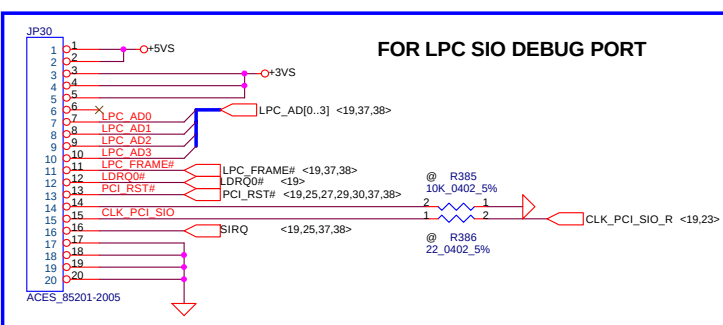
Consumer IR



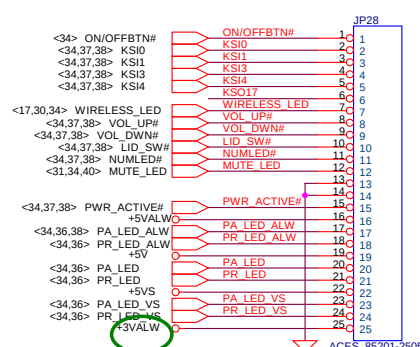
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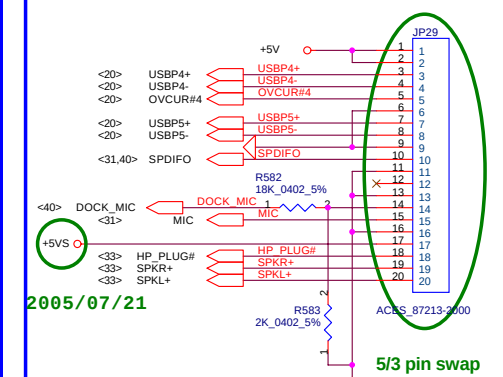
FOR LPC SIO DEBUG PORT



Switch board conn



Audio board conn

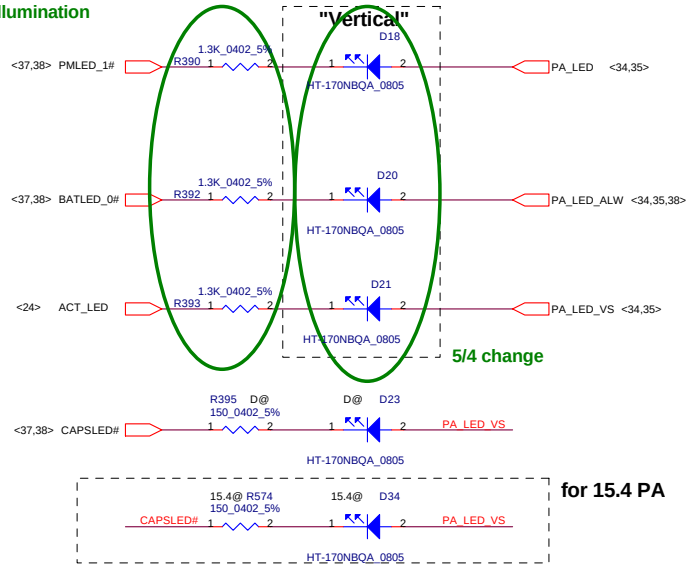


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9/1 change, For
Boxster PV LED
illumination

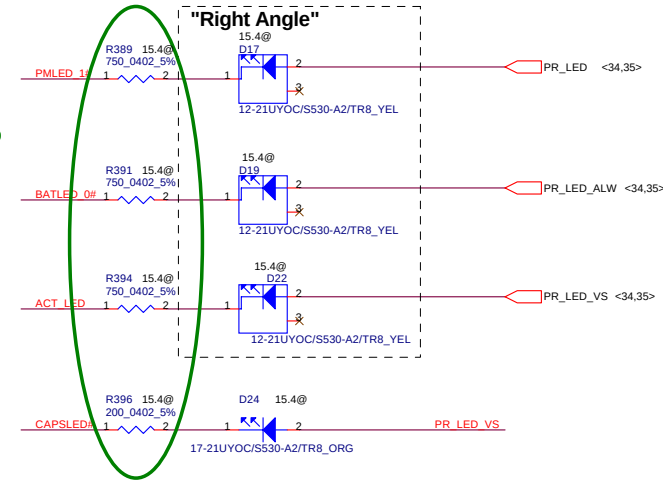
For PA

FOR POWER BUTTON BACKLIGHT SYSTEM POWER

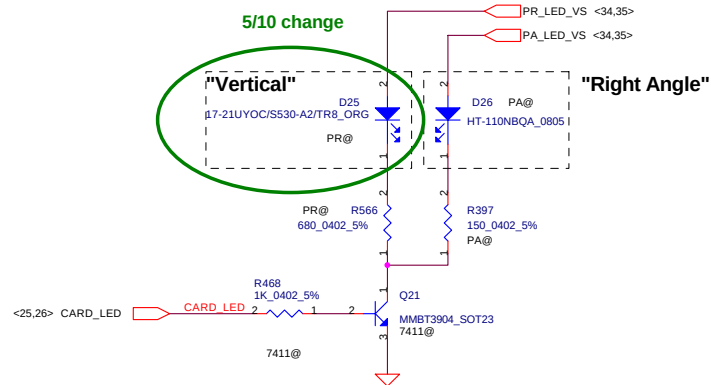


For PR

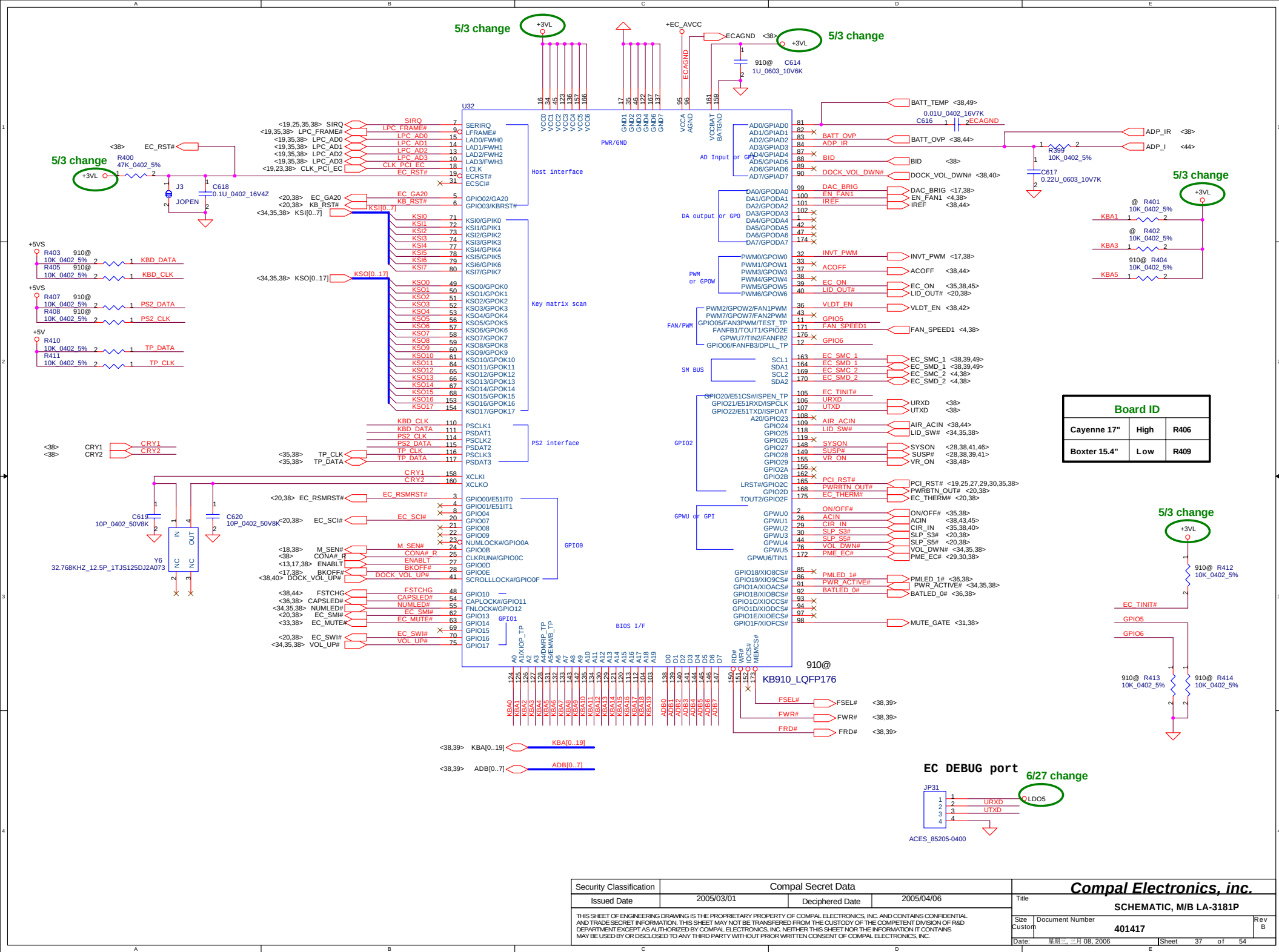
FOR POWER BUTTON BACKLIGHT SYSTEM POWER

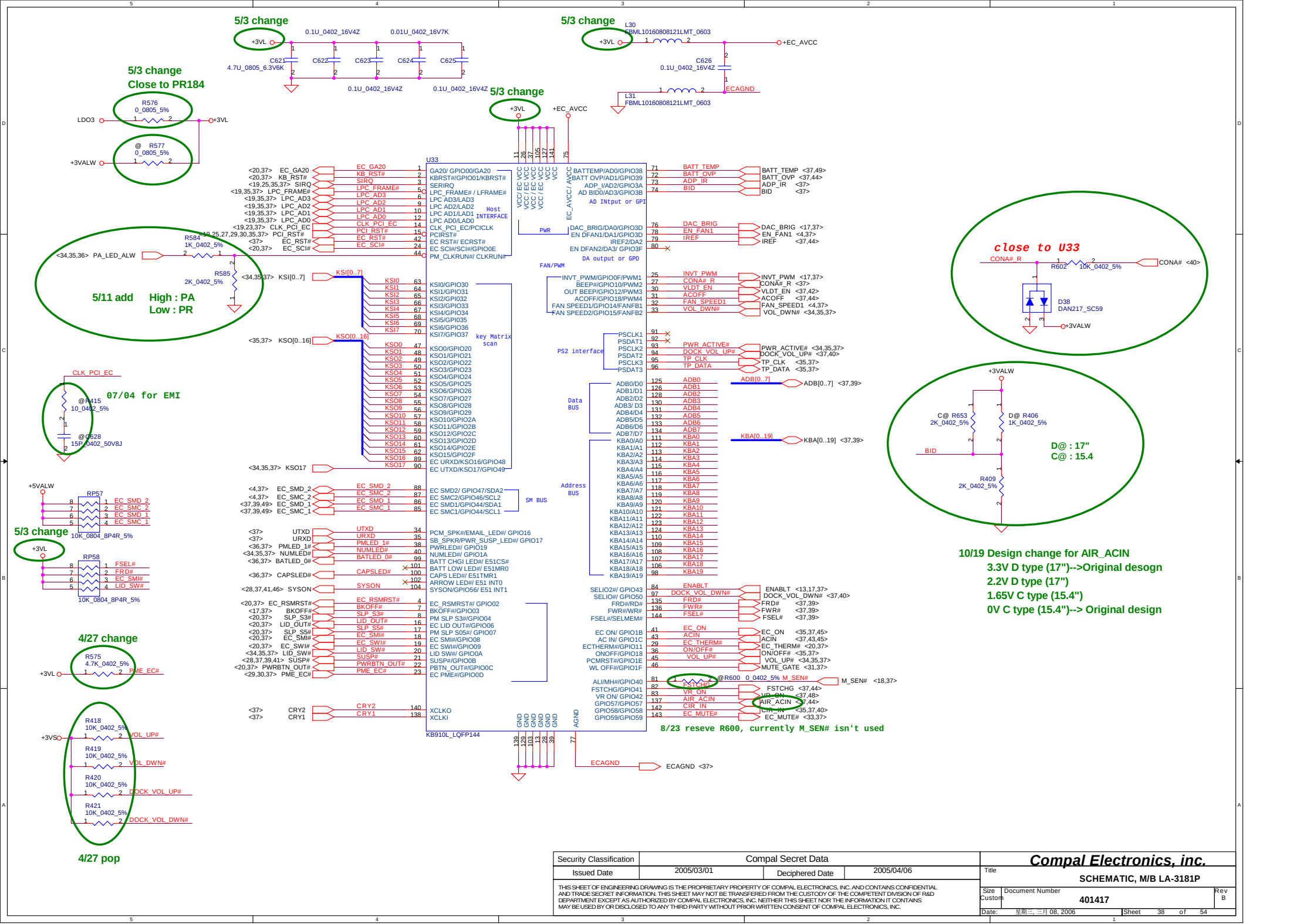


5/10 change

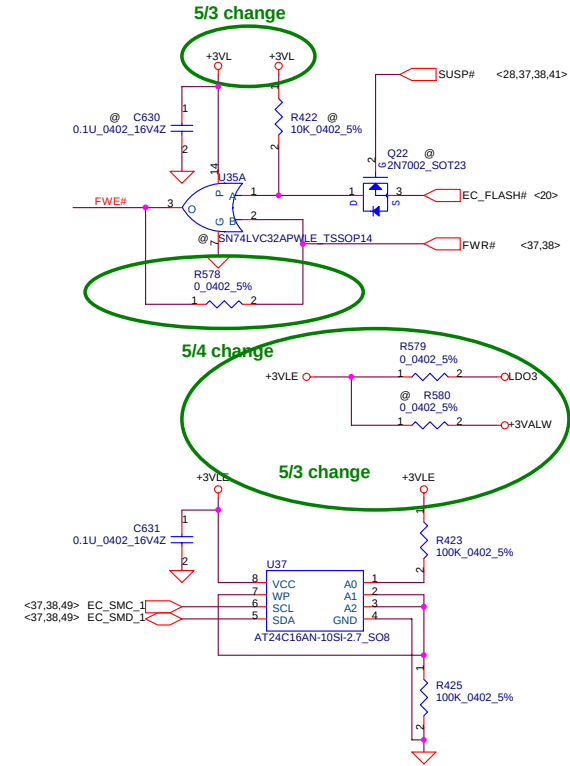
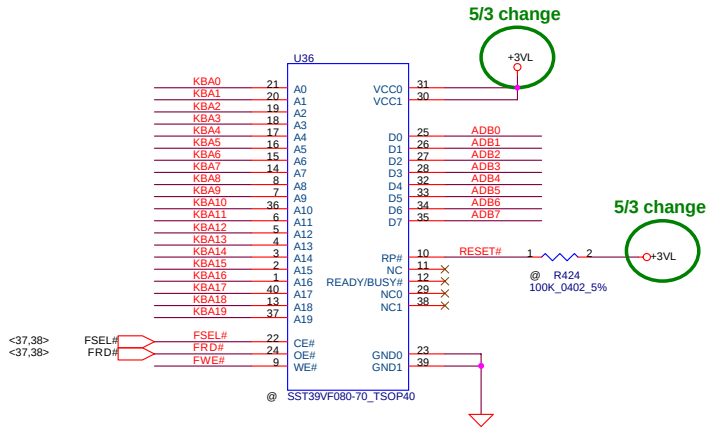
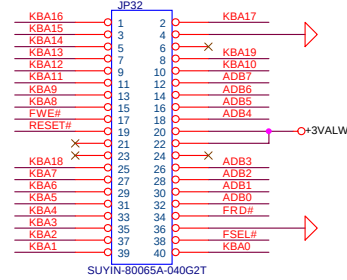
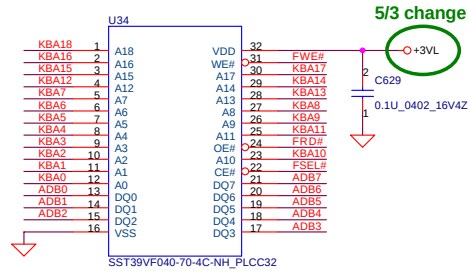


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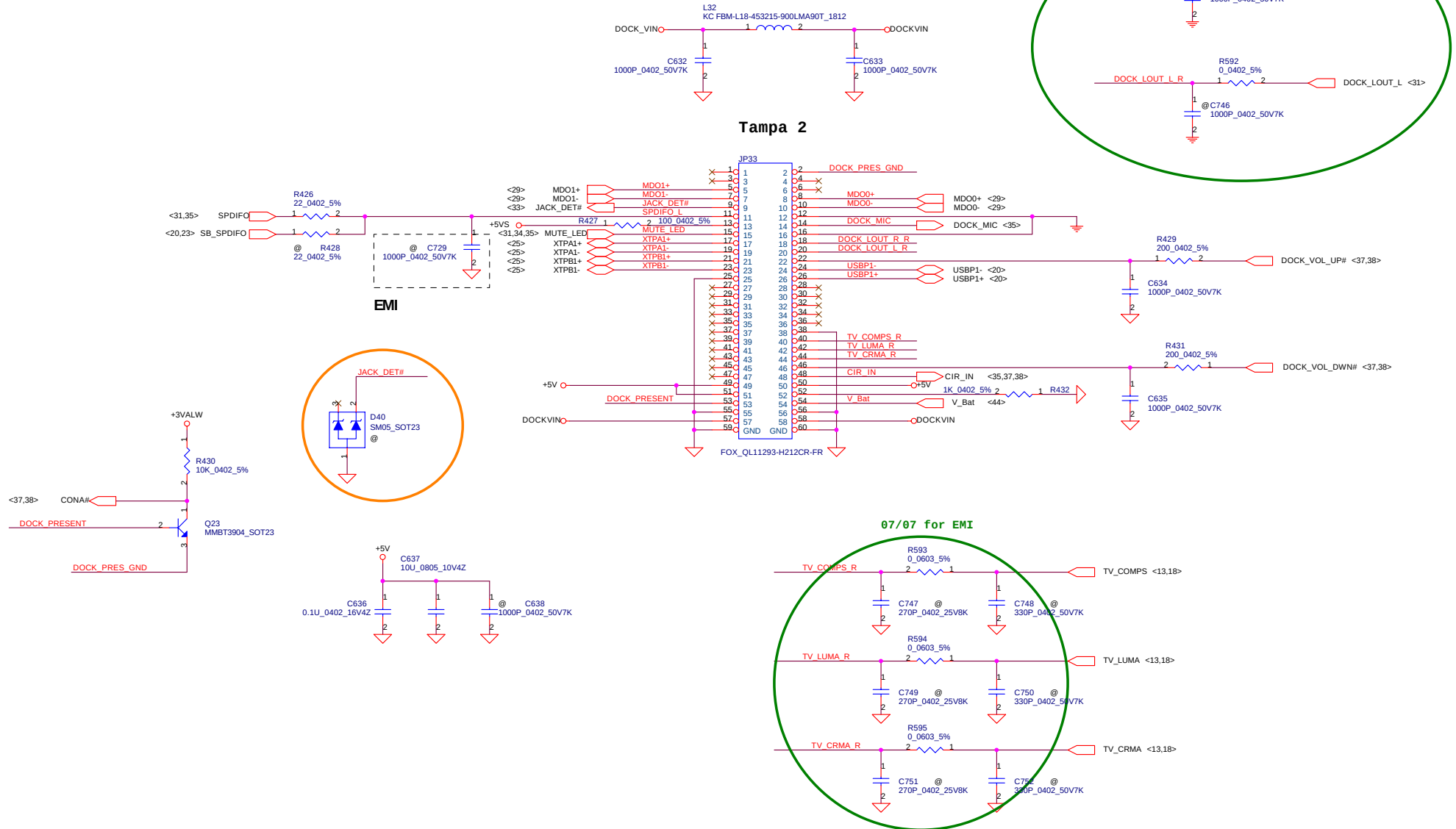


<37,38> ADB[0..7]  ADB[0..7]
<37,38> KBA[0..19]  KBA[0..19]

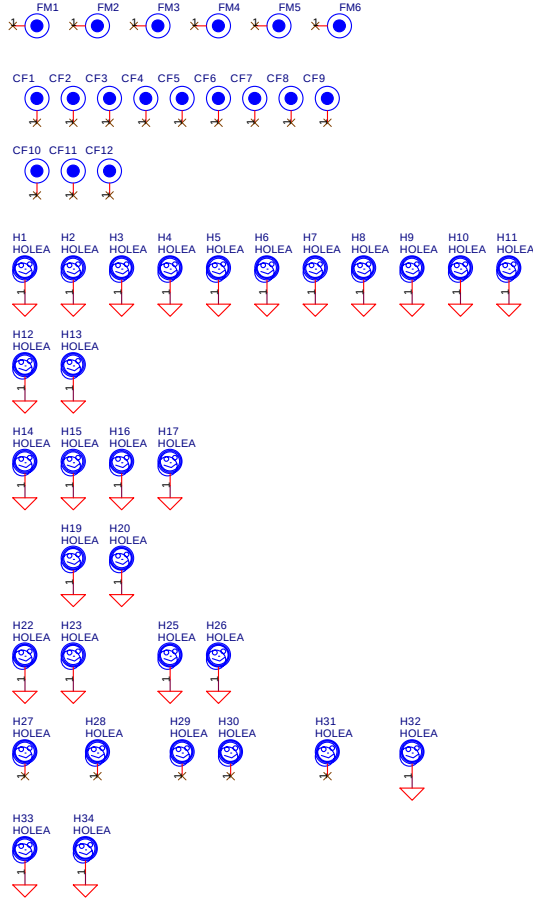
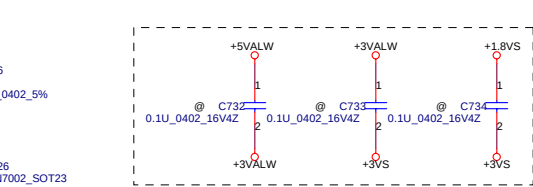
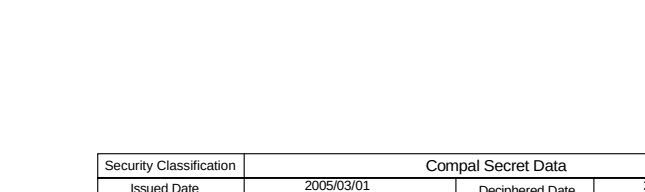
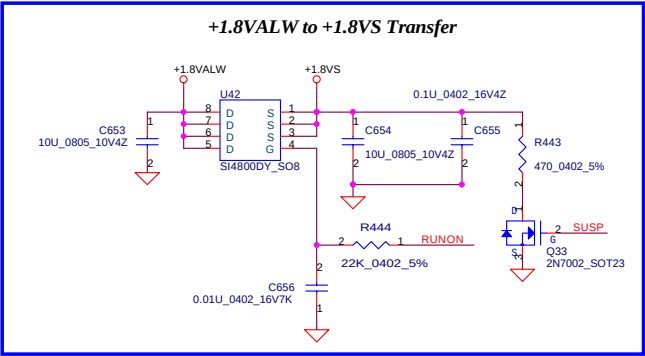
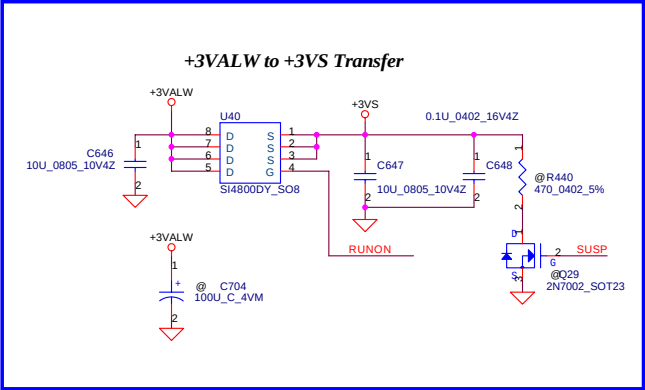
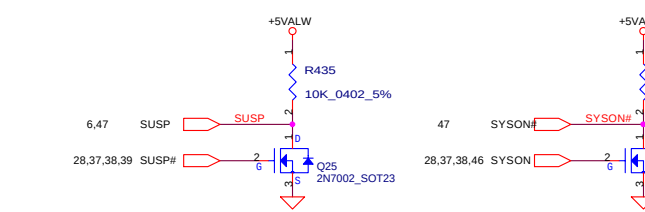
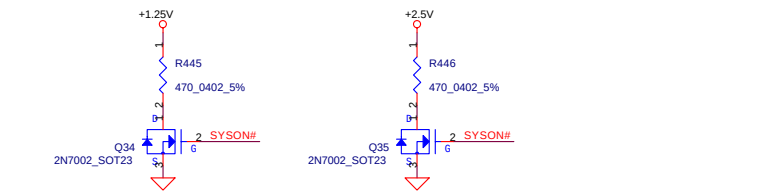
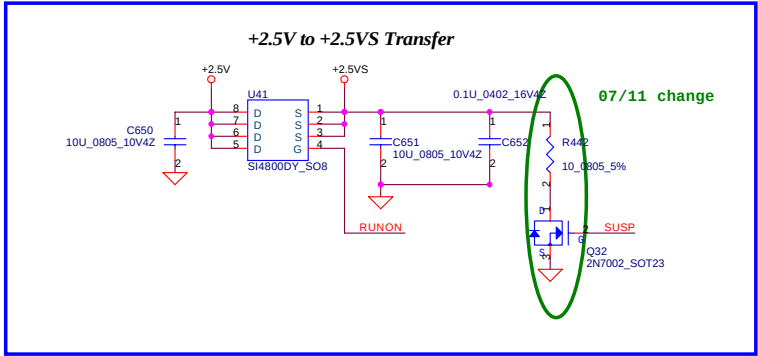
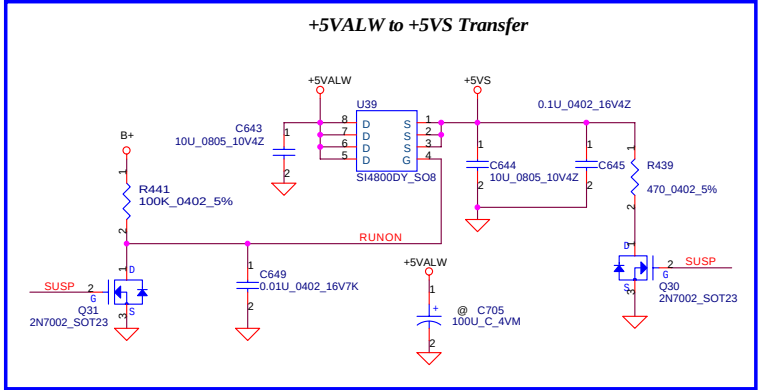
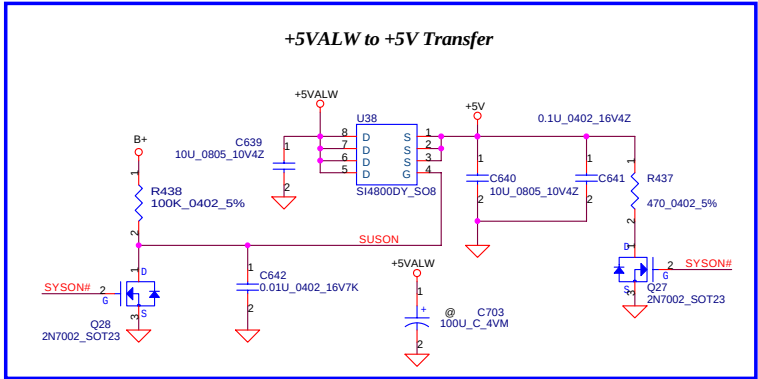


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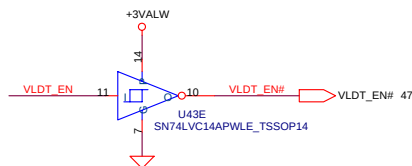
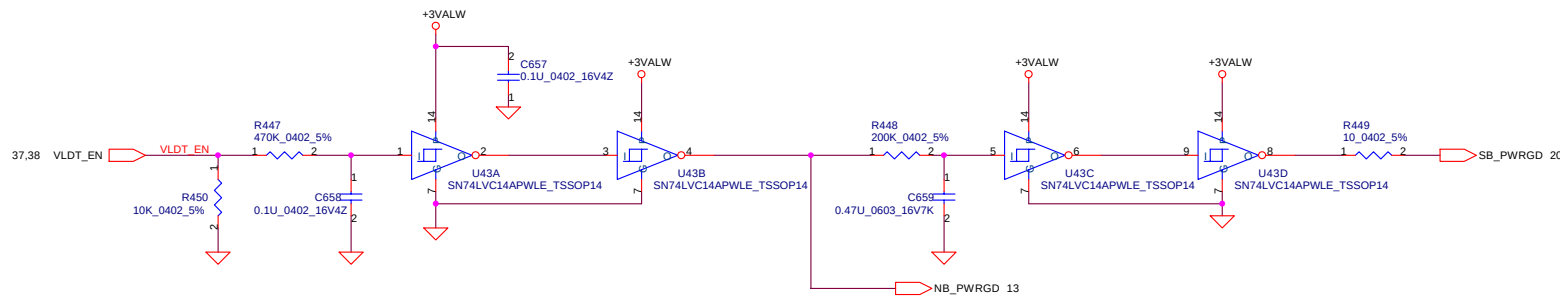
Tampa 2



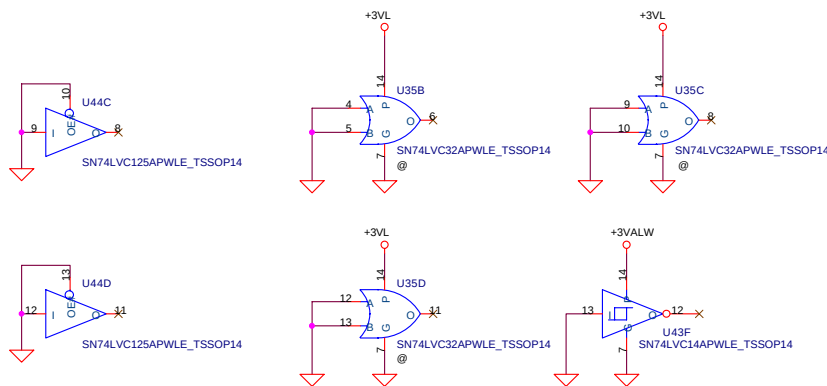
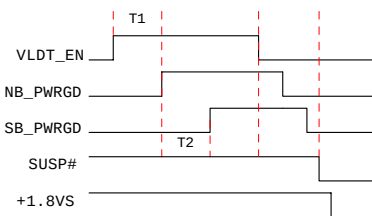
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note:T1 minimum 15ms,T2 minimum 33ms/maximum 500ms,
SUSP# goes to low after SB_PWRGD goes to low for power
down.



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Detector

Vin Detector : Cayenne		
18.234	17.841	17.449
17.597	17.210	16.813

Vin Detector : Boxster		
14.352	13.950	13.555
13.818	13.411	13.000

Cayenne : PR5=22K; PR6=19.6K		
Boxster : PR5=47K; PR6=27K		

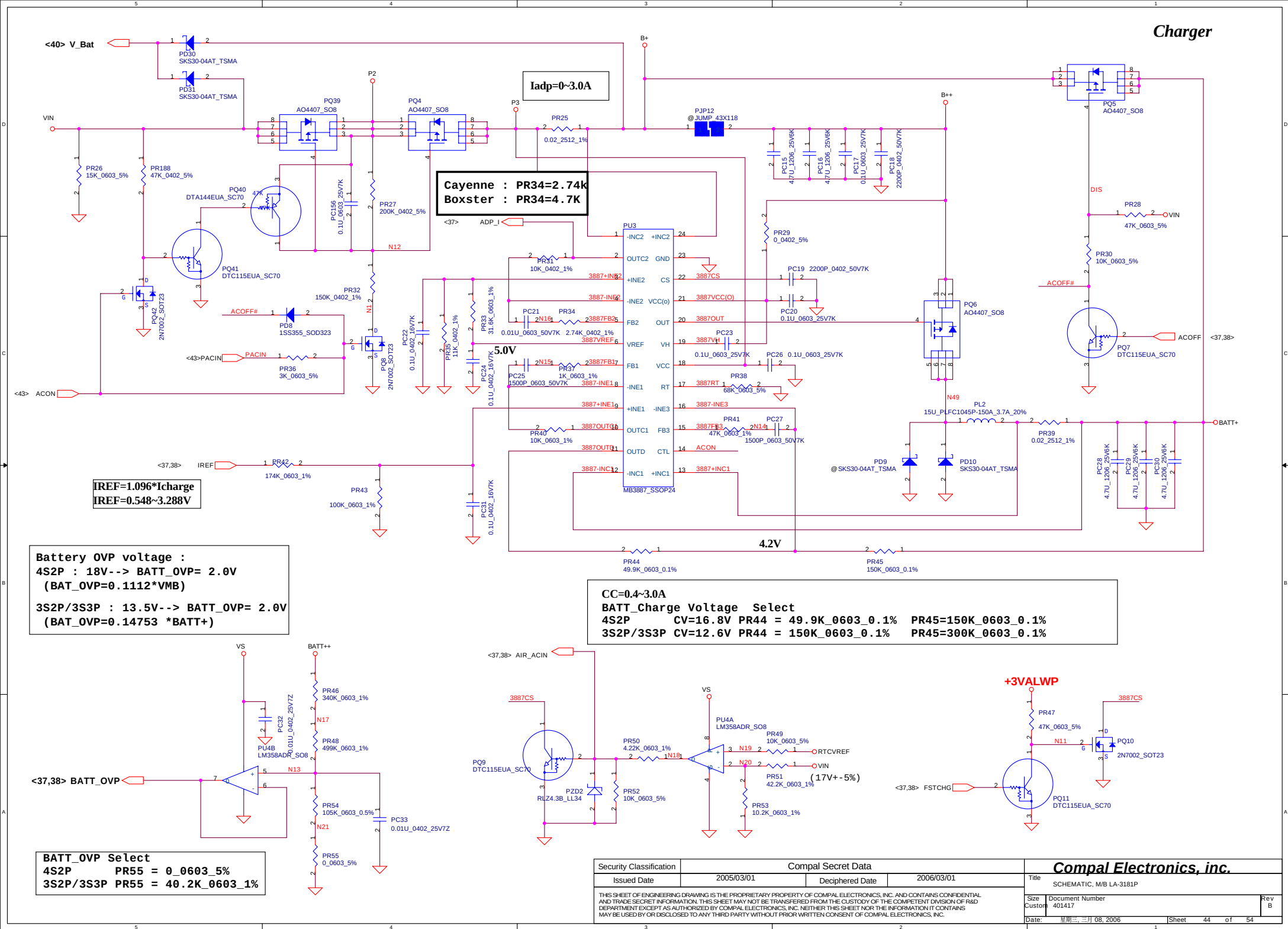
ACIN : Cayenne		
Precharge detector		
14.805	14.333	13.872
13.355	12.933	12.465

ACIN : Boxster		
Precharge detector		
12.384	12.000	11.624
10.927	10.600	10.223

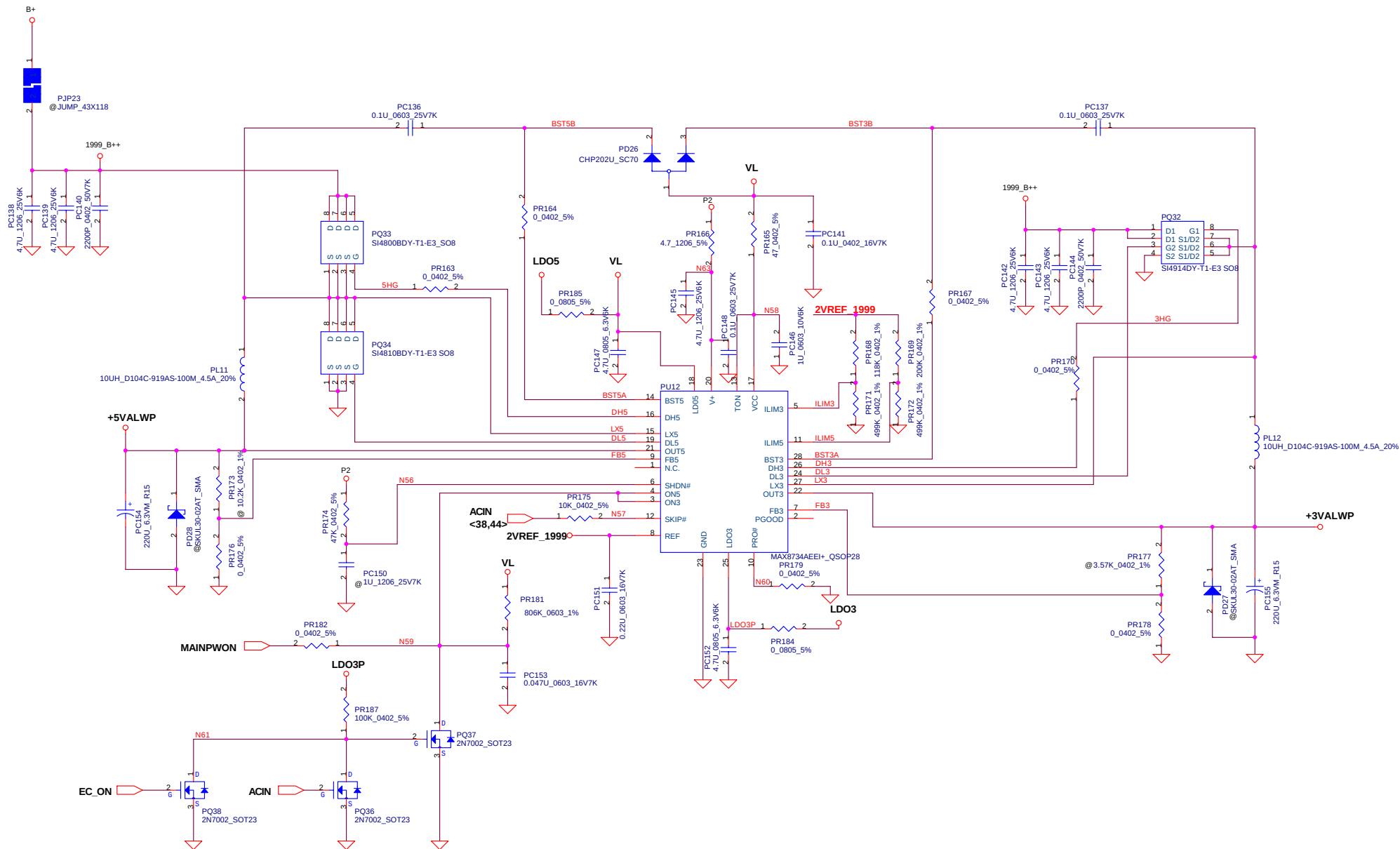
BATT		
Detector		
7.558	7.333	7.112
6.108	5.933	5.704

Cayenne : PR21=200K		
Boxster : PR21=300K		

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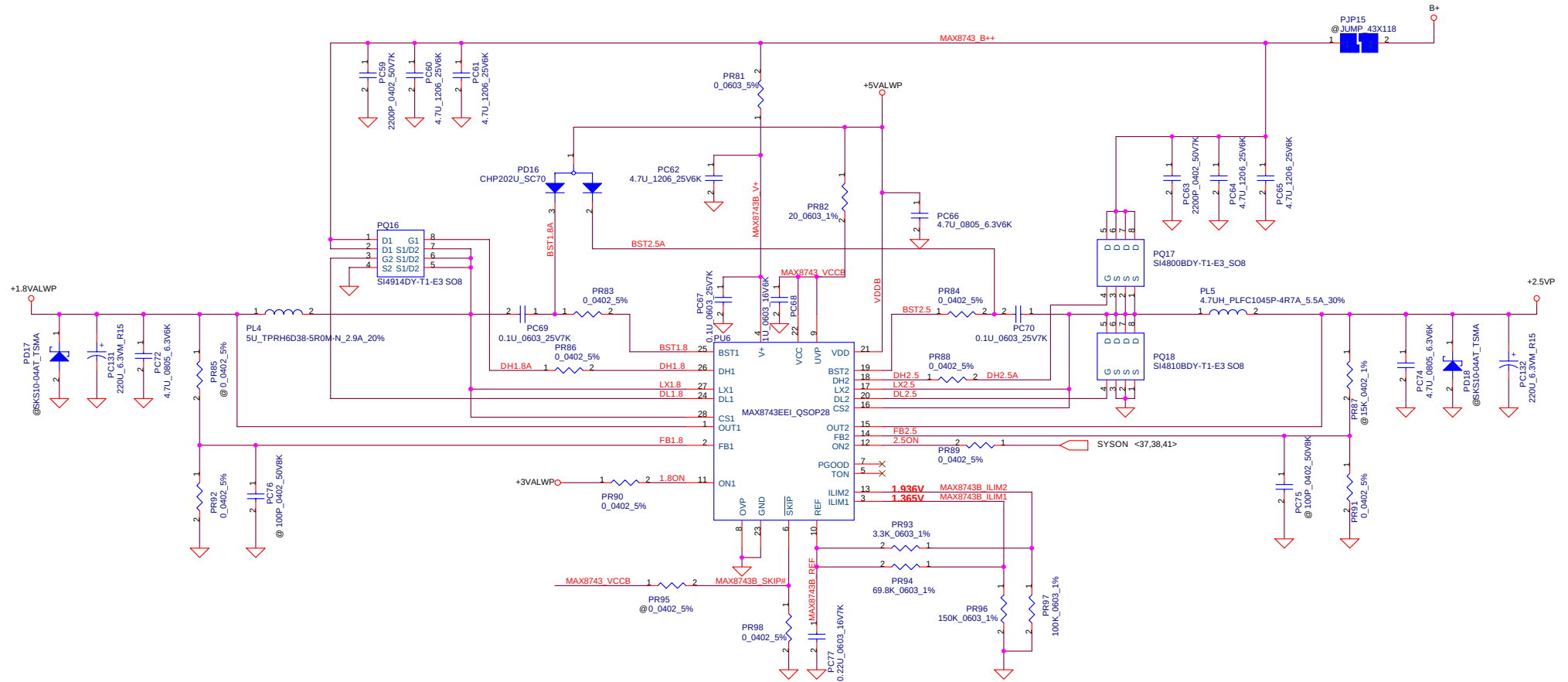


+3VALWP/+5VALWP



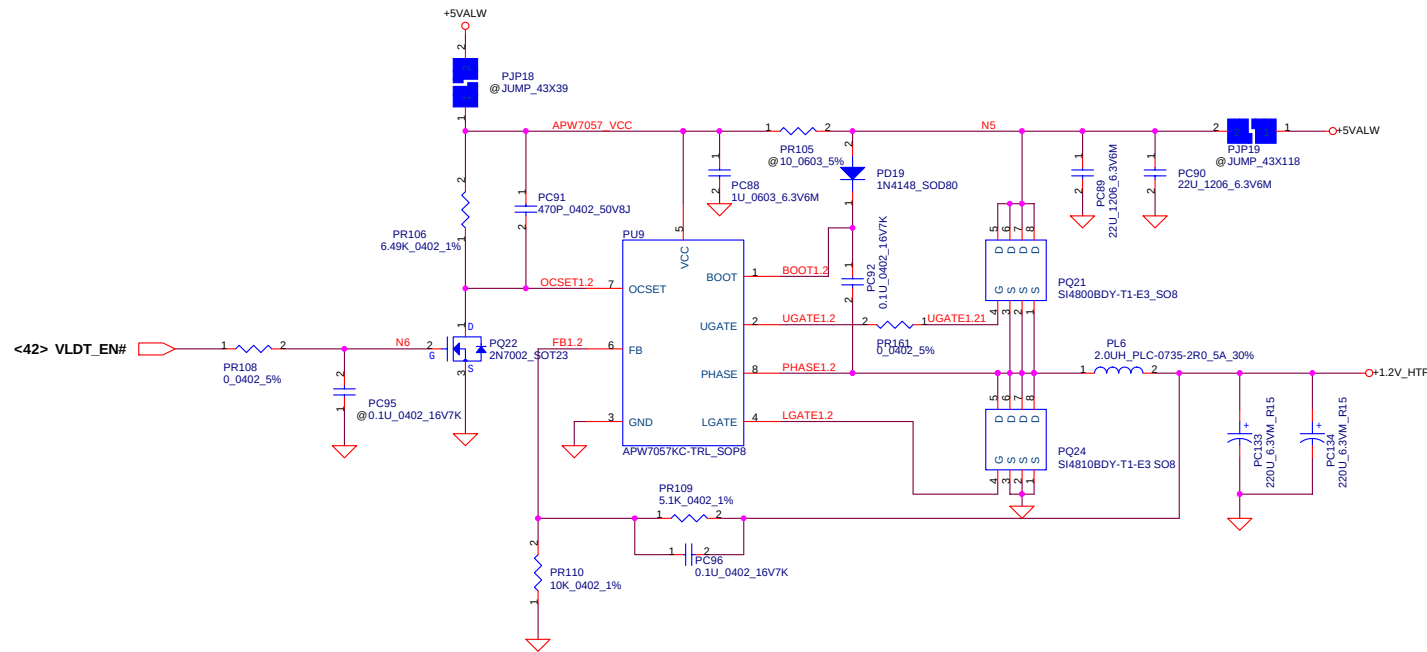
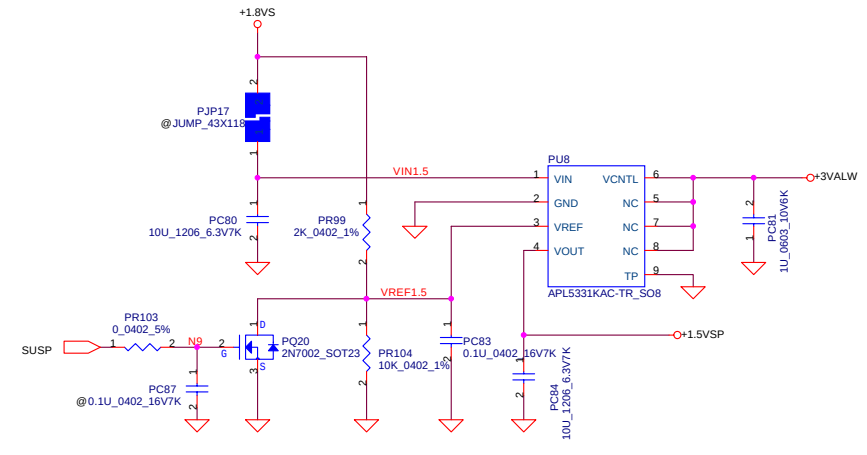
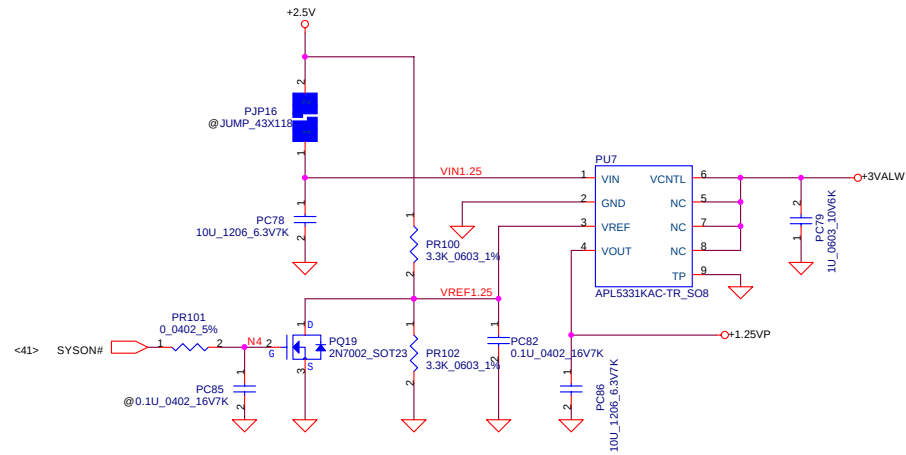
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+1.8VALWP/+2.5VP

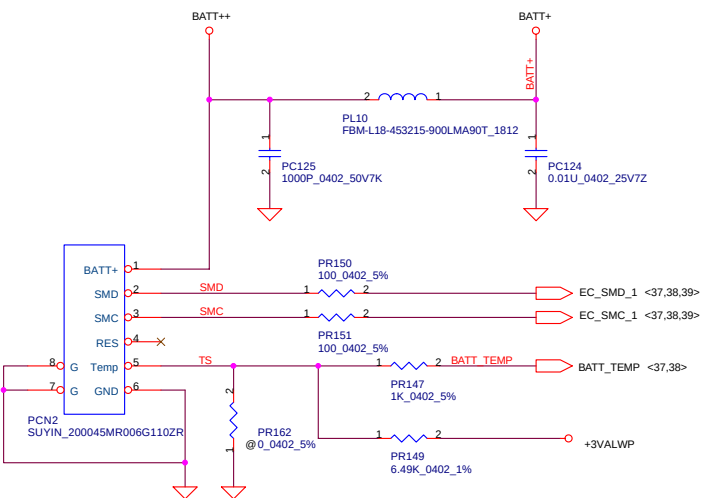


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+1.2V_HTP/+1.5VSP/+1.25VP



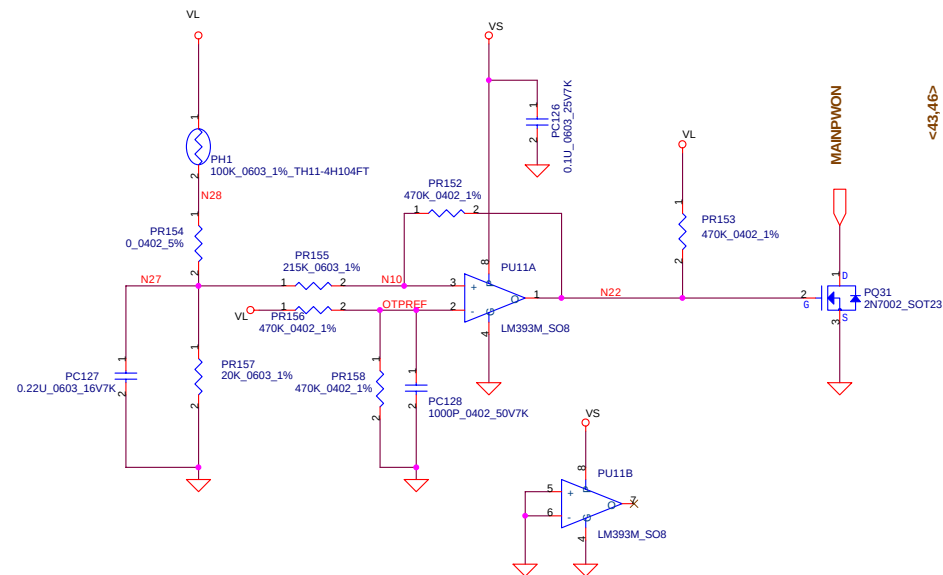
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PJPB1 battery connector
SMART
Battery:
1.BATT+
2.SMBD
3.SMBC
4.Res
5.Temp
6.GND

CPU

PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 50 +-3 degree C



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Battery Connect/OTP

Compal Electronics, inc.

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Item	Reason for change	PG #	Modify List	Date	B.Ver #
1	Add the functionality to turn on the system on from Off and S4 with the consumer IR.	45	Change 3/5VALWP regulator from MAX1902 to MAX1999	2005.04.08	
2	Change PCN1 from SP020022200 to SP020024800.	49	Change PCN1 from SP02000A000 to DC040001P00.	2005.04.08	
3	Because EMI test fail	48	Change CPU_CORE HI-SIDE MOS from A04408 to FDS6294, LOW-SIDE from A04410 to FDS6676AS	2005.05.18	
4	Because V_bat to Calgary havn a leakage current, cause precharge can't finisn.	44	Add PD30 and PD31 to supply the V_bat power.	2005.06.09	
5	Add air-adapter detector	44	Add PU4 to detector air-adapter in.	2005.07.02	
6	Adjust the MB3887 CC to CP response cause the adapter OCP.	44	Change the PR31 from 100k_0402_1% to 10k_0402_1% Change the PR34 from 10k_0402_1% to 2.74k_0402_1% Change the PC21 from 4700p_0603_50V to 0.01u_0603_50v	2005.07.29	

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5					4					3					2					1										
Item					Fixed Issue					Reason for change					PAGE					Modify List					M.B. Ver.					
<2005.04.18>					1						HP Jack + SPDIF change type					31 , 33					Del : U27 , C563 , C564 Add: Q52 , Q53 , Q54 , Q56 , Q57 , R571 , C730 , C731 , R567 , R569 , R568 , R570					0.2				
					2						Support CIR wake up from battery mode					4 , 37 , 38 , 41 , 35					12VALW change to B+ +3VALW change to LDO3 , +5VALW change to LDO5					0.2				
					3						for Marvell express card Rest timing					20 , 28					Add: Q55					0.2				
					4						for some HDD's LED alway on					24					Del: D29 , R259 , Q10					0.2				
					5						for card bus can't work					27					S1_VCC and S1_VPP change to +S1_VCC and +S1_VPP					0.2				
					6						For nissan common design					35					JP28 and JP29 pin swap					0.2				
					7						For keyboard issue					37					Del: D27					0.2				
<2005.04.27>					1						wake up from LAN					38					Add: R575(Pull UP PME_EC#)					0.3				
					2						For VOL_UP,DOWN function issue					38					POP: R418,R419,R420,R421					0.3				
<2005.05.3>					1						For CIR wake up					38					Add: R576, R577 to option					0.3				
<2005.05.4>					1						EC 910L include portion circuit					39					Add: R578 , Del:C630 , R422 , Q22 , U35A					0.3				
					2						ME change LED type					36					D18,D20,D21 from right angle change to vertical type					0.3				
<2005.05.6>					1						Add wireless LED current limit resister					17					Add: R581 current limit resister					0.3				
<2005.05.9>					1						TP conn pin reverse					35					Pin swap									
<2005.05.10>					1						ME change LED type					36					D25 from right angle change to vertical type									
					2						HP requirement from 75 ohm change to 33 ohm					33					R567 , R569 from 75 ohm change to 33 ohm									
					3						For nissan common design					35					Add: R582 , R583									
<2005.05.11>					1						For 2 way and 4 way touch pad					36					Add: R584 , R585									
<2005.06.10>											update JP23 dual USB connector to reverse type															0.4				
											DFX modification for Rev0.4 MB																			
											Change MR954, MC928, MR924, MR922, MR932, MC944, MC970, MC976, MC978, MC926 to correct pad size with Compal layout rule																			
											update USB connector to reverse type																			
											Change D6 form RB411 to RB491																			

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
<2005.06.27> 1		For clear H_RST# glitch	41	Add Q61	0.5
<2005.07.04> 1		For +1.8VS EMI	11	Change R61, R84 value from 0 ohm to 120 ohm	0.5
2		For +1.2V_HT power ripple	14	Change C197, C209, C254, C248, C251, C256, C258 value from 0.1U 16V4Z 0402 to 1U 6.3V4Z 0402	0.5
3		For +2.5VS EMI	15	Add C737, C738, C741, C742 220P 50V8J 0402	0.5
4		For +2.5VS EMI	15	Add C739, C740, C743, C744 1000P 50V7K 0402	0.5
5		For Mini-PCI_CLK EMI	30	Mount R325 and C512	
6		For CardBus chip PCI_CLK EMI	25	mount R279 and C442	0.5
7		For LAN chip PCI_CLK EMI	29	Mount R322 and C504	0.5
8		For EC K/B chip PCI_CLK EMI	30	Mount R415 and C628	
<2005.07.05> 1		For USB EMI	34	Add L33, L34	
2		For USB EMI	34	change R561,R559,R562,R560 size from 0603 to 0402	
<2005.07.07> 1		For dock Docking audio noise	31	Add Q58, R589, Q60, R590, Q59, R589	
2		For Dock_LOUTR/L EMI	40	Add R591, C745, R592, C746	
3		For Docking TV_out signals EMI	40	Add R593, C747, R594, C748,C749, C750, R595, C751, C752	
<2005.07.11> 1		For accelerate +2.5VS discharge speed	40	change R442 size and value from 470_0402 to 10_0805	
2		For LAN lamp	29	Swap Activity and Link Lamp	
<2005.07.25> 1		For SanDisk SD 256M card could not work issue	25	delete U48 Quick switch reserve schematics	
2		For SanDisk SD 256M card could not work issue	25	Delete R463, R465, R466, R476, R268	
3		For SanDisk SD 256M card could not work issue	26	Delete R270, R267, R547, R548	
4		For SanDisk SD 256M card could not work issue	26	Mount R550 and R549	
<2005.07.28> 1		For lower power consumption	38	Add and un-mount R596	
2		For CRT Assy	18	change CRT footprint	

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5					4					3					2					1				
Item		Fixed Issue			Reason for change			PAGE		Modify List					M.B. Ver.									
<2005.08.11>		1			Delect all reserve 0 ohm resistors.			41		Delete R24, R125, R21 , R73 , R263, R565					0.5									
		2			For EMI solution on switch connector			11		Add C753~C771 total 19 pcs					0.5									
		3			For ATI suggestion on RS480			14		Change C200, C202, C242, C232 from 0.1U 16V4Z 0402 to 1U 6.3V4K 0402					0.5									
<2005.08.23>		4			Relocate damping resistor to solve Sandisk issue			15		Relocate R266, R458, R459, R460, R461, R462					0.8									
		5			Change from AGND to DGND for Codec precision improvement			15		Change Q16/Q17 pin3 and R334 pin2 to DGND					0.8									
		6			Add +3VALW power rail for Boxster lid switch use			30		Add +3VALW to JP28 pin25					0.8									
<2005.09.05>		1			EMI Requirement			34		Add Varistor on C756, C757, C758 and Add Caps on C760, C761, C762, C763, C765 (9/5 Cayenne MV)					1A									
<2005.09.26>		1			EMI Requirement			34		Add Varistor on C754, C755 and Add Caps on C753, C759, C764, C766, C767, C768, C769, C779, C771 (9/26 Cayenne MV2)					1A									
		2			Codec lost issue			31		Add R356, R587, 47Kohm					1B									
		3			Codec lost issue			33		Change R359 and R586 to 1Kohm					1B									
<2005.10.17>		1			Codec lost issue			31		Add R650 and R651 10Kohm, reserve R652					1B									
<2005.10.19>		1			AIR_ACIN function			20		Change AIR_ACIN from pin80 to pin137, add R653 for BID recognition					1B									

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<2005.11.08>

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		Change power plane to +VCC 480/482 for RS482M	11, 13, 14	Add PJP30 and PJP31	LA2771 R01
2		Reserve R601, SUS_STAT# should be NC if populate RS482M/SB450	20	Resereve R600	LA2771 R01
3		Reserve R71, SUS_STAT# should be NC if populate RS482M/SB450	14	Reserve R71	LA2771 R01
4		To solve Q24 damage issue when plug Tempa2	40	Add D40	LA2771 R01
5		To solve Q24 damage issue when plug Tempa2	15	Add R607	LA2771 R01
6		To distinguish new VRAM to old VRAM (Hynix/Samsung)	20	Add R606 and R605	LA2771 R01
1			20		
1			34		
2			31		
3			33		
1			31		
1					
3			40		
1			40		
2			29		
1			25		
2			25		
3			26		
4			26		
1			38		
2			18		

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