

Compal Confidential

HBL50 Schematics Document

Intel Yonah Processor with 945GM/945PM + DDRII + ICH7M
(With nVIDIA NB7M-SE)

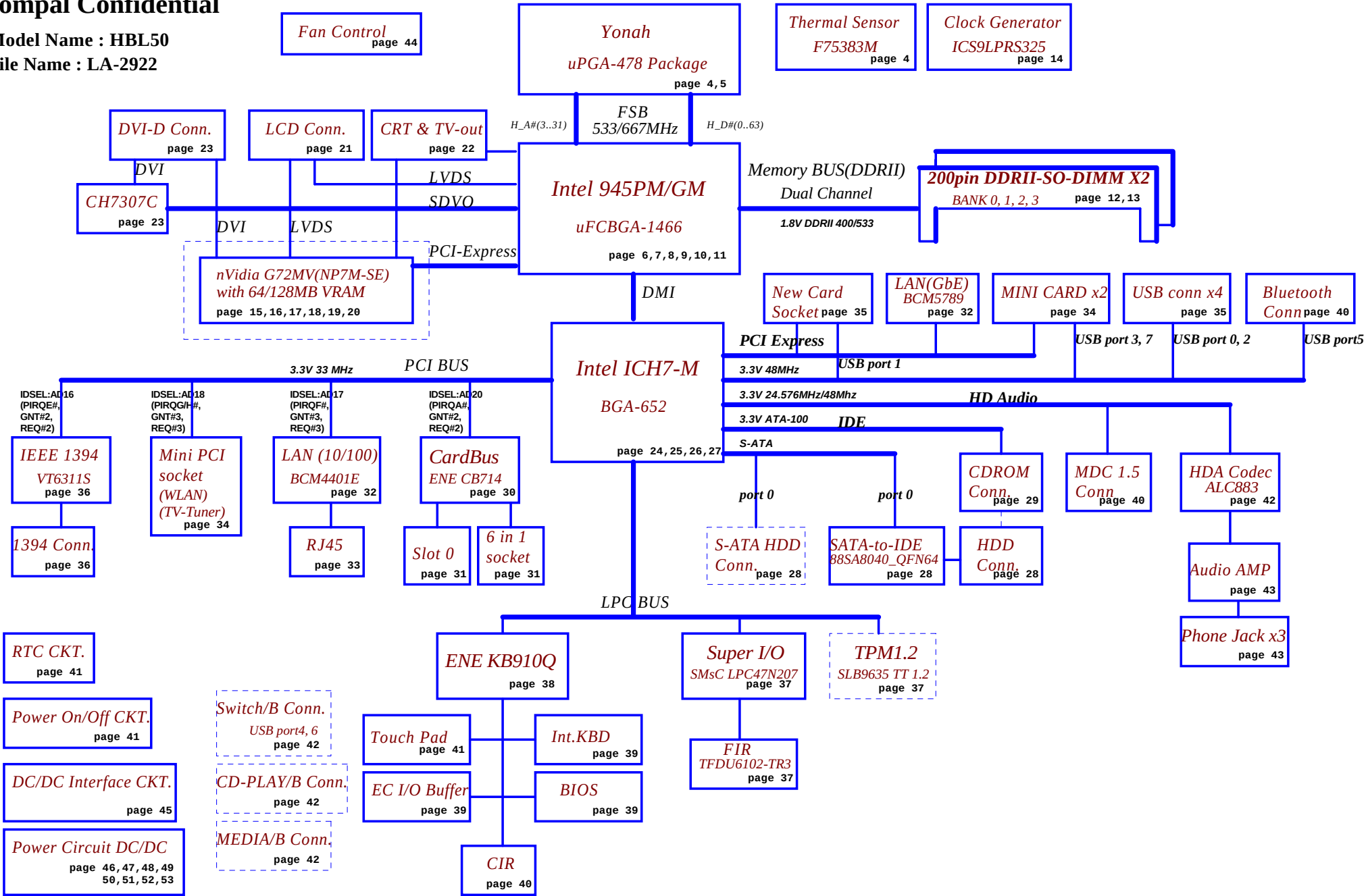
2006-09-05

REV: 1.0

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					401454
				Date: 星期四, 九月 14, 2006	Sheet 1 of 55

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Model Name : HBL50
File Name : LA-2922



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				Document Number
				401454
				Rev A
				Date: 星期四, 九月 14, 2006
				Sheet 2 of 55

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Fintek F75383M	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

EC SM Bus2 address

ICH7M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

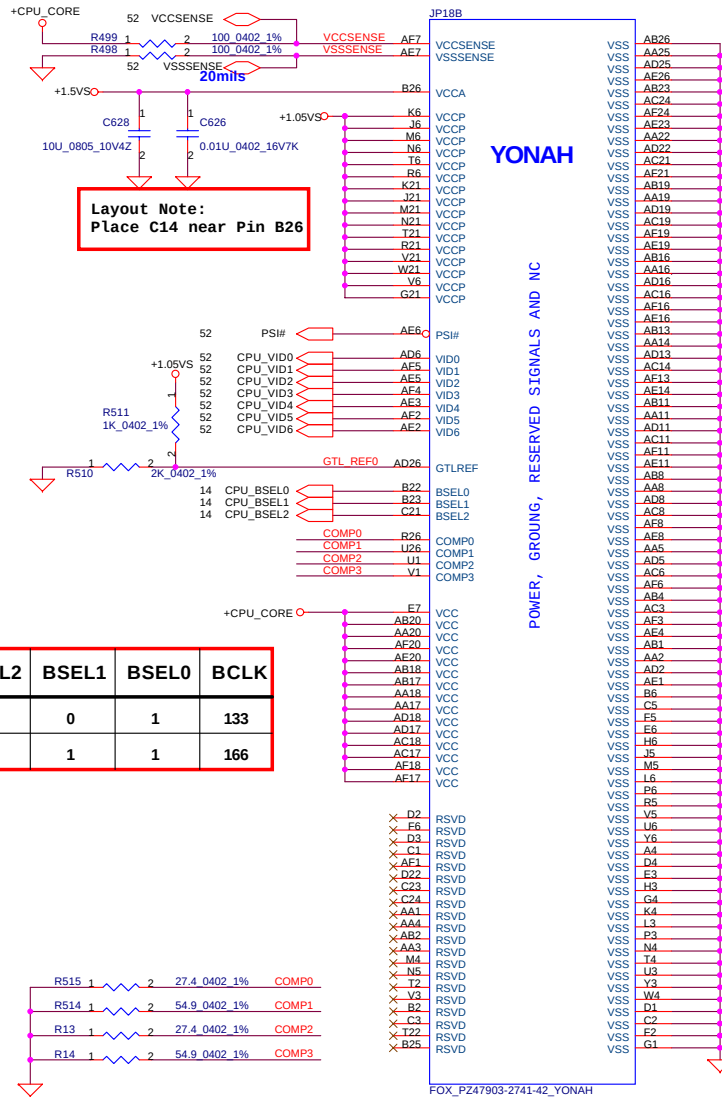
BTO Item	BOM Structure
VGA	PM@ + VGA@
UMA	GM@
UMA's DVI	7307@
LAN(10/100)	4401@
LAN(GIGA)	5789@
MINI_CARD1	MINI1@
MINI_CARD2	MINI2@
SATA-to-IDE	8040@
PATA	PATA@
GRAPEVINE	GRA@
G72MV Only	G72@
G73 Only	G73@
VRAM	X76@
VRAM 64M	64@
VRAM 128M	64@+128@
VRAM 256M	64@+128@+256@
MEDIA/B	MEDIA@
CIR	CIR@
FIR	FIR@
GENEVA	GEN@
Sub-woofer	SUB@
5789&5787	8789@
4401&5789	0189@
VP1020	VP1020@
INTERNAL MIC	INTMIC@
1394	1394@
SATA HDD	SATA@
DVI	DVI@
CardReader	4IN1@
New Card	EXP@

SKU ID Table

SKU ID	SKU
0	PM
1	GM
2	
3	
4	
5	
6	
7	

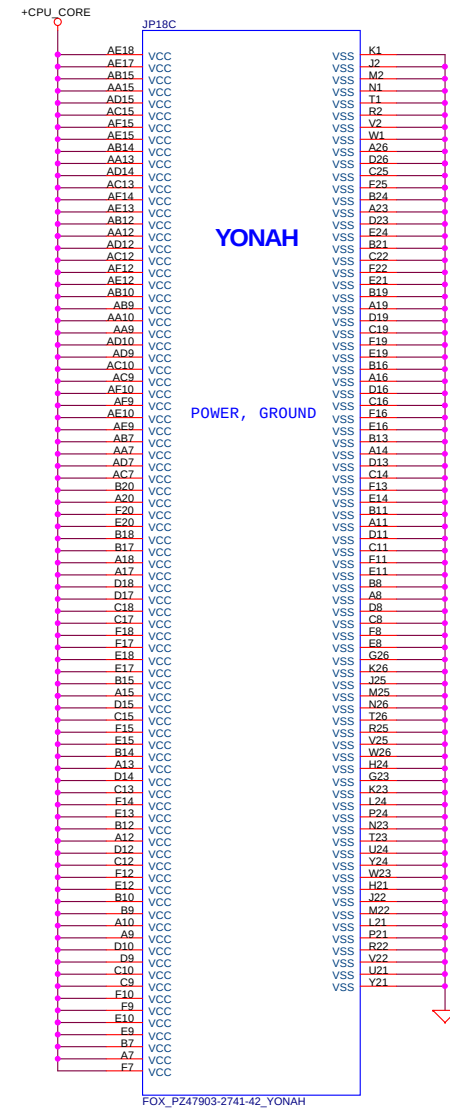
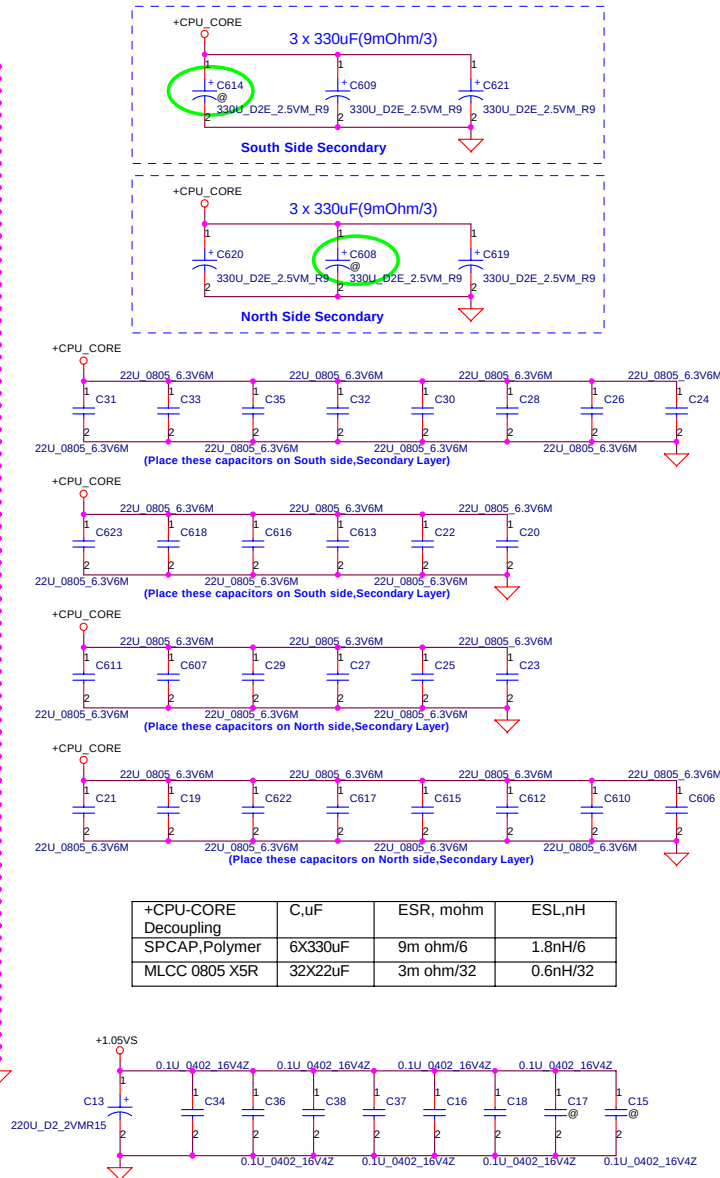
G72MV	G72MV@
	G72MV64@
	G72MV128@
G72MZ	G72MZ@
G73	G73M128@

Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.40hms
with 50 mil spacing.
Place PU and PD within 1 inch of CPU.



TRACE CLOSELY CPU < 0.5'

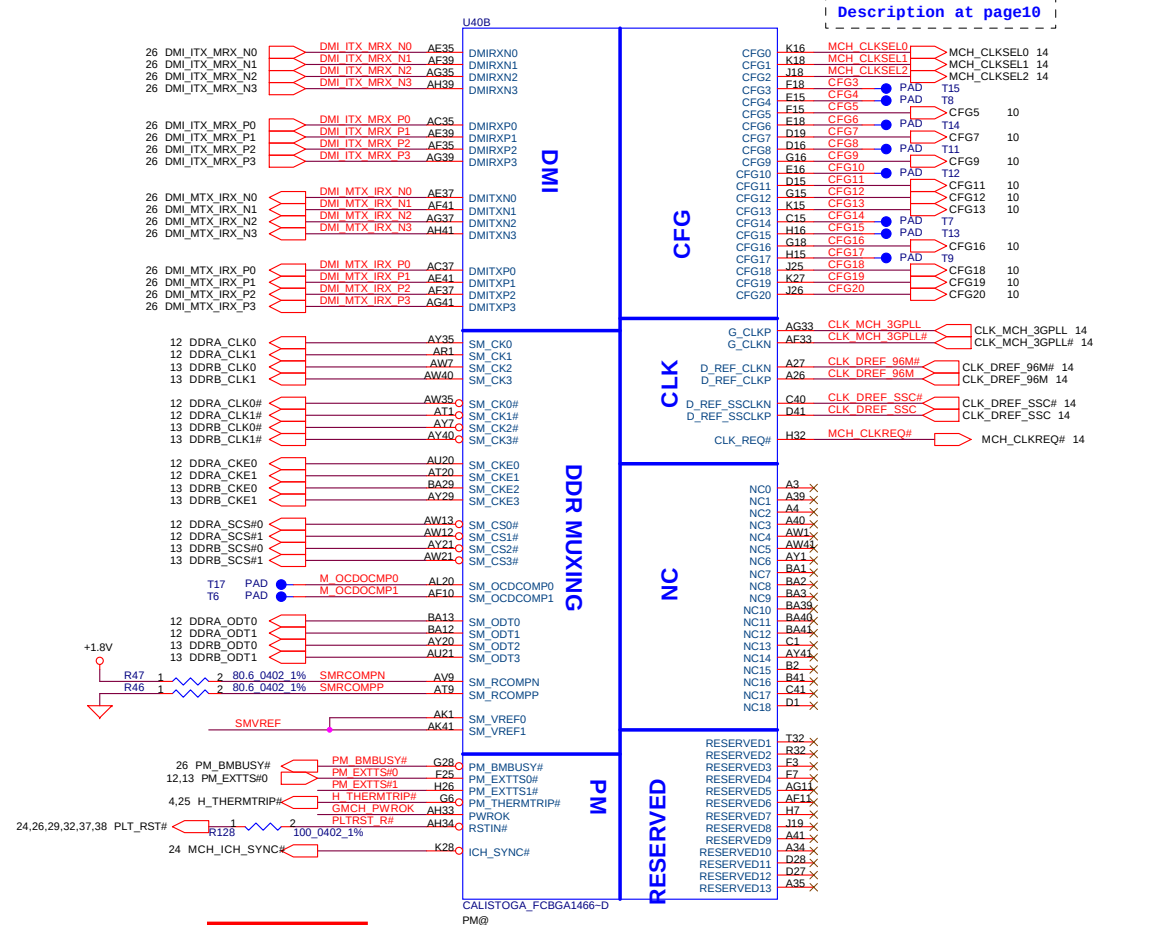
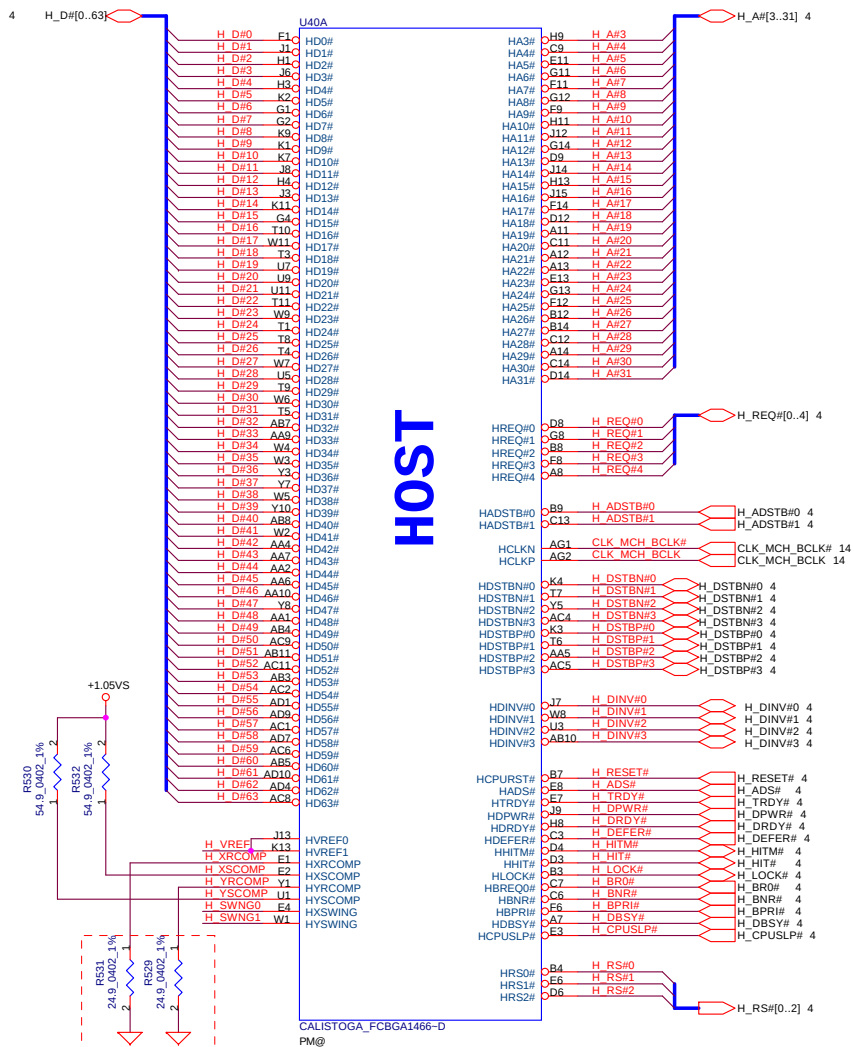
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.40hms)
COMP1, COMP3 layout : Space 25mils (550hms)



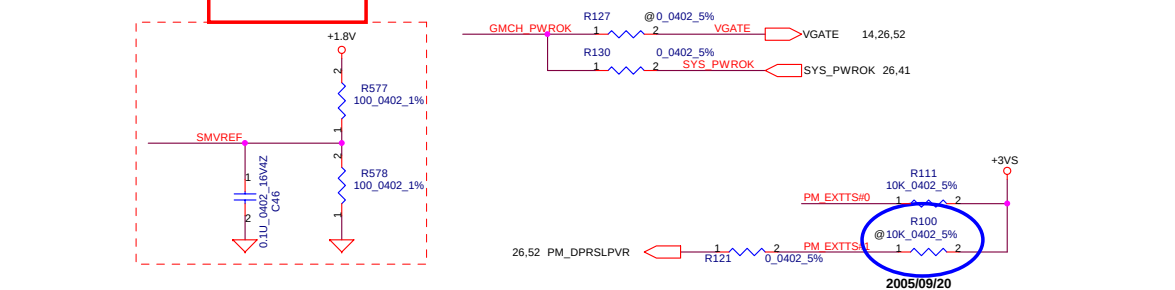
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					401454
				Date	星期日, 九月 14, 2006
				Sheet	5 of 55

945GM(SL8Z2)[A3]: SA0000059K0(ABO!)

945PM(SL8Z4)[A3]: SA00000KDE0(ABO!)

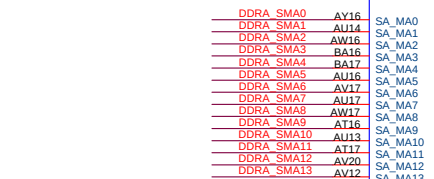
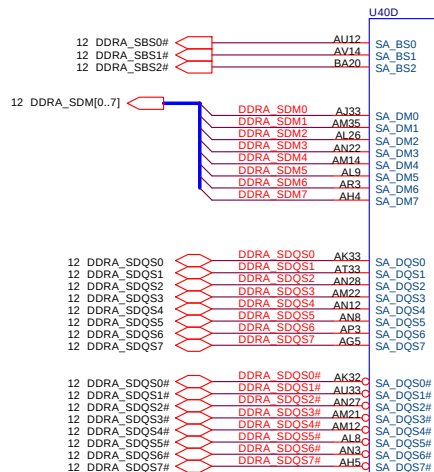
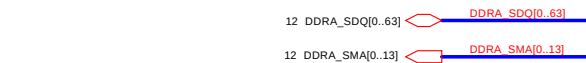


Layout Note:
SMVREF trace
width and spacing
is 20/20.



Layout Note:
H_XRCOMP / H_YRCOMP / H_VREF / H_SWNG0 /
H_SWNG1 trace width and spacing is 10/20.

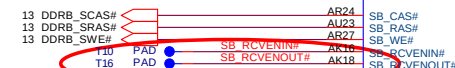
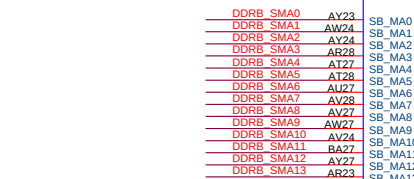
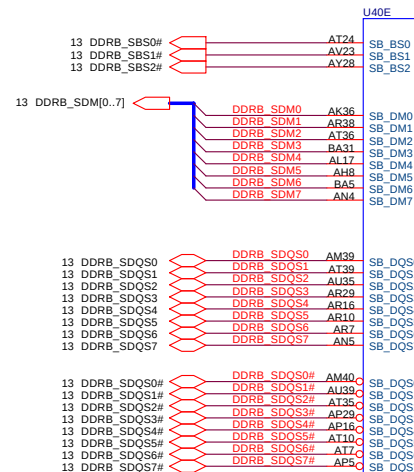
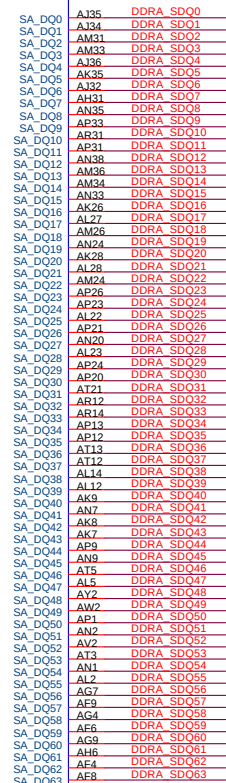
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						Size		Document Number		Rev	
						B		401454		A	
						Date		星期四, 九月 14, 2006		Sheet 6 of 55	



check layout

CALISTOGA_FCBGA1466-D
PM@

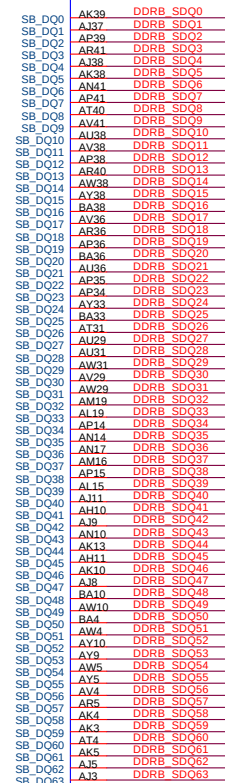
DDR SYS MEMORY A



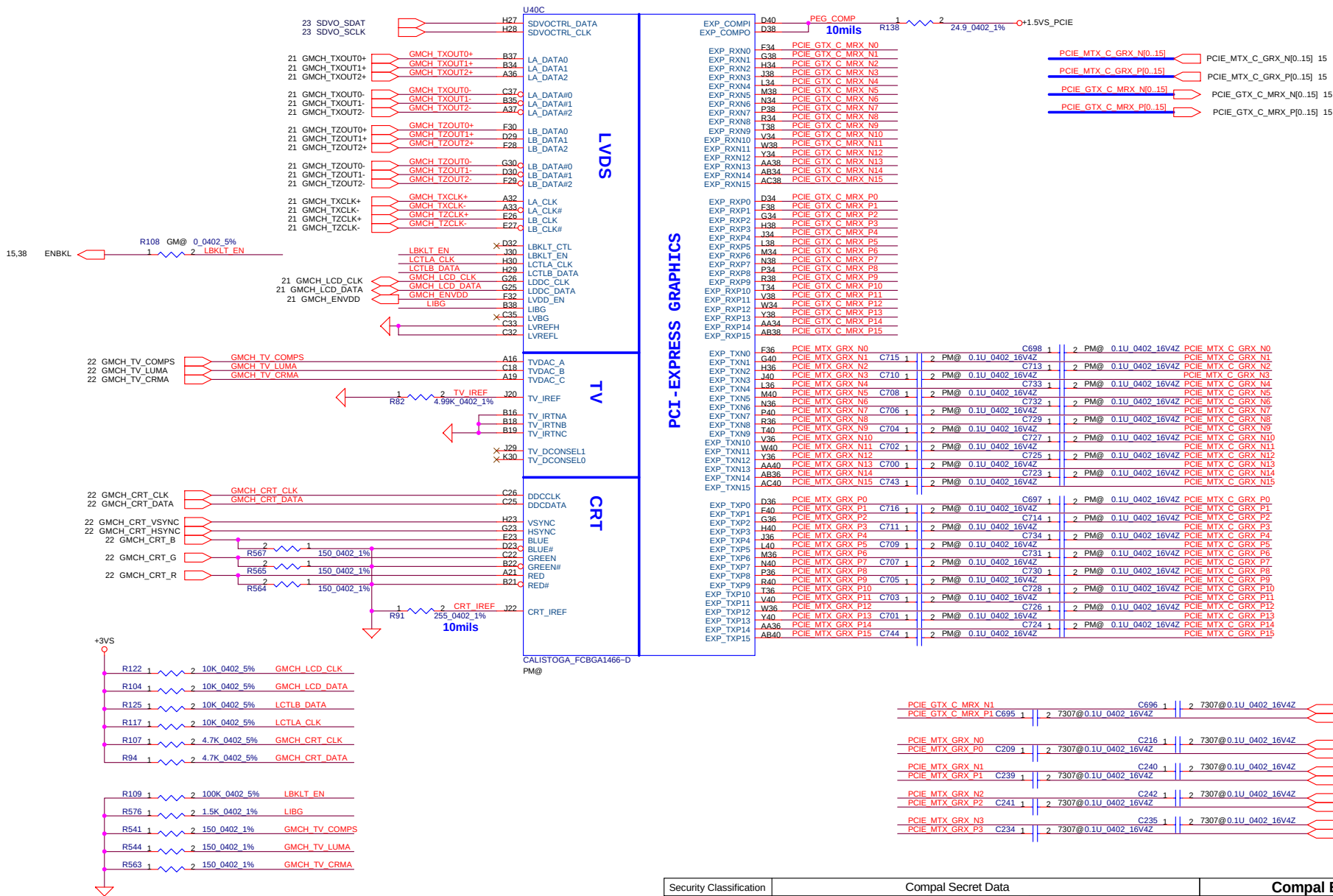
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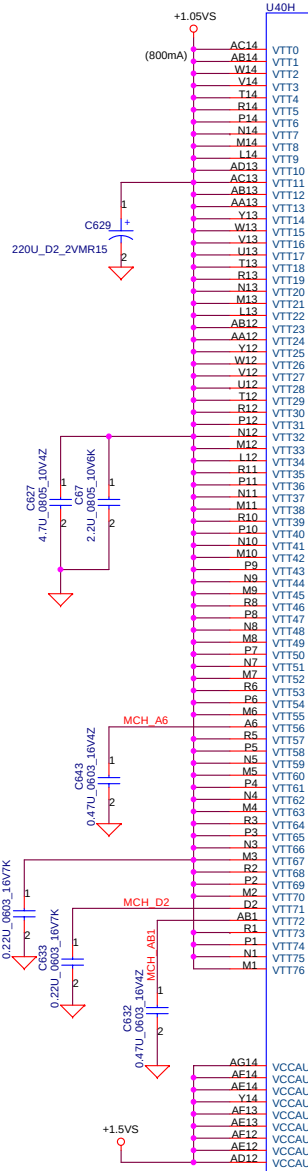
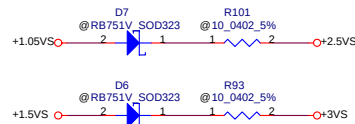
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PM@

DDR SYS MEMORY B

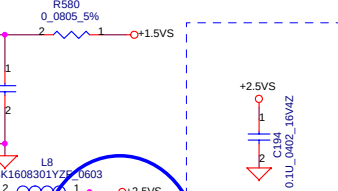
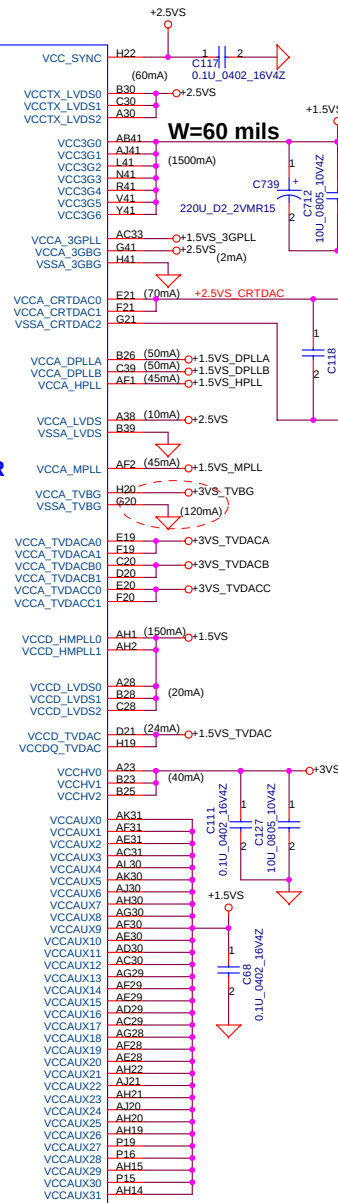


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Size B		Document Number		Rev A	
Date		401454		Sheet 7 of 55	
Date		星期四, 九月 14, 2006		1	

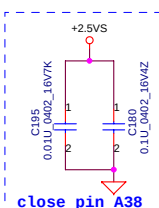




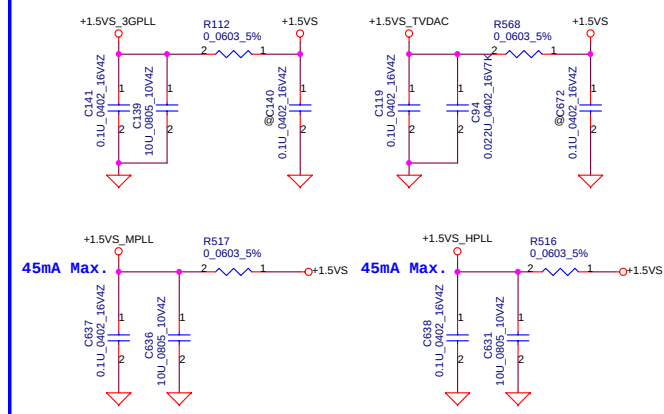
POWER



CR7DAC: Route caps within 250mil of Alvisto. Route FB within 3" of Calistoga



PCI-E/MEM/PSB PLL decoupling

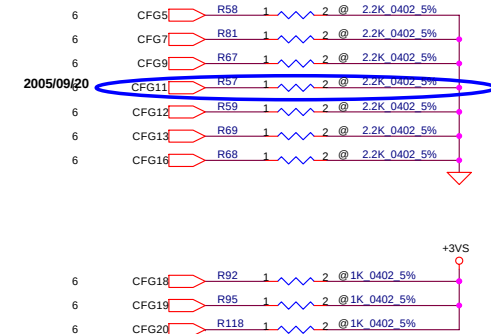
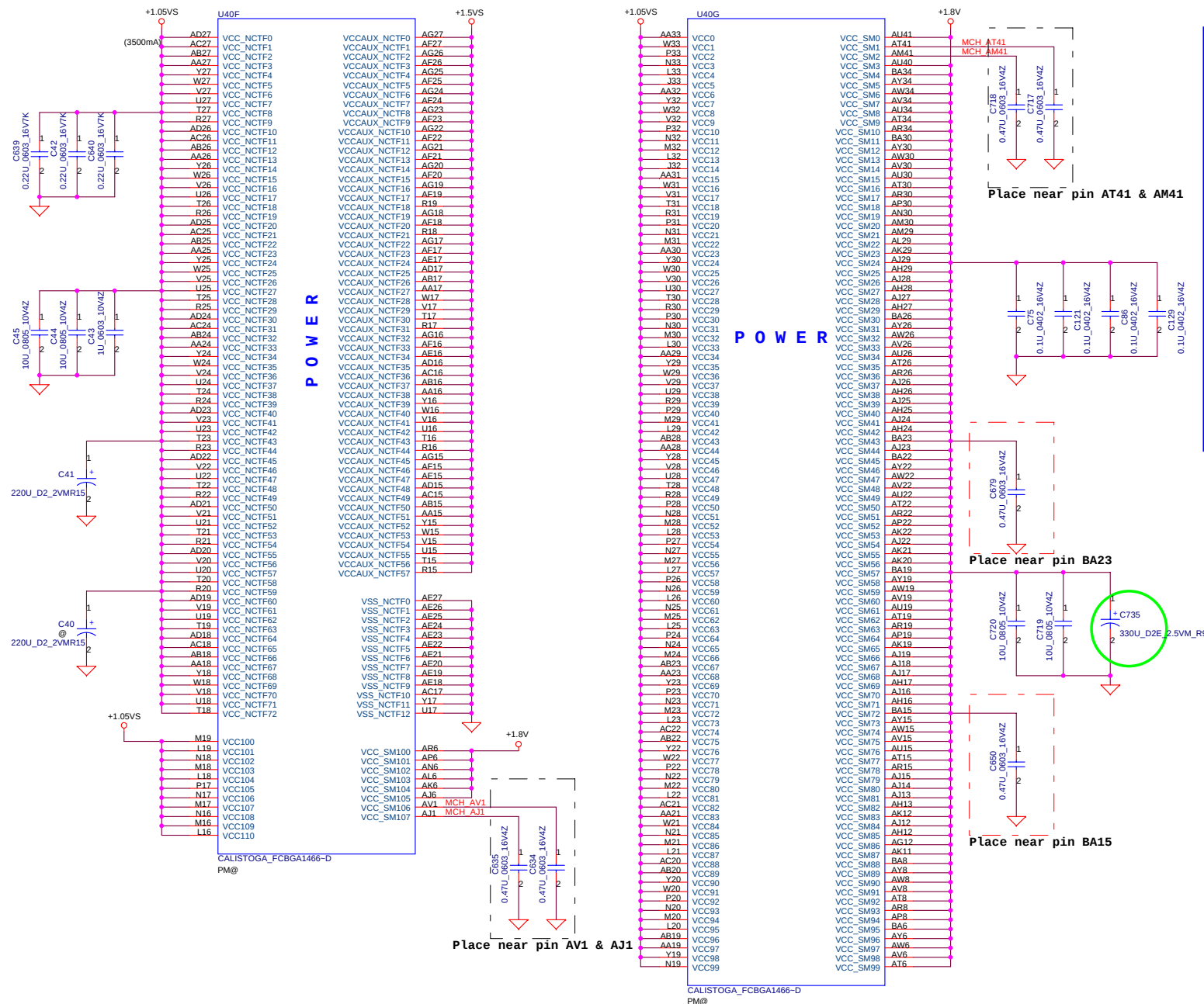


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				401454	Rev A
				Date: 星期四, 九月 14, 2006	Sheet 9 of 55

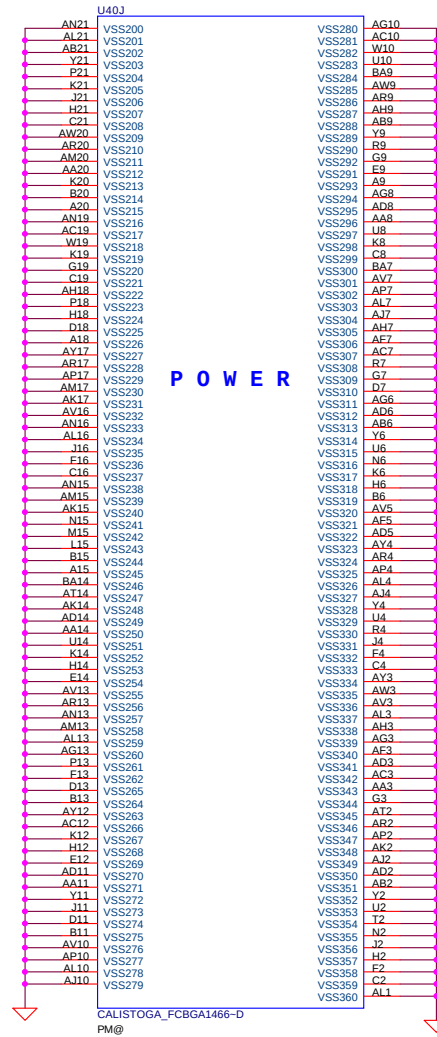
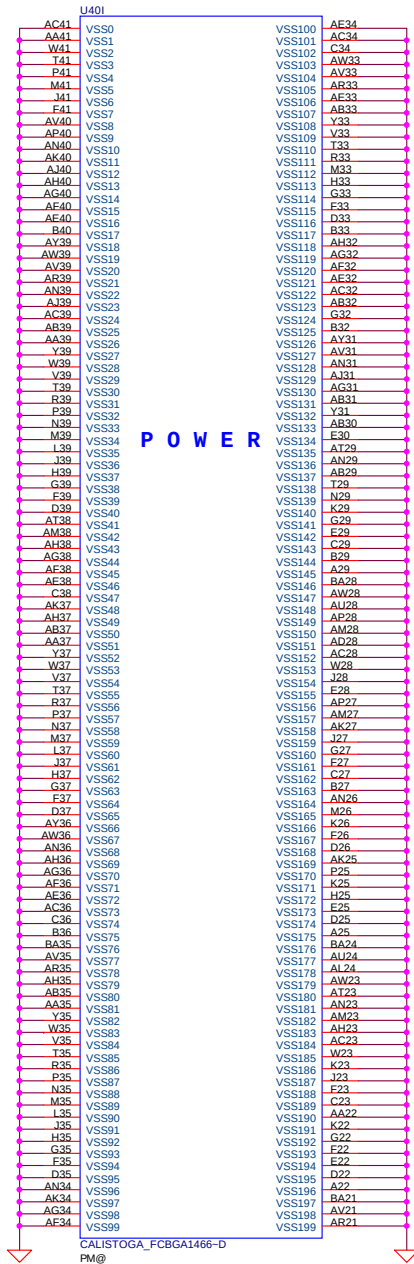
Strap Pin Table

CF6[3:17] have internal pull up
CF6[19:18] have internal pull down

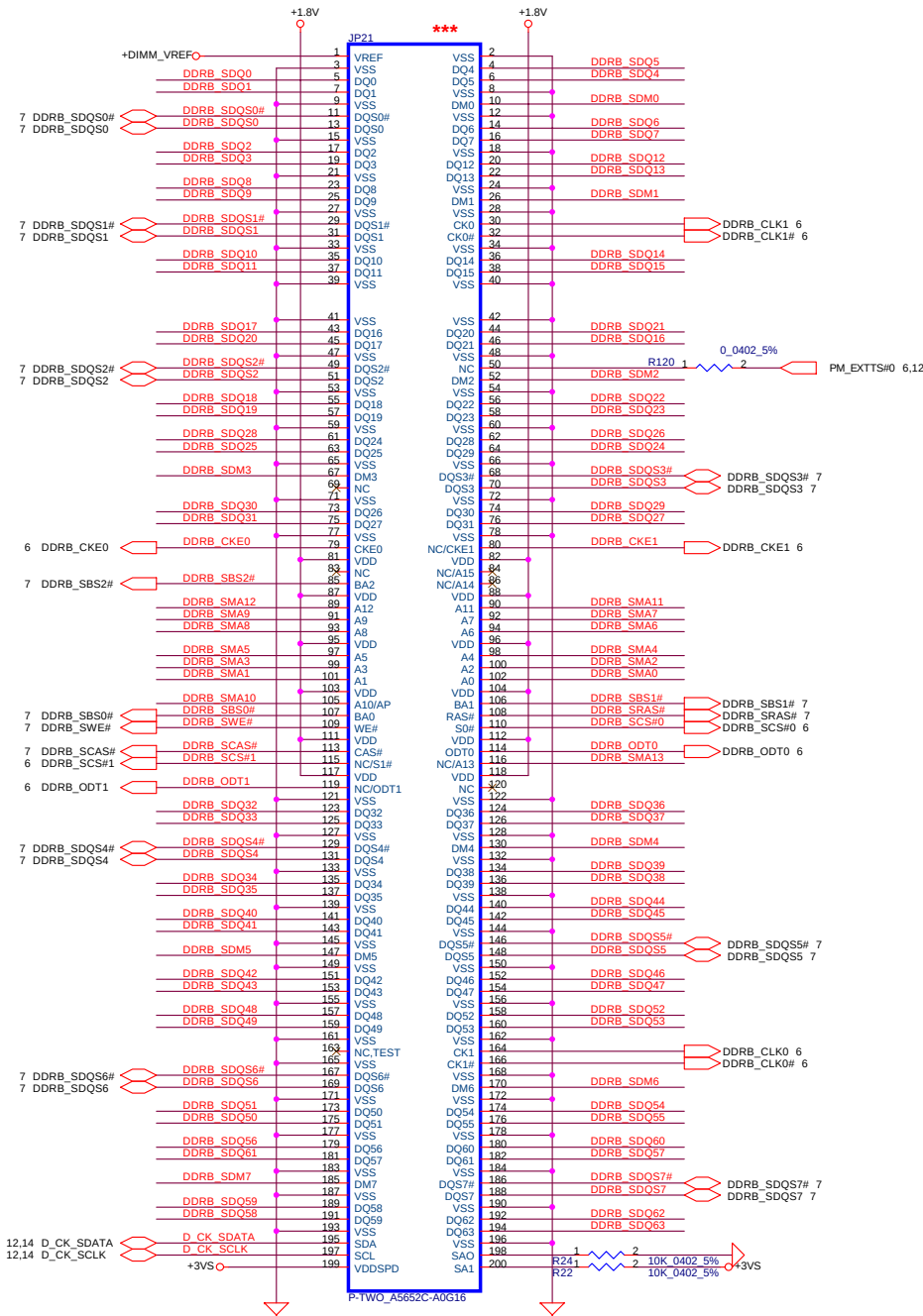
CF6[2:0]	011 = 667MT/s 001 = 533MT/s FSB
CF65	0 = DMI x 2 1 = DMI x 4 *(Default)
CF67	0 = Reserved 1 = Mobile Yonah CPU*(Default)
CF69	0 = Lane Reversal Enable 1 = Normal operation*(Default)
CF611	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CF6[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CF616	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CF618	0 = 1.95V *(Default) 1 = 1.5V
CF619	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CF620 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.



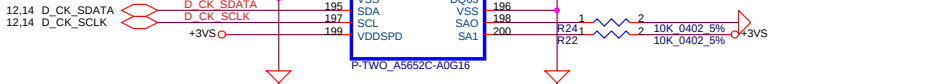
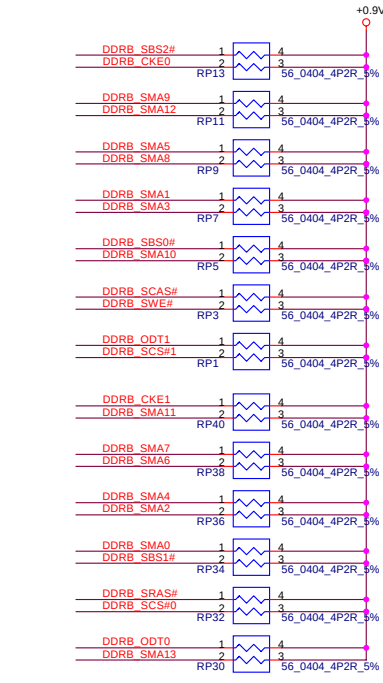
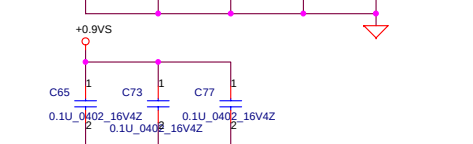
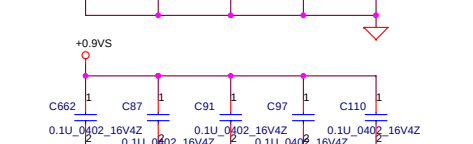
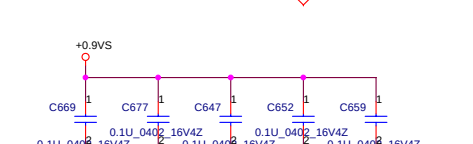
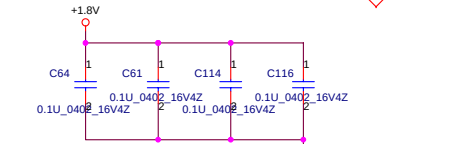
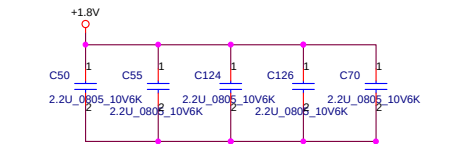
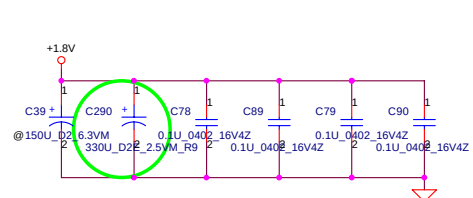
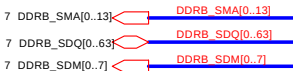
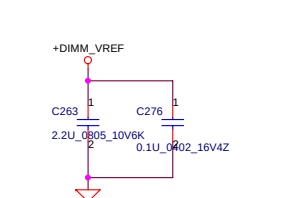
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				B				A			
				401454							
				Date: 星期四, 九月 14, 2006				Sheet 10 of 55			



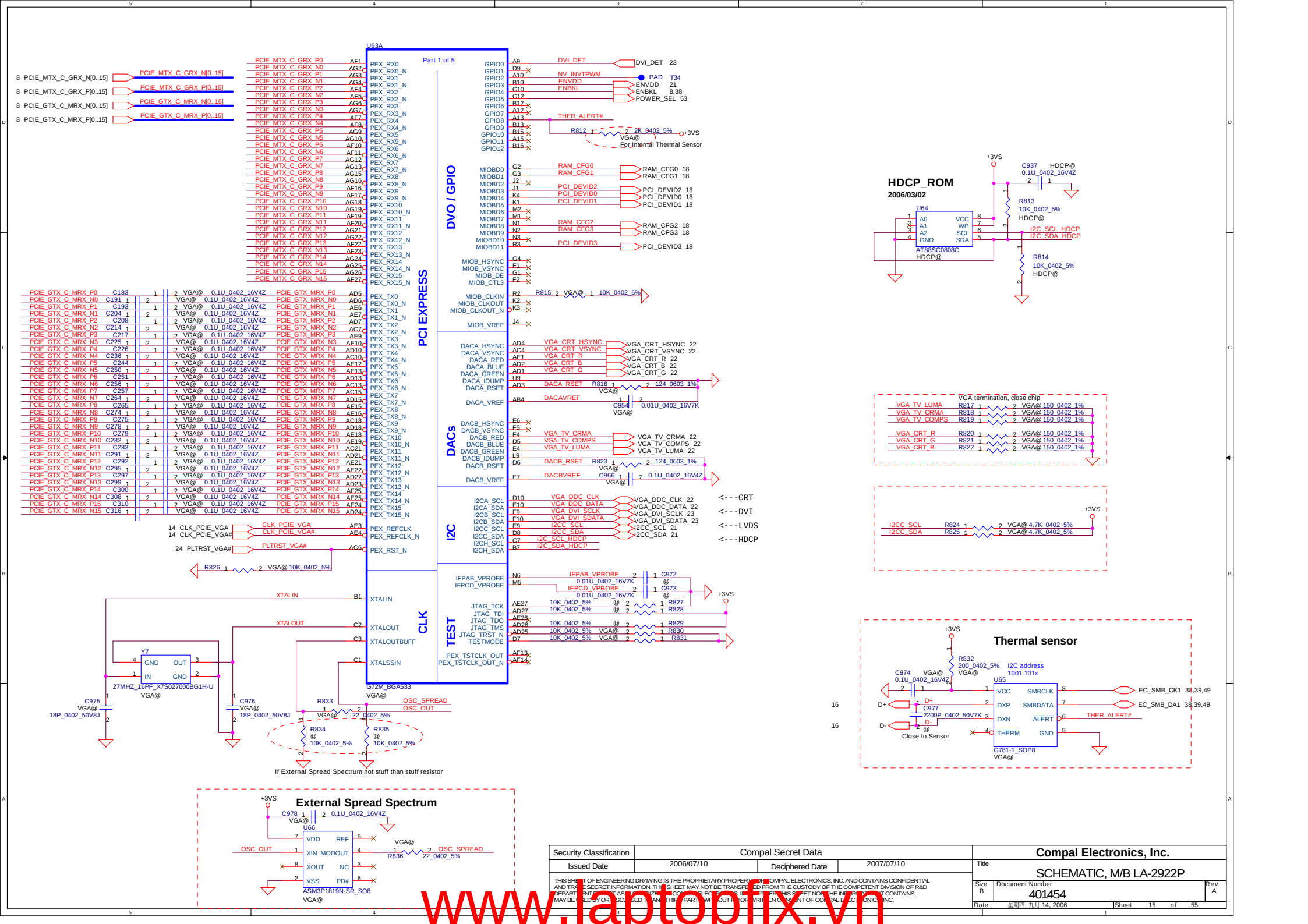
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				Date: 星期四, 九月 14, 2006	Sheet 11	of 55

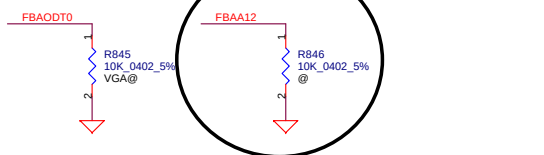


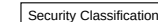
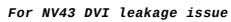
DIMM1 STD H:5.2mm (BOT)



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				401454	Rev A
				Date: 星期四, 九月 14, 2006	Sheet 13 of 55



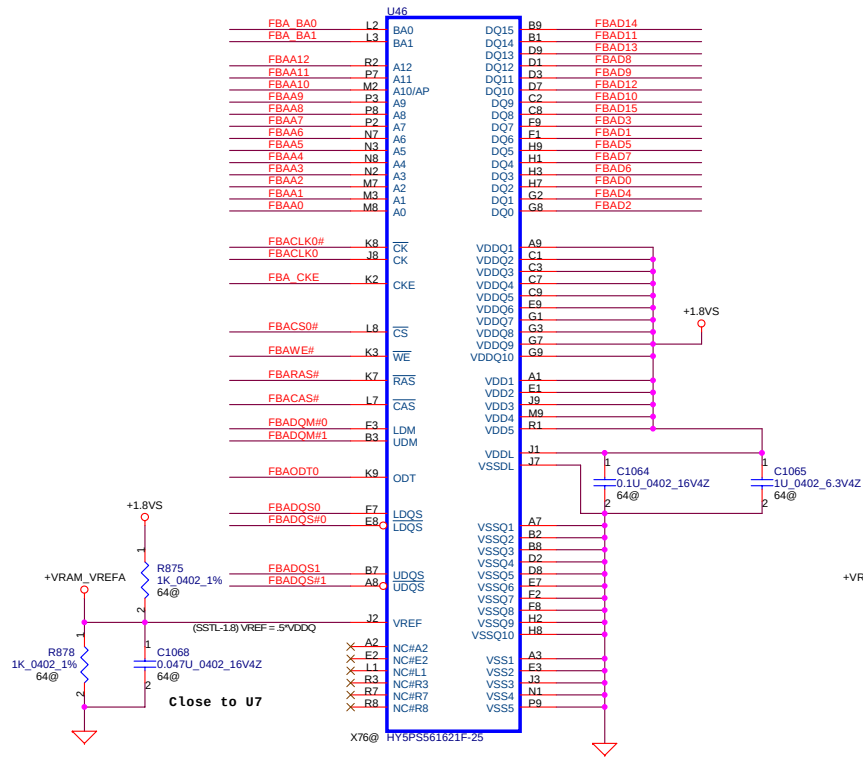




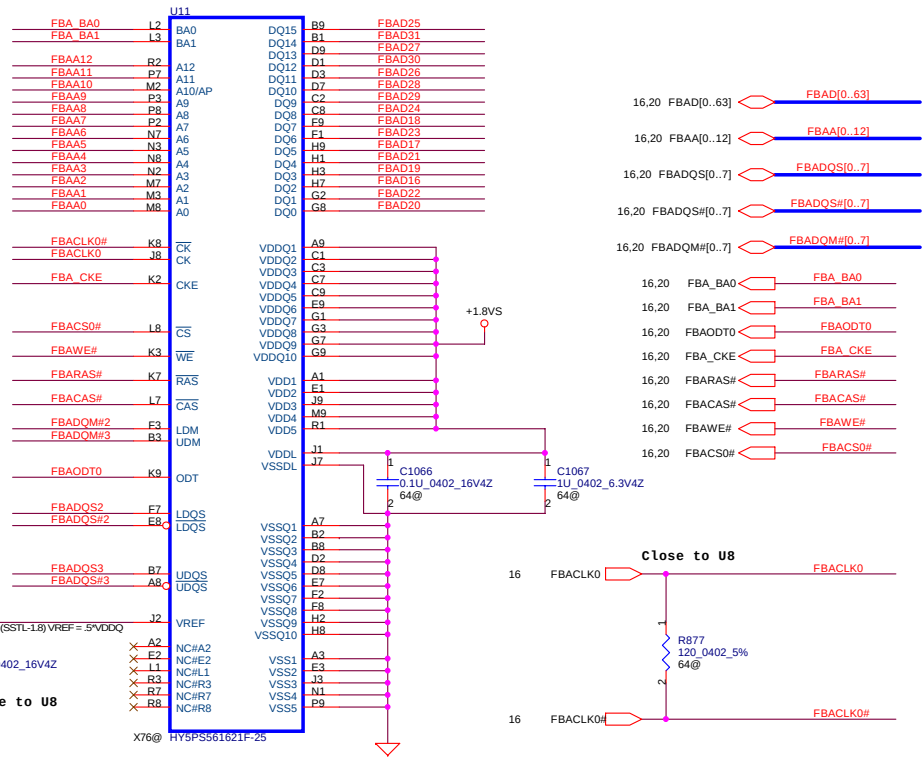
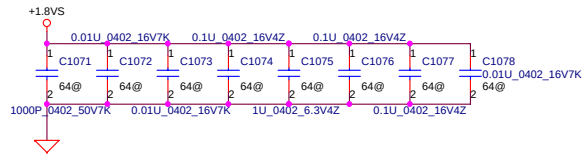
POWER



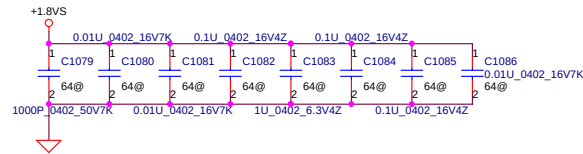
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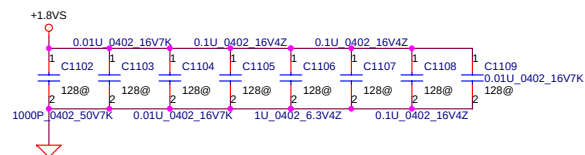
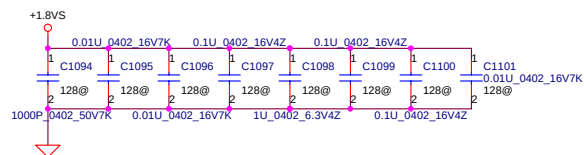
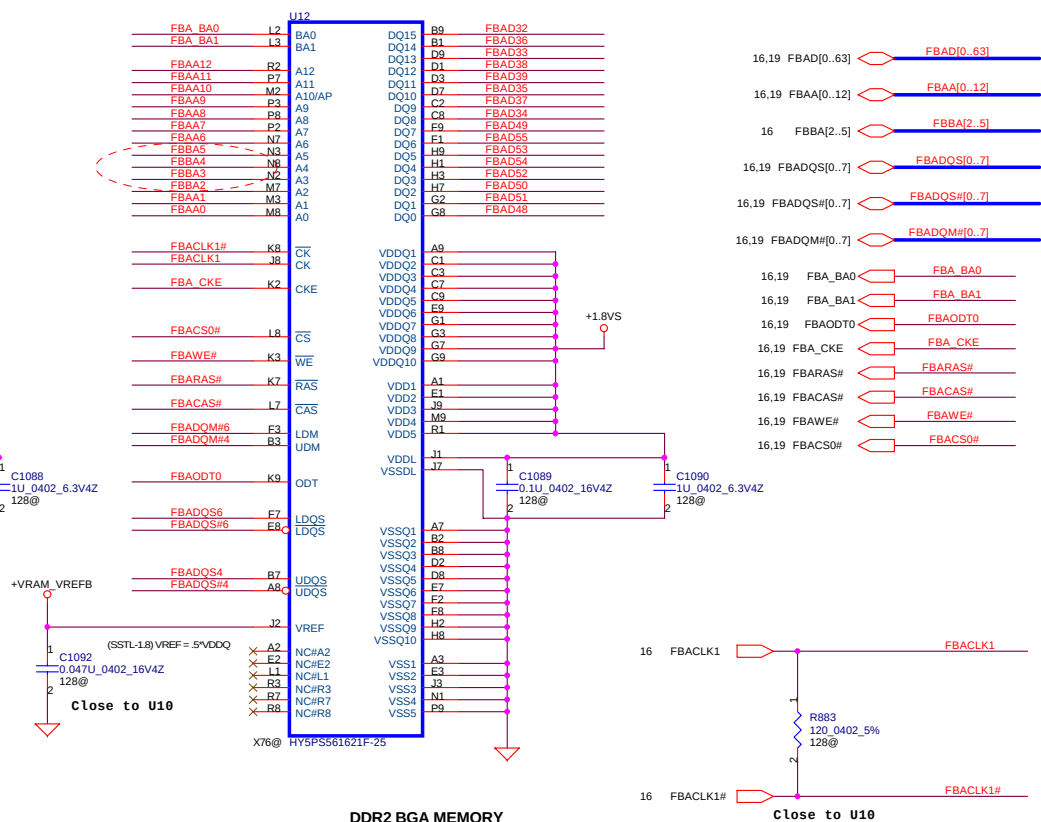
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DDR2 BGA MEMORY

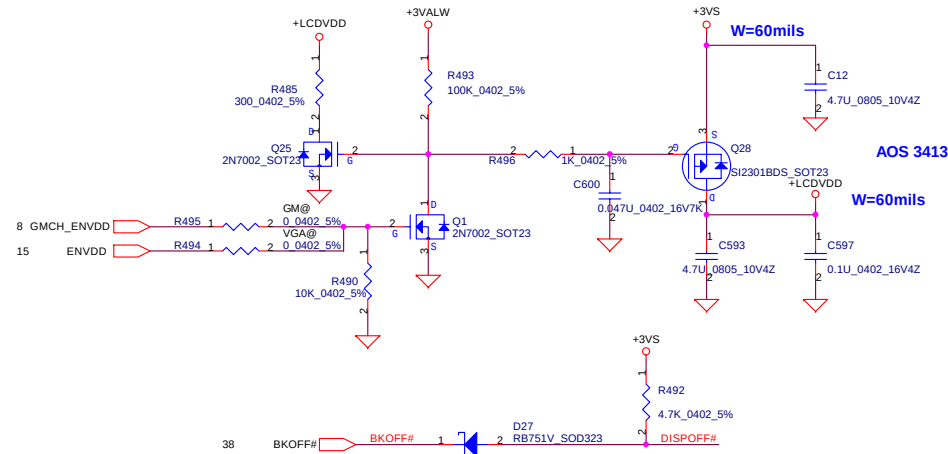


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				Size	Document Number
				Custom	401454
				Date	Rev A
				星期四, 九月 14, 2006	Sheet 19 of 55

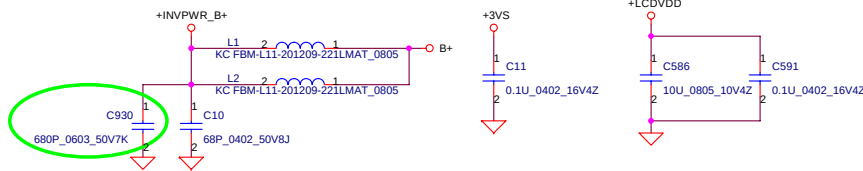
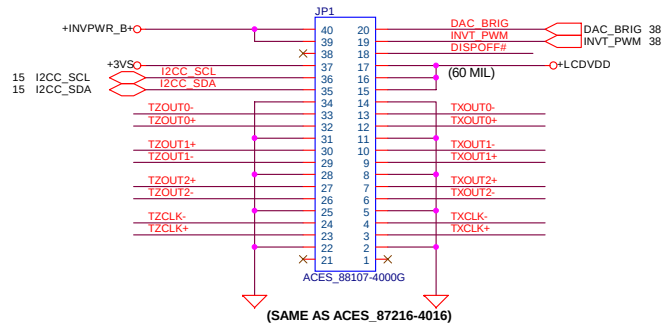
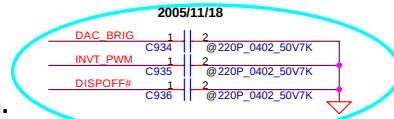


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CUSTOM		401454		Rev A	
Date:		星期日, 九月 14, 2006		Sheet 20 of 55	

LCD POWER CIRCUIT

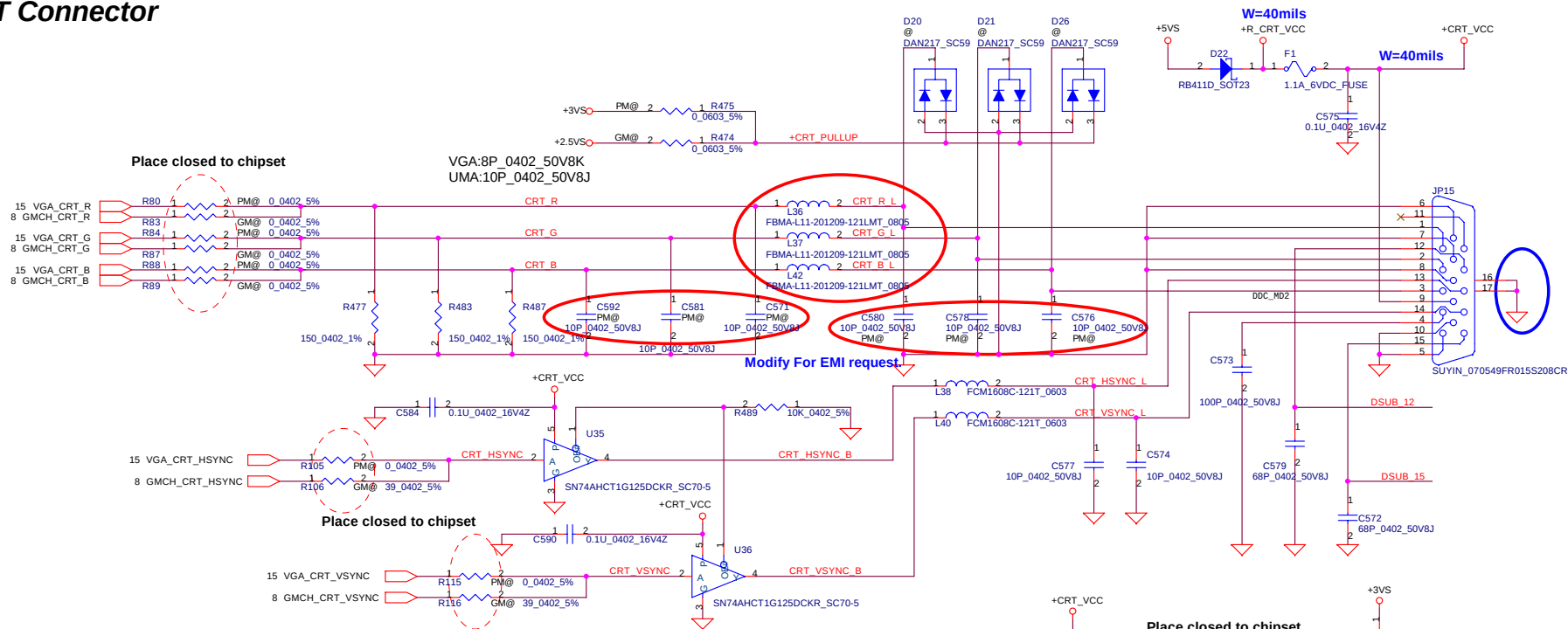


LCD/PANEL BD. Conn.

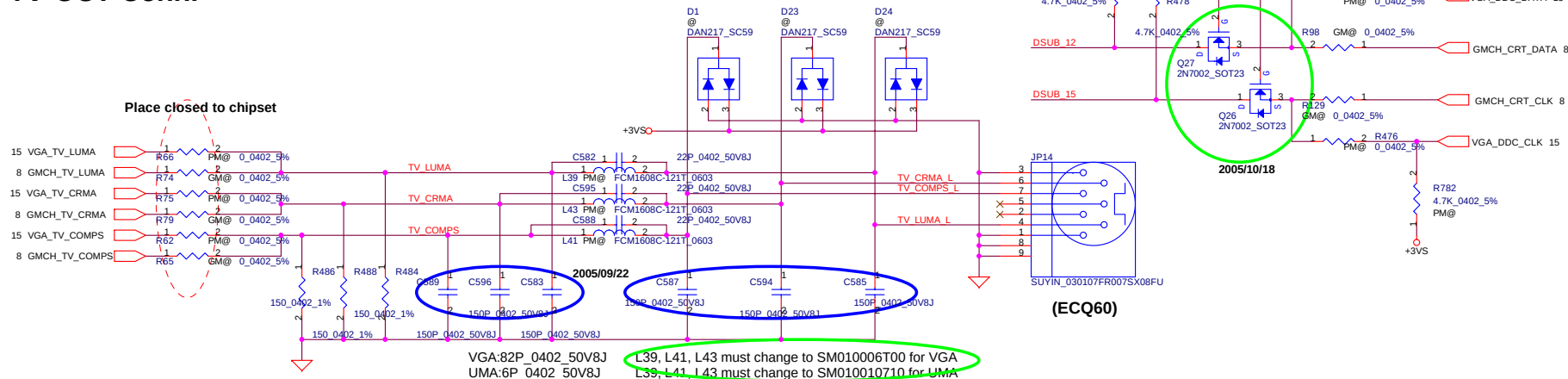


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				401454	
				Date	Rev A
				2006/07/14	2006/07/14
				Sheet 21	of 55

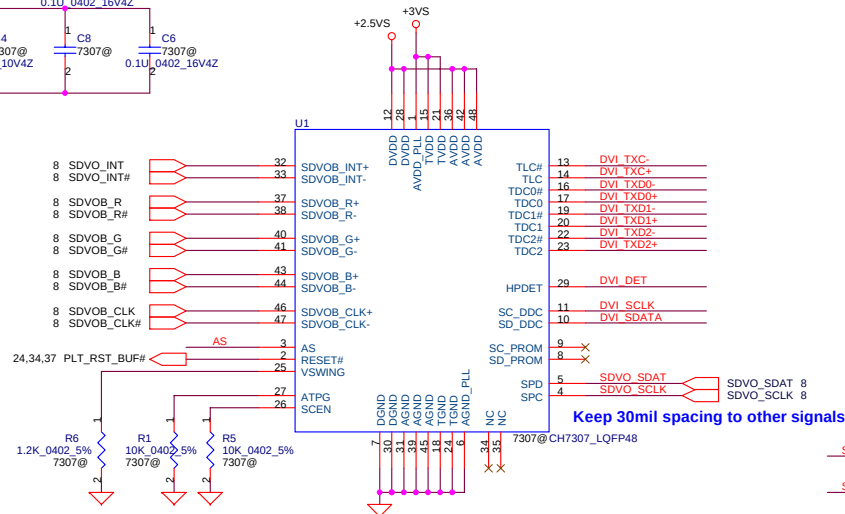
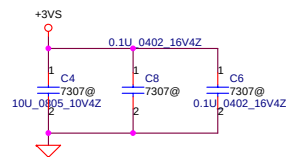
CRT Connector



TV-OUT Conn.

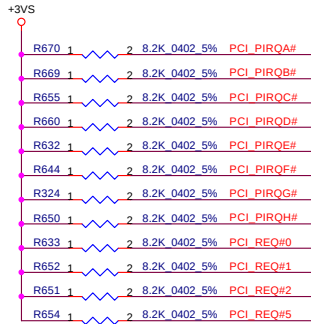
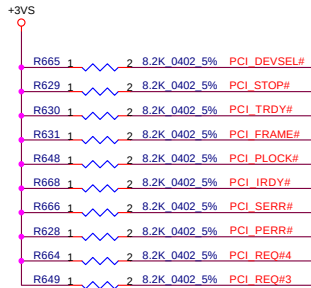


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					401454
				Date	Rev A
				2006/07/14	
				Sheet 22 of 55	

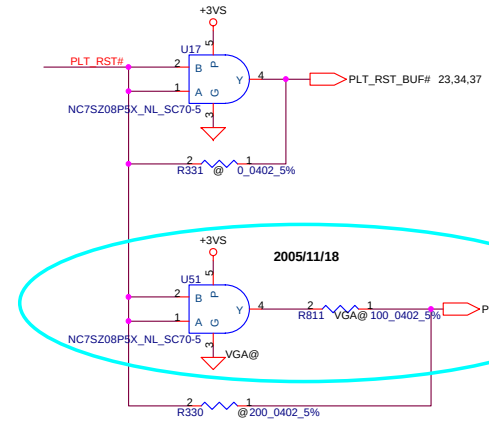
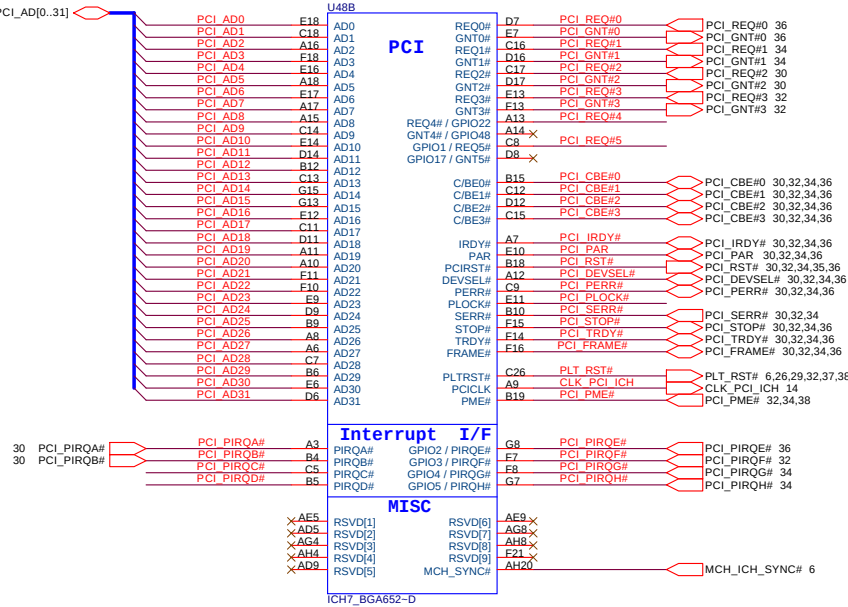


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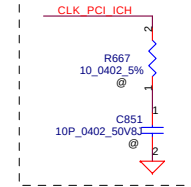
ICH7M(SL8YB) [B-0] : SA00000V190 (AB0!)



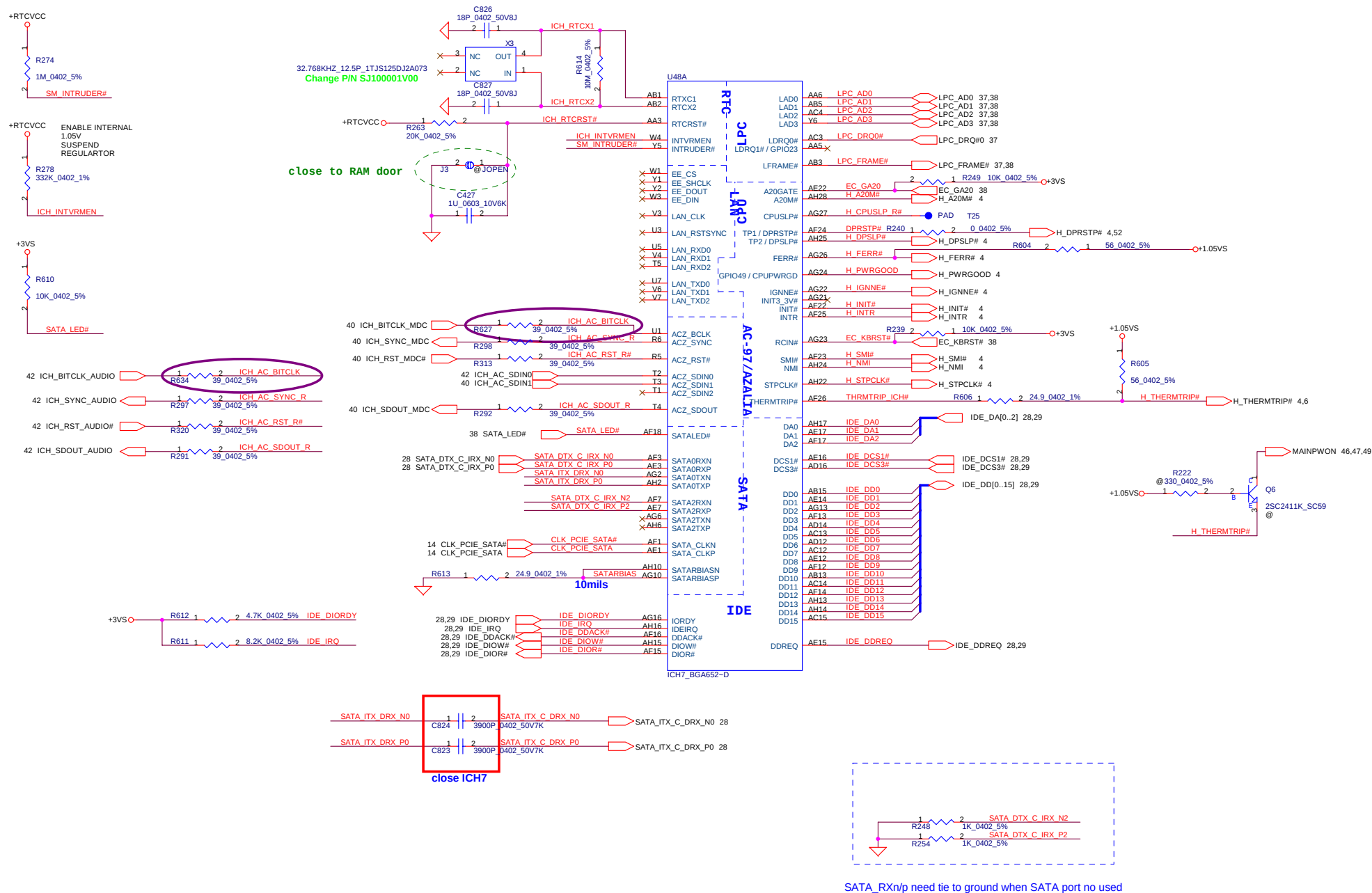
30,32,34,36 PCI_AD[0..31]



Place closely pin A9

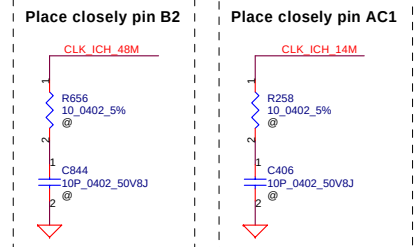
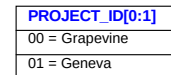


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					401454
				Date	星期四, 九月 14, 2006
				Sheet	24 of 55

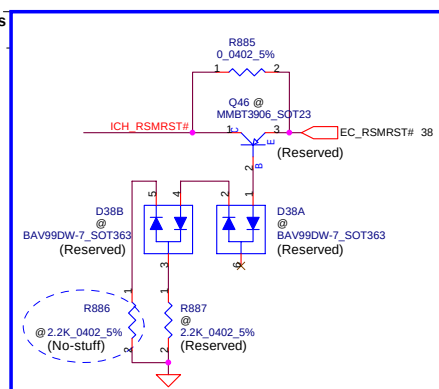
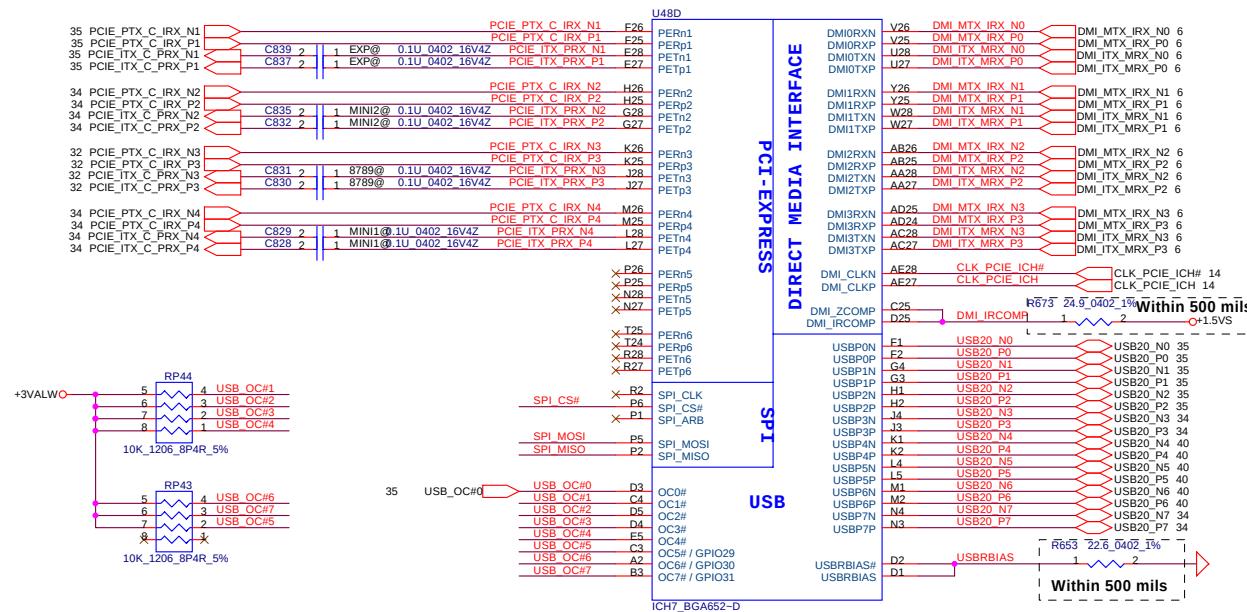
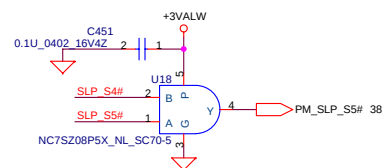


SATA_Rx/n need tie to ground when SATA port no used

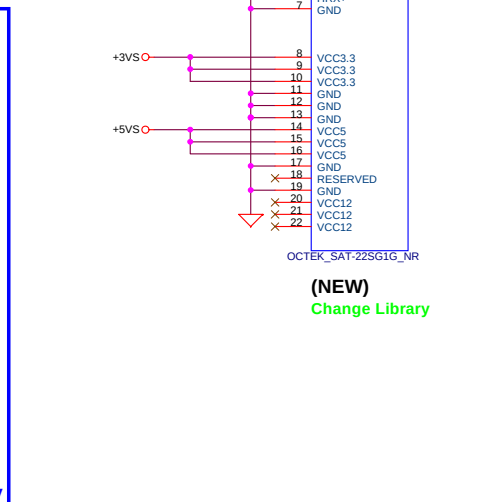
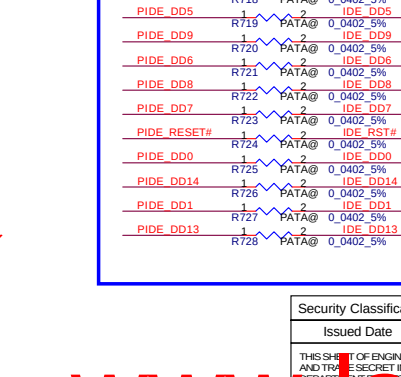
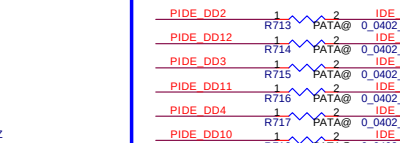
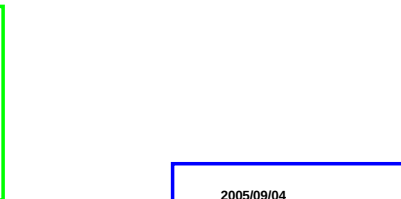
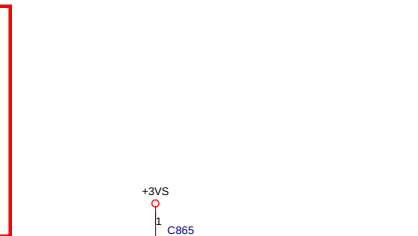
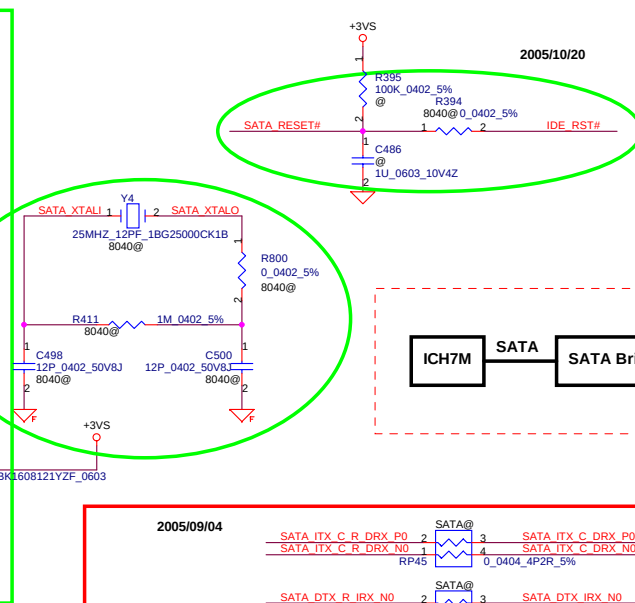
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				Custom	401454
				Date	星期四, 九月 14, 2006
				Sheet	25 of 55



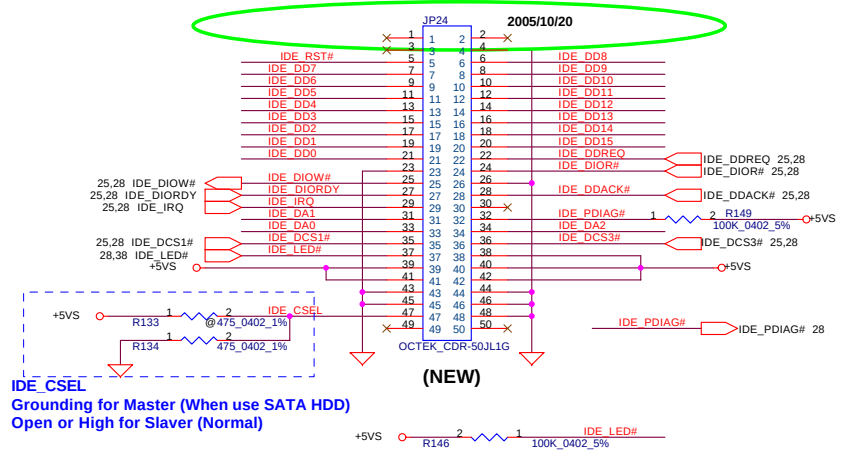
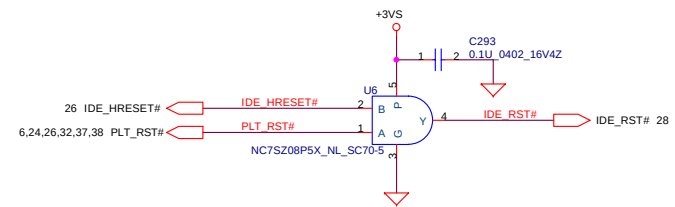
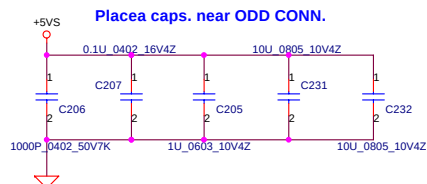
PM_DPRSLPVR : Need to series a 500Ohm resistor to IMVP6



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				Custom	401454
Date: 星期日, 九月 14, 2006				Sheet	26 of 55



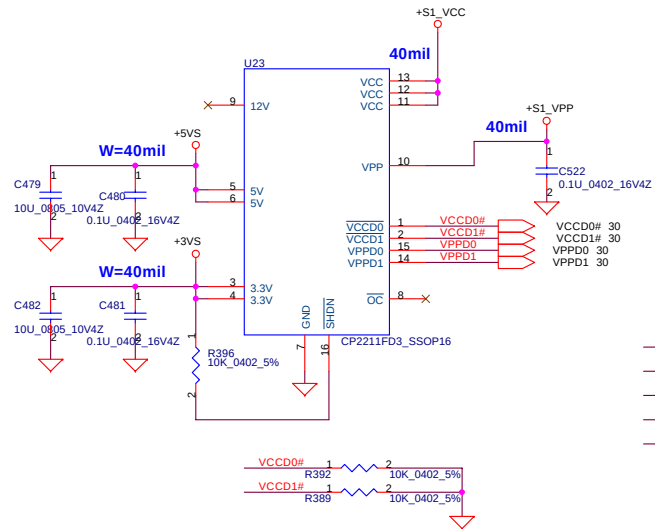
AND TRUE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DEPARTMENT OR OFFICE. IT IS TO BE KEPT IN THE OFFICE OF THE COMPETENT DEPARTMENT OR OFFICE. IT MAY BE USED BY OR FOR THE COMPETENT DEPARTMENT OR OFFICE ONLY. IT MAY NOT BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT THE WRITTEN CONSENT OF THE COMPETENT DEPARTMENT OR OFFICE.



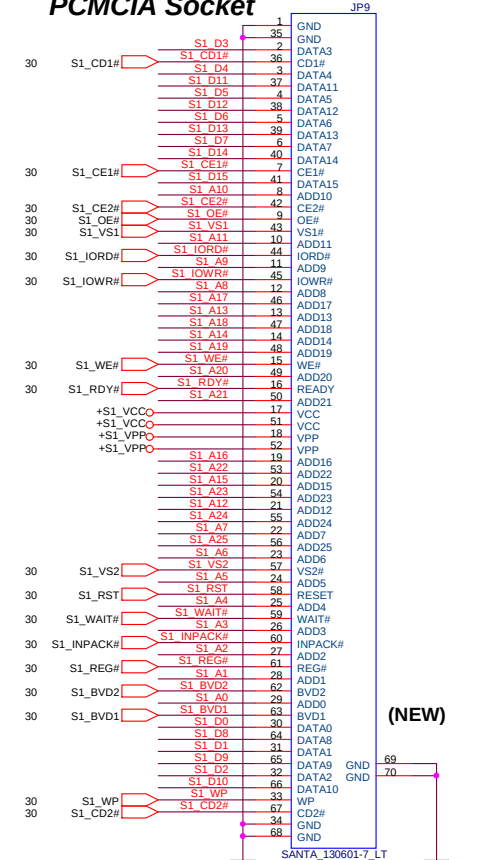
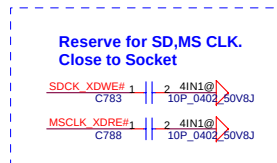
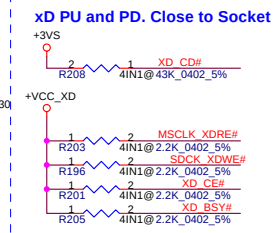
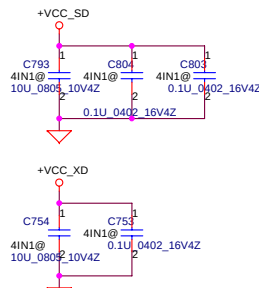
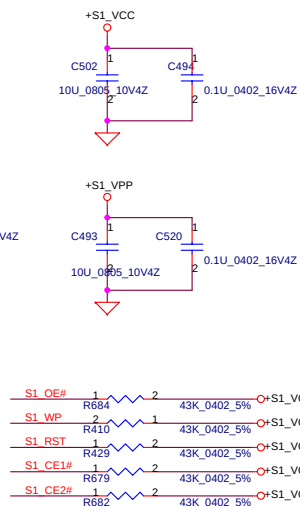
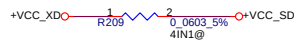
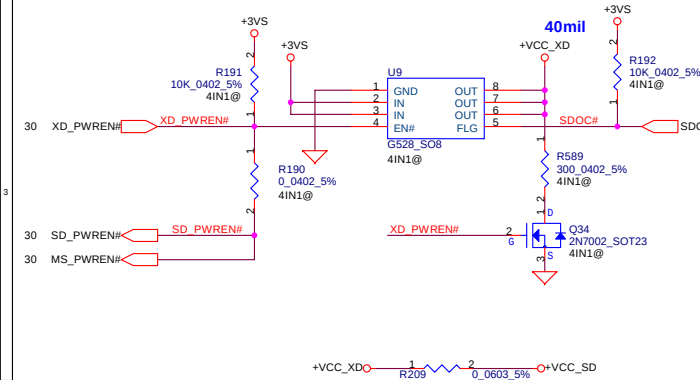
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Size B		Document Number		401454		Rev A			
Date:		星期四, 九月 14, 2006		Sheet 29		of 55			

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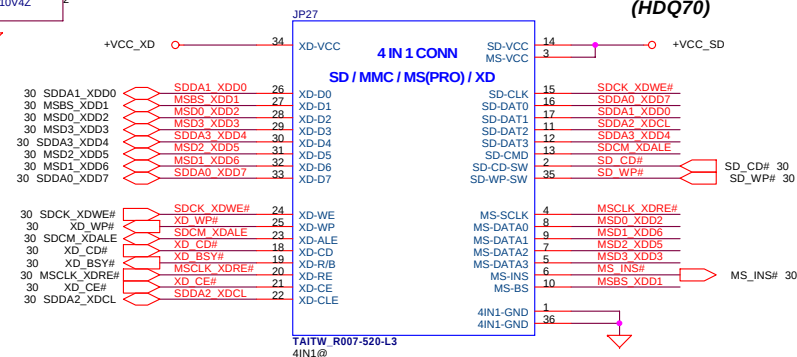
PCMCIA Power Control



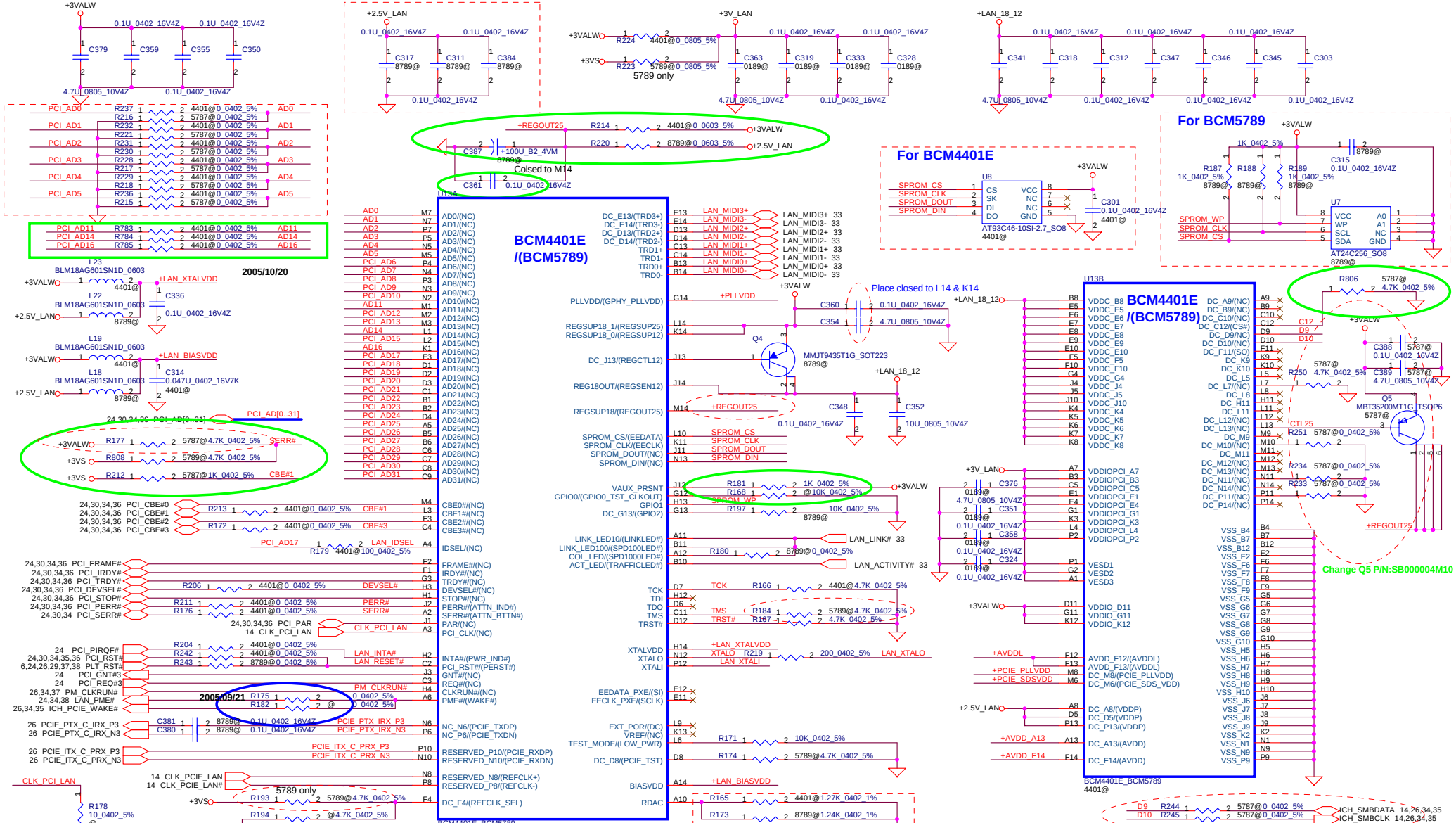
SD/MS Power Control
XD Power Control



4 IN 1 Socket
(HDQ70)



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					401454
				Date:	星期四, 九月 14, 2006
				Sheet	31 of 55



(SA000000D10) (SA000000S200) (SA000000YJ00)			
PN	4401E(10/100 LAN)	5789(10/100/1000 LAN)	5787(10/100/1000 LAN)
RDAC	1.27K	1.24K	1.24K

BOM structure	4401E(10/100 LAN)	5789(10/100/1000 LAN)	5787(10/100/1000 LAN)
4401@	Stuff	No_Stuff	No_Stuff
5789@	No_Stuff	Stuff	No_Stuff
5787@	No_Stuff	No_Stuff	Stuff
8789@	No_Stuff	Stuff	Stuff
@	No_Stuff	No_Stuff	No_Stuff

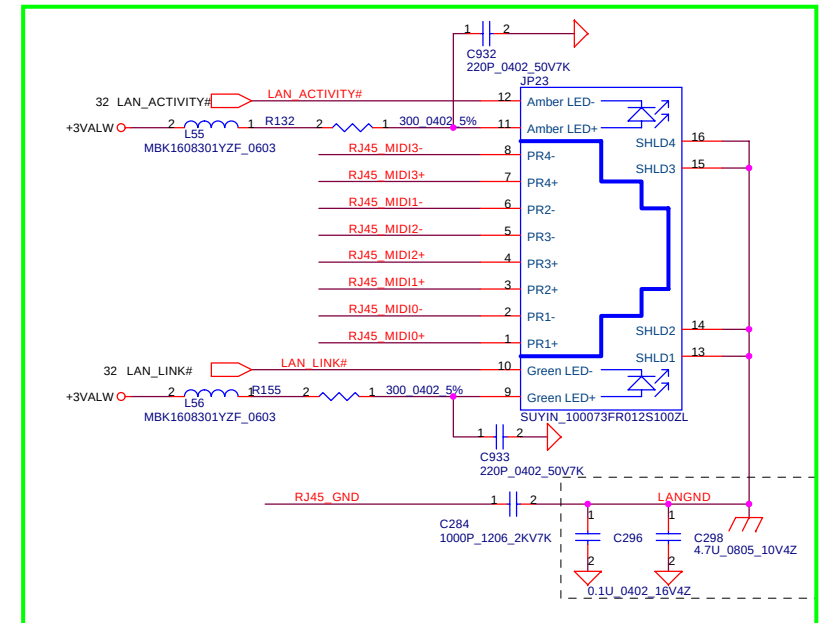
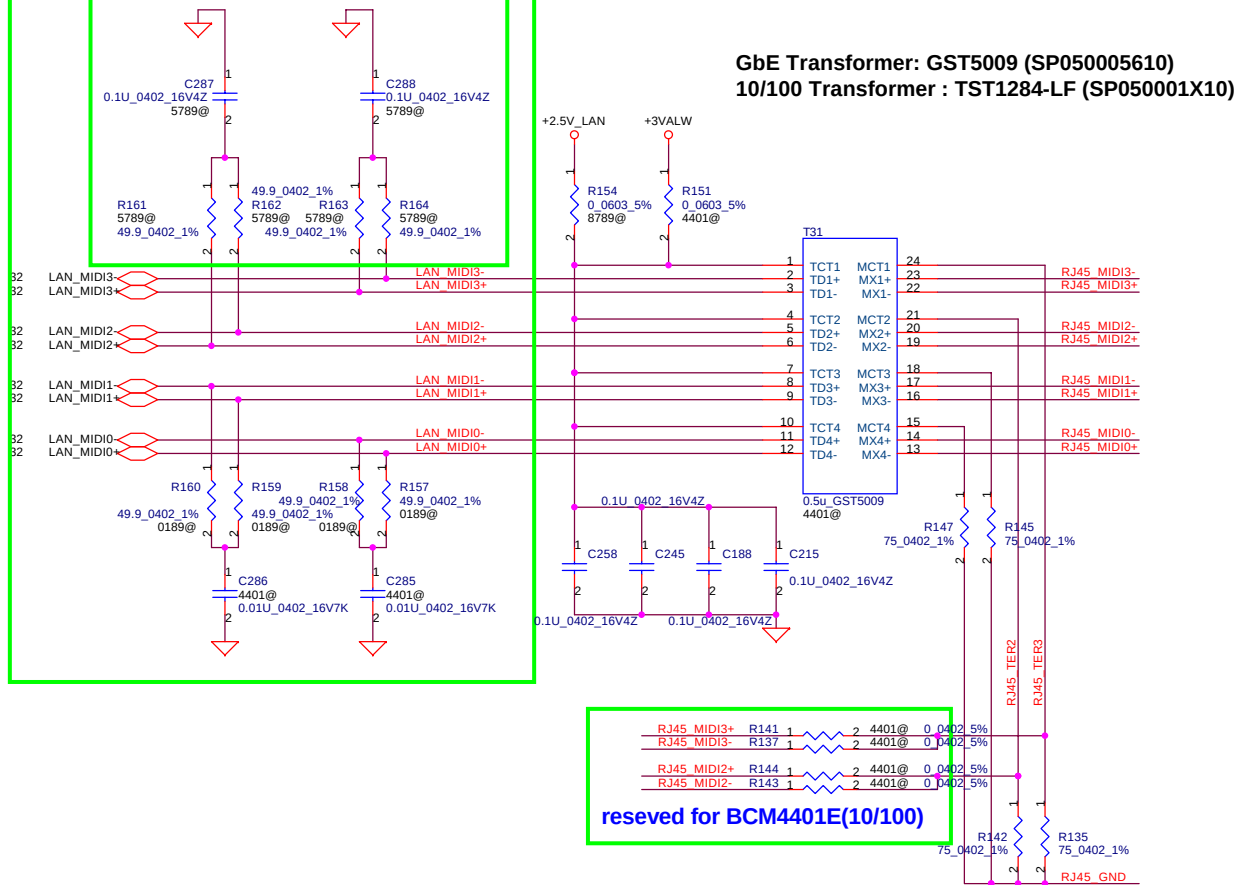
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SCHEMATIC, M/B LA-2922P			
Size	Document Number	Rev	
B	401454	A	
Date:	星期四, 九月 14, 2006	Sheet	32 of 55

LAN BCM4401E/ BCM5789

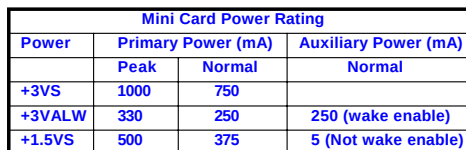
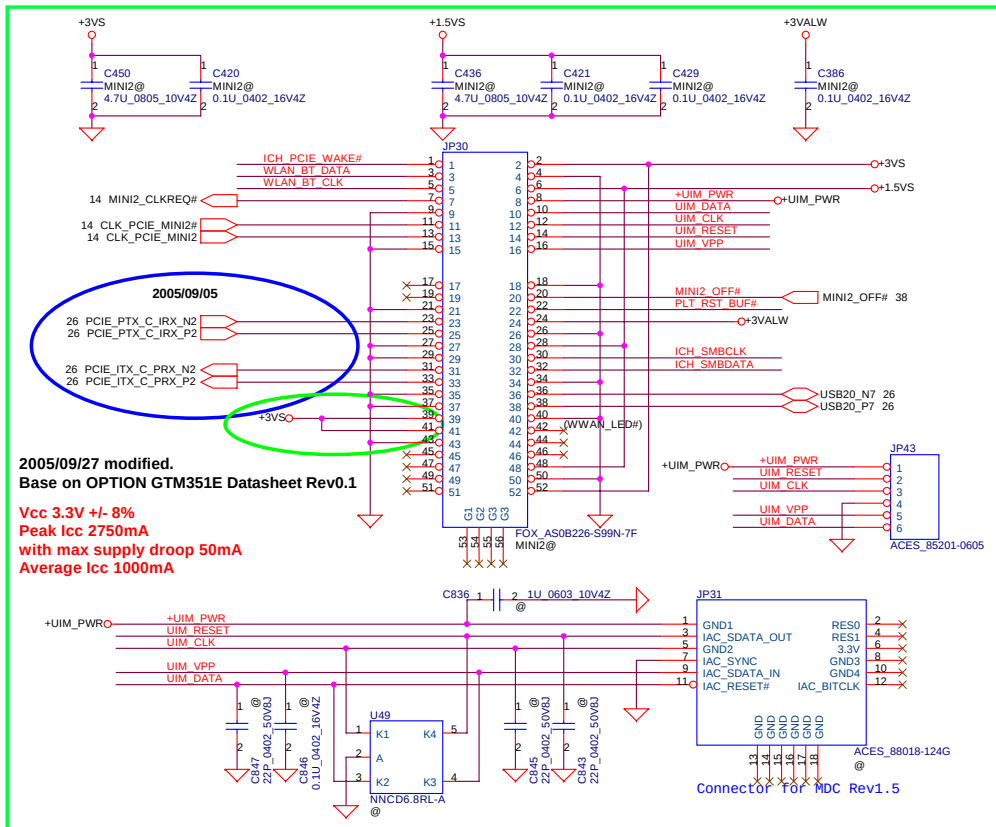
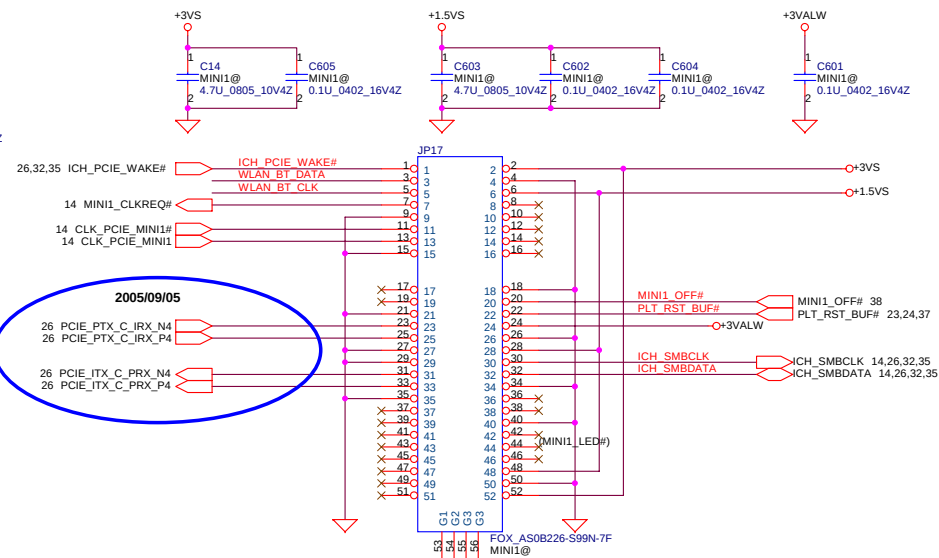
Place these components colsed to LAN chip

unpop when use BCM4401E(10/100)



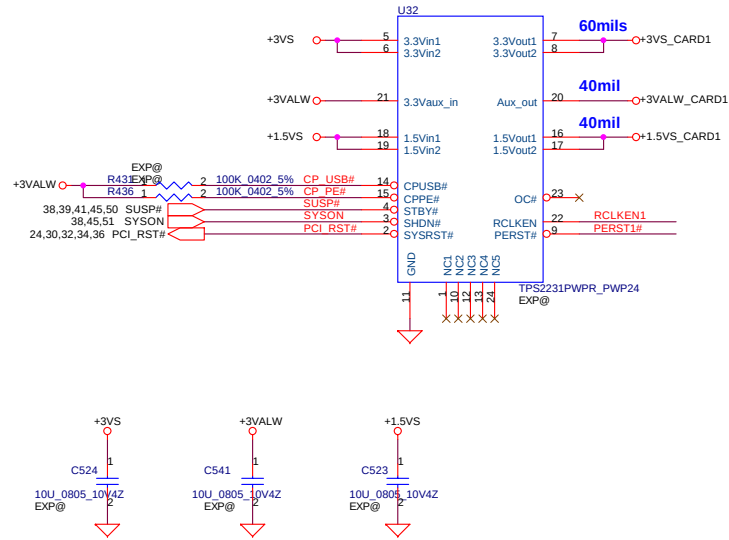
reserved for BCM4401E(10/100)

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					401454	
				Date:	星期四, 九月 14, 2006	Sheet 33 of 55

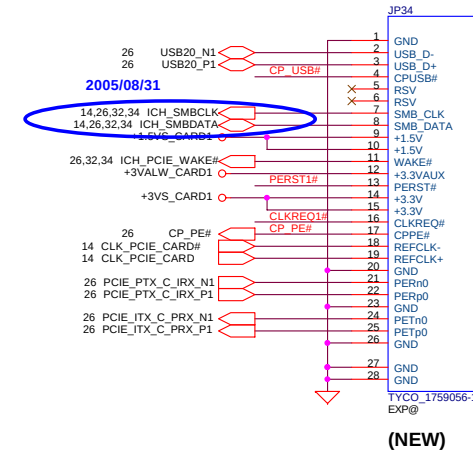


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				Date: 星期四, 九月 14, 2006	Sheet 34 of 55

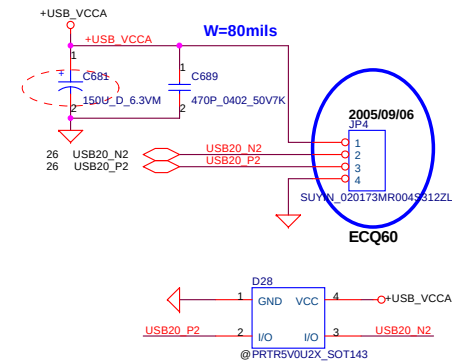
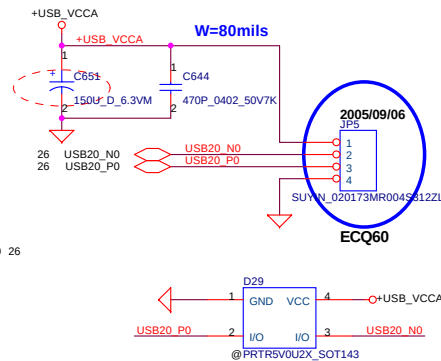
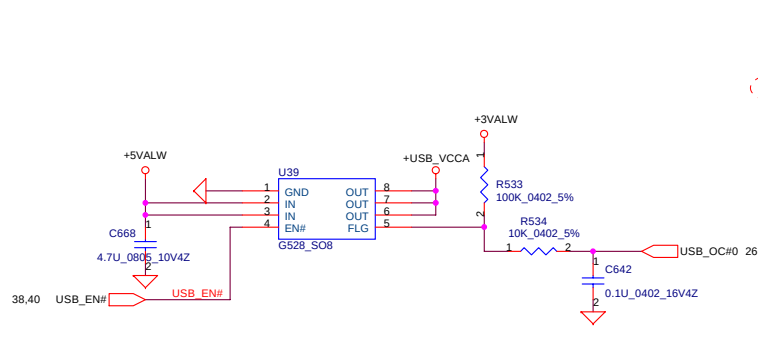
New Card Power Switch



New Card Socket (Left)



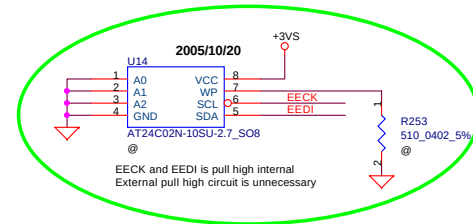
USB CONN. 1 & 2



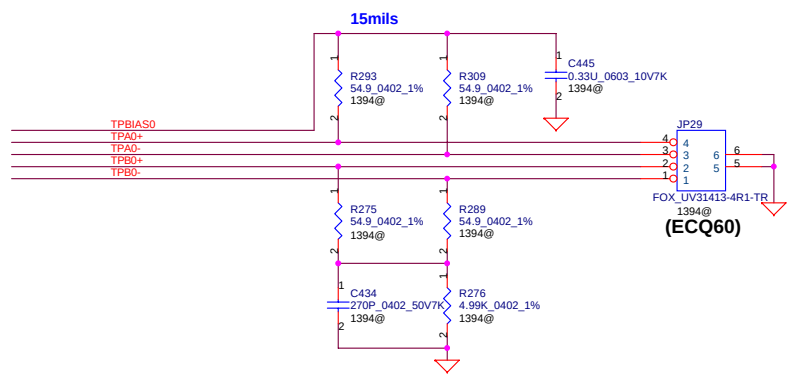
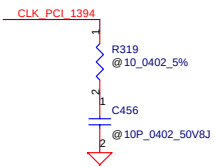
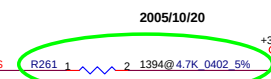
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Size	B	Document Number	401454	Rev	
Date	星期四, 九月 14, 2006	Sheet	35 of 55		

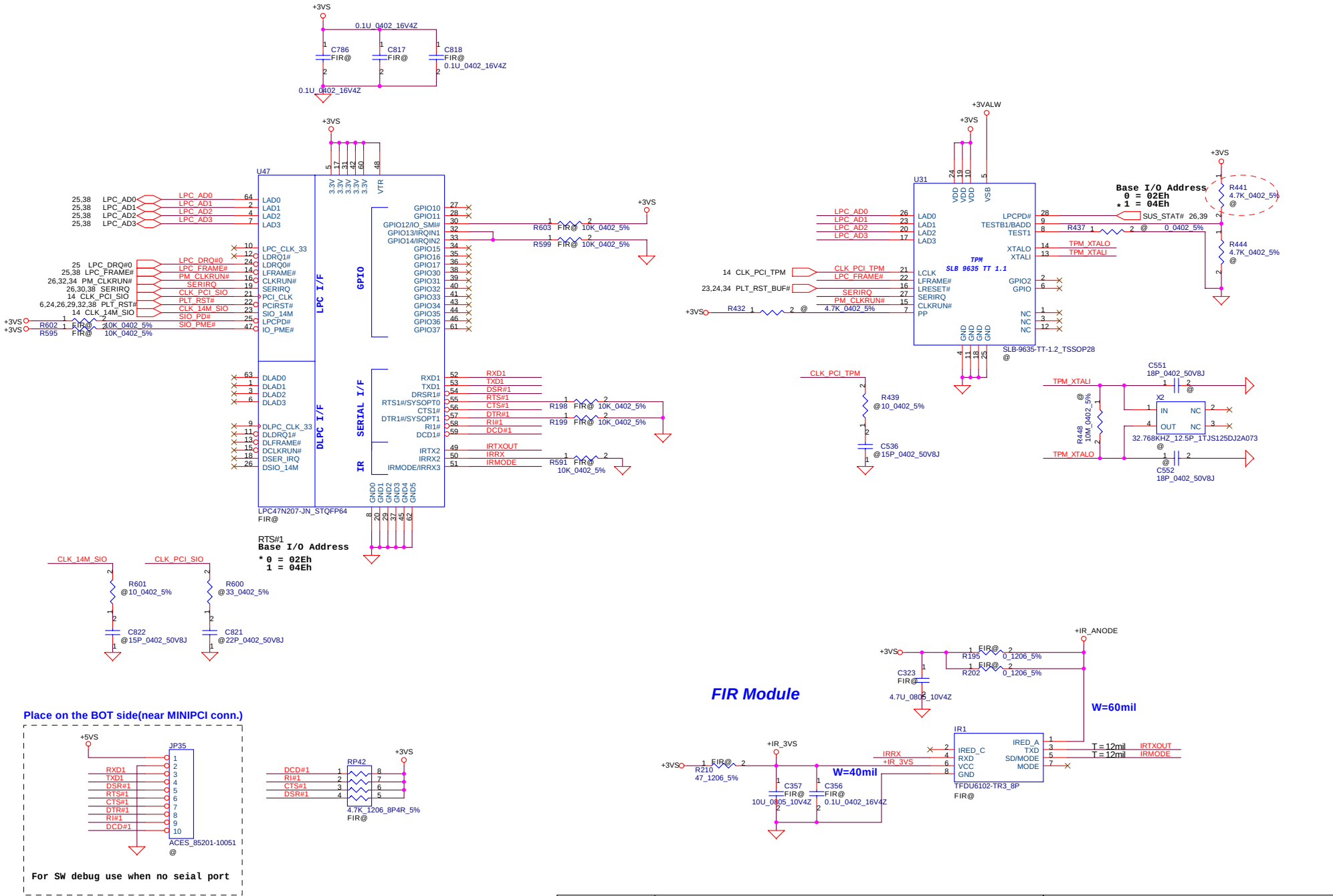


**When use external BJT
Populate Q35, R279**

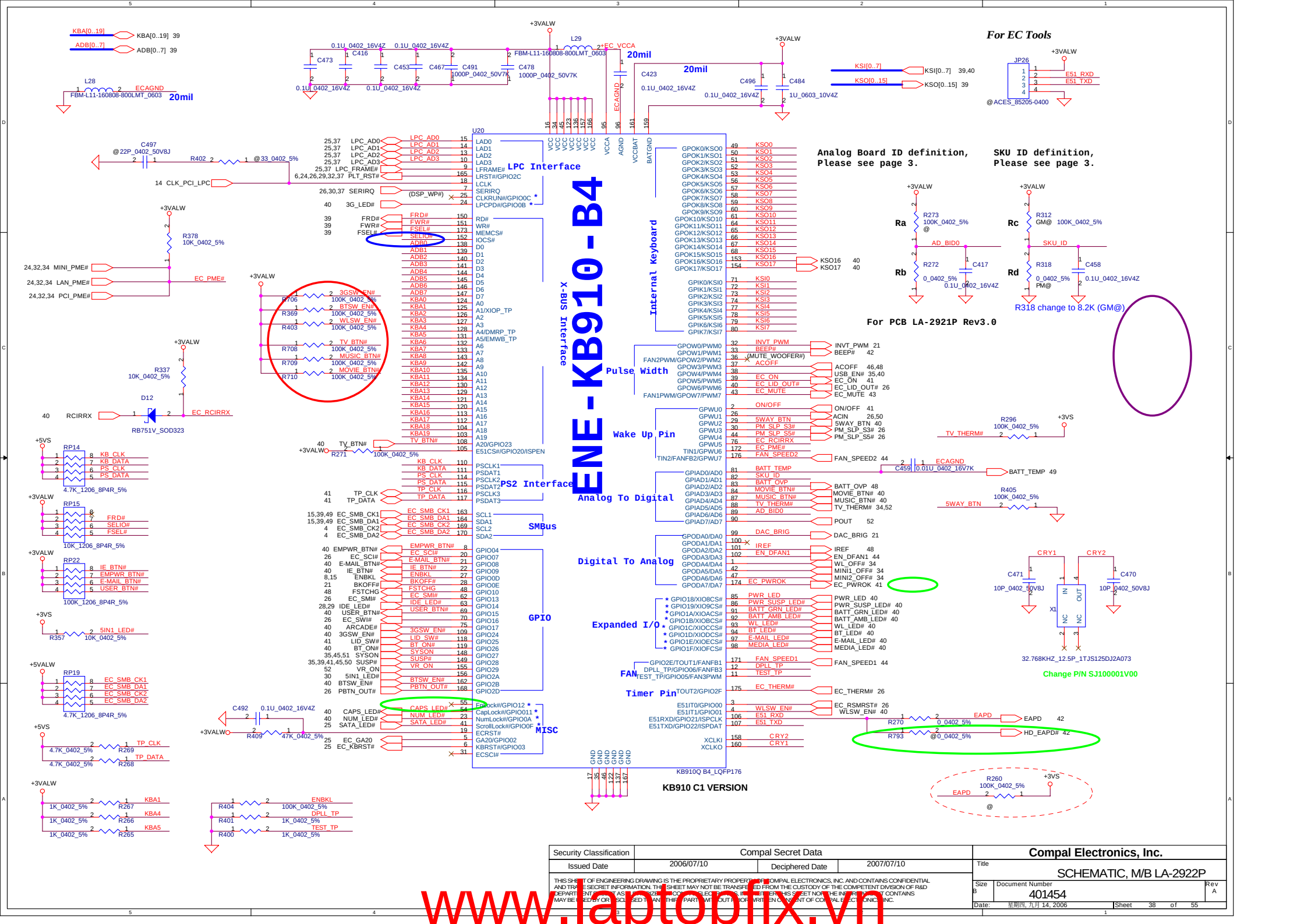


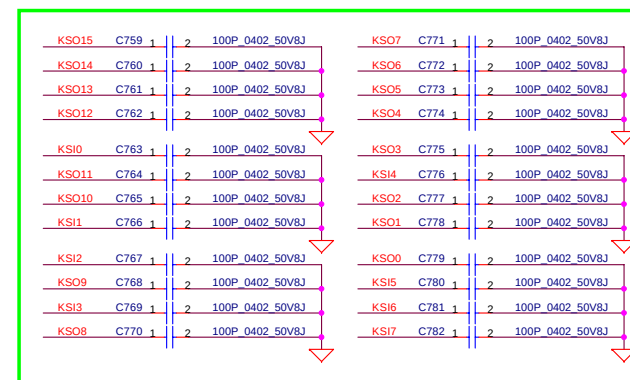
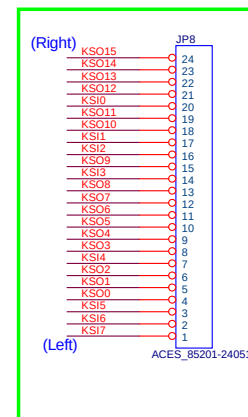
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				Size B	Document Number	Rev A
				401454		
Date:				星期四, 九月 14, 2006	Sheet 36 of 55	

SUPER I/O SMsC LPC47N207



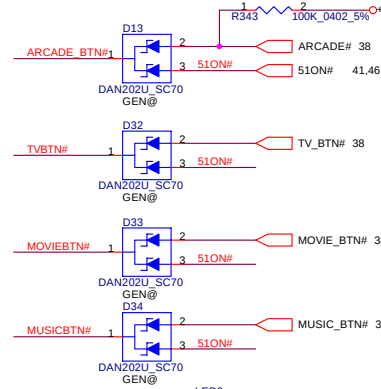
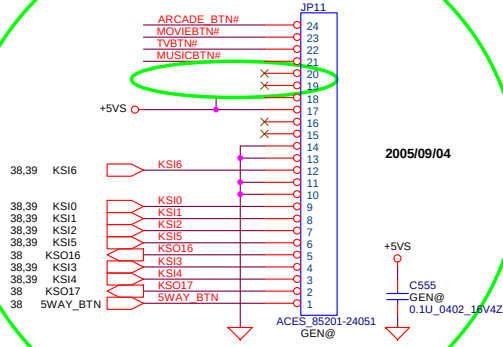
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Size	Document Number	Rev		
B	401454	A		
Date	星期四, 九月 14, 2006	Sheet	37	of 55



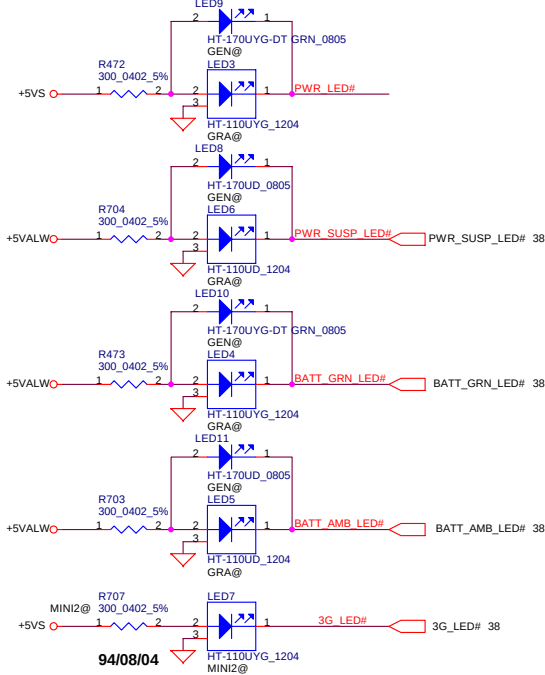
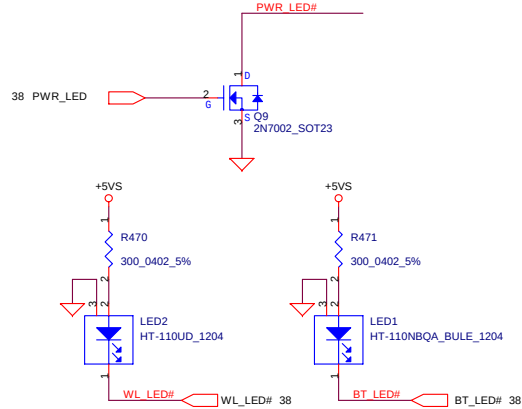
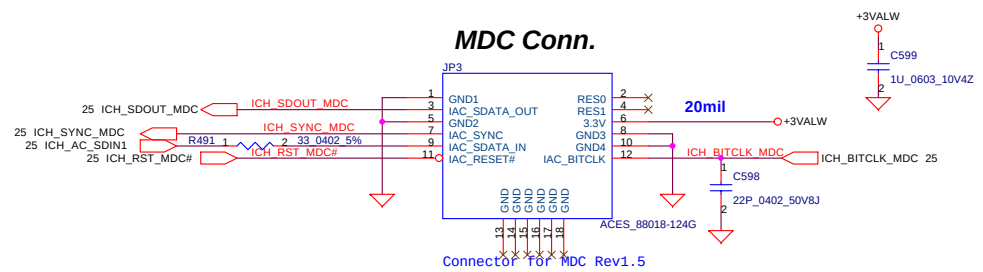


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						Size	Document Number		Rev. A
						401454			
Date		星期四, 九月 14, 2006		Sheet	39 of 55				

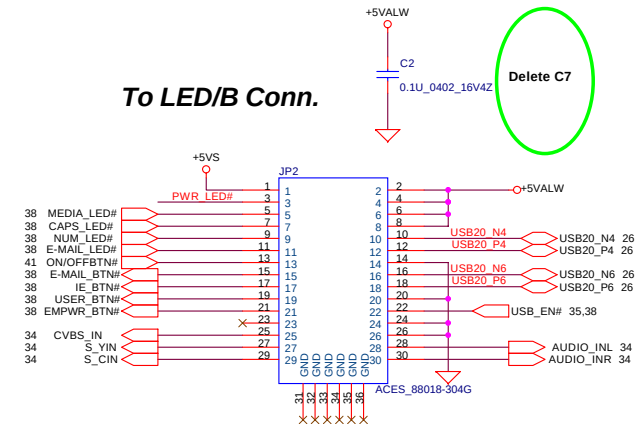
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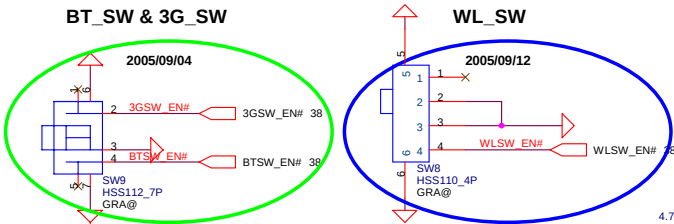
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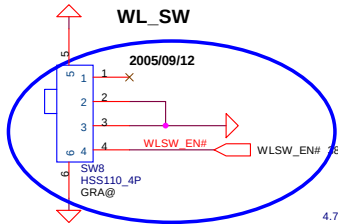
To LED/B Conn.



BT_SW & 3G_SW

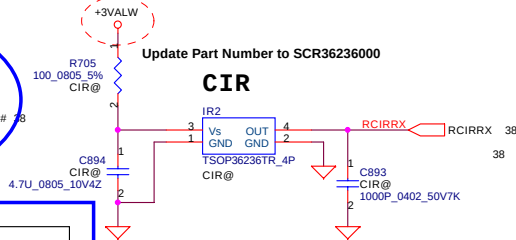


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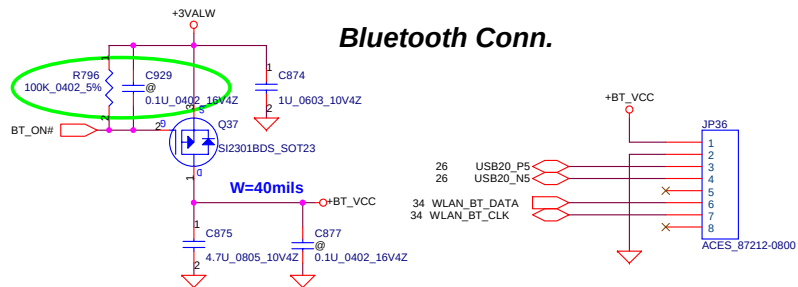


Update Part Number to SCR36236000

CIR



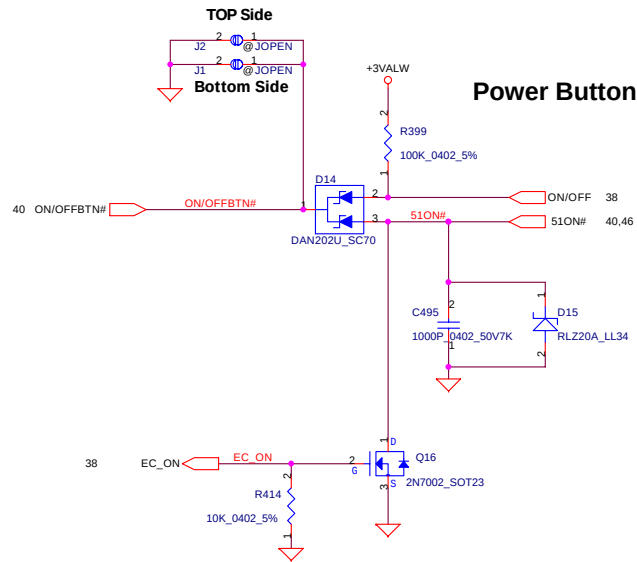
Bluetooth Conn.



Geneva		Grapevine	
KSO16	KSO17	KSO16	KSO17
KSI0	VOL_UP	KSI2	PLAY
KSI1	RIGHT	KSI3	STOP
KSI2	PLAY	KSI4	NEXT
KSI3	STOP	KSI5	REV
KSI4	NEXT		
KSI5	REV		
KSI6	RECORD		

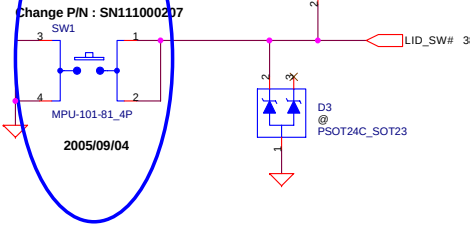
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				Date: 星期四, 九月 14, 2006	Sheet 40 of 55

ON/OFF switch

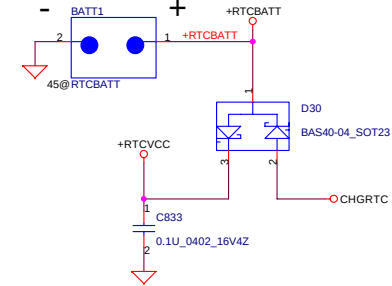


Power Button

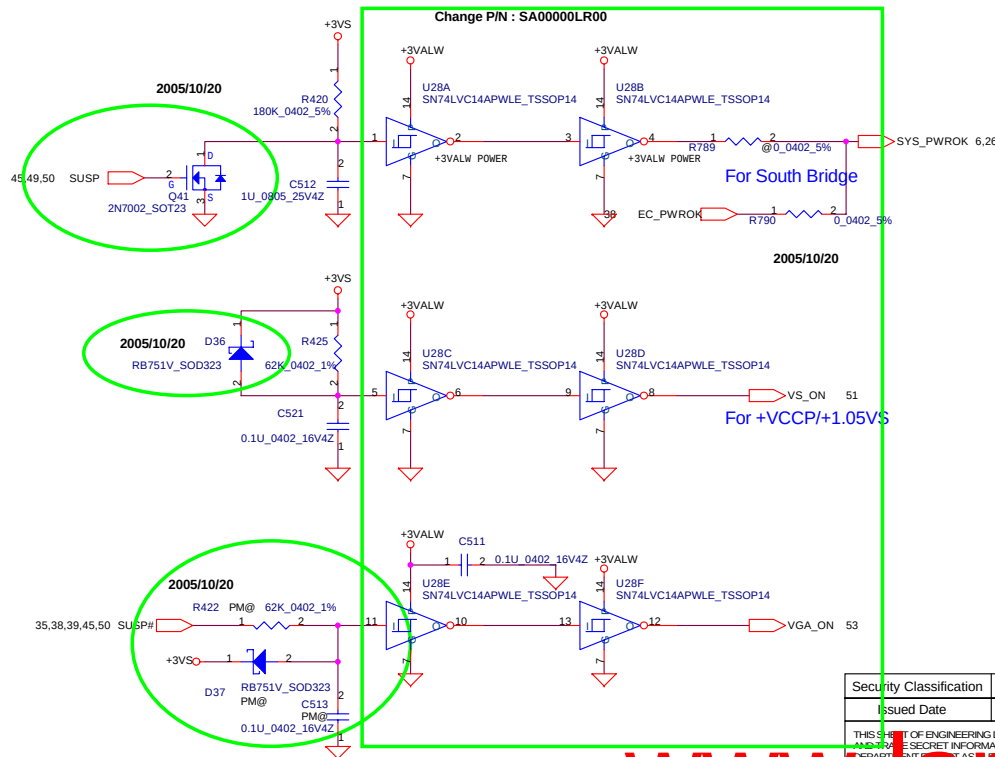
Lid Switch



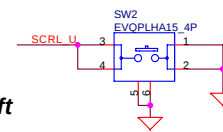
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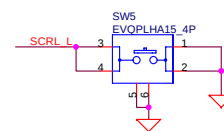
Power ON Circuit



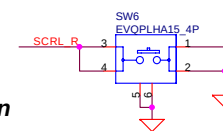
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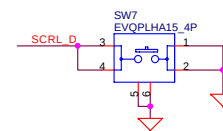
Scroll Left



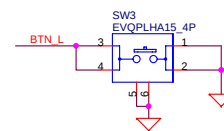
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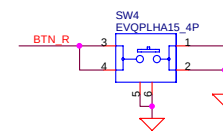
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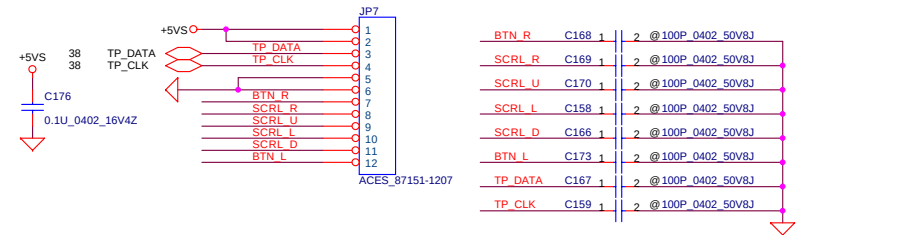
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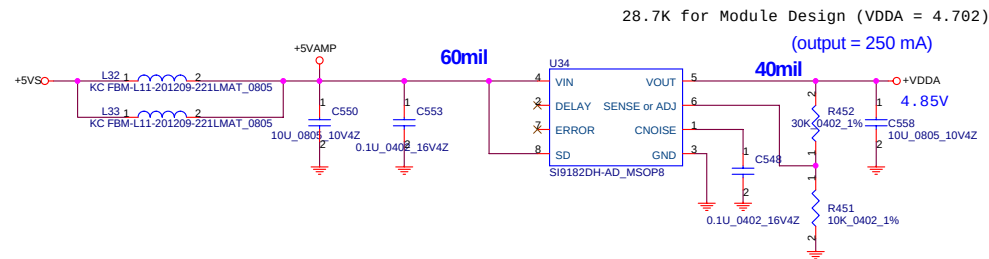
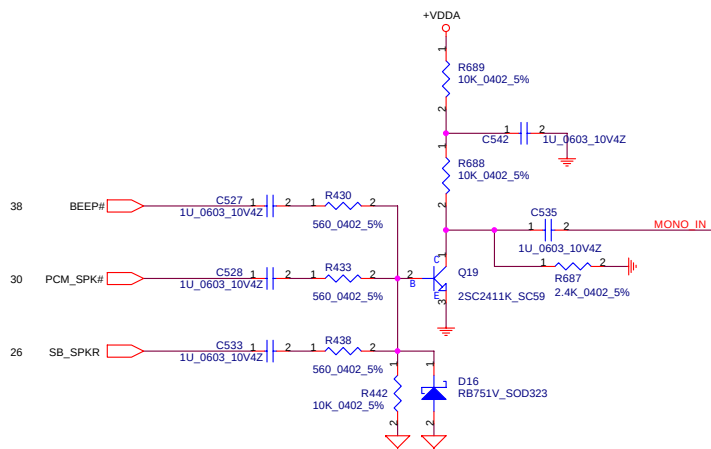
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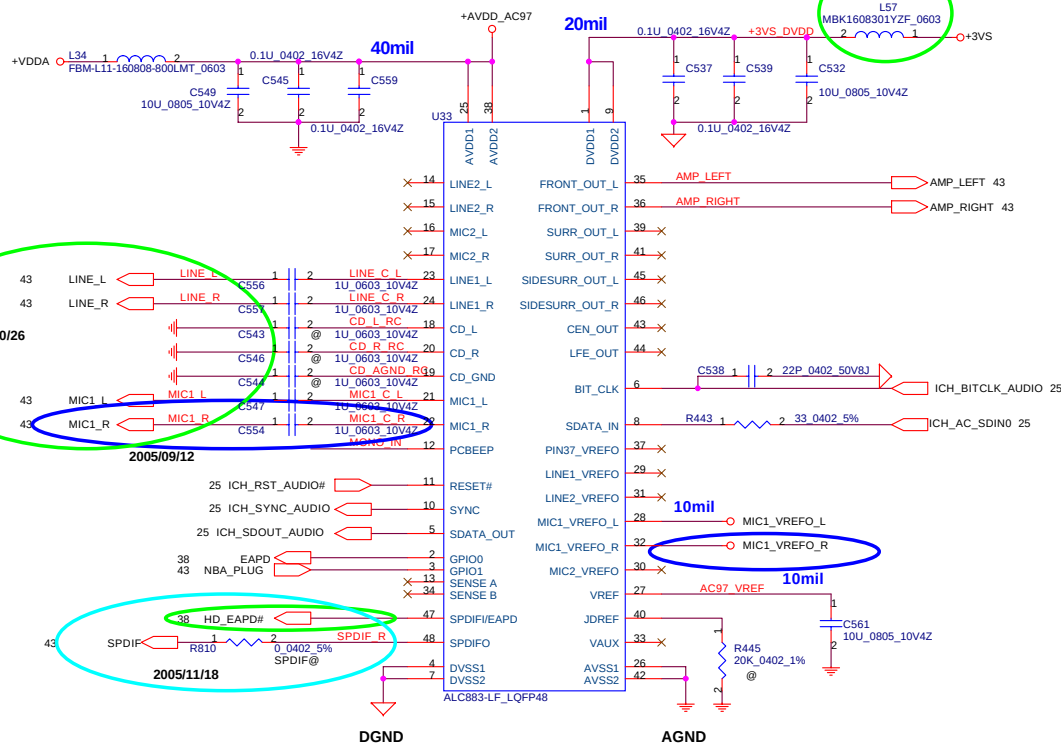
To TP/B Conn.



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					401454
				Date	Rev A
				2006/09/14	
				Sheet 41 of 55	



HD Audio Codec

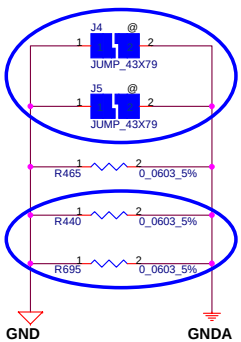


2005/10/26

2005/09/12

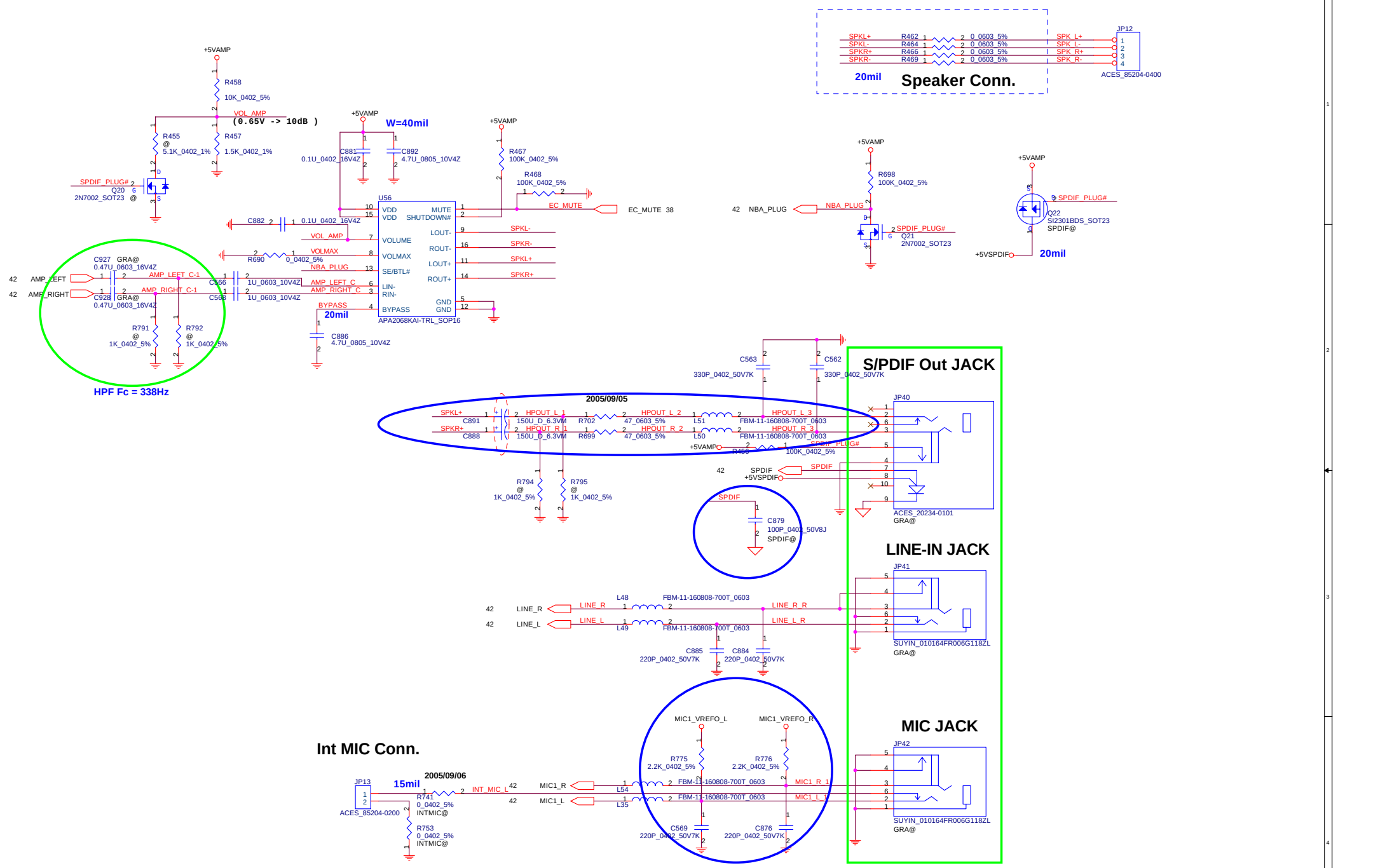
2005/11/18

2005/09/20



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Size B	Document Number	401454		Rev A	
Date:	星期四, 九月 14, 2006	Sheet	42	of	55

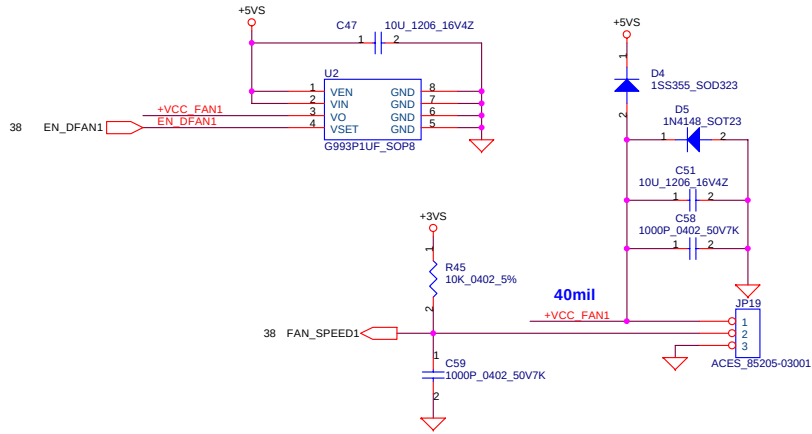
www.laptopfix.vn



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					401454
				Date	Rev A
				2006/07/14	
				Sheet	43 of 55

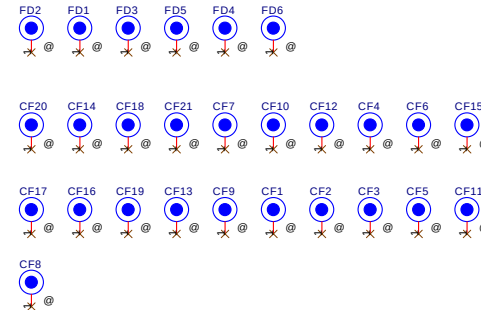
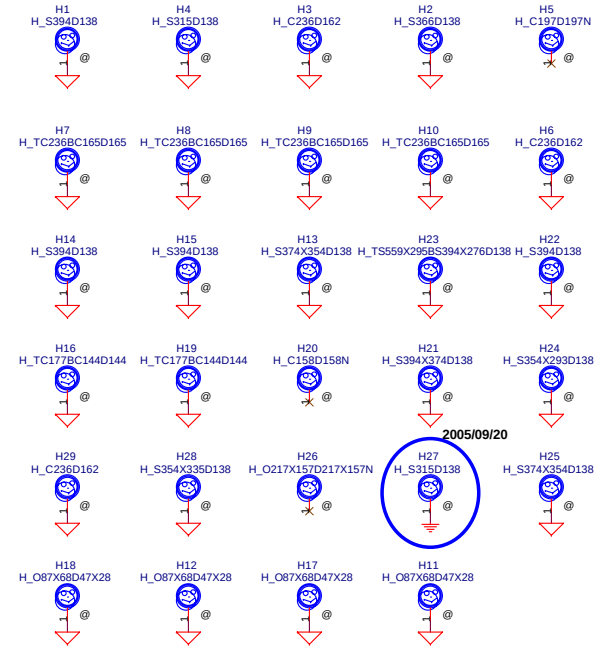
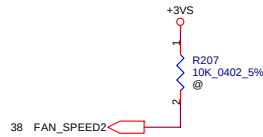
www.laptopfix.vn

FAN1 Conn



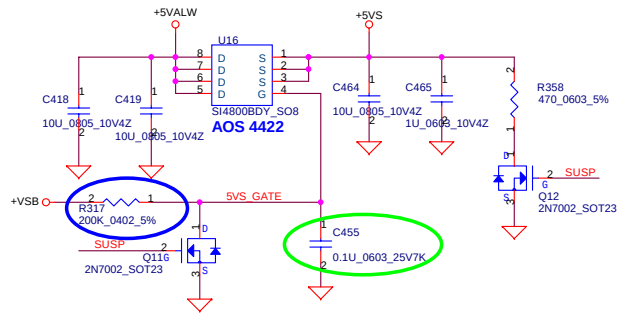
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2005/12/29: Remove 2nd FAN support components

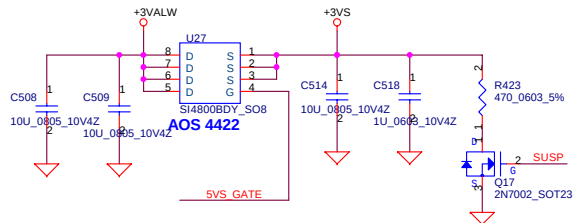


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				B	401454
				Date:	Rev A
				星期四, 九月 14, 2006	Sheet 44 of 55

+5VALW TO +5VS

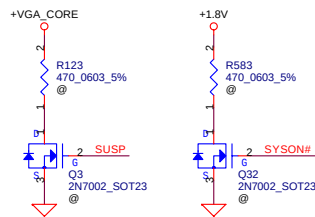
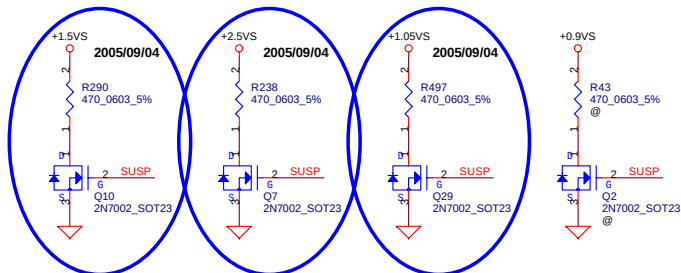
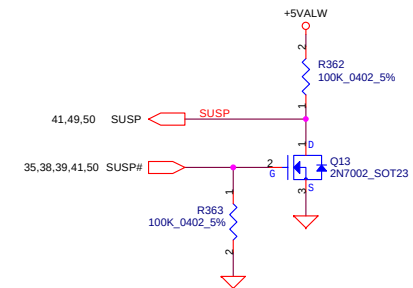
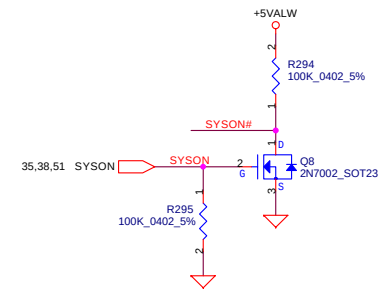
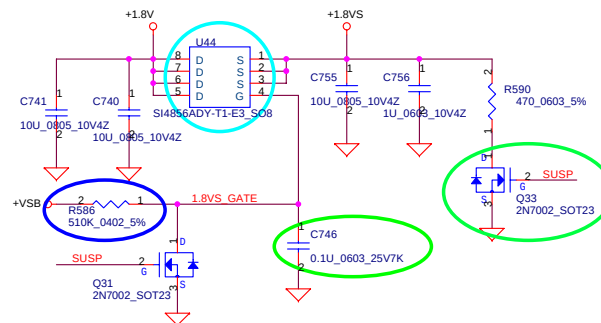


+3VALW TO +3VS

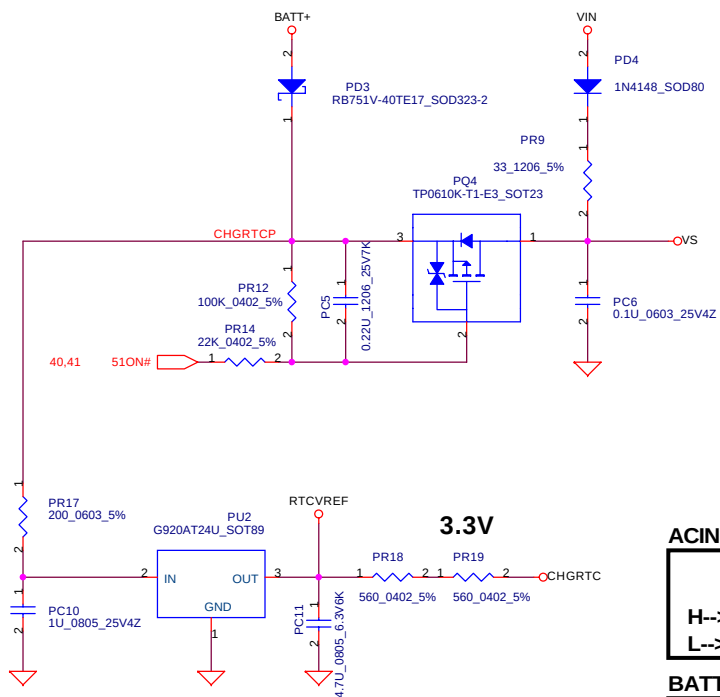
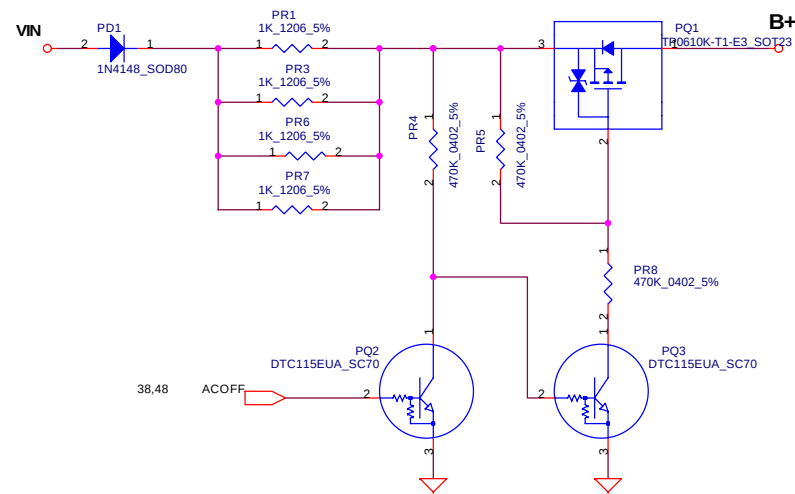
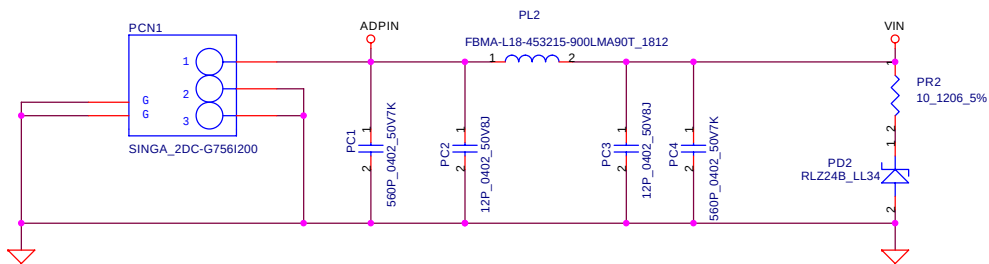


2005/12/18
Change P/N : SB000001Y00(New) SI4856ADY
SB548000310(Old)

+1.8V to +1.8VS



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				Size B	Document Number	REV A
				401454		
Date: 星期四, 九月 14, 2006				Sheet	45 of 55	



ACIN

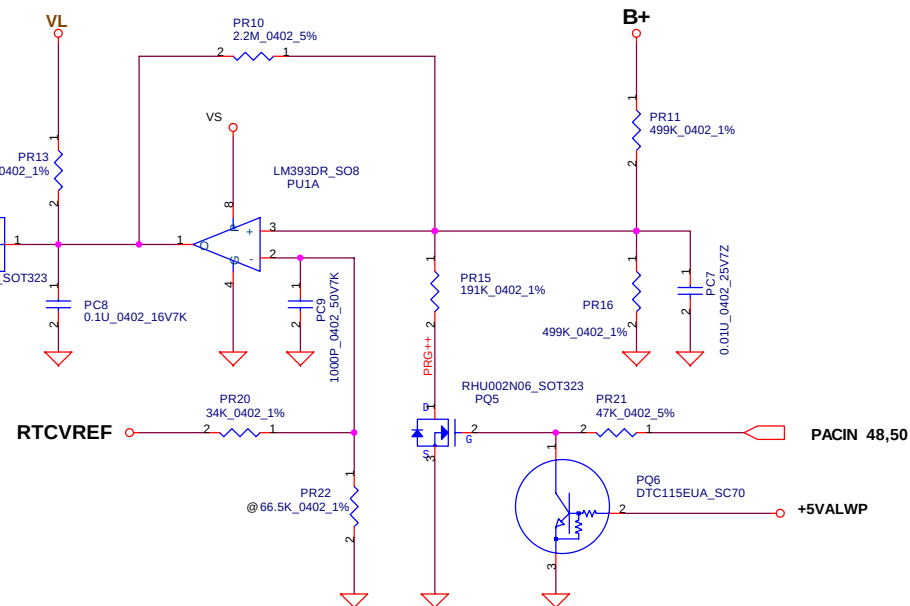
Precharge detector

	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

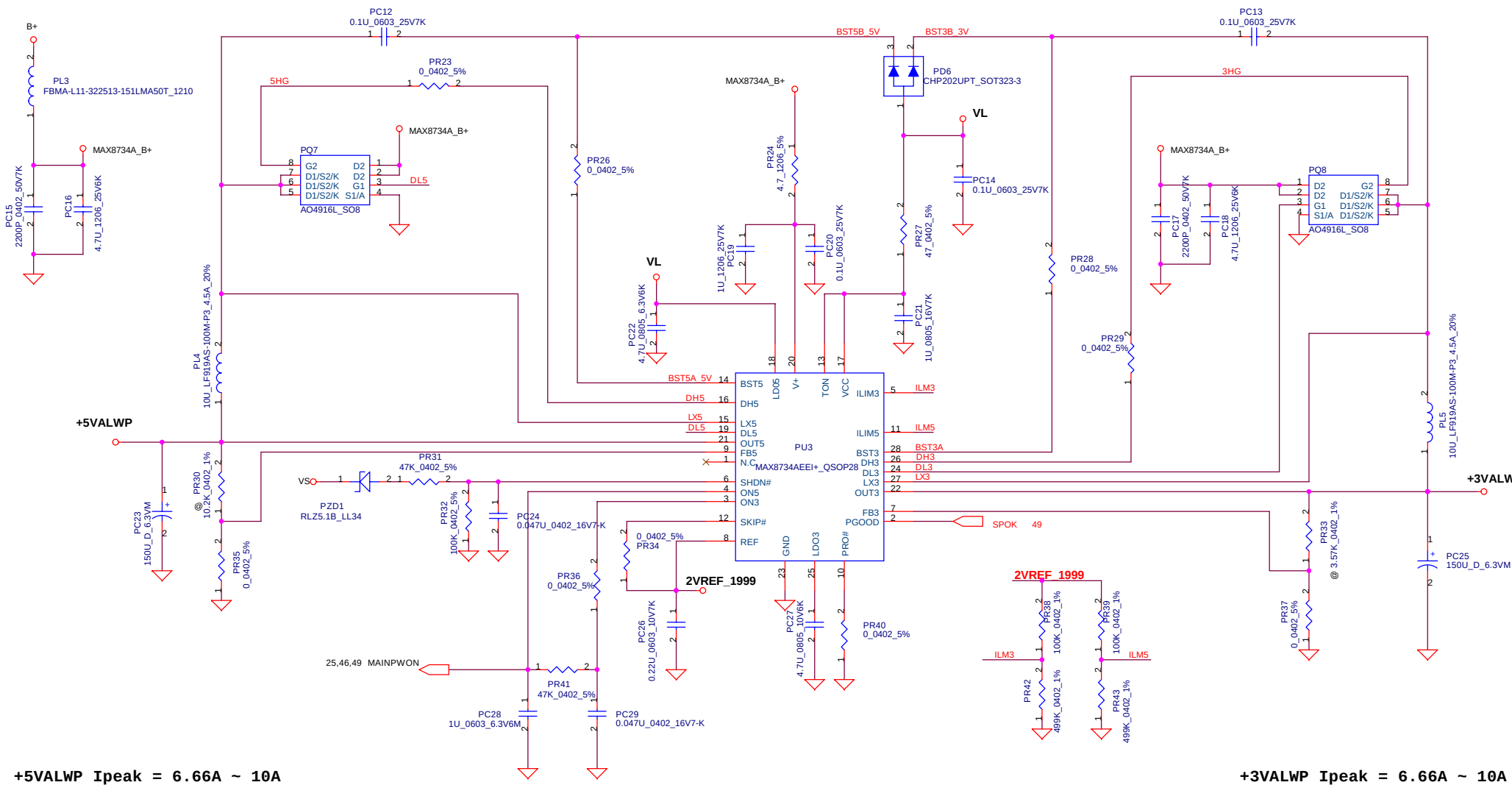
BATT ONLY

Precharge detector

	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



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				401454	Rev A
				Date: 星期四, 九月 14, 2006	Sheet 46 of 55

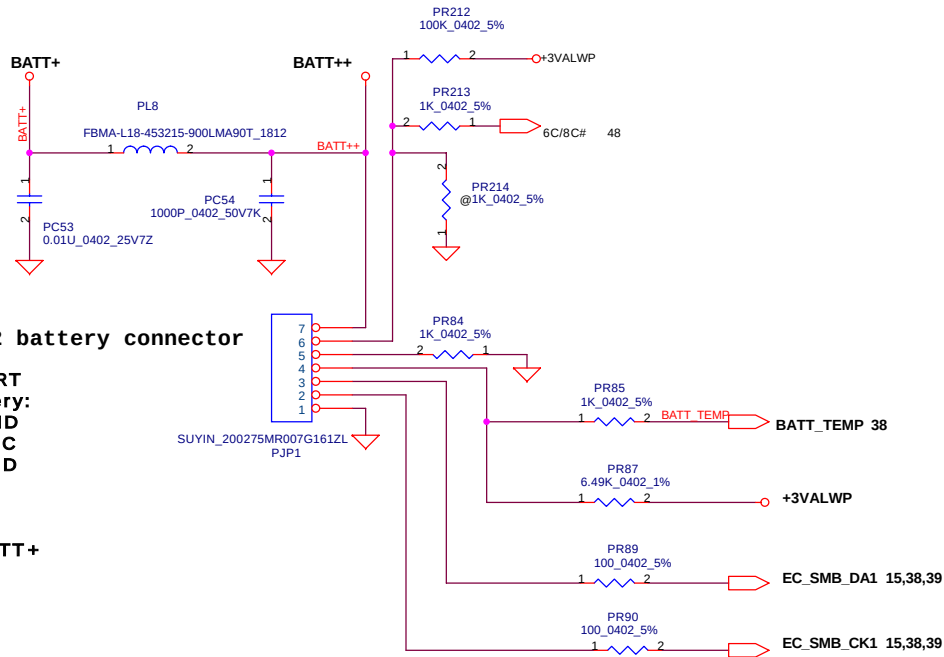


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				Custom	401454
				Date	Rev A
				星期四, 九月 14, 2006	Sheet 47 of 55

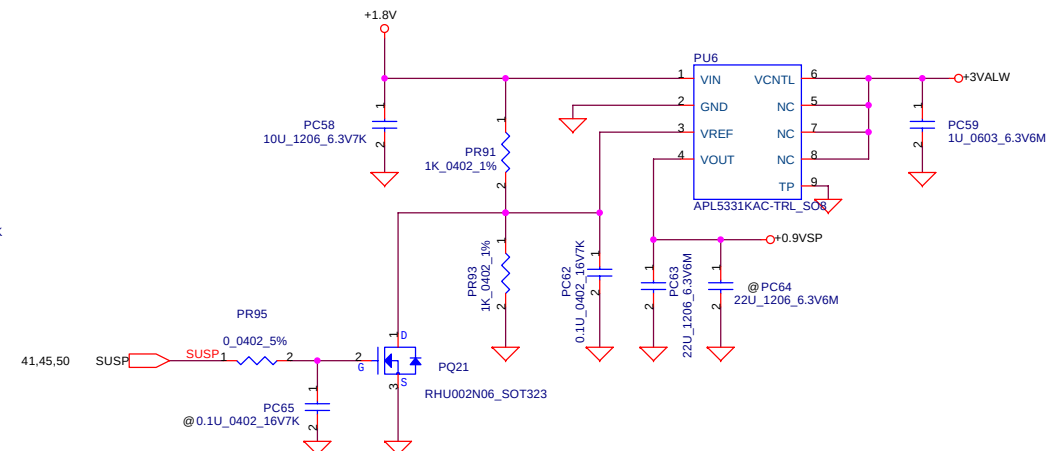
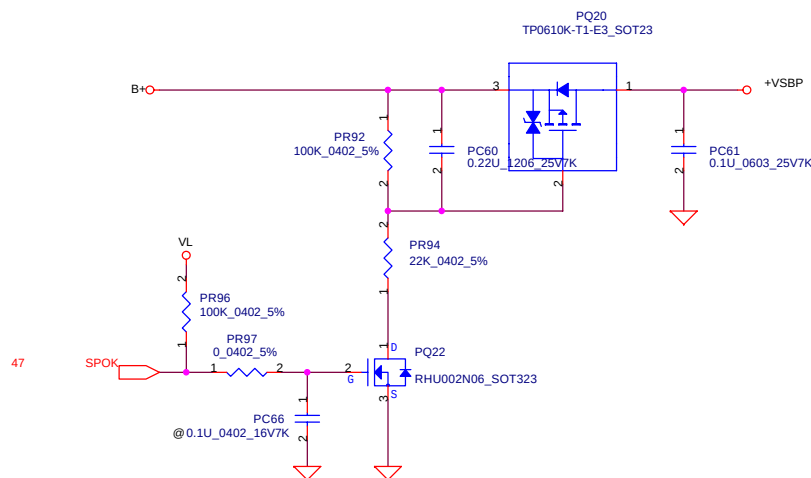
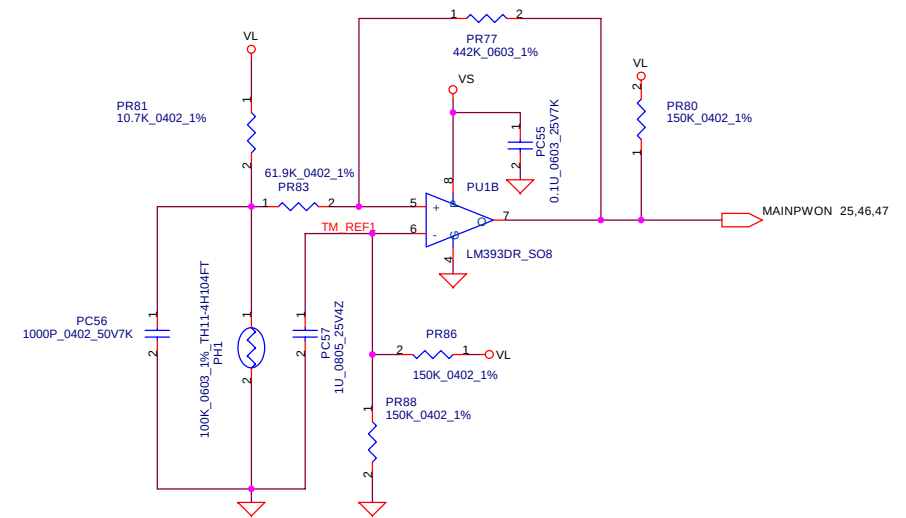
www.laptopfix.vn

PJP2 battery connector

SMART Battery:
1.GND
2.SMC
3.SMD
4.TS
5.B/I
6.ID
7.BATT+



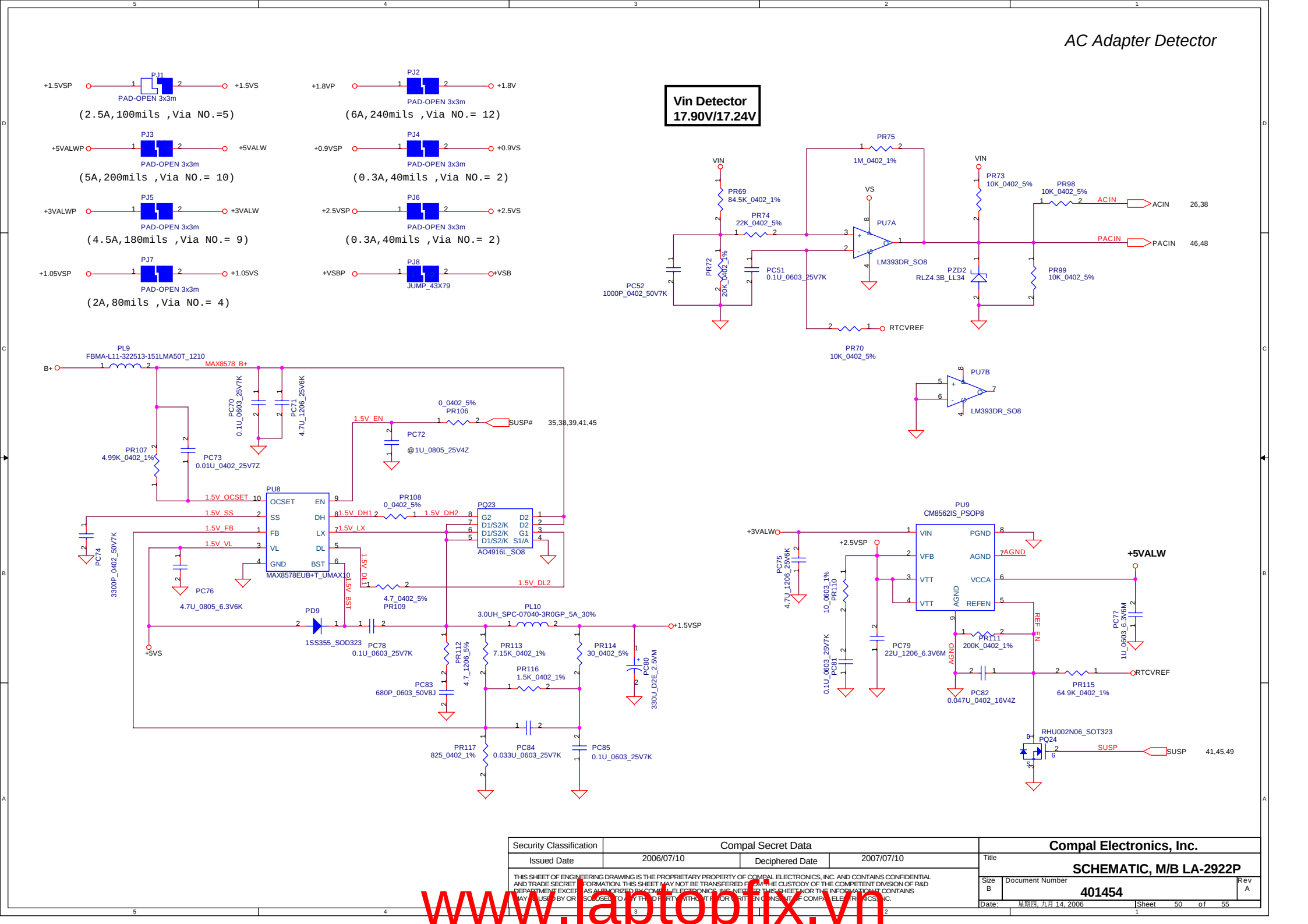
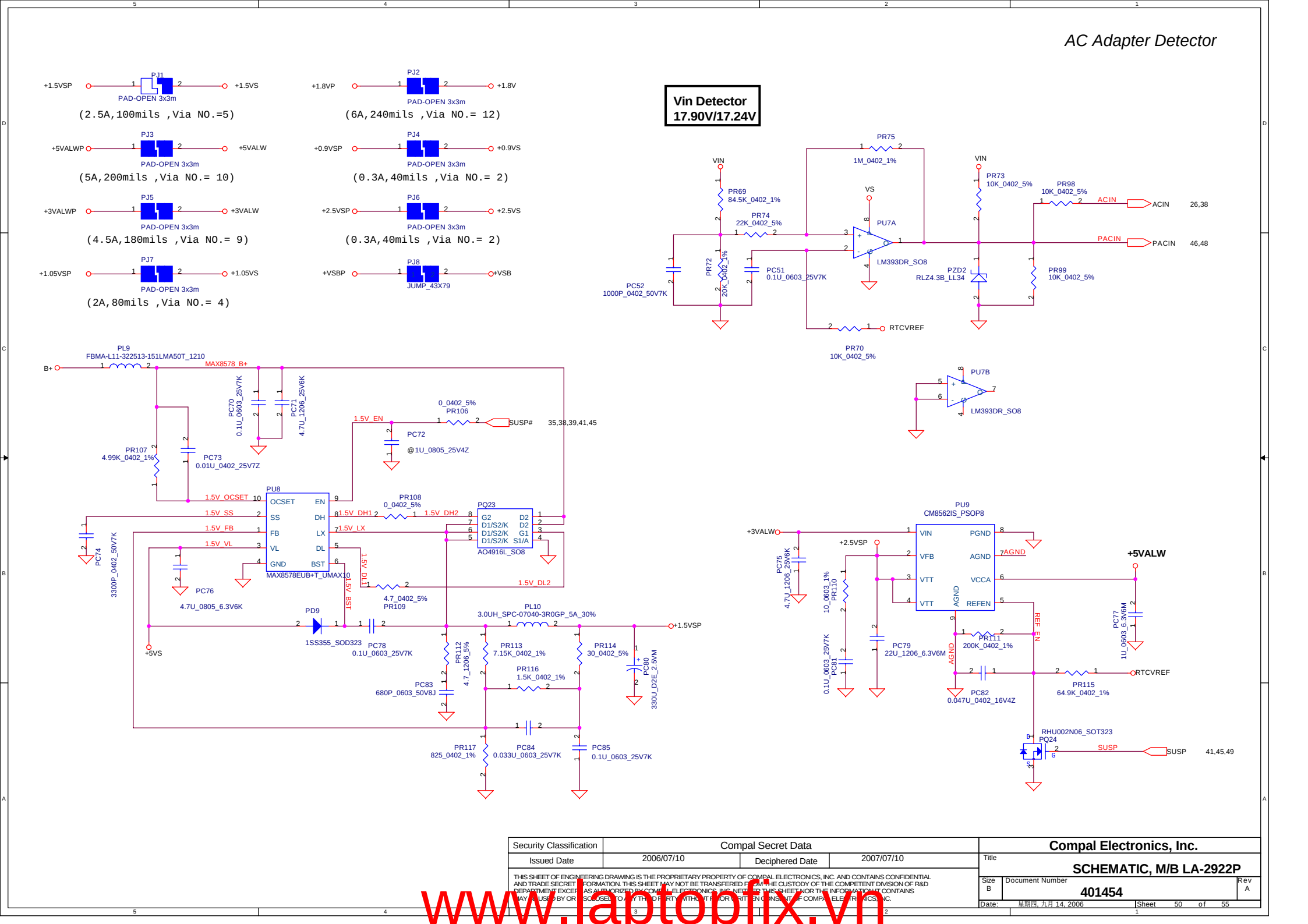
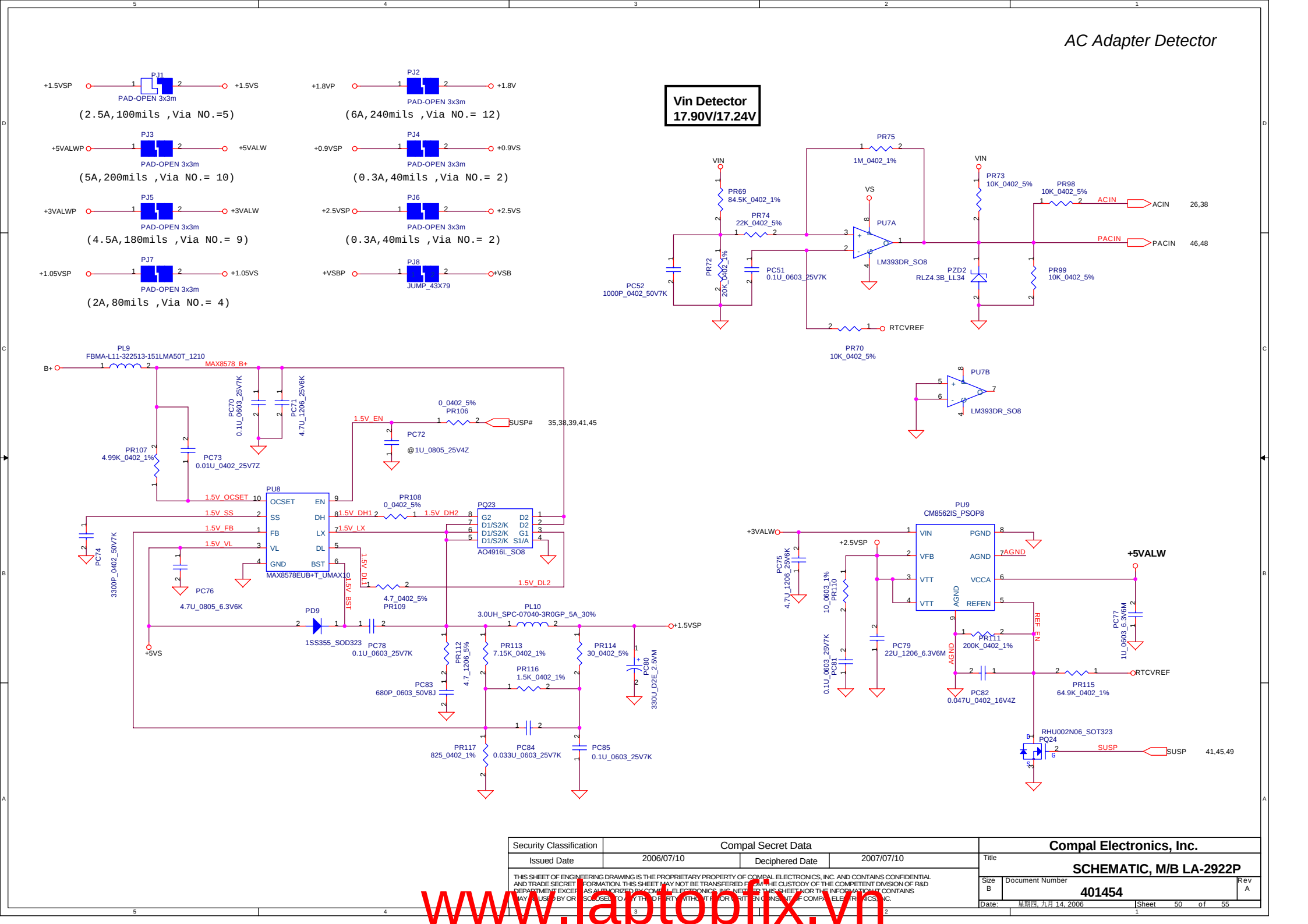
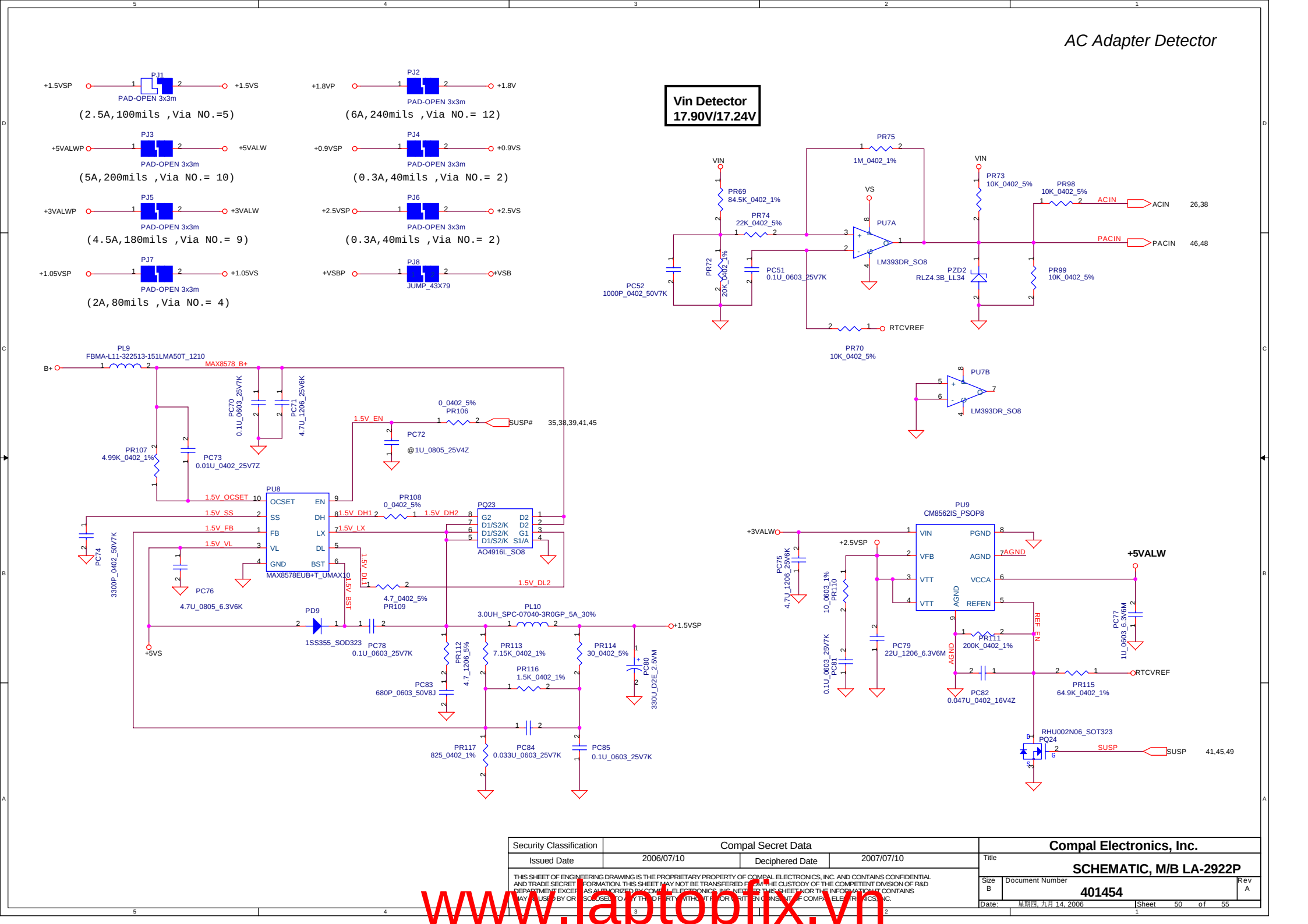
PH1 under CPU botten side :
CPU thermal protection at 80 degree C
Recovery at 44(45) degree C



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				Date: 星期四, 九月 14, 2006	Sheet 49 of 55

AC Adapter Detector

Vin Detector 17.90V/17.24V

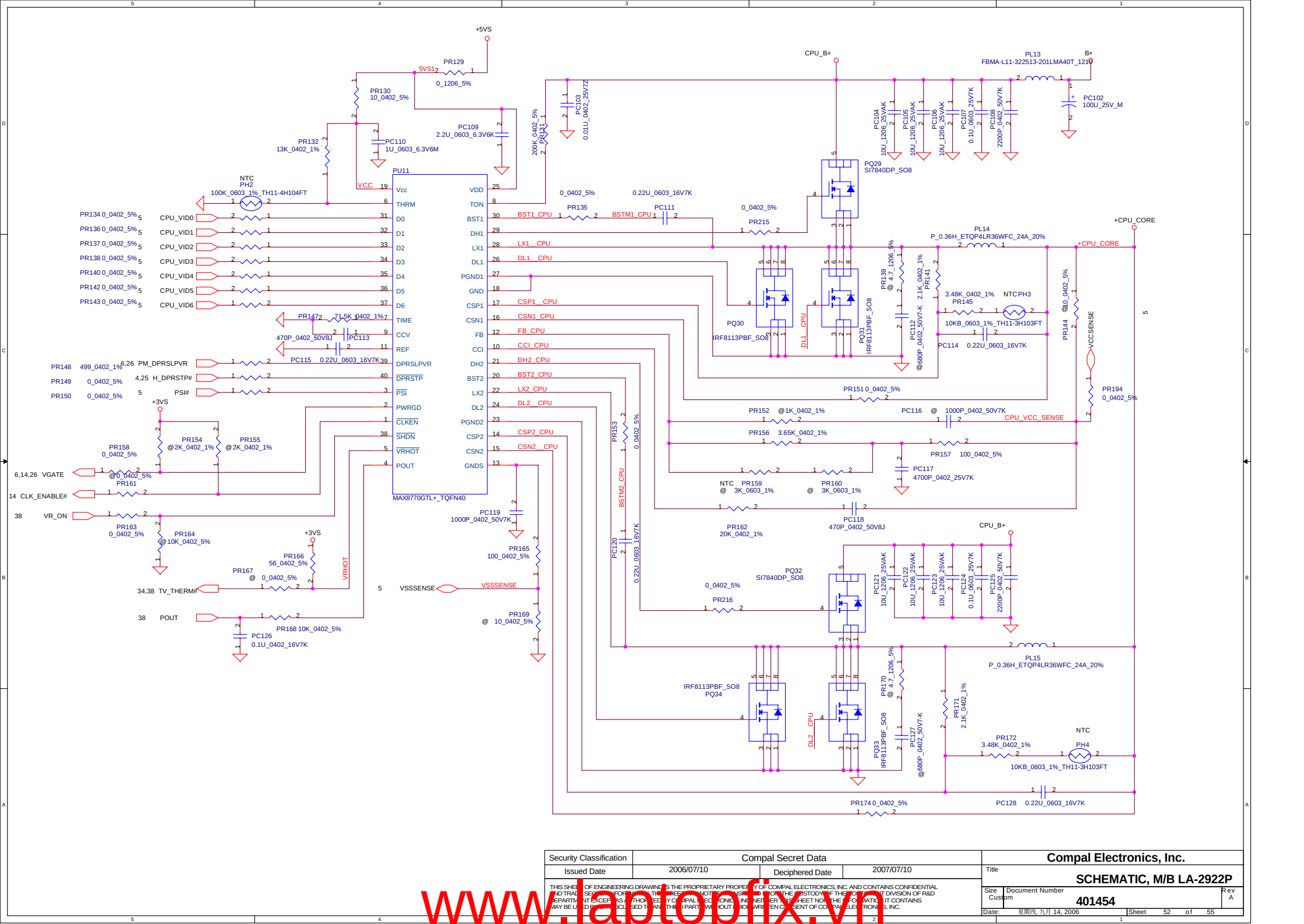


AC Adapter Detector

Vin Detector 17.90V/17.24V

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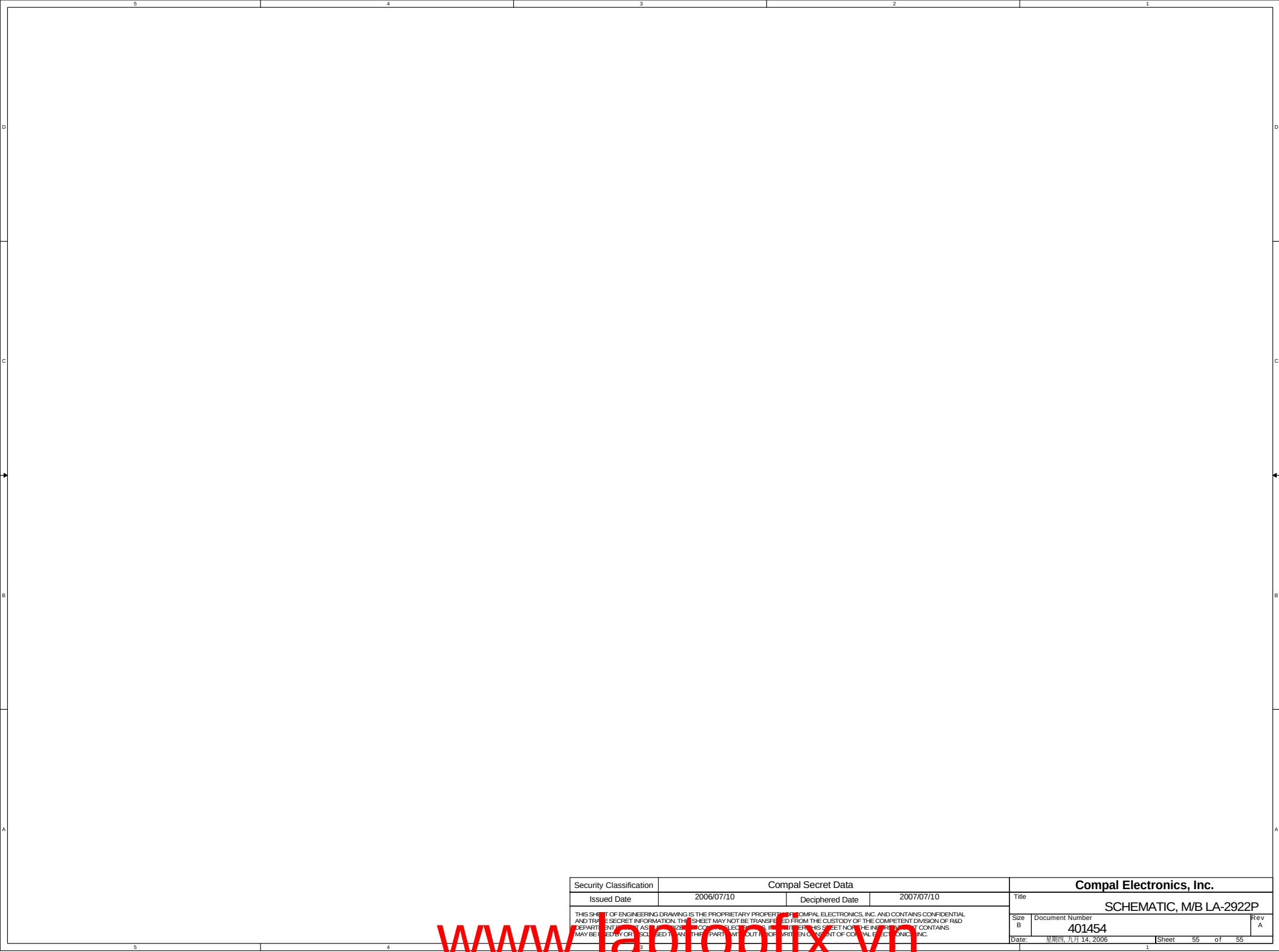


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Rev 0.1 --> Rev 1.0 Change List

- 1. Page15 : Change BOM structure of R831 to VGA@
- 2. Page17 : Add C1110 to C1120 on power plane for EMI Require.
- 3. Page26 : Add BOM structure @ on D38 & R887

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				Sheet 55 of 55	1