

COMPAL CONFIDENTIAL

MODEL NAME : *EDL70/71*
COMPAL P/N :
PCB NO :
Revision : *1B*

EDL70/71 Schematics Document

uFCBGA/uFCPGA Mobile Dothan
Intel Alviso + ICH6M

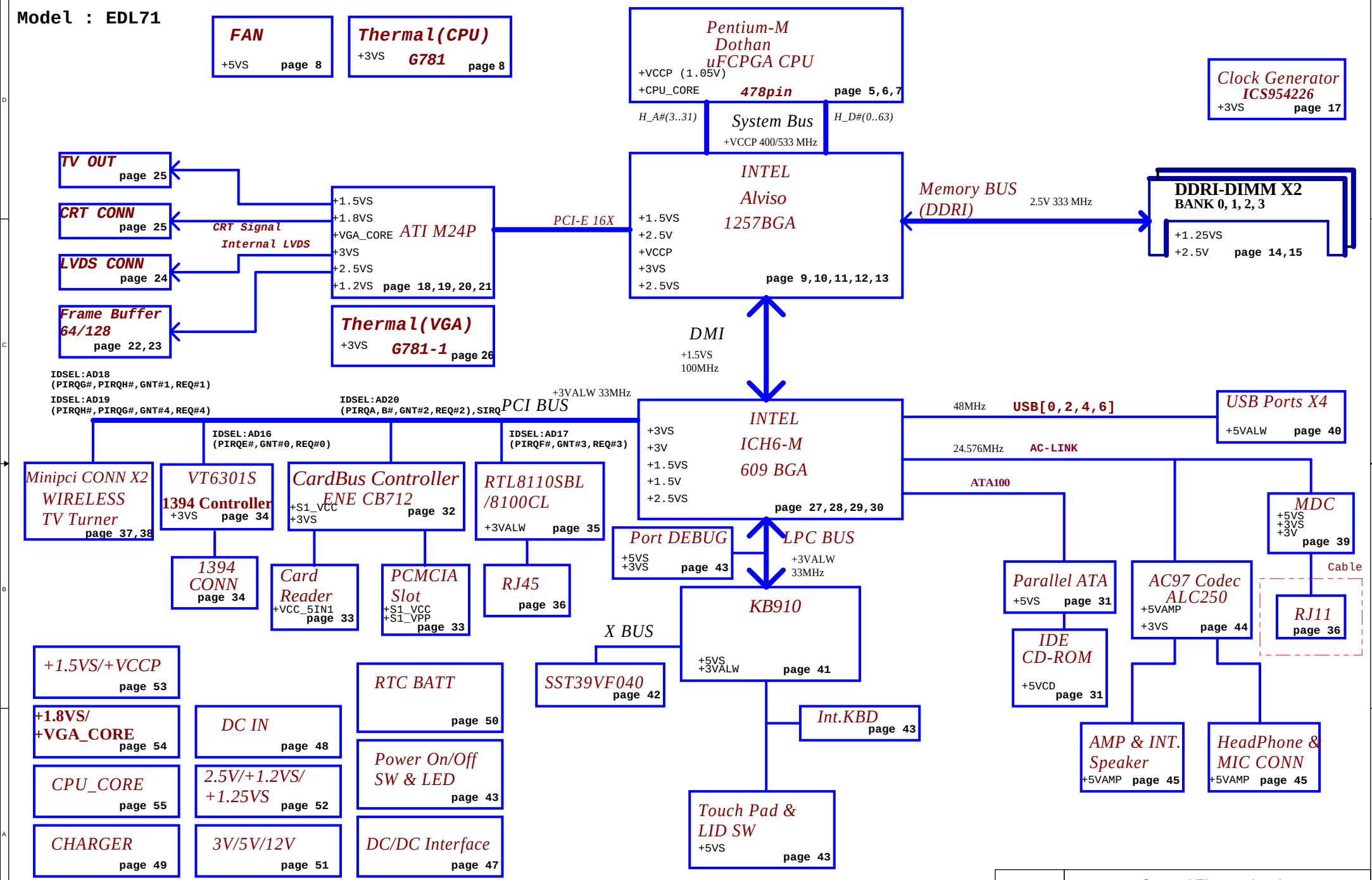
2005 - 02 - 25

REV : 1B

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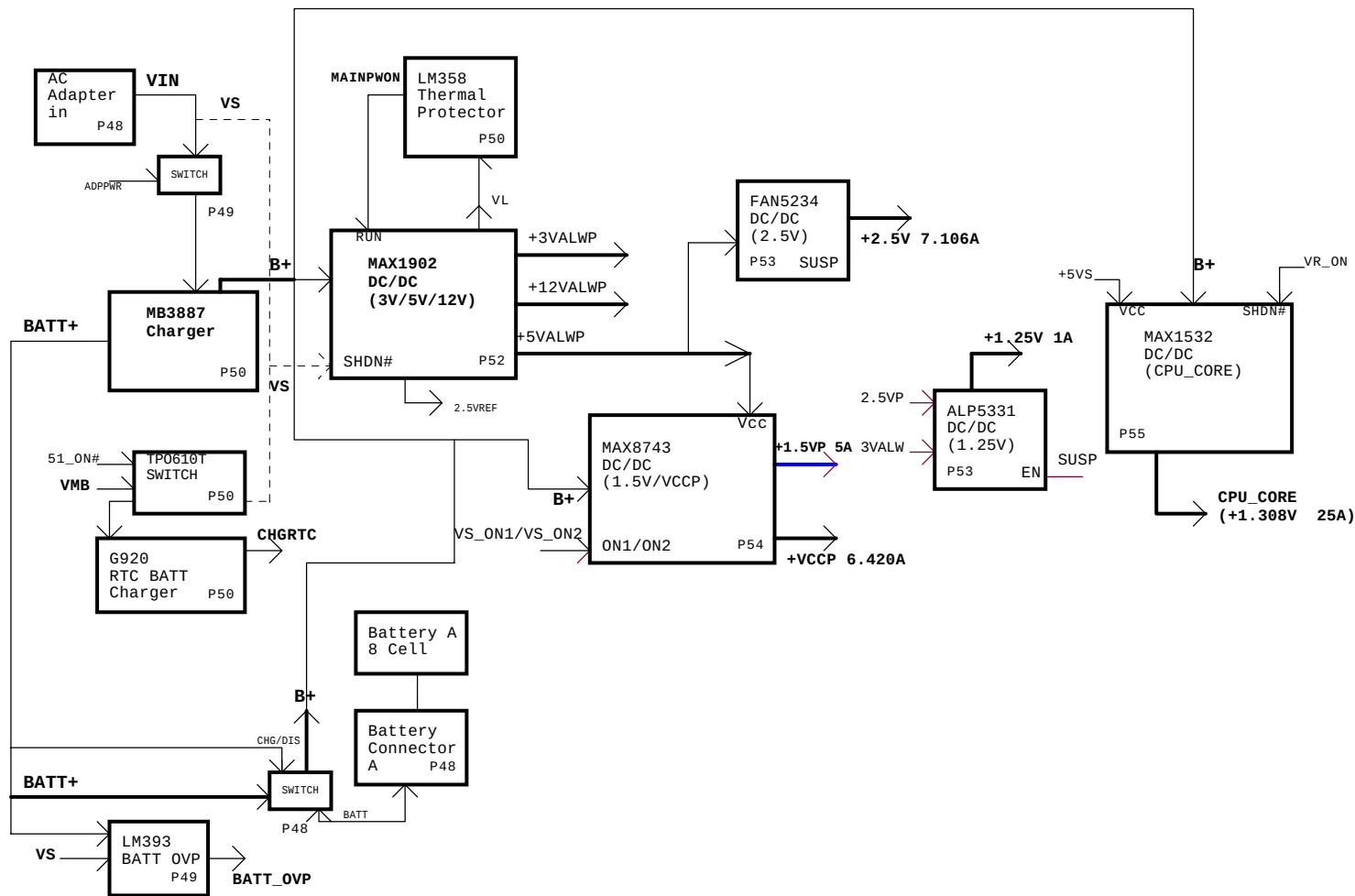
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Model : EDL71



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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+PCIE_1.2VS	+PCIE_1.2VS power rail for VGA PCIExpress	ON	OFF	OFF
+0.9VS	0.9VS for DDR2 Termination	ON	OFF	OFF
+VGA_CORE	VGA Core Power	ON	OFF	OFF
+1.5VS	MCH & ICH Core Power	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5VS switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
VGA			PIRQA
1394	AD16	0	PIRQE
LAN	AD17	3	PIRQF
CardBus	AD20	2	PIRQA,B
Mini-PCI	AD18	1	PIRQG/PIRQH
Mini-PCI II for TV Tunner	AD19	4	PIRQH/PIRQG

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	G781	1001 100X b
EEPROM(24C16/02)	1010 000X b		
G781-1	1001 101X b		

ICH6 SM Bus address

Device	Address
Clock Generator (ICS954206)	1101 001Xb
DDR II DIMM0	1010 000Xb
DDR II DIMM1	1010 001Xb

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	0.6
6	1.0
* 7	1.B

SKU ID Table

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

SKU ID	EDL71 SKU
* 0	EDL71 10/100 LAN WO/TV TUNER
1	EDL71 GIGA LAN W/TV TURNER
2	EDL71 10/100LAN W/TV TUNER
3	EDL71 GIGA WO/TV TUNER
4	EDL71 10/100 LAN WO/TV TUNER
5	EDL71 10/100LAN W/TV TUNER
6	EDL71 GIGA WO/TV TUNER
7	EDL71 GIGA LAN W/TV TURNER

NOTE1:

SWDJ@ : SWDJ
NOSWDJ@ : W/O SWDJ

TV@ : TV Tunner

@XX : Depop component

100@ : 10/100M LAN

1@XX : Pop for Integrated Graphic

GIGA@ : 10/100M/1000M LAN

2@XX : Pop for External Graphic

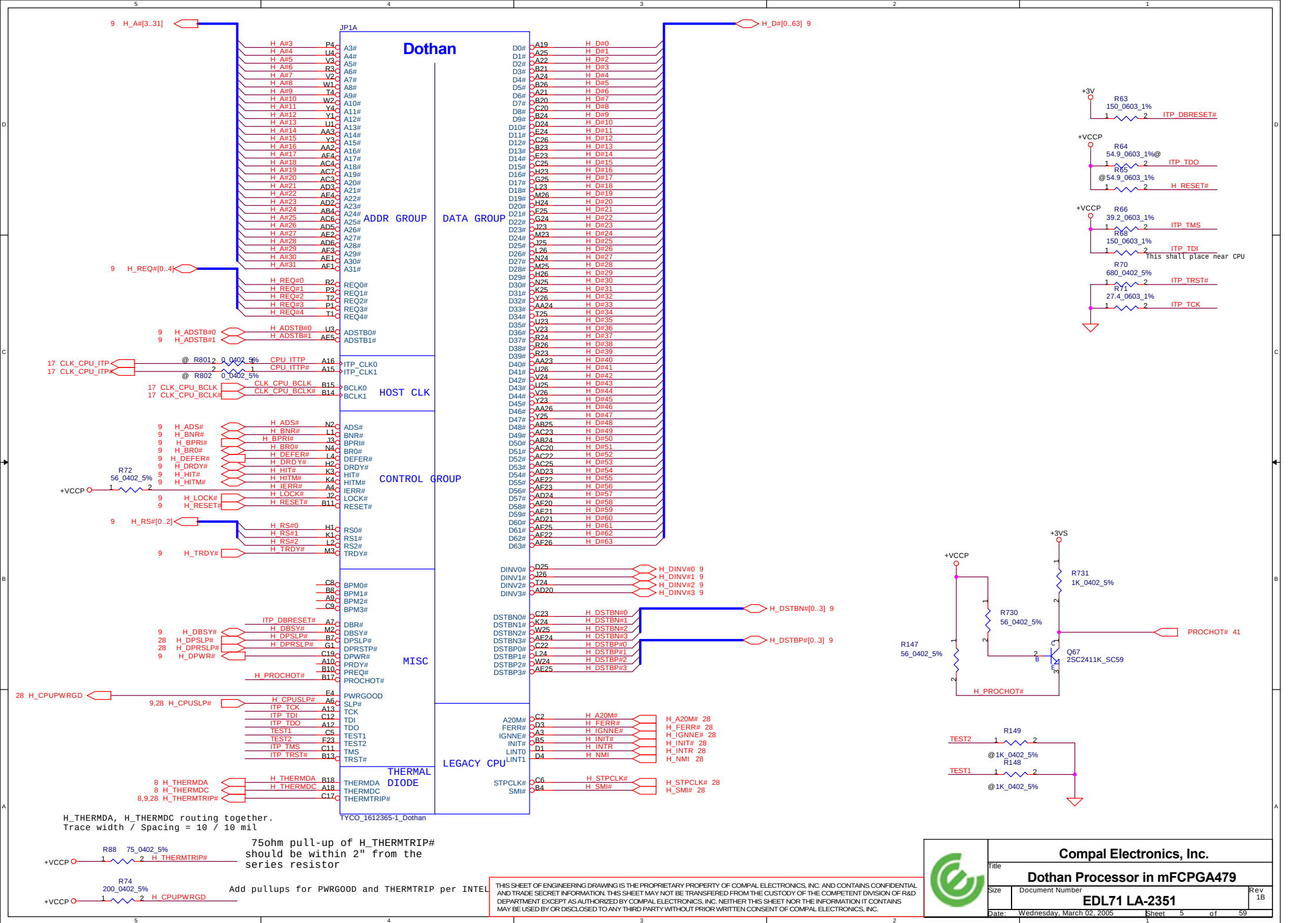
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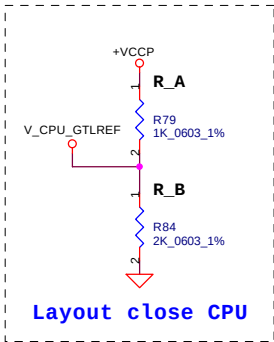
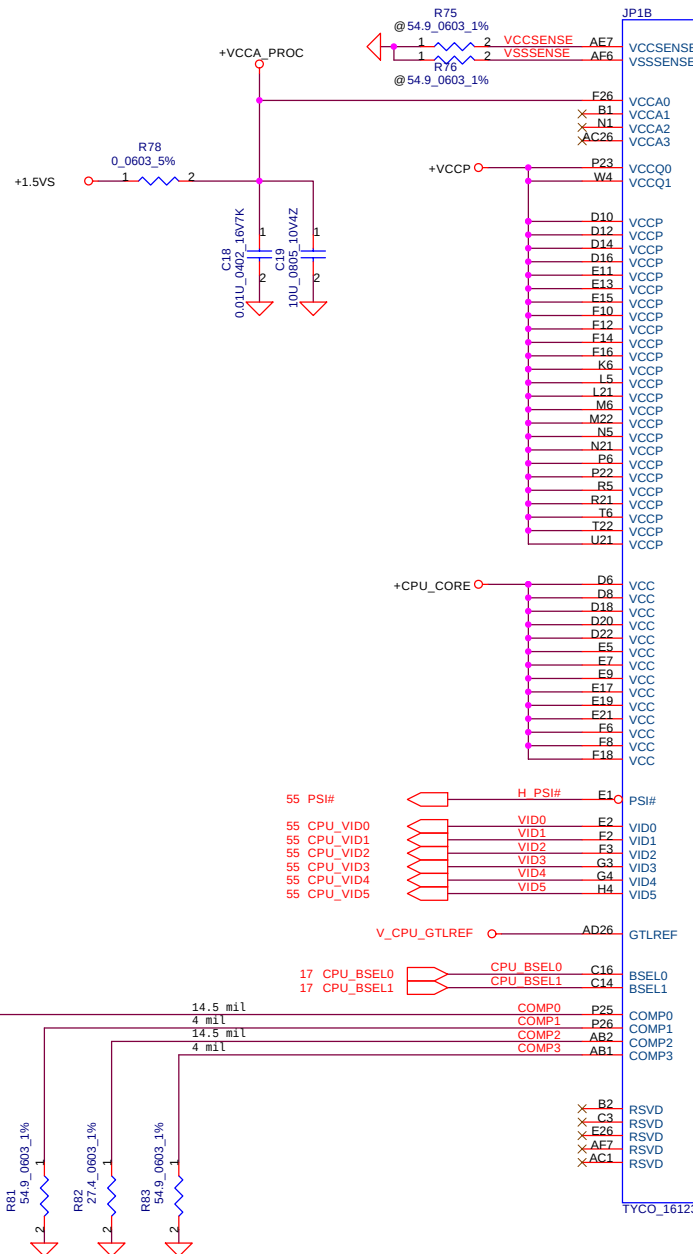


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Notes List

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Resistor placed within 0.5" of CPU pin. Trace should be at least 25 miles away from any other toggling signal.

Layout close CPU

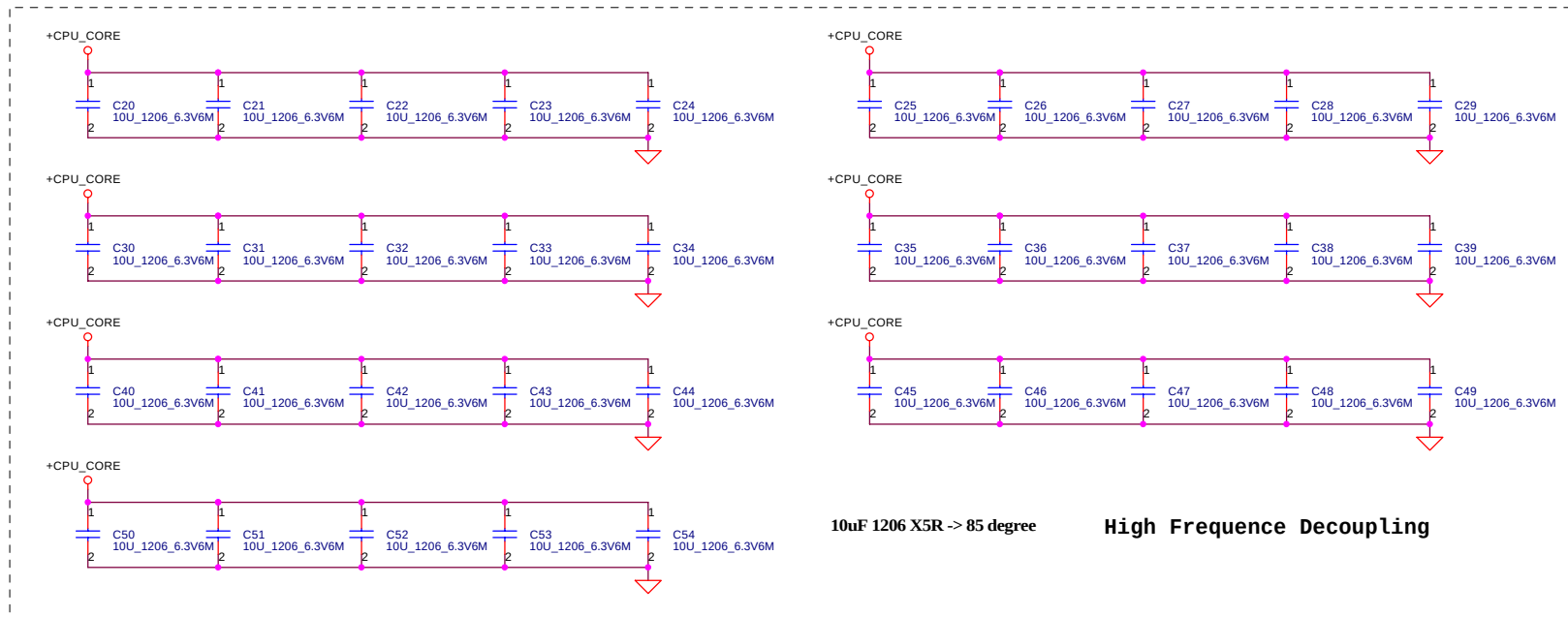
Dothan
POWER, GROUND, RESERVED SIGNALS AND NC

Dothan
POWER, GROUND

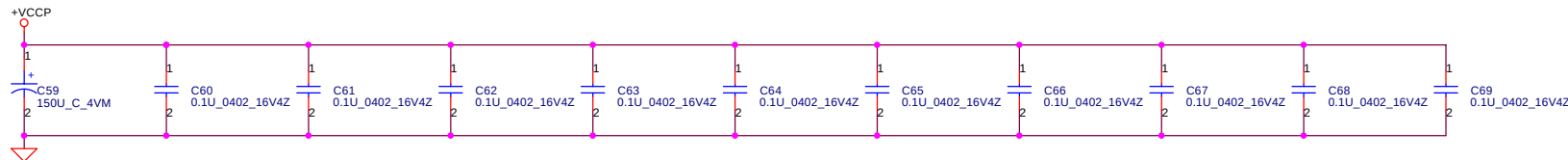
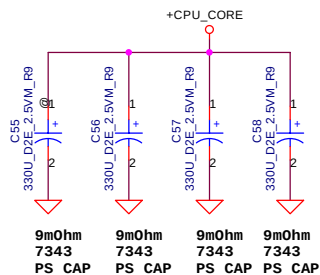


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Dothan Processor in mFCPGA479			
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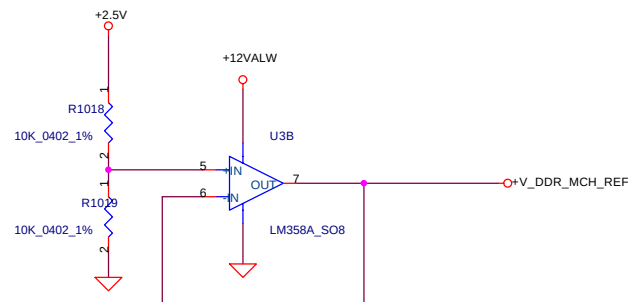
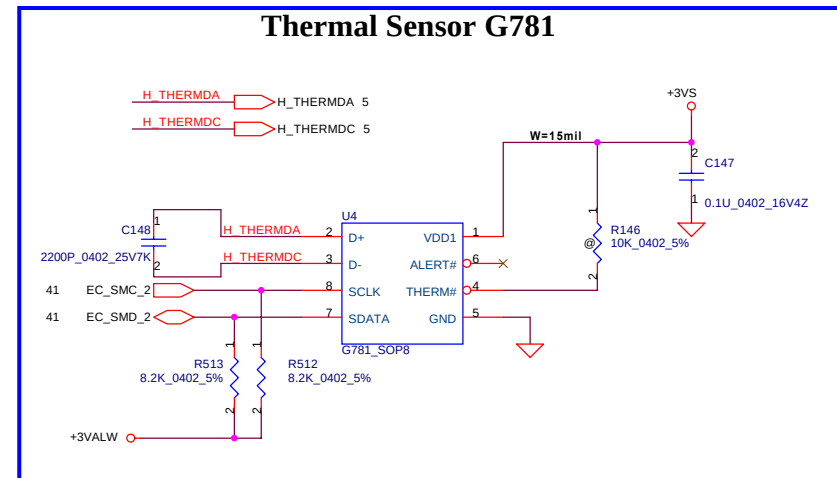
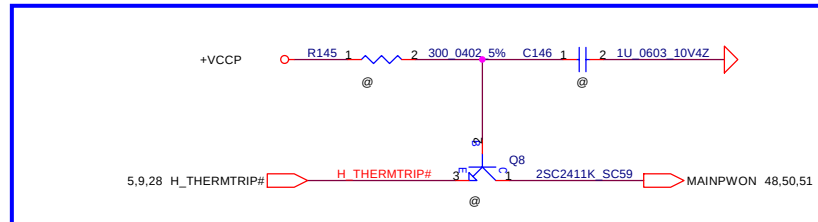
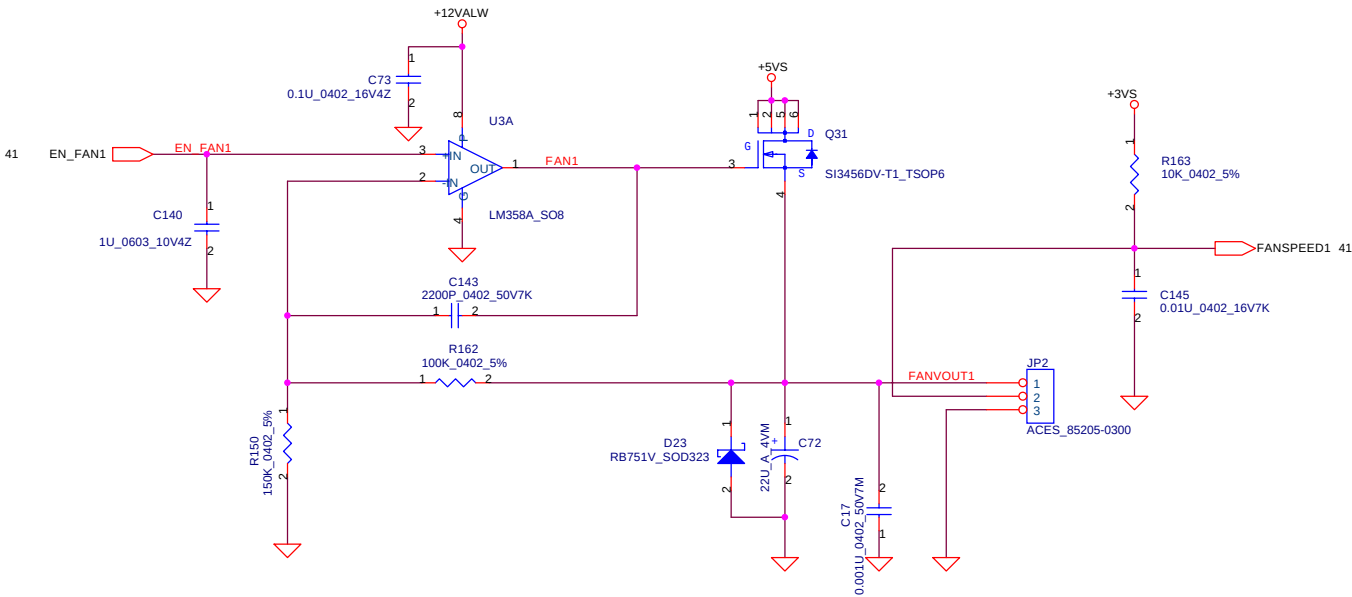
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Near VCORE regulator.

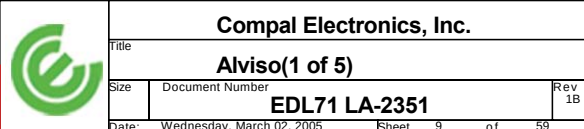


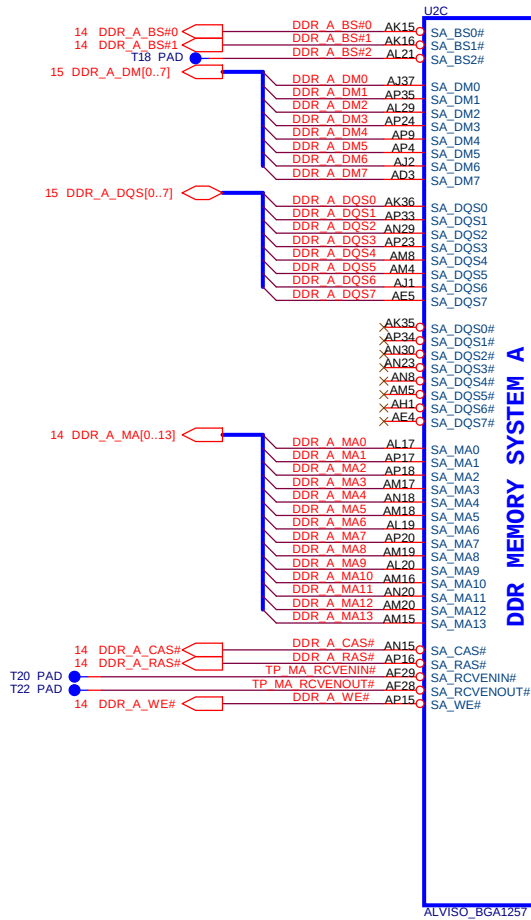
Fan Control circuit



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FAN & Thermal Sensor			
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POWER

POWER

W=30 mils

Note : All VCCSM pin shorted internally.

Note : C126, C129 No stuff for Ext. VGA. Stuff for Int. VGA.

Note : R137, R138 stuff for Ext. VGA. R137, R138 no stuff for Int. VGA.

Route VSSA_TVBG GND from GMCH to decoupling cap ground lead and then connect to the GND plane.

Route VSSA3GBG gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.

CRTDAC: Route caps within 250mil of Alviso. Route FB within 3" of Alviso.

Route VSSACRTDAC gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.

CRT DAC Voltage Follower Circuit - 700mV TV DAC Voltage Follower Circuit - 700mV

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Alviso(4 of 5)

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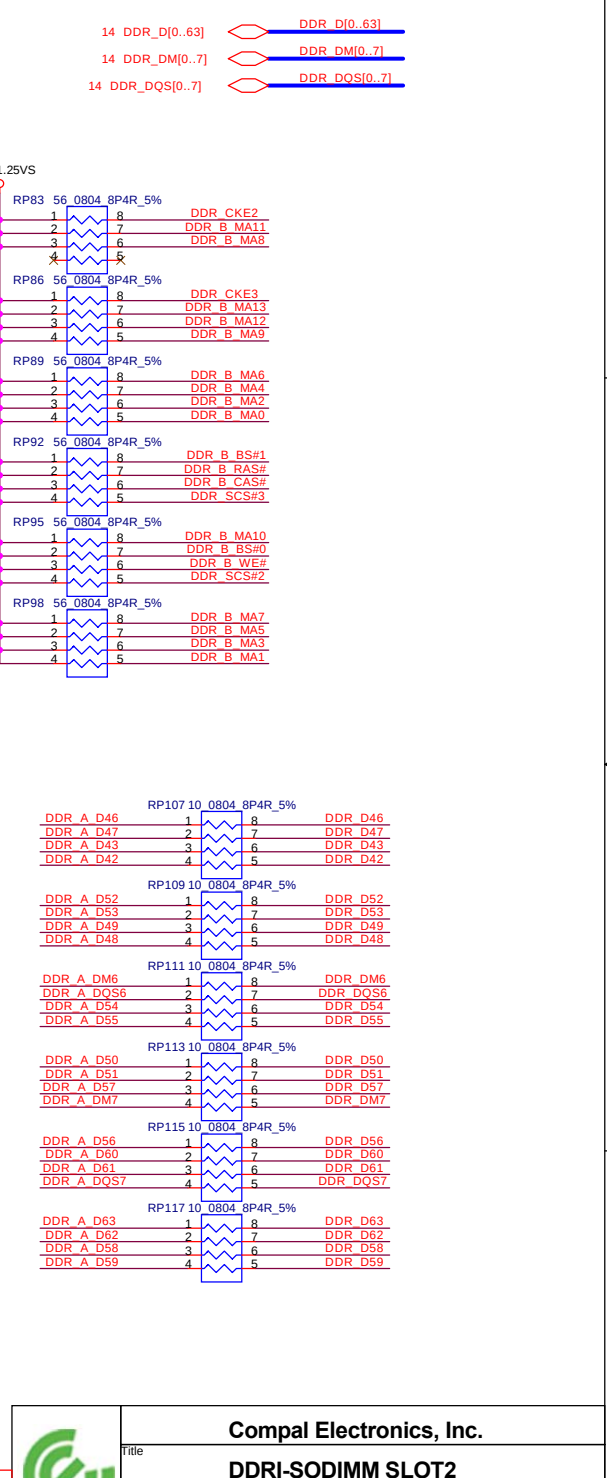
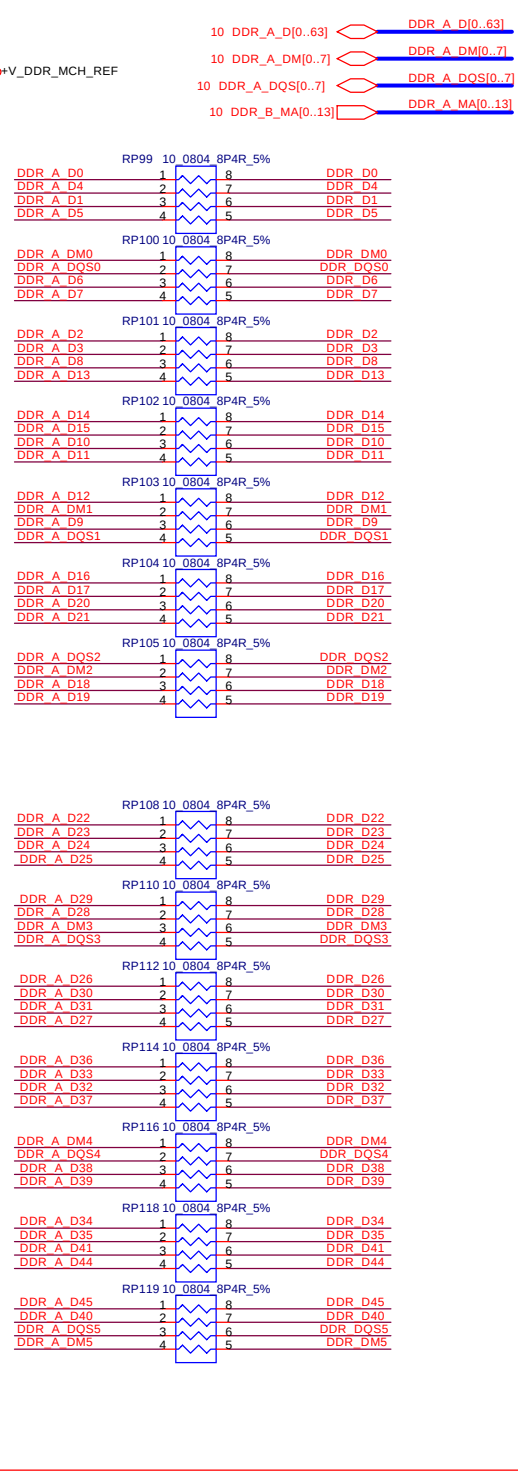
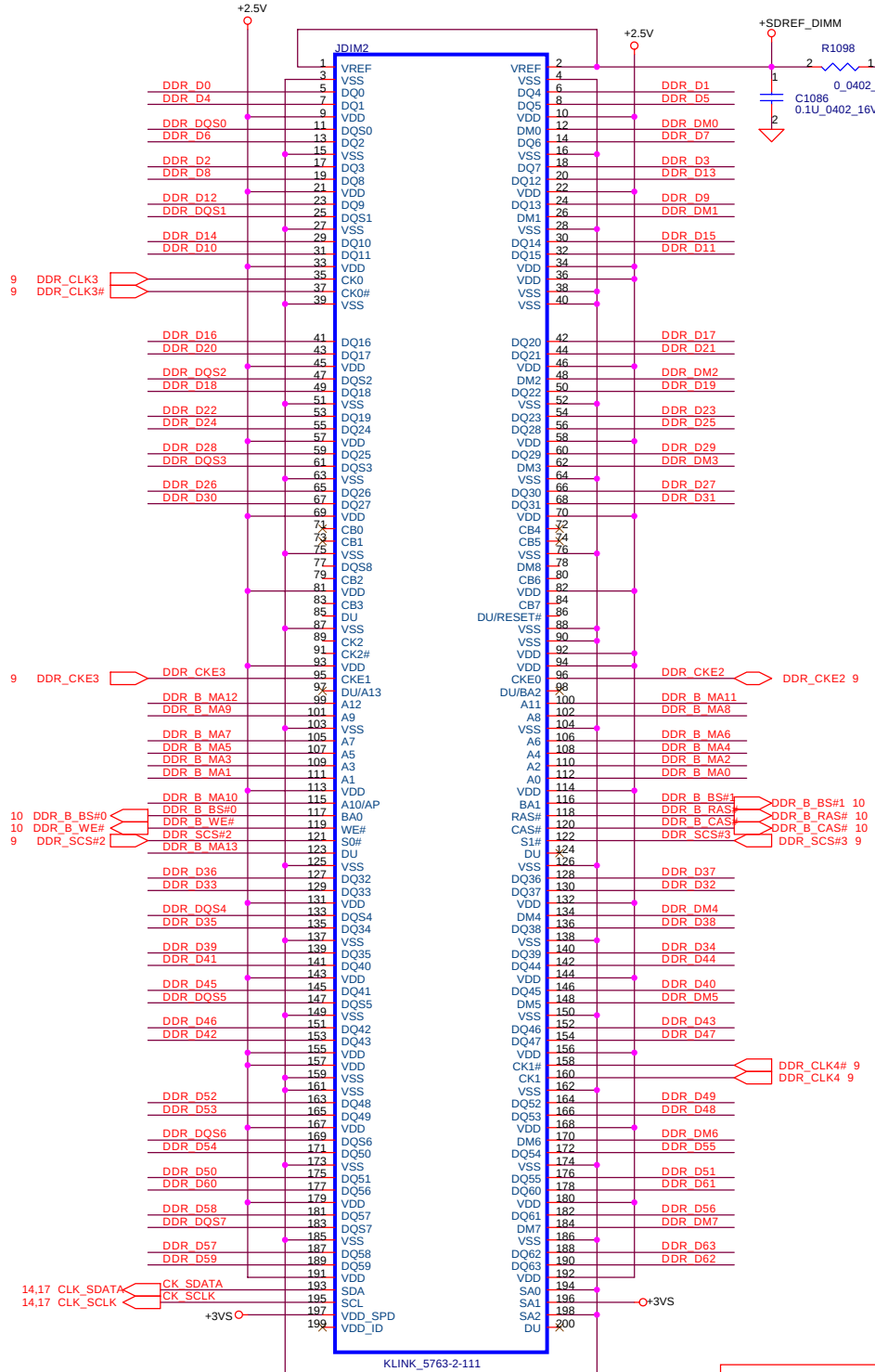
VSS

VSS

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Title

DDR1-SODIMM SLOT2

EDL71 LA-2351

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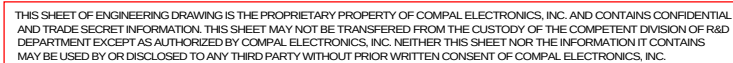
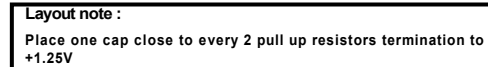
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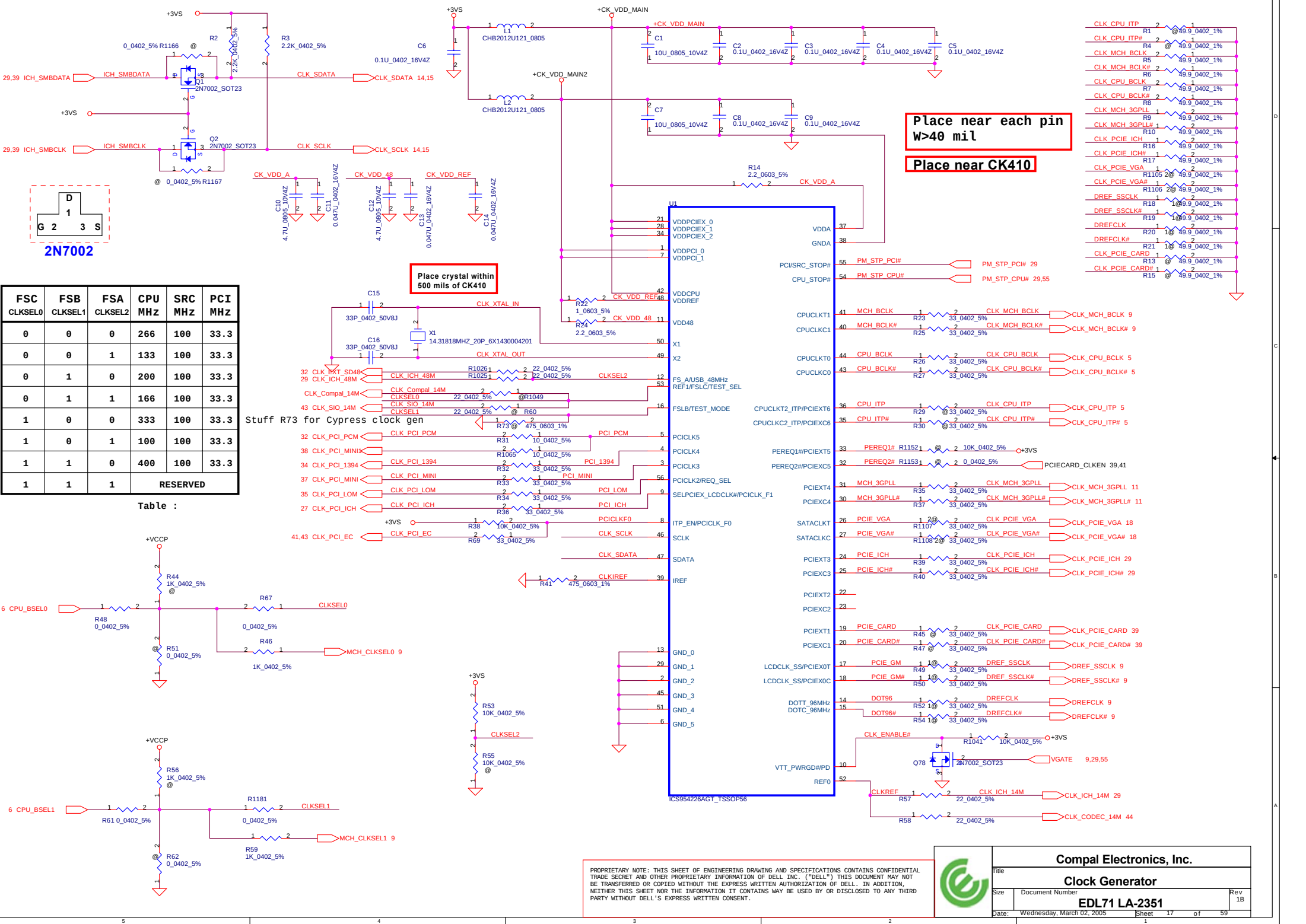
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Distribute as close as possible to DDR-SODIMM.



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DDR Decoupling			
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FSC	FSB	FSA	CPU	SRC	PCI
CLKSEL0	CLKSEL1	CLKSEL2	MHZ	MHZ	MHZ
0	0	0	266	100	33.3
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3
1	0	0	333	100	33.3
1	0	1	100	100	33.3
1	1	0	400	100	33.3
1	1	1	RESERVED		

Table :

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Clock Generator		
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FLASH ROM
(if no problem can be remove)

U60 UNMOUNT : VBIOS MUST COMBINE WITH SYSTEM BIOS

- USA
- Part 1 of 5
- DVO / EXT TMD5 / GPIO
- PCI EXPRESS
- LVDS
- TMD5
- DAC2
- CLK SS
- THERM

MEM Type Selection		
	MEMSEL0	MEMSEL1
64M Samsung	LOW	LOW
64M Hynix	LOW	HI
128M Samsung	HI	LOW
128M Hynix	HI	HI

Note:
Keep toggling signals always from
RSET/RSET2 resistor and trace.
Layout wider in resistor to GND.

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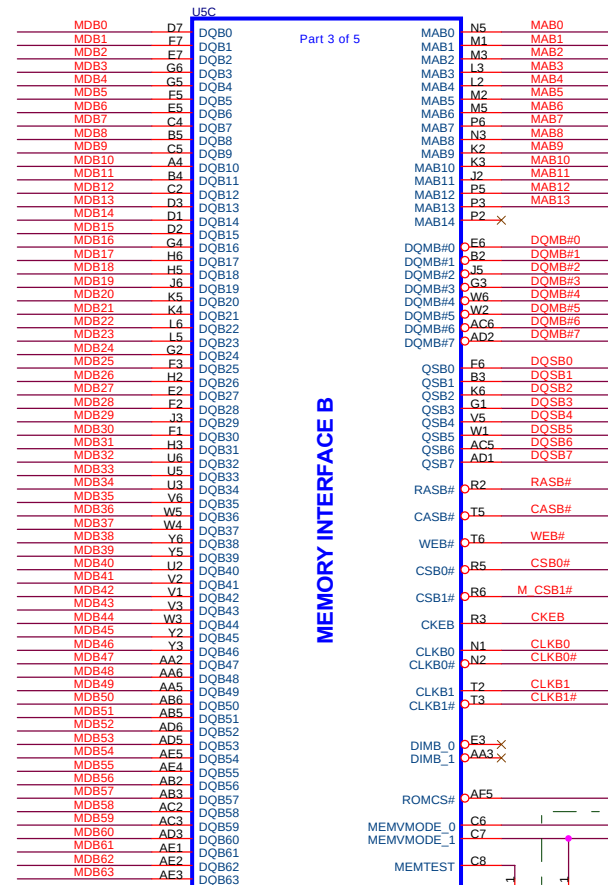
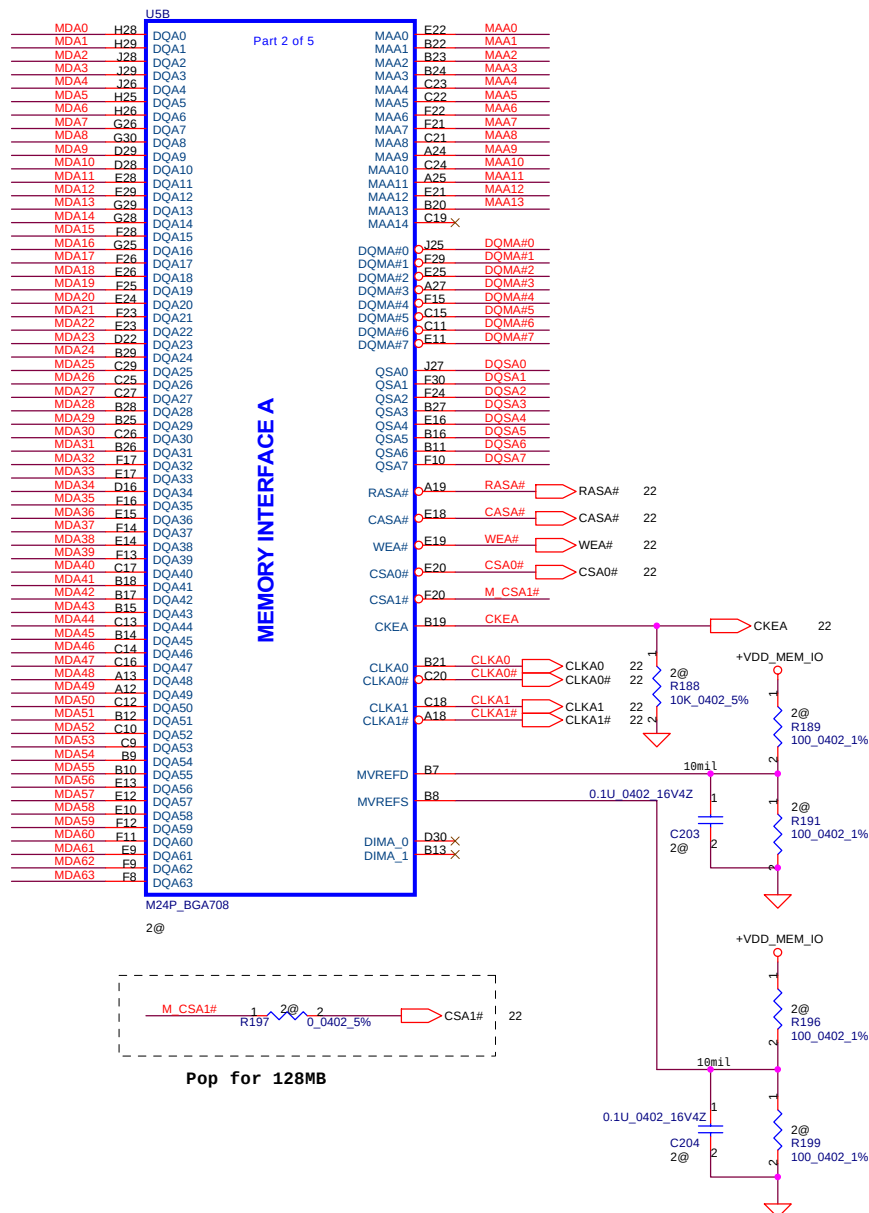


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MDA[63:0] 22
MAA[13:0] 22
DQSA[7:0] 22
DQMA[7:0] 22

MDB[63:0] 23
MAB[13:0] 23
DQSB[7:0] 23
DQMB[7:0] 23

NOTE :Elpida Memory Data Groups
Swapping Possibilities--
Shaded group belonging to QS1 and QS5
can't be swapped with other groups
(MD15:8) & (MD47:40)



MEM IO Voltage Selection

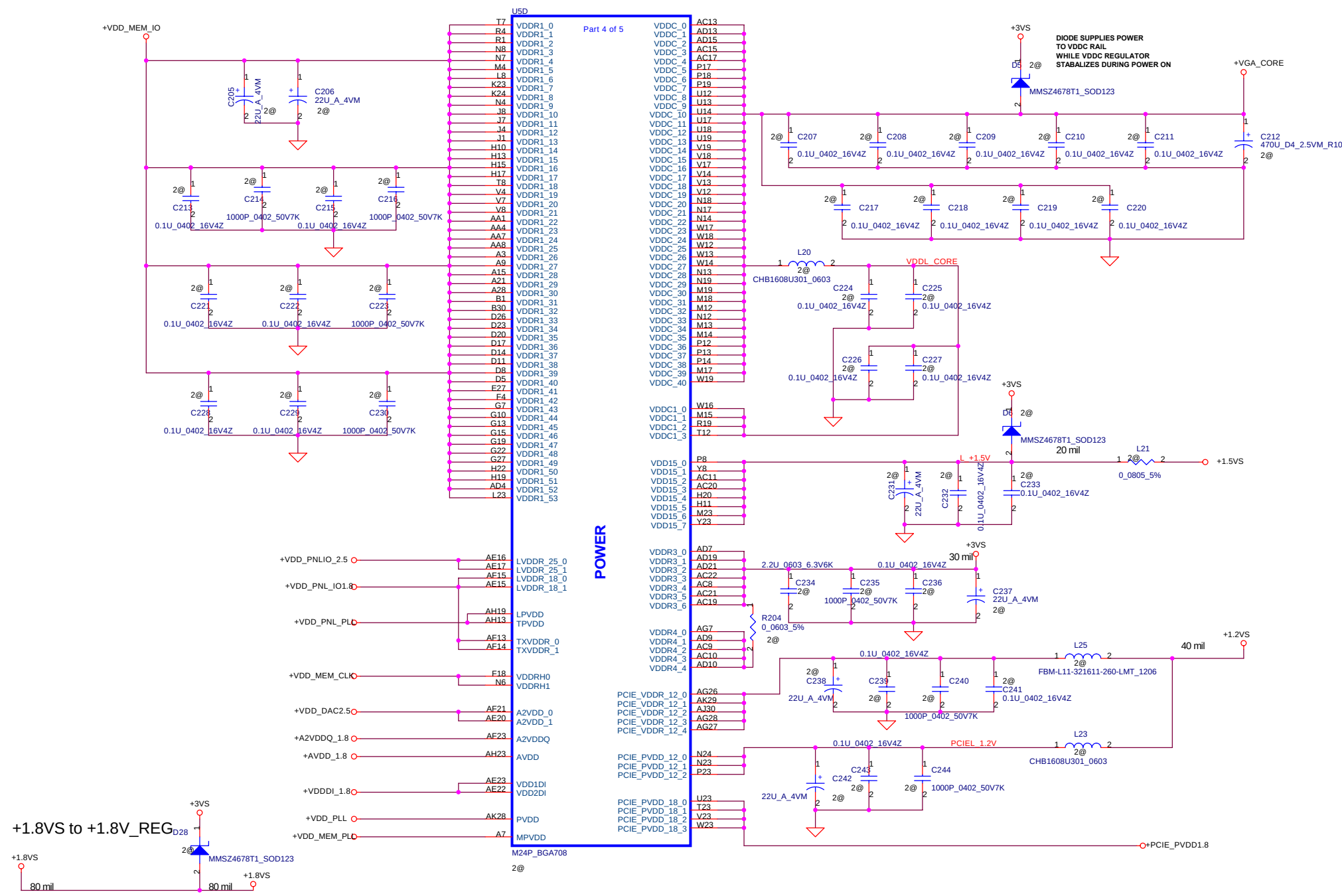
	2.5V * VDDR1	1.8V VDDR1
MEMVMODE0	HI	LOW
MEMVMODE1	LOW	HI

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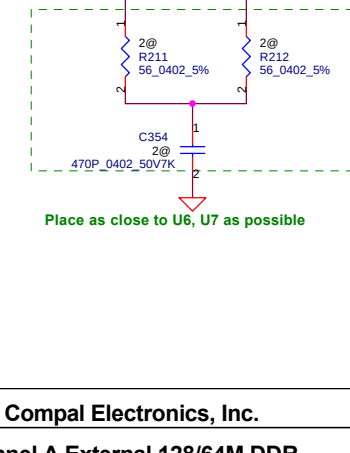
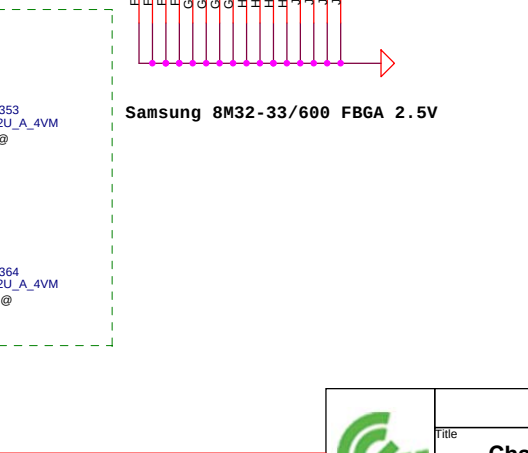
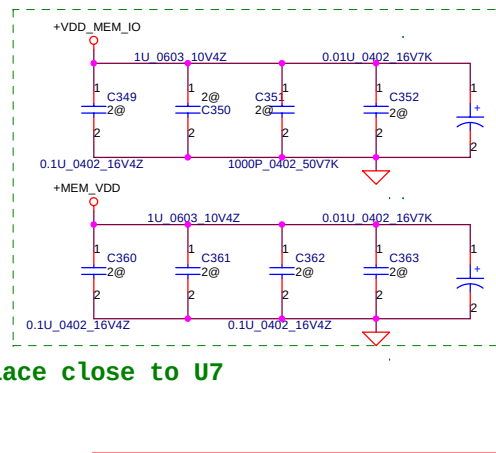
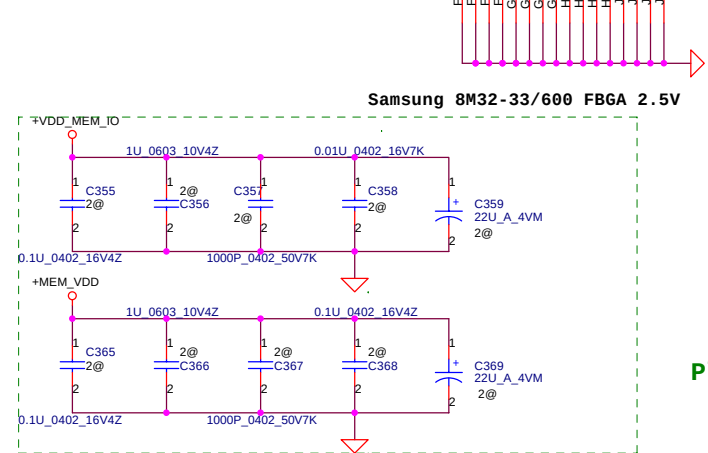
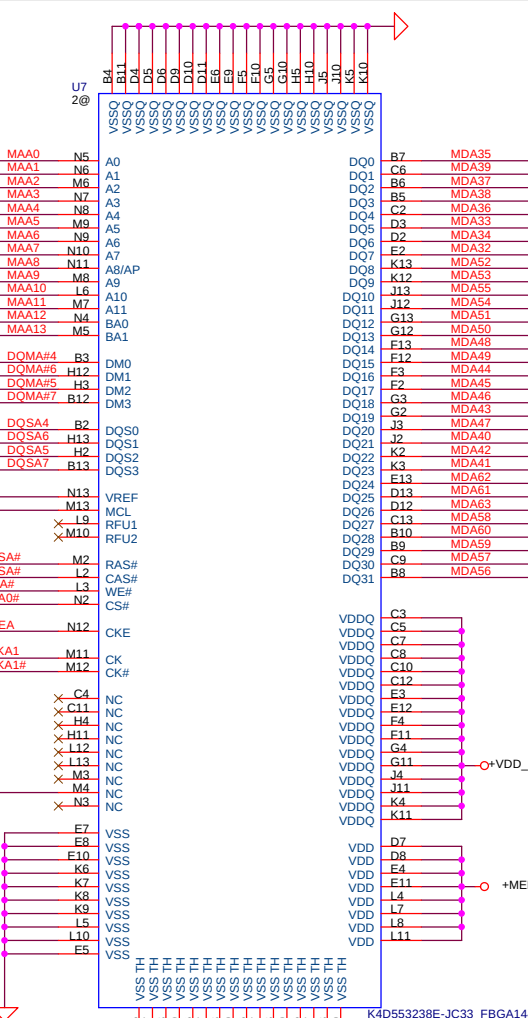
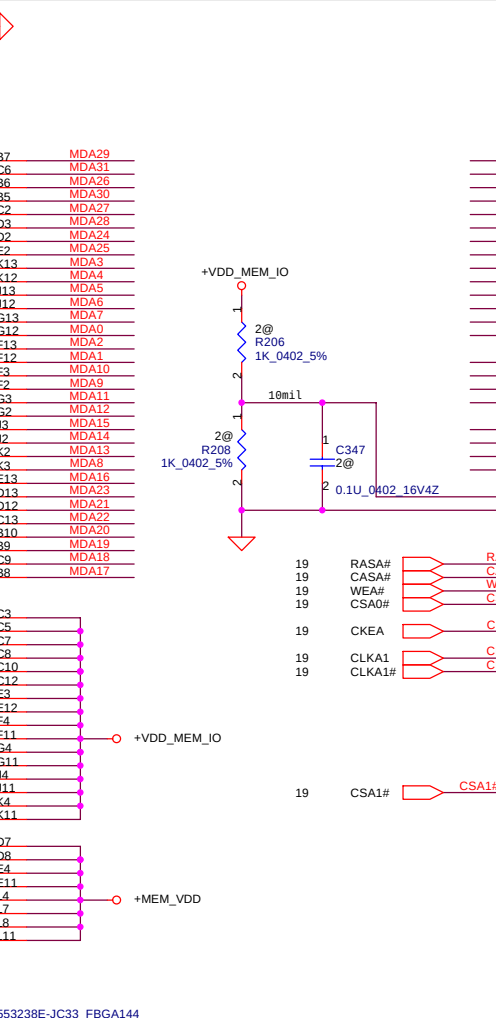
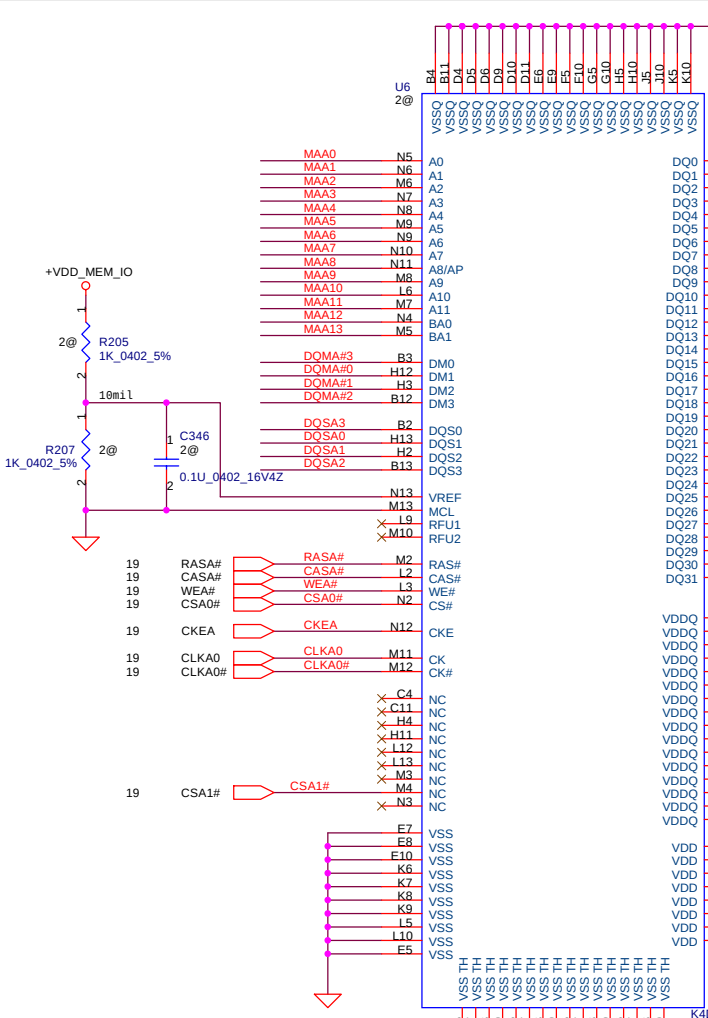
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ATI M24P MEM Interface		
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ATI M24P I/O PWR(1/2)			
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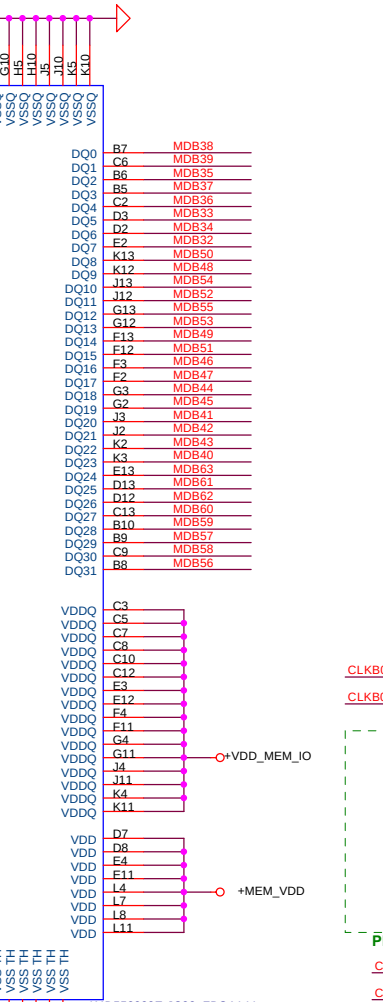
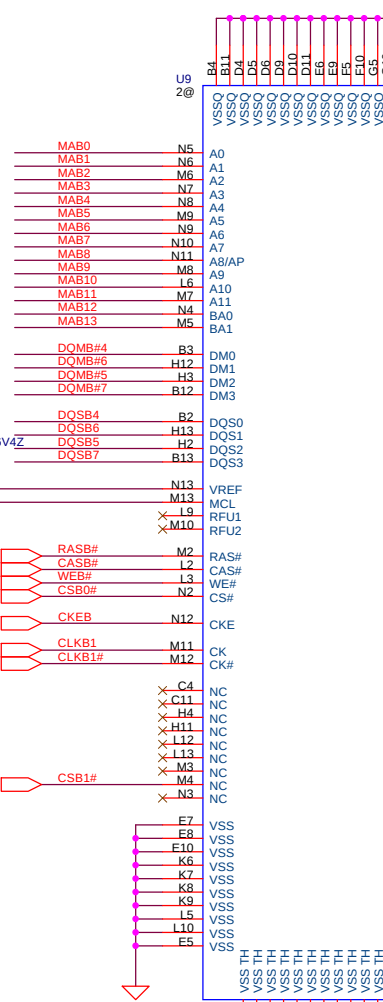
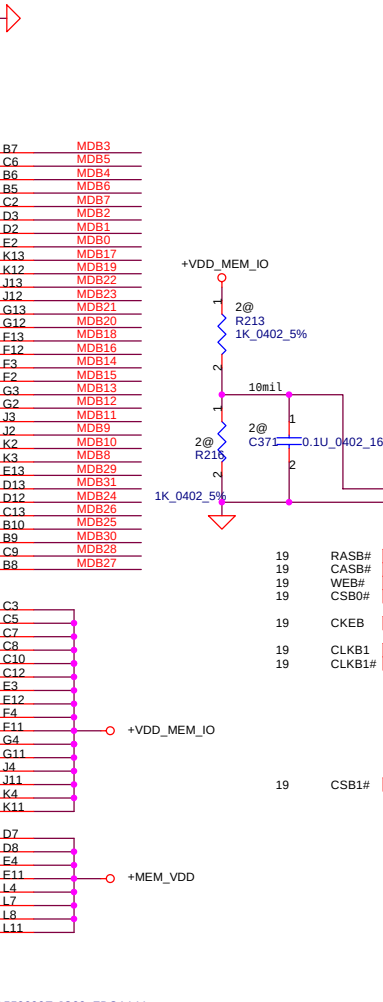
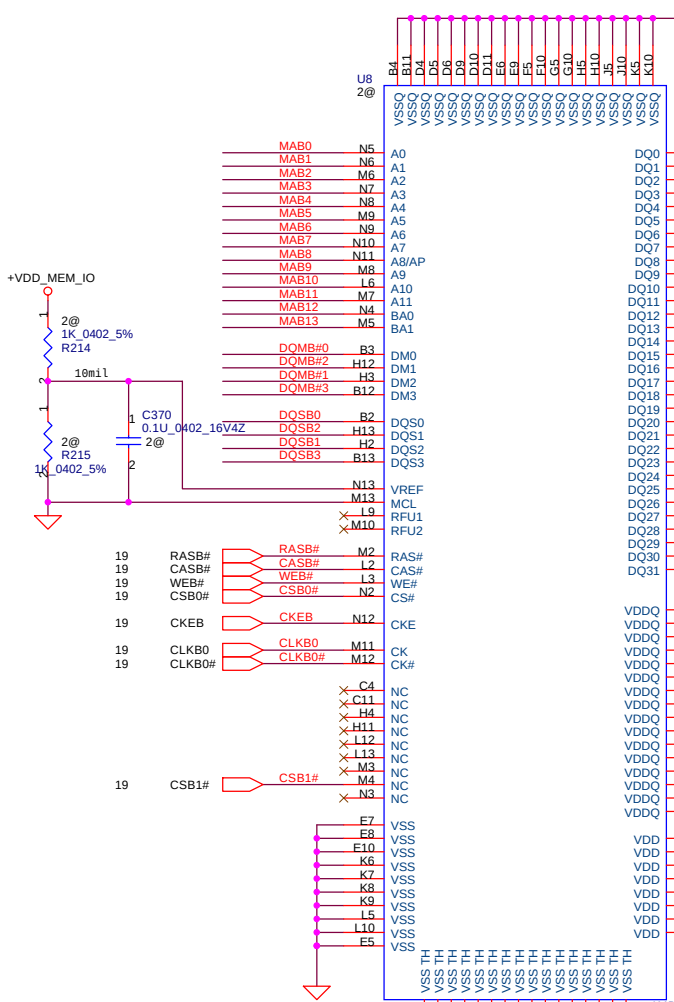
Place close to U6

Place close to U7

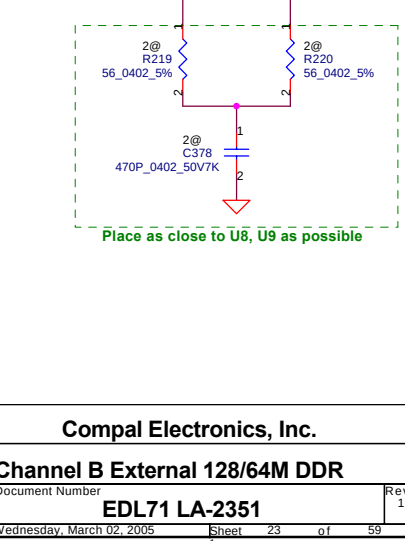
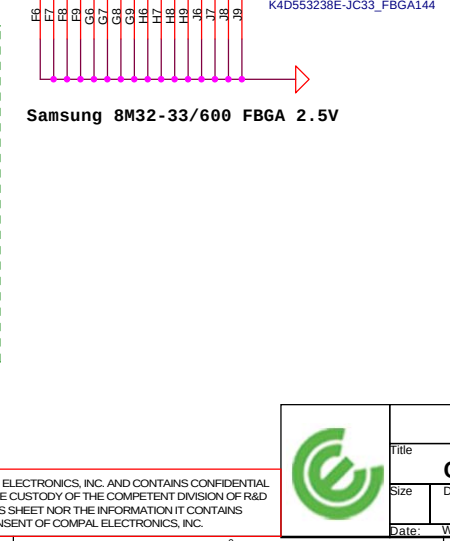
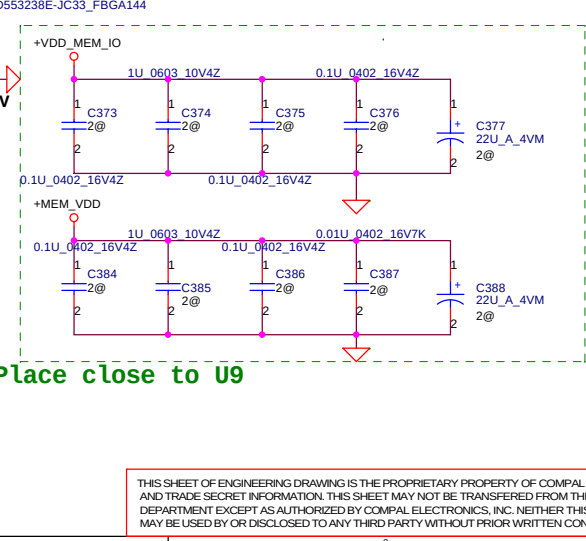
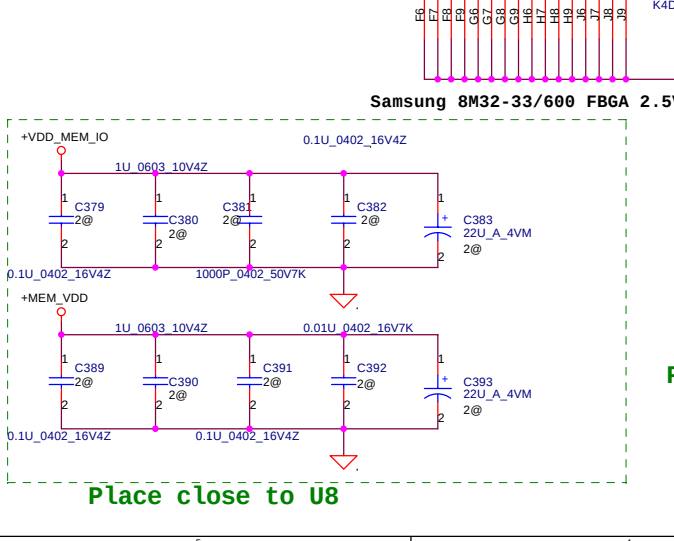
Place as close to U6, U7 as possible

Place as close to U6, U7 as possible

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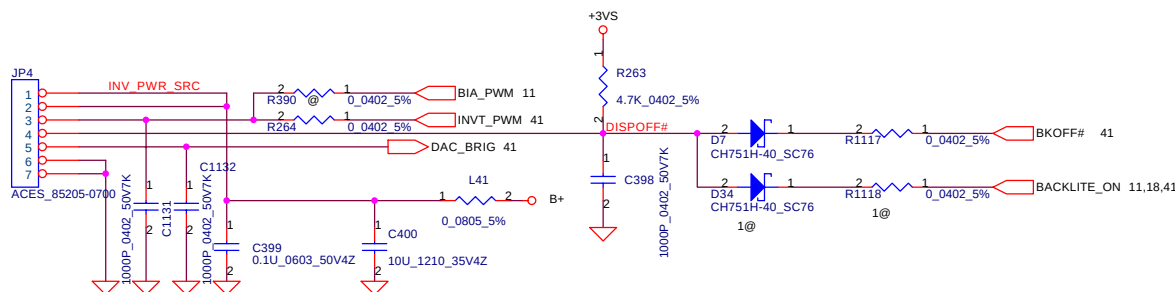
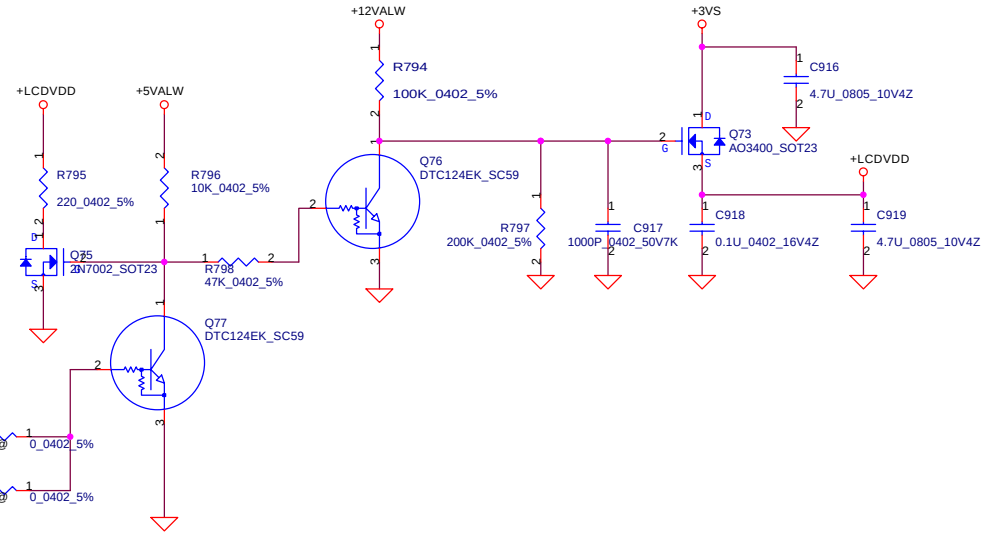
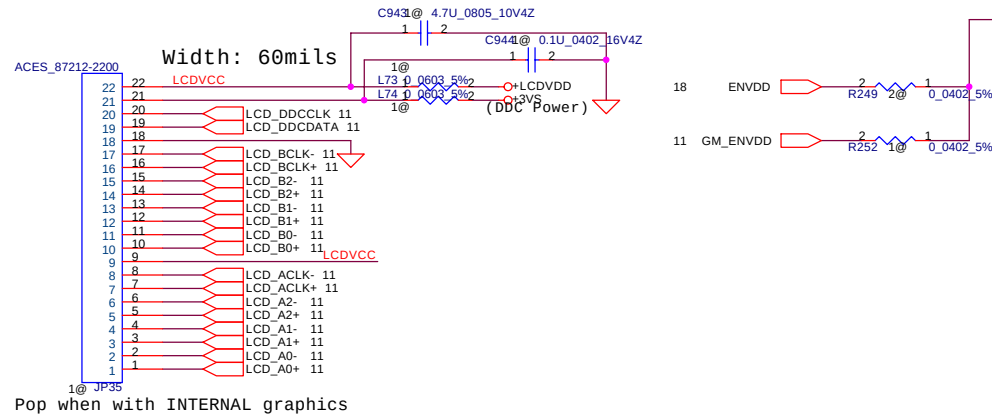
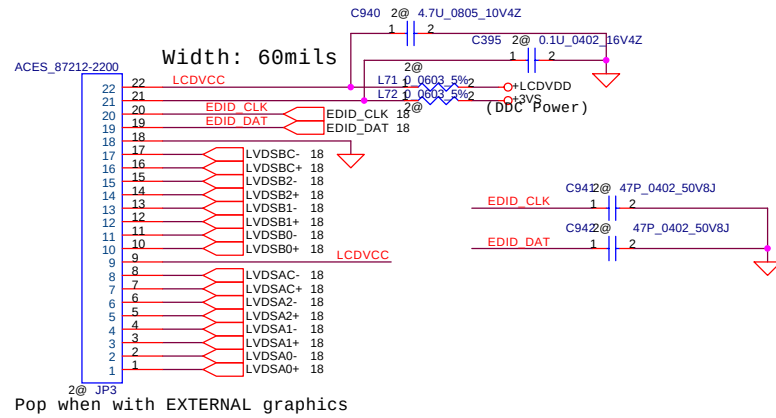


- 19 DQMB#[7:0] DQMB#[7:0]
- 19 MAB[13:0] MAB[13:0]
- 19 DQSB#[7:0] DQSB#[7:0]
- 19 MDB[63:0] MDB[63:0]



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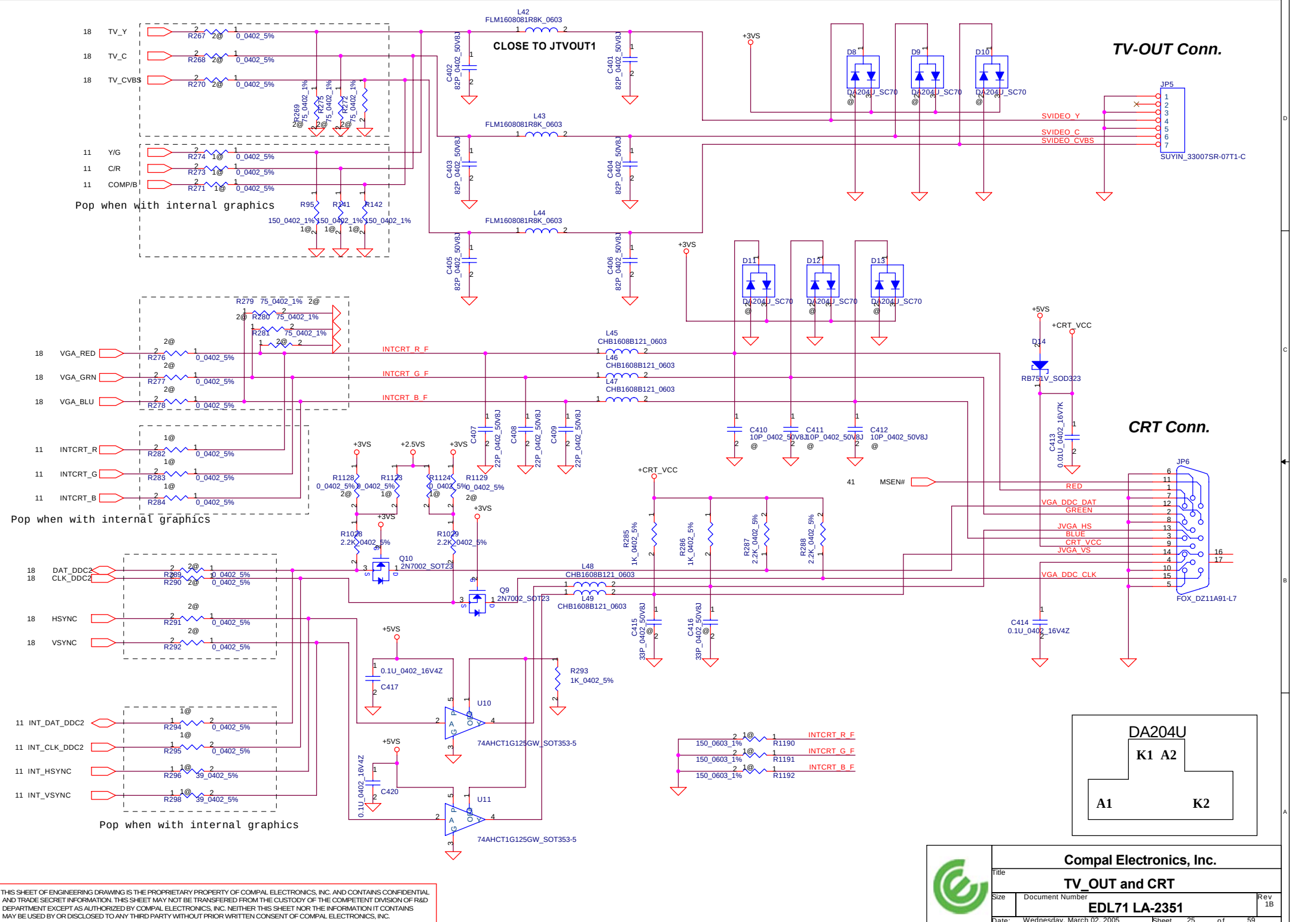
LCD CONN NOTE : place need to ASIC

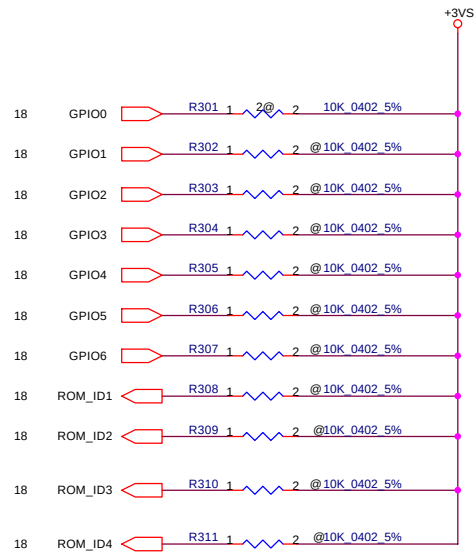


INVERTER CONN

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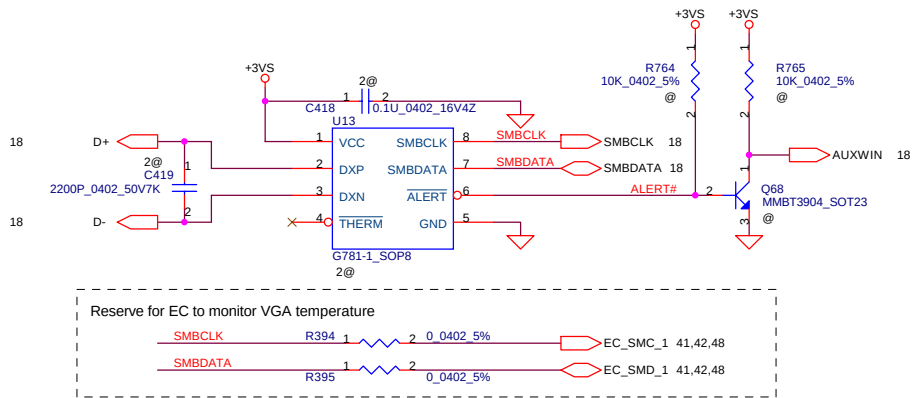
Compal Electronics, Inc.			
Title			
LVDS Connector			
Size	Document Number		Rev
	EDL71 LA-2351		1B
Date	Wednesday, March 02, 2005		Sheet 24 of 59



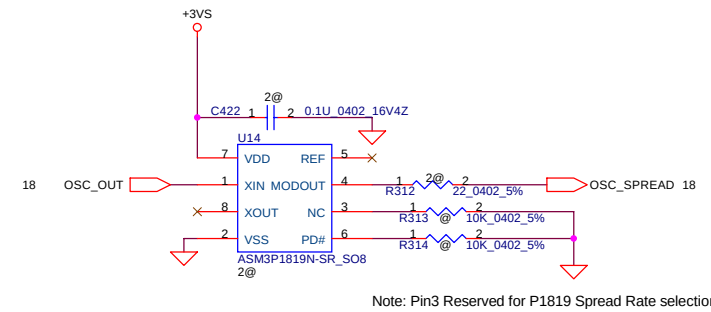


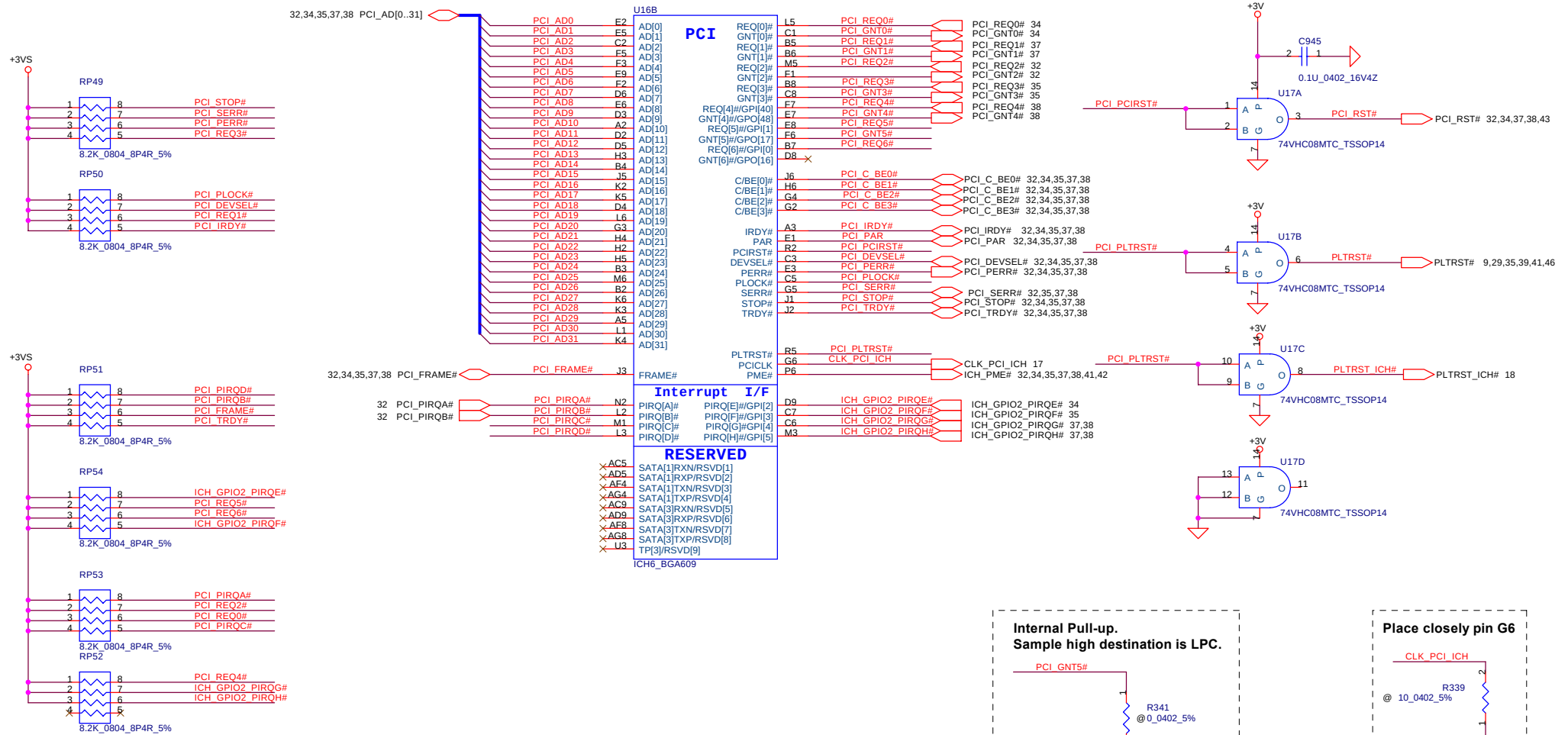
STRAPS	PIN	DESCRIPTION	DEFAULT
CAL_BG_BACKUP	GPIO0	PCI-EXPRESS CURRENT CALIBRATION BANDCAP BACKUP USING REFERENCE VOLTAGE FROM BANDGAP	0
PLL_CAL_FORCE_EN	GPIO1	PCI-EXPRESS FORCE PLL CALIBRATION DISABLED	0
PCIE_MODE(1:0)	GPIO(3:2)	PCI-EXPRESS 1:0A MODE	00
CAL_OFF	GPIO4	ENABLE TURN OFF PCI-EXPRESS IMPEDENCE/STRENGTH CALIBRATION	0
BYPASS_PLL	GPIO5	BYPASS PCI-EXPRESS PLL	0
ICOMP	GPIO6	NORMAL PCI-EXPRESS TRANSMITTER CURRENT COMPENSATION	0
DEBUG_ACCESS	GPIO8	DEBUG SIGNALS NOT BROUGHT OUT	0
ROMIDCFG(3:0)	ROMID (4:1)	SERIAL M25P10 ROM	1011

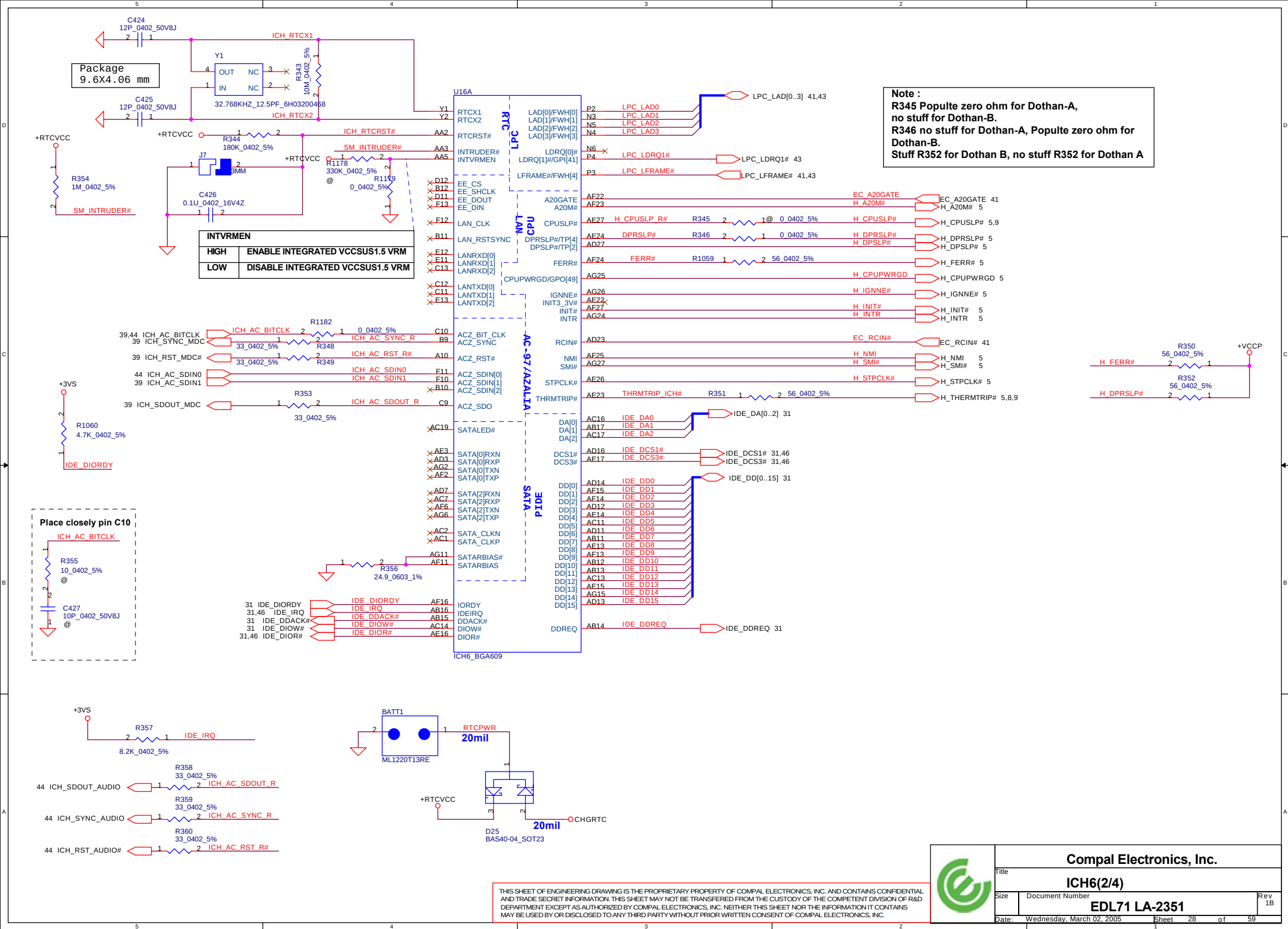
THERMAL SENSOR Theraml Chip for M24P only

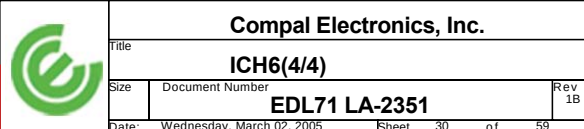


DDR SPREAD SPECTRUM



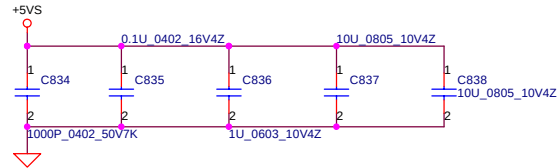
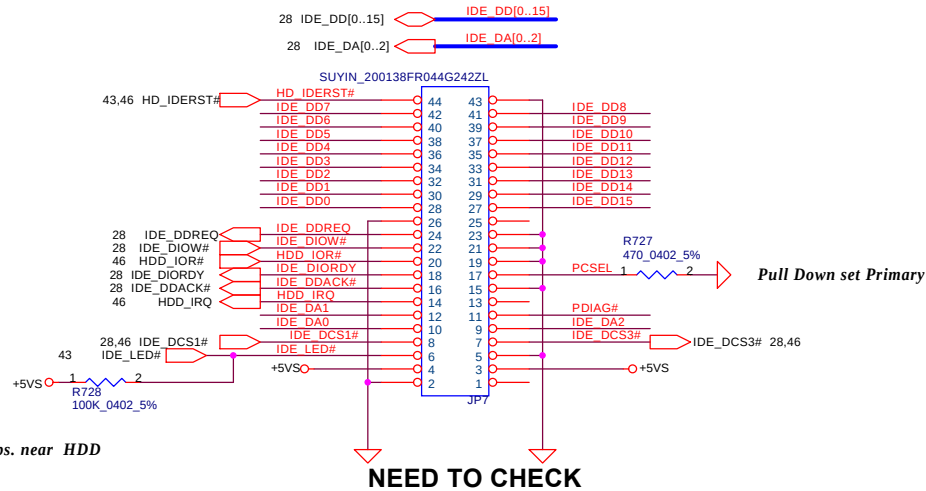




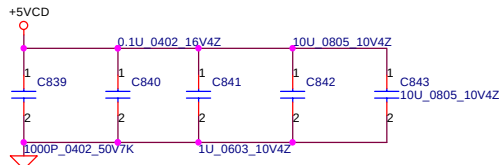
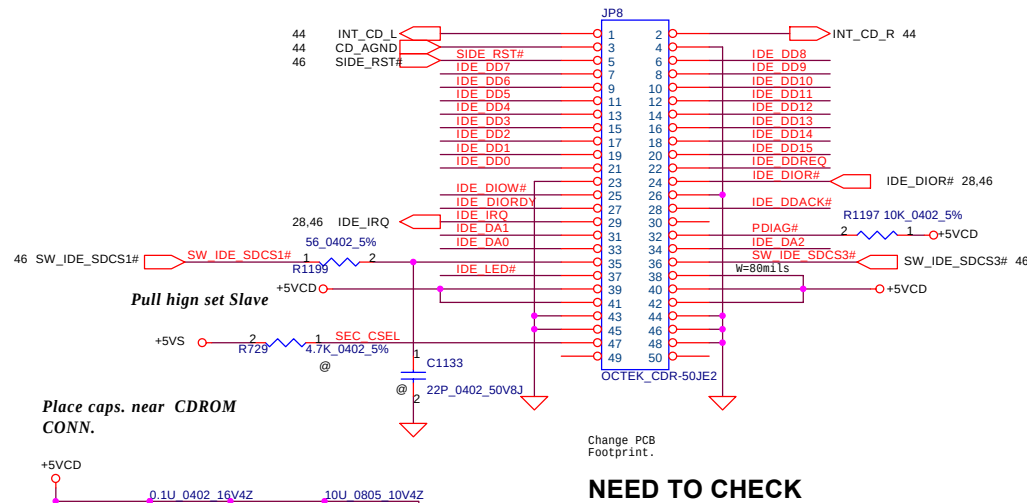


HDD Connector

HDD FOOTPRINT ERROR

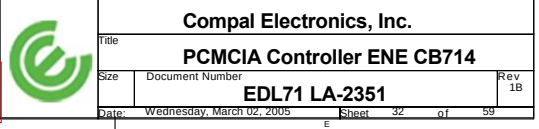


CD-ROM Connector

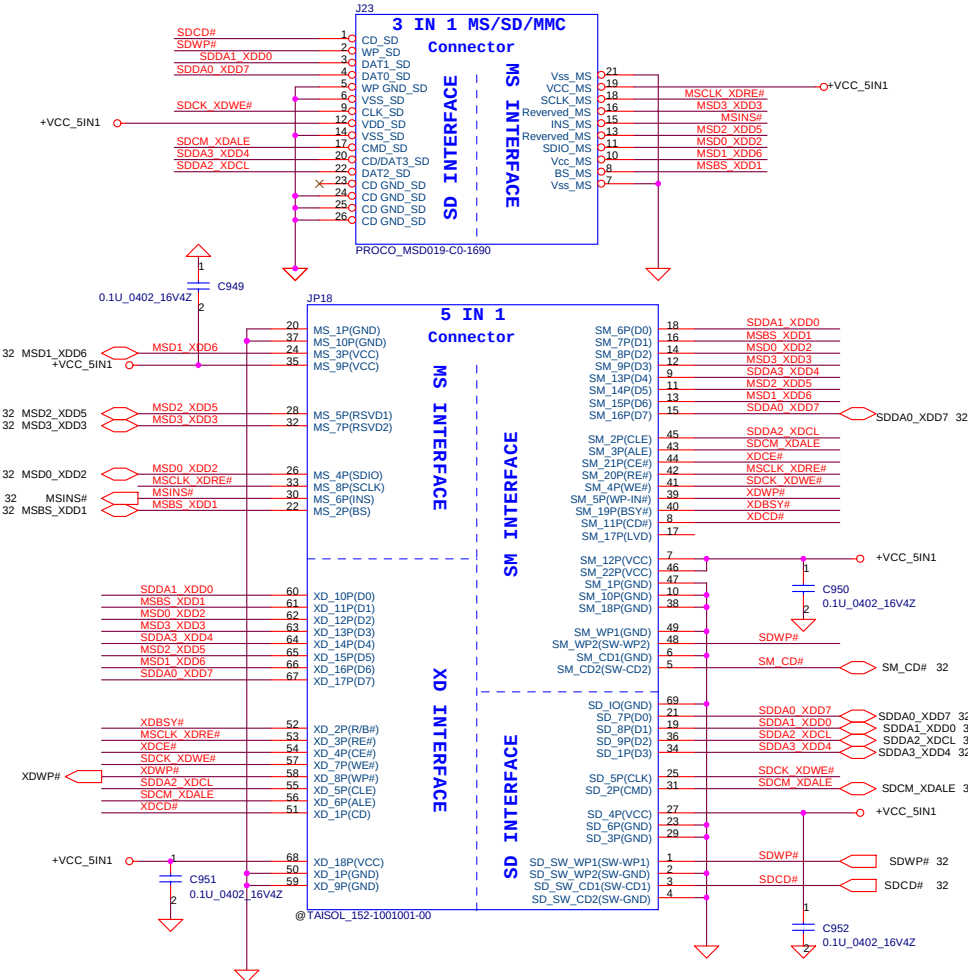
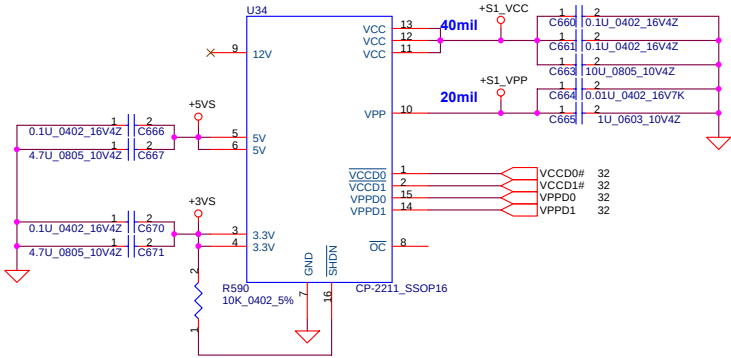


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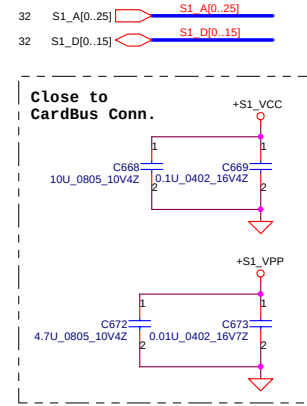
Compal Electronics, Inc.			
Title			
IDE CONNECTOR			
Size	Document Number		Rev
	EDL71 LA-2351		1B
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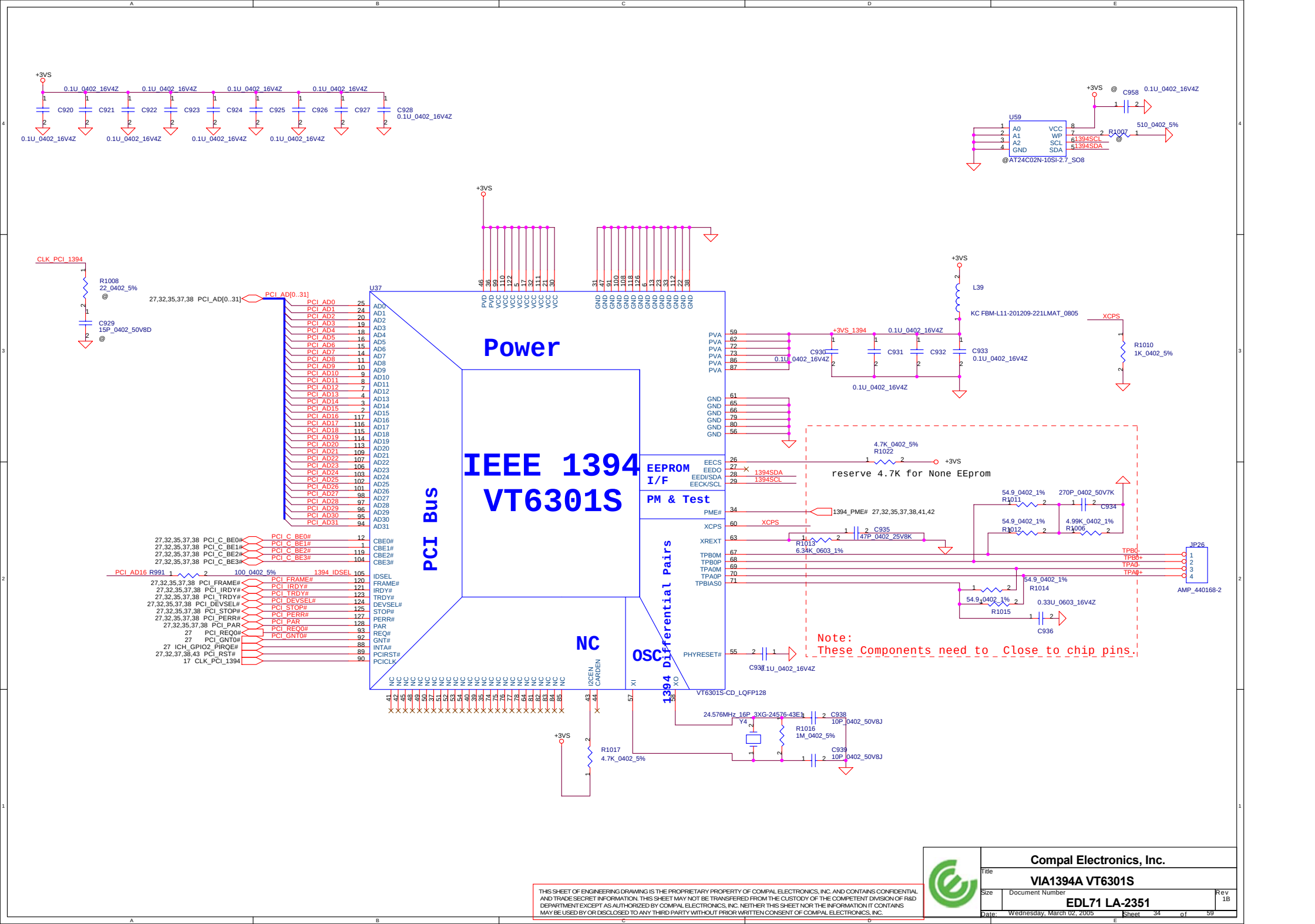


PCMCIA Power Controller



CardBus Socket

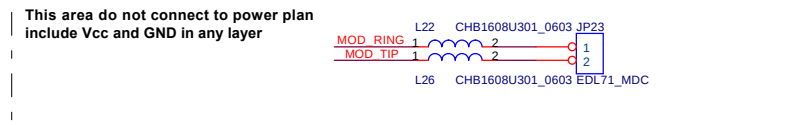
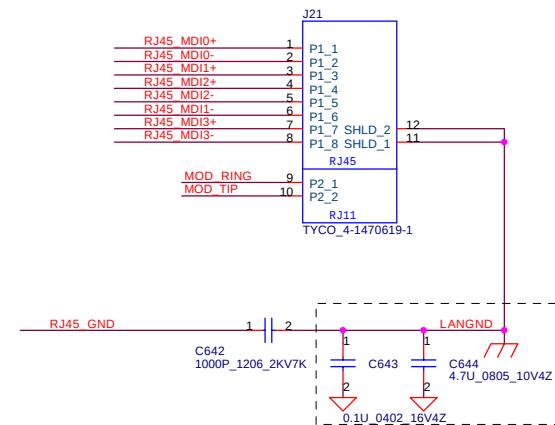
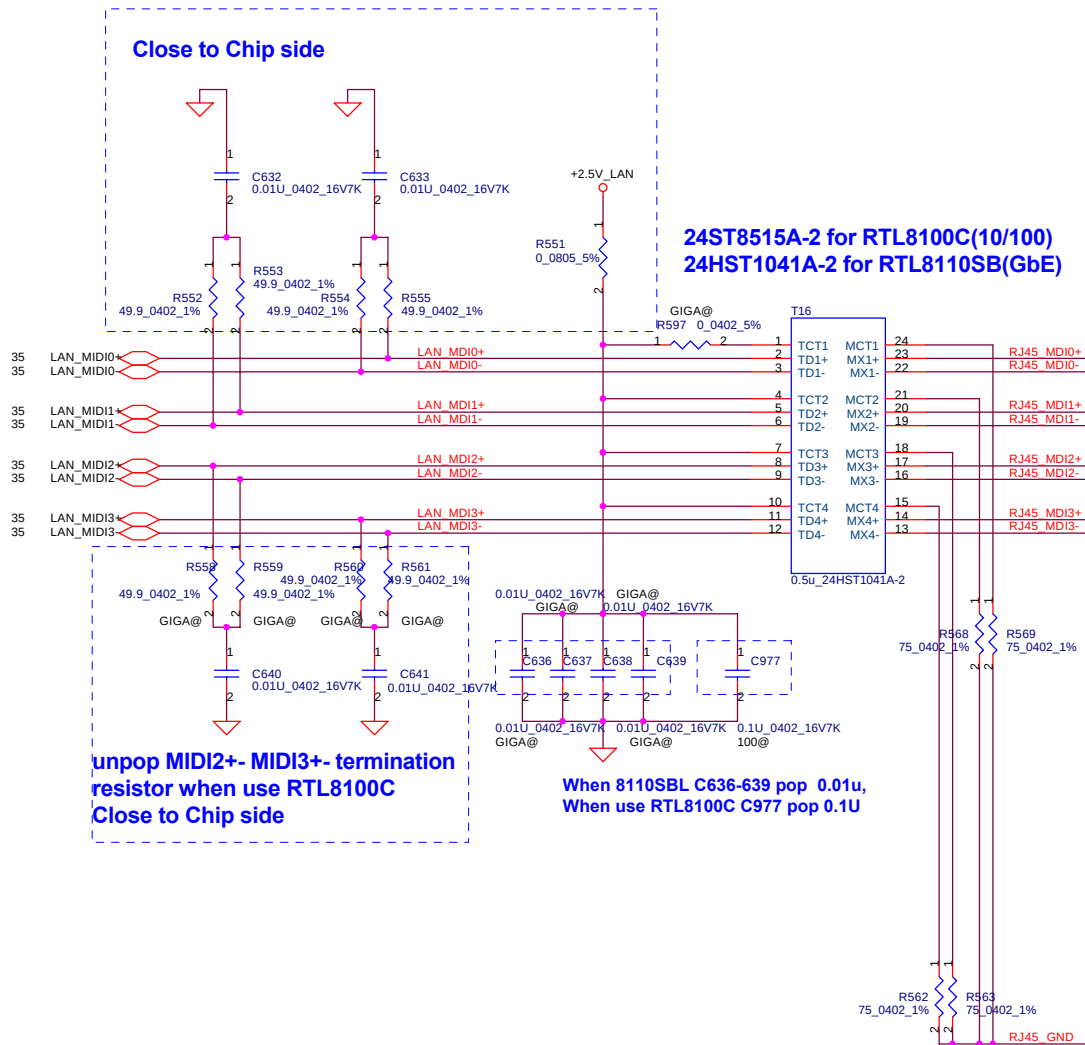


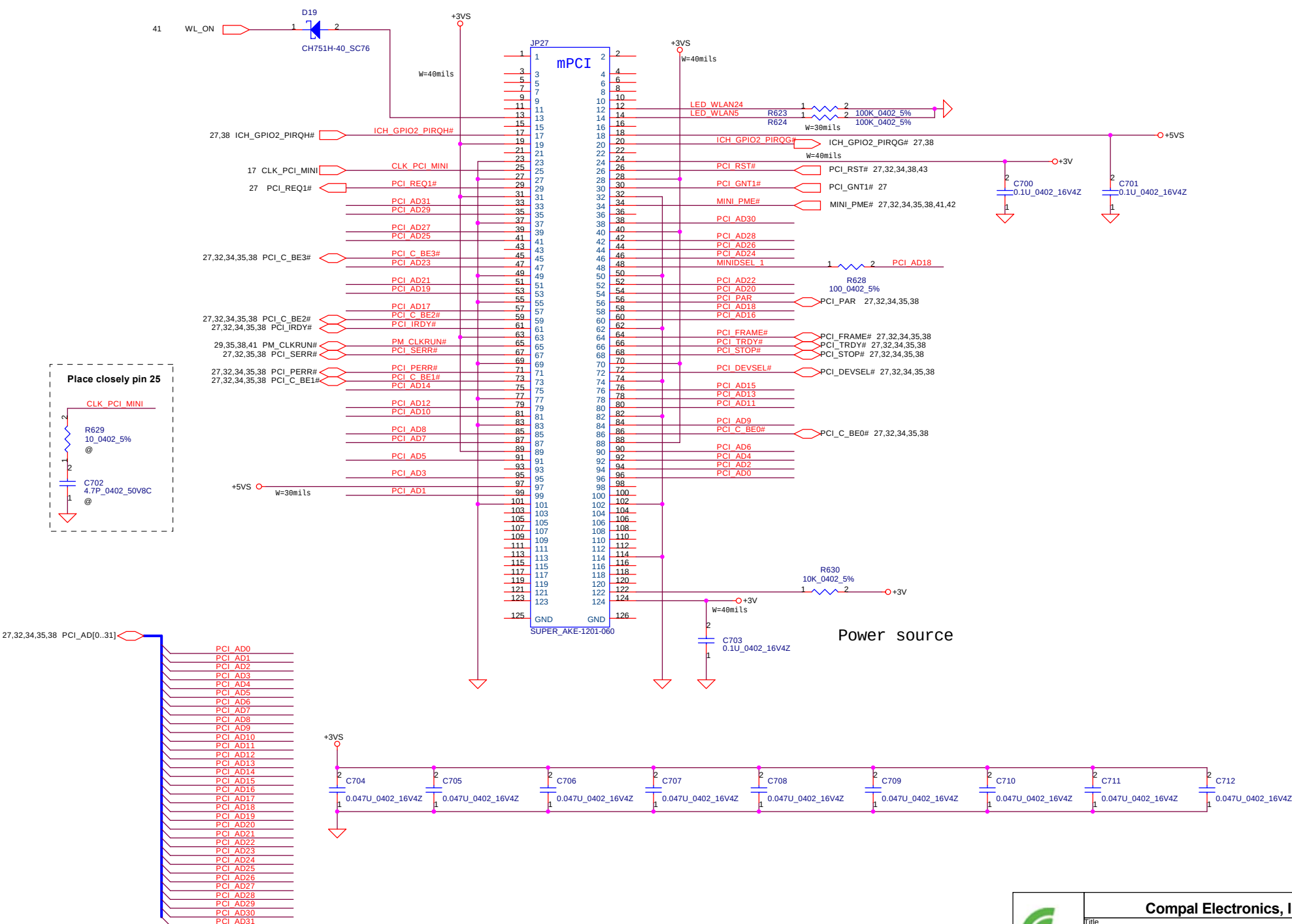


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Date:	Wednesday, March 02, 2005	Sheet 35 of 59



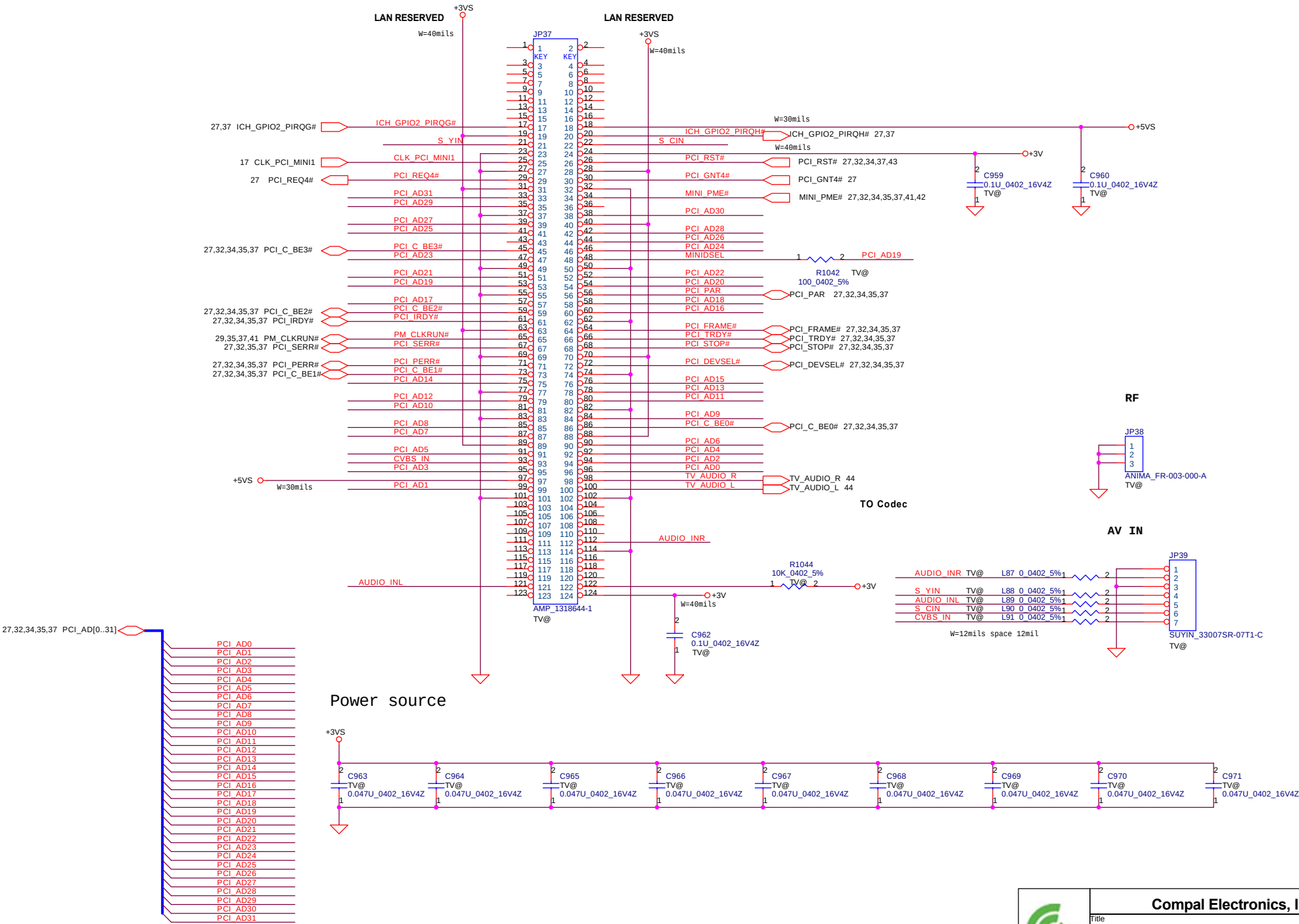
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Compal Electronics, Inc.			
Title MINIPCI			
Size	Document Number EDL71 LA-2351		
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Sheet	37	of	59
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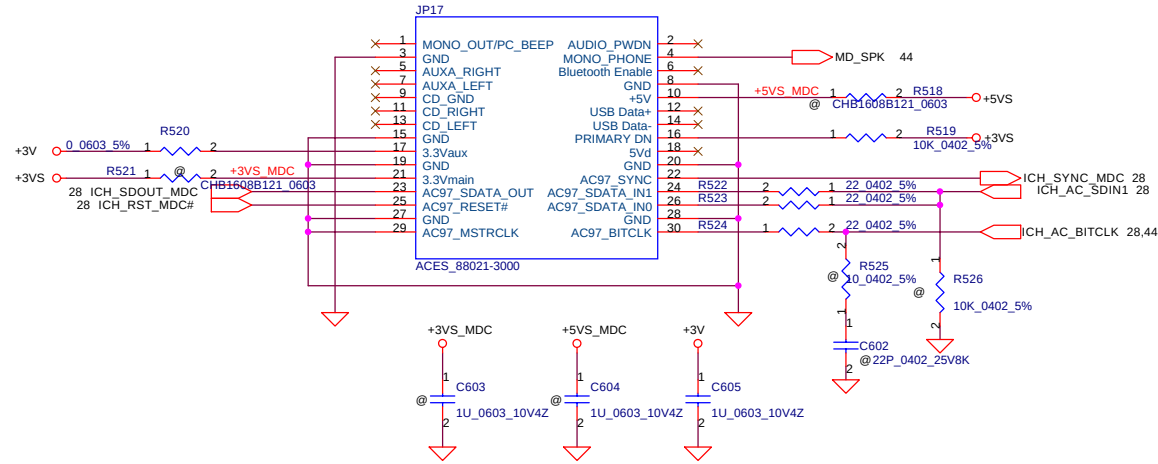


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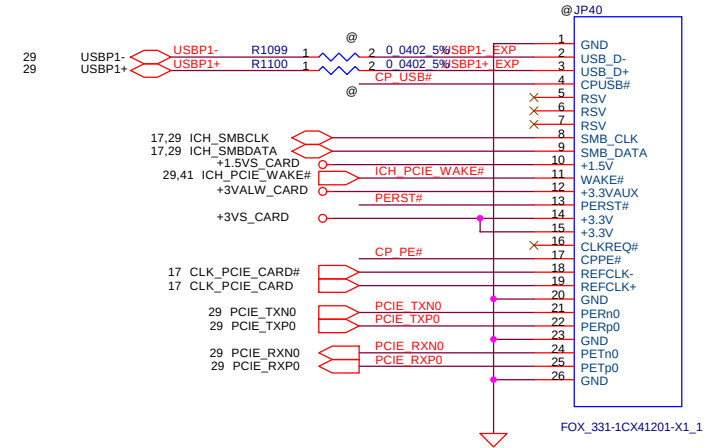


Compal Electronics, Inc.			
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		EDL71 LA-2351	
Date:		Wednesday, March 02, 2005	Sheet 38 of 59
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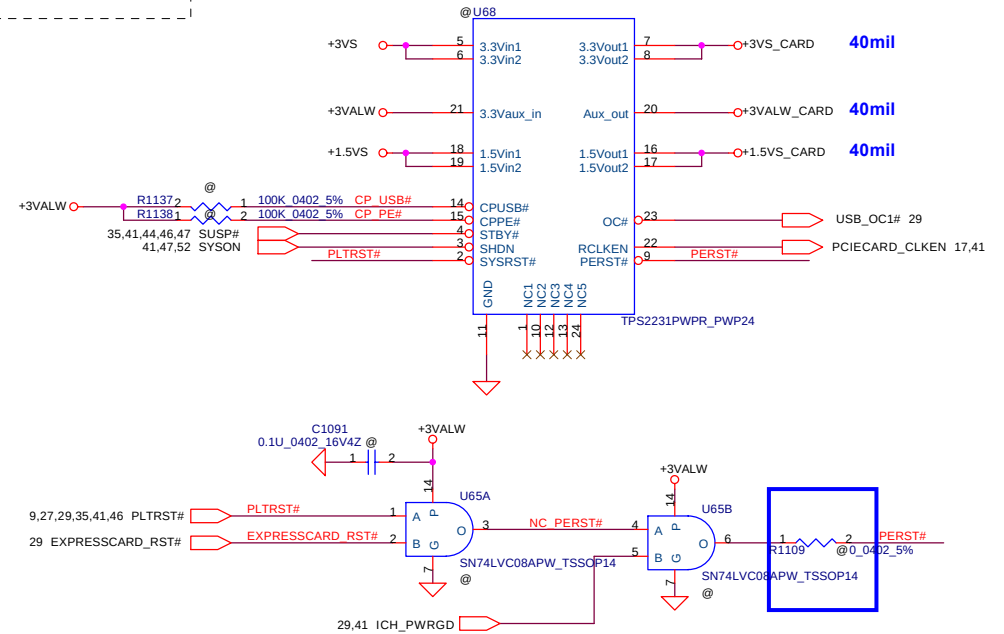
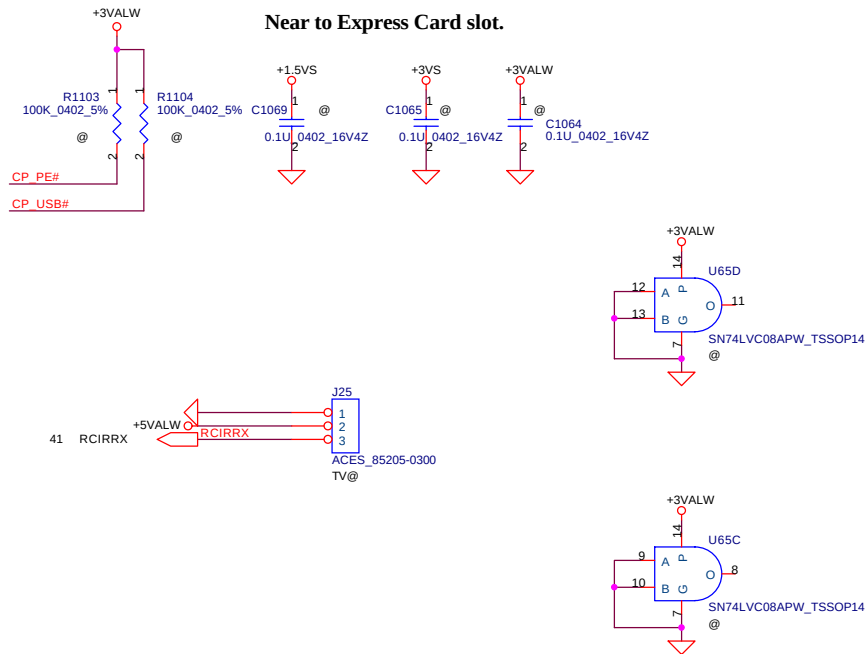
MDC Conn.



Express Card Conn.

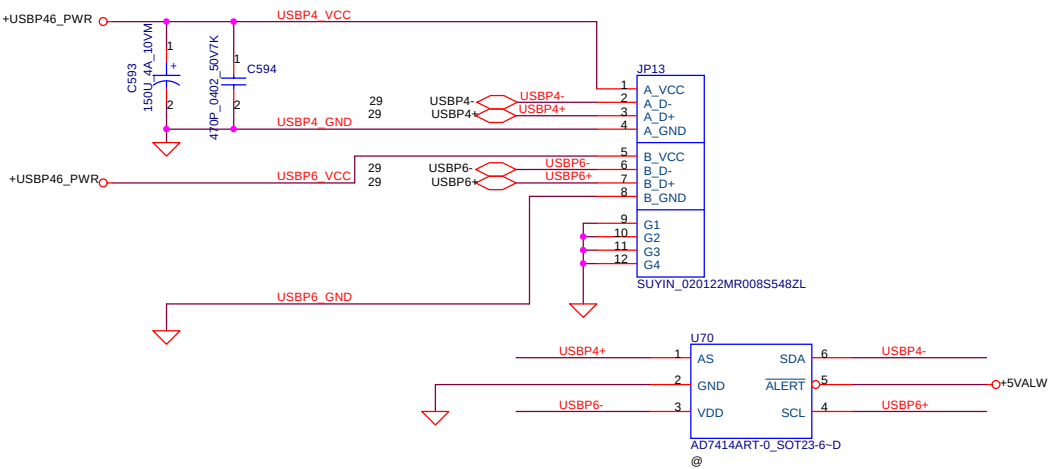
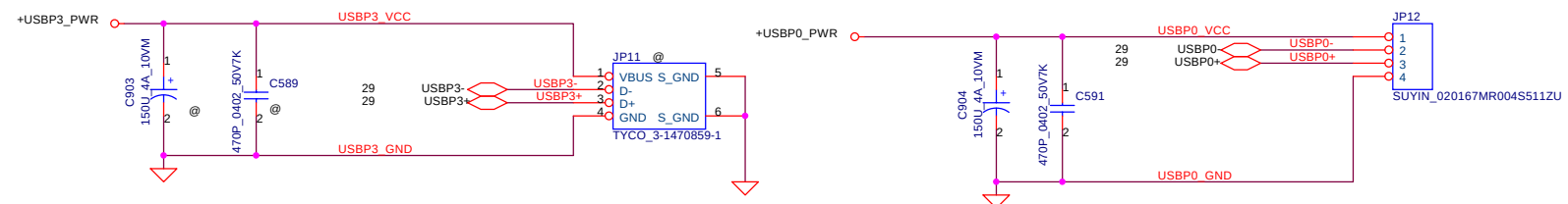


Near to Express Card slot.

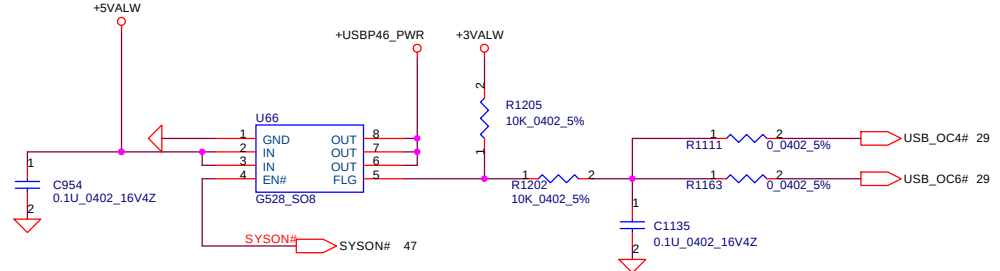


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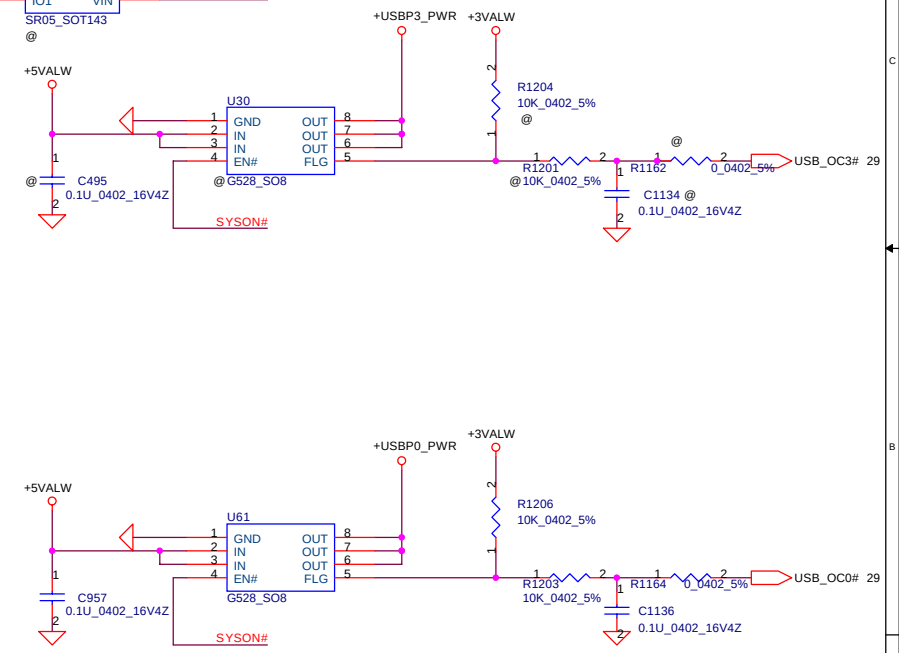
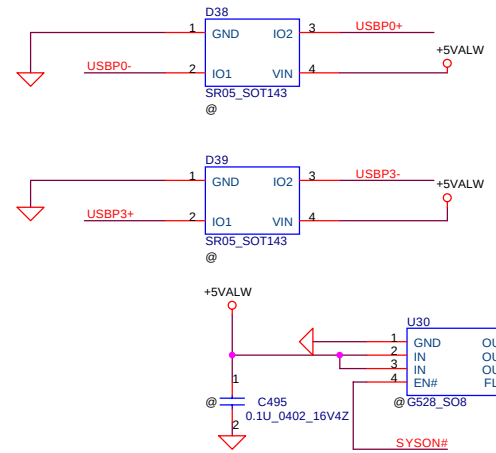
Compal Electronics, Inc.			
MDC Express Card Conn.			
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USB Over Current



Note:
USB_AS=USB_BS=Trace width=40mils



USB PORT#	DESTINATION
0	JUSB1 (JP12)
1	Express Card
2	JUSB2 (JP11)
3	Reserve
4	JUSB3 (JP13UP)
5	Reserve
6	JUSB3 (JP13LOW)
7	Reserve

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Compal Electronics, Inc.

Title

USB 2.0 Port

Size

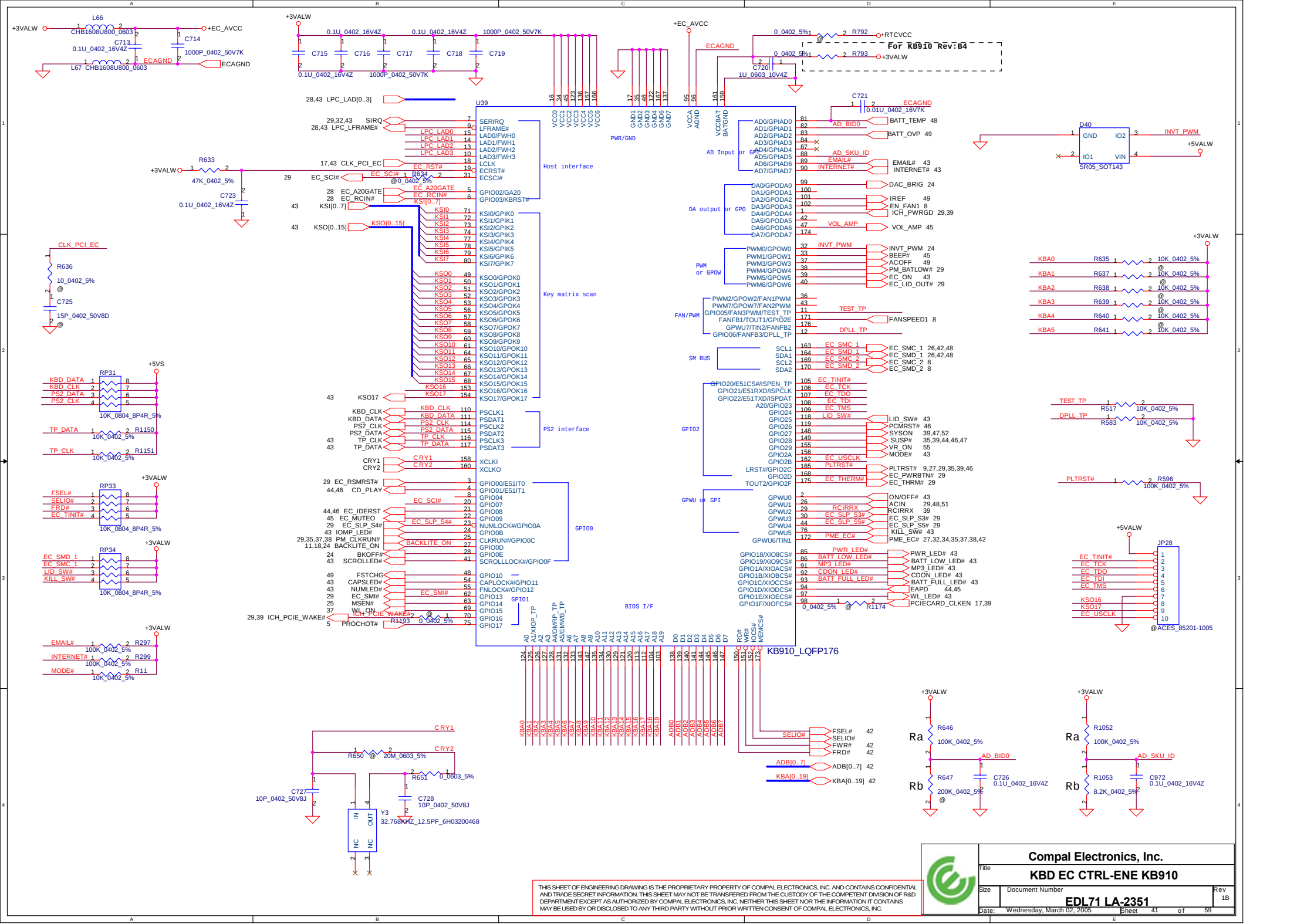
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EDL71 LA-2351

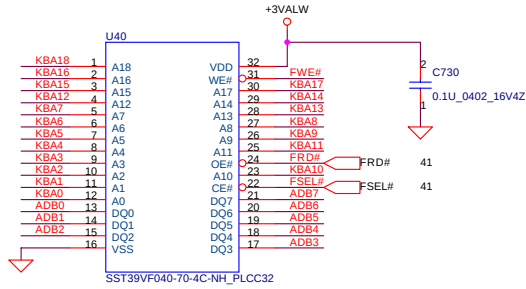
Rev 1B

Date: Wednesday, March 02, 2005

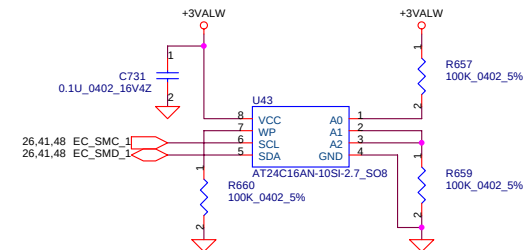
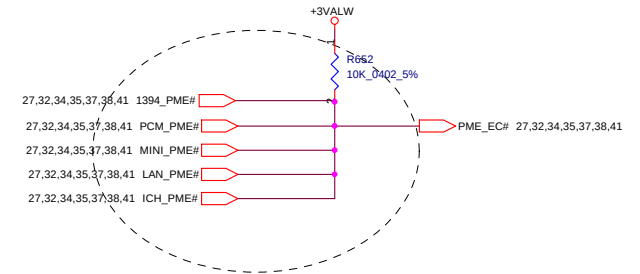
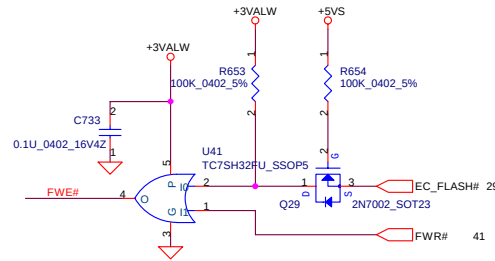
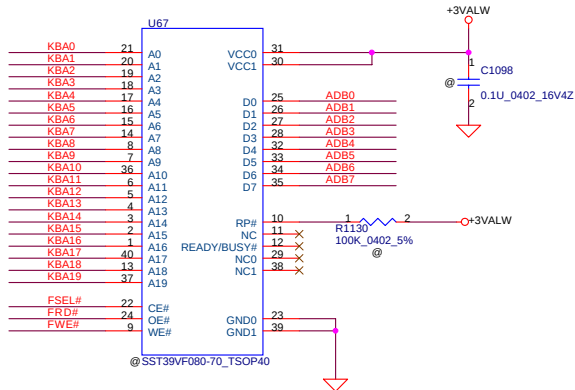
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41 ADB[0..7]  ADB[0..7]
41 KBA[0..19]  KBA[0..19]



1MB Flash ROM

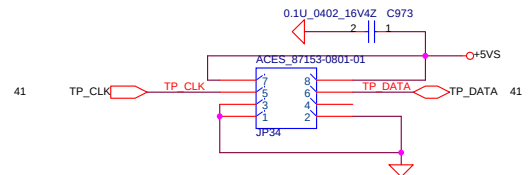
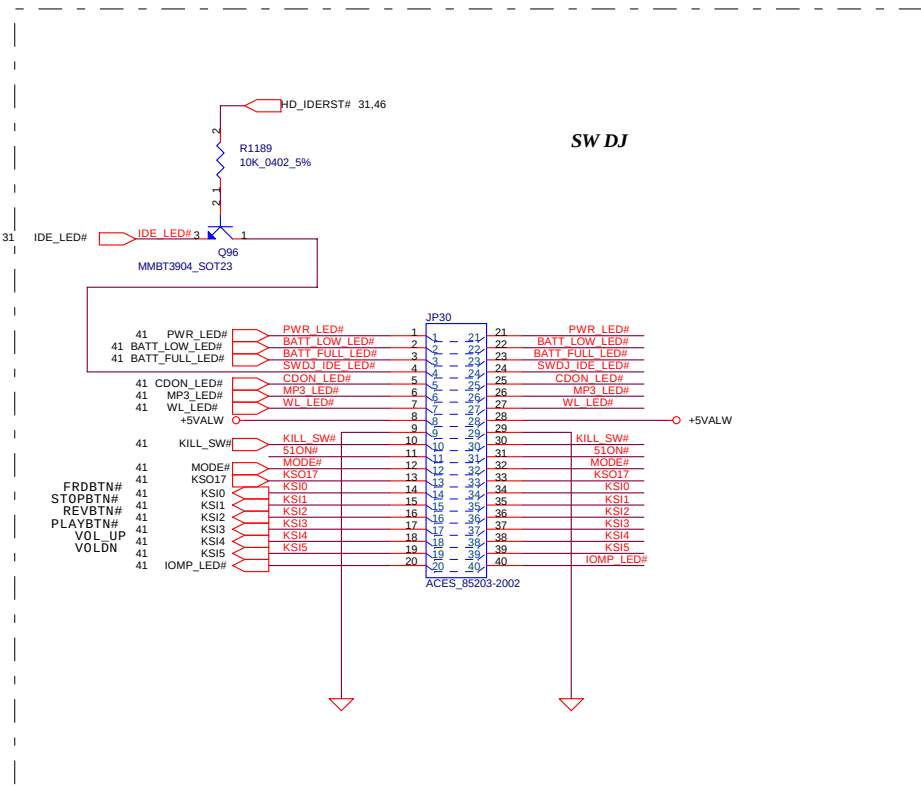
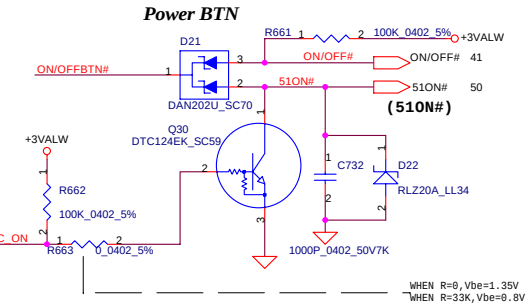
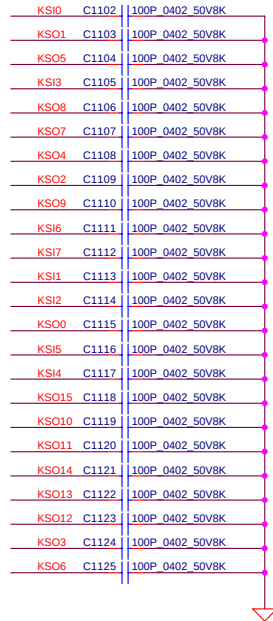


Compal Electronics, Inc.

Title			
BIOS & EC I/O Port			
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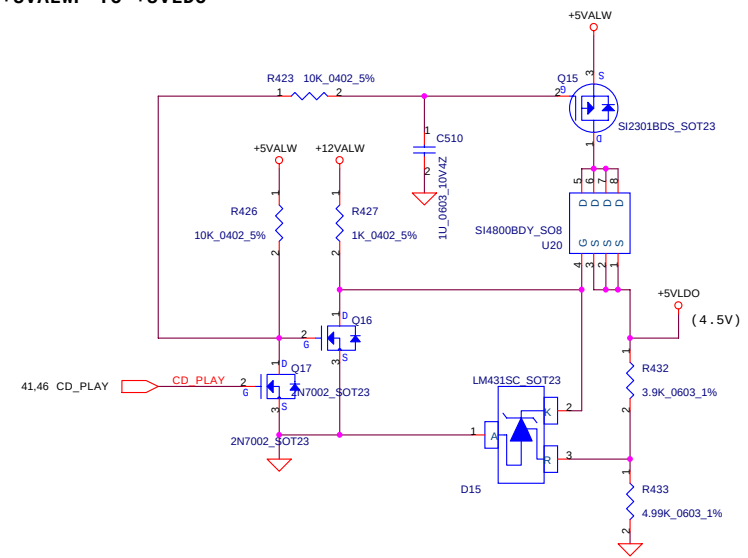
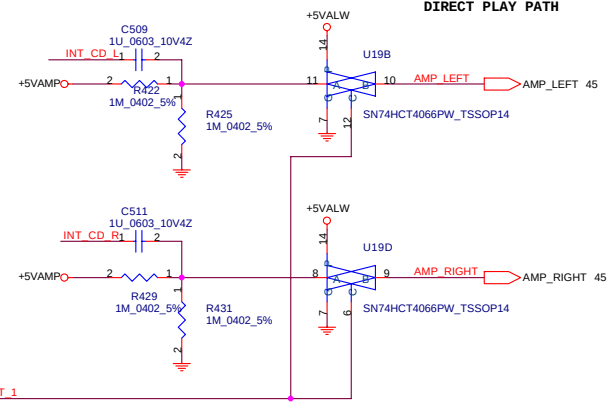
LID Switch



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The schematic diagram illustrates the CD L circuit. It features two input signals, INT_CD_L and INT_CD_R, which are connected to a network of resistors and capacitors. The circuit includes resistors R447, R448, R449, R450, and R452, and capacitors C542 and C543. The output is labeled CD L. The circuit is powered by a 5V supply and ground.

Key components and connections:

- Inputs:** INT_CD_L and INT_CD_R (both labeled 31).
- Resistors:**
 - R447: 20K, 0402_1%
 - R448: 20K, 0402_1%
 - R449: 20K, 0402_1%
 - R450: 6.8K, 0402_5%
 - R452: 6.8K, 0402_5%
- Capacitors:**
 - C542: 1u, 0603_10V4Z
 - C543: 1u, 0603_10V4Z
- Output:** CD L (labeled 2).
- Power:** 5V supply and ground.

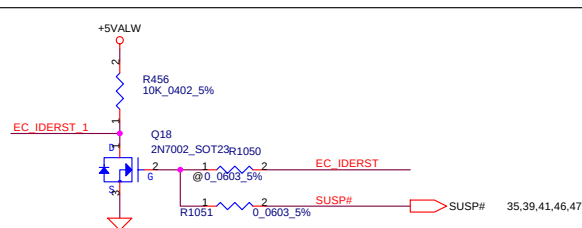
31 CD_AGNND

20K_0402_1% R454

CD_GNA

R799 0.0603_5%

R455 6.8K_0402_5%

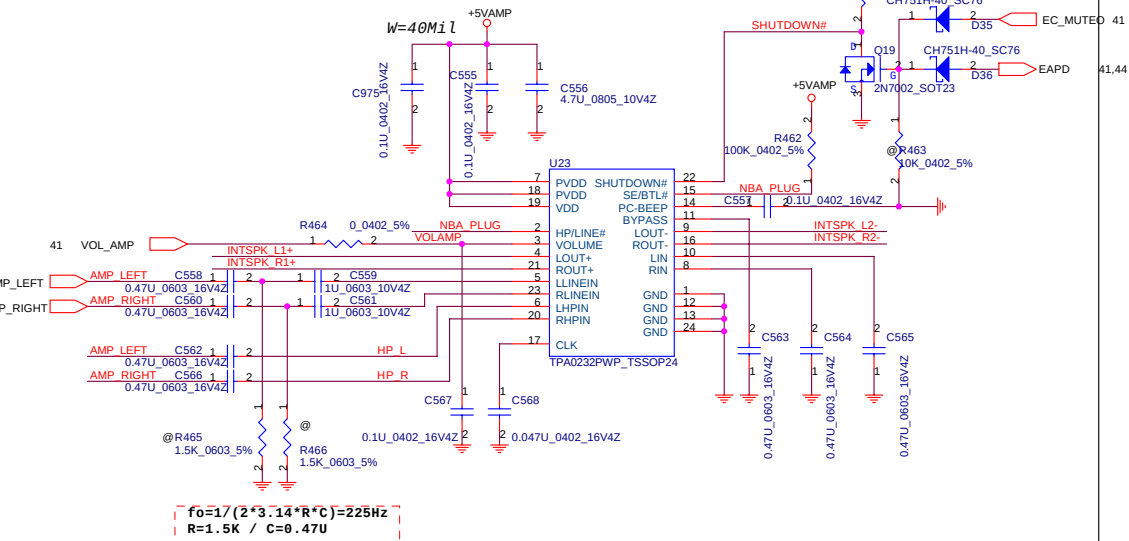


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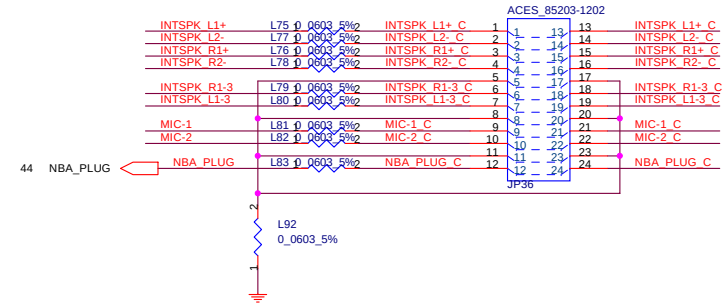


Compal Electronics, Inc.			
Title AC_Link-Codec			
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Audio Amplifier

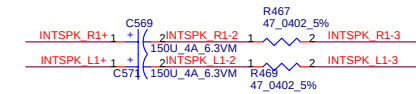


Left Speaker Connector Right Speaker Connector

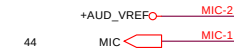


CHANGE CONN

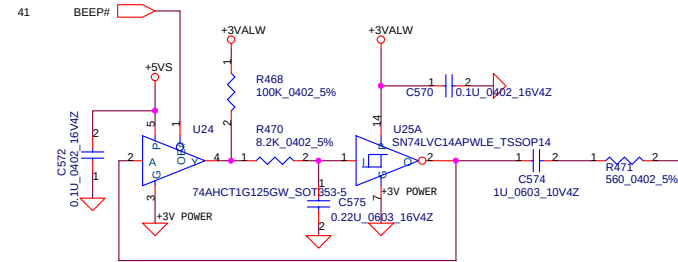
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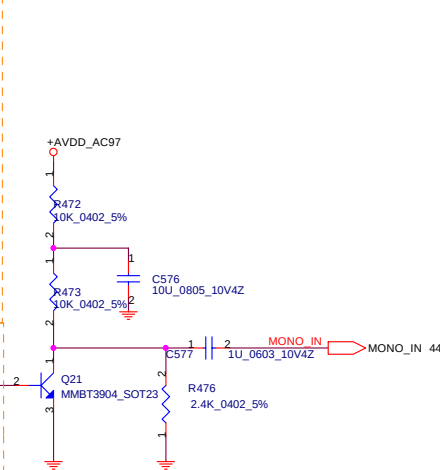
MICROPHONE IN JACK



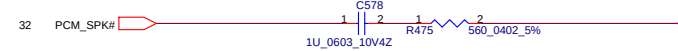
EC BEEP



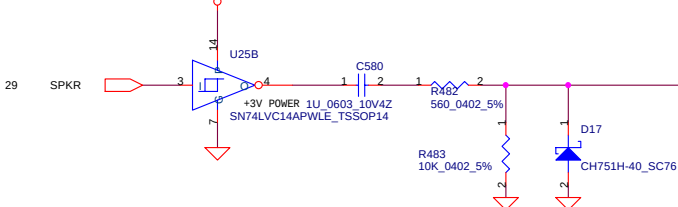
System BEEP To AC97' Codec



CardBus BEEP

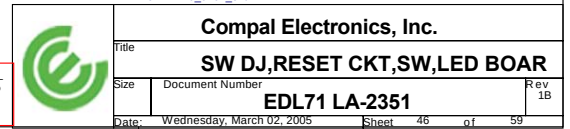
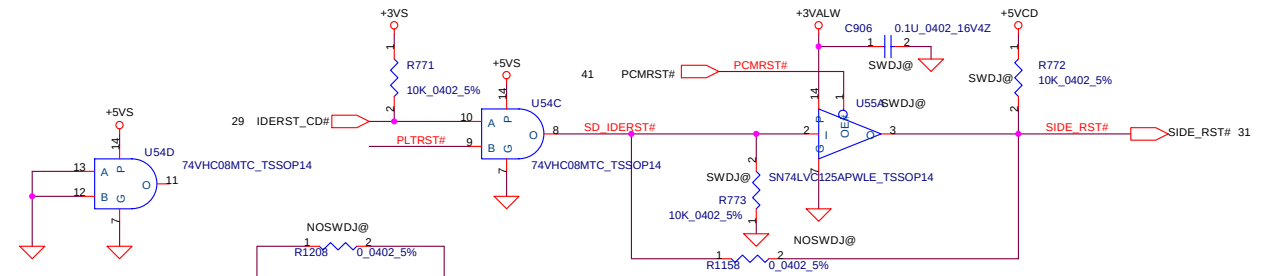
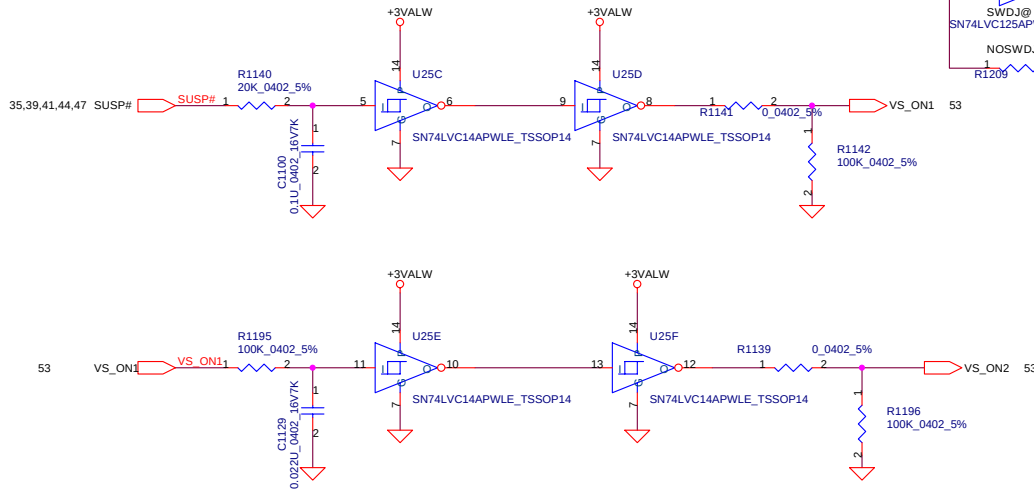


PCI BEEP

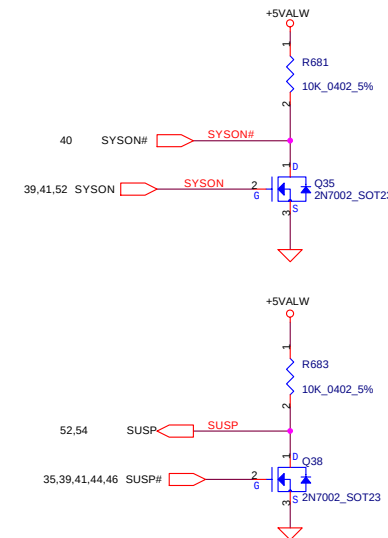
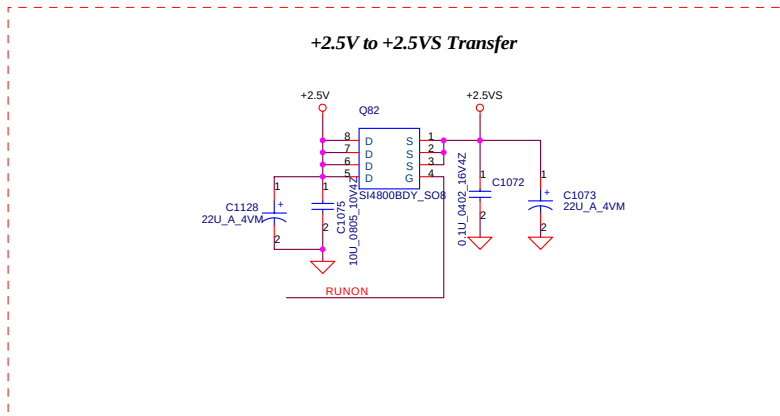
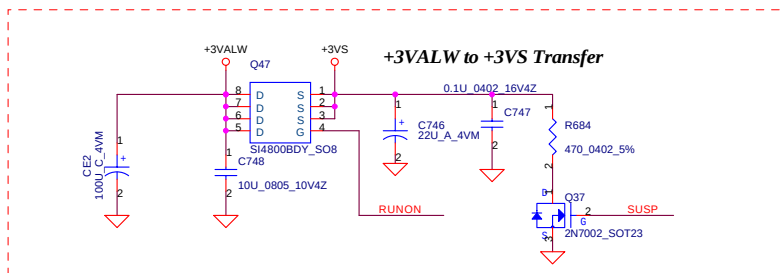
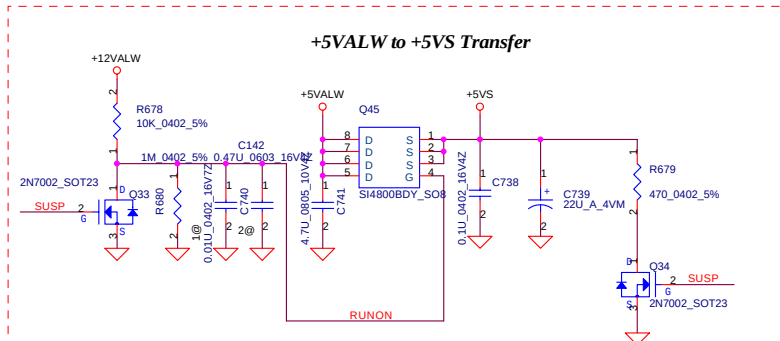
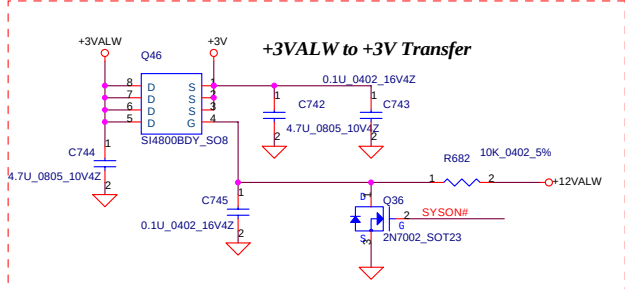
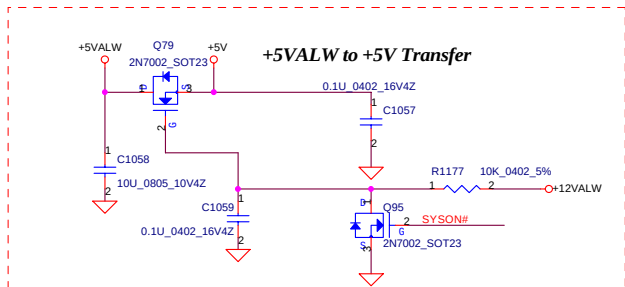


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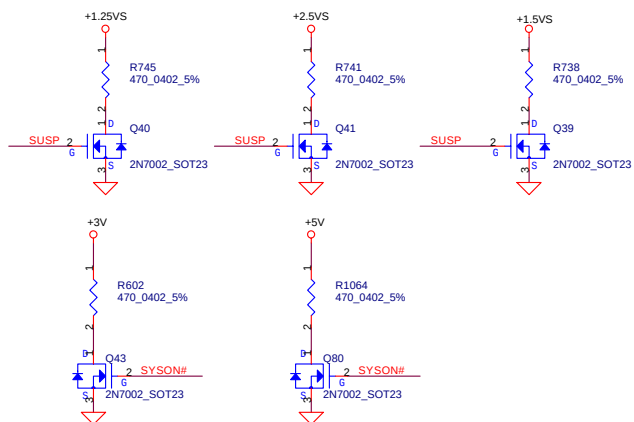
Compal Electronics, Inc.			
Title			
Audio_AMP&JACKs			
Size	Document Number	Rev 18	
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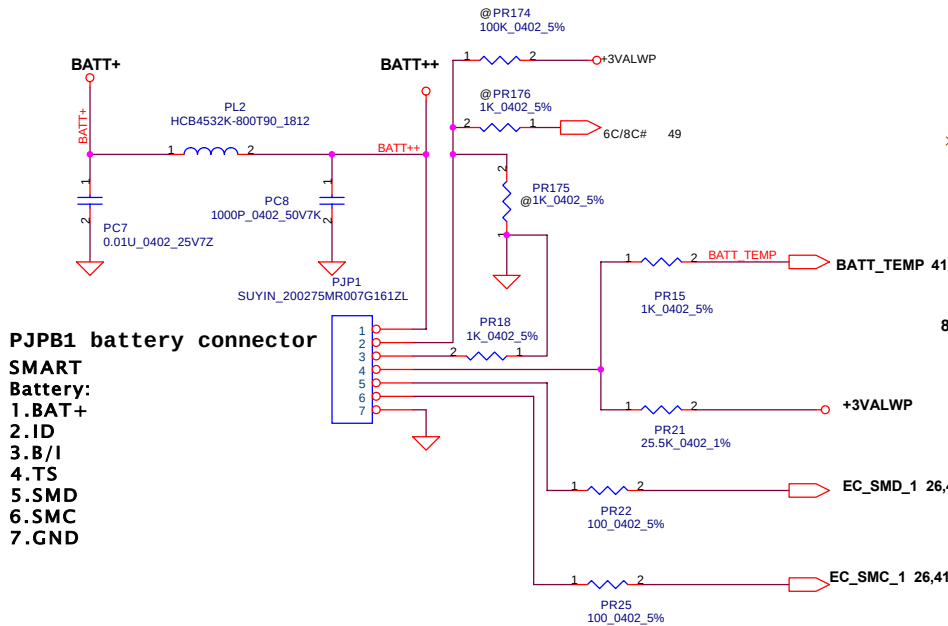
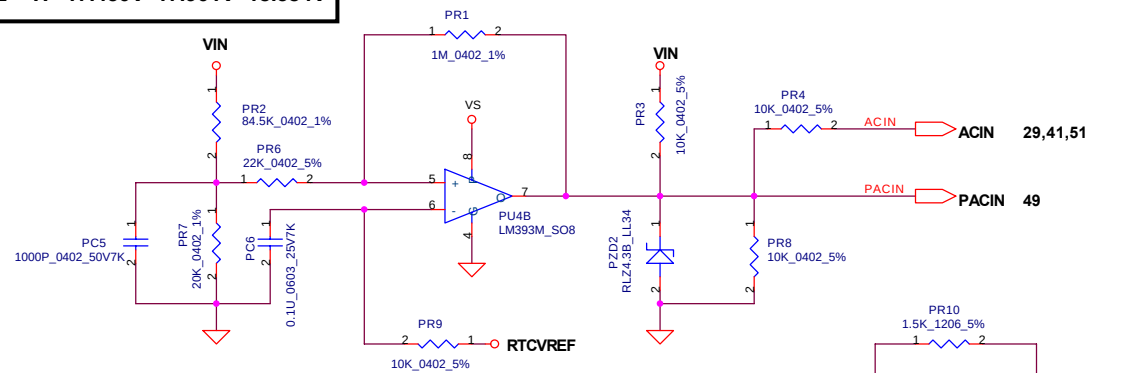
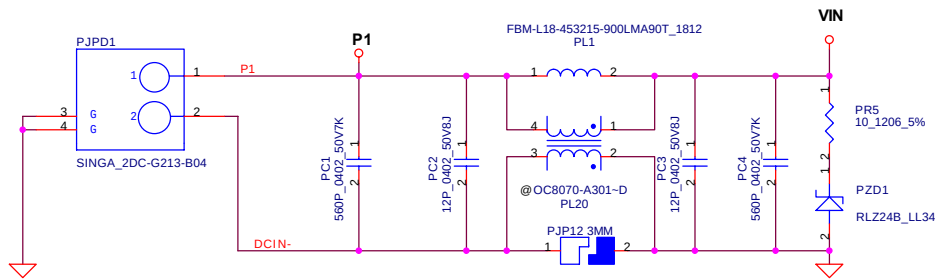
Discharge circuit



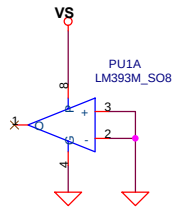
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Compal Electronics, Inc.			
Title			
DC/DC Circuits			
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	EDL71 LA2351	1B	
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Vin Detector			
	Min.	typ.	Max.
H->L	16.976V	17.257V	17.728V
L->H	17.430V	17.901V	18.384V



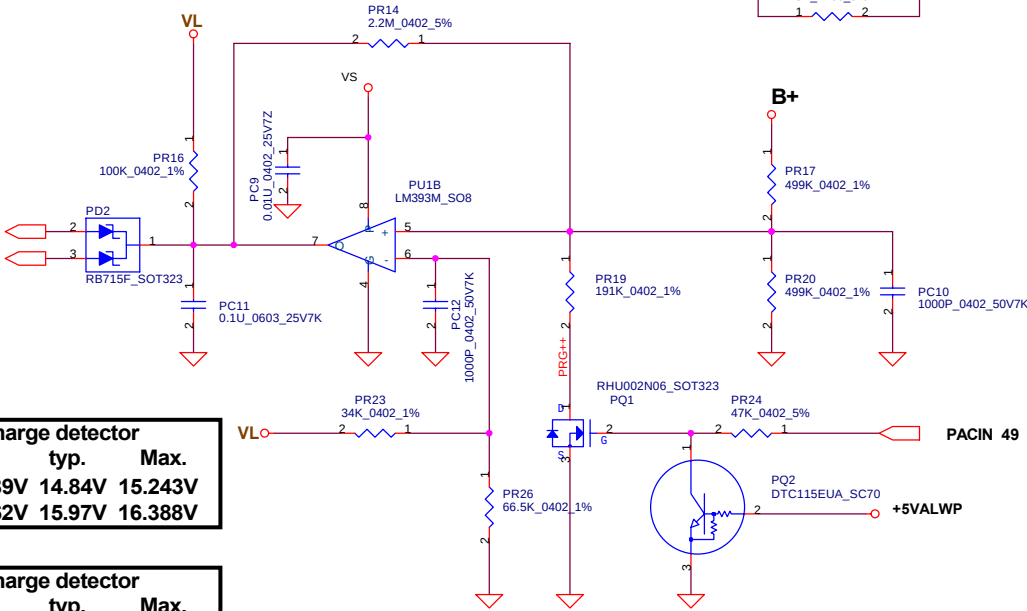
PJPB1 battery connector
SMART Battery:
 1.BAT+
 2.ID
 3.B/I
 4.TS
 5.SMD
 6.SMC
 7.GND



8,50,51 MAINPWON
 49 ACON

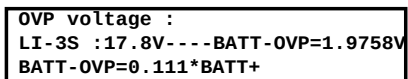
ACIN			
Precharge detector			
	Min.	typ.	Max.
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

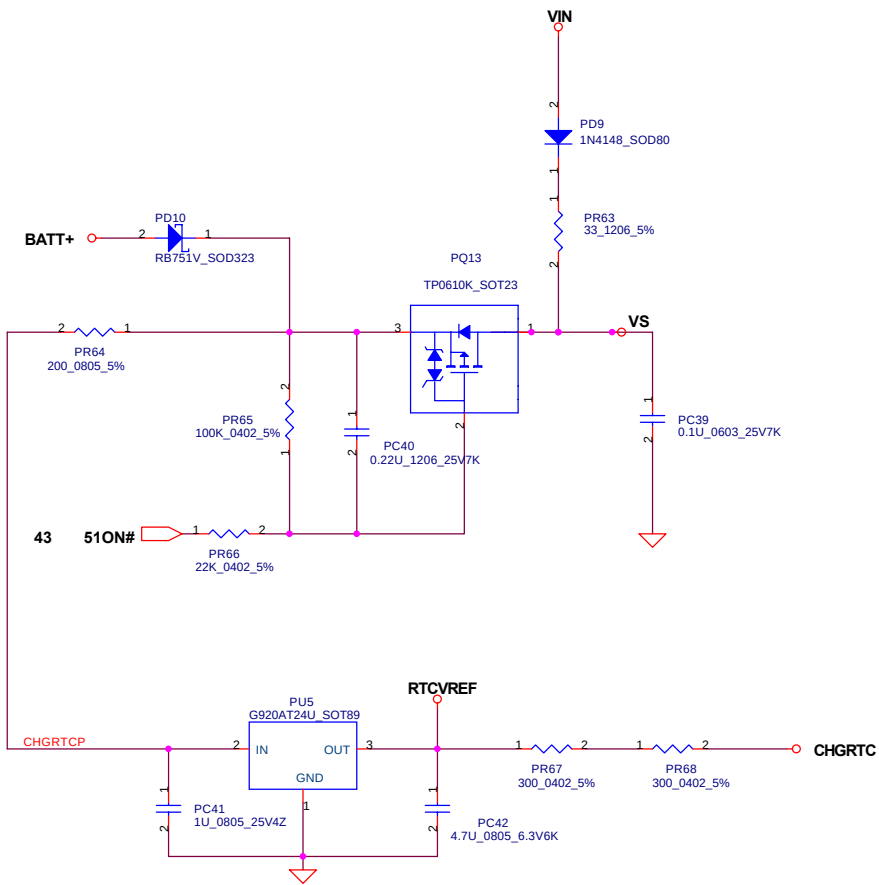
BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V



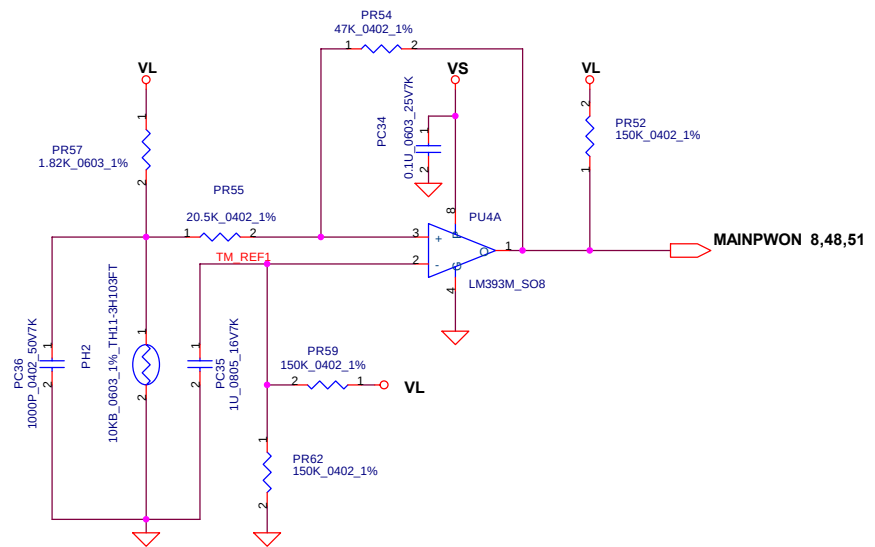
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Compal Electronics, Inc.			
Title			
DCIN & DETECTOR & Precharge			
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PH2 under CPU botten side :
 CPU thermal protection at 80 degree C
 Recovery at 44(45) degree C



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Compal Electronics, Inc.			
Title		RTC Battery & OTP	
Size	Document Number	Rev	
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+3.3V/+5V/+12V

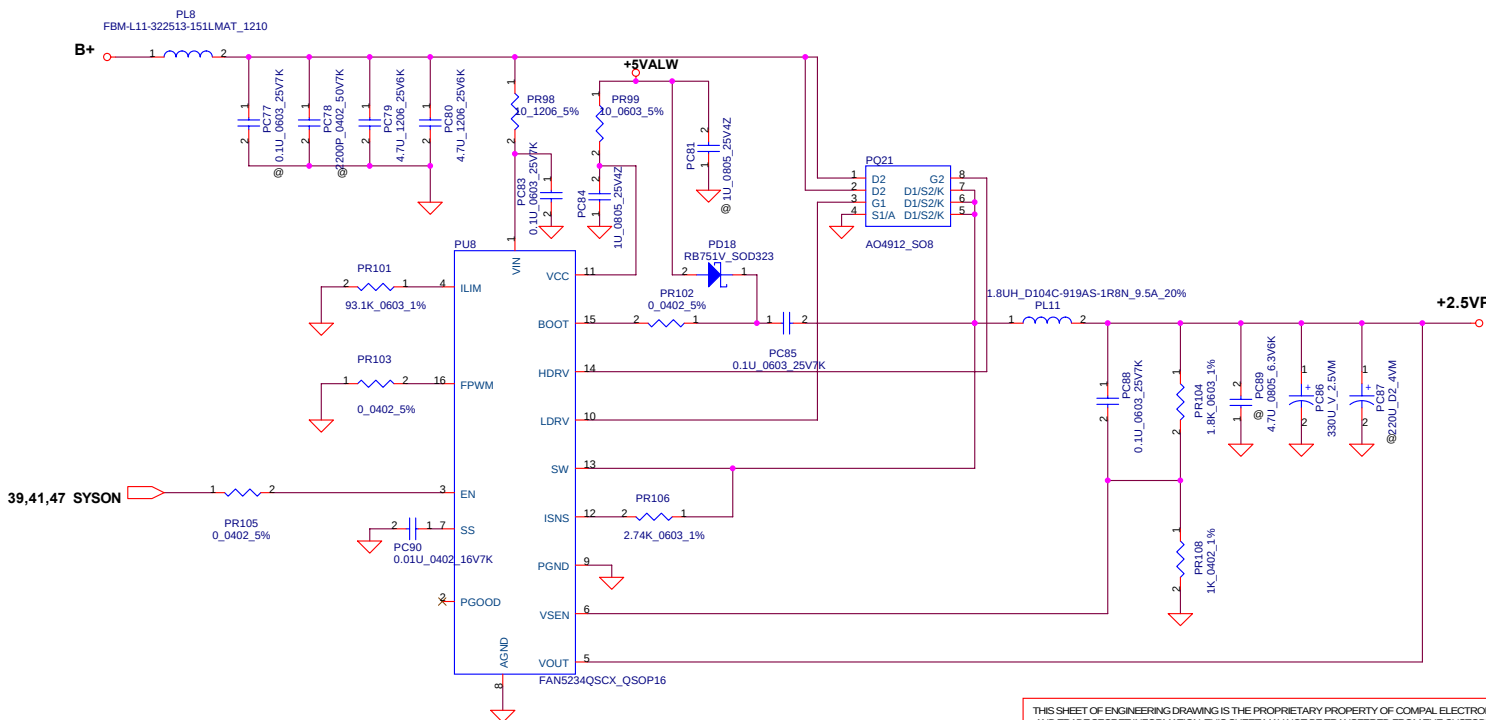
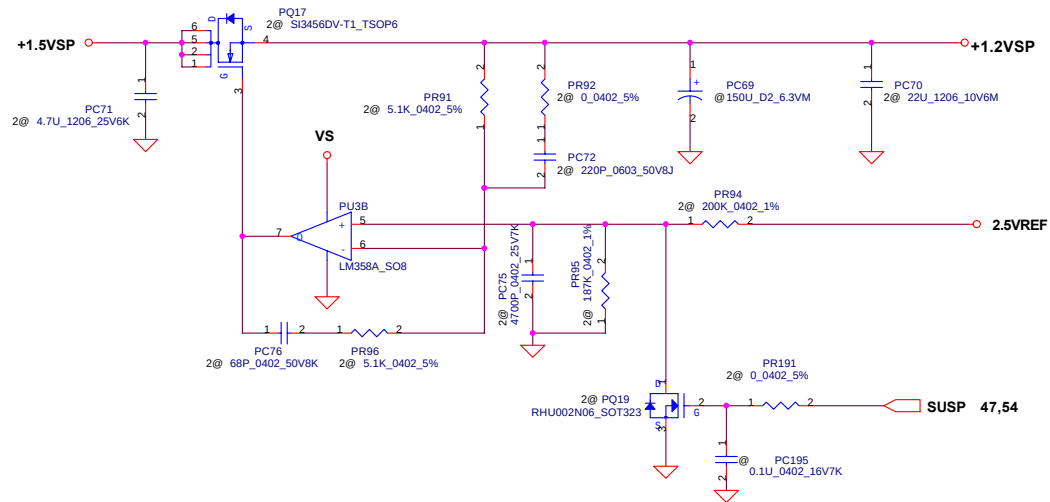
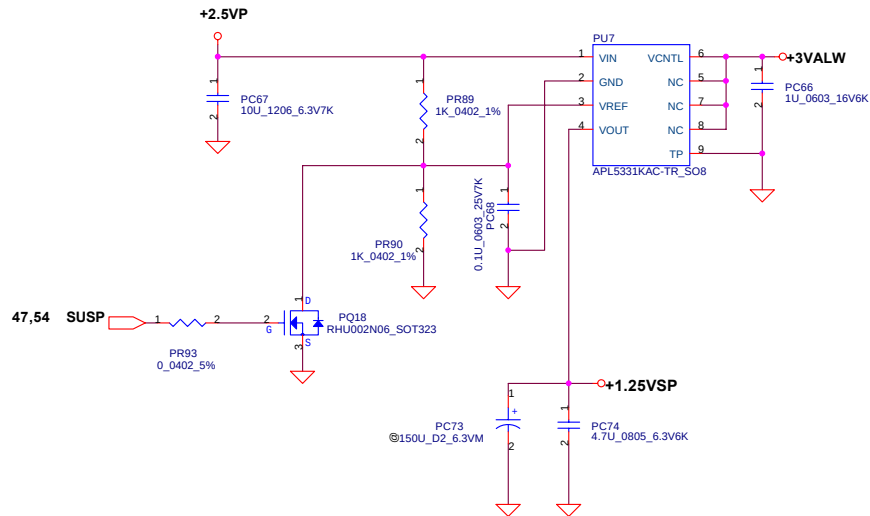
+3VALWP Choke DCR = 26.5mΩ.
Current limit Threshold Min.=80 mV Mx.=120mV.
OCP Min.= 80mV/1.27K*(1.27K+1.27K)/26.6=6.038A
OCP Max.=120mV/1.27K*(1.27K+1.27K)/26.5=9.056A

+5VALWP Choke DCR = 40mΩ.
Current limit Threshold Min.=80 mV Mx.=120mV.
OCP Min.= 80mV/0.698K*(1.54K+0.698K)/40=6.412A
OCP Max.=120mV/0.698K*(0.698K+1.54K)/40=9.593A

RS2(PR64)=RS1(PR58)*RS3(PR61)/(RS1+RS3)
L/RL(DCR)=RS1*RS3(PR61)/(RS1+RS3)*Cs(PC56)

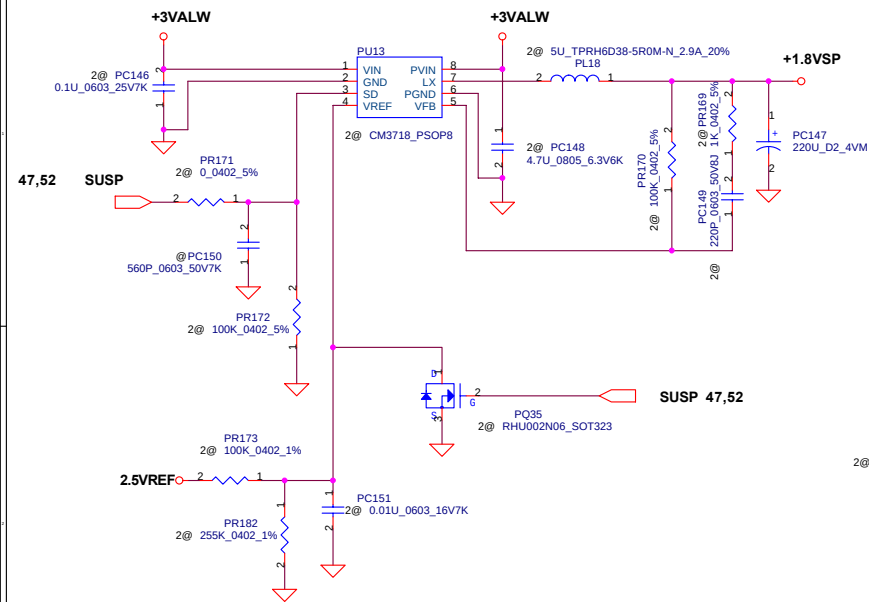
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Compal Electronics, Inc.			
Title			
3.3V / 5V / 12V			
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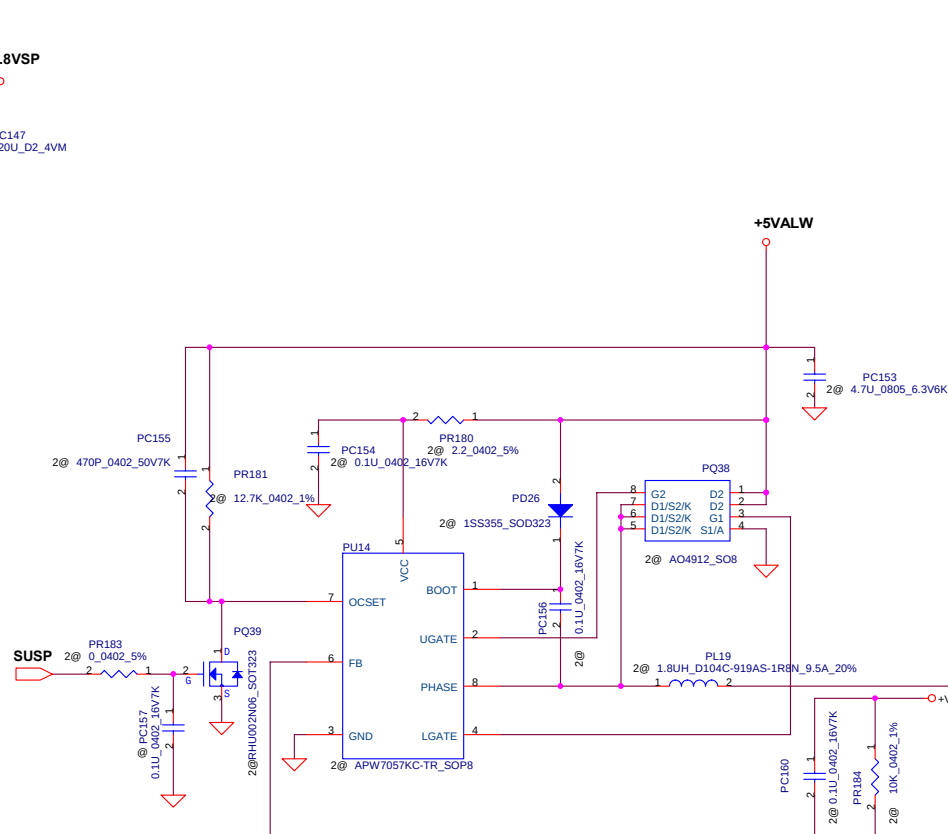
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Title			
1.25VSP/2.5VP/1.2VSP			
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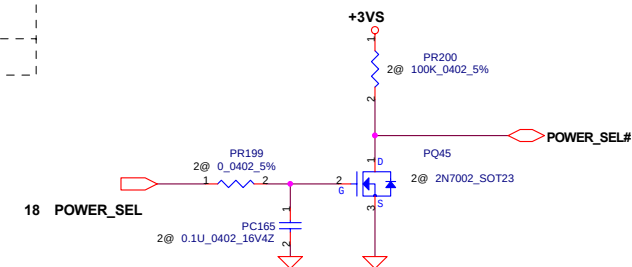


SUSP 47,52

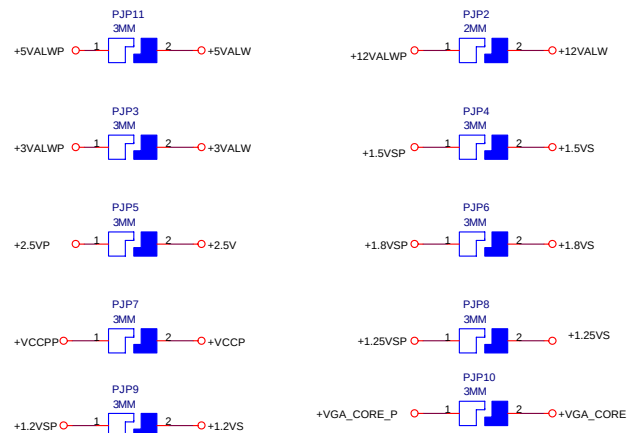
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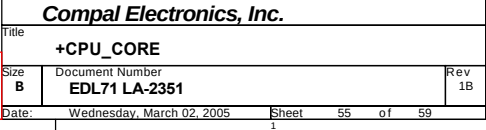


	POWER_SEL	VGA_CORE
	H	1.0V
	L	1.2V
VGA_CORE for ATI-M24		



18 POWER_SEL





Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1	Change DDRII to DDRI.	Change DDRII to DDRI.	0.2	54	1.Change PR104 from 1K_0603_1% to 1.8K_0603_1% 2.Change PR106 from 2K_0402_5% to 2.74K_0603_1% 3.Change PR101 from 107K_0402_1% to 93.1K_0603_1%.	0.2	DVT
2	Ripple voltage of +1.2VSP is large	The output voltage is unstable, so increase capacitance to improve it.	0.2	54	1.Change PC70 from 4.7U_1206_25V6K to 22U_1206_10V6M	0.2	DVT
3	Ripple voltage of +VCCPP is large	Ripple voltage is over spec.	0.2	55	Change PC106 from 150U_D2_6.3VM(45m) to 150U_D2_6.3VMV(15m)		
4	+1.5VP is poor supply by using CM3718.	Use MAX1845 to convert +1.5VP	0.2	56	1.Delete PU11 CM3718. 2.Delete PQ26 RHU002N06. 3.Delete PL14 5U_TPRH6D38-5R0M 4.Delete PC113 150U_D_6.3V 5.Delete PC115 4.7U_1206_25V6K. 6.Delete PC111,PC117PC121,PR123,PR125,PR127,PR129,PR130,PR131.	0.2	DVT
5	+1.5VP is poor supply by using CM3718.	Use MAX1845 to convert +1.5VP	0.2	55	1.Delete the PQ22 RHU002N06. 2.Delete PR109 100K_0402_1% 3.Delete the PC91 0.01U_0402_25V7Z 4.Change PR168 from 2K_0402_1% to 5.1K_0402_1%. 5.Change PC103 from 150U_D2_6.3VM(45m) to 150U_D2_6.3VMV(15m) 6.Change PL9 from 1.8UH_D104C-919AS-1R8N to 4.7UH_D104C-919AS-4R7N	0.2	DVT
6	Change +2.5VSP to +1.8VP	Change +2.5VSP to +1.8VP	0.2	56	1.Change PR173 from 10K_0402_1% to 100K_0402_1%. 2..Add PR182 255K_0402_1%.	0.2	DVT
7	For UMA platform can no populate +1.2VSP.	For UMA platform can no populate +1.2VSP.	0.2	54	No populate PC71,PQ17,PR91,PR92,PC72,PR96,PC76,PC70,PR94,PR95,PC75,PQ19,PR97,PQ20,PR100 and PC82.	0.2	DVT
8	For UMA platform can no populate +1.8VSP.	For UMA platform can no populate +1.8VSP.	0.2	55	No populate PU13,PC146,PR171,PR172,PR173,PR182,PC151,PQ35,PL18,PC148,PR170,PR169,PC149 and PC147.	0.2	DVT
9	For charge current accuracy requirement	For charge current accuracy requirement	0.2	50	Change PR43 from 120K_0402_5% to 120K_0402_1%.	0.2	DVT
10	For charge voltage accuracy requirement	For charge voltage accuracy requirement	0.2	50	Change PR46 from 49.9K_0402_1% to 49.9K_0603_0.1%	0.2	DVT
11	Use lower rating capacitors to improve cost down.	Use lower rating capacitors to improve cost down.	0.2	50	1.Change PC42 from 4.7U_1206_25V6K to 4.7U_0805_6.3V6K. 2.Change PC74 from 4.7U_1206_25V6K to 4.7U_0805_6.3V6K. 3.Change PC94 from 4.7U_1206_25V6K to 4.7U_0805_6.3V6K. 4.Change PC148 from 4.7U_1206_25V6K to 4.7U_1206_6.3V6K without populate.	0.2	DVT
12	For pull high to VGATE.	For pull high to VGATE.	0.2	50	Populate PR133 with 10K_0402_1%.	0.2	DVT
13	To avoid inrush current.	To avoid inrush current.	0.2	50	Add PR190 between PD14 pin2 and VS with 10_1206_5%.	0.2	DVT
14	To solve the no load PWM waveform issue.	To solve the no load PWM waveform issue.	0.2	53	Change PC86 from 220U_D2_4VM to 220U_D2_4V_15m.	0.2	DVT
15	To solve the shutdown negtive voltage issue.	To solve the shutdown negtive voltage issue.	0.2	54	Add PQ41(2N7002_SOT23) and PR196(33K_0402_1%) and PR197(11K_0402_1%)	0.2	DVT

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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
16	To cost down.	To cost down.	0.2	54	Change Max1845 to Max8743 and remove PD20 and PD21	0.2	DVT
17	To solve Max1902 can locked as adapter plug in and uproot out the electric socket continuous.	To solve Max1902 can locked as adapter plug in and uproot out the electric socket continuous.	0.2	52	Add Precharge circuit.	0.2	DVT
18	Power select action correct	Power select action correct	0.2	55	Add PQ45 and PR199 and PR200 and PC165.	0.2	DVT
19	Increase choke rating of 5VALWP.	Increase choke rating of 5VALWP.	0.3	52	Change PL6 from SH136100020 to SH13690AM00.	0.3	PVT
20	BOM Error of PD2	PD2 shows wrong location PD5 on SAP system, I update it.	0.3	49	Change its location from PD5 to PD2.	0.3	PVT
21	BOM Error of PQ41 and PQ45.	SAP system has quantity but shows no location of PQ41 and PQ45.	0.3	52,55	Update the location of PQ41 and delete PQ45.	0.3	PVT
22	EMI issue.	EMI's request.	0.3	56	Change PR136 and PR159 from SD028000000 to SB028220B00.	0.3	PVT
23	Production EOL.	SB906100109(TP0610T) will go EOL.	0.3	50	Change SB906100109 to SB906100200.	0.3	PVT
24	Time sequence error.	Time sequence is error such that B+ can't build.	0.3	51,52	Change PR52 from SD034470200 to SD028150300. Un-populate PC65. Change PR87 from SD028470200 to SD028000000.	0.3	PVT
25	OTP setting adjust.	Because we change PR52 such that OTP needs to reset.	0.3	50	1 Change PR55 from SD034169200 to SD034205200. 2 Change PR57 from SD014215108 to SD014182102.	0.3	PVT
26	Add other circuit of precharge.	Because we need to populate this circuit such that precharge can enable.	0.3	48	1 Add PD1 SC11N4148T8(S DIO 1N4148(SM)). 2 Add PR10 SD0111501T6(S RES 1/4W 1.5K +-5% 1206). 3 Add PR11 SD0111501T6(S RES 1/4W 1.5K +-5% 1206). 4 Add PR12 SD0111501T6(S RES 1/4W 1.5K +-5% 1206). 5 Add PR13 SD0111501T6(S RES 1/4W 1.5K +-5% 1206).	0.3	PVT
27	Un-populate VGA_CORE_P.	Because EDL71 is Aviso GM plate form, we don't populate PQ45, PR199, PR200, PC165.	0.3	54	Delete PQ45, PR199, PR200, PC165.	0.3	PVT
28	Adjust CP point.	Because we need to change CP point to improve CP mode.	0.4	49	Change PR35 from SD034226200 to SD034249200.	0.3	EVT
29	Add PC146 for EDL70.	We need to add PC146 such that Vin can more clear and stable.	0.4	54	Add PC146 for 1.8VSP of EDL70.	0.3	EVT
30	To cost down.	To cost down.	0.4	54	Change PC147 from SG020151300 to SGA20221120.	0.3	EVT
31	Precharge circuit tolerance adjust.	Because the tolerance should be 1% but the material on BOM is 5% so we update it.	0.4	54	Change PR52 from SD028150300 to SD034150300.	0.4	EVT
32	UUT has Zi Zi noise issue.	Because we have UUT zi zi noise issue, we add two capacitor to solve it.	0.4	54	Add PC126 and PC127 with SF10004M008.	54	EVT
33	Noise on S3 mode.	Because we found noise on ceramic capacitor, we increase capacitance to decrease this noise.	0.4	54	Change PC43 from SE142475K00 to SE142106M00.	54	EVT

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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
1	S4 auto resume	Can't auto resume from S4	0.4	30	Change VCCSUS3_3 from +3V to +3VALW	0.5	PVT
2	C615 short	C615 short to logic low cause can't boot	0.4	35	Change C613 and C615 to SGN01220100	0.5	PVT
3	bo niose when shut down	speaker generate "bo" niose when system shut down	0.4	45	Change R460 to R461	0.5	PVT
4	C904 too close to JP12	C904 too close to JP12 if C904 fail can't repair	0.4	40	JP12 change to DC233104020	0.5	PVT
5	+1.5V rising edge	+1.5V 's rising edge is not smooth	0.4	30	Add R12	0.5	PVT
6	SW DJ can't play with Hitach HDD	Hitachi HDD send IDE_DIOR# in SW DJ S0 mode	0.4	31,46	Add Q97, R1197, R1198	0.5	PVT
7	Modem noise	Modem dial tone have noise	0.4	39	Change R518, R521 from SD0130000T4 to SM010012000	0.5	PVT
8	KB910 damage issue	KB910 INVT_PWM pin damage issue	0.5	41	Add D32,D33	0.6	PVT
9	S4 auto resume	Can't auto resume from S4	0.5	29,30	Change +3V to +3VALW for SMBUS and LINKALERT#, EC_SMI#, SYS_RESET# PM_BATLOW#, GPI11, ICH_PCIE_WAKE# 1.5V LDO	0.6	PVT
10	Bo noise	Bo noise gernerate in SWDJ mode and power up	0.5	45	Del R460 and R461, add D35 and D36	0.6	PVT
11	Backlight issue	backlight timing error	0.5	24	Add D34 and R1118	0.6	PVT
12	Sighting Alert	Alviso SMVREF Sighting Alert (# 68363)	0.5	9	No stuff R100 and R101	0.6	PVT
13	CRT ISSUE	CRT NOISE issue	0.5	12	Change C119 from SE053106Z00 to SE077226M10	0.6	PVT
14	SWDJ issue	SWDJ can't play	0.5	46	Add Q98	0.6	PVT
15	USB OC	Add USB OC delay circuit	0.5	40	Add R1201,R1202,R1203,R1204,R1205, R1206,C1134,C1135,C1136	0.6	PVT
16	SVIDEO ISSUE	SVIDEO out noise issue	0.5	12	Change C92 from SE107475M00 to SE077226M10	0.6	PVT
17	TV TUNNER	No sound in IOMP mode	0.5	38	ADD TV_AUDIO_R and TV_AUDIO_L	0.6	PVT
18	Power sequence	Power sequence	0.5	47	Add C172 for EDL70 power sequence	0.6	PVT
19	LCD Power sequence for EDL70/72	Power off white screen issue	1.0	24	Add 1@ on R1118 and D34	1.1	PVT
20	ESD	Add ESD diode for USB data and EC INVT_PWM pin	1.0	40, 41	Add U70, D38, D39 and D40	1.1	PVT

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