LAGUNA

REV : X00

@ : Depop Component

PRELIMINARY

Dothan Schematic with Capture CIS and Function field

uFCPGA Dothan
02-07-2004
REV: 0.3

DELL CONFIDENTIAL/PROPRIETARY

Title: **Cover Sheet**

Size	Document Number	Rev
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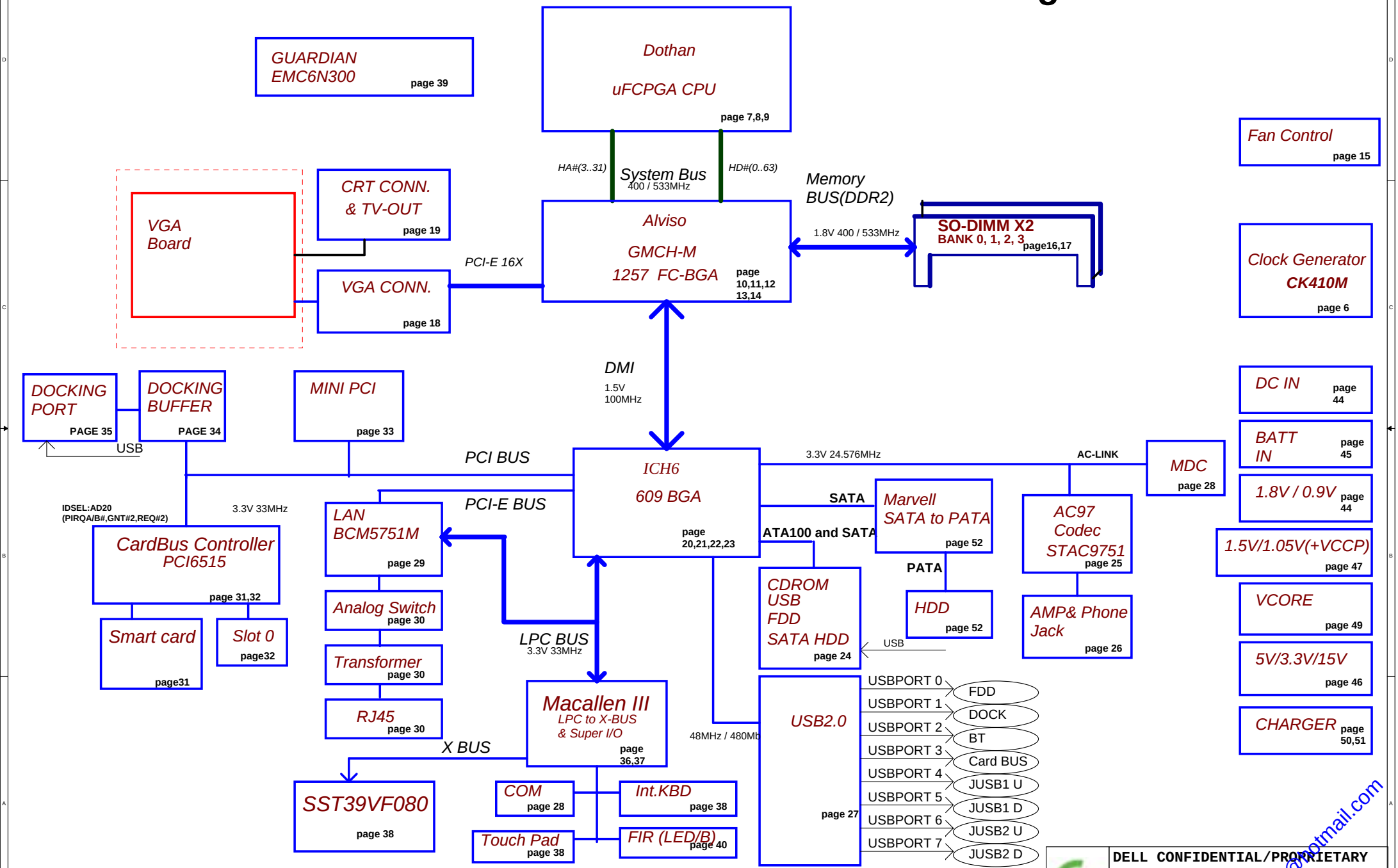
Compal confidential

Block Diagram



DELL CONFIDENTIAL/PROPRIETARY

Title: Block Diagram

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PM TABLE

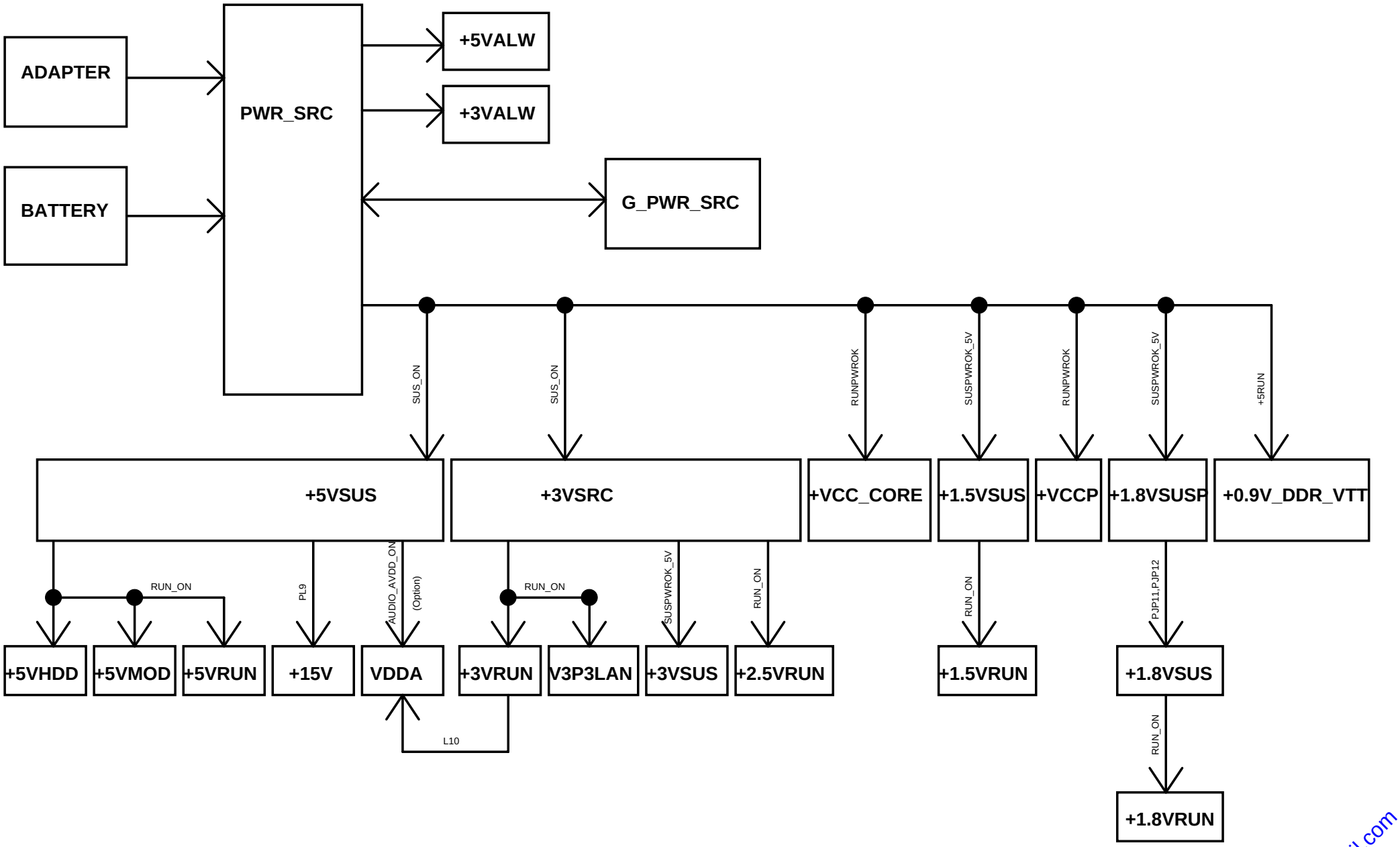
State \ power plane	+3VALW +5VALW	+3VSUS +5VSUS +1.8VSUS +1.5VSUS	+5VRUN +RTC_CELL +3VRUN +0.9V_DDR_VTT +2.5VRUN +1.8VRUN +1.5VRUN +VCC_CORE +VCCP +15V
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
CARD BUS	AD17	1	D,C
DOCK	AD24	0	A
MINI PCI	AD19	3	D,B

USB TABLE

USB PORT#	DESTINATION
0	FDD (module bay)
1	DOCK
2	MPCI (BlueTooth)
3	NEW Connector
4	USB Port 1(Top)
5	USB Port 1(Bottom)
6	USB Port 2(Top)
7	USB Port 2(Bottom)



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Title: **Power Rail**

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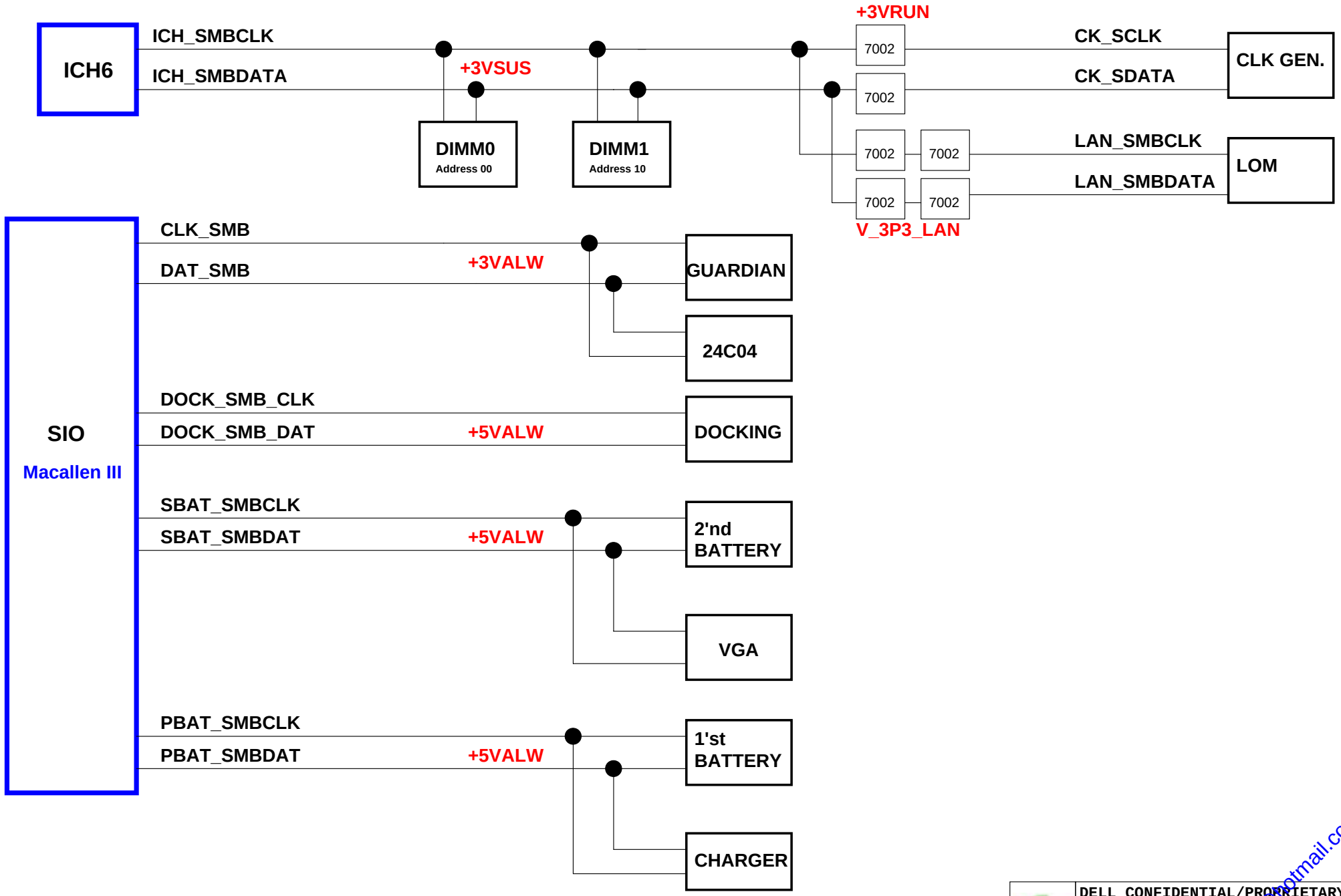

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Title: SMBUS TOPOLOGY

Size | Document Number: Board Number LA2111 | Rev: 0.3

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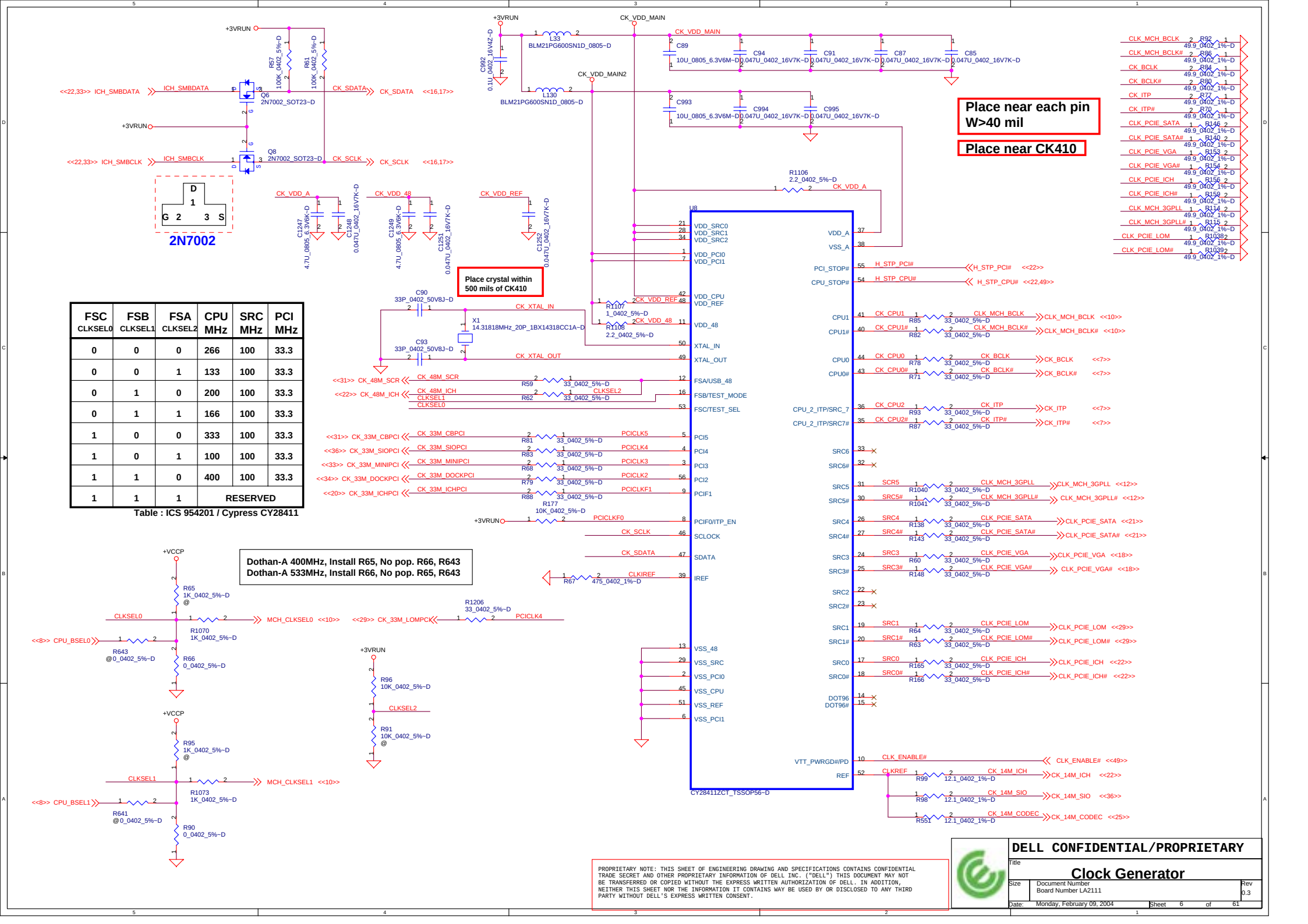

FSC CLKSEL0	FSB CLKSEL1	FSA CLKSEL2	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3
1	0	0	333	100	33.3
1	0	1	100	100	33.3
1	1	0	400	100	33.3
1	1	1	RESERVED		

Table : ICS 954201 / Cypress CY28411

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Title: Clock Generator

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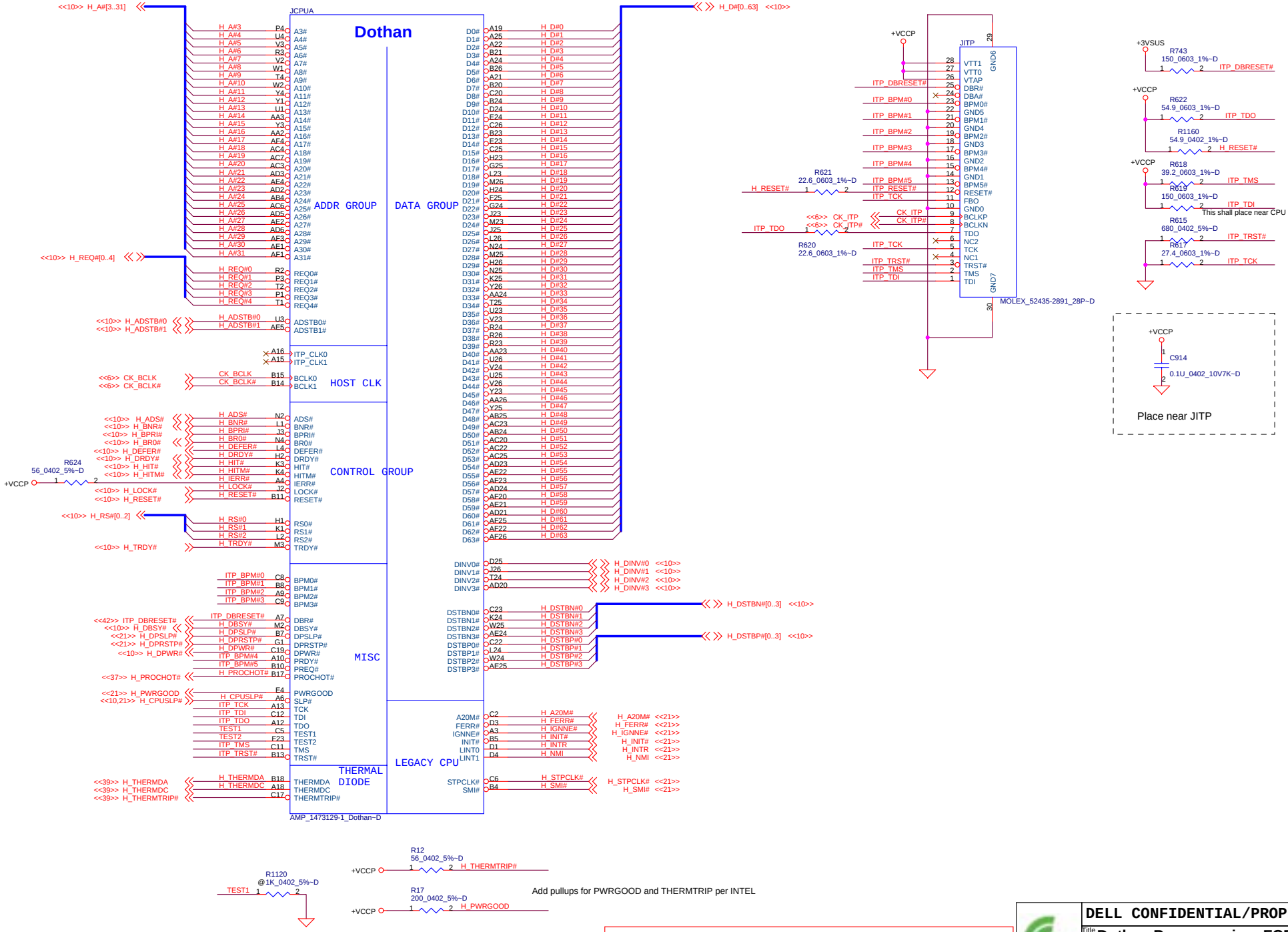

DELL CONFIDENTIAL/PROPRIETARY

Title: Dothan Processor in mFCPGA479

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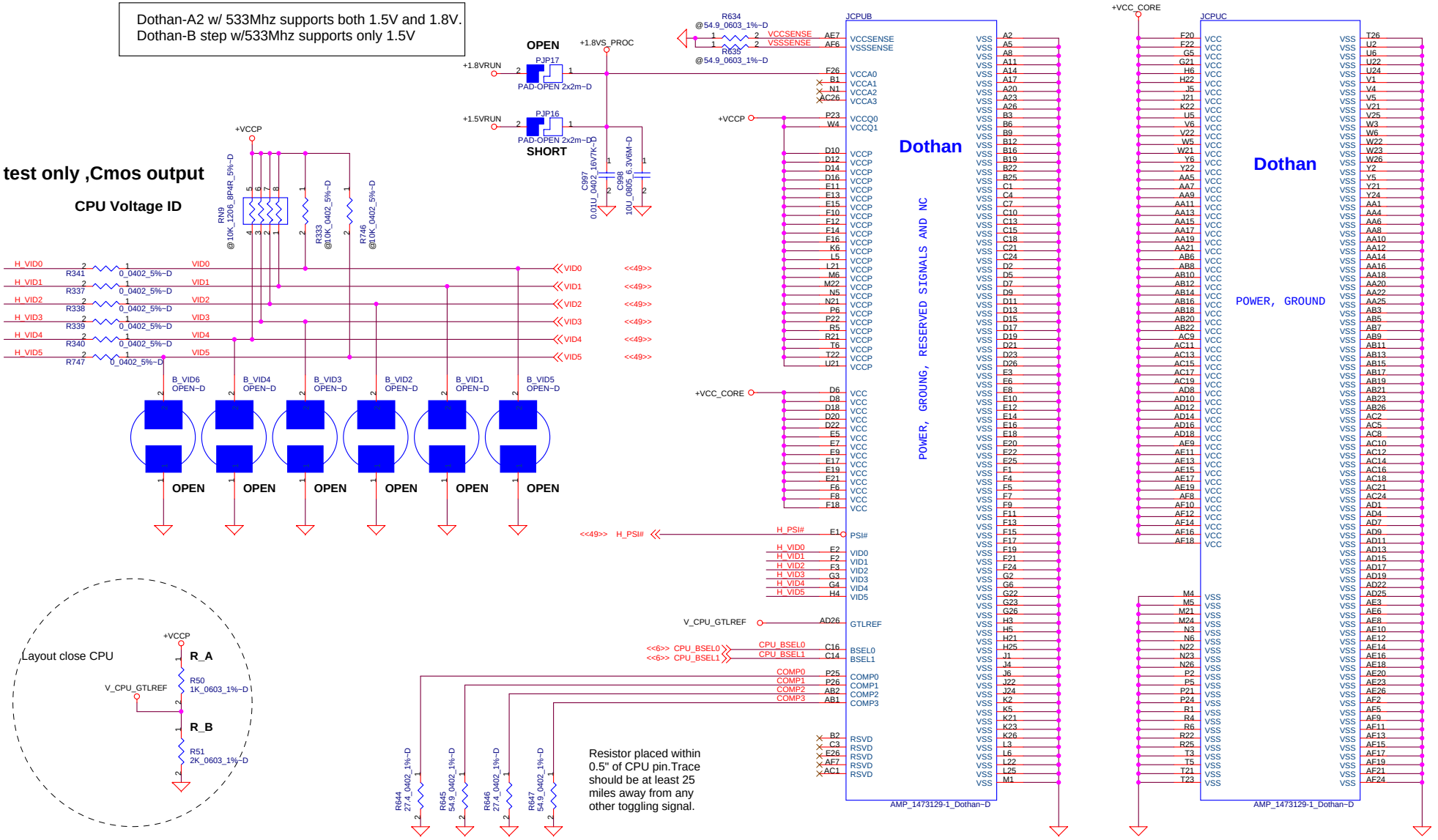
Dothan-A2 w/ 533Mhz supports both 1.5V and 1.8V.
Dothan-B step w/533Mhz supports only 1.5V

For test only ,Cmos output

CPU Voltage ID



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Title: **Dothan Processor in mFCPGA479**

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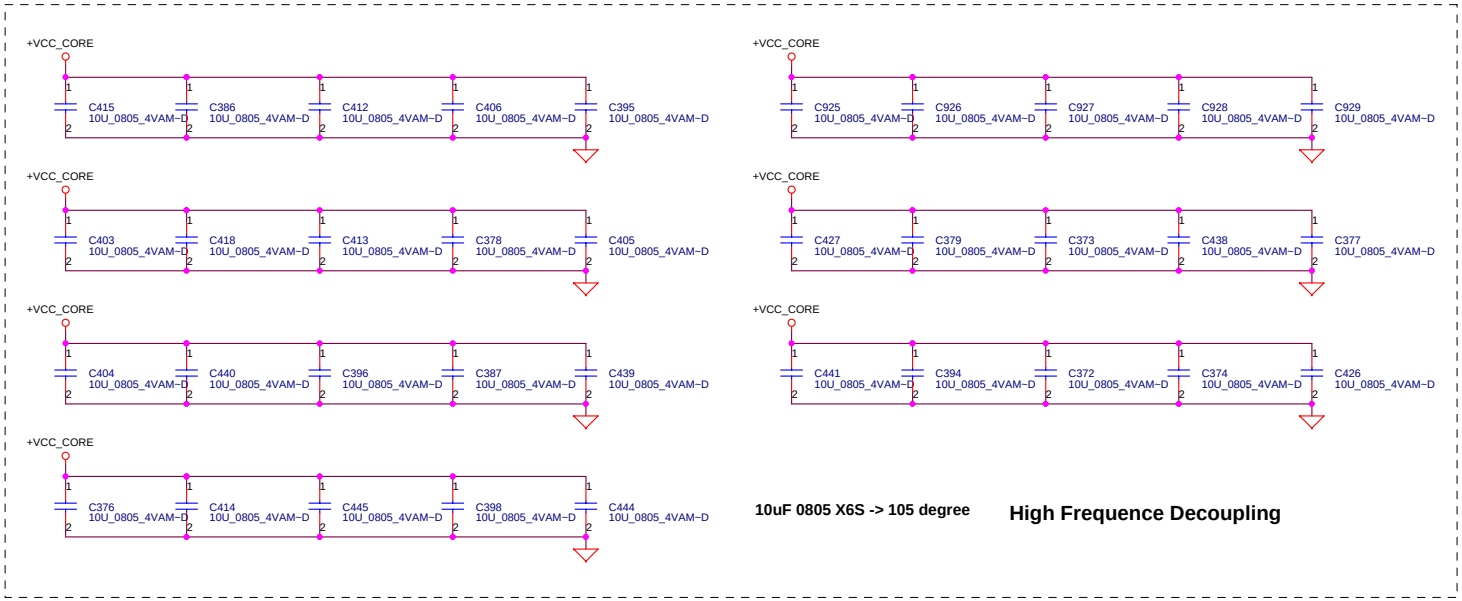
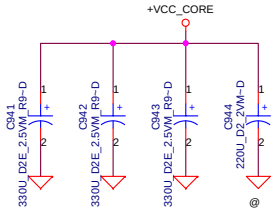
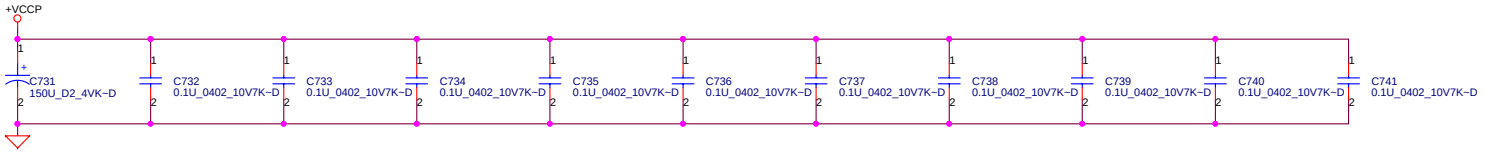


Near VCORE regulator.



9mOhm 7343 PS CAP **9mOhm 7343 PS CAP** **9mOhm 7343 PS CAP**

ESR <= 3m ohm
Capacitor > 880uF



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Title **CPU Bypass**

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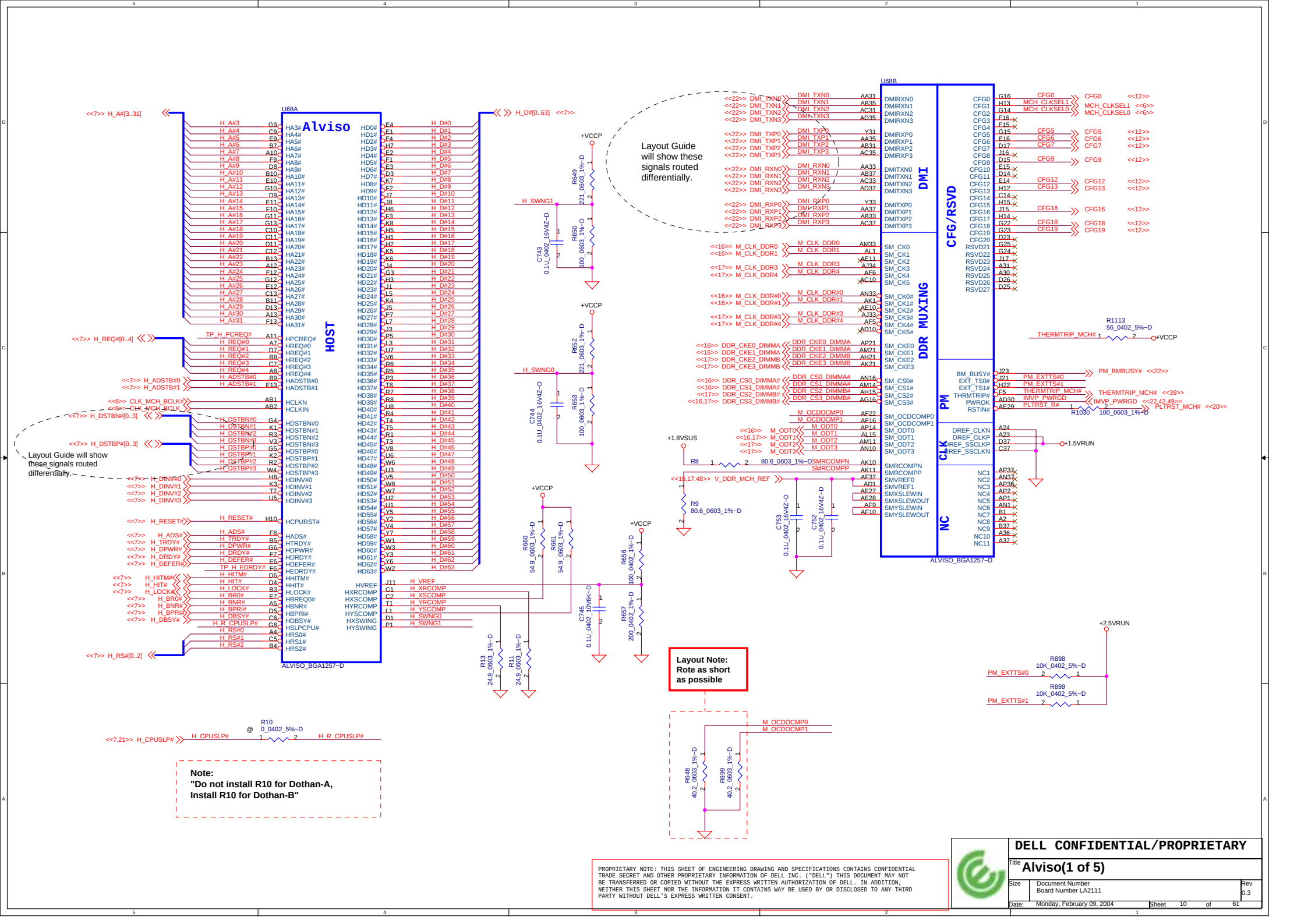
U68A
Alviso
HOST
ALVISO_BGA1257~D
U68B
DMI
DDR MUXING
CFG/RSVD
PM
CLK
NC
ALVISO_BGA1257~D
Layout Guide will show these signals routed differentially.
Layout Guide will show these signals routed differentially.
Layout Note: Rote as short as possible
Note: "Do not install R10 for Dothan-A, Install R10 for Dothan-B"
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Alviso(1 of 5)
Document Number
Board Number LA2111
Rev 0.3
Monday, February 09, 2004
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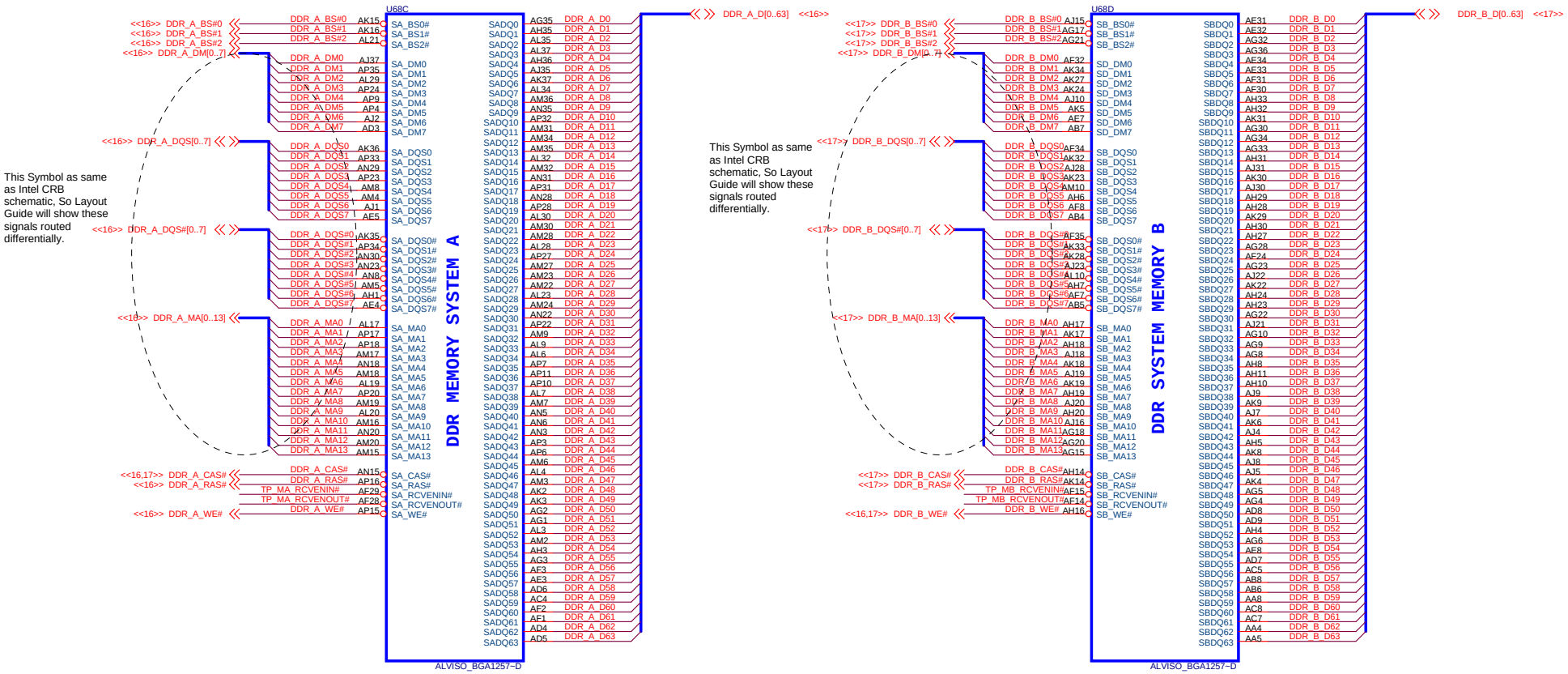

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Title: **Alviso(2 of 5)**

Size	Document Number	Rev
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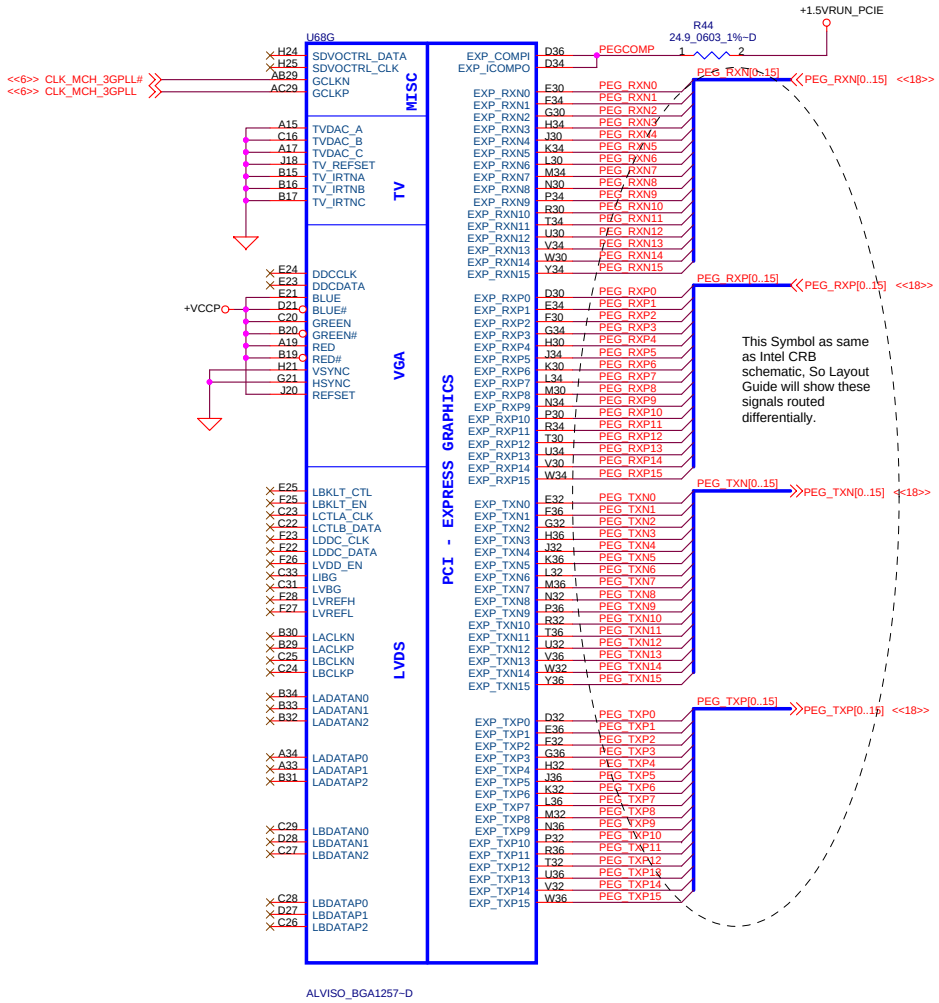
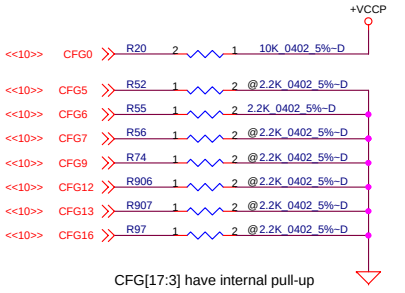
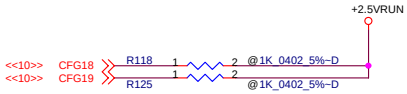


This Symbol as same as Intel CRB schematic, So Layout Guide will show these signals routed differentially.

CFG[2:0]	**Refer to sheet 6 for FSB frequency select**
CFG5	**Low = DMI x 2** **High = DMI x 4** *
CFG6	**Low = DDR-II** * **High = DDR-I**
CFG7	**Low = DT/Transportable CPU** **High = Mobile CPU** *
CFG9	**Low = Reverse Lane** **High = Normal Operation** *
CFG[13:12]	**00 = Reserved** **01 = XOR Mode Enabled** **10 = All Z Mode Enabled** **11 = Normal Operation (Default)** *
CFG16 (FSB Dynamic ODT)	**Low = Disabled** **High = Enabled** *
CFG18 (VCC Select)	**Low = 1.05V (Default)** * **High = 1.5V**
CFG19 (VTT Select)	**Low = 1.05V (Default)** * **High = 1.2V**



CFG[17:3] have internal pull-up



CFG[19:18] have internal pull-down

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Title: **Alviso(3 of 5)**

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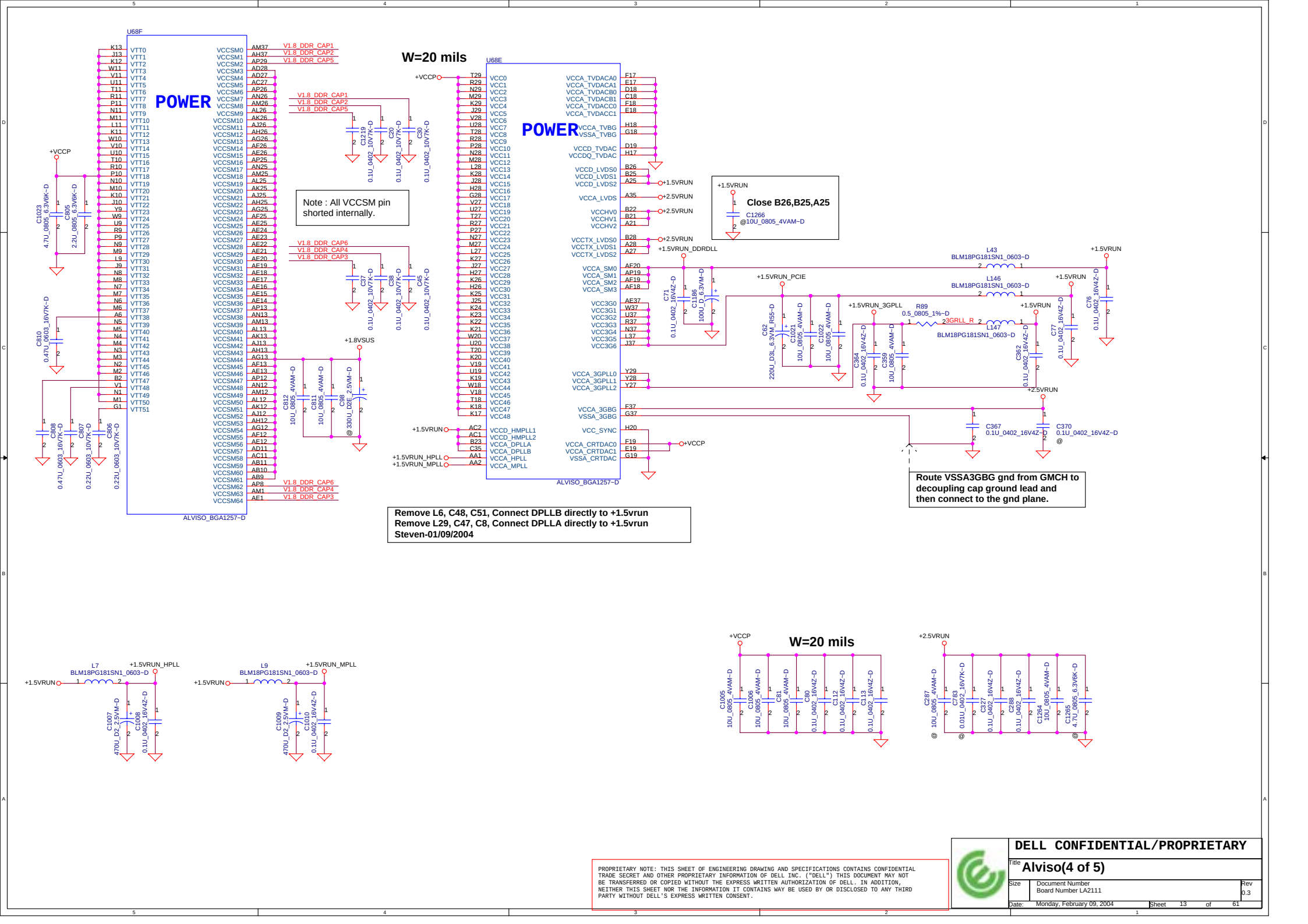

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Title: Alviso(4 of 5)

Size	Document Number	Rev
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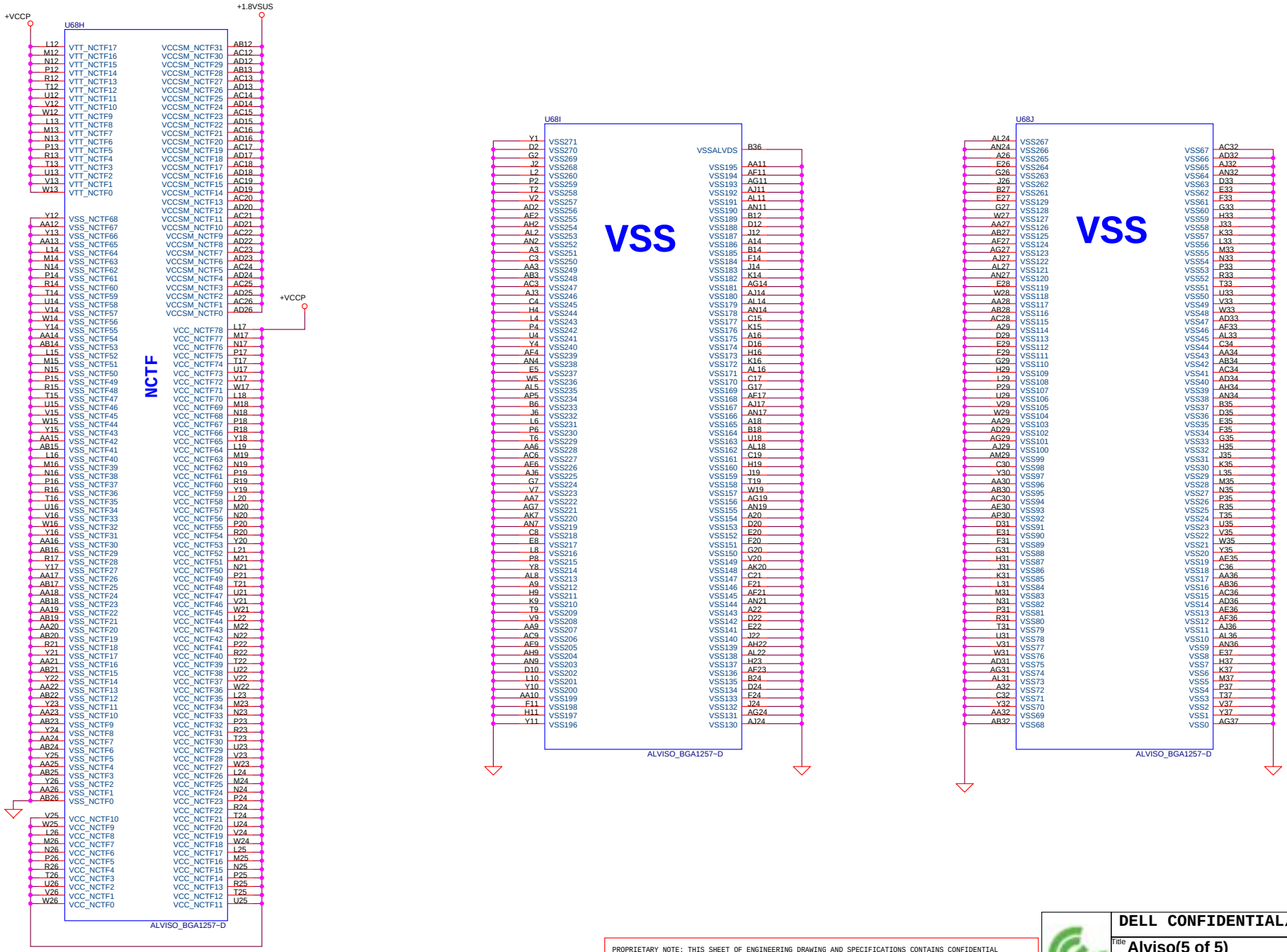

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Title: **Alviso(5 of 5)**

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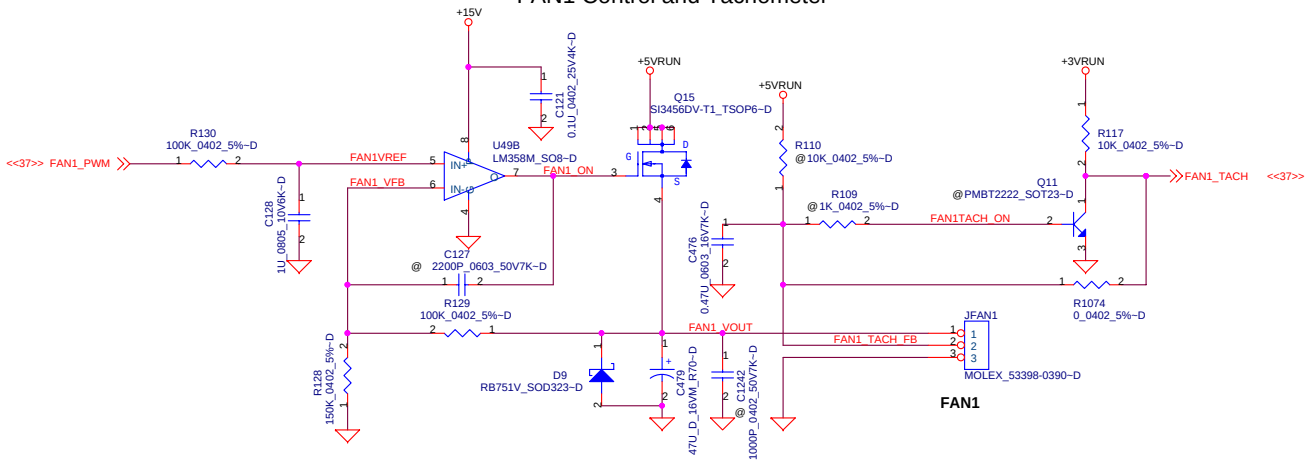
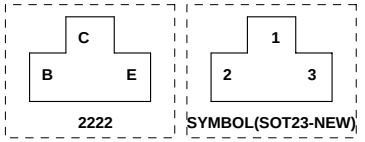
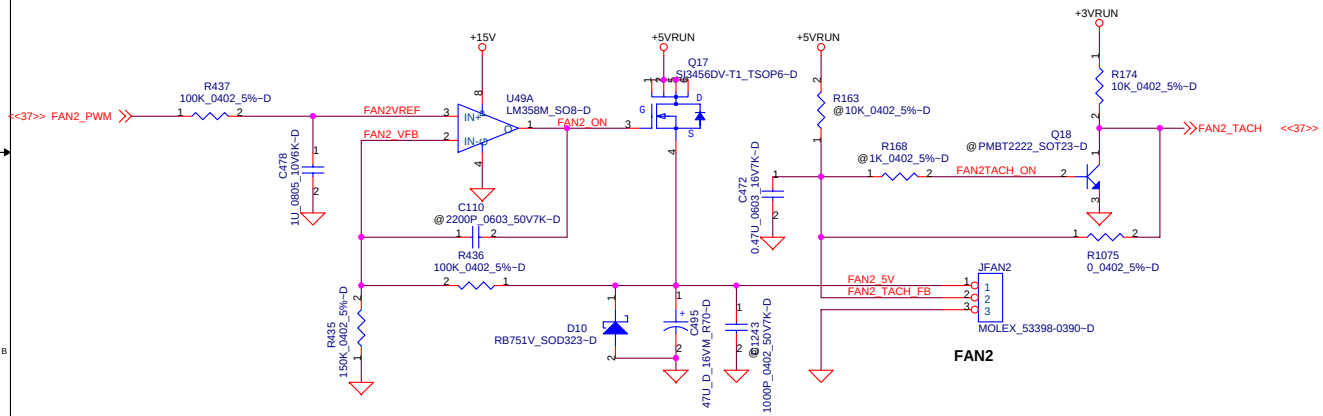
FAN1 Control and Tachometer





FAN2 Control and Tachometer



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Title: **ITP Debug CONN. & FAN**

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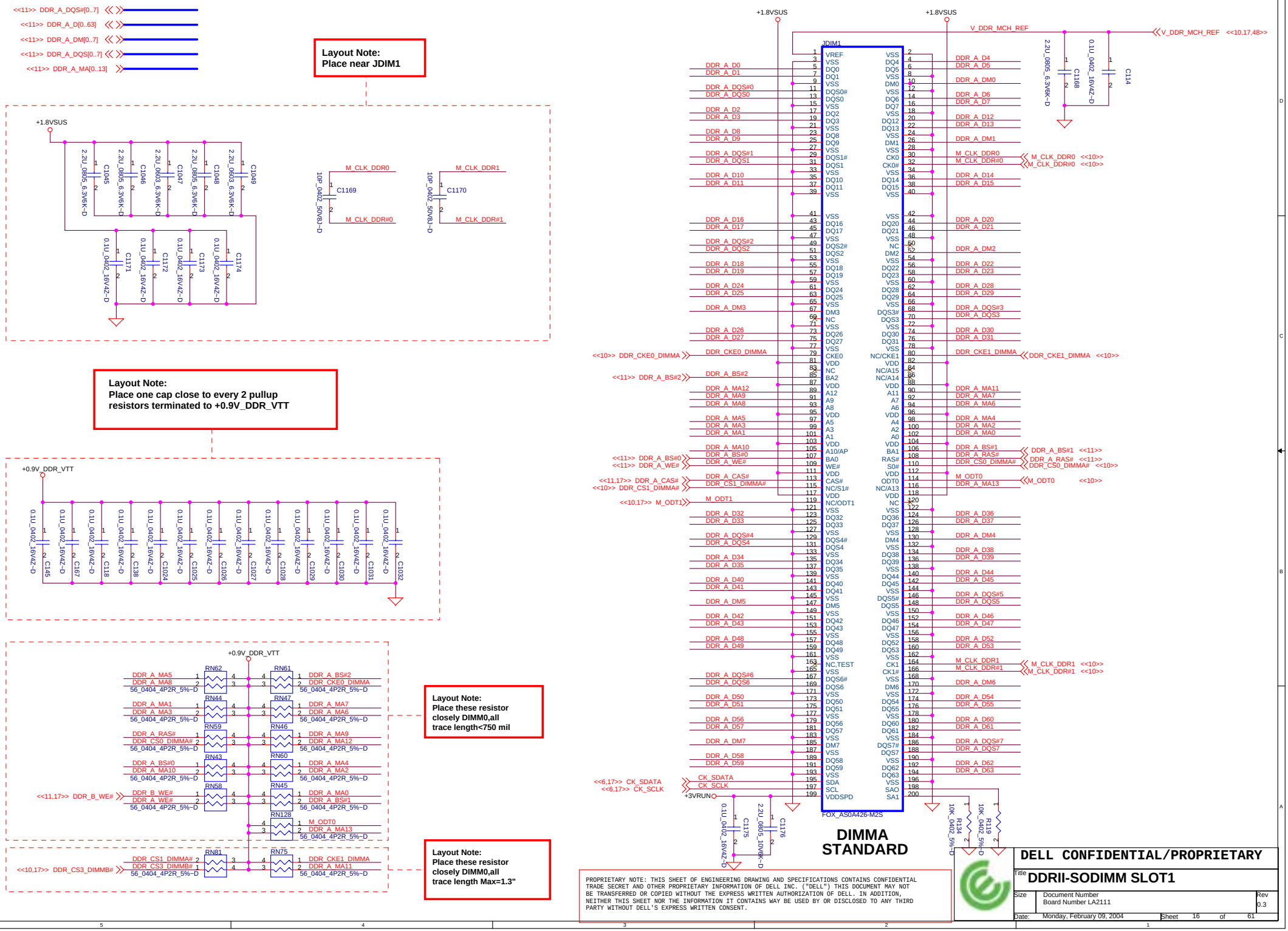
Layout Note:
Place near JDIM1
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT
Layout Note:
Place these resistor
closely DIMM0,all
trace length<750 mil
Layout Note:
Place these resistor
closely DIMM0,all
trace length Max=1.3"
JDIM1
FOX_AS0A426-M2S
DIMMA
STANDARD
DELL CONFIDENTIAL/PROPRIETARY
DDRII-SODIMM SLOT1
Size
Document Number
Board Number LA2111
Rev
0.3
Date: Monday, February 09, 2004
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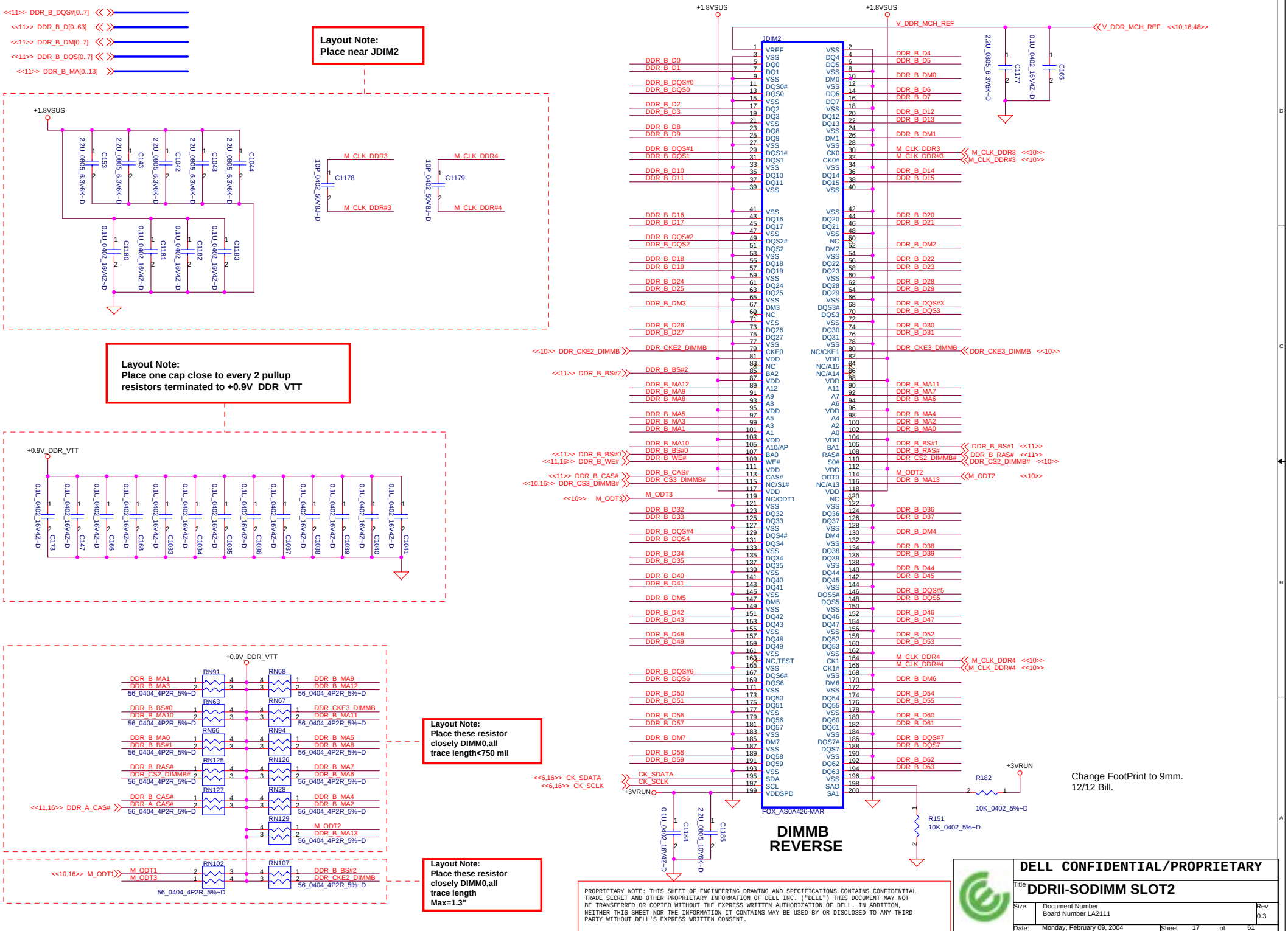
Layout Note:
Place near JDIM2
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9V_DDR_VTT
Layout Note:
Place these resistor
closely DIMM0,all
trace length<750 mil
Layout Note:
Place these resistor
closely DIMM0,all
trace length
Max=1.3"
JDIM2
FOX_AS0A426-MAR
DIMMB
REVERSE
Change FootPrint to 9mm.
12/12 Bill.
DELL CONFIDENTIAL/PROPRIETARY
DDRII-SODIMM SLOT2
Size
Document Number
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0.3
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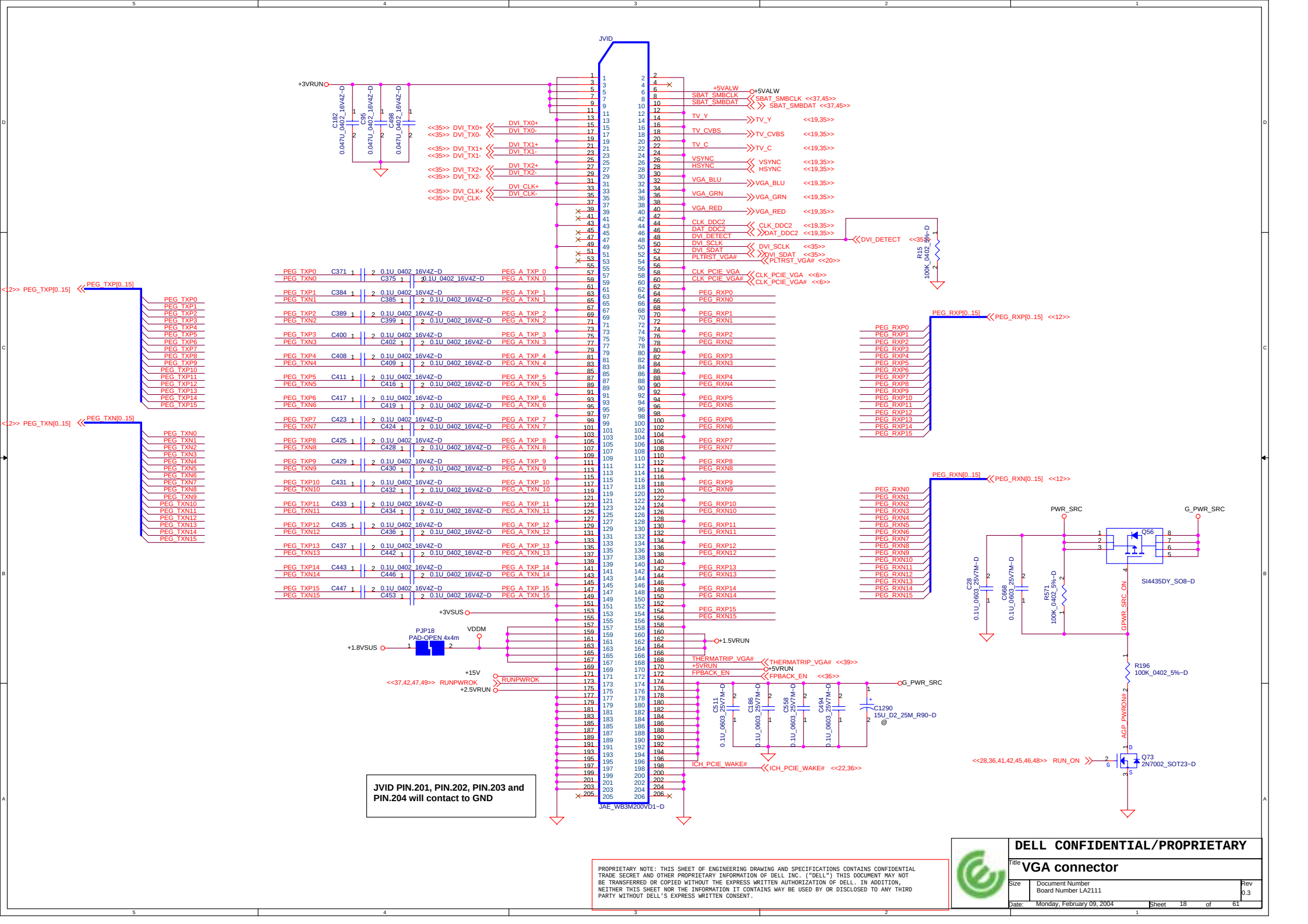
JVID
JAE_WB3M200VD1-D
+3VRUN
C182 0.047U_0402_16V4Z-D
C95 0.047U_0402_16V4Z-D
C98 0.047U_0402_16V4Z-D
<<35>> DVI_TX0+
<<35>> DVI_TX0-
DVI_TX0+
DVI_TX0-
<<35>> DVI_TX1+
<<35>> DVI_TX1-
DVI_TX1+
DVI_TX1-
<<35>> DVI_TX2+
<<35>> DVI_TX2-
DVI_TX2+
DVI_TX2-
<<35>> DVI_CLK+
<<35>> DVI_CLK-
DVI_CLK+
DVI_CLK-
+5VALW
SBAT_SMBCLK
SBAT_SMBDAT
SBAT_SMBCLK <<37,45>>
SBAT_SMBDAT <<37,45>>
TV_Y
TV_CVBS
TV_C
VSYNC
HSYNC
VGA_BLU
VGA_GRN
VGA_RED
CLK_DDC2
DAT_DDC2
DVI_DETECT
DVI_SCLK
DVI_SDAT
PLTRST_VGA#
CLK_PCIE_VGA
CLK_PCIE_VGA#
DVI_DETECT <<35>>
R15 100K_0402_5%~D
PEG_TXP[0..15]
PEG_TXN[0..15]
<<12>> PEG_TXP[0..15]
<<12>> PEG_TXN[0..15]
PEG_TXP0 C371 0.1U_0402_16V4Z~D PEG_A_TXP_0
PEG_TXN0 C375 0.1U_0402_16V4Z~D PEG_A_TXN_0
PEG_TXP1 C384 PEG_A_TXP_1
PEG_TXN1 C385 PEG_A_TXN_1
PEG_TXP2 C389 PEG_A_TXP_2
PEG_TXN2 C399 PEG_A_TXN_2
PEG_TXP3 C400 PEG_A_TXP_3
PEG_TXN3 C402 PEG_A_TXN_3
PEG_TXP4 C408 PEG_A_TXP_4
PEG_TXN4 C409 PEG_A_TXN_4
PEG_TXP5 C411 PEG_A_TXP_5
PEG_TXN5 C416 PEG_A_TXN_5
PEG_TXP6 C417 PEG_A_TXP_6
PEG_TXN6 C419 PEG_A_TXN_6
PEG_TXP7 C423 PEG_A_TXP_7
PEG_TXN7 C424 PEG_A_TXN_7
PEG_TXP8 C425 PEG_A_TXP_8
PEG_TXN8 C428 PEG_A_TXN_8
PEG_TXP9 C429 PEG_A_TXP_9
PEG_TXN9 C430 PEG_A_TXN_9
PEG_TXP10 C431 PEG_A_TXP_10
PEG_TXN10 C432 PEG_A_TXN_10
PEG_TXP11 C433 PEG_A_TXP_11
PEG_TXN11 C434 PEG_A_TXN_11
PEG_TXP12 C435 PEG_A_TXP_12
PEG_TXN12 C436 PEG_A_TXN_12
PEG_TXP13 C437 PEG_A_TXP_13
PEG_TXN13 C442 PEG_A_TXN_13
PEG_TXP14 C443 PEG_A_TXP_14
PEG_TXN14 C446 PEG_A_TXN_14
PEG_TXP15 C447 PEG_A_TXP_15
PEG_TXN15 C453 PEG_A_TXN_15
0.1U_0402_16V4Z~D
PEG_RXP0
PEG_RXN0
PEG_RXP1
PEG_RXN1
PEG_RXP2
PEG_RXN2
PEG_RXP3
PEG_RXN3
PEG_RXP4
PEG_RXN4
PEG_RXP5
PEG_RXN5
PEG_RXP6
PEG_RXN6
PEG_RXP7
PEG_RXN7
PEG_RXP8
PEG_RXN8
PEG_RXP9
PEG_RXN9
PEG_RXP10
PEG_RXN10
PEG_RXP11
PEG_RXN11
PEG_RXP12
PEG_RXN12
PEG_RXP13
PEG_RXN13
PEG_RXP14
PEG_RXN14
PEG_RXP15
PEG_RXN15
PEG_RXP[0..15]
PEG_RXN[0..15]
<<12>> PEG_RXP[0..15]
<<12>> PEG_RXN[0..15]
+3VSUS
+1.8VSUS
PJP18
PAD-OPEN 4x4m
VDDM
+1.5VRUN
THERMATRIP_VGA#
<<39>> THERMATRIP_VGA#
+5VRUN
FPBACK_EN
<<36>> FPBACK_EN
G_PWR_SRC
+15V
<<37,42,47,49>> RUNPWROK
RUNPWROK
+2.5VRUN
C511 0.1U_0603_25V7M~D
C186 0.1U_0603_25V7M~D
C558 0.1U_0603_25V7M~D
C494 0.1U_0603_25V7M~D
C1290 15U_D2_25M_R90~D
@
ICH_PCIE_WAKE#
<<22,36>> ICH_PCIE_WAKE#
PWR_SRC
G_PWR_SRC
Q56
SI4435DY_SO8~D
C28 0.1U_0603_25V7M~D
C668 0.1U_0603_25V7M~D
R571 100K_0402_5%~D
GPWR_SRC_ON
R196 100K_0402_5%~D
AGP_PWRON#
<<28,36,41,42,45,46,48>> RUN_ON
Q73
2N7002_SOT23~D
JVID PIN.201, PIN.202, PIN.203 and PIN.204 will contact to GND
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Title VGA connector
Size
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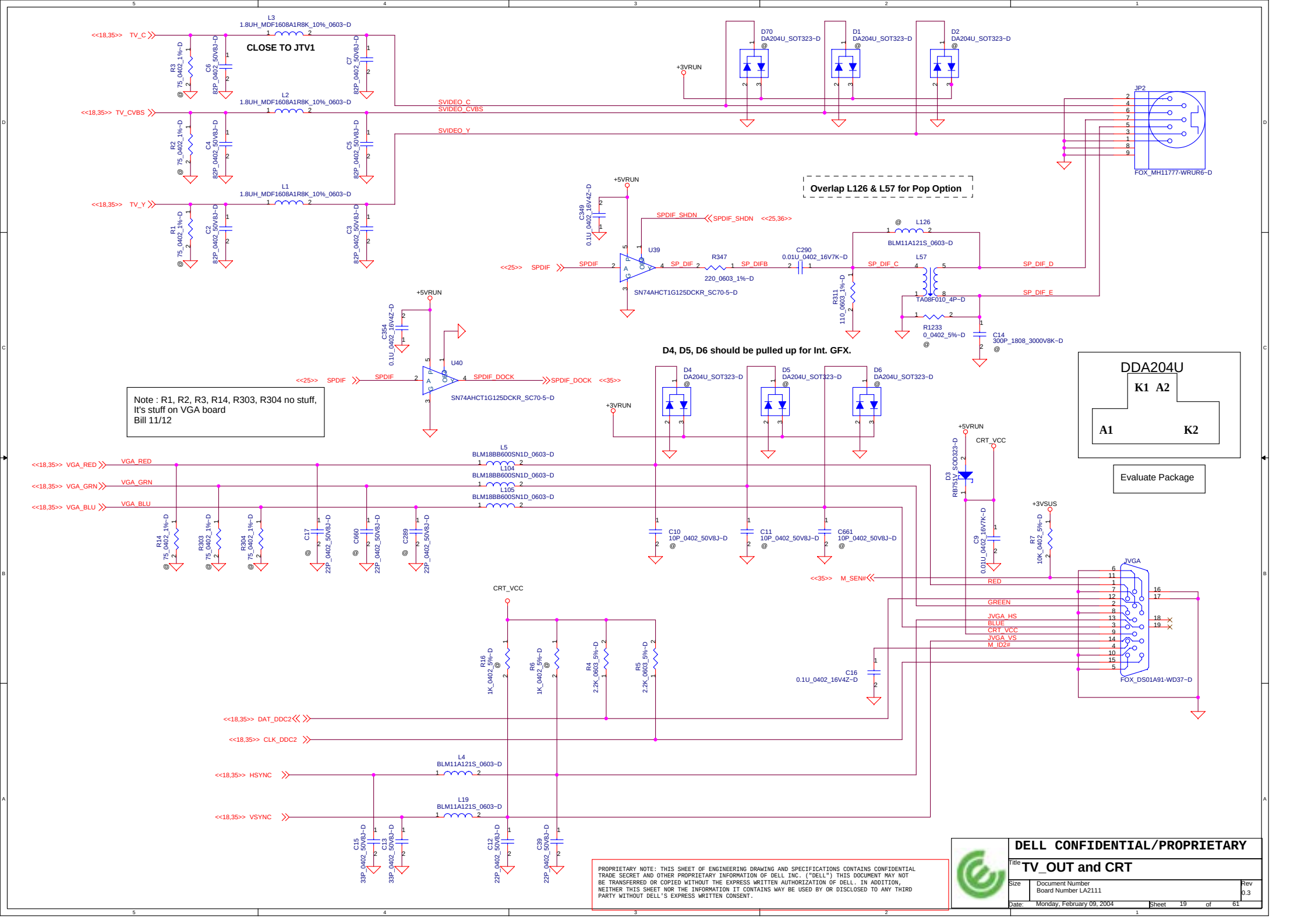
CLOSE TO JTV1
Overlap L126 & L57 for Pop Option
D4, D5, D6 should be pulled up for Int. GFX.
Note : R1, R2, R3, R14, R303, R304 no stuff,
It's stuff on VGA board
Bill 11/12
DDA204U
K1 A2
A1 K2
Evaluate Package
DELL CONFIDENTIAL/PROPRIETARY
TV_OUT and CRT
Size
Document Number
Board Number LA2111
Rev 0.3
Date: Monday, February 09, 2004
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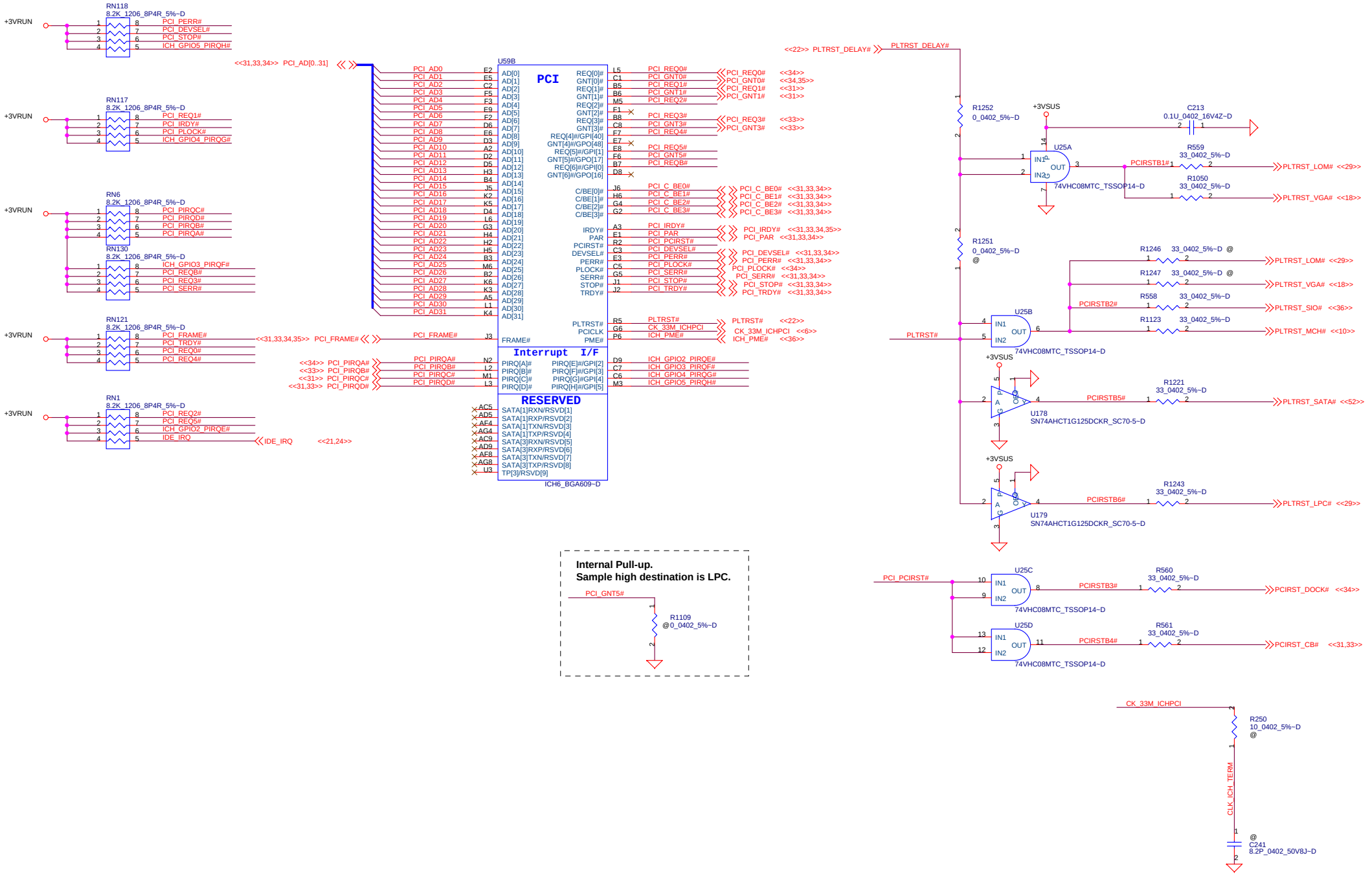

DELL CONFIDENTIAL/PROPRIETARY

Title: **ICH6(1/4)**

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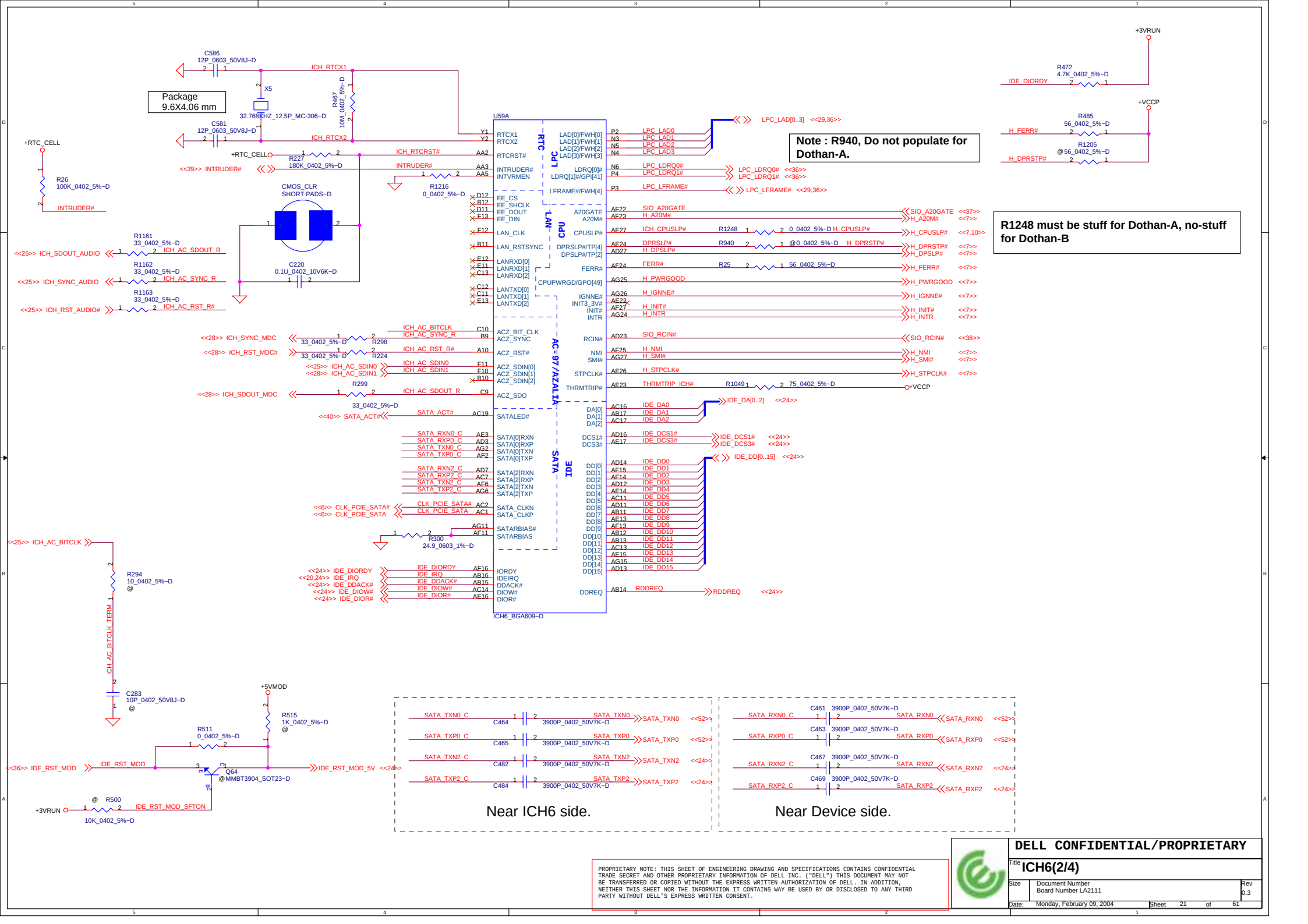

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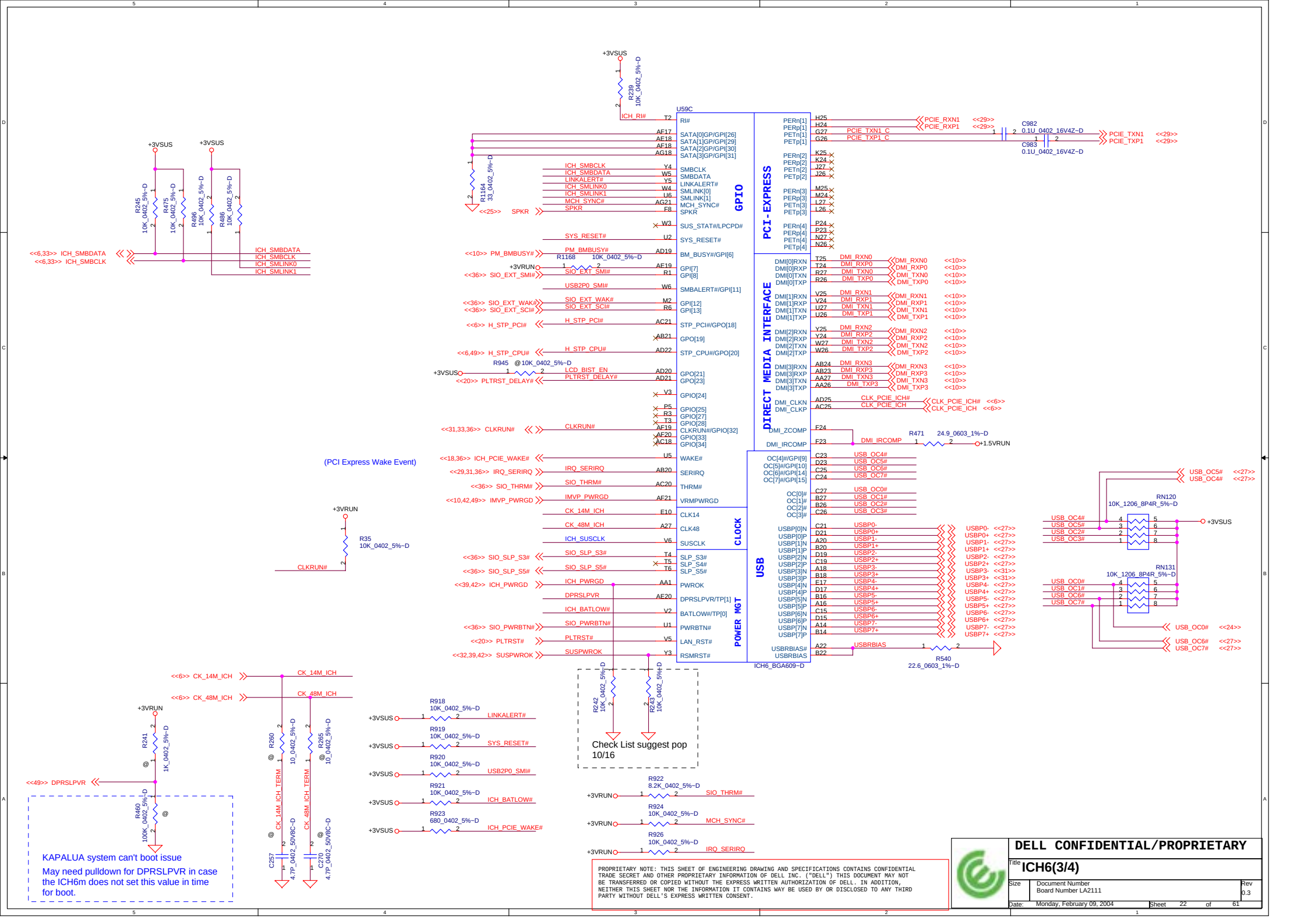
Title: ICH6(2/4)

Size: Document Number: Board Number LA2111 | Rev: 0.3

Date: Monday, February 09, 2004 | Sheet 21 of 61


U59C
GPIO
PCI-EXPRESS
DIRECT MEDIA INTERFACE
CLOCK
USB
POWER MGT
ICH6_BGA609~D
(PCI Express Wake Event)
Check List suggest pop 10/16
KAPALUA system can't boot issue
May need pulldown for DPRSLPVR in case the ICH6m does not set this value in time for boot.
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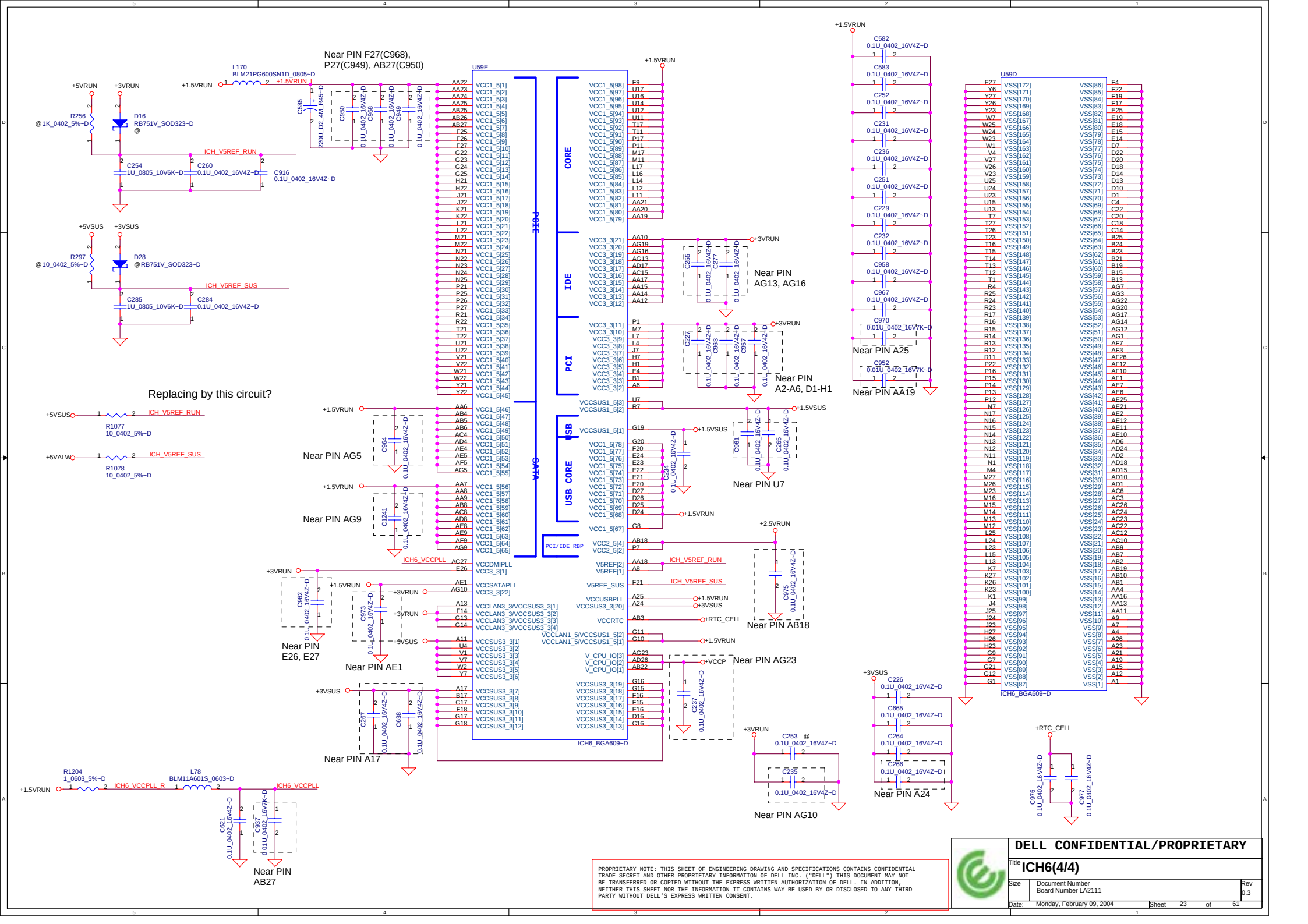
DELL CONFIDENTIAL/PROPRIETARY
Title ICH6(3/4)
Size Document Number Board Number LA2111 Rev 0.3
Date: Monday, February 09, 2004 Sheet 22 of 61



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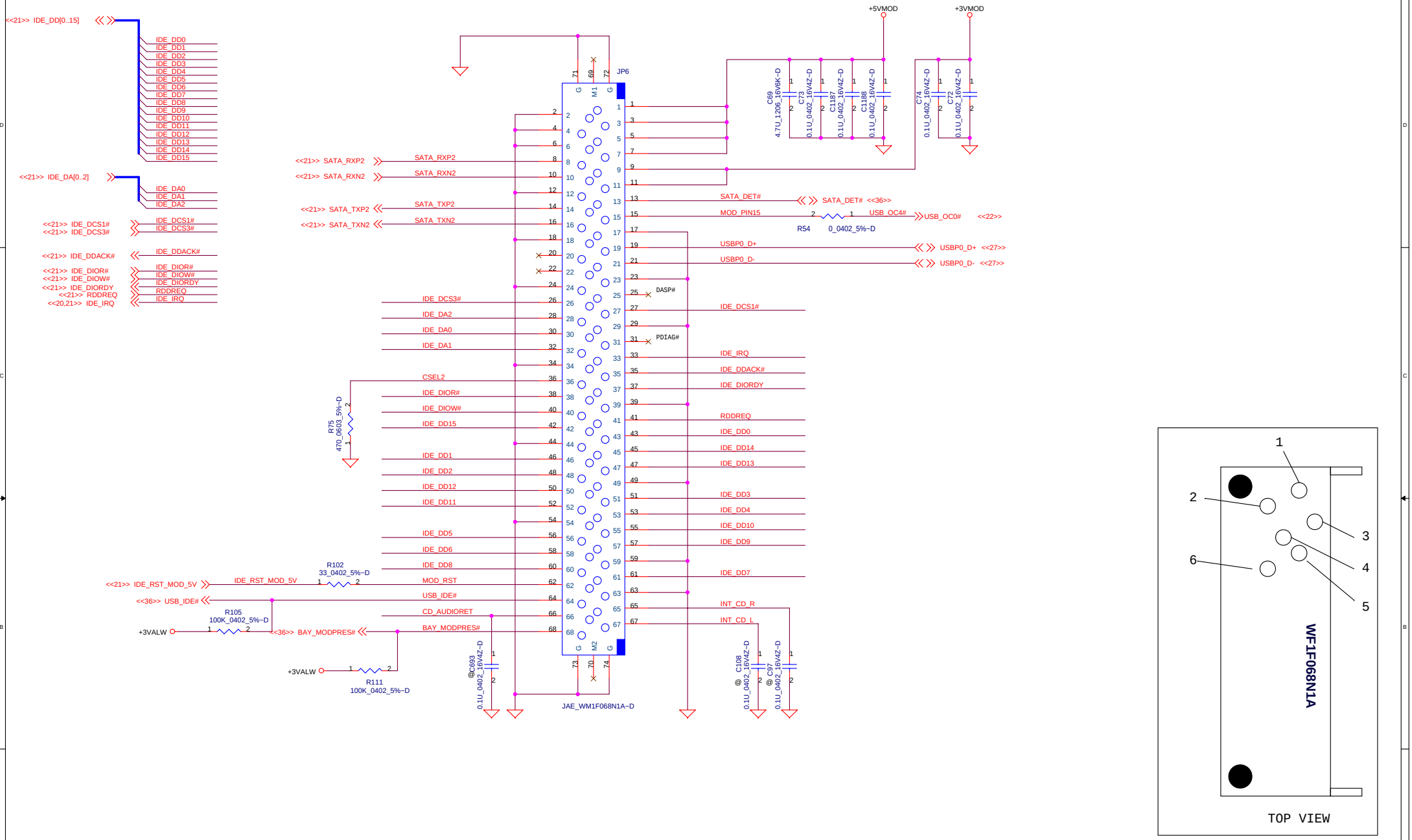

DELL CONFIDENTIAL/PROPRIETARY

Title: DVD MODULE

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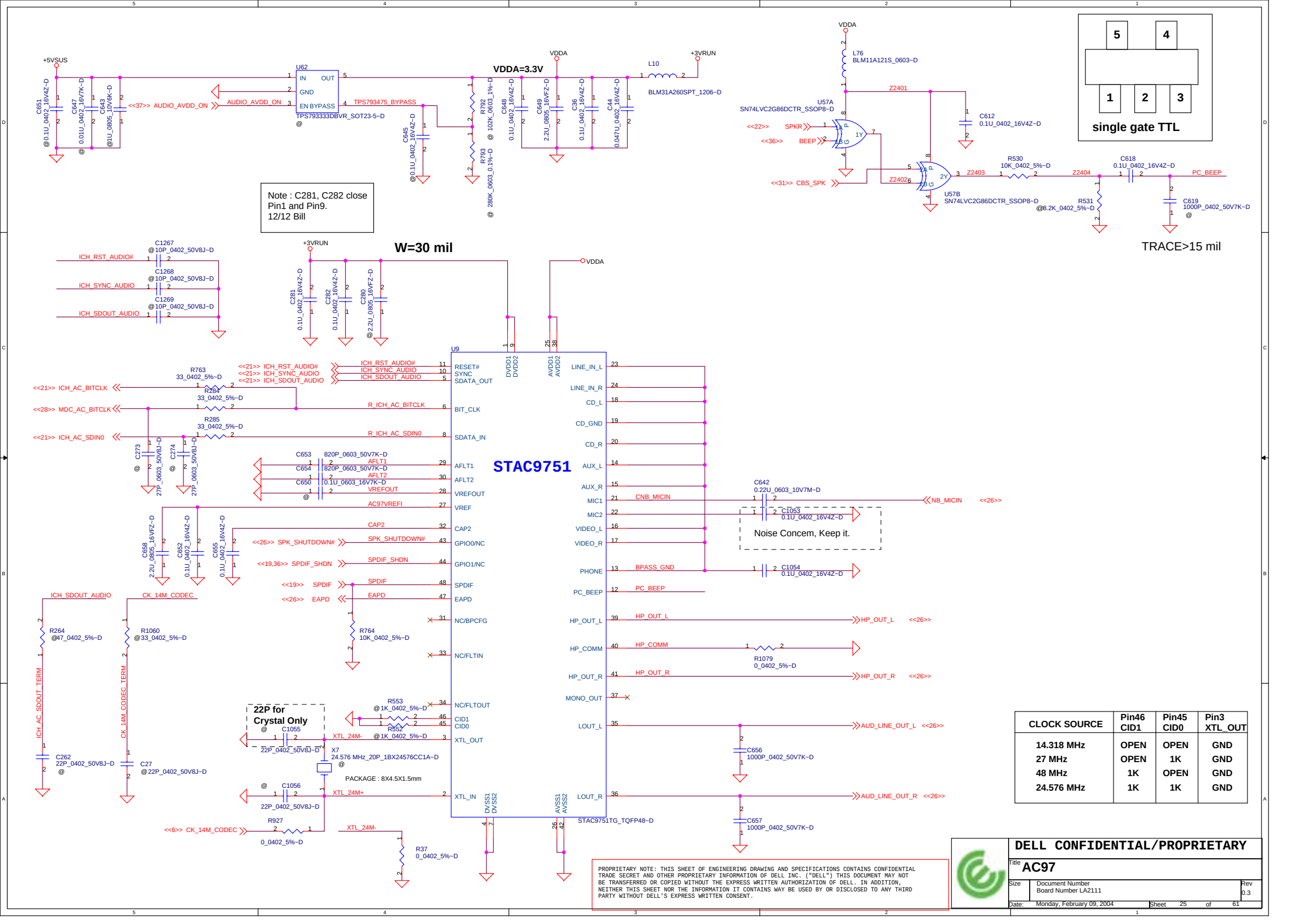
+5VSUS
U62
IN
OUT
GND
EN
BYPASS
TPS793333DBVR_SOT23-5-D
AUDIO_AVDD_ON
TPS793475_BYPASS
VDDA=3.3V
VDDA
+3VRUN
L10
BLM31A260SPT_1206-D
L76
BLM11A121S_0603-D
Z2401
U57A
SN74LVC2G86DCTR_SSOP8-D
SPKR
BEEP
CBS_SPK
Z2402
Z2403
U57B
R530
10K_0402_5%-D
R531
@8.2K_0402_5%-D
Z2404
C618
0.1U_0402_16V4Z-D
PC_BEEP
C619
1000P_0402_50V7K-D
single gate TTL
Note : C281, C282 close Pin1 and Pin9.
12/12 Bill
W=30 mil
TRACE>15 mil
ICH_RST_AUDIO#
ICH_SYNC_AUDIO
ICH_SDOUT_AUDIO
U9
STAC9751
RESET#
SYNC
SDATA_OUT
BIT_CLK
SDATA_IN
AFLT1
AFLT2
VREFOUT
VREF
CAP2
GPIO0/NC
GPIO1/NC
SPDIF
EAPD
NC/BPCFG
NC/FLTIN
NC/FLTOUT
CID1
CID0
XTL_OUT
XTL_IN
DVDD1
DVDD2
AVDD1
AVDD2
DVSS1
DVSS2
AVSS1
AVSS2
LINE_IN_L
LINE_IN_R
CD_L
CD_GND
CD_R
AUX_L
AUX_R
MIC1
MIC2
VIDEO_L
VIDEO_R
PHONE
PC_BEEP
HP_OUT_L
HP_COMM
HP_OUT_R
MONO_OUT
LOUT_L
LOUT_R
STAC9751TG_TQFP48-D
R763
33_0402_5%-D
R284
33_0402_5%-D
R285
33_0402_5%-D
R_ICH_AC_BITCLK
R_ICH_AC_SDIN0
SPK_SHUTDOWN#
SPDIF_SHDN
EAPD
CNB_MICIN
BPASS_GND
HP_OUT_L
HP_COMM
HP_OUT_R
R764
10K_0402_5%-D
R1079
0_0402_5%-D
C642
0.22U_0603_10V7M-D
C1053
0.1U_0402_16V4Z-D
Noise Concem, Keep it.
C1054
0.1U_0402_16V4Z-D
NB_MICIN
HP_OUT_L
HP_OUT_R
AUD_LINE_OUT_L
AUD_LINE_OUT_R
C656
1000P_0402_50V7K-D
C657
1000P_0402_50V7K-D
22P for Crystal Only
C1055
22P_0402_50V8J-D
C1056
22P_0402_50V8J-D
X7
24.576 MHz_20P_1BX24576CC1A-D
PACKAGE : 8X4.5X1.5mm
R553
@1K_0402_5%-D
R552
@1K_0402_5%-D
R927
0_0402_5%-D
R37
0_0402_5%-D
C262
22P_0402_50V8J-D
C27
@22P_0402_50V8J-D
R264
@47_0402_5%-D
R1060
@33_0402_5%-D
ICH_SDOUT_AUDIO
CK_14M_CODEC
ICH_AC_SDOUT_TERM
CK_14M_CODEC_TERM
CLOCK SOURCE
Pin46 CID1
Pin45 CID0
Pin3 XTL_OUT
14.318 MHz OPEN OPEN GND
27 MHz OPEN 1K GND
48 MHz 1K OPEN GND
24.576 MHz 1K 1K GND
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DELL CONFIDENTIAL/PROPRIETARY
Title AC97
Size
Document Number
Board Number LA2111
Rev 0.3
Date: Monday, February 09, 2004
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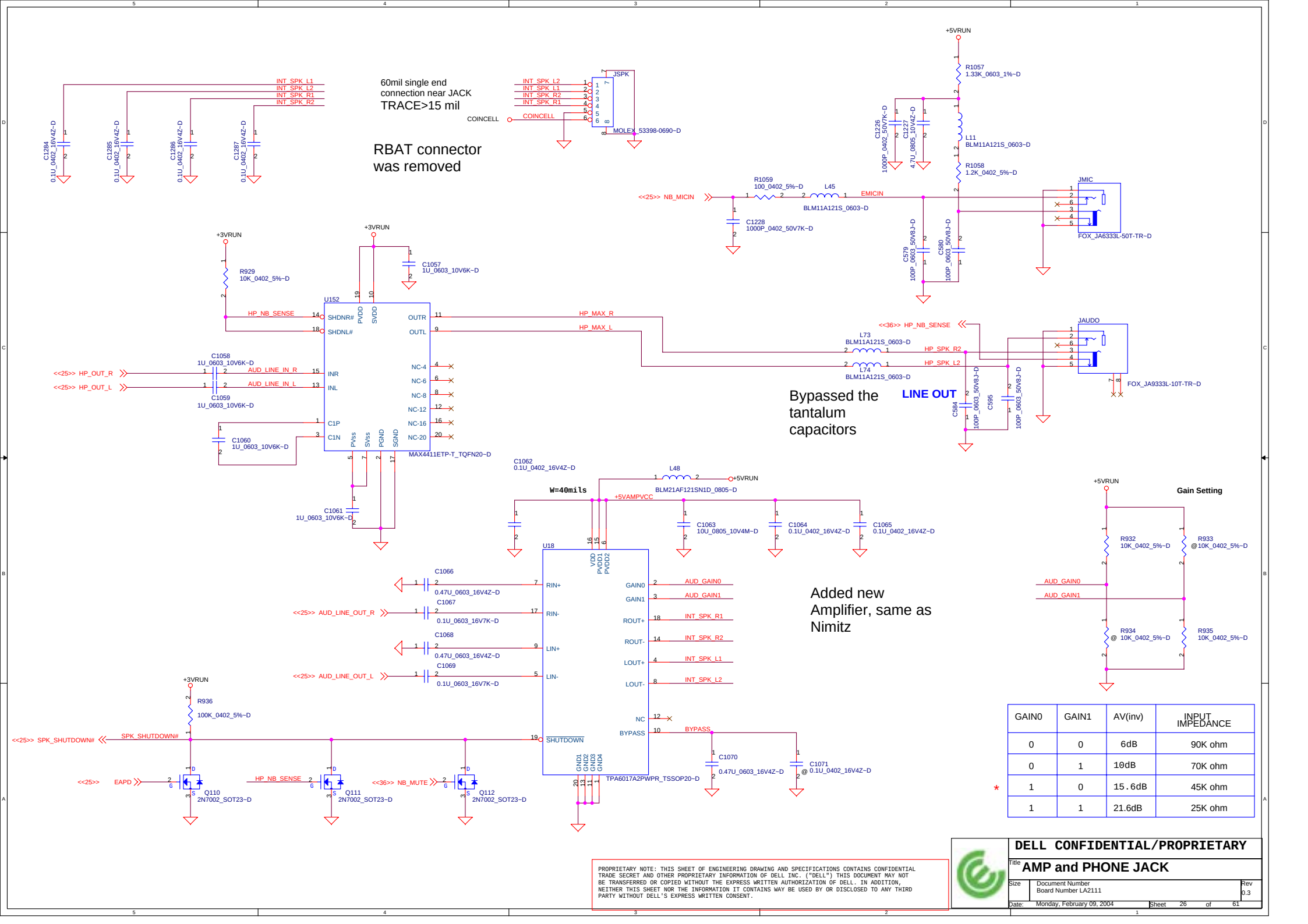

GAIN0	GAIN1	AV(inv)	INPUT IMPEDANCE
0	0	6dB	90K ohm
0	1	10dB	70K ohm
1	0	15.6dB	45K ohm
1	1	21.6dB	25K ohm

*

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Title: AMP and PHONE JACK

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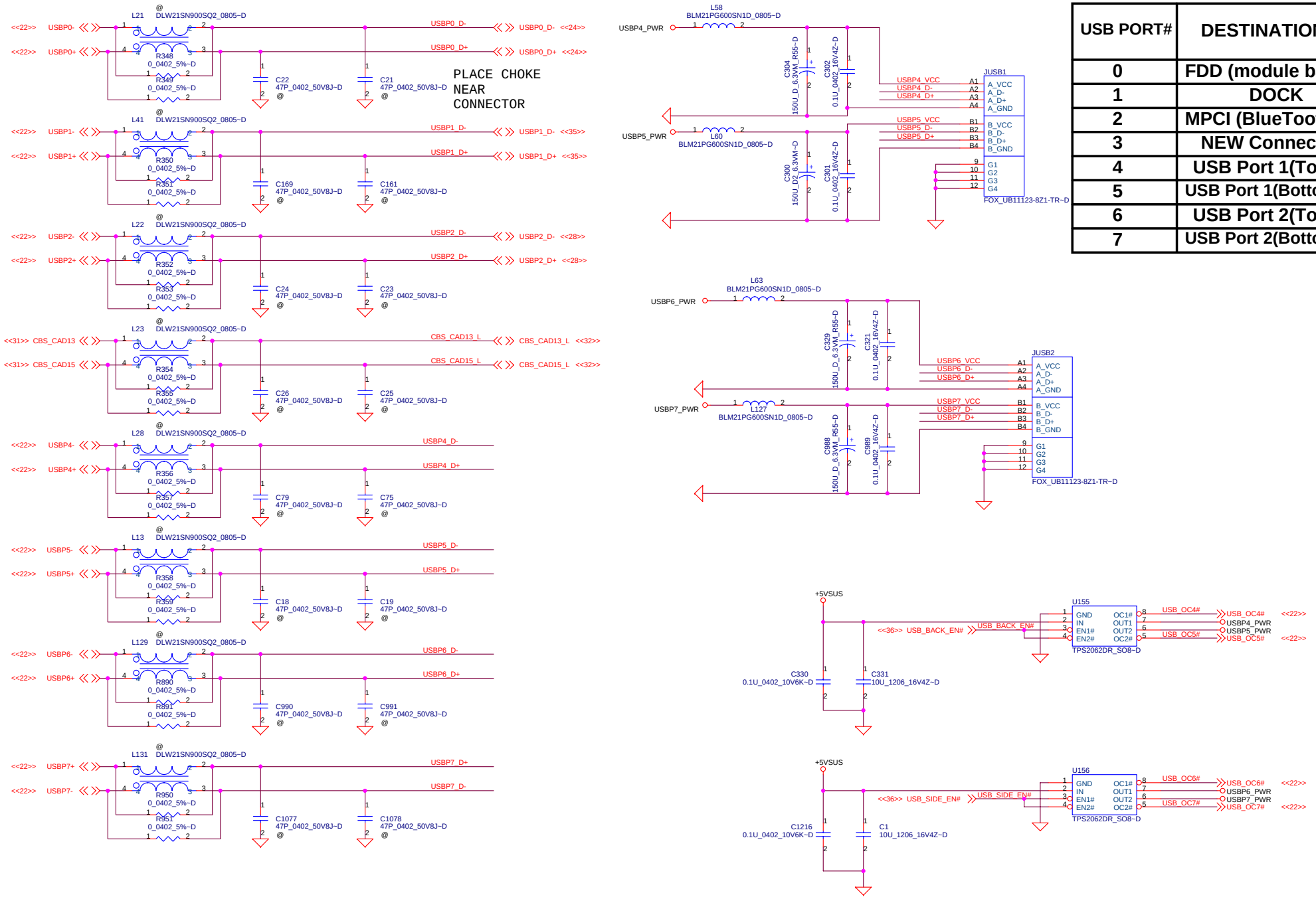

USB PORT#	DESTINATION
0	FDD (module bay)
1	DOCK
2	MPCI (BlueTooth)
3	NEW Connector
4	USB Port 1(Top)
5	USB Port 1(Bottom)
6	USB Port 2(Top)
7	USB Port 2(Bottom)

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Title: USB 2.0

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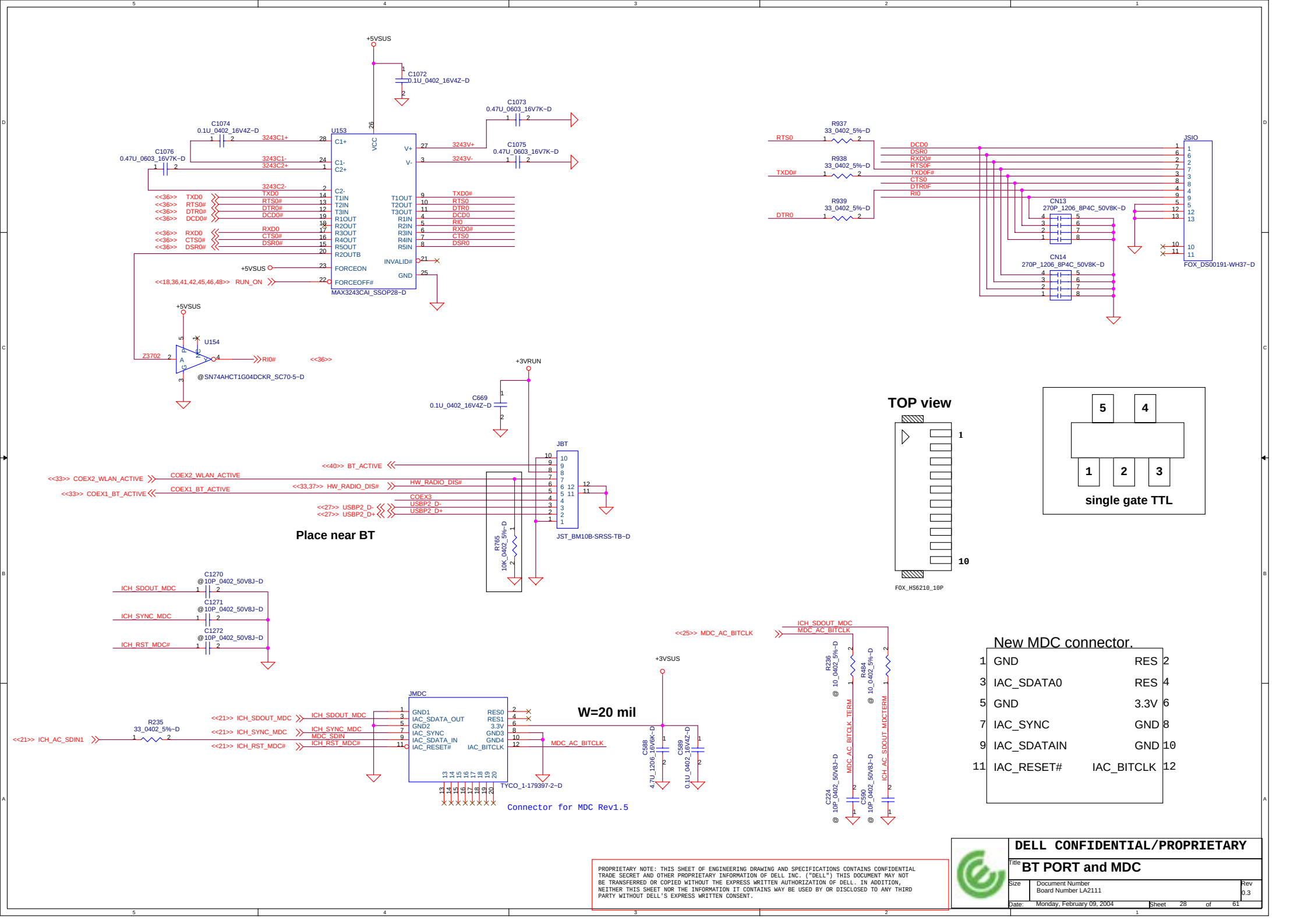

DELL CONFIDENTIAL/PROPRIETARY

Title: **BT PORT and MDC**

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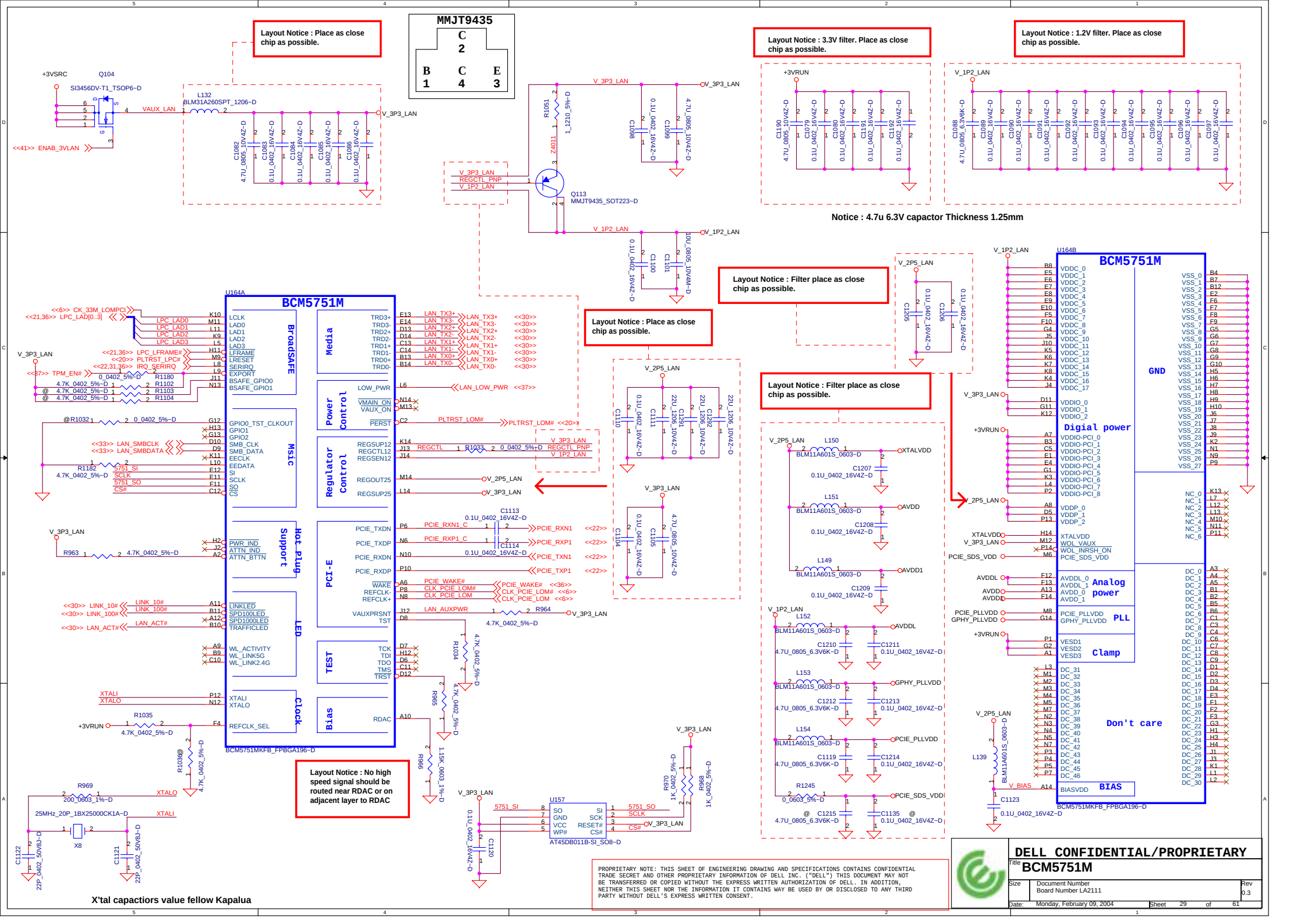
Layout Notice : Place as close chip as possible.
MMJT9435
C 2
B 1
C 4
E 3
Layout Notice : 3.3V filter. Place as close chip as possible.
Layout Notice : 1.2V filter. Place as close chip as possible.
Notice : 4.7u 6.3V capactor Thickness 1.25mm
Layout Notice : Filter place as close chip as possible.
Layout Notice : Place as close chip as possible.
Layout Notice : Filter place as close chip as possible.
Layout Notice : No high speed signal should be routed near RDAC or on adjacent layer to RDAC
X'tal capactiors value fellow Kapalua
BCM5751M
BCM5751MKFB_FPBGA196~D
AT45DB011B-SI_SO8~D
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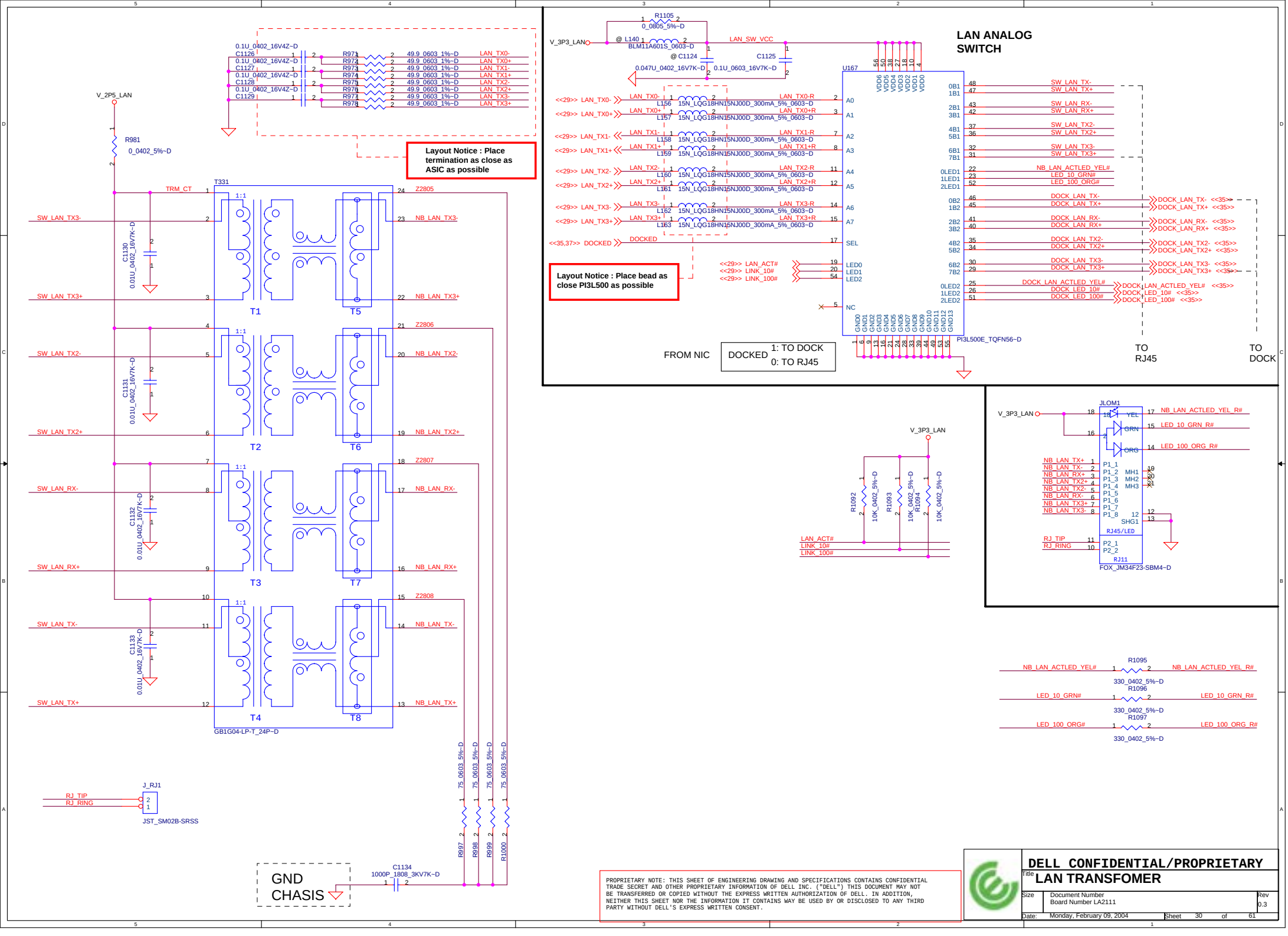
DELL CONFIDENTIAL/PROPRIETARY
Title BCM5751M
Size Document Number Board Number LA2111 Rev 0.3
Date: Monday, February 09, 2004 Sheet 29 of 61


LAN ANALOG SWITCH
Layout Notice : Place termination as close as ASIC as possible
Layout Notice : Place bead as close PI3L500 as possible
FROM NIC
DOCKED 1: TO DOCK 0: TO RJ45
TO RJ45
TO DOCK
PI3L500E_TQFN56~D
GB1G04-LP-T_24P~D
FOX_JM34F23-SBM4~D
JST_SM02B-SRSS
GND CHASIS
DELL CONFIDENTIAL/PROPRIETARY
LAN TRANSFOMER
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Document Number
Board Number LA2111
Rev 0.3
Date: Monday, February 09, 2004
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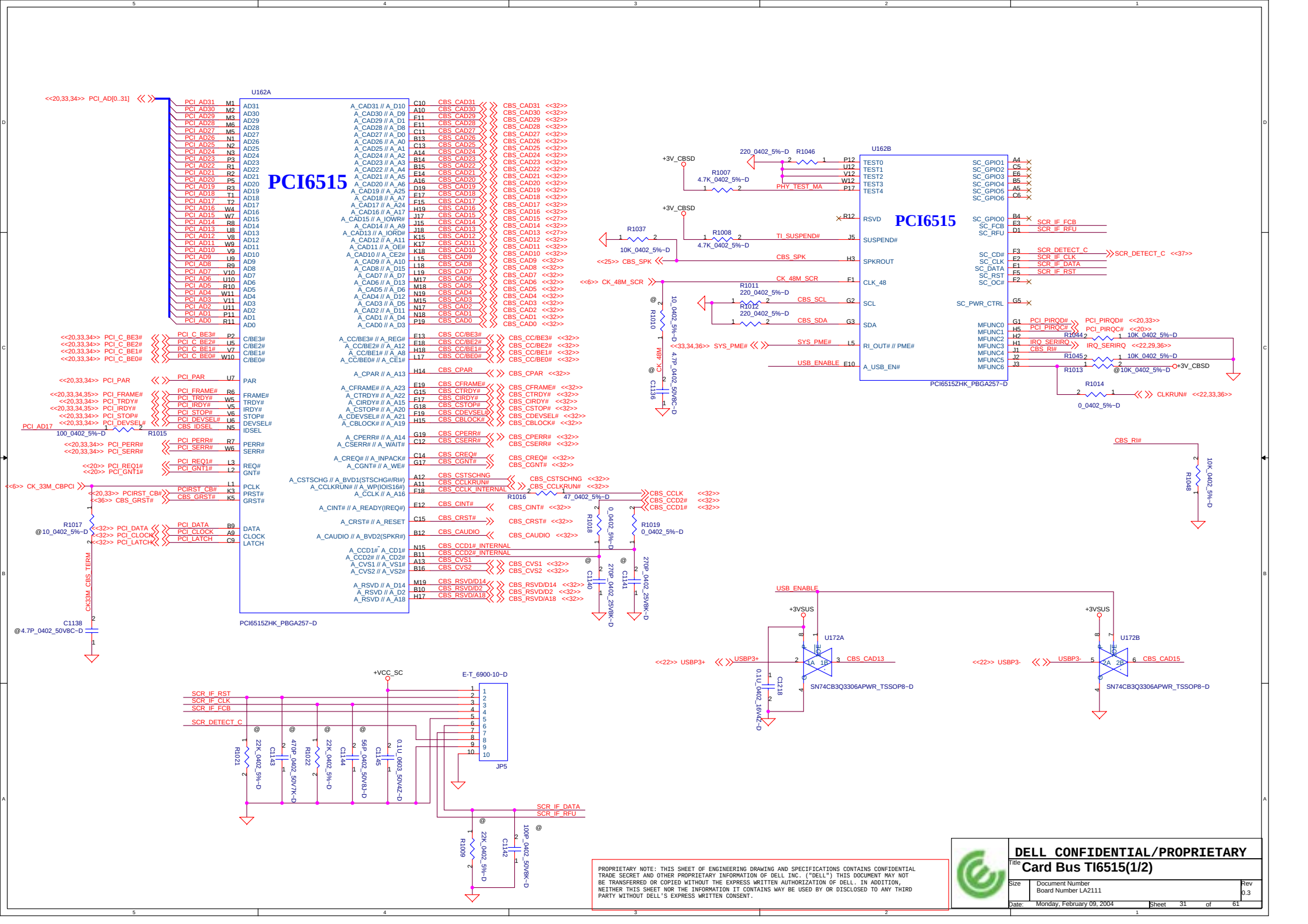
U162A
PCI6515
PCI6515ZHK_PBGA257~D
<<20,33,34>> PCI_AD[0..31]
PCI_AD31 M1
PCI_AD30 M2
PCI_AD29 M3
PCI_AD28 M6
PCI_AD27 M5
PCI_AD26 N1
PCI_AD25 N2
PCI_AD24 N3
PCI_AD23 P3
PCI_AD22 R1
PCI_AD21 R2
PCI_AD20 P5
PCI_AD19 R3
PCI_AD18 T1
PCI_AD17 T2
PCI_AD16 W4
PCI_AD15 W7
PCI_AD14 R8
PCI_AD13 U8
PCI_AD12 V8
PCI_AD11 W9
PCI_AD10 V9
PCI_AD9 U9
PCI_AD8 R9
PCI_AD7 V10
PCI_AD6 U10
PCI_AD5 R10
PCI_AD4 W11
PCI_AD3 V11
PCI_AD2 U11
PCI_AD1 P11
PCI_AD0 R11
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
A_CAD31 // A_D10 C10 CBS_CAD31
A_CAD30 // A_D9 A10 CBS_CAD30
A_CAD29 // A_D1 F11 CBS_CAD29
A_CAD28 // A_D8 E11 CBS_CAD28
A_CAD27 // A_D0 C11 CBS_CAD27
A_CAD26 // A_A0 B13 CBS_CAD26
A_CAD25 // A_A1 C13 CBS_CAD25
A_CAD24 // A_A2 A14 CBS_CAD24
A_CAD23 // A_A3 B14 CBS_CAD23
A_CAD22 // A_A4 B15 CBS_CAD22
A_CAD21 // A_A5 E14 CBS_CAD21
A_CAD20 // A_A6 A16 CBS_CAD20
A_CAD19 // A_A25 D19 CBS_CAD19
A_CAD18 // A_A7 E17 CBS_CAD18
A_CAD17 // A_A24 F15 CBS_CAD17
A_CAD16 // A_A17 H19 CBS_CAD16
A_CAD15 // A_IOWR# J17 CBS_CAD15
A_CAD14 // A_A9 J15 CBS_CAD14
A_CAD13 // A_IORD# J18 CBS_CAD13
A_CAD12 // A_A11 K15 CBS_CAD12
A_CAD11 // A_OE# K17 CBS_CAD11
A_CAD10 // A_CE2# K18 CBS_CAD10
A_CAD9 // A_A10 L15 CBS_CAD9
A_CAD8 // A_D15 L18 CBS_CAD8
A_CAD7 // A_D7 L19 CBS_CAD7
A_CAD6 // A_D13 M17 CBS_CAD6
A_CAD5 // A_D6 M18 CBS_CAD5
A_CAD4 // A_D12 N19 CBS_CAD4
A_CAD3 // A_D5 M15 CBS_CAD3
A_CAD2 // A_D11 N17 CBS_CAD2
A_CAD1 // A_D4 N18 CBS_CAD1
A_CAD0 // A_D3 P19 CBS_CAD0
CBS_CAD31 <<32>>
CBS_CAD30 <<32>>
CBS_CAD29 <<32>>
CBS_CAD28 <<32>>
CBS_CAD27 <<32>>
CBS_CAD26 <<32>>
CBS_CAD25 <<32>>
CBS_CAD24 <<32>>
CBS_CAD23 <<32>>
CBS_CAD22 <<32>>
CBS_CAD21 <<32>>
CBS_CAD20 <<32>>
CBS_CAD19 <<32>>
CBS_CAD18 <<32>>
CBS_CAD17 <<32>>
CBS_CAD16 <<32>>
CBS_CAD15 <<27>>
CBS_CAD14 <<32>>
CBS_CAD13 <<27>>
CBS_CAD12 <<32>>
CBS_CAD11 <<32>>
CBS_CAD10 <<32>>
CBS_CAD9 <<32>>
CBS_CAD8 <<32>>
CBS_CAD7 <<32>>
CBS_CAD6 <<32>>
CBS_CAD5 <<32>>
CBS_CAD4 <<32>>
CBS_CAD3 <<32>>
CBS_CAD2 <<32>>
CBS_CAD1 <<32>>
CBS_CAD0 <<32>>
PCI_C_BE3# P2
PCI_C_BE2# U5
PCI_C_BE1# V7
PCI_C_BE0# W10
C/BE3#
C/BE2#
C/BE1#
C/BE0#
A_CC/BE3# // A_REG# E13 CBS_CC/BE3#
A_CC/BE2# // A_A12 E18 CBS_CC/BE2#
A_CC/BE1# // A_A8 U18 CBS_CC/BE1#
A_CC/BE0# // A_CE1# L17 CBS_CC/BE0#
CBS_CC/BE3# <<32>>
CBS_CC/BE2# <<32>>
CBS_CC/BE1# <<32>>
CBS_CC/BE0# <<32>>
PCI_PAR U7
PAR
A_CPAR // A_A13 H14 CBS_CPAR
CBS_CPAR <<32>>
PCI_FRAME# R6
PCI_TRDY# W5
PCI_IRDY# V5
PCI_STOP# V6
PCI_DEVSEL# U6
CBS_IDSEL N5
FRAME#
TRDY#
IRDY#
STOP#
DEVSEL#
IDSEL
A_CFRAME# // A_A23 E19 CBS_CFRAME#
A_CTRDY# // A_A22 G15 CBS_CTRDY#
A_CIRDY# // A_A15 F17 CBS_CIRDY#
A_CSTOP# // A_A20 G18 CBS_CSTOP#
A_CDEVSEL# // A_A21 F19 CBS_CDEVSEL#
A_CBLOCK# // A_A19 H15 CBS_CBLOCK#
CBS_CFRAME# <<32>>
CBS_CTRDY# <<32>>
CBS_CIRDY# <<32>>
CBS_CSTOP# <<32>>
CBS_CDEVSEL# <<32>>
CBS_CBLOCK# <<32>>
PCI_PERR# R7
PCI_SERR# W6
PERR#
SERR#
A_CPERR# // A_A14 G19 CBS_CPERR#
A_CSERR# // A_WAIT# C12 CBS_CSERR#
CBS_CPERR# <<32>>
CBS_CSERR# <<32>>
PCI_REQ1# L3
PCI_GNT1# L2
REQ#
GNT#
A_CREQ# // A_INPACK# C14 CBS_CREQ#
A_CGNT# // A_WE# G17 CBS_CGNT#
CBS_CREQ# <<32>>
CBS_CGNT# <<32>>
PCIRST_CB# K3
CBS_GRST# K5
PCLK
PRST#
GRST#
A_CSTSCHG // A_BVD1(STSCHG#/RI#) A12 CBS_CSTSCHNG
A_CCLKRUN# // A_WP(IOIS16#) A11 CBS_CCLKRUN#
A_CCLK // A_A16 F18 CBS_CCLK_INTERNAL
CBS_CSTSCHNG <<32>>
CBS_CCLKRUN# <<32>>
A_CINT# // A_READY(IREQ#) E12 CBS_CINT#
CBS_CINT# <<32>>
A_CRST# // A_RESET C15 CBS_CRST#
CBS_CRST# <<32>>
A_CAUDIO // A_BVD2(SPKR#) B12 CBS_CAUDIO
CBS_CAUDIO <<32>>
PCI_DATA B9
PCI_CLOCK A9
PCI_LATCH C9
DATA
CLOCK
LATCH
A_CCD1# // A_CD1# N15 CBS_CCD1#_INTERNAL
A_CCD2# // A_CD2# B11 CBS_CCD2#_INTERNAL
A_CVS1 // A_VS1# A13 CBS_CVS1
A_CVS2 // A_VS2# B16 CBS_CVS2
CBS_CVS1 <<32>>
CBS_CVS2 <<32>>
A_RSVD // A_D14 M19 CBS_RSVD/D14
A_RSVD // A_D2 B10 CBS_RSVD/D2
A_RSVD // A_A18 H17 CBS_RSVD/A18
CBS_RSVD/D14 <<32>>
CBS_RSVD/D2 <<32>>
CBS_RSVD/A18 <<32>>
CBS_CCLK <<32>>
CBS_CCD2# <<32>>
CBS_CCD1# <<32>>
<<6>> CK_33M_CBPCI
<<20,33>> PCIRST_CB#
<<36>> CBS_GRST#
<<32>> PCI_DATA
<<32>> PCI_CLOCK
<<32>> PCI_LATCH
<<20,33,34>> PCI_PAR
<<20,33,34,35>> PCI_FRAME#
<<20,33,34>> PCI_TRDY#
<<20,33,34,35>> PCI_IRDY#
<<20,33,34>> PCI_STOP#
<<20,33,34>> PCI_DEVSEL#
<<20,33,34>> PCI_PERR#
<<20,33,34>> PCI_SERR#
<<20>> PCI_REQ1#
<<20>> PCI_GNT1#
PCI_AD17
<<20,33,34>> PCI_C_BE3#
<<20,33,34>> PCI_C_BE2#
<<20,33,34>> PCI_C_BE1#
<<20,33,34>> PCI_C_BE0#
R1015 100_0402_5%~D
R1016 47_0402_5%~D
R1017 @10_0402_5%~D
R1018 0_0402_5%~D
R1019 0_0402_5%~D
C1136 @ CK_48M 10_0402_5%~D 4.7P_0402_50V8C~D
C1138 @4.7P_0402_50V8C~D
C1140 @ 270P_0402_25V8K~D
C1141 @ 270P_0402_25V8K~D
CK33M_CBS_TERM
U162B
PCI6515
PCI6515ZHK_PBGA257~D
+3V_CBSD
R1007 4.7K_0402_5%~D
R1008 4.7K_0402_5%~D
R1037 10K_0402_5%~D
R1046 220_0402_5%~D
PHY_TEST_MA
TI_SUSPEND#
CBS_SPK
<<25>> CBS_SPK
<<6>> CK_48M_SCR
CK_48M_SCR
R1011 220_0402_5%~D
R1012 220_0402_5%~D
CBS_SCL
CBS_SDA
<<33,34,36>> SYS_PME#
SYS_PME#
USB_ENABLE
TEST0 P12
TEST1 U12
TEST2 V12
TEST3 W12
TEST4 P17
RSVD R12
SUSPEND# J5
SPKROUT H3
CLK_48 F1
SCL G2
SDA G3
RI_OUT# // PME# L5
A_USB_EN# E10
SC_PWR_CTRL G5
SC_GPIO1 A4
SC_GPIO2 C5
SC_GPIO3 E6
SC_GPIO4 B5
SC_GPIO5 A5
SC_GPIO6 C6
SC_GPIO0 B4
SC_FCB E3
SC_RFU D1
SC_CD# F3
SC_CLK E2
SC_DATA E1
SC_RST F5
SC_OC# F2
MFUNC0 G1
MFUNC1 H5
MFUNC2 H2
MFUNC3 H1
MFUNC4 J1
MFUNC5 J2
MFUNC6 J3
SCR_IF_FCB
SCR_IF_RFU
SCR_DETECT_C
SCR_IF_CLK
SCR_IF_DATA
SCR_IF_RST
SCR_DETECT_C <<37>>
PCI_PIRQD# <<20,33>>
PCI_PIRQC# <<20>>
IRQ_SERIRQ <<22,29,36>>
CBS_RI#
CLKRUN# <<22,33,36>>
R1044 10K_0402_5%~D
R1045 10K_0402_5%~D
R1013 @10K_0402_5%~D
R1014 0_0402_5%~D
+3V_CBSD
R1048 10K_0402_5%~D
USB_ENABLE
+3VSUS
U172A
U172B
SN74CB3Q3306APWR_TSSOP8~D
<<22>> USBP3+
USBP3+
CBS_CAD13
<<22>> USBP3-
USBP3-
CBS_CAD15
C1218 0.1U_0402_16V4Z~D
+VCC_SC
E-T_6900-10~D
JP5
SCR_IF_RST
SCR_IF_CLK
SCR_IF_FCB
SCR_DETECT_C
SCR_IF_DATA
SCR_IF_RFU
R1021 22K_0402_5%~D
C1143 470P_0402_50V7K~D
R1022 22K_0402_5%~D
C1144 56P_0402_50V8J~D
C1145 0.1U_0603_50V4Z~D
R1009 22K_0402_5%~D
C1142 100P_0402_50V8K~D
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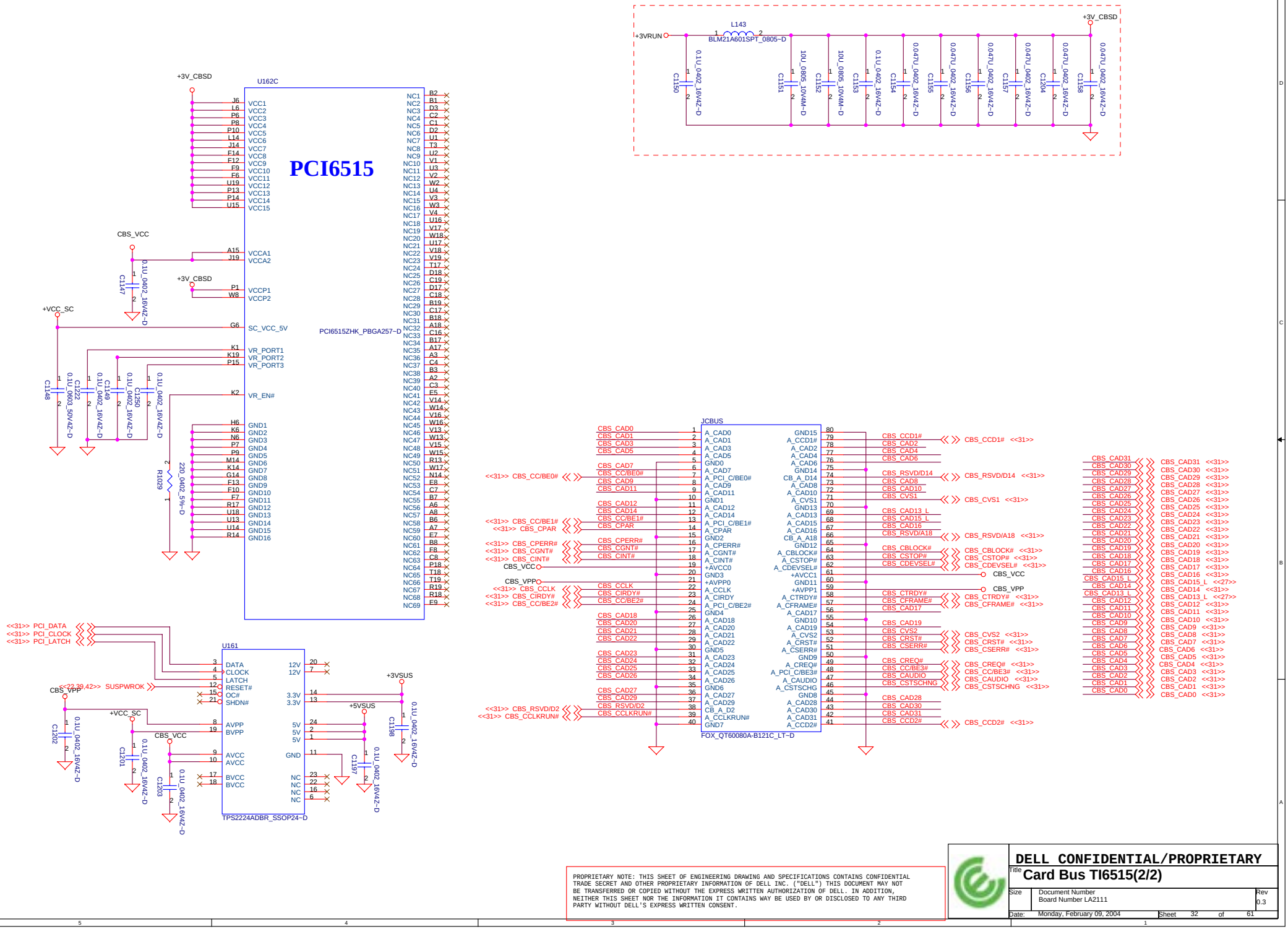
DELL CONFIDENTIAL/PROPRIETARY
Title Card Bus TI6515(1/2)
Size
Document Number
Board Number LA2111
Rev 0.3
Date: Monday, February 09, 2004
Sheet 31 of 61



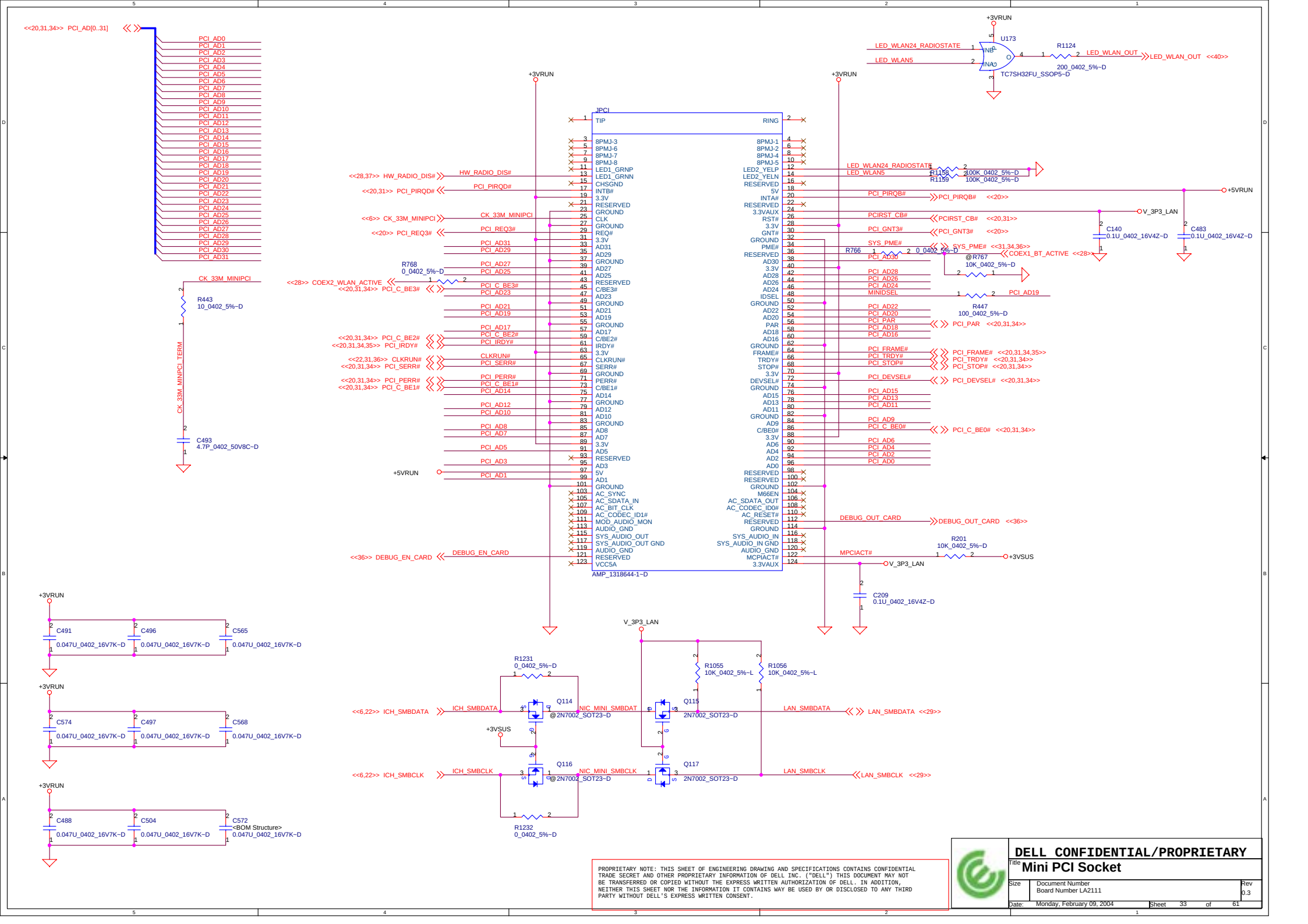
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

DELL CONFIDENTIAL/PROPRIETARY

Title: **Card Bus TI6515(2/2)**

Size	Document Number	Rev
	Board Number LA2111	0.3

Date: Monday, February 09, 2004 Sheet 32 of 61



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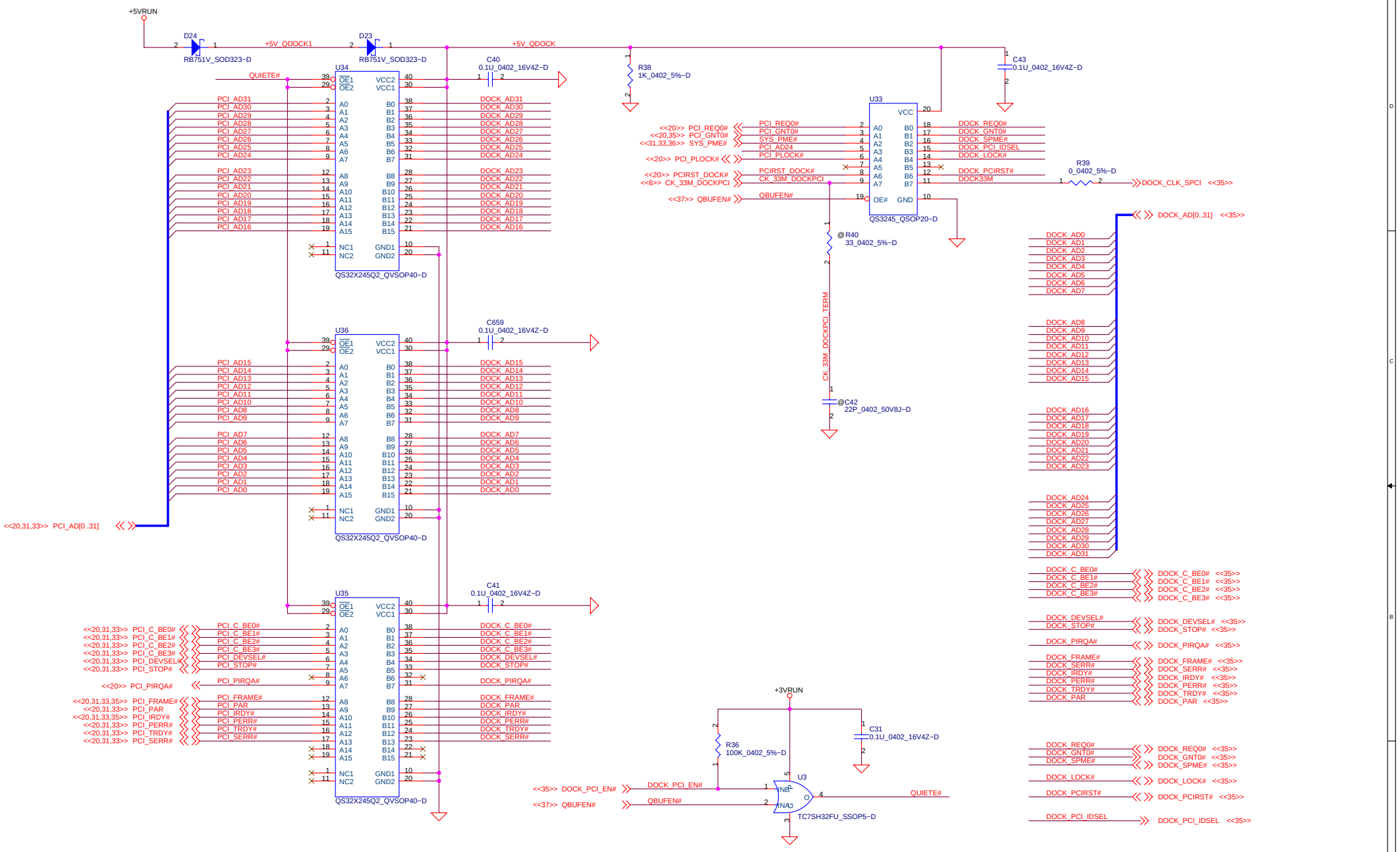
DELL CONFIDENTIAL/PROPRIETARY

Title: **Mini PCI Socket**

Size	Document Number	Rev
	Board Number LA2111	0.3

Date: Monday, February 09, 2004 Sheet 33 of 61

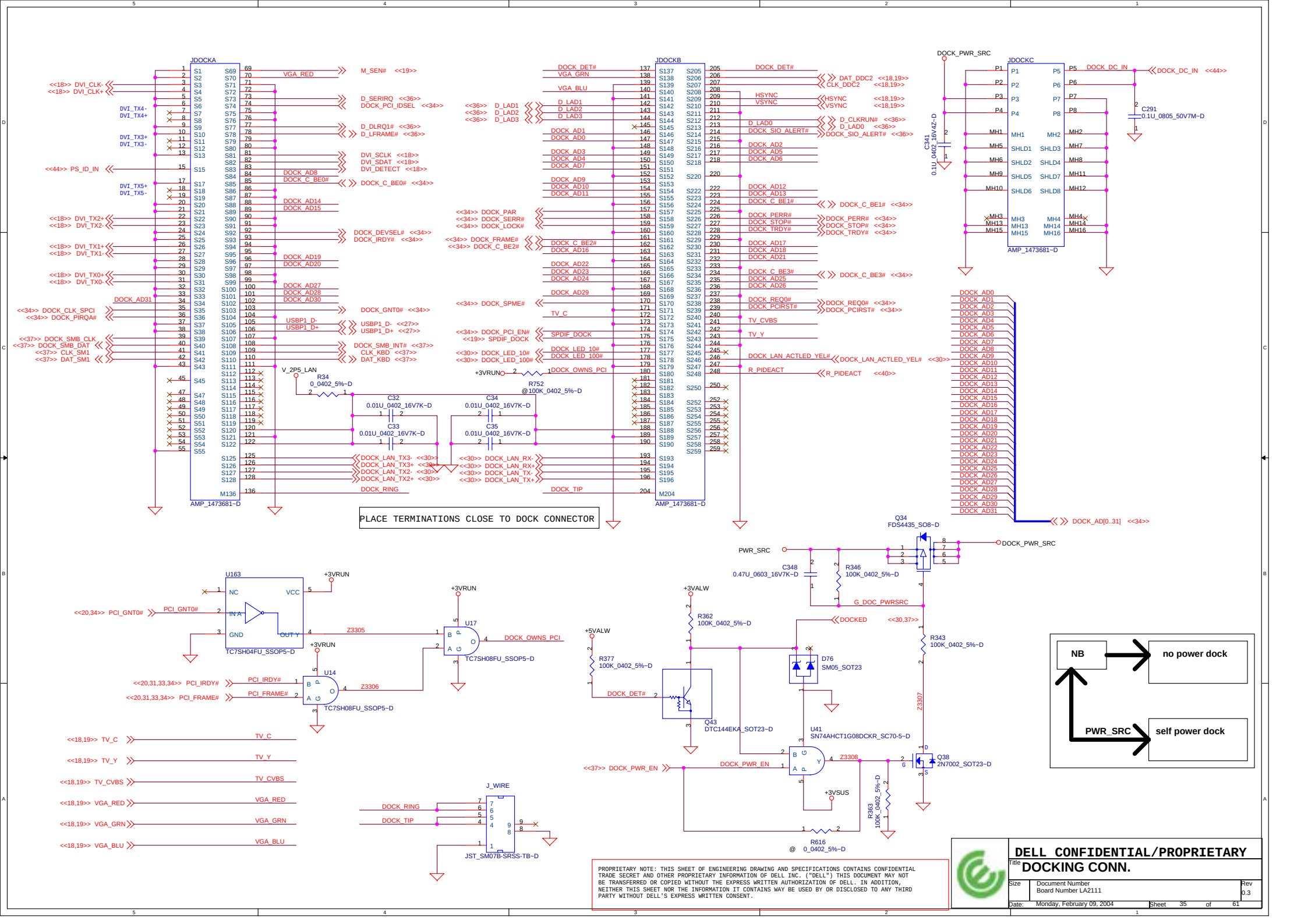


DELL CONFIDENTIAL/PROPRIETARY

Title: **DOCKING BUFFER**

Size	Document Number	Rev
	Board Number LA2111	0.3

Date: Monday, February 09, 2004 Sheet 34 of 61



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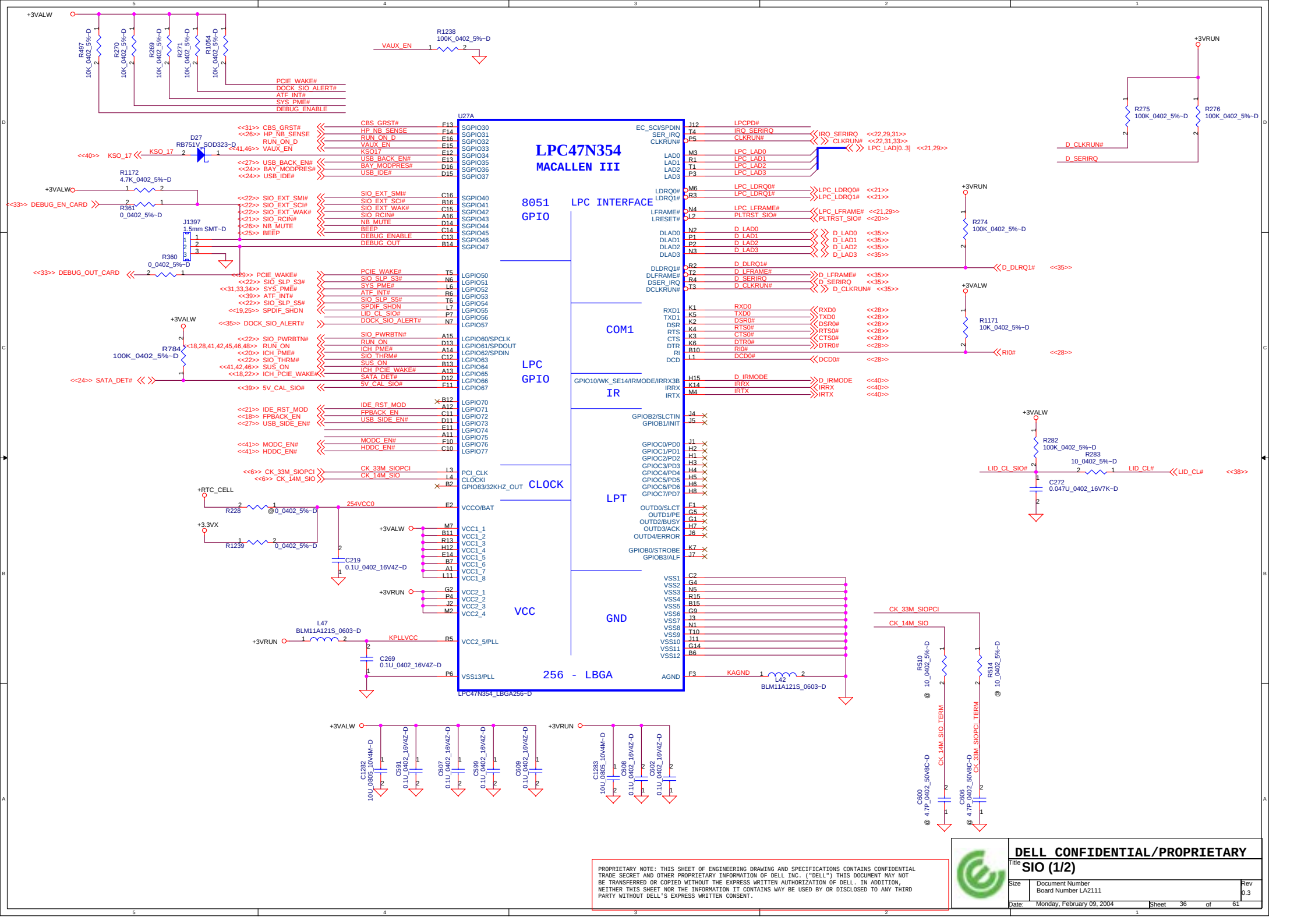
DELL CONFIDENTIAL/PROPRIETARY

Title: **DOCKING CONN.**

Size	Document Number	Rev
	Board Number LA2111	0.3

Date: Monday, February 09, 2004 Sheet 35 of 61


LPC47N354
MACALLEN III
U27A
8051
GPIO
LPC INTERFACE
LPC
GPIO
COM1
IR
CLOCK
LPT
VCC
GND
256 - LBGA
LPC47N354_LBGA256~D
+3VALW
+3VRUN
+3.3VX
+RTC_CELL
DEBUG_EN_CARD
DEBUG_OUT_CARD
SATA_DET#
PCIE_WAKE#
DOCK_SIO_ALERT#
SYS_PME#
ATF_INT#
DEBUG_ENABLE
VAUX_EN
CBS_GRST#
HP_NB_SENSE
RUN_ON_D
KSO17
USB_BACK_EN#
BAY_MODPRES#
USB_IDE#
SIO_EXT_SMI#
SIO_EXT_SCI#
SIO_EXT_WAK#
SIO_RCIN#
NB_MUTE
BEEP
DEBUG_OUT
SIO_SLP_S3#
SIO_SLP_S5#
SPDIF_SHDN
LID_CL_SIO#
SIO_PWRBTN#
RUN_ON
ICH_PME#
SIO_THRM#
SUS_ON
ICH_PCIE_WAKE#
5V_CAL_SIO#
IDE_RST_MOD
FPBACK_EN
USB_SIDE_EN#
MODC_EN#
HDDC_EN#
CK_33M_SIOPCI
CK_14M_SIO
254VCC0
KPLLVCC
LPCPD#
IRQ_SERIRQ
CLKRUN#
LPC_LAD0
LPC_LAD1
LPC_LAD2
LPC_LAD3
LPC_LDRQ0#
LPC_LDRQ1#
LPC_LFRAME#
PLTRST_SIO#
D_LAD0
D_LAD1
D_LAD2
D_LAD3
D_DLRQ1#
D_LFRAME#
D_SERIRQ
D_CLKRUN#
RXD0
TXD0
DSR0#
RTS0#
CTS0#
DTR0#
RI0#
DCD0#
D_IRMODE
IRRX
IRTX
KAGND
LID_CL#
D_CLKRUN#
D_SERIRQ
R497 10K_0402_5%~D
R270 10K_0402_5%~D
R269 10K_0402_5%~D
R271 10K_0402_5%~D
R1054 10K_0402_5%~D
R1238 100K_0402_5%~D
R275 100K_0402_5%~D
R276 100K_0402_5%~D
R274 100K_0402_5%~D
R1171 10K_0402_5%~D
R1172 4.7K_0402_5%~D
R361 0_0402_5%~D
R360 0_0402_5%~D
R784 100K_0402_5%~D
R228 @0_0402_5%~D
R1239 0_0402_5%~D
R282 100K_0402_5%~D
R283 10_0402_5%~D
R510 @ 10_0402_5%~D
R514 @ 10_0402_5%~D
D27 RB751V_SOD323~D
J1397 1.5mm SMT~D
L47 BLM11A121S_0603~D
L42 BLM11A121S_0603~D
C219 0.1U_0402_16V4Z~D
C269 0.1U_0402_16V4Z~D
C272 0.047U_0402_16V7K~D
C1282 10U_0805_10V4M~D
C591 0.1U_0402_16V4Z~D
C607 0.1U_0402_16V4Z~D
C599 0.1U_0402_16V4Z~D
C609 0.1U_0402_16V4Z~D
C1283 10U_0805_10V4M~D
C608 0.1U_0402_16V4Z~D
C602 0.1U_0402_16V4Z~D
C600 @ 4.7P_0402_50V8C~D
C606 @ 4.7P_0402_50V8C~D
CK_14M_SIO_TERM
CK_33M_SIOPCI_TERM
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DELL CONFIDENTIAL/PROPRIETARY
Title SIO (1/2)
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Date: Monday, February 09, 2004
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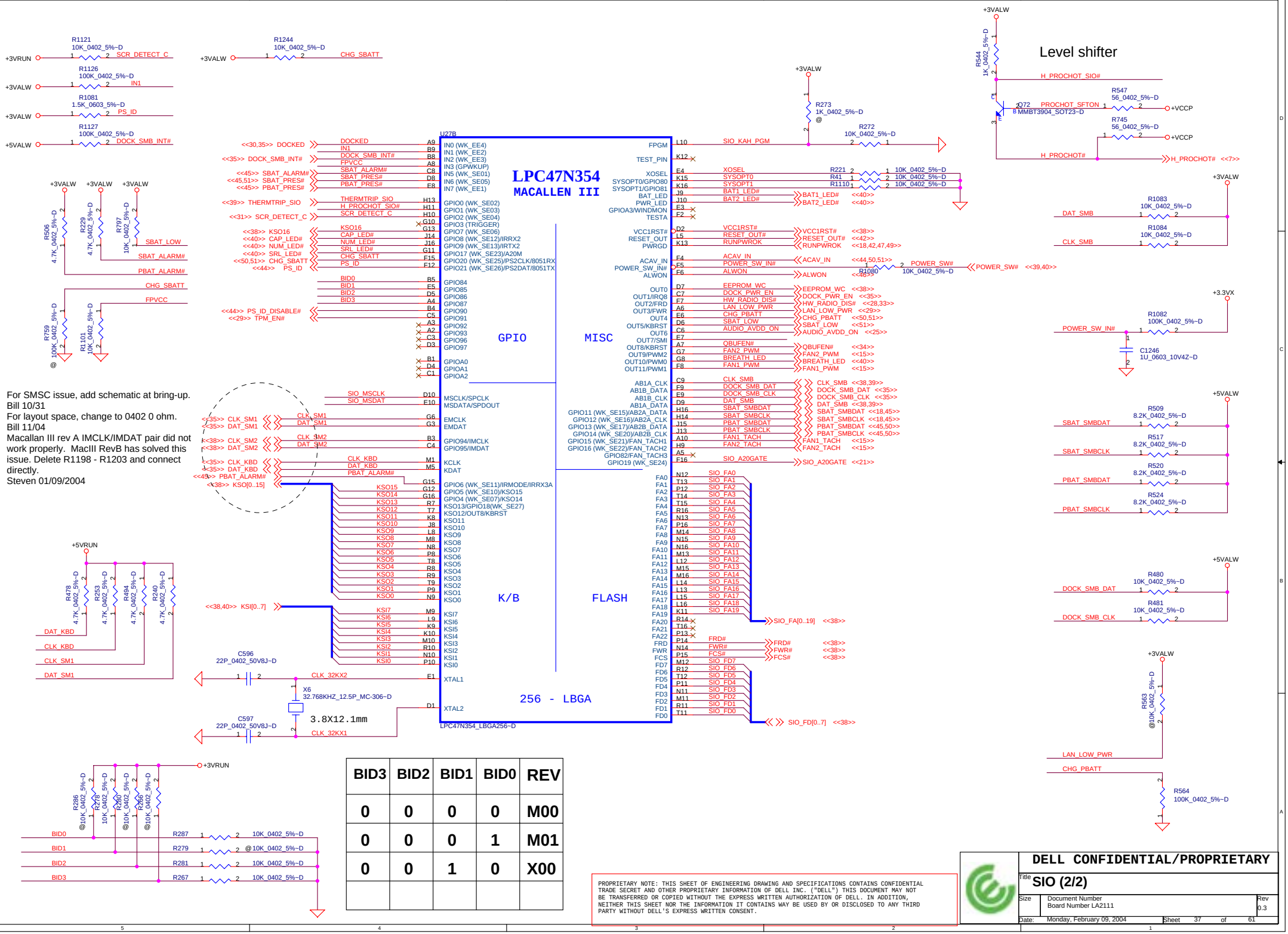
Level shifter
LPC47N354
MACALLEN III
GPIO
MISC
K/B
FLASH
256 - LBGA
LPC47N354_LBGA256~D
For SMSC issue, add schematic at bring-up.
Bill 10/31
For layout space, change to 0402 0 ohm.
Bill 11/04
Macallan III rev A IMCLK/IMDAT pair did not work properly. MacIII RevB has solved this issue. Delete R1198 - R1203 and connect directly.
Steven 01/09/2004
3.8X12.1mm
BID3 BID2 BID1 BID0 REV
0 0 0 0 M00
0 0 0 1 M01
0 0 1 0 X00
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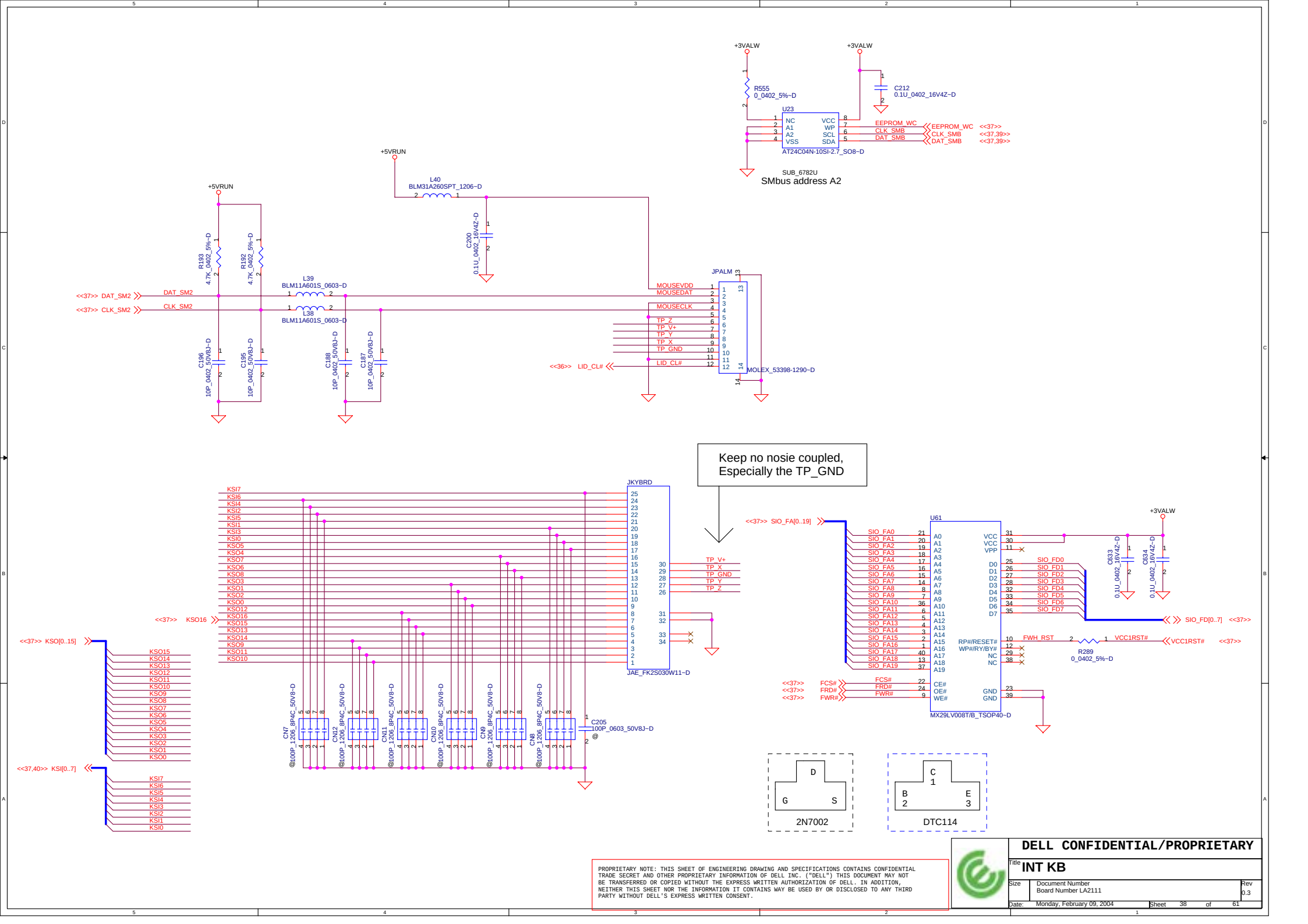
DELL CONFIDENTIAL/PROPRIETARY
Title SIO (2/2)
Size Document Number Board Number LA2111 Rev 0.3
Date: Monday, February 09, 2004 Sheet 37 of 61


+3VALW
+3VALW
R555
0_0402_5%~D
C212
0.1U_0402_16V4Z~D
U23
NC
A1
A2
VSS
VCC
WP
SCL
SDA
EEPROM_WC
CLK_SMB
DAT_SMB
<<37>>
<<37,39>>
<<37,39>>
AT24C04N-10SI-2.7_SO8~D
SUB_6782U
SMbus address A2
+5VRUN
L40
BLM31A260SPT_1206~D
C200
0.1U_0402_16V4Z~D
+5VRUN
R193
4.7K_0402_5%~D
R192
4.7K_0402_5%~D
L39
BLM11A601S_0603~D
L38
BLM11A601S_0603~D
<<37>> DAT_SM2
<<37>> CLK_SM2
DAT_SM2
CLK_SM2
C196
10P_0402_50V8J~D
C195
10P_0402_50V8J~D
C188
10P_0402_50V8J~D
C187
10P_0402_50V8J~D
JPALM
MOUSEVDD
MOUSEDAT
MOUSECLK
TP_Z
TP_V+
TP_Y
TP_X
TP_GND
LID_CL#
<<36>> LID_CL#
MOLEX_53398-1290~D
Keep no nosie coupled,
Especially the TP_GND
JKYBRD
KSI7
KSI6
KSI4
KSI2
KSI5
KSI1
KSI3
KSI0
KSO5
KSO4
KSO7
KSO6
KSO8
KSO3
KSO1
KSO2
KSO0
KSO12
KSO16
KSO15
KSO13
KSO14
KSO9
KSO11
KSO10
TP_V+
TP_X
TP_GND
TP_Y
TP_Z
JAE_FK2S030W11~D
<<37>> KSO16
<<37>> KSO[0..15]
<<37,40>> KSI[0..7]
KSO15
KSO14
KSO13
KSO12
KSO11
KSO10
KSO9
KSO8
KSO7
KSO6
KSO5
KSO4
KSO3
KSO2
KSO1
KSO0
KSI7
KSI6
KSI5
KSI4
KSI3
KSI2
KSI1
KSI0
CN7
CN12
CN11
CN10
CN9
CN8
@100P_1206_8P4C_50V8~D
C205
100P_0603_50V8J~D
@
<<37>> SIO_FA[0..19]
U61
SIO_FA0
SIO_FA1
SIO_FA2
SIO_FA3
SIO_FA4
SIO_FA5
SIO_FA6
SIO_FA7
SIO_FA8
SIO_FA9
SIO_FA10
SIO_FA11
SIO_FA12
SIO_FA13
SIO_FA14
SIO_FA15
SIO_FA16
SIO_FA17
SIO_FA18
SIO_FA19
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
VCC
VCC
VPP
D0
D1
D2
D3
D4
D5
D6
D7
RP#/RESET#
WP#/RY/BY#
NC
NC
CE#
OE#
WE#
GND
GND
SIO_FD0
SIO_FD1
SIO_FD2
SIO_FD3
SIO_FD4
SIO_FD5
SIO_FD6
SIO_FD7
SIO_FD[0..7]
<<37>>
FWH_RST
VCC1RST#
VCC1RST#
<<37>>
R289
0_0402_5%~D
C633
0.1U_0402_16V4Z~D
C634
0.1U_0402_16V4Z~D
<<37>> FCS#
<<37>> FRD#
<<37>> FWR#
FCS#
FRD#
FWR#
MX29LV008T/B_TSOP40~D
D
G
S
2N7002
C
B
E
DTC114
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DELL CONFIDENTIAL/PROPRIETARY
Title
INT KB
Size
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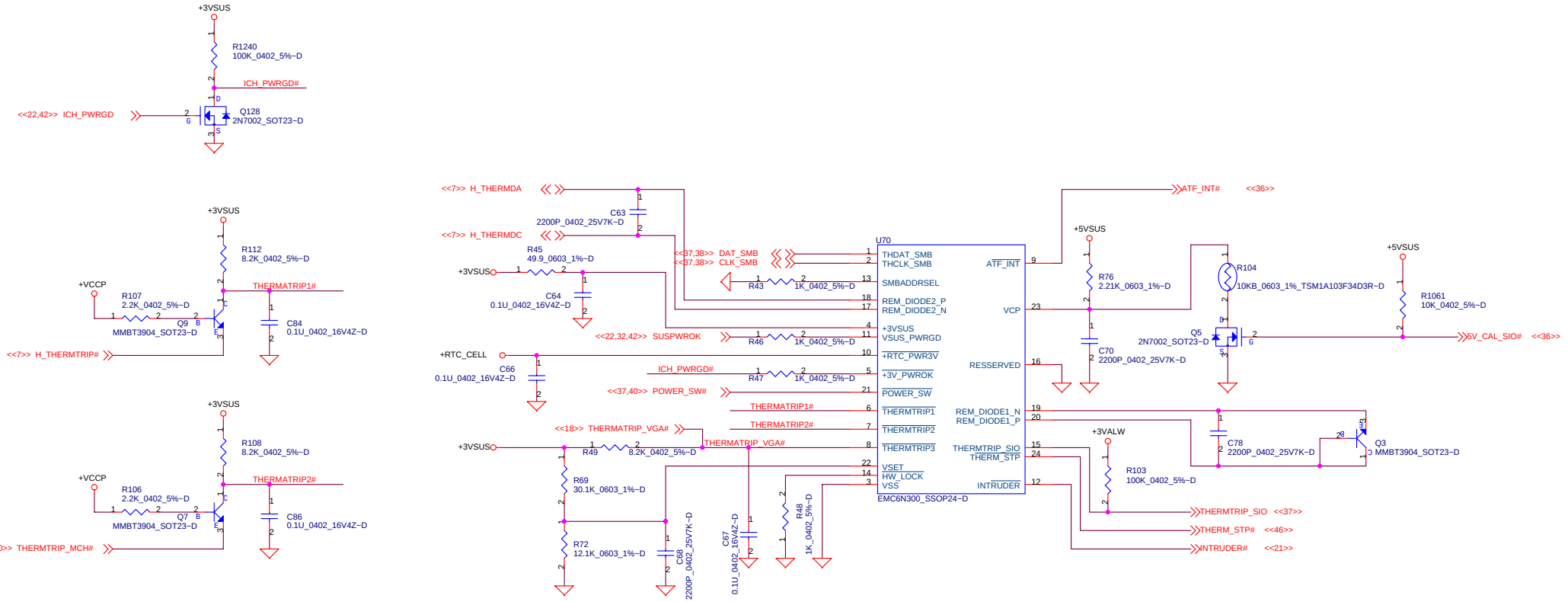
+3VSUS
R1240
100K_0402_5%~D
ICH_PWRGD#
<<22,42>> ICH_PWRGD
Q128
2N7002_SOT23~D
+3VSUS
R112
8.2K_0402_5%~D
+VCCP
R107
2.2K_0402_5%~D
THERMATRIP1#
Q9
MMBT3904_SOT23~D
C84
0.1U_0402_16V4Z~D
<<7>> H_THERMTRIP#
+3VSUS
R108
8.2K_0402_5%~D
+VCCP
R106
2.2K_0402_5%~D
THERMATRIP2#
Q7
MMBT3904_SOT23~D
C86
0.1U_0402_16V4Z~D
<<10>> THERMTRIP_MCH#
<<7>> H_THERMDA
C63
2200P_0402_25V7K~D
<<7>> H_THERMDC
R45
49.9_0603_1%~D
+3VSUS
C64
0.1U_0402_16V4Z~D
<<37,38>> DAT_SMB
<<37,38>> CLK_SMB
R43
1K_0402_5%~D
<<22,32,42>> SUSPWROK
R46
1K_0402_5%~D
+RTC_CELL
C66
0.1U_0402_16V4Z~D
ICH_PWRGD#
R47
1K_0402_5%~D
<<37,40>> POWER_SW#
THERMATRIP1#
THERMATRIP2#
<<18>> THERMATRIP_VGA#
THERMATRIP_VGA#
+3VSUS
R49
8.2K_0402_5%~D
R69
30.1K_0603_1%~D
R72
12.1K_0603_1%~D
C68
2200P_0402_25V7K~D
C67
0.1U_0402_16V4Z~D
R48
1K_0402_5%~D
U70
THDAT_SMB
THCLK_SMB
SMBADDRSEL
REM_DIODE2_P
REM_DIODE2_N
+3VSUS
VSUS_PWRGD
+RTC_PWR3V
+3V_PWROK
POWER_SW
THERMTRIP1
THERMTRIP2
THERMTRIP3
VSET
HW_LOCK
VSS
ATF_INT
VCP
RESSERVED
REM_DIODE1_N
REM_DIODE1_P
THERMTRIP_SIO
THERM_STP
INTRUDER
EMC6N300_SSOP24~D
ATF_INT# <<36>>
+5VSUS
R76
2.21K_0603_1%~D
C70
2200P_0402_25V7K~D
R104
10KB_0603_1%_TSM1A103F34D3R~D
Q5
2N7002_SOT23~D
+5VSUS
R1061
10K_0402_5%~D
5V_CAL_SIO# <<36>>
+3VALW
R103
100K_0402_5%~D
C78
2200P_0402_25V7K~D
Q3
MMBT3904_SOT23~D
THERMTRIP_SIO <<37>>
THERM_STP# <<46>>
INTRUDER# <<21>>
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PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.
DELL CONFIDENTIAL/PROPRIETARY
Title Thermtrip
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Document Number
Board Number LA2111
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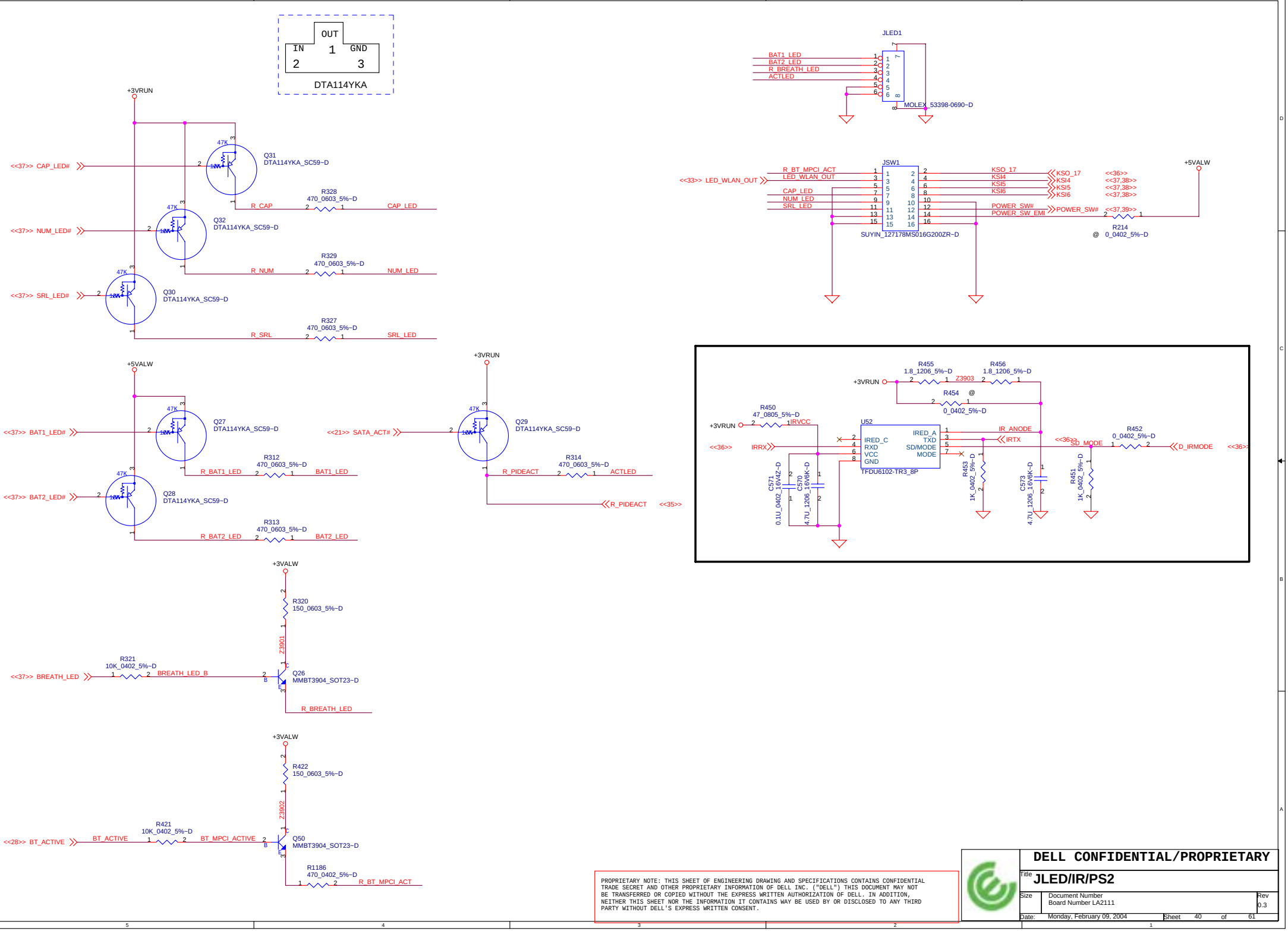

DELL CONFIDENTIAL/PROPRIETARY

Title: **JLED/IR/PS2**

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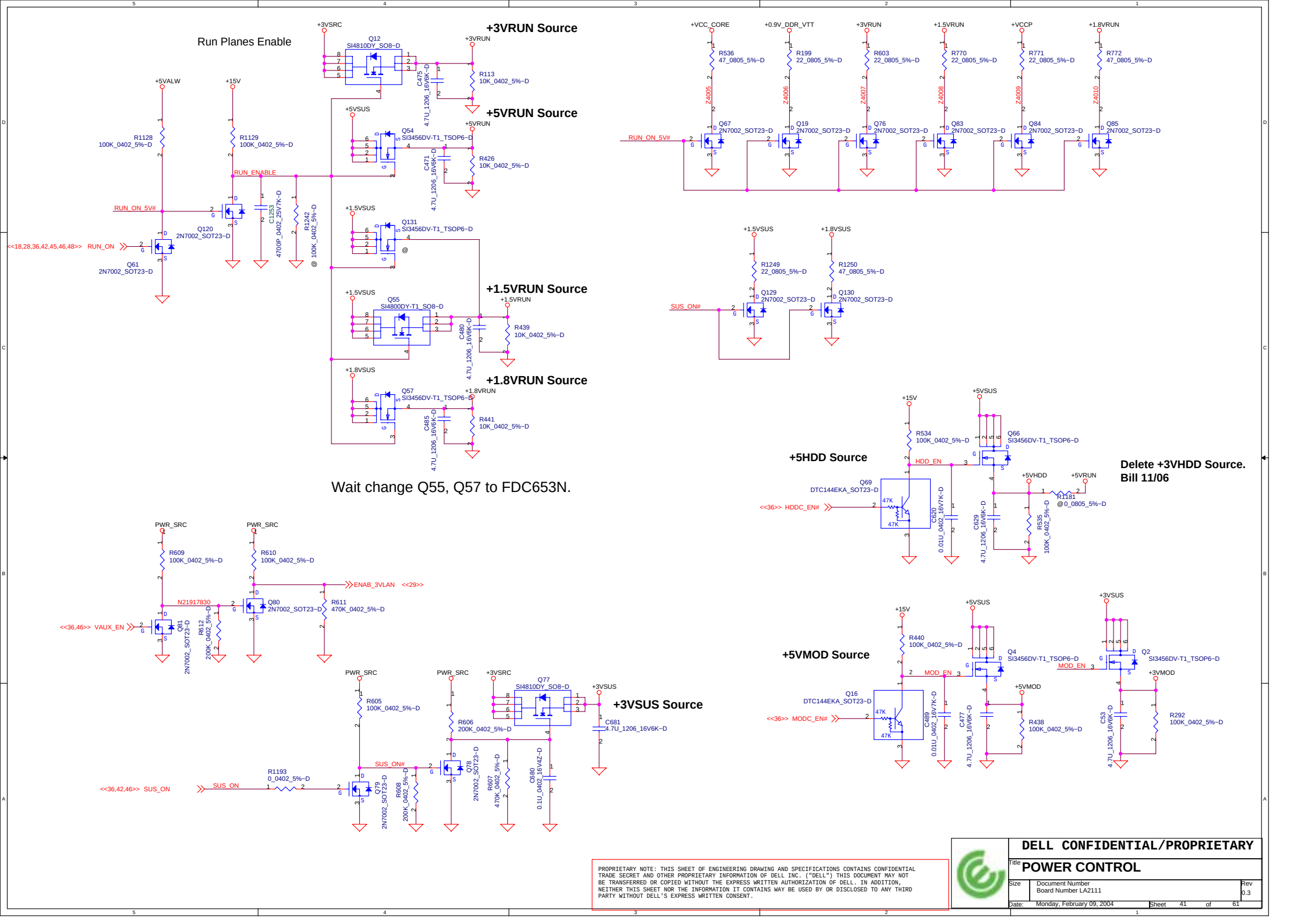
Run Planes Enable
+3VRUN Source
+5VRUN Source
+1.5VRUN Source
+1.8VRUN Source
Wait change Q55, Q57 to FDC653N.
+5HDD Source
Delete +3VHDD Source.
Bill 11/06
+5VMOD Source
+3VSUS Source
RUN_ON_5V#
RUN_ENABLE
SUS_ON#
HDD_EN
MOD_EN
ENAB_3VLAN
VAUX_EN
SUS_ON
HDDC_EN#
MODC_EN#
RUN_ON
+VCC_CORE
+0.9V_DDR_VTT
+3VRUN
+1.5VRUN
+VCCP
+1.8VRUN
+5VALW
+15V
+5VSUS
+1.5VSUS
+1.8VSUS
+5VHDD
+3VMOD
PWR_SRC
DELL CONFIDENTIAL/PROPRIETARY
POWER CONTROL
PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS WAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.
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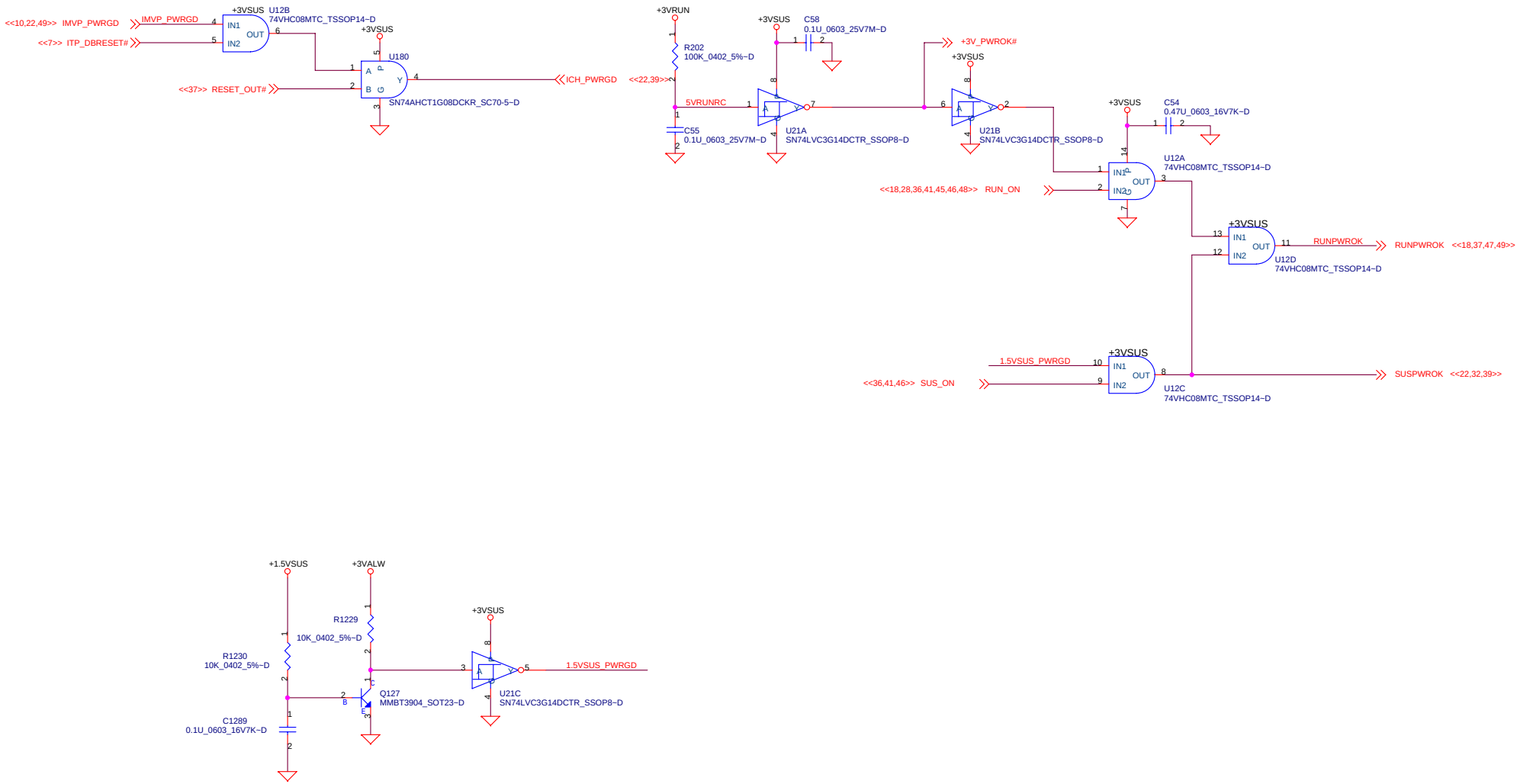

DELL CONFIDENTIAL/PROPRIETARY

Title: **Power Sequence**

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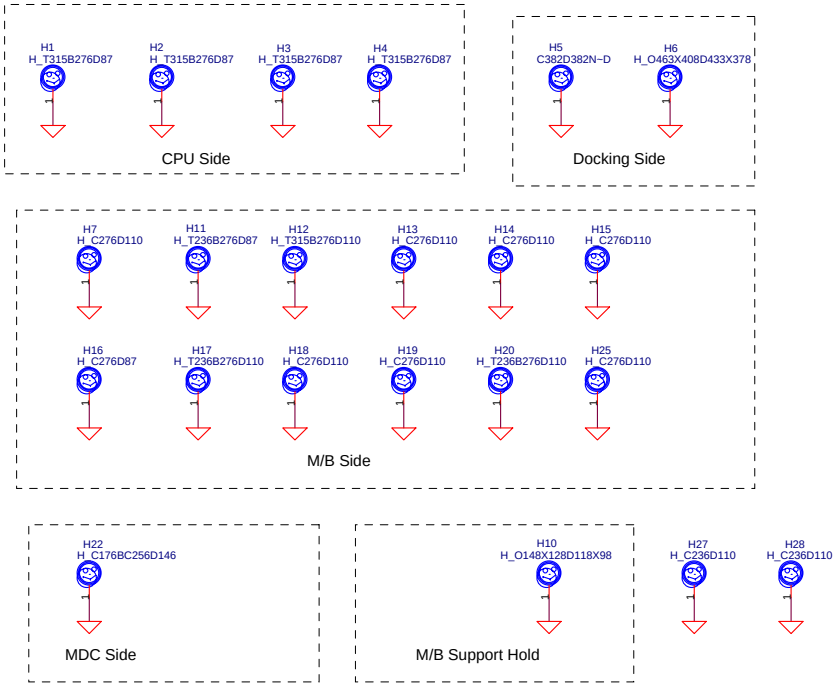
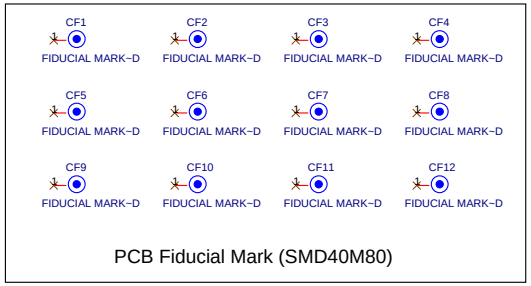
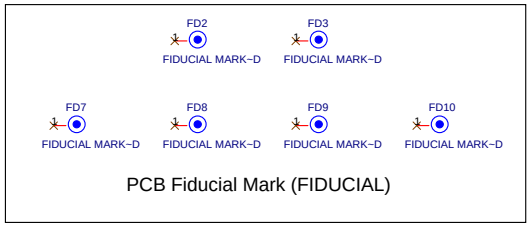
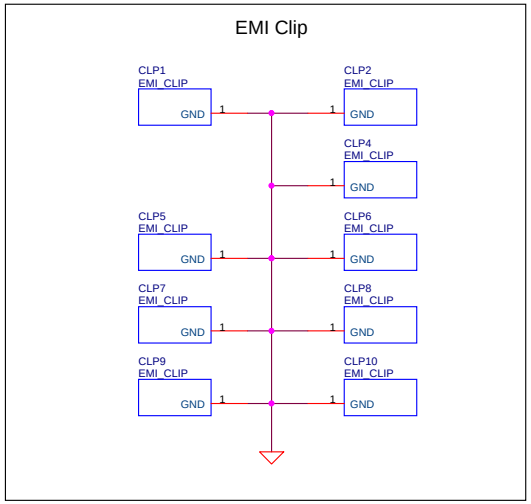


Fiducial Mark







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Title: **PAD and Standoff**

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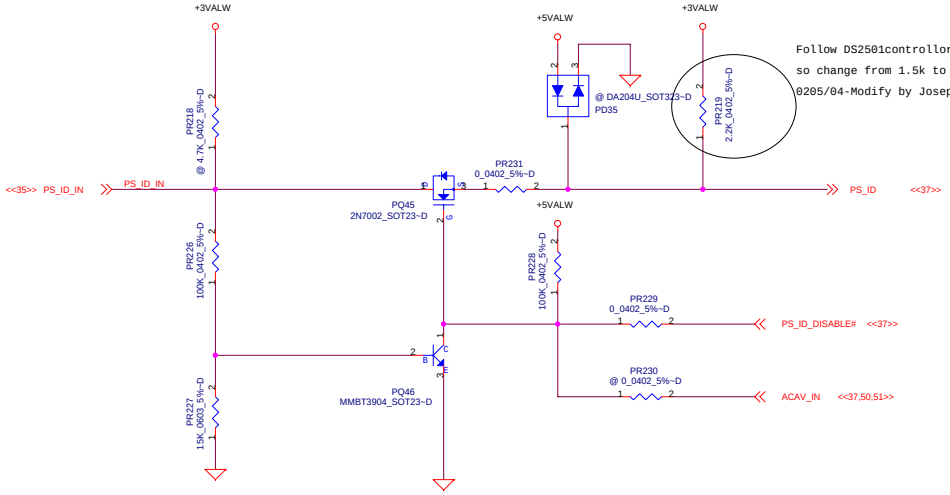
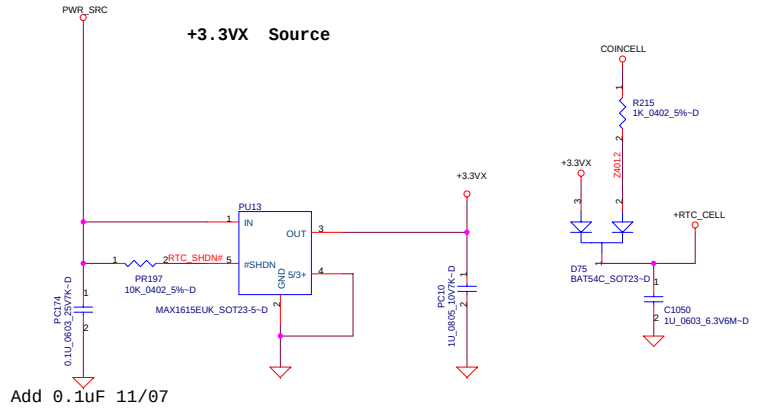
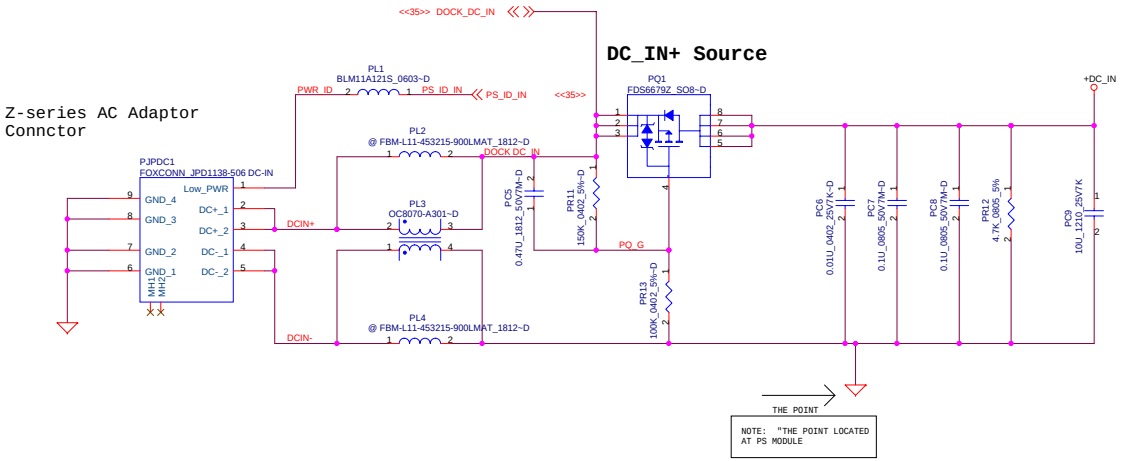




Add 0.1uF 11/07



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Title	+DCIN	
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Secondary Battery Connector

ESD Diodes

+3VALW

PD1 @ DA204U_SOT323-D
PD2 @ DA204U_SOT323-D
PD3 @ DA204U_SOT323-D
PD4 @ DA204U_SOT323-D

PJP1
BATT1+
BATT2+
SMB_CLK
SMB_DAT
BATT_PRES#
SYSPRES#
BATT_VOLT
GND BATT1-
GND BATT2-
SUYIN_200025MR009G500NL-D

PC2 220P_0402_50V7K-D

Z4301
Z4302
Z4303

PR2 100_0402_5%-D
PR3 100_0402_5%-D
PR4 100_0402_5%-D
PR5 100_0402_5%-D

SBAT_SMBCLK <<18,37>>
SBAT_SMBDAT <<18,37>>
SBAT_ALARM# <<37>>

PC1 0.1U_0805_50V7M-D
PL21 FBM-L11-453215-900LMAT_1812-D
SBATT+

+3VALW
PR1 10K_0402_5%-D
SBAT_PRES# <<37,51>>

Update PJP1 symbol -01/29/2004

Primary Battery Connector

ESD Diodes

+3VALW

PD5 @ DA204U_SOT323-D
PD6 @ DA204U_SOT323-D
PD7 @ DA204U_SOT323-D
PD8 @ DA204U_SOT323-D

PJP2
BATT1+
BATT2+
SMB_CLK
SMB_DAT
BATT_PRES#
SYSPRES#
BATT_VOLT
GND BATT1-
GND BATT2-
SUYIN_200275MR009G516ZL-D

PC4 220P_0402_50V7K-D

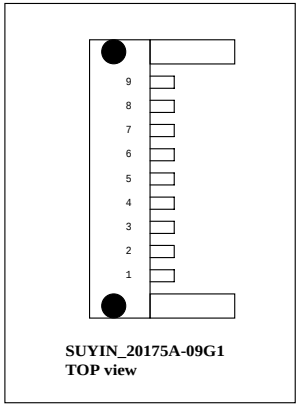
Z4304
Z4305
Z4306

PR7 100_0402_5%-D
PR8 100_0402_5%-D
PR9 100_0402_5%-D
PR10 100_0402_5%-D

PBAT_SMBCLK <<37,50>>
PBAT_SMBDAT <<37,50>>
PBAT_ALARM# <<37>>

PC3 0.1U_0805_50V7M-D
PL22 FBM-L11-453215-900LMAT_1812-D
PBATT+

+3VALW
PR6 10K_0402_5%-D
PBAT_PRES# <<37>>



SUYIN_20175A-09G1
TOP view

+2.5VRUN

R1=R2* (Vo/ 0.8 -1), R2:25K~100K.

+3VSUS

PU2
IN IN POK SHDN# OUT OUT SET GND1 GND2
MAX1806EUA25_8UMAX-D

+2.5VRUNP

PC32 0.1U_0805_25V7K-D
PC33 1U_0805_10V7K-D
PR38 10K_0402_5%-D
PR37 66.5K_0402_1%
PC34 10U_1206_6.3V7K-D
PC35 0.1U_0805_25V7K-D
PR39 30.9K_0402_1%-D

2P5V_PWRGD

<<18,28,36,41,42,46,48>> RUN_ON
PR233 27K_0402_5%-D
RUN_ON_2.5
PC176 0.1U_0603_25V7K-D

+2.5VRUNP
PJP5
PAD-OPEN 4x4m
+2.5VRUN

Add Delay schematic, the value wait change.
12/16 Change to PWR materials

Change PR233 to achieve proper 1ms powerup delay.
Modify PR233 from 10 k to 27k by Joseph. -02/05

DELL CONFIDENTIAL/PROPRIETARY

Title: **Battery Conn./+2.5V**

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DC/DC +3V/ +5V/ +15V

Modify by Joseph 01/28/04

Reserve Jump for EMI test

Place these CAPs close to FETs

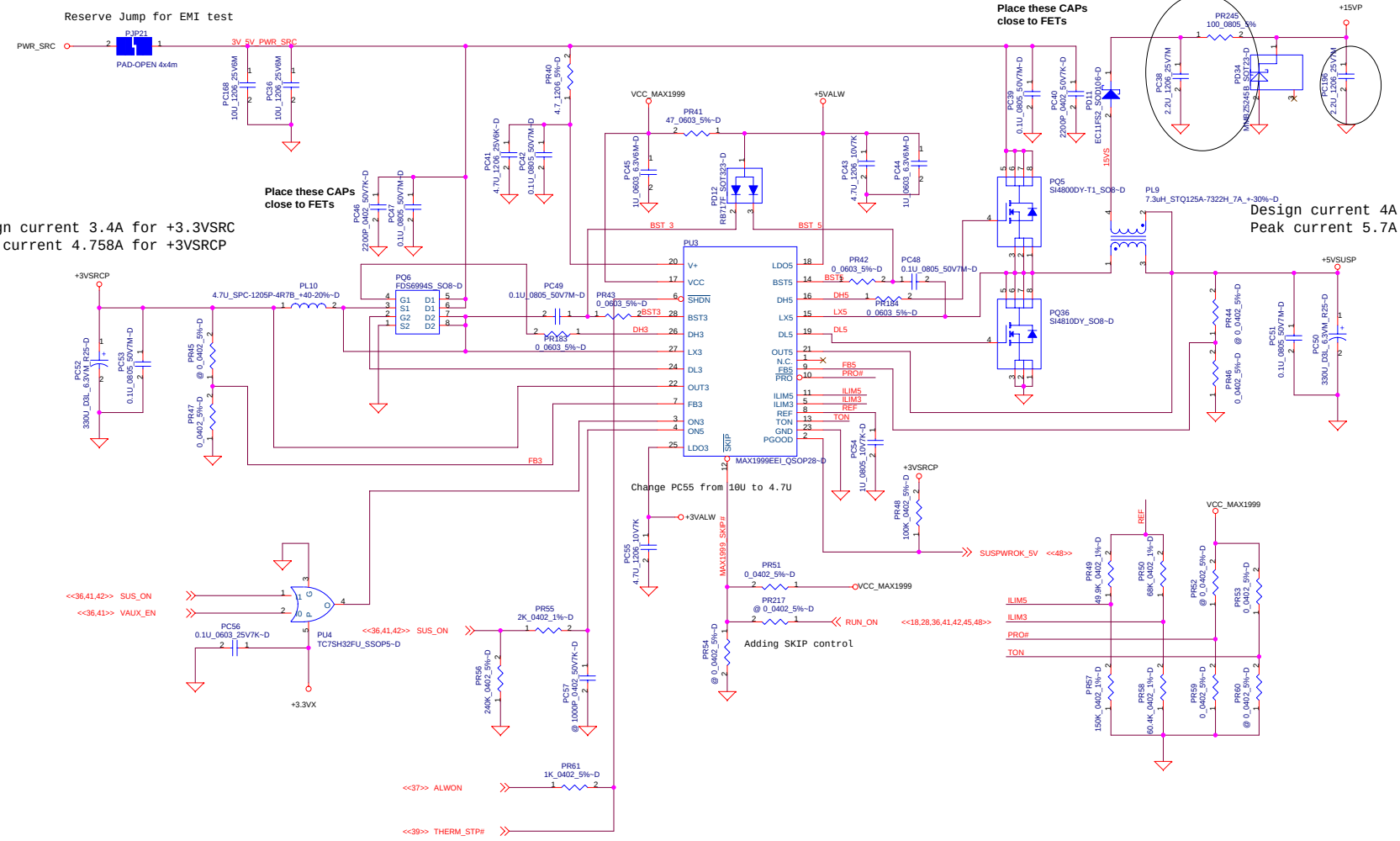
Place these CAPs close to FETs

Design current 3.4A for +3.3VSRC
Peak current 4.758A for +3VSRCP

Design current 4A for +5VSUS
Peak current 5.7A for +5VSUSP

Change PC55 from 10U to 4.7U

Adding SKIP control



+15VP — PJP6 — PAD-OPEN 2x2m~D — +15V (150mA,Via NO.= 2)

+5VSUSP — PJP7 — PAD-OPEN 4x4m — +5VSUS (6A,240mils ,Via NO.= 12)

+3VSRCP — PJP8 — PAD-OPEN 4x4m — +3VSRC (4A,160mils ,Via NO.= 8)

+3VSRCP:
OCP: (((Ilim3 / 10) /Low-side MOSFET Rdson) +0.5* IL)*(+-1.07)
Ilimit3=REF(60.4K/60.4K+68K)=0.94V
Low side MOSFET Rdson:22.75m ohms at 100C
iL=((Vin-Vo) / L)*Ton=((19.5-3.3) / 4.7u)* ((1/300K) * 3.3/19.5))=1.944 A
OCP TYP: 5.1A

+5VSUSP
OCP: (((Ilim5 / 10) /Low-side MOSFET Rdson) +0.5* IL)*(+-1.07)
Ilimit5=REF(150K/150K+49.9K)=1.5V
Low side MOSFET Rdson: SI4810DY =25m ohms at 100C
iL=((Vin-Vo) / L)*Ton=((19.5-5) / 7.3u)* ((1/200K) * 5/19.5))=2.546 A
OCP TYP: 7.273A

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Title: +3.3V/+5V/+15V

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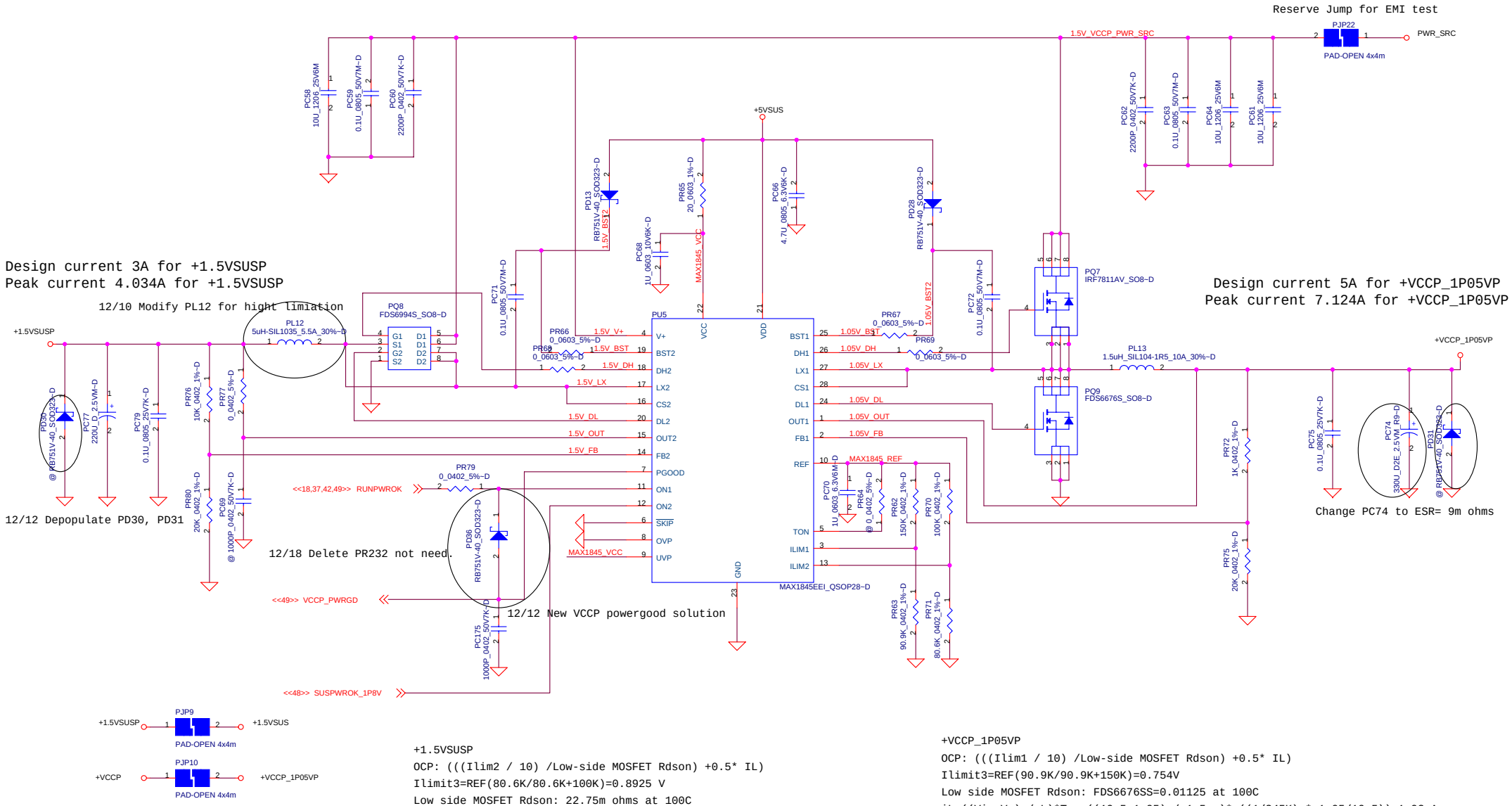
+1.5VSUSP / +VCCP_1P05VP



+1.5VSUSP
OCP: (((Ilim2 / 10) /Low-side MOSFET Rdson) +0.5* IL)
Ilimit3=REF(80.6K/80.6K+100K)=0.8925 V
Low side MOSFET Rdson: 22.75m ohms at 100C
iL=((Vin-Vo) / L)*Ton=((19.5-1.5) / 5u)* ((1/255K) * 1.5/19.5))=1.23 A
OCP TYP: 4.462A

+VCCP_1P05VP
OCP: (((Ilim1 / 10) /Low-side MOSFET Rdson) +0.5* IL)
Ilimit3=REF(90.9K/90.9K+150K)=0.754V
Low side MOSFET Rdson: FDS6676SS=0.01125 at 100C
iL=((Vin-Vo) / L)*Ton=((19.5-1.05) / 1.5u)* ((1/345K) * 1.05/19.5))=1.92 A
OCP TYP: 7.66 A

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Title: +1.5VSUSP /+VCCP_1P05VP

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+1.8VSUSP/ +0.9V_DDR_VTT

DDR2 Termination

Reserve Jump for EMI test

PWR_SRC — PJP26 PAD-OPEN 4x4m — 1.8V_0.9V_PWR_SRC

PC177 10U_1206_25V6M
PC178 10U_1206_25V6M
PC179 0.1U_0805_25V7K~D
PC180 2200P_0603_50V7K~D

0202/04-Modify by Joseph

Update design current to 10.6A -0128/04

Design current 10.6A for +1.8V_SUSP

+5VSUS
+3VSUS
+1.8VSUSP
+1.5VSUS
+0.9V_DDR_VTTP

PD38 RB751V-40_SOD323~D
PC181 4.7U_0805_6.3V6K~D
PR235 10_0603_5%~D
PC182 1U_0603_6.3V6M~D
PR236 100K_0402_5%~D
PR237 100K_0402_5%~D
PR239 100K_0402_5%~D
PQ49 2N7002_SOT23~D
RUN_ON <<18,28,36,41,42,45,46>>

PQ47 IRF7821_SO8~D
PC183 0.1U_0805_50V7M~D
PR238 0_0603_5%~D
1.8V_0.9V_PWR_SRC
SUSPWROK_1P8V <<47>>
+0.9V_PWRGD
SUSPWROK_5V <<46>>

PU14 MAX8550ETI_TQFN28~D
VDD OVP/UVP SHDNB AVDD
BST DH LX DL PGND1 VOUT FB TON REF
VIN POK1 POK2 SHDNA STBY VTTI REFIN PGND2 VTT VTTS VTTR
ILIM SKIP GND SS

1.8V_DH
1.8V_LX
1.8V_DL
1.8V_FB
1.8V_REF

PL24 1.4UH_CEP125-1R4_15.5A_20%~D

PC185 330U_D2E_2.5VM~D
PC186 330U_D2E_2.5VM~D
PC188 0.1U_0805_25V7K~D

0130/2004-Modify by Joseph.

PR240 27.4K_0603_1%~D
PR243 17.4K_0402_1%~D
PR247 4.7_1206_5%~D
PQ48 FDS7788_SO8~D
PC197 1000P_0603_50V7K~D @ 4.7_1206_5%~D
PR241 @ 0_0402_5%~D
PR242 100K_0402_1%~D
PC193 0.22U_0603_10V7M~D
PR244 48.7K_0402_1%~D
PC194 1000P_0402_50V7K~D
PC195 1U_0603_6.3V6M~D

PR246 20_1206_5%
PC187 0.1U_0603_25V7K~D
PC184 10U_1206_6.3V7K~D

PJP31 PAD-OPEN 2x2m~D
PJP32 PAD-OPEN 2x2m~D

0202/04-Modify by Joseph
Install jumper on PJP32 pad and depop PJP31
0207/2004

PC189 0.1U_0805_25V7K~D
PC190 22U_1206_6.3VAM~D
PC191 22U_1206_6.3VAM~D
PC192 22U_1206_6.3VAM~D
PC198 @ 22U_1206_6.3VAM~D

Change from 22uF to 10uF for cost down.
0202/04-Modify by Joseph
0205/04- Reserve PC198. Modify by Joseph

V_DDR_MCH_REF <<10,16,17>>

Install jumper on PJP30 pad.

PJP30 PAD-OPEN 2x2m~D — AGND — GND

0128/04-Modify by Joseph for updated OCP.
0202/04-Modify by Joseph

PJP27 PAD-OPEN 4x4m
PJP28 PAD-OPEN 4x4m
+1.8VSUSP — +1.8VSUS **(10A,320mils ,Via NO.=20)**

PJP29 PAD-OPEN 4x4m
+0.9V_DDR_VTTP — +0.9V_DDR_VTT **(2A,200mils ,Via NO.=4)**

+1.8VSUSP
OCP: (((Ilim / 10) /Low-side MOSFET Rdson) +0.5* IL)
Ilimit=REF(53.6K/53.6K+100K)=0.6979 V
Low side MOSFET Rdson:6.5m ohms at 100C
iL=((Vin-Vo) / L)*Ton=((19.5-1.8) / 1.4u)* ((1/450K) * 1.8/19.5))=2.59A
OCP TYP: 11.37A

V I D						Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V
0	1	1	1	1	0	1.484
0	1	1	0	0	1	1.308
1	0	1	1	1	1	0.956
1	1	1	1	0	0	0.748

Reserve Jump for EMI test

PWR_SRC — PJP24 PAD-OPEN 4x4m — CPU_PWR_SRC

PJP25 PAD-OPEN 4x4m

Reserve PC170 PC171 PC172 PC173 for audio noise issue

DCR=1.1 m ohms

Output Capatitors 330uF_9m ohms place H/W, spec ESR=3m ohms

Remote Vcore sense

Change from 47p to 270p -1212

Change PR123 from 2.47K to 1.24K

Deeper Mode (C3) offset -1.2%

PSI need pull high

PBOOT voltage seeting up on 1.212V

The C4 Mode voltage is 0.748V, S2 open

Change PR125:30.1k. Delete PR129/PQ21/PQ40/PQ20/PQ41/PR124/PR205/PR203 and PR201 for BANIAS and DOTHAN

PR129/PQ21/PQ40/PQ20/PQ41/PR124/PR205/PR203 and PR201 are only for YONAH CPU.

TRANSITION TIMING:

(a): START-UP and SHUTDOWN(SUS=LOW,RUNPWROK=LOW):2mV/us

(b): ENTER SUSPEND (SUS=HIGH,RUNPWROK=HIGH): 8.6mV/us

(c): EXIT SUSPEND (SUS=LOW, RUNPWROK=HIGH): 24.7mV/us

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Title: +VCORE

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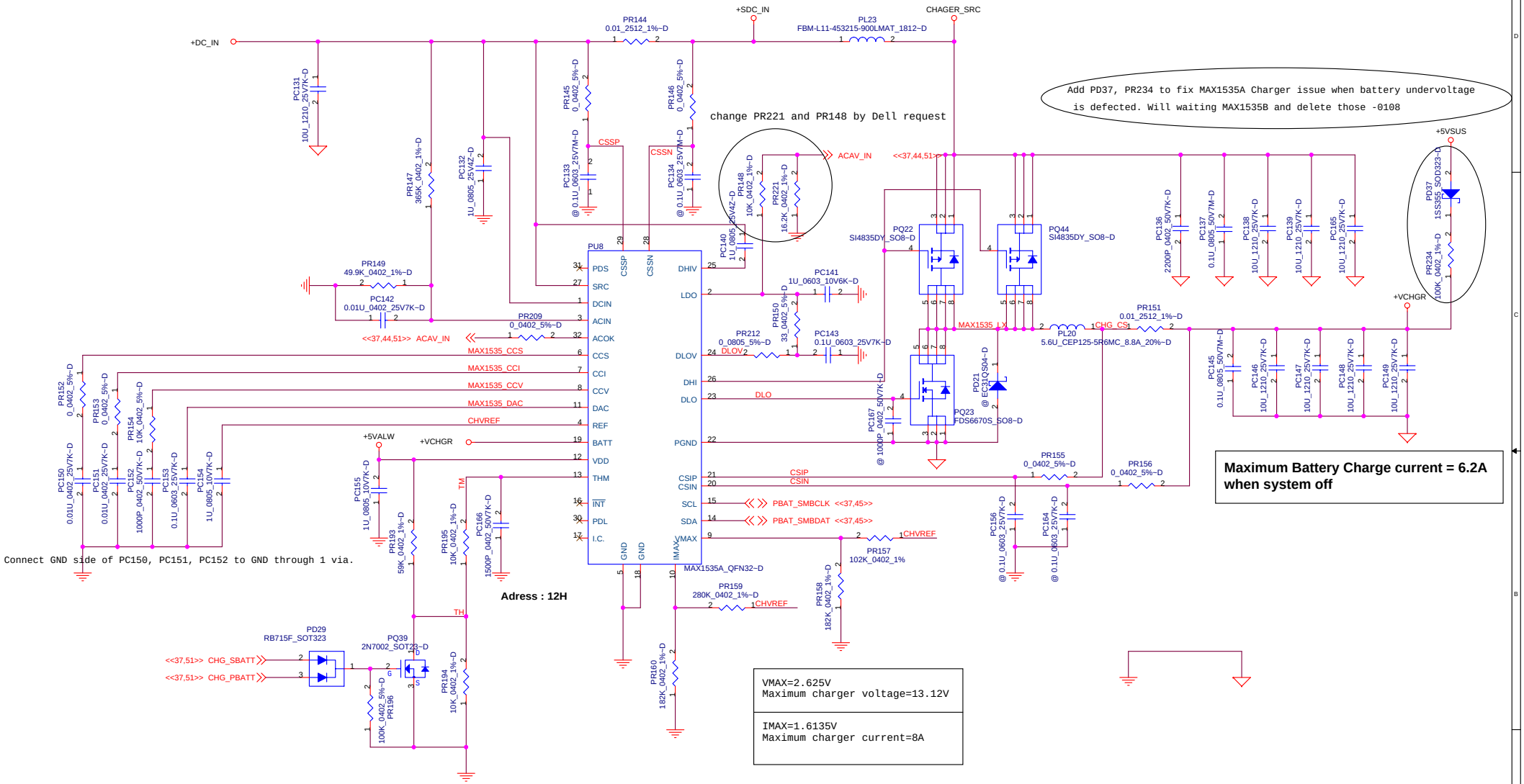

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Title: **Charger**

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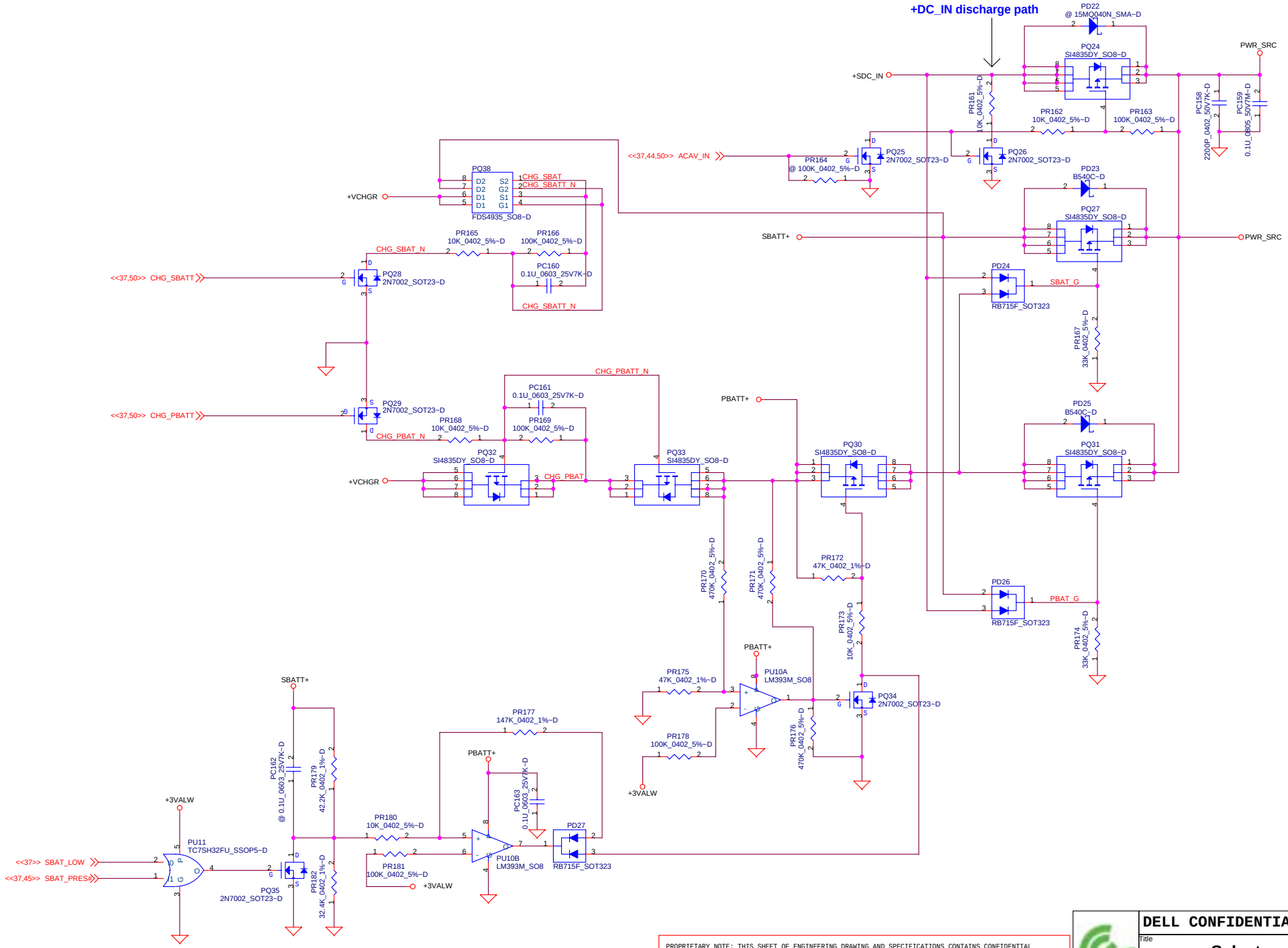

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Title: **Selector**

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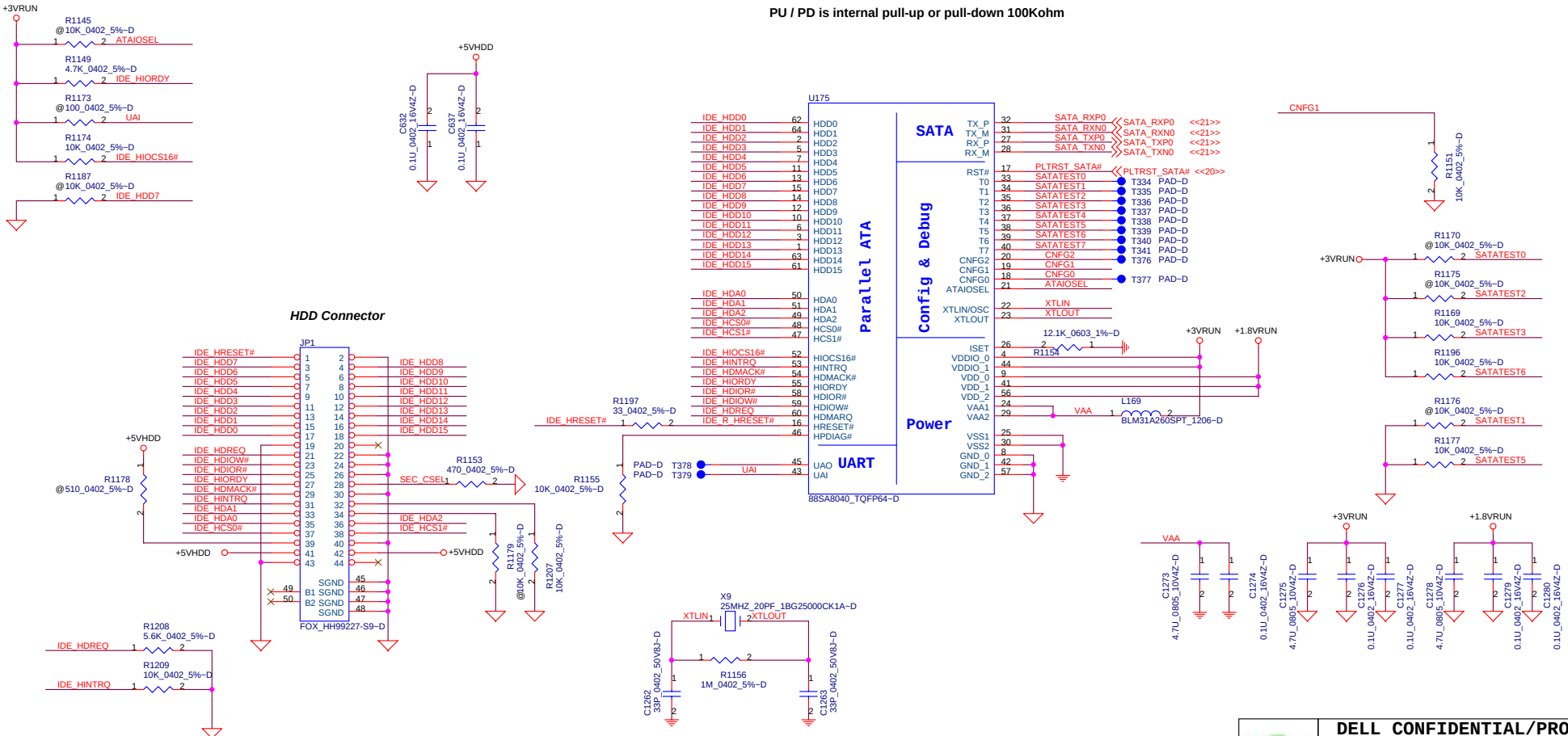
SATATEST3	SATATEST4	
0	0	20MHz
* 0	1	25MHz
1	0	30MHz
1	1	40MHz

Pin Name	Pin No.	Int. PU/PD	Settings
SATATEST0	33	PD	NC
SATATEST1	34	PU	NC
SATATEST2	35	PD	NC
SATATEST3	36	PD	1
SATATEST4	37	PD	NC
SATATEST5	38	PU	0
SATATEST6	39	PD	NC
SATATEST7	40	PD	NC
CFG0	20	PD	NC
CFG1	19	PU	0
CFG2	18	PD	NC

PU / PD is internal pull-up or pull-down 100Kohm

Sets maximum transfer rate and UDMA mode

	CNFG2	CNFG1	CNFG0	NOTE
*	0	0	0	Device Mode 100MB/s
	0	0	1	Device Mode 133MB/s
	0	1	0	Device Mode 150MB/s
	1	0	0	Host Mode 100MB/s
	1	0	1	Host Mode 133MB/s
	1	1	0	Host Mode 150MB/s
	0	1	1	Reserved
	1	1	1	Reserved



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Title: SATA Bridge

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	13	H/W	12/10	Bill	Power drop issue.	L43, L146 and L147 material change from BLM11A601S to BLM21PG600SN1D(3000mA).	0.2
2	20	H/W	12/10	Bill	VGA and LOM PLTRST# delay.	U25 Pin1 & Pin2 net name change to "PLTRST_DELAY#"	0.2
3	22	H/W	12/10	Bill	VGA and LOM PLTRST# delay.	U59 Pin AD21 add net name "PLTRST_DELAY#"	0.2
4	29	H/W	12/10	Bill	LOM isolation LRESET and PERST.	U164 Pin.M9 change net name to "PLTRST#".	0.2
5	32	M/E	12/11	Bill	Cardbus connector change.	Cardbus connector change to FOXCONN QT600806-7121.	0.2
6	39	H/W	12/11	CS	Populate Q9	Needed for full guardian.	0.2
7	10,22,42	H/W	12/11	CS	Delete R22 and connect IMVP_PWRGD directly to MCH and ICH	Resistor not needed.	0.2
8	42	H/W	12/11	CS	Delete R1228	Not used.	0.2
9	42	H/W	12/11	CS	Change U12 pin 10 to 1.5VSUS_PWRGD. Eliminate the need for U42D.	Simplifying the SUSPWROK logic, and this gate can be removed.	0.2
10	42	H/W	12/11	CS	Delete R753, C922, U67, R21, and C921	Not used.	0.2
11	42	H/W	12/11	CS	Change R1229 voltage to +3VALW	This will eliminate the glitch at the output of 1.5VSUS_PWRGD (U21 pin 5).	0.2
12	42	H/W	12/11	CS	Delete R1190, C1281, R1188, Q124, R1189, Q123, and R1195.	We are now using SUSPWROK_1P8V signal to enable the 1.5V rail.	0.2
13	9	H/W	12/11	CS	Remove C944 capacitor at +VCC_CORE.	Delete C944	0.2
14	33	H/W	12/11	CS	Add a No-Pop 0-ohm resistor connecting pin 3 of Q114 to Pin 3 of Q115. This is for future testing of the SMBUS to the LOM without the isolation. There is a push on the Dell side to remove this Isolation.	Add R1231	0.2
15	33	H/W	12/11	CS	Add a No-Pop 0-ohm resistor connecting pin 3 of Q116 to Pin 3 of Q117. This is for future testing of the SMBUS to the LOM without the isolation. There is a push on the Dell side to remove this Isolation.	Add R1232	0.2
16	13	H/W	12/11	GF	No stuff C287 and C1265. Change C1264 to 10uf	Modify OK.	0.2
17	21	H/W	12/11	GF	Can we delete some 0-ohm ser. Resistors on CPU interface?	Modify OK.	0.2
18	19	H/W	12/11	CS	Add a NO POP 0-Ohm resistor between pin 1 and pin 8 of L57 for a ground connection when L57 is removed.	Add R1233	0.2
19	38	M/E	12/12	Bill	Change JPLAM cconnector.	Change Pin define and connector library.	0.2
20	40	M/E	12/12	Bill	Change JLED1 and JSW1 cconnector.	Change Pin define and connector library.	0.2

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
21	19	H/W	12/12	Bill	Remove Q125, Q126, U176, U177, R1222 and R1223 for Docking connector shift-up 1mm.	Layout space issue, delete that component and add R1234, R1235, R1236 and R1237 for isolation int. GFX.	0.2
22	42	H/W	12/12	Bill	Delete R1132, R1131, R1130, Q122, Q121, C1254, and U174 and use VCCP_PWRGD generated by MAX1845.	Using new MAX1845 solution with Diode between PGOOD and ON1 for VCCP Powergood.	0.2
23	36	H/W	12/12	CS	Add a No Pop 100K-ohm pulldown resistor to VAUX_EN signal for potential SMSC floating pins on power down. Nimitz team reccomended this pulldown for safety.	Add R1238	0.2
24	36	H/W	12/12	CS	Add a o-ohm resistor in parallel with R228 connected to +3.3VX.	Add R1239	0.2
25	36	H/W	12/12	CS	No Pop R228. Change Macallan VCC0 voltage from +RTC_CELL to +3.3VX per D'05 reccomendation.. CMOS settings are now stored in ICH6, thus the RTC rail doesn't need to power this signal.	No pop R228	0.2
26	37	H/W	12/12	CS	Change R1082 pullup voltage to +3.3VX	Modify it.	0.2
27	40	M/E	12/15	Bill	M/E request change JLED1 connector.	Connector change to MOLEX_53398-0690.	0.2
28	30	H/W	12/15	PN	R971-978 should be 0603 package.	Change from 0402 package to 0603 package.	0.2
29	7	H/W	12/15	CS	Change R1160 to 54.9 ohms per Intel.	Change from 220 Ohm to 54.9 Ohm.	0.2
30	7	H/W	12/15	CS / GF	Change R17 to 200 ohms per Intel.	Change from 330 Ohm to 220 Ohm.	0.2
31	19	H/W	12/16	GF	Move D4, D5, D6 back to +3vrun	Modify done	0.2
32	39	H/W	12/17	CS	Invert ICH_PWRGD signal with a 7002 FET and a 100K pullup to +3VSUS. Name the signal ICH_PWRGD# and connect it to pin 1 of R47.	Modify done	0.2
33	43	M/E	12/17	Bill	Add 2 screw on HDD side	Add H27, H28	0.2
34	33	H/W	12/17	CS	No Pop Q114 and Q116.	Following Azeda and using only one level of isolation for SMBUS.	0.2
35	28	M/E	12/17	Bill	Change BT connector.	Change Pin define, to be change to 9 pin connector.	0.2
36	41	H/W	12/18	Bill	RUN_ENABLE singal reserve voltage issue.	Add R1242 no pop.	0.2
37	28	H/W	12/18	Bill	Swap JBT pin define.	For layout route easy, change pin define.	0.2
38	20	H/W	12/18	CS	U164 pin M9 PLTRST# signal should be bufferred here for sufficient signal drive strength.	Add U179, R1243	0.2
39	20	H/W	12/18	CS	Regulatory team has reported damage to FETs in the Dock area, want to ensure proper rating of near 3KV.	Q43 change to DTC144EKA_SOT23	0.2

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40	38	H/W	12/18	Bill	Remove BIOS debug connector.	For layout space issue, delete it.	0.2
41	39	H/W	12/19	Bill	Delete R1241 and signal "+3V_PWROK#" same as Tobago, Sullivan, Azeda	Modify Done	0.2
42	37	H/W	12/21	CS	No Pop R1202 and R1203, Populate R1198, R1199, R1200, and R1201	Modify Done	0.2
43	37	H/W	12/21	Bill	Change Board ID	R286 no stuff, R287 stuff.	0.2
44	38	M/E	12/21	Bill	Change JPLAM connector to Molex_53398-1290.	For M/E request, change it.	0.2
45	31	M/E	12/21	Bill	Change JP5 connector to Molex_53398-0990.	For M/E request, change Samrt-Card connector.	0.2
46	29	H/W	12/24	PN	Dell LOM team requests to make notation 0.5W capacity on R1051	Change to 1210 Size	0.2
47	37	H/W	12/24	CS	U27 GPIO20 is actually an open drain signal, so CHG_SBATT should be pulled high.	Add Pop resister R1244, non-pop R759.	0.2
48	13	H/W	12/24	Bill	Add +VCCP_CRT and +1.5VRUN_TV.	For layout easy control.	0.2
49	26	H/W	12/24	Bill	Change Audio jack location.	Audio jack from JP8 change to JAUDO, JAUDIOD change to JMIC	0.2
50	19	H/W	12/24	Bill	JVGA connector footprint error.	Footprint change, change pin 16, 17 to NC, Pin 17, 18 to GND.	0.2
51	43	M/E	12/24	Bill	Add screw H24	For M/E request add H24.	0.2
52	27	H/W	12/24	Bill	Change USBP7 pair for layout issue.	Exchange USBP7+/USBP7- and USBP7_D+/USBP7_D-.	0.2
53	52	M/E	12/24	Bill	Change HDD connector.	Change HDD same Nimiz.	0.2
54	29/22	H/W	12/24	Bill	Change net name for PCIE pair.	Add net name singal easy control for PCIE.	0.2
55	35	H/W	12/25	Bill	R616 add @.	Same as LBK.	0.2
56	6/10/12 13/19	H/W	12/29	Bill	Int. GFX disable.	No stuff R1071, R1072R1133, R1134, R1135, R1136, R1137, R1138, R1139, R1140, R1141, R1142, R1210, L8, C201, C207, C245, R1234, R1235, R1236, R1237. Stuff R1211, R1212, R1213, R1214.	0.2
57	13	H/W	12/29	Bill	Change Inductor	Change L6, L9, L29, L7 from BLM11A601S to BLM18PG181SN1.	0.2
58	13	H/W	01/02	GF	Change Inductor	Change L43, L146, L147 from BLM21PG600SN1D to BLM18PG181SN1.	0.3
59	37	H/W	01/02	Bill	Change Board ID	R279, R286 no stuff, R278, R287 stuff.	0.3
60	43	EMI	01/02	Bill	Add EMI Clip	Add EMI Clip 7 pcs.	0.3
61	13	H/W	01/02	Bill	Change R1212 pin 2 to GND.	Follow Intel check list, change VCC_SYNC to GND for int. GFX disable.	0.3
62	37	H/W	01/05	PN	Change R1121 pu-high to +3VRUN	Modify.	0.3
63	10	H/W	01/06	GF	Remove R1213 and connect DREFCLK directly to +1.5vrun	Modify.	0.3

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64	10	H/W	01/06	GF	Remove R1214 and connect DREFCLK# directly to GND	Modify.	0.3
65	6	H/W	01/06	GF	Remove R178 and connect DREF_SSCLKP directly to +1.5vrun	Modify.	0.3
66	12	H/W	01/06	GF	Remove R1071, R1072, R1118, R1119	Modify.	0.3
67	12	H/W	01/06	GF	Remove R1133, R1134, R1135	Modify.	0.3
68	12	H/W	01/06	GF	Remove R1064, R1065, R1066. Connect TV_YR, TV_CVBS_R, TV_C_R directly to ground	Modify.	0.3
69	12	H/W	01/06	GF	Remove R1062.Connect pin J18 directly to gnd.	Modify.	0.3
70	12	H/W	01/06	GF	Remove R1136-R1140.	Modify.	0.3
71	12	H/W	01/06	GF	Connect Alviso pins blue/blue#, red/red#, green/green# directly to +vccp	Modify.	0.3
72	12	H/W	01/06	GF	Remove R1063, connect directly to +vccp.	Modify.	0.3
73	12	H/W	01/06	GF	Remove R1141, R1142. Connect these pins directly to gnd.	Modify.	0.3
74	12	H/W	01/06	GF	Remove R1067, R1068, R1069	Modify.	0.3
75	13	H/W	01/06	GF	Remove L164-L168, C1229-C1240.	Modify.	0.3
76	13	H/W	01/06	GF	Connect Alviso pins F17, E17, D18,C18, F18, E18, H18, D19, H17 directly to gnd. (VCCA_TVDAC A,B,C and VCCA_TVBG)	Modify.	0.3
77	13	H/W	01/06	GF	Remove R1210. Connect directly to gnd.	Modify.	0.3
78	13	H/W	01/06	GF	Remove L8, C201, C207, C245. Connect pins E19 and F19 directly to +VCCP	Modify.	0.3
79	13	H/W	01/06	GF	Remove R1192, R1191, D80, D79	Modify.	0.3
80	42	H/W	01/06	CS	Delete R24	Modify.	0.3
81	42	H/W	01/06	CS	Delete All 4 instances of U42	Modify.	0.3
82	42	H/W	01/06	CS	Add a single 5-pin AND gate to replace U42A.(Or an unused AND gate if nearby) Connect RESET_OUT# to the second input pin.	Modify.	0.3
83	42	H/W	01/06	CS	Delete R23	Modify.	0.3
84	42	H/W	01/06	CS	Delete R1225 and R1227	Modify.	0.3
85	42	H/W	01/06	CS	Connect RUN_ON to pin 2 of U12.	Modify.	0.3

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86	41	H/W	01/06	CS	Delete R1194	Modify.	0.3
87	27	H/W	01/06	CS	Populate 0-Ohm Resistors or USB filters instead of the Inductors (No POP L21, L41 L22, L23, L28, L13, L129, and L131 Populate R348 - 359 ad R890, R891, R950, and R951) Please do this for M01 board build and for X00 Schematic	Modify.	0.3
88	27	H/W	01/06	CS	Remove L59, L62, L61, and L128 and replace all with 0-Ohm resistors for M01 Build and for X00 Schematic	Modify.	0.3
89	7	H/W	01/09	Steven	Del T332, T333 from schematic.	We add test point for SST2 now. So we remove the test point symbol. That will avoid test point double layered.	0.3
90	10	H/W	01/09	Steven	Del T380, T381, T300, T6 from schematic.	We add test point for SST2 now. So we remove the test point symbol. That will avoid test point double layered.	0.3
91	11	H/W	01/09	Steven	Del T2, T3, T4, T5 from schematic.	We add test point for SST2 now. So we remove the test point symbol. That will avoid test point double layered.	0.3
91	19	H/W	01/09	Steven	Del T375 from schematic.	We add test point for SST2 now. So we remove the test point symbol. That will avoid test point double layered.	0.3
92	21	H/W	01/09	Steven	Del T155 from schematic.	We add test point for SST2 now. So we remove the test point symbol. That will avoid test point double layered.	0.3
93	28	H/W	01/09	Steven	Del T280 from schematic.	We add test point for SST2 now. So we remove the test point symbol. That will avoid test point double layered.	0.3
94	36	H/W	01/09	Steven	Del T255, T259, T342, T344, T345, T346, T347, T348, T349, T350, T351, T352, T353, T354, T355, T356, T357, T358, T359, T360, T361, T362, T363, T364 from schematic.	We add test point for SST2 now. So we remove the test point symbol. That will avoid test point double layered.	0.3
95	37	H/W	01/09	Steven	Del T366, T367, T368, T370, T372, T373, T257, T258, T343, T365, T369, T374 from schematic.	We add test point for SST2 now. So we remove the test point symbol. That will avoid test point double layered.	0.3
96	37	H/W	01/09	CS	Delete R1198, R1199, R1200, R1201, R1202, R1203 and connect directly. Macallan III rev A IMCLK/IMDAT pair did not work properly. MacIII RevB has solved this issue.	Modify.	0.3
97	12	H/W	01/09	GF	Remove R1215 from schematic.	Modify.	0.3
98	13	H/W	01/09	GF	Remove L29, C47, C8, Connect DPLLA directly to +1.5vrun Remove L6, C48, C51, Connect DPLLB directly to +1.5vrun	Modify.	0.3
99	13	H/W	01/09	GF	Change C811 to the same component as C812.	Modify.	0.3
100	13	H/W	01/09	GF	No stuff C783 to support ext. vga.	Modify.	0.3

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101	18	H/W	01/09	CS	Add an 15U 25V De-pop capacitor C1290 in G_PWR_SRC for improve this power plane stablility	Modify.	0.3
102	18	H/W	01/12	CF	Add a no stuff cap. for add a CPU bulk decoupling pads back to layout.	Modify.	0.3
103	7	H/W	01/13	CF	Remove C450, C452 non-use item for saving Layout space	Modify.	0.3
104	43	H/W	01/17	CF	Delete H23 from M/B.	Modify.	0.3
105	16, 17	H/W	01/19	Bill	DDR termination swap.	For layout routing easy, swap pin define.	0.3
106	6	H/W	01/27	GF	Change BOM to support Dothan 533Mhz	No stuff R65, pop. R66.	0.3
107	29	H/W	01/27	PN	Change C1111 from 10uF to 22uF (1206)	Modify.	0.3
108	8	H/W	01/27	GF	Short PJP16 and open PJP17 for X00 build.	Modify.	0.3
109	29	H/W	01/27	PN	Populate R1180 to allow activating TPM mode.	Modify.	0.3
110	32	H/W	01/28	GF	changing C1201, C1202 to be the same as 0402 package as C1203 to save board space.	Modify.	0.3
111	10	H/W	01/28	GF	Intel recommends pop C745 with 0.1uf cap.	Modify.	0.3
112	36	H/W	01/28	CS	Populate R1238 for eliminate glitch..	Modify.	0.3
113	15	H/W	01/29	CS	C479 and C495 change to 47UF like Nimitz for cost savings.	Modify.	0.3
114	29	H/W	01/29	PN	V_2P5_LAN needs bigger bulk caps, add 2 more 22uF caps C1291, C1292	Modify.	0.3
115	29	H/W	01/30	PN	L155 replaced by 0 ohm resistor (R1245, 0Ohm 0603), C1215 and C1135 nopop.	Modify.	0.3
116	29	H/W	01/30	PN	L149, C1209 nopop.	Modify.	0.3
117	40	H/W	02/02	CS	no pop R454	Modify.	0.3
118	40	H/W	02/02	CS	Change U52 from the discontinued TFDU6101E to the new TFDU6102.	Modify.	0.3
119	20	H/W	02/02	CS	Add a no pop 33-ohm resistor (R1246) to PLTRST_LOM# and connect to PCIRSTB2# for pop option.	Modify.	0.3
120	20	H/W	02/02	CS	Add a no pop 33-ohm resistor (R1247) to PLTRST_VGA# and connect to PCIRSTB2# for pop option.	Modify.	0.3
121	41	H/W	02/02	CS	Q55 change to DI4810.-02/02	Modify.	0.3
122	29	H/W	02/02	CS	Removed F14 connect from L151 Pin 1	Modify.	0.3
123	42	H/W	02/02	CS	Change R1230 from 330 to 1K	Modify.	0.3

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124	43	H/W	02/02	CS	Change H6 to H_O463X408D433X378 Change H10 to H_O148X128D118X98	Modify.	0.3
125	16	H/W	02/02	CS	change C1047, C1049 to 0603 size for avoid highlimit issue in DIMM region.	Modify.	0.3
126	16	H/W	02/02	GF	Change C1048, C1046, C1045 and C1168 voltage rating to 6.3V for saving cost.	Modify.	0.3
127	17	H/W	02/02	GF	Change C143, C153, C1042-C1044 and C1177 voltage rating for save cost	Modify.	0.3
128	43	H/W	02/03	Steven	Add 3 EMI clip.	Modify.	0.3
129	29	H/W	02/04	PN	Pop R1102. Depop R1103, R1104	Modify.	0.3
130	21	H/W	02/04	GF	Populate R1248	Modify.	0.3
131	20	H/W	02/04	CS	Add a 0 ohm series termination R1251 between the ICH and U25A. This way we can go back to the origional M00 design	Modify.	0.3
132	29	H/W	02/04	PN	L149 and C1209 and connect U164 pin F14.	Modify.	0.3
133	6	H/W	02/04	CS	Move SATA clock pair to SRC4 pair on CK410. and connect PCIE_VGA clock to SRC3, PCIE_LOM clock to SRC1	Modify.	0.3
134	21	H/W	02/04	CS	Follow Issue list 1648 to remove the note of R940.	Modify.	0.3
135	21	H/W	02/04	CS	Follow Issue list 1646 to remove the note of R1248.	Modify.	0.3
136	20	H/W	02/05	GF	Add a pop resister R1252	Modify.	0.3
137	21	H/W	02/05	Steven	Currect the Note of R940 and R1248.	Modify.	0.3
138	20,22,28	H/W	02/05	Steven	SWAP RN118, RN117, RN6, RN130, RN121, RN1, RN120, RN131, C13, C14 pin connect for layout routing.	Modify.	0.3
139	43	H/W	02/06	ME	Modify H1, H2, H3, H4, H12, H20 as ME request	Modify.	0.3
140	41	H/W	02/06	CS	Change R605 to 100K for proper voltage level during low battery charge state.	Modify.	0.3
141	35	H/W	02/07	CS	Add D76 in Q43 DOCKED for potection ESD damage.	Modify.	0.3
142	41	H/W	02/07	CS	Change Q55 to DI4800 for cost saving.	Modify.	0.3
143	41	H/W	02/07	Steven	Add a no-pop Q131 3456 parallel with Q55 for this build.	Modify.	0.3
144	43	H/W	02/07	Steven	Remove a no use EMI clip CLP3	Modify.	0.3
145	30	H/W	02/07	Steven	Change RJ1 connector from 5PIN to 2PIN.	Modify.	0.3
146	41	H/W	02/07	ME	Change smart card connector as ME request.	Modify.	0.3

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P47	+1.5VSUSP / +VCCP_1P05VP	12/09/2003	Dell	PL12 choke had height limitation on secondary side	Change PL12 from CDRH125 4.4uH_5A to SIL1035 5uH_5.5A	0.1
2	P48	+1.8VSUSP/ +0.9V_DDR_VTT	12/09/2003	Compal	Change SC1486 to SC1486A for DDR2 (REFIN threshold voltage change from 0.8V to 0.5V)	Change PU6 from SC1486 to SC1486A version	0.1
3	P47	+1.5VSUSP / +VCCP_1P05VP	12/12/2003	Dell	Add a diode between the PU5 PGOOD signal and ON1 signal, so that when ON1 is low, PGOOD is low. And when ON1 is high, PGOOD is released and can go high.	This is a new VCCP powergood solution. Changing to match Azeda.	0.1
4	P47	+1.5VSUSP / +VCCP_1P05VP	12/12/2003	Dell	Change PR232 pull-up voltage to +3VSUS.	Change PR232 pull-up voltage from +5VSUS to +3VSUS.	0.1
5	P47	+1.5VSUSP / +VCCP_1P05VP	12/12/2003	Dell	Change MAX1845_PWRGD signal name to VCCP_PWRGD	Implementing new powergood solution for VCCP.	0.1
6	P47	+1.5VSUSP / +VCCP_1P05VP	12/12/2003	Dell	Depopulate PD30 and PD31	Don't use for cost down	0.1
7	P49	+VCORE	12/12/2003	Dell	Change PC123 from 47pF to 270pF	Improve noise immunity with a reduction in the transient response speed.	0.1
8	P47	+1.5VSUSP / +VCCP_1P05VP	12/12/2003	Dell	Change SUSPWROK_1.5V signal to SUSPWROK_1P8V.	To match other D'05 platforms, this change will also reduce the amount of logic gates for power sequencing circuitry.	0.1
9	P45	Battery Conn./+2.5V	12/16/2003	Compal	Change to Power materials	Change C1288 to PC176, R1224 to PR233.	0.1
10	P47	+1.5VSUSP / +VCCP_1P05VP	12/18/2003	Dell	Delete PR232, not needed	Deleted because PR105 had existed.	0.1
11	P50	Charger	01/08/2004	Dell	Add PD37, PR234 to fix MAX1535A Charger issue when battery undervoltage is defected. Will waiting MAX1535B and delete it.	Add PD37, PR234	X00
12	P48	+1.8VSUSP/ +0.9V_DDR_VTT	01/27/2004	Dell	Implement MAX8550 regulator	Delete SC1486A regulator and adding MAX8550 Regulator for DDR2 power source.	X01
13	P46	+3.3V/+5V/+15V	01/28/2004	Dell	Adding +15V current limit	Add PC196 PR245 and Change PC38	X01
14	P47	+1.5VSUSP / +VCCP_1P05VP	02/02/2004	Dell	Change PC74 ESR from SER 15m to 9 m ohms.	Change PC74 from 330u_15m to 330u_9m.	X01
15	P48	+1.8VSUSP/ +0.9V_DDR_VTT	02/02/2004	Dell	Adding PJP31, PJP32 Jump, +1.8VSUS or 1.5VRUN input voltage for VTTI of Max8550	Adding PJP31, PJP32 Jump.	X01
16	P48	+1.8VSUSP/ +0.9V_DDR_VTT	02/02/2004	Dell	Modify +1.8VSUS Regulator OCP	Change PR244 from 53.6K to 48.7K.	X01
17	P48	+1.8VSUSP/ +0.9V_DDR_VTT	02/02/2004	Dell	Modify Bypass capacitor Power supply for DL Gate driver of MAX8550	Change PC181 from 1uF to 4.7uF.	X01
18	P48	+1.8VSUSP/ +0.9V_DDR_VTT	02/05/2004	Dell	Reserve PC198 for the future cost down.	Add @ PC198.	X01
19	P44	+DCIN	02/05/2004	Dell	Change PR219 to 2.2Kohms per AC Adapter group reccomendation.	Change PR219 from 1.5K to 2.2K ohms.	X01
20	P45	Battery Conn./+2.5V	02/05/2004	Dell	Change PR233 to achieve proper 1ms powerup delay.	Change PR233 from 10k to 27kohms.	X01
21	P50	Charger	02/05/2004	Dell	Add note to +VCHGR rail - "Maximum Battery Charge current = 6.2A when system off"	Add note to Charger circuit	X01
22	P48	+1.8VSUSP/ +0.9V_DDR_VTT	02/06/2004	Compal	Change 1.8V Regulator switch frequence from 450k to 300kHz	depopulate PR241	X01
23	P48	+1.8VSUSP/ +0.9V_DDR_VTT	02/07/2004	Dell	Install jumper on PJP32 pad to connect to 1.5VSUS	PopPJP32 pad and depop PJP31.	X01

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24	P47	+1.5VSUSP / +VCCP_1P05VP	02/09/2004	Compal	Bypass power derating	Change PC68 from 1uF_6.3v to 1uF_10v	X01
25	P50	Charger	02/09/2004	Compal	Bypass power derating	Change PC141 from 1uF_6.3v to 1uF_10v	X01