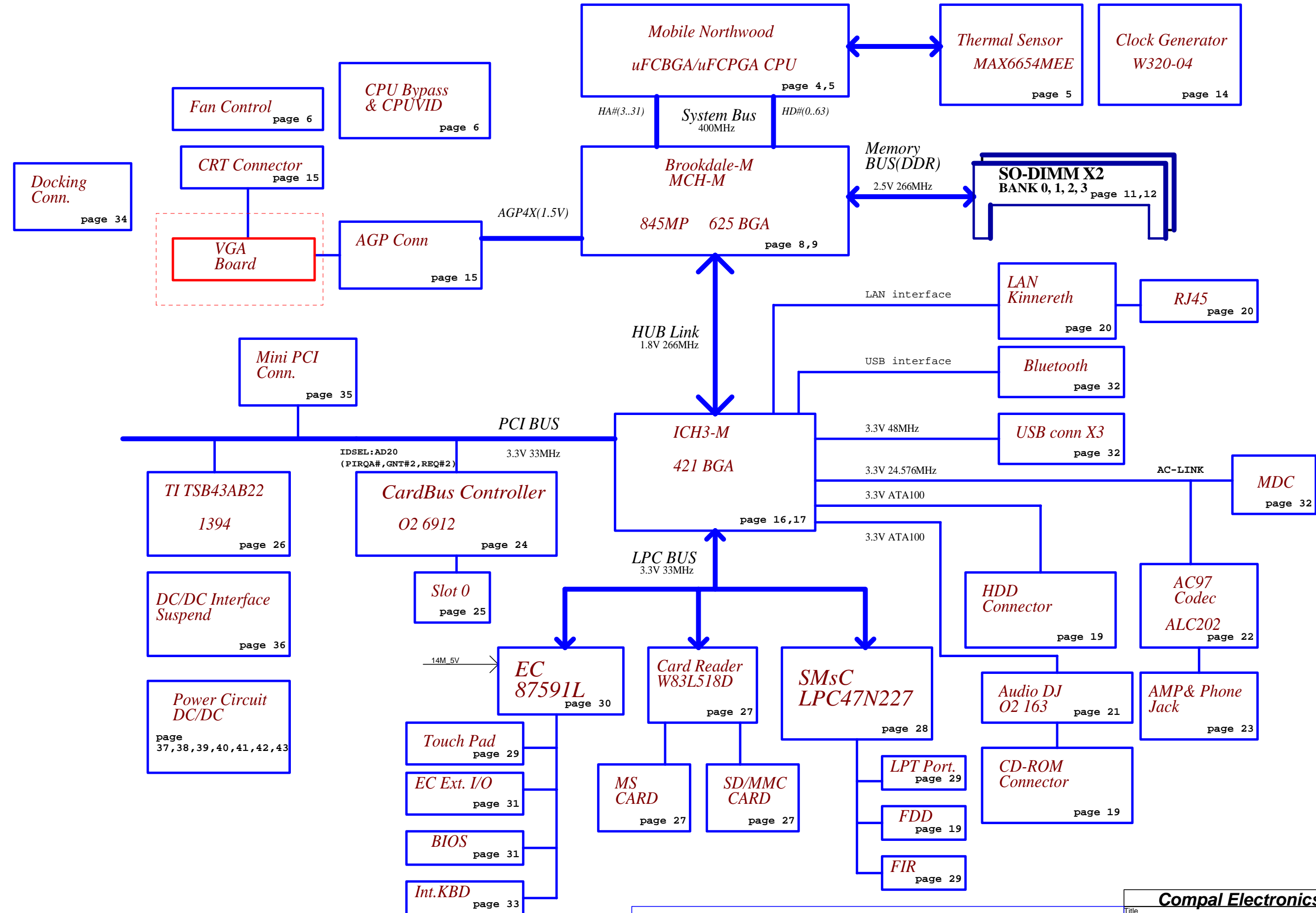


LA-1511 REV1.0 Schematics Document

uFCBGA/uFCPGA Northwood with Brookdale chipset(845MP+ICH3-M)

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Power Managment table

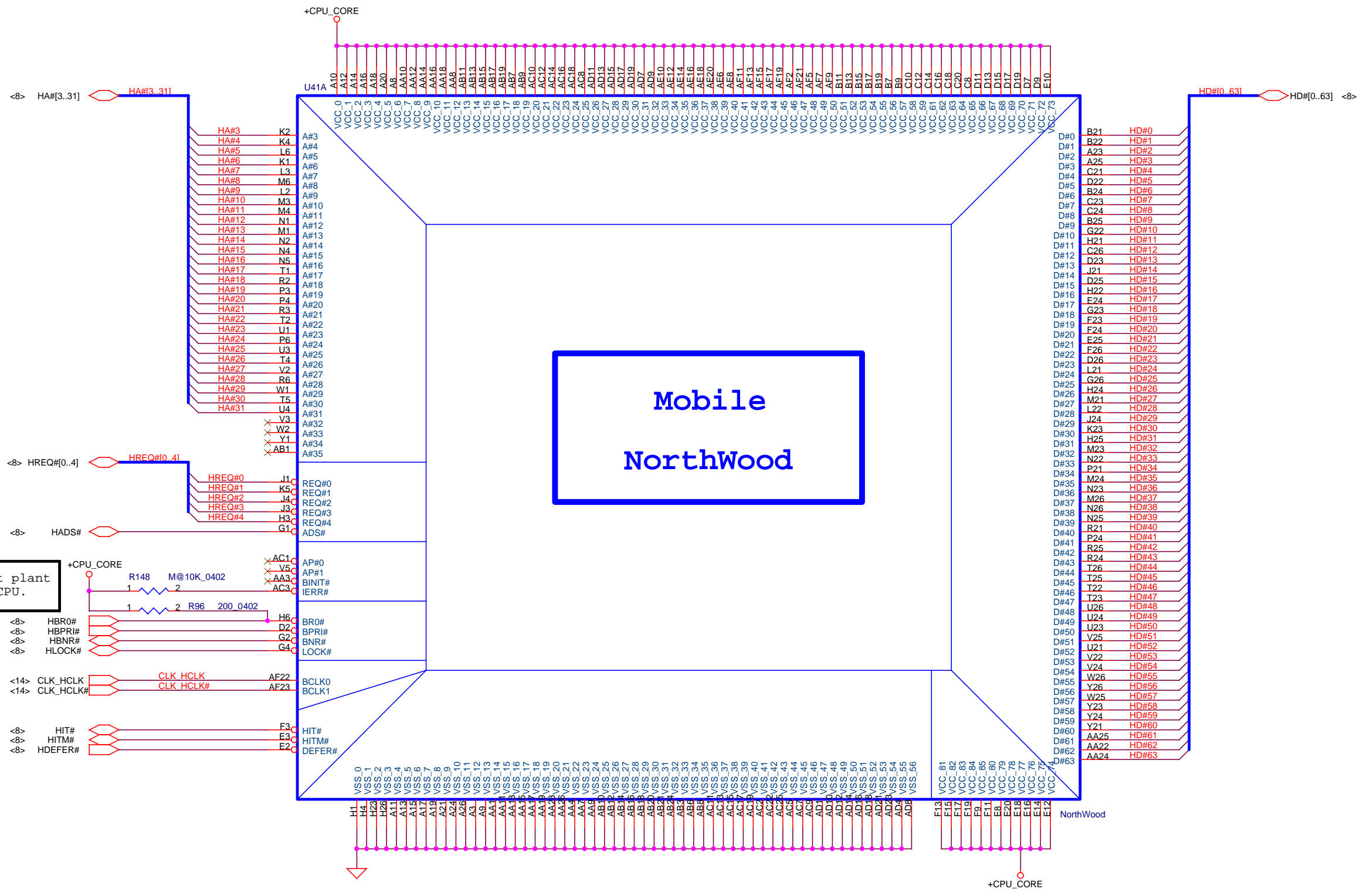
State \ Signal	+3VALW +5VALW +1.8VALW +12VALW	+3V +5V +2.5V	+12VS +5VS +3VS +2.5VS +1.8VS +1.5VS +1.2VP +CPU_CORE +1.25VS +1.25VS_VGA
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

	NB Chip Rev	SB Chip Rev

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Mobile NorthWood

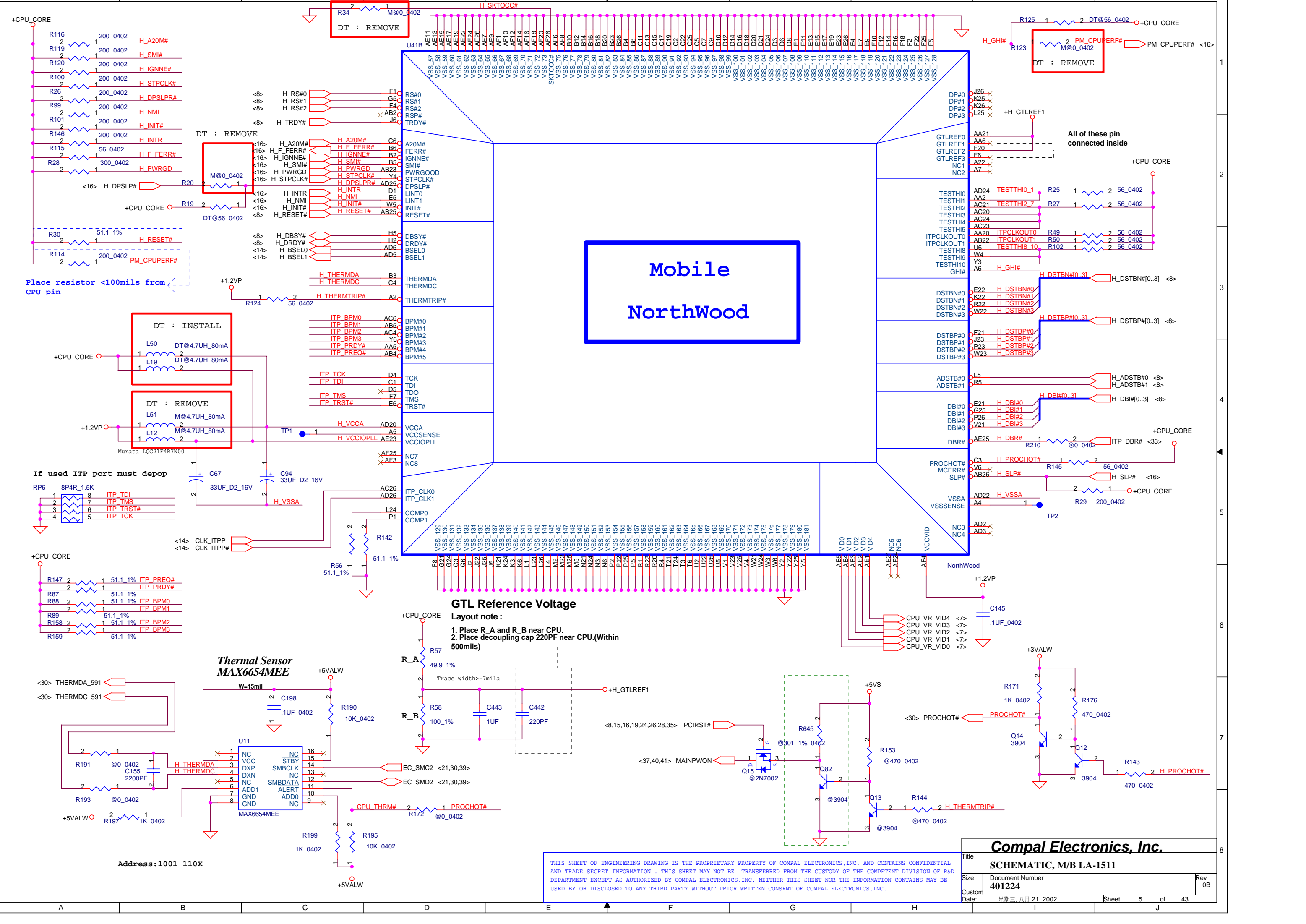


R148 not plant for DT CPU.

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Mobile NorthWood



GTL Reference Voltage
Layout note:
 1. Place R_A and R_B near CPU.
 2. Place decoupling cap 220PF near CPU.(Within 500mils)

Thermal Sensor
MAX6654MEE

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Place resistor <100mils from CPU pin

All of these pin connected inside

DT : REMOVE

DT : INSTALL

DT : REMOVE

If used ITP port must depop

Address: 1001_110X

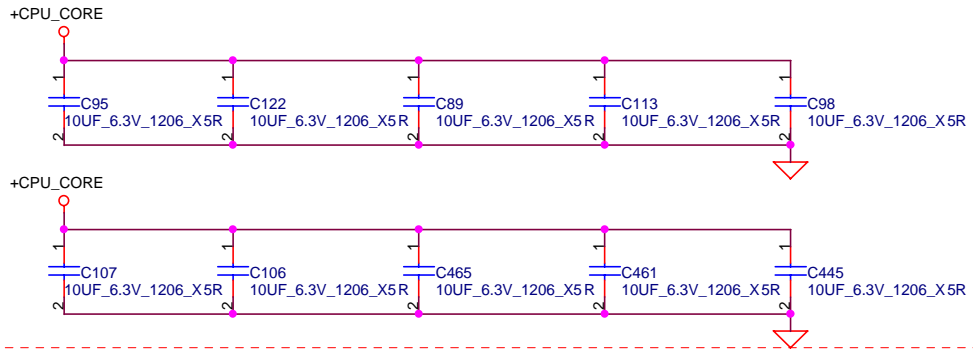
Layout note :
 Place close to CPU, Use 2-3 vias per PAD.
 Place .22uF caps underneath balls on solder side.
 Place 10uF caps on the peripheral near balls.
 Use 2-3 vias per PAD.

Layout note :
 Place close to CPU power and ground pin as possible (<1inch)

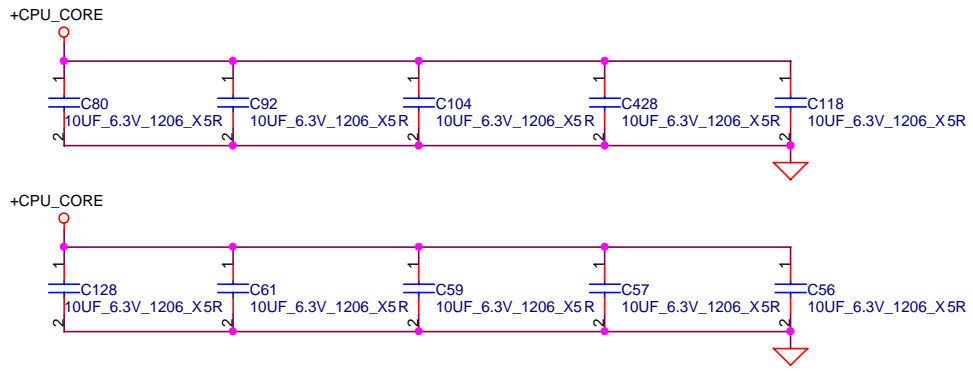
For Desktop's CPU:
 ESR total=0.75m ohm
 C total=6350uF

For Mobile's CPU:
 ESR total=1.875m ohm
 C total=2590uF

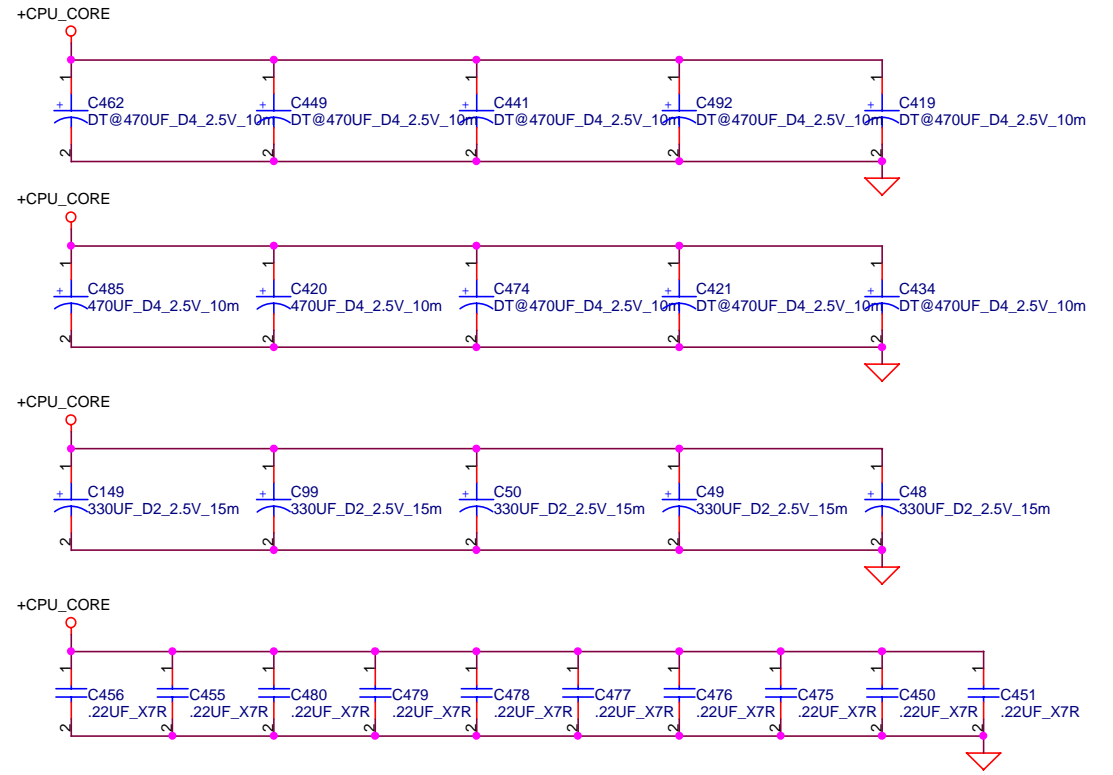
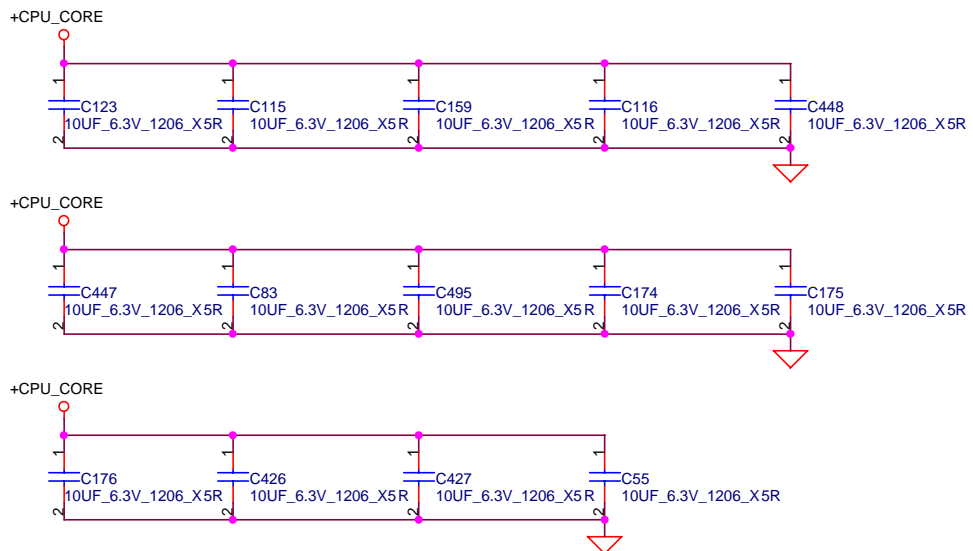
Please place these cap in the socket cavity area



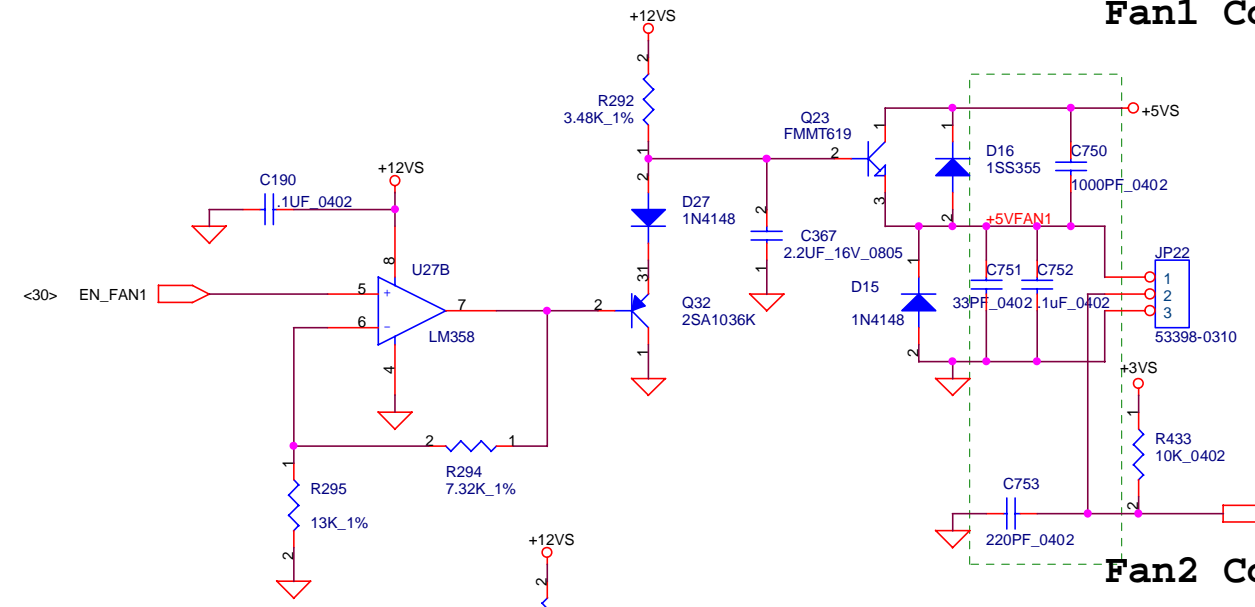
Please place these cap on the socket north side



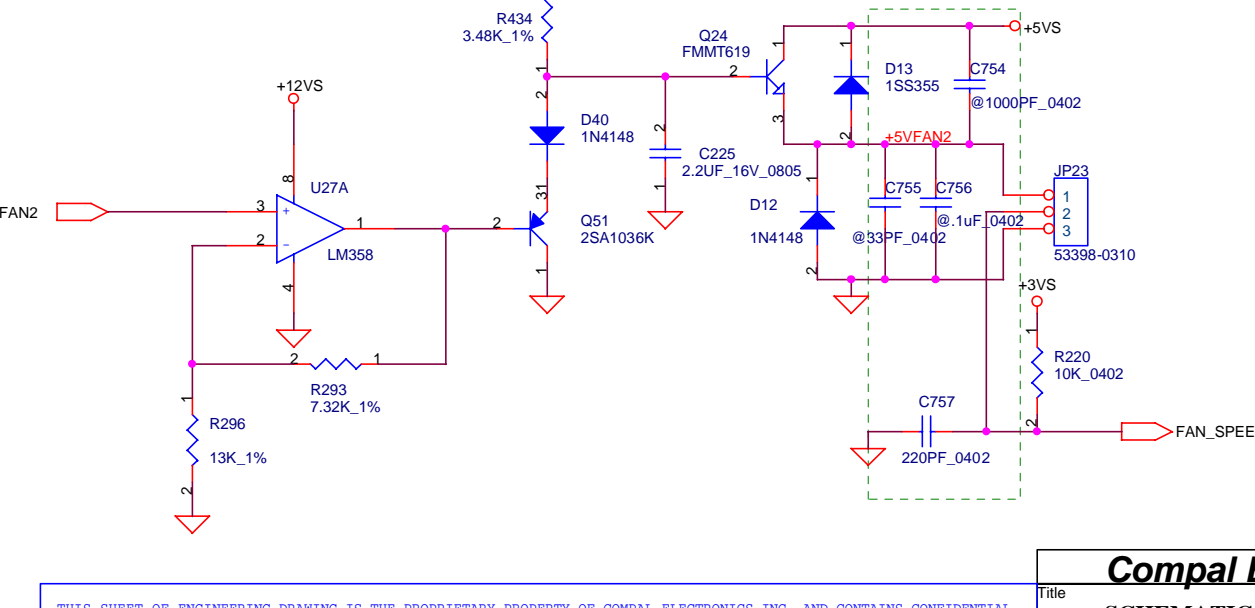
Please place these cap on the socket south side



Fan1 Control circuit



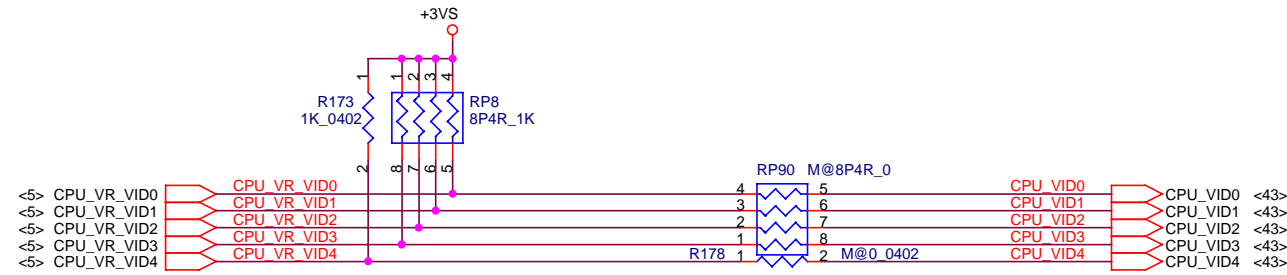
Fan2 Control circuit



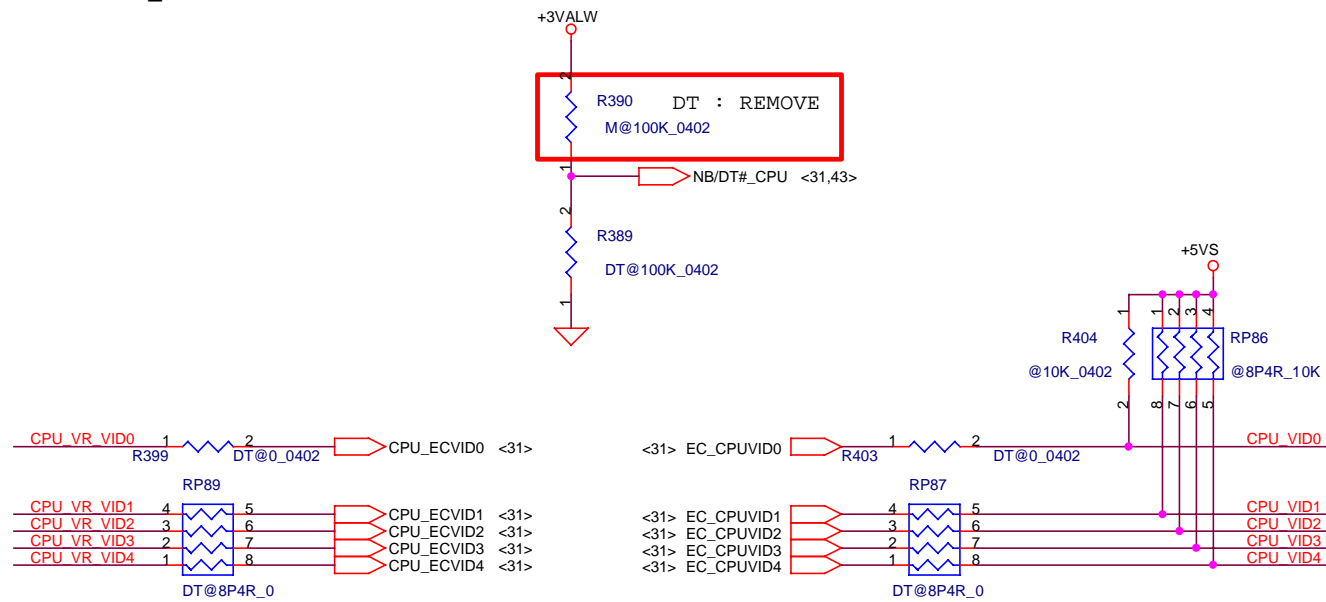
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For Mobile CPU



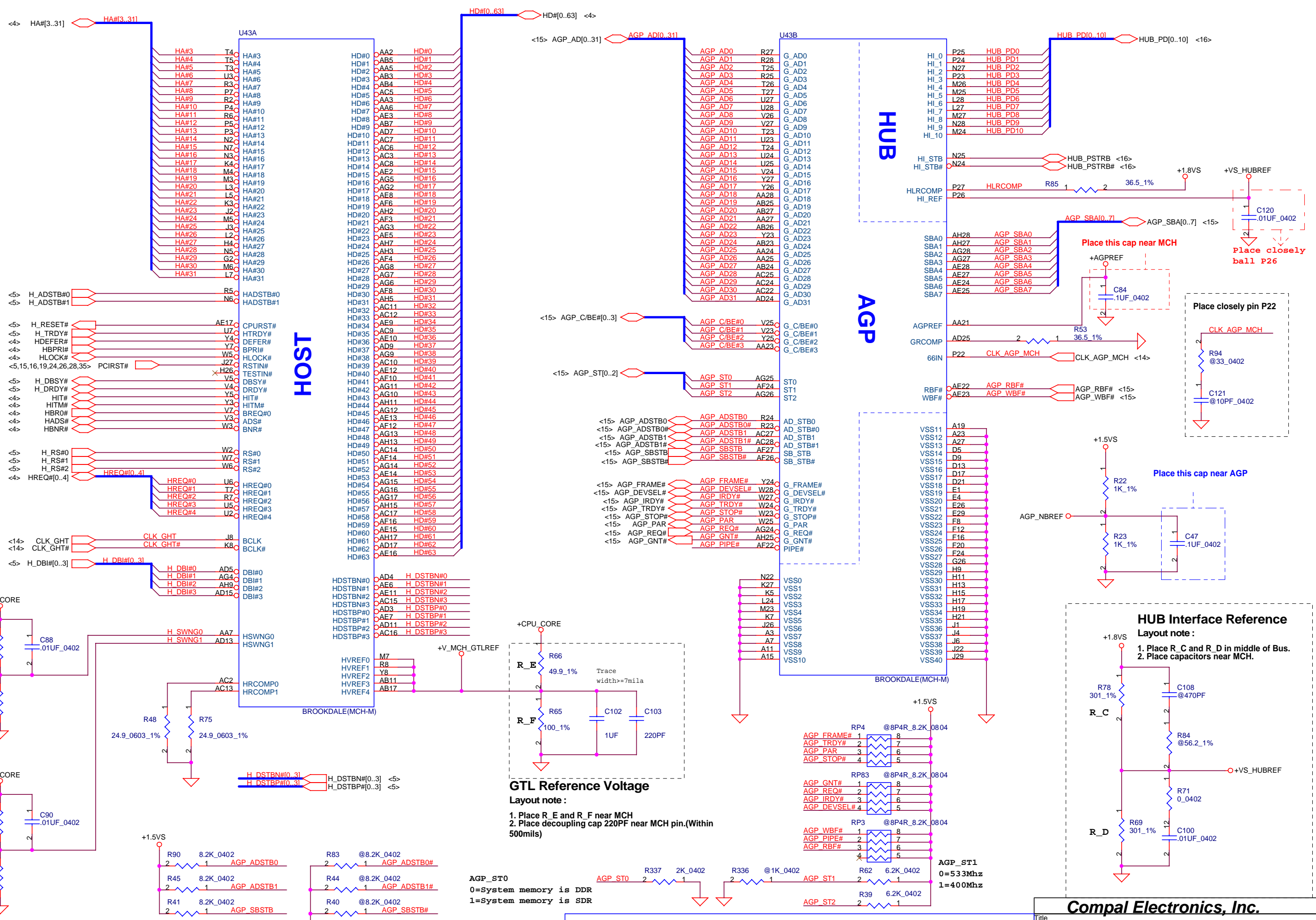
For Desktop CPU



	Mobil CPU					Destop CPU				
NB/DT_CPU	1					0				
VID	4	3	2	1	0	4	3	2	1	0
VCC										
1.750V	0	0	0	0	0	0	0	1	0	0
1.700V	0	0	0	0	1	0	0	1	1	0
1.650V	0	0	0	1	0	0	1	0	0	0
1.600V	0	0	0	1	1	0	1	0	1	0
1.550V	0	0	1	0	0	0	1	1	0	0
1.500V	0	0	1	0	1	0	1	1	1	0
1.450V	0	0	1	1	0	1	0	0	0	0
1.400V	0	0	1	1	1	1	0	0	1	0
1.350V	0	1	0	0	0	1	0	1	0	0
1.300V	0	1	0	0	1	1	0	1	1	0
1.250V	0	1	0	1	0	1	1	0	0	0
1.200V	0	1	0	1	1	1	1	0	1	0
1.150V	0	1	1	0	0	1	1	1	0	0
1.100V	0	1	1	0	1	1	1	1	1	0
1.050V	0	1	1	1	0	X	X	X	X	X
1.000V	0	1	1	1	1	X	X	X	X	X
0.975V	1	0	0	0	0	X	X	X	X	X
0.950V	1	0	0	0	1	X	X	X	X	X
0.925V	1	0	0	1	0	X	X	X	X	X
0.900V	1	0	0	1	1	X	X	X	X	X
0.875V	1	0	1	0	0	X	X	X	X	X
0.850V	1	0	1	0	1	X	X	X	X	X
0.825V	1	0	1	1	0	X	X	X	X	X
0.800V	1	0	1	0	1	X	X	X	X	X
0.775V	1	1	0	1	0	X	X	X	X	X
0.750V	1	1	0	0	1	X	X	X	X	X
0.725V	1	1	0	1	0	X	X	X	X	X
0.700V	1	1	0	1	1	X	X	X	X	X
0.675V	1	1	1	0	0	X	X	X	X	X
0.650V	1	1	1	0	1	X	X	X	X	X
0.625V	1	1	1	1	0	X	X	X	X	X
0.600V	1	1	1	1	1	X	X	X	X	X
VRM output off	1	1	1	1	1	1	1	1	1	1

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HOST

HUB

AGP

GTL Reference Voltage

- Layout note :
1. Place R_E and R_F near MCH
 2. Place decoupling cap 220PF near MCH pin.(Within 500mils)

AGP_ST0
 0=System memory is DDR
 1=System memory is SDR

HUB Interface Reference

Layout note :

1. Place R_C and R_D in middle of Bus.
2. Place capacitors near MCH.

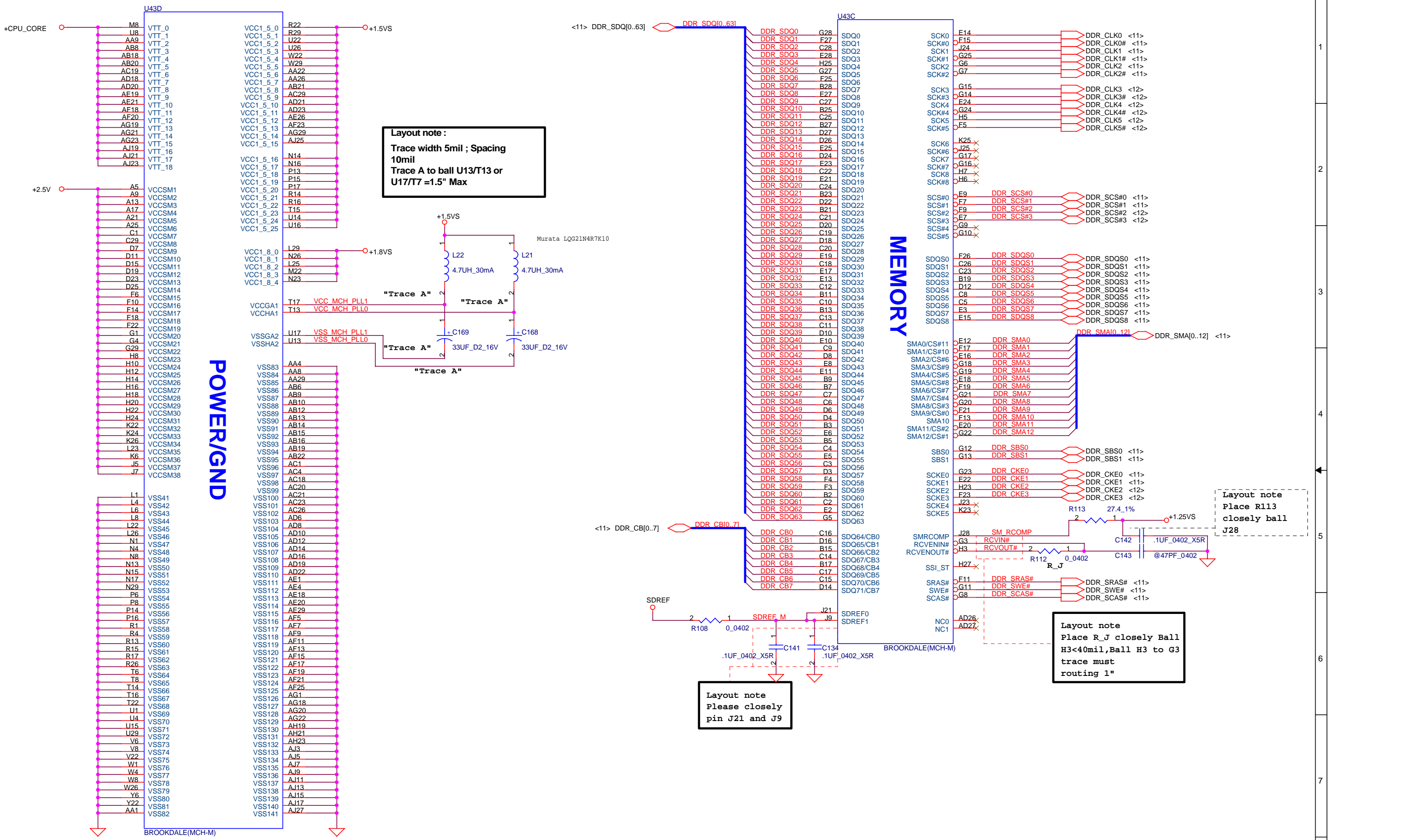
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Layout note :
 Trace width 5mil ; Spacing 10mil
 Trace A to ball U13/T13 or U17/T7 =1.5" Max

Layout note
 Place R113 closely ball J28

Layout note
 Place R_J closely Ball H3<40mil, Ball H3 to G3 trace must routing 1"

Layout note
 Please closely pin J21 and J9

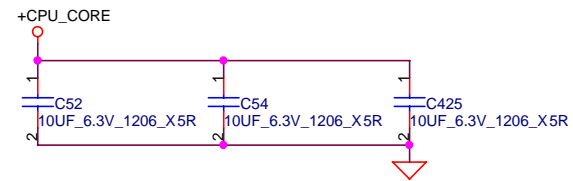
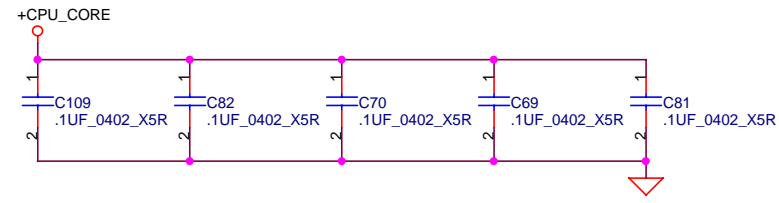
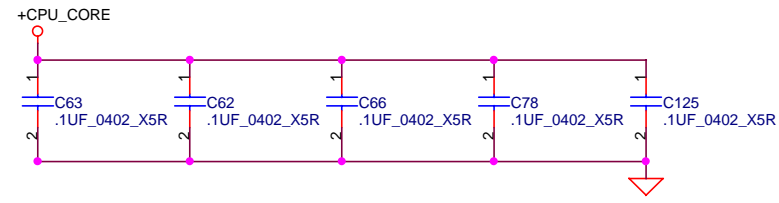
POWER/GND

MEMORY

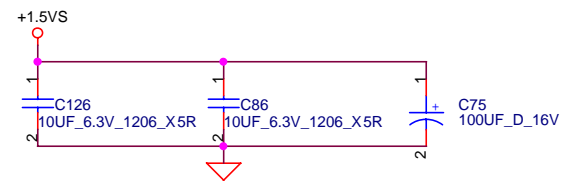
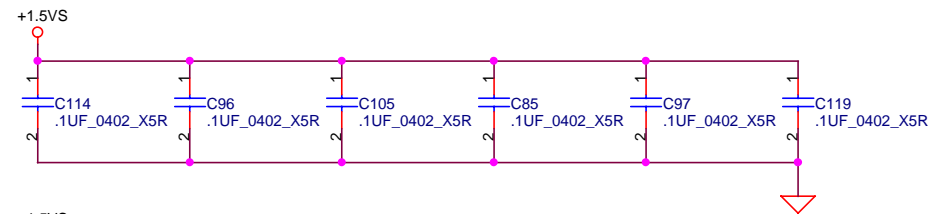
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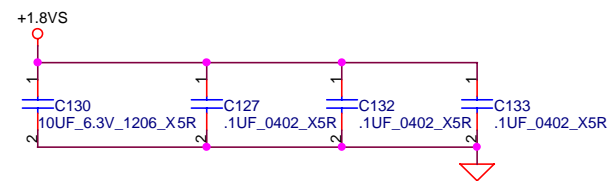
Layout note : Processor system bus
Distribute as close as possible to MCH Processor Quadrant.(between VTTF5B and VSS pin)



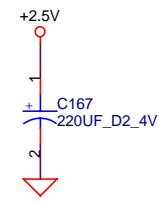
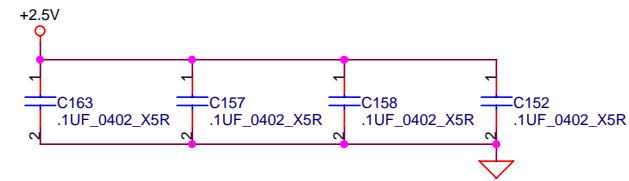
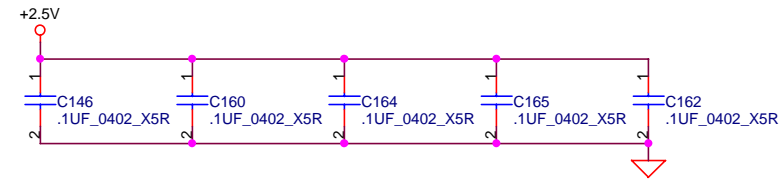
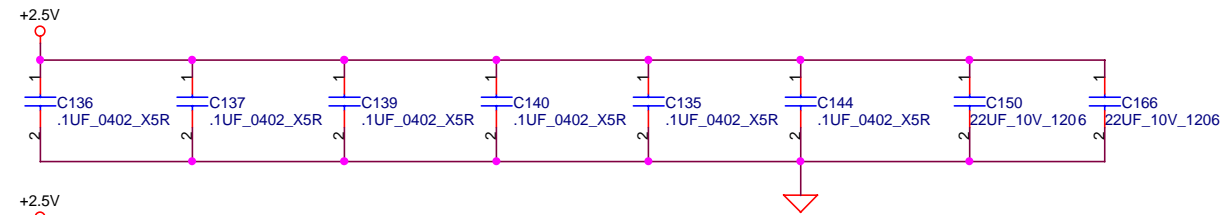
Layout note : AGP / CORE
Distribute as close as possible to MCH Processor Quadrant.(between VCCAGP/VCCCORE and VSS pin)



Layout note : Hub-Link
Distribute as close as possible to MCH Processor Quadrant.(between VCCHL and VSS pin)



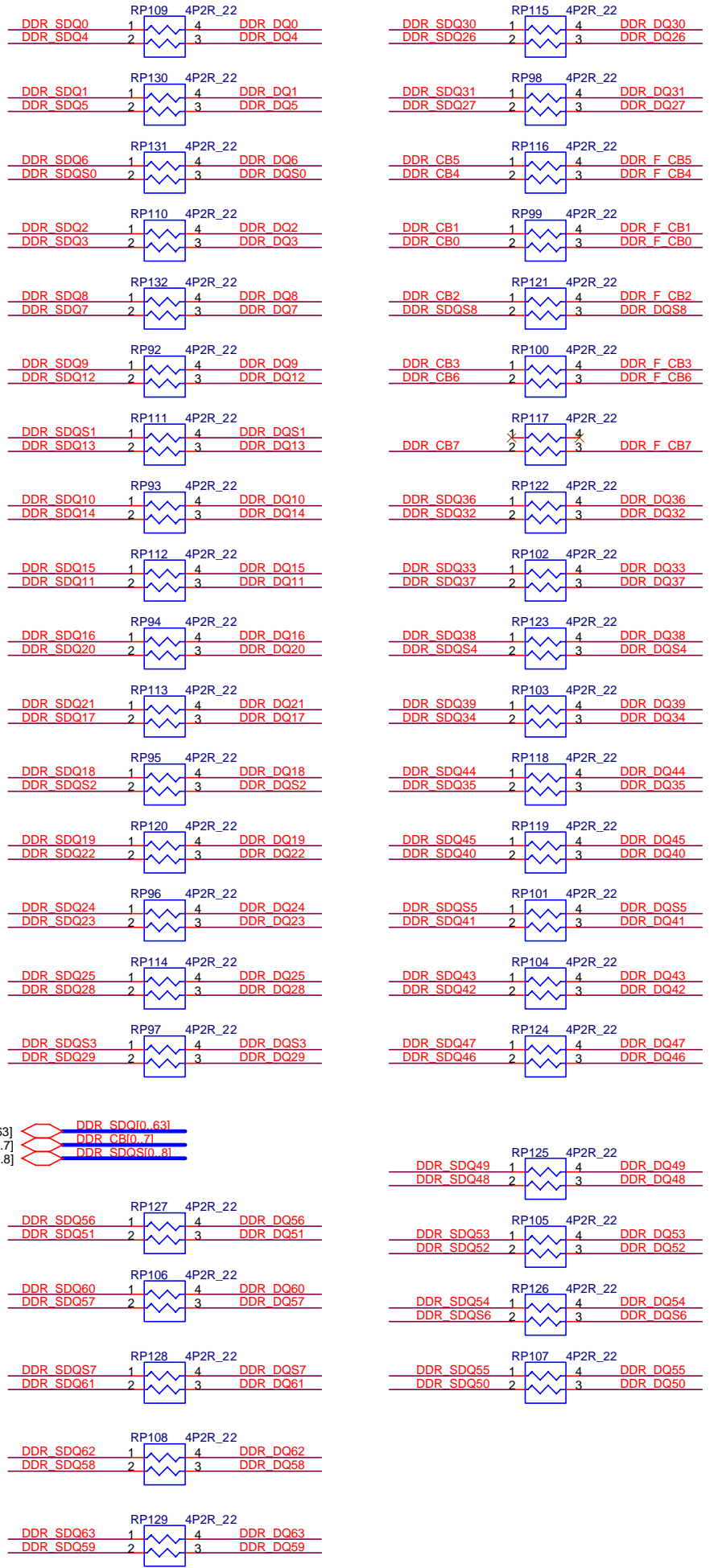
Layout note : DDR Memory interface
Distribute as close as possible to MCH Processor Quadrant.(between VCCSM and VSS pin)



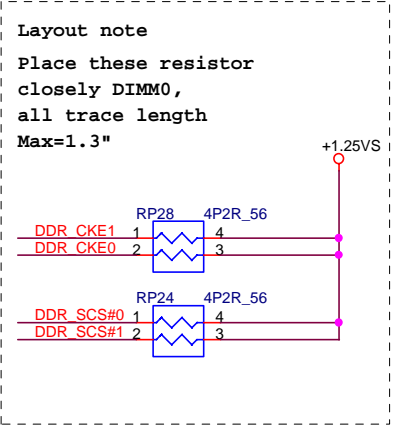
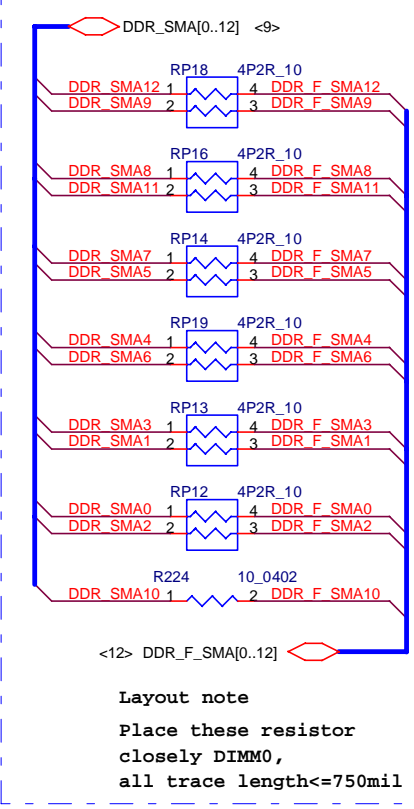
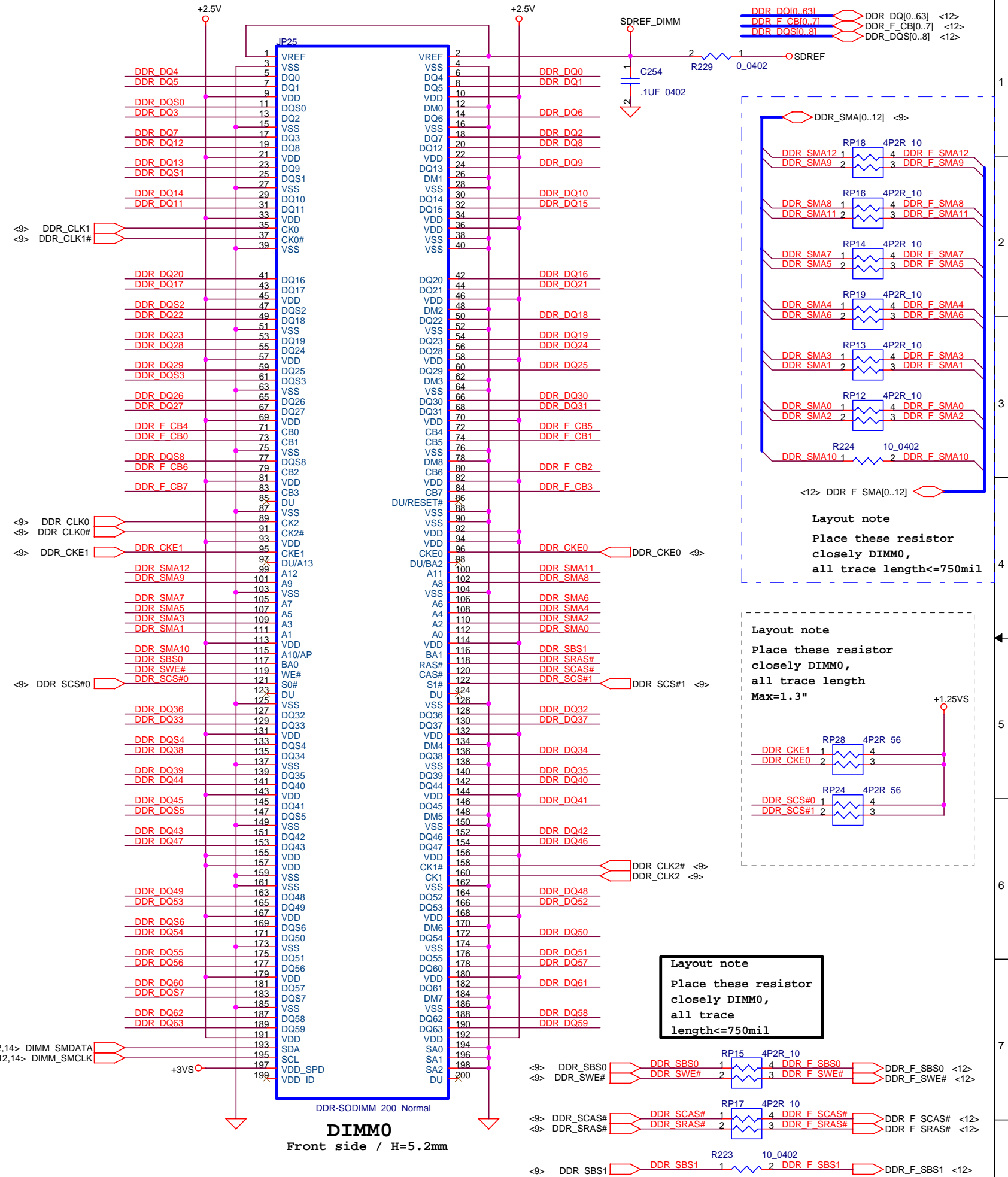
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Layout note
Place these resistor closely DIMM0, all trace length<750mil



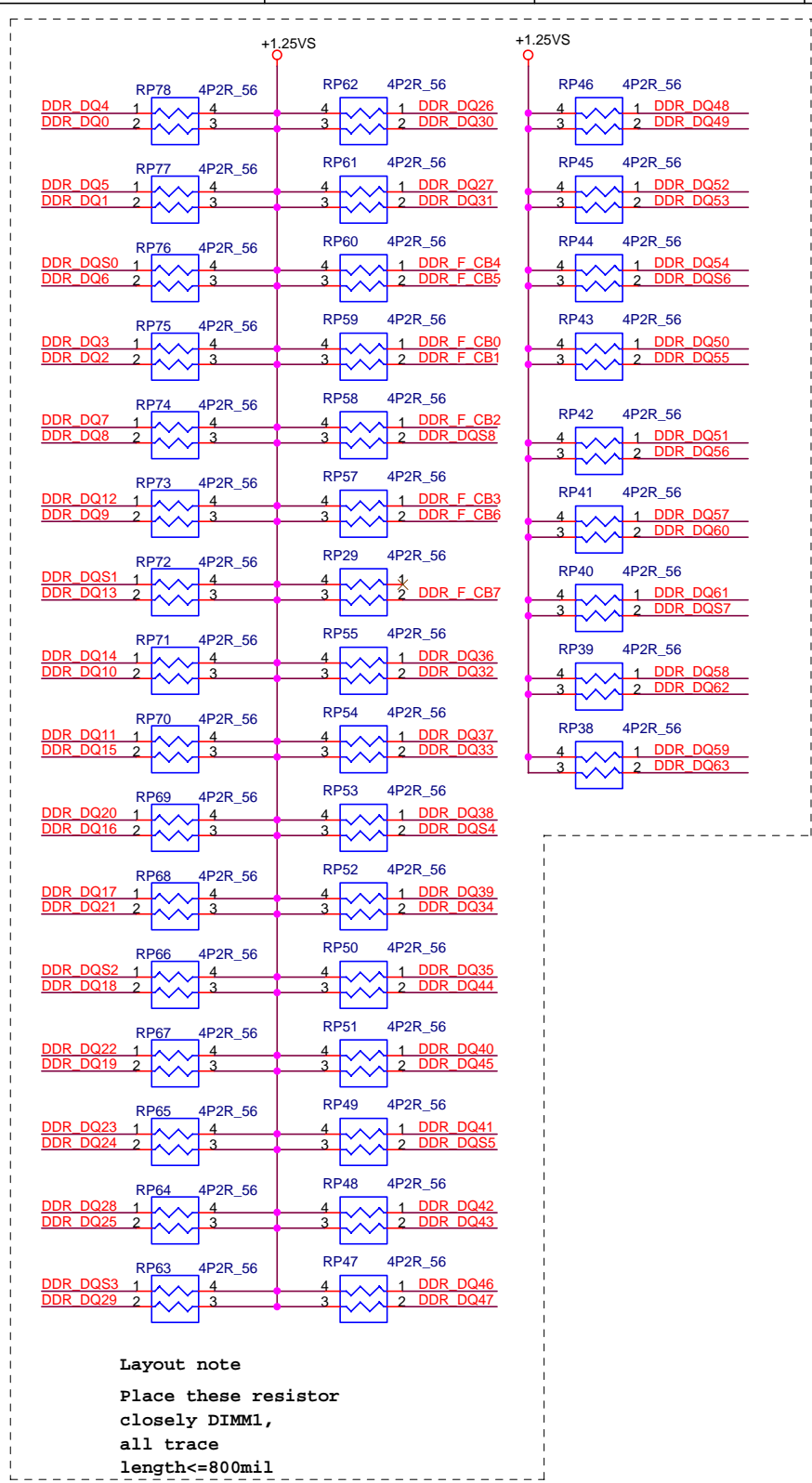
<9> DDR_SQ[0..63] DDR_SQ[0..63]
<9> DDR_CB[0..7] DDR_CB[0..7]
<9> DDR_QS[0..8] DDR_QS[0..8]



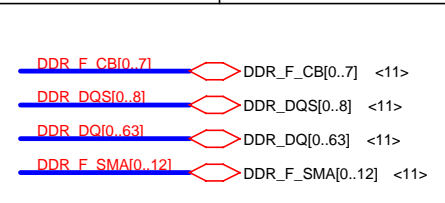
Layout note
Place these resistor closely DIMM0, all trace length<=750mil

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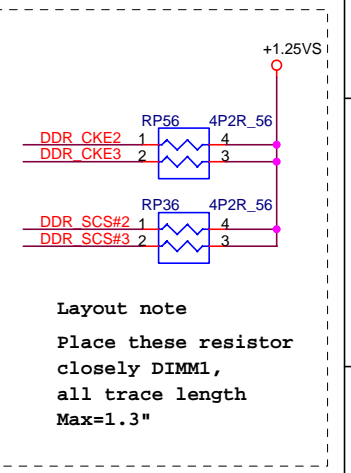
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Layout note
Place these resistor closely DIMM1, all trace length=<800mil



DIMM1
Back side / H=9.2mm

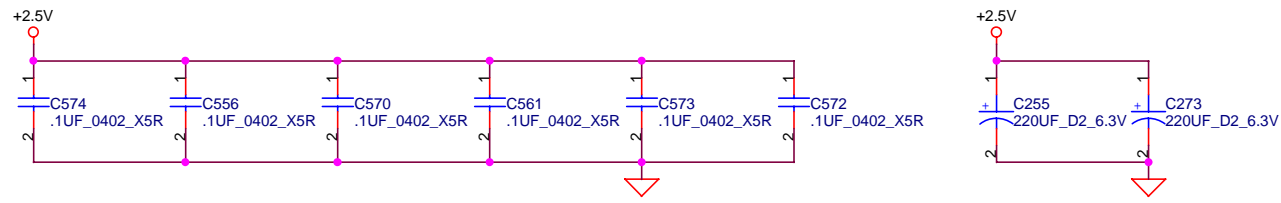
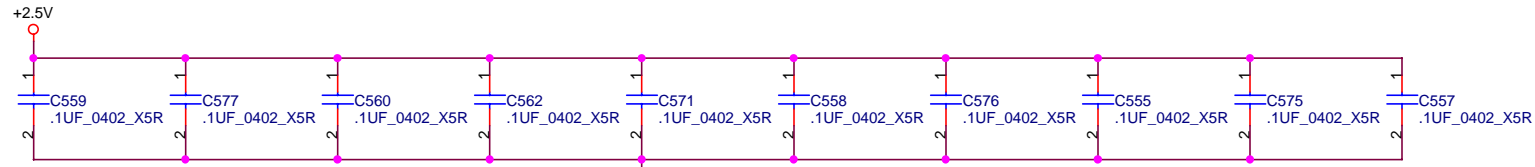


Layout note
Place these resistor closely DIMM1, all trace length Max=1.3"

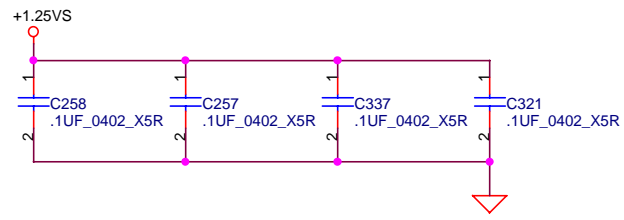
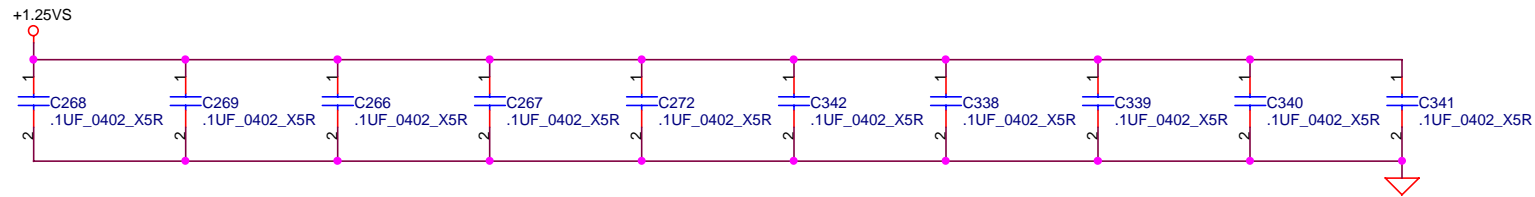
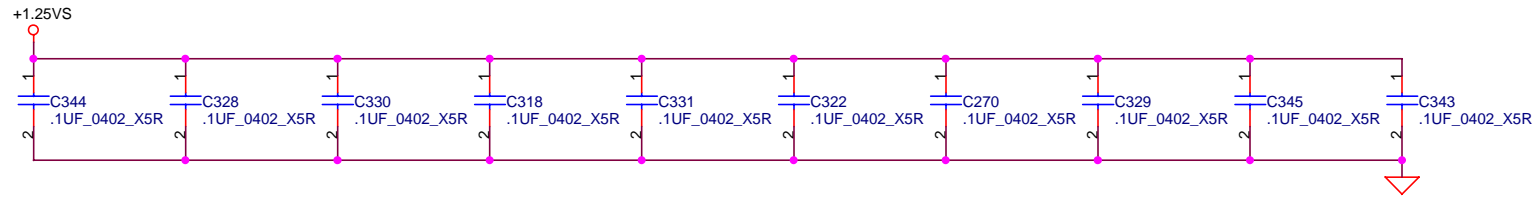
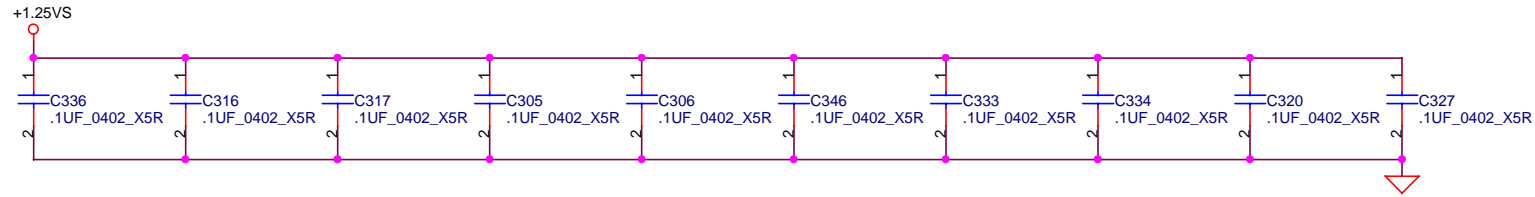
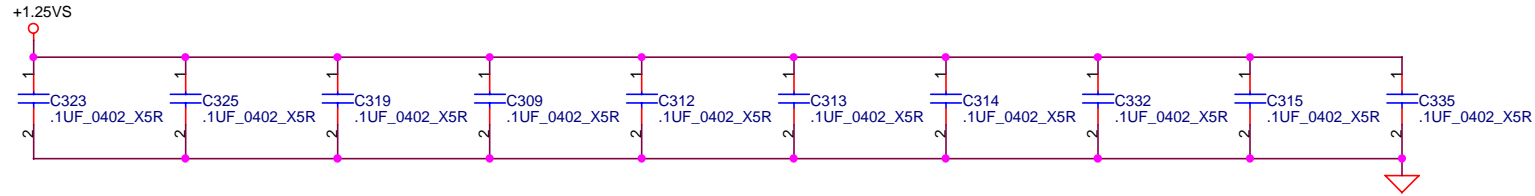
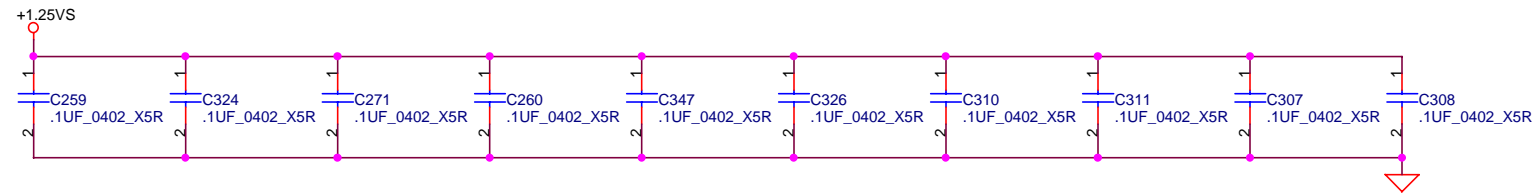
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Layout note :
Distribute as close as possible to DDR-SODIMM.



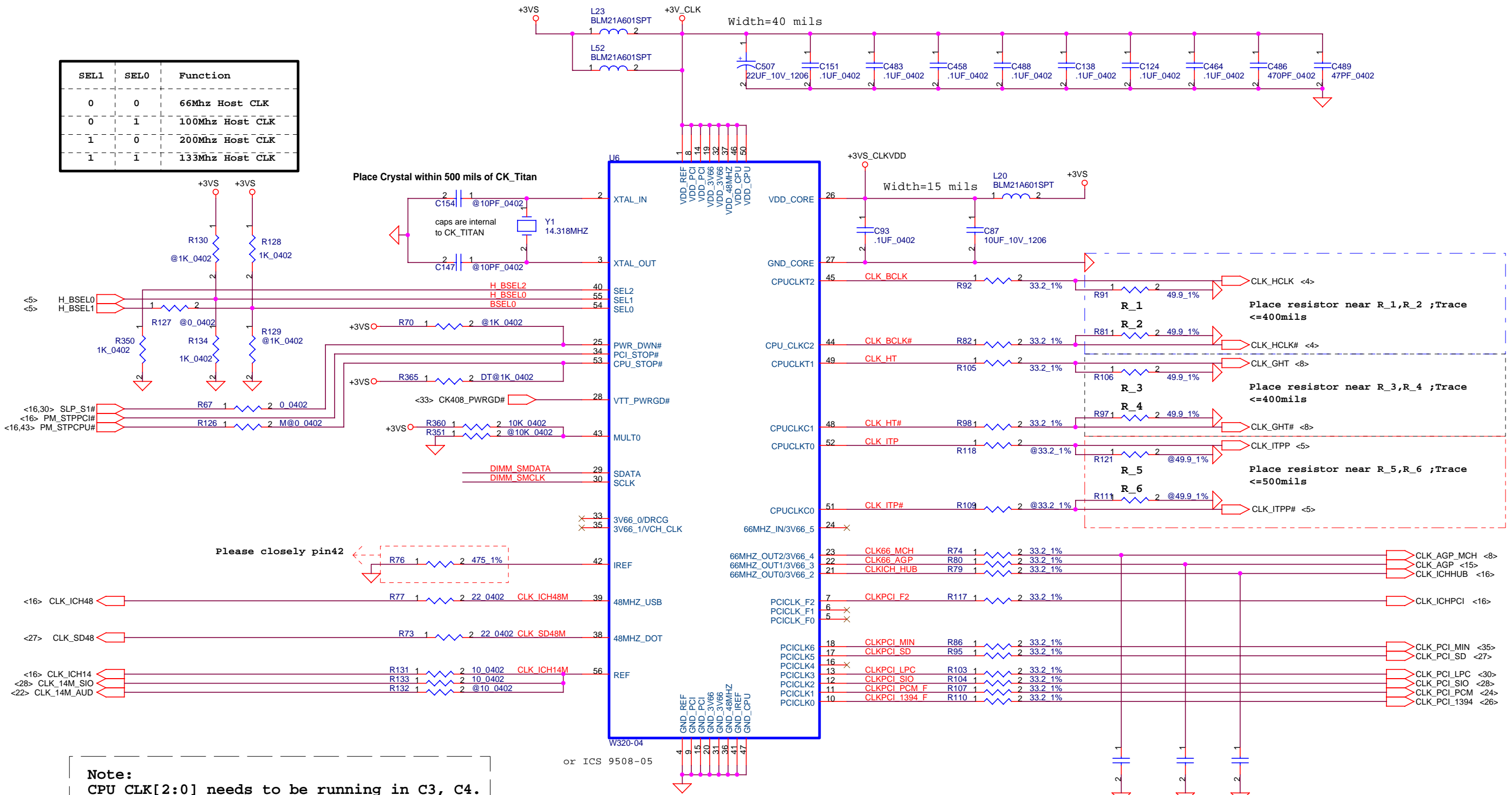
Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25V



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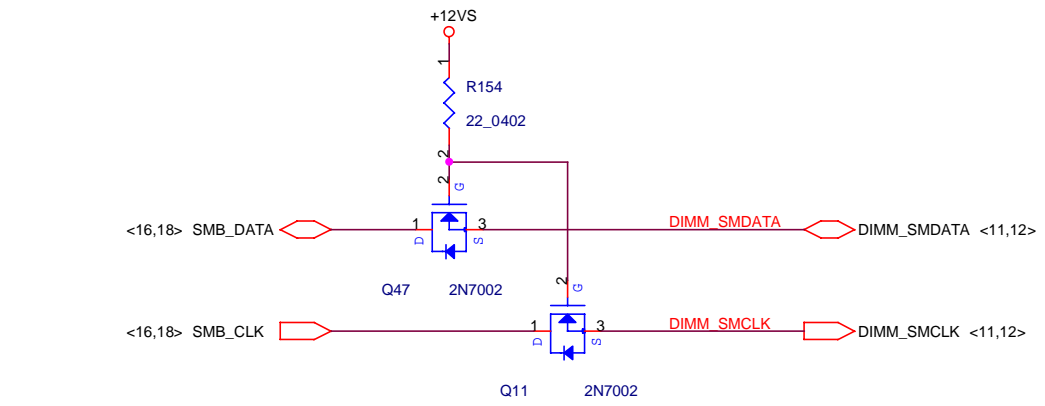
SEL1	SEL0	Function
0	0	66MHz Host CLK
0	1	100MHz Host CLK
1	0	200MHz Host CLK
1	1	133MHz Host CLK



Place Crystal within 500 mils of CK_Titan

Please closely pin42

Note: CPU_CLK[2:0] needs to be running in C3, C4.



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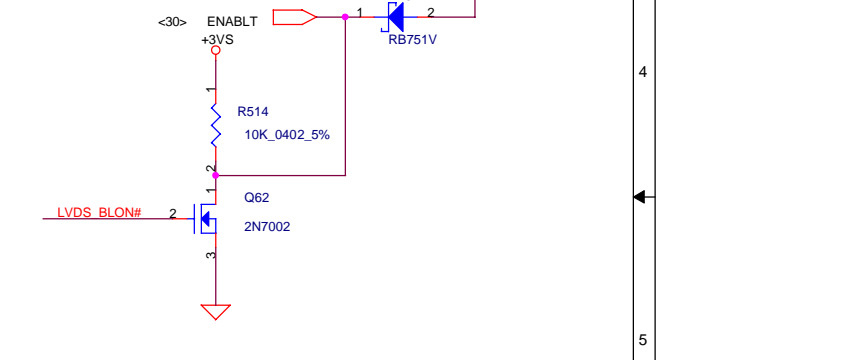
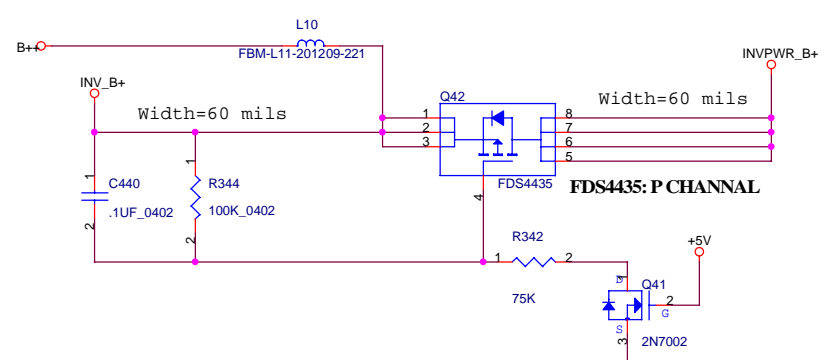
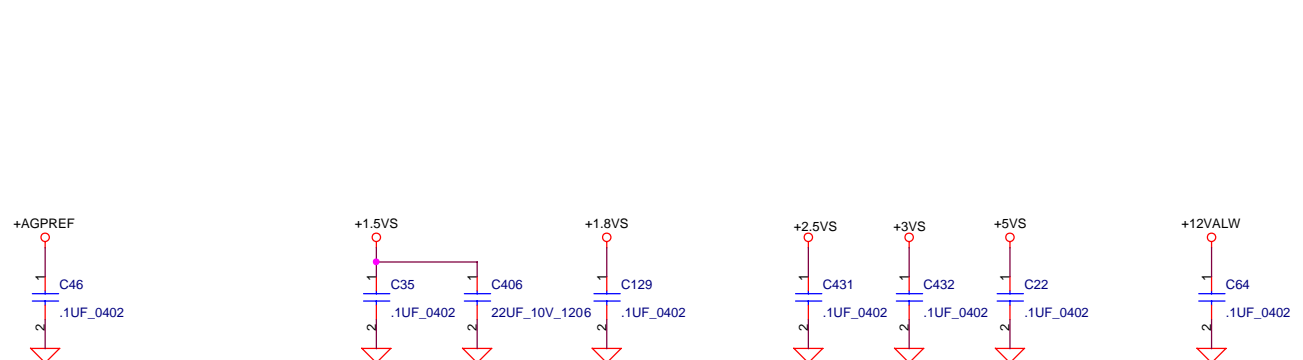
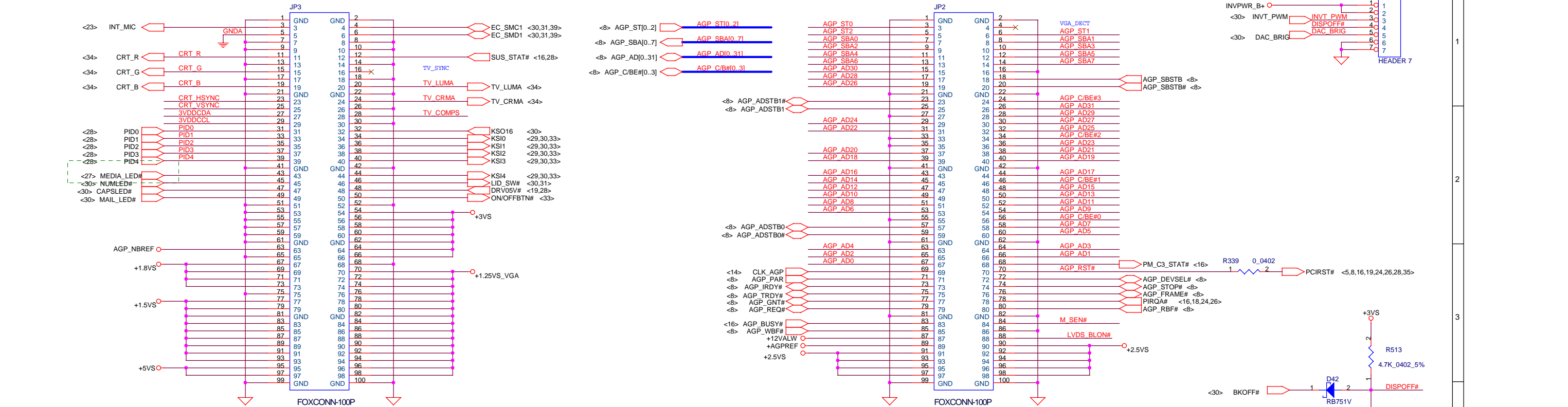
Compal Electronics, Inc.

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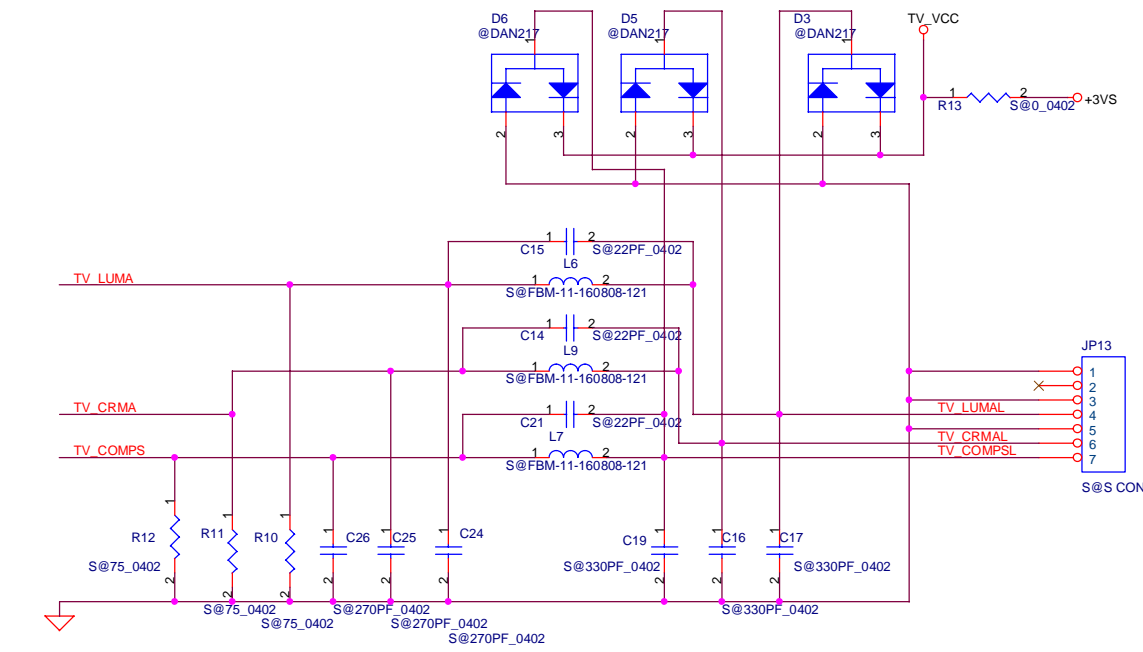
Size: Document Number 401224 Rev 0B

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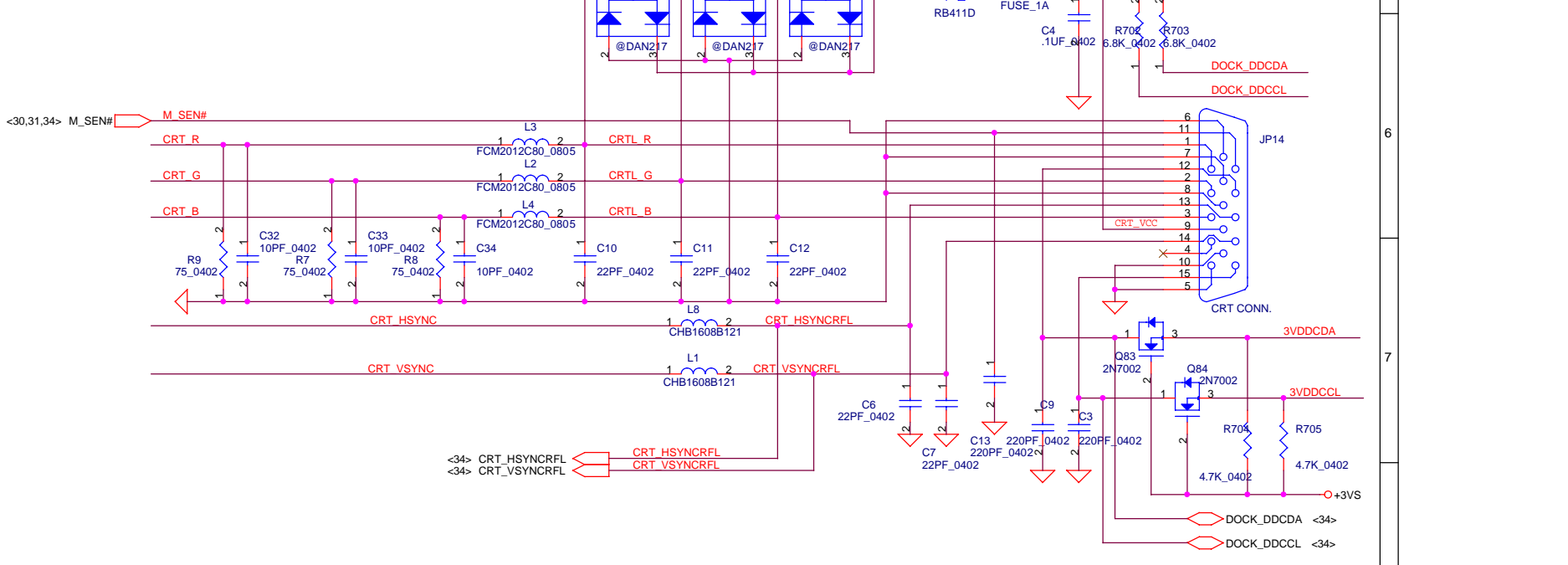
AGP 100X2 Pin connector



TV_OUT CONNECTOR

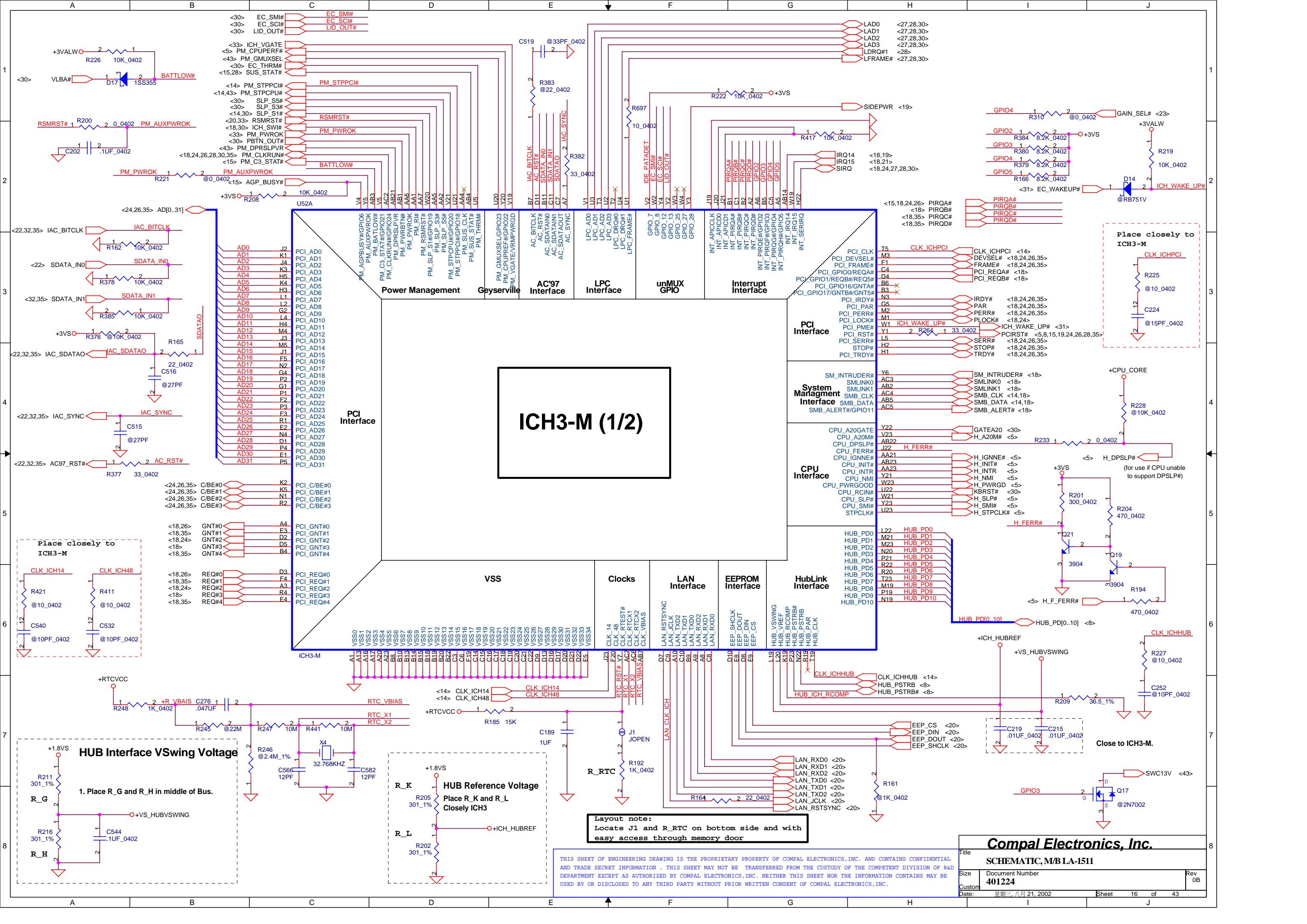


CRT CONNECTOR



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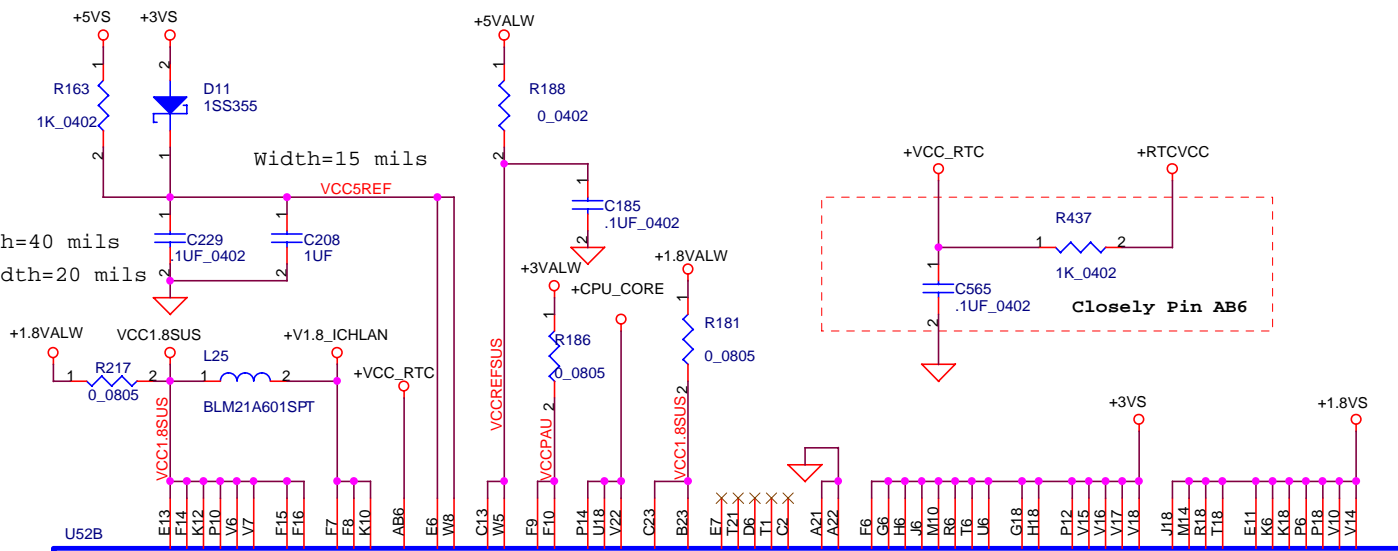
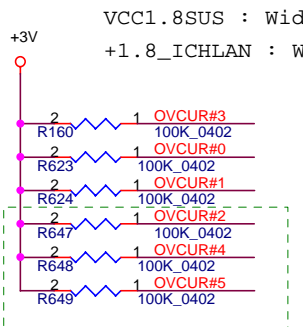
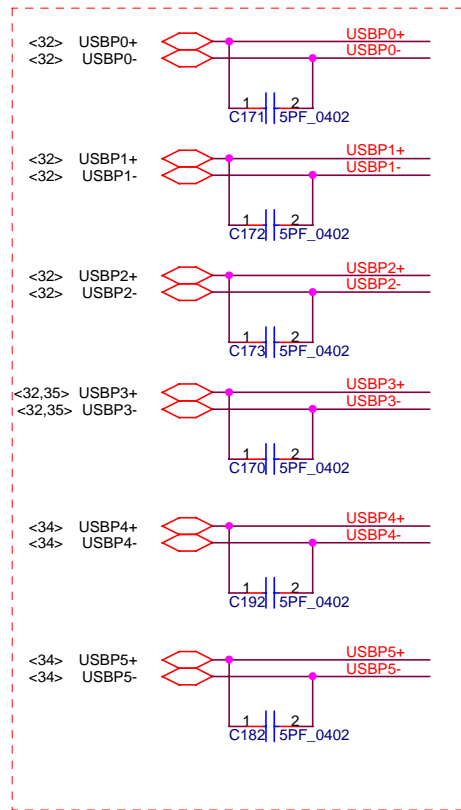


ICH3-M (1/2)

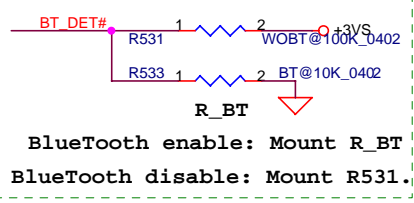
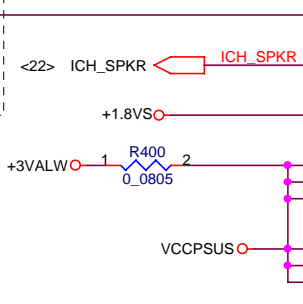
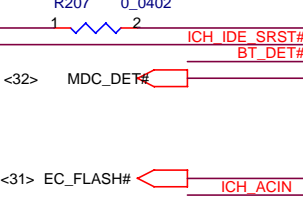
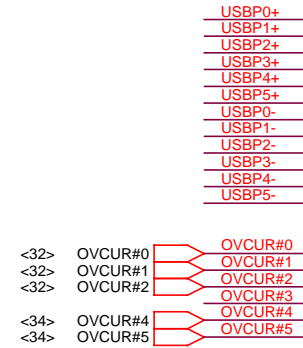
Layout note:
 Locate J1 and R_RTC on bottom side and with easy access through memory door

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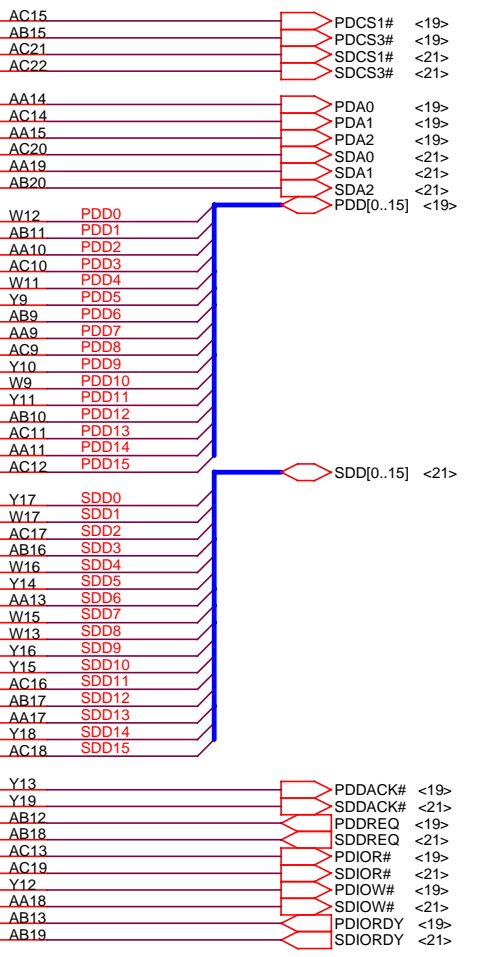
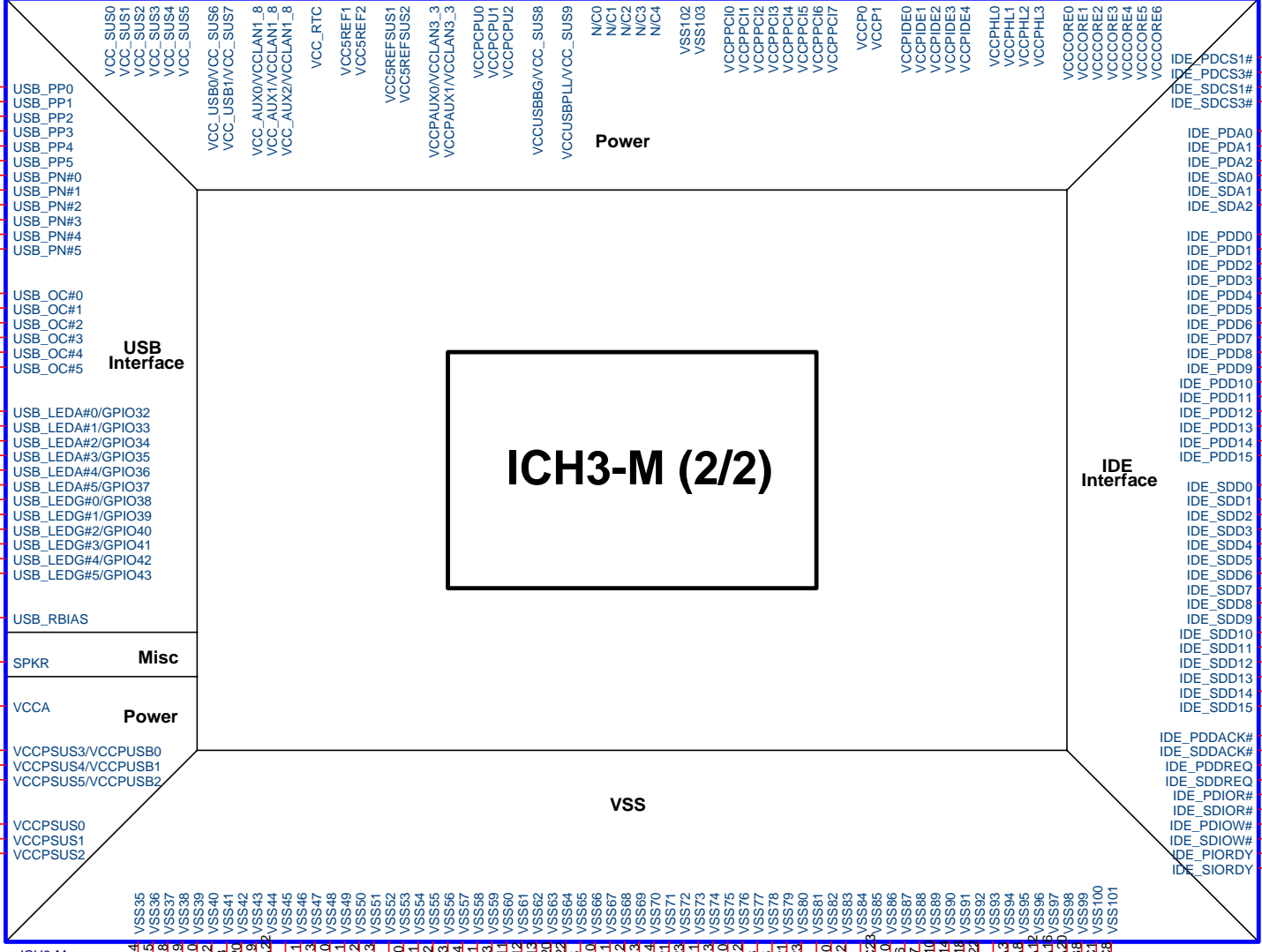
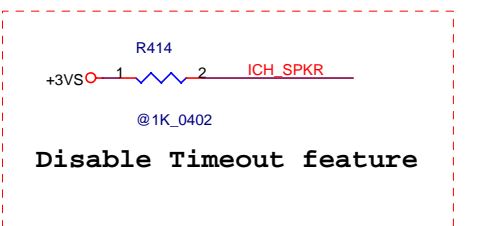
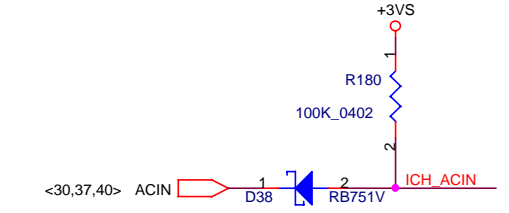


Layout note The Cap close to ICH3-M (< 1 inch)



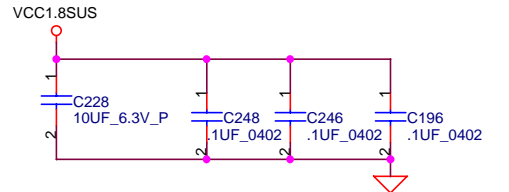
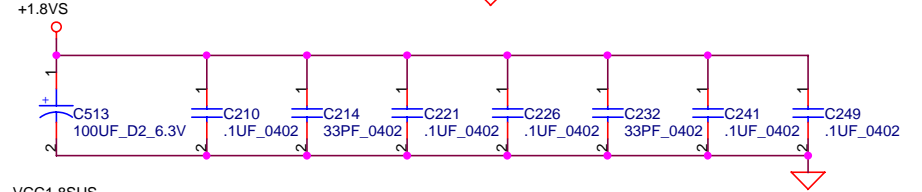
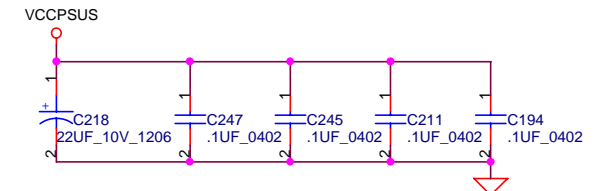
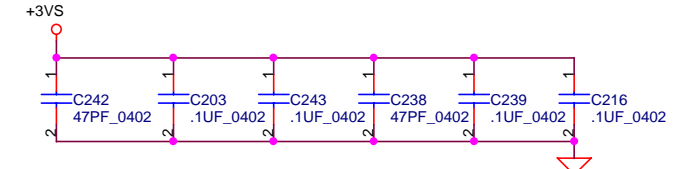
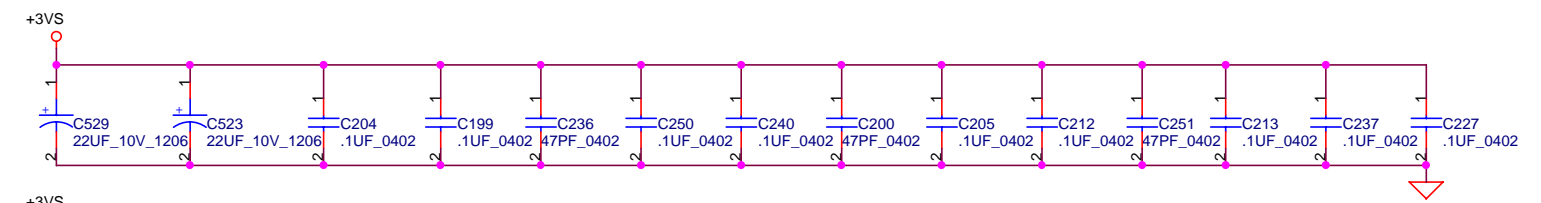
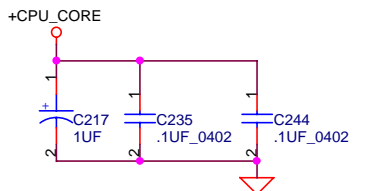
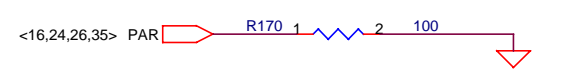
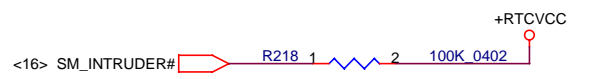
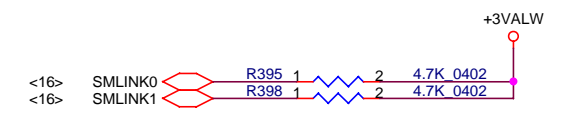
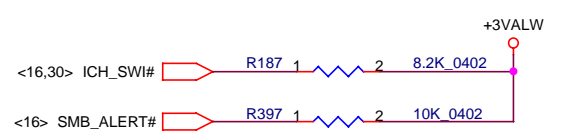
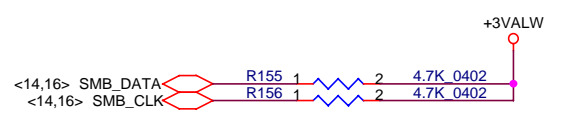
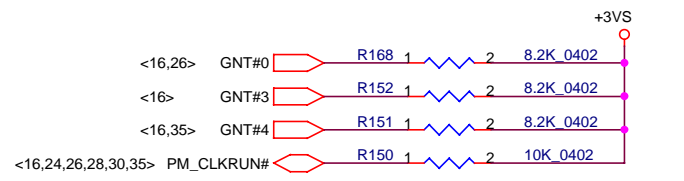
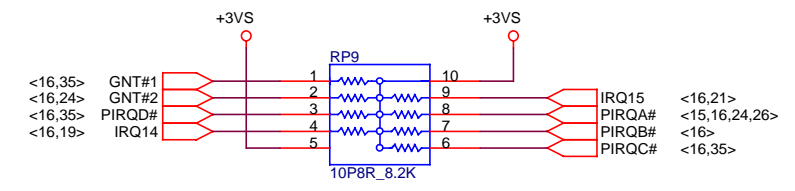
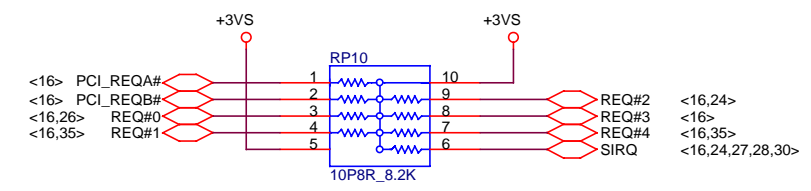
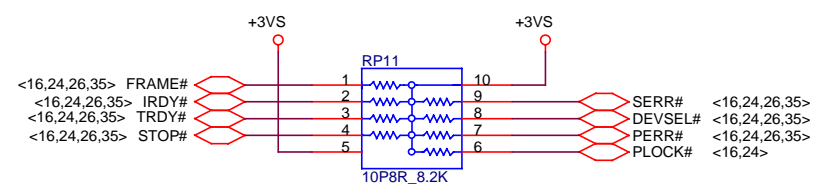
BlueTooth enable: Mount R_BT
BlueTooth disable: Mount R531.

Note:
R376=22.6_1% for B0(QB63 part)
R376=18.2_1% for B0(QB62 & SL5LF part)



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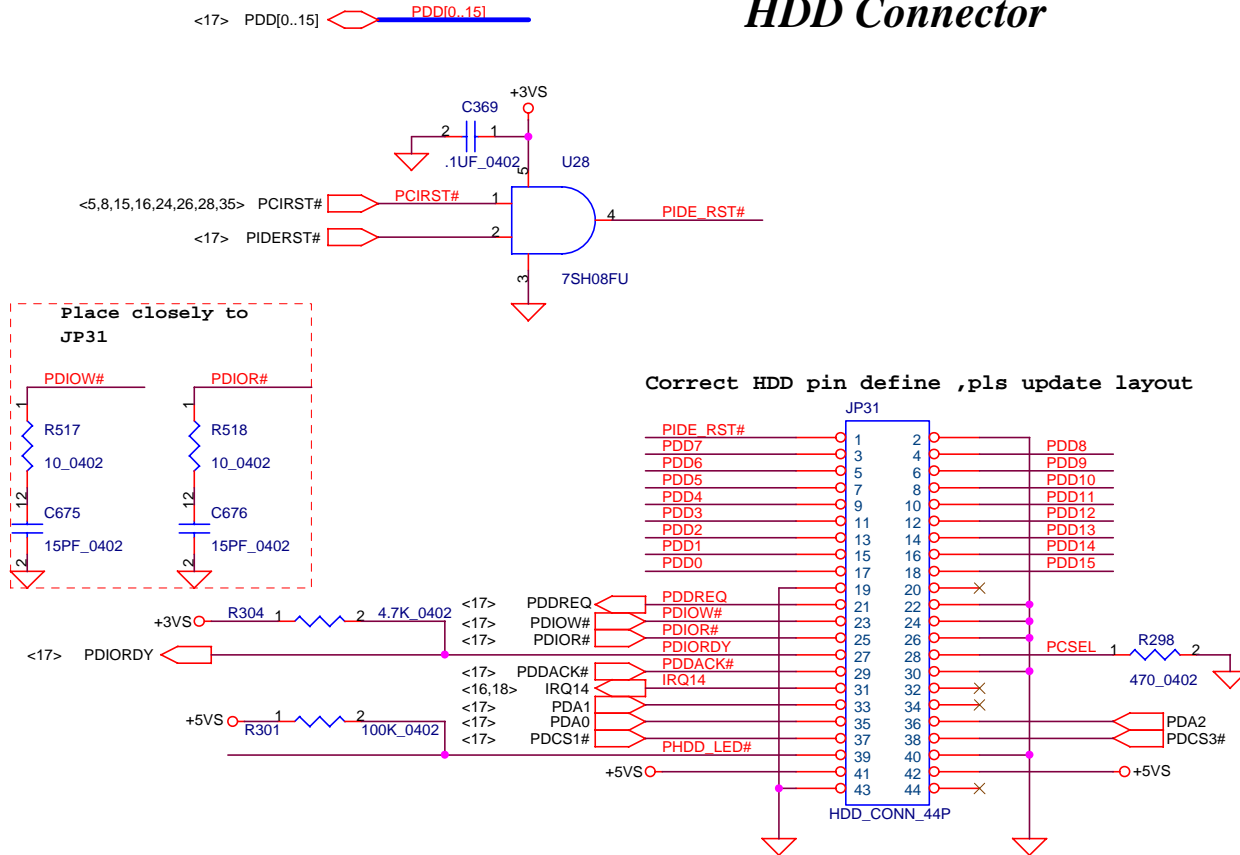
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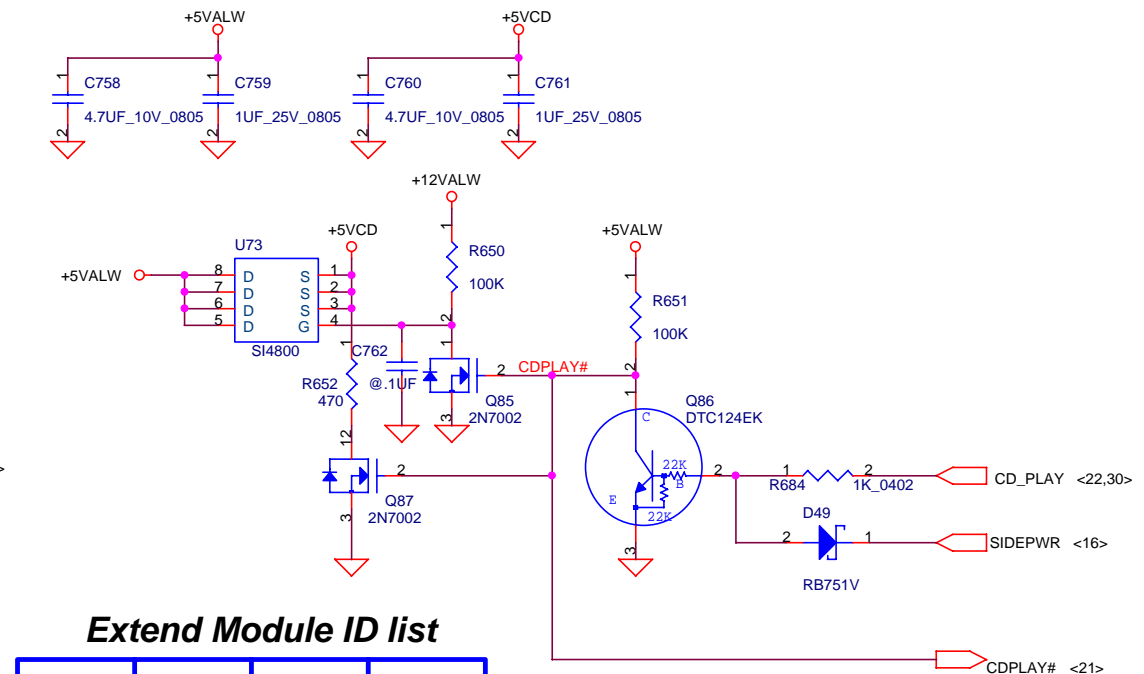
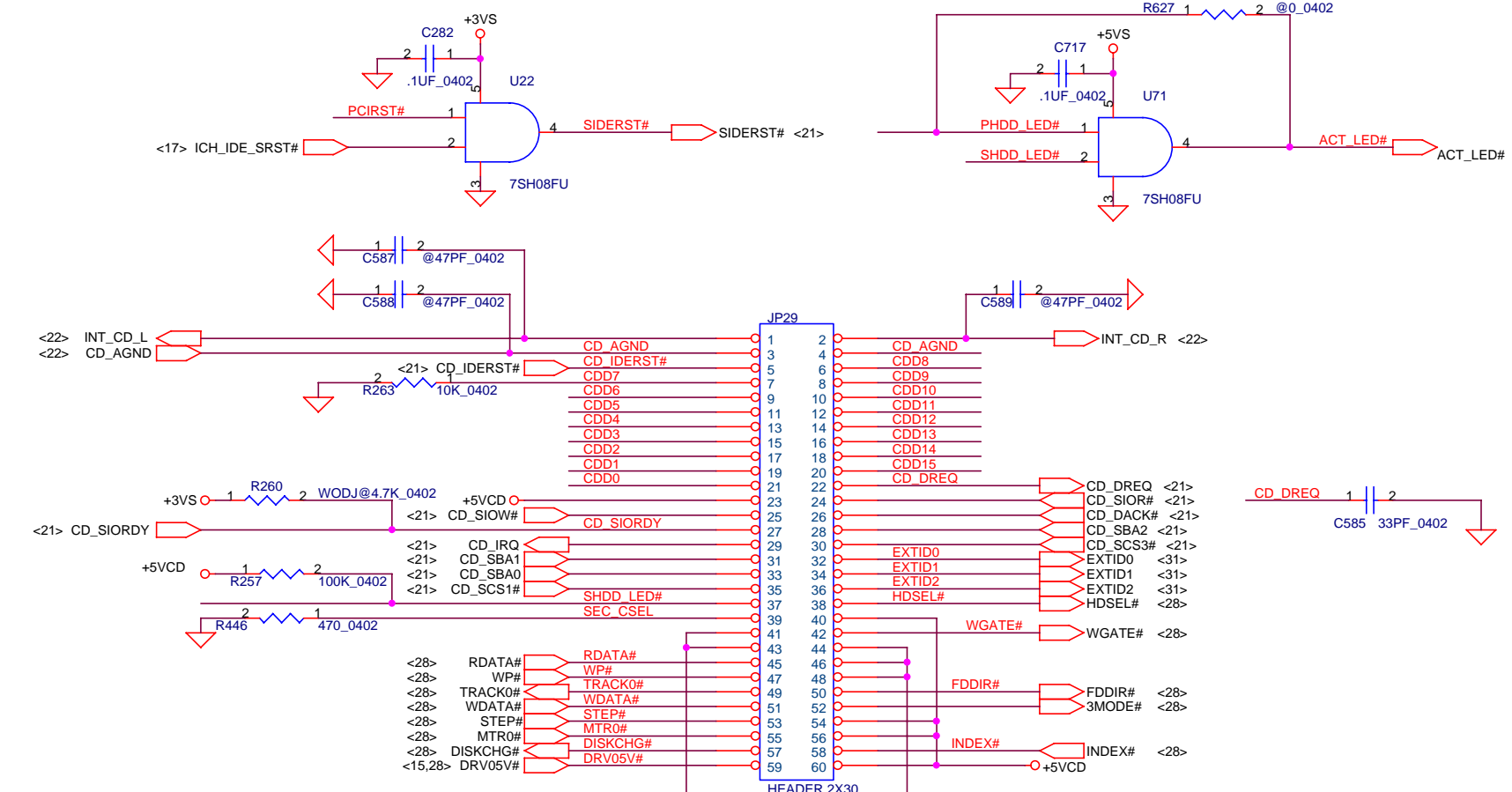
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HDD Connector

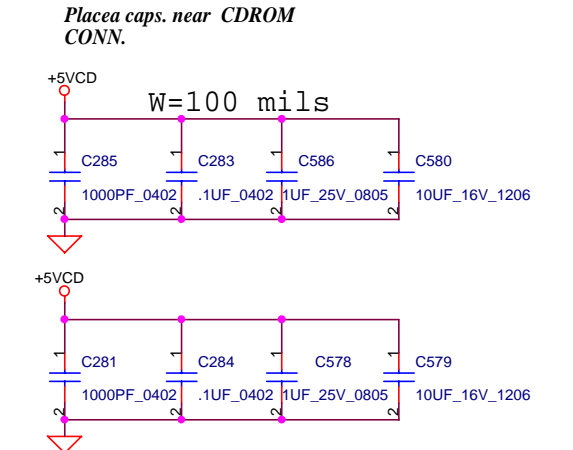


CD-ROM Connector



Extend Module ID list

DEVICE	EXTID2	EXTID1	EXTID0
FDD	0	0	0
CD-ROM	0	0	1
LS-120	0	1	0
2'nd HDD	0	1	1
NONE	1	1	1



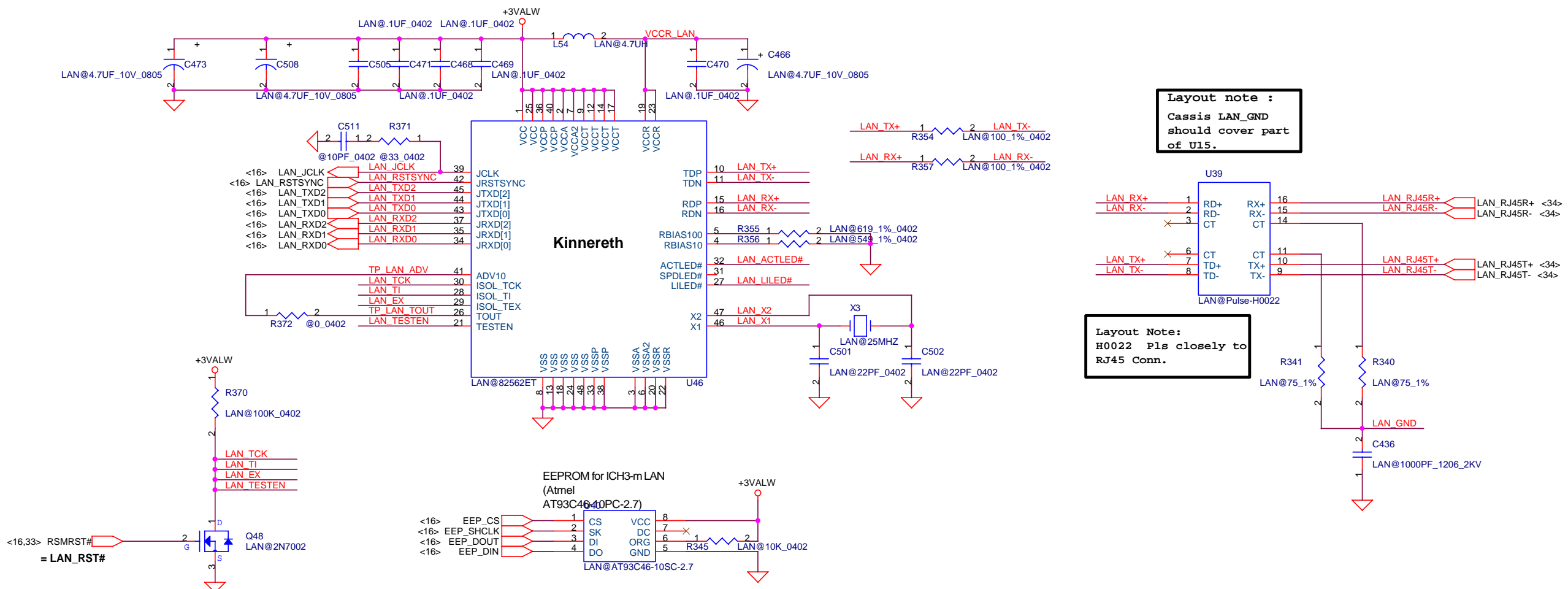
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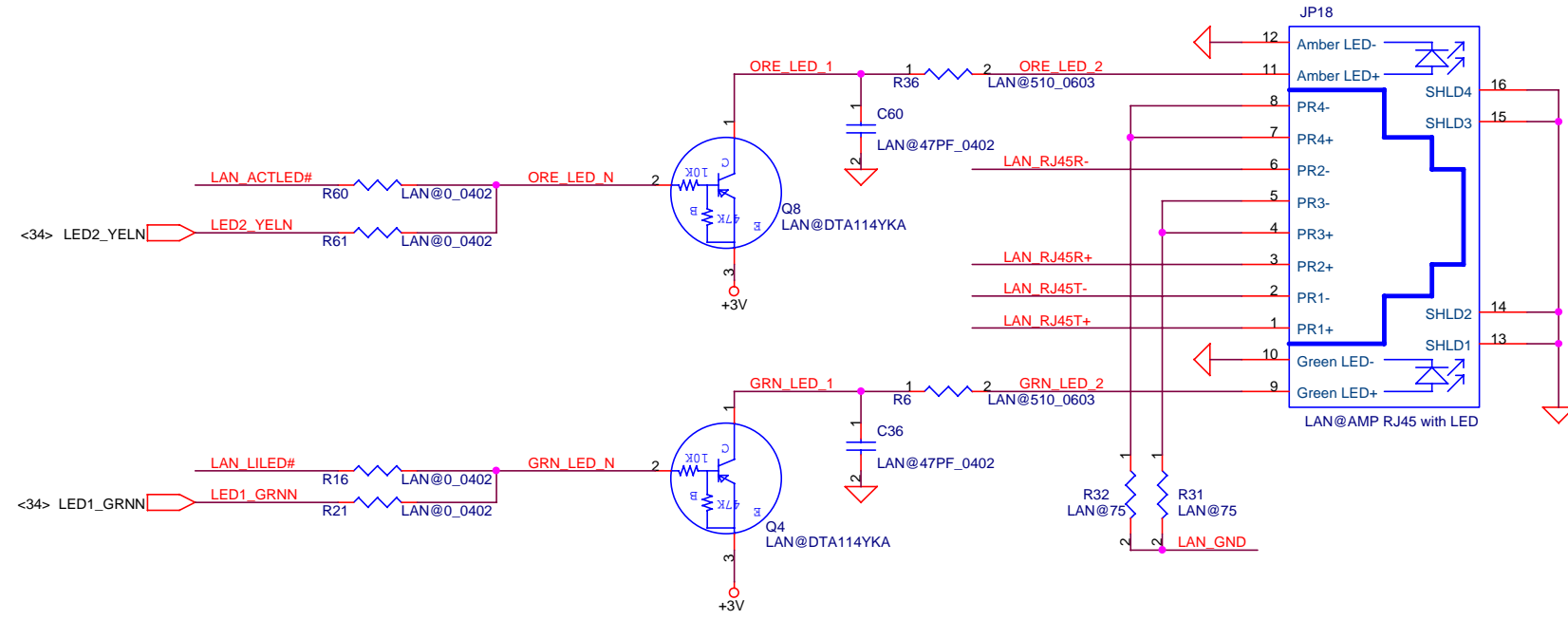
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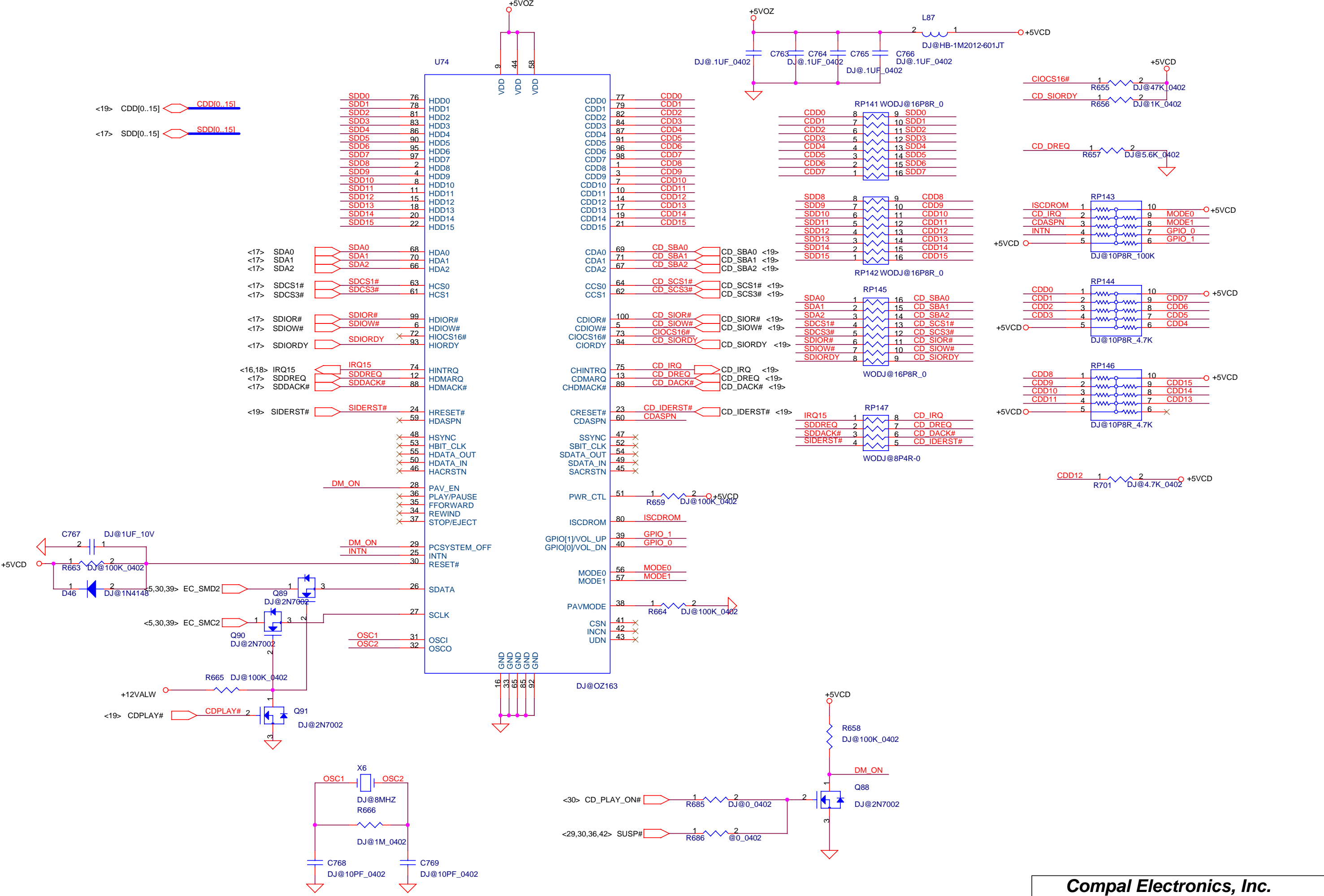
Layout note :
Cassis LAN_GND should cover part of U15.

Layout Note:
H0022 Pls closely to RJ45 Conn.



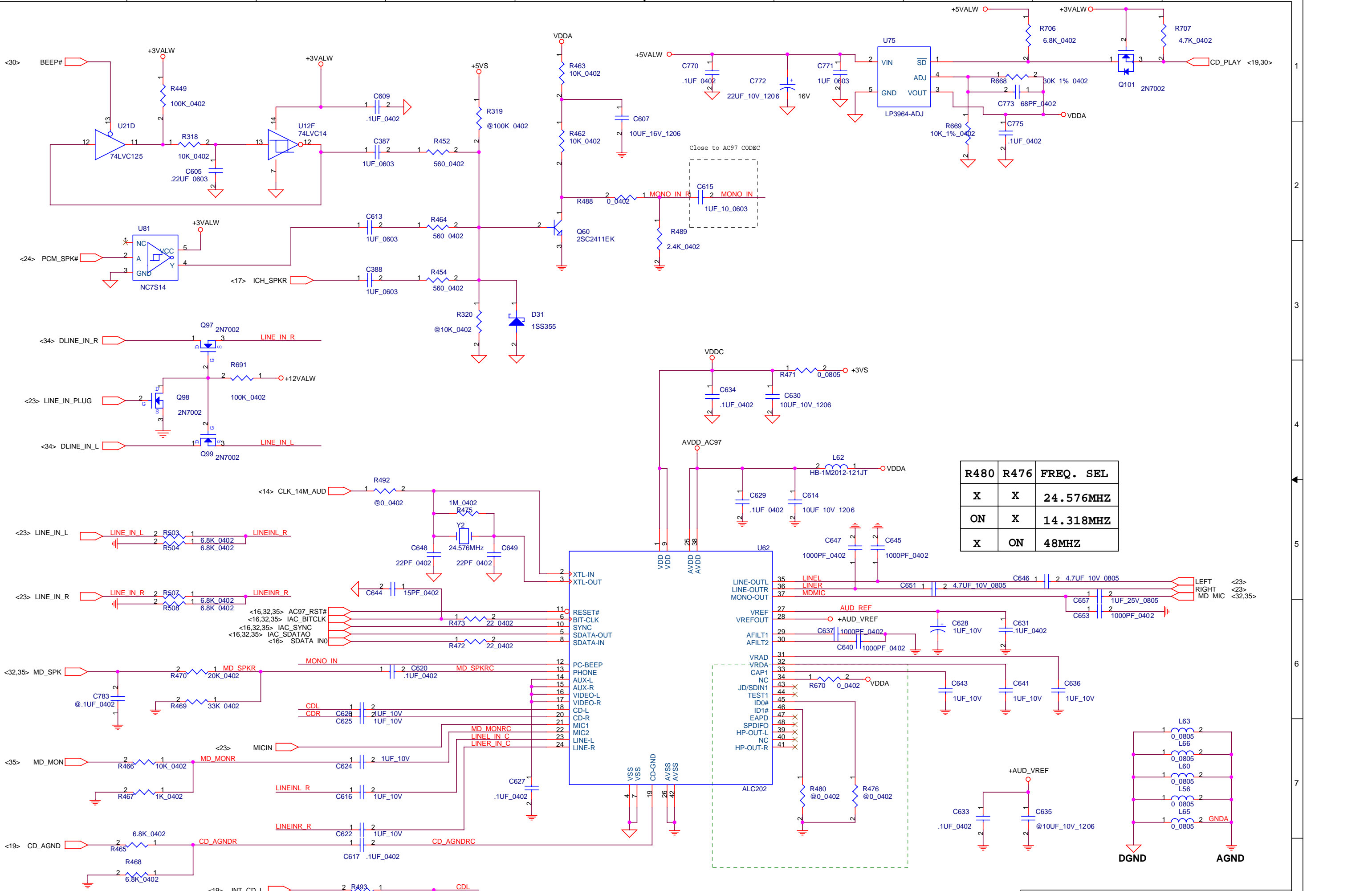
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R480	R476	FREQ. SEL
X	X	24.576MHZ
ON	X	14.318MHZ
X	ON	48MHZ

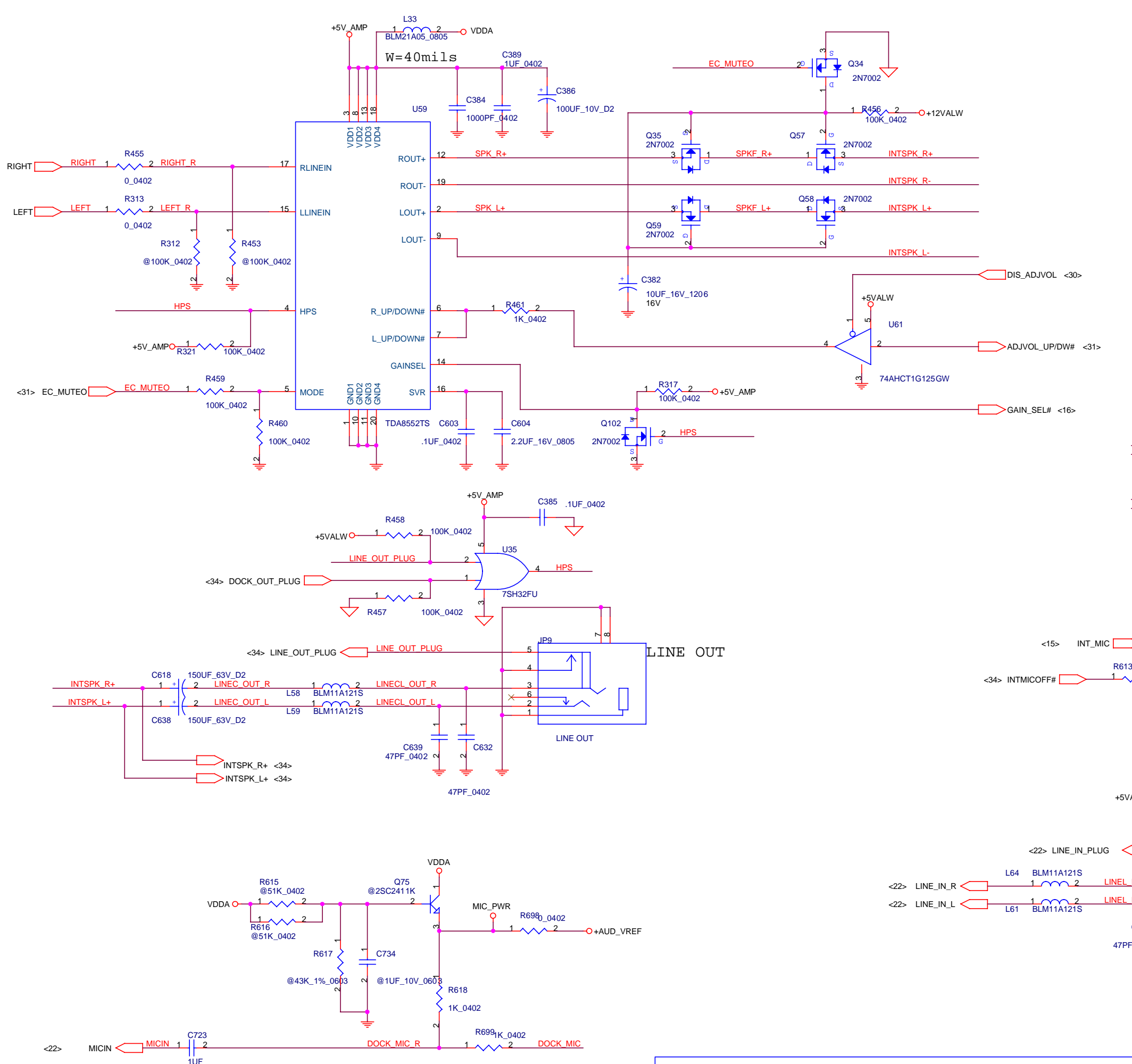
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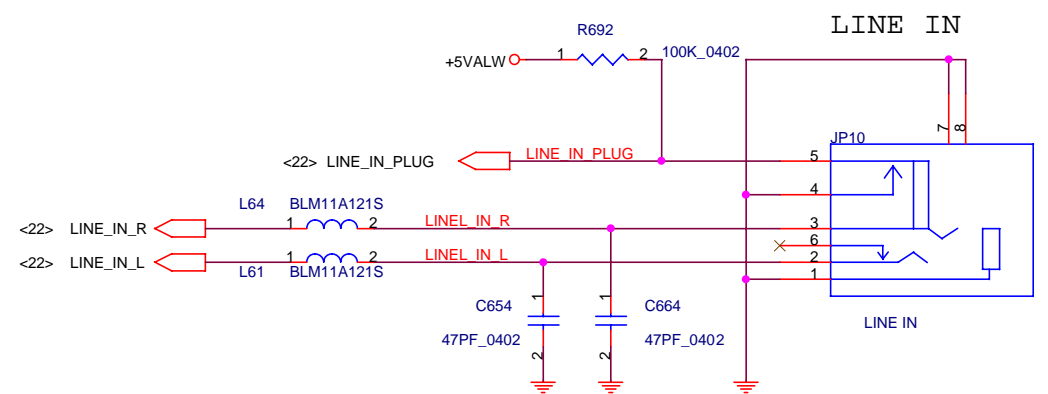
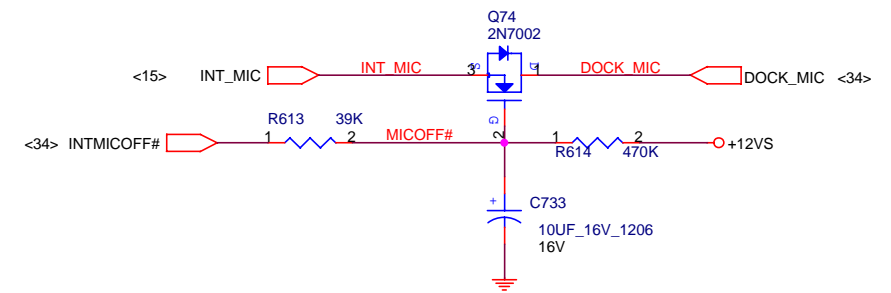
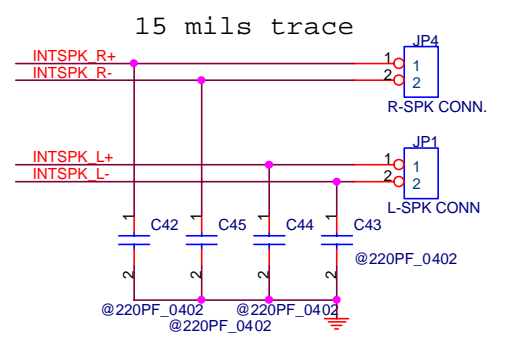
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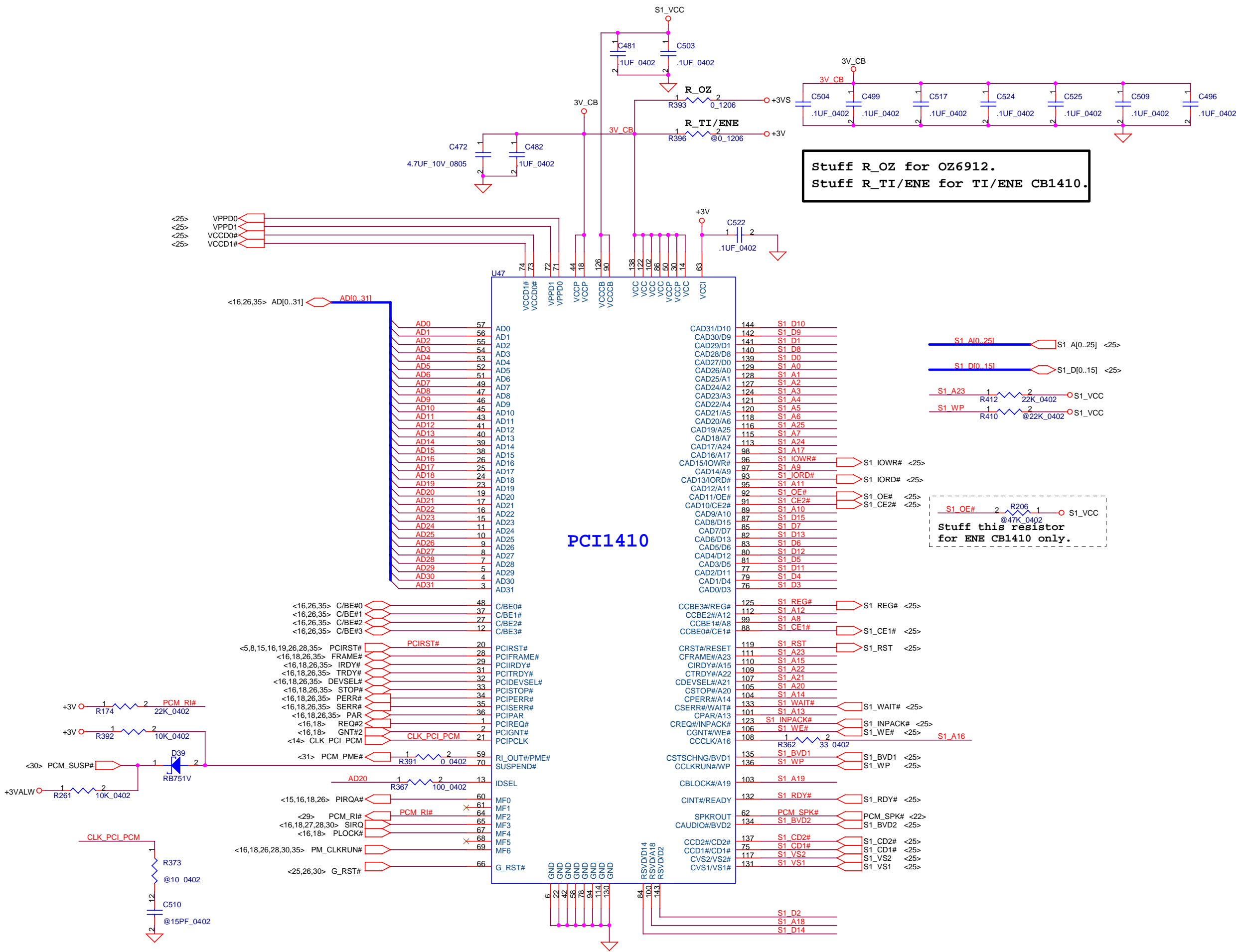
Layout note:

- Trace width=15 mils.
- 1.SPKF_R+,SPKF_L+,SPKF_R+,SPKF_L+
- 2.INTSPK_R+/- ,INTSPK_L+/-
- 3.LINEOUT_L,LINEOUT_R



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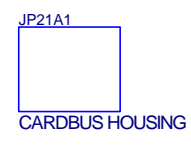
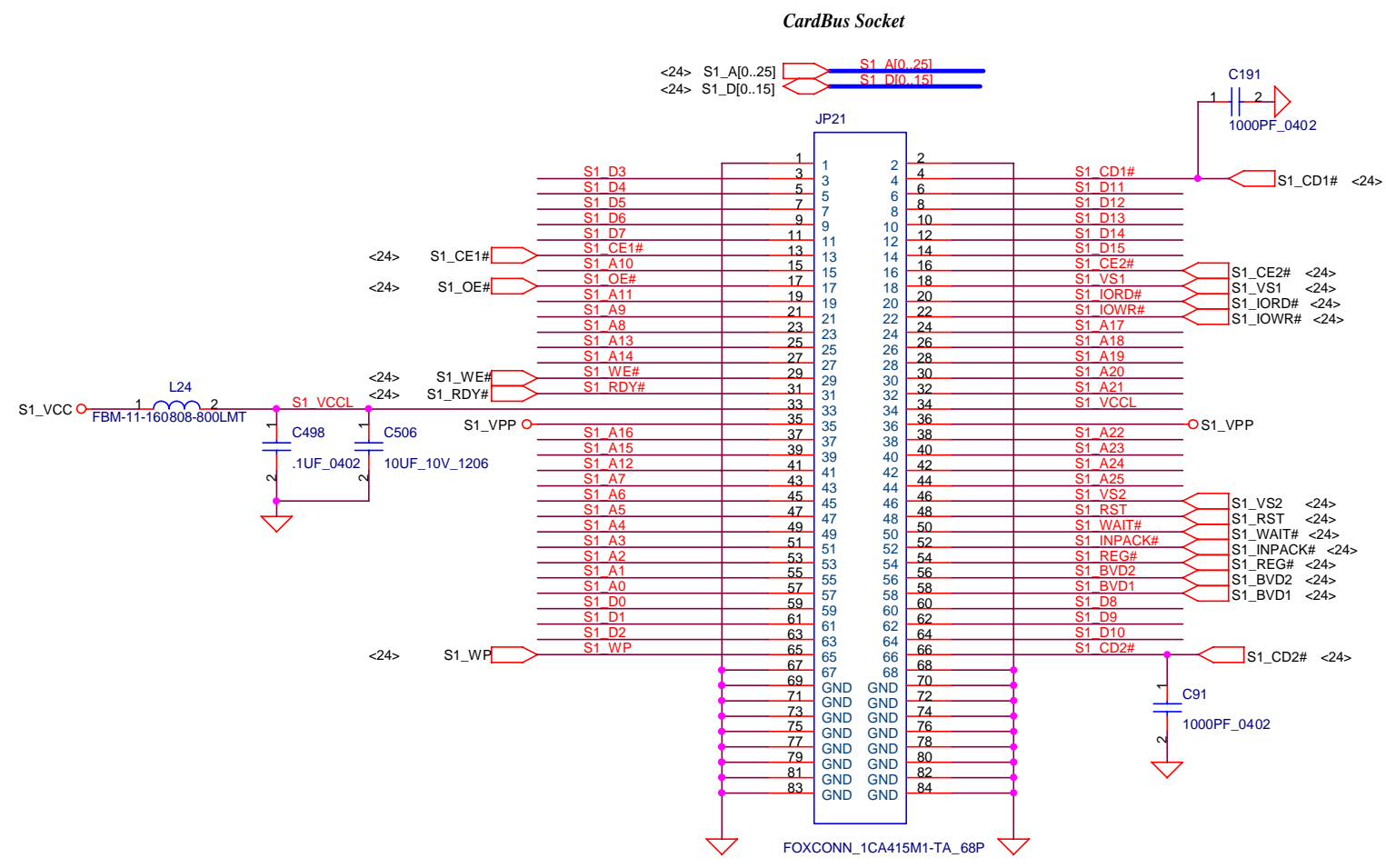
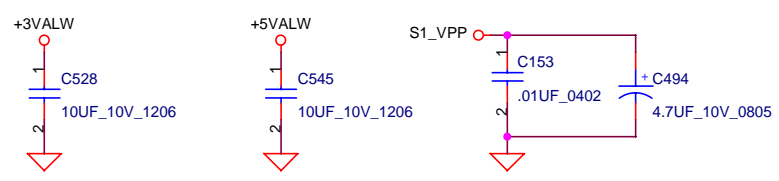
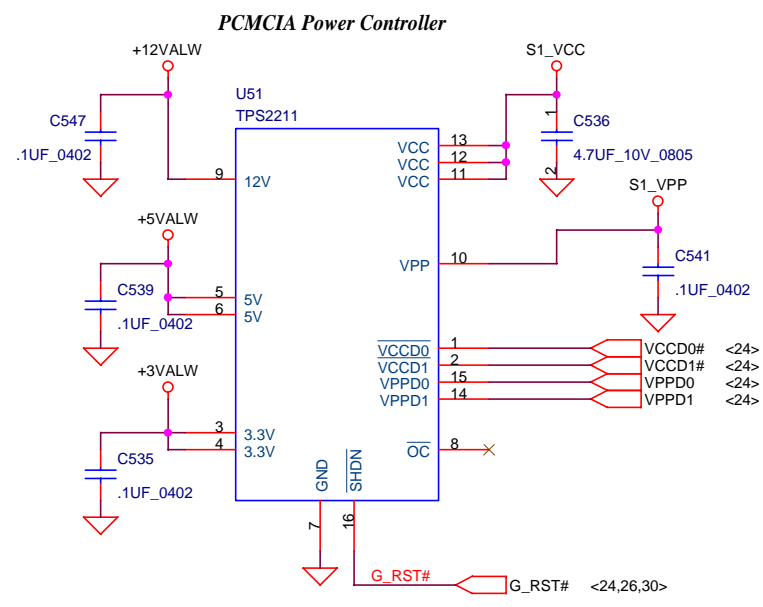


Stuff R_OZ for OZ6912.
 Stuff R_TI/ENE for TI/ENE CB1410.

S1_A[0..25] <25>
 S1_D[0..15] <25>
 S1_A23 R412 22K_0402 S1_VCC
 S1_WP R410 @22K_0402 S1_VCC
 S1_OE# R206 @47K_0402 S1_VCC
 Stuff this resistor for ENE CB1410 only.

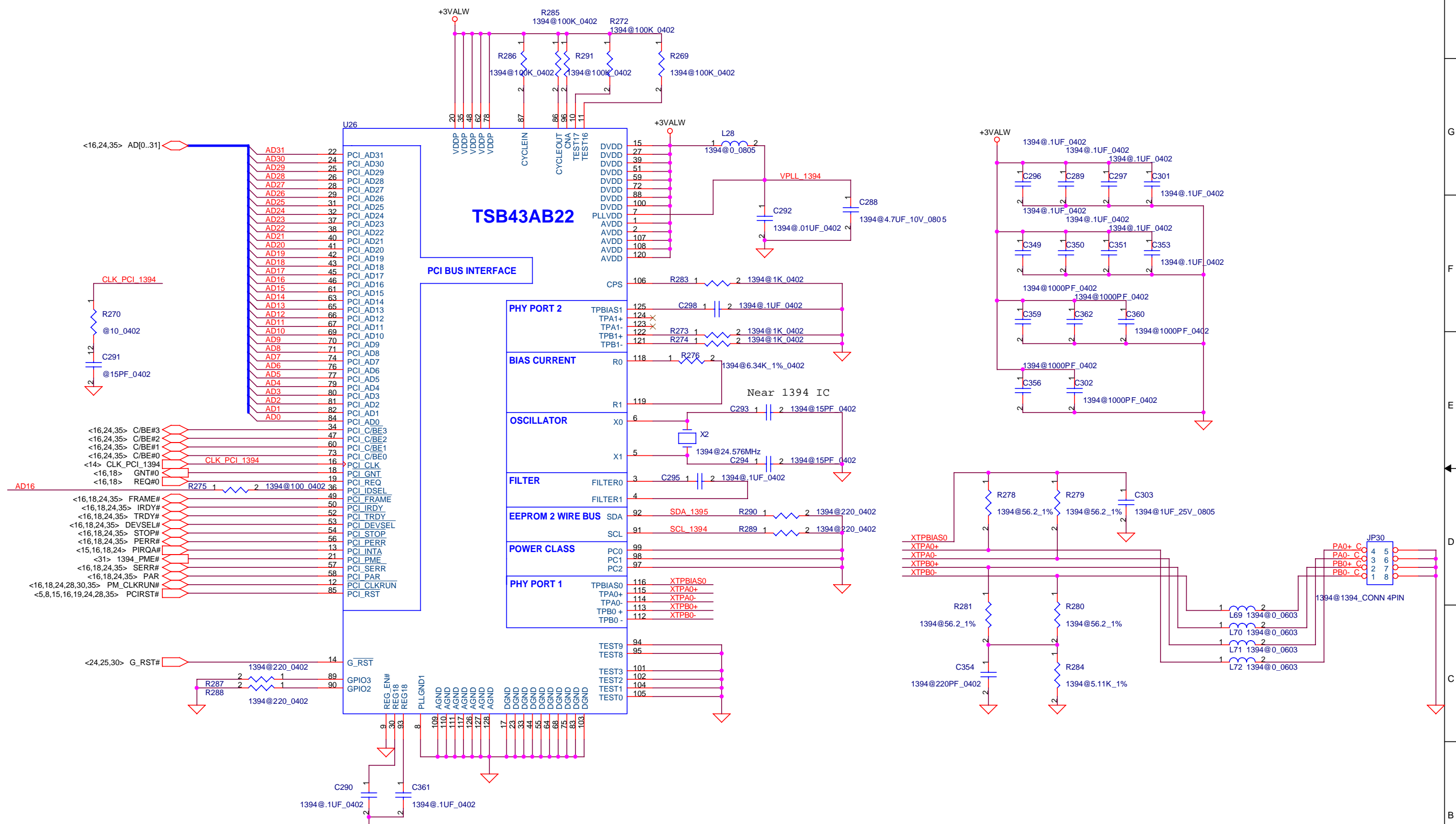
PCI1410

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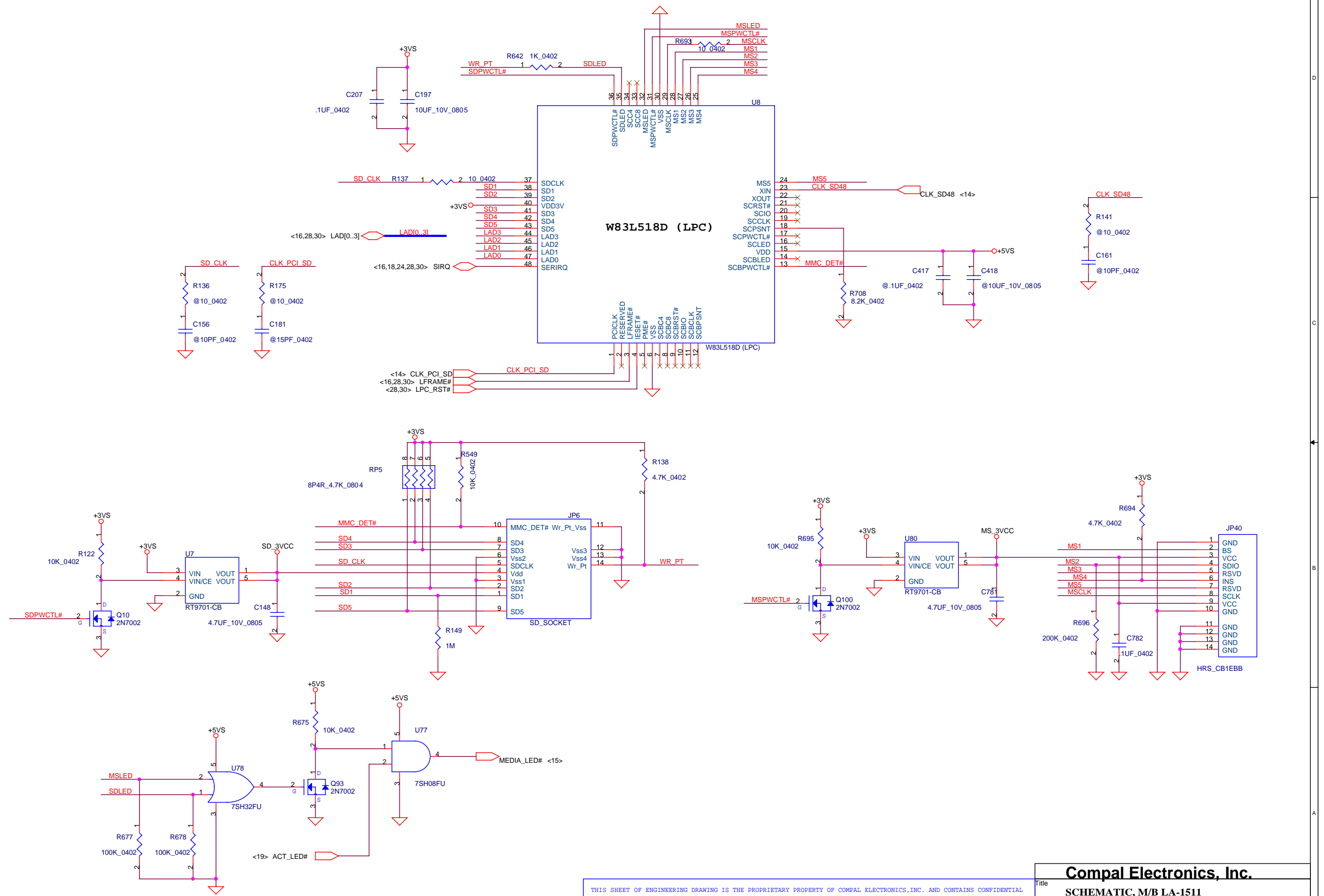


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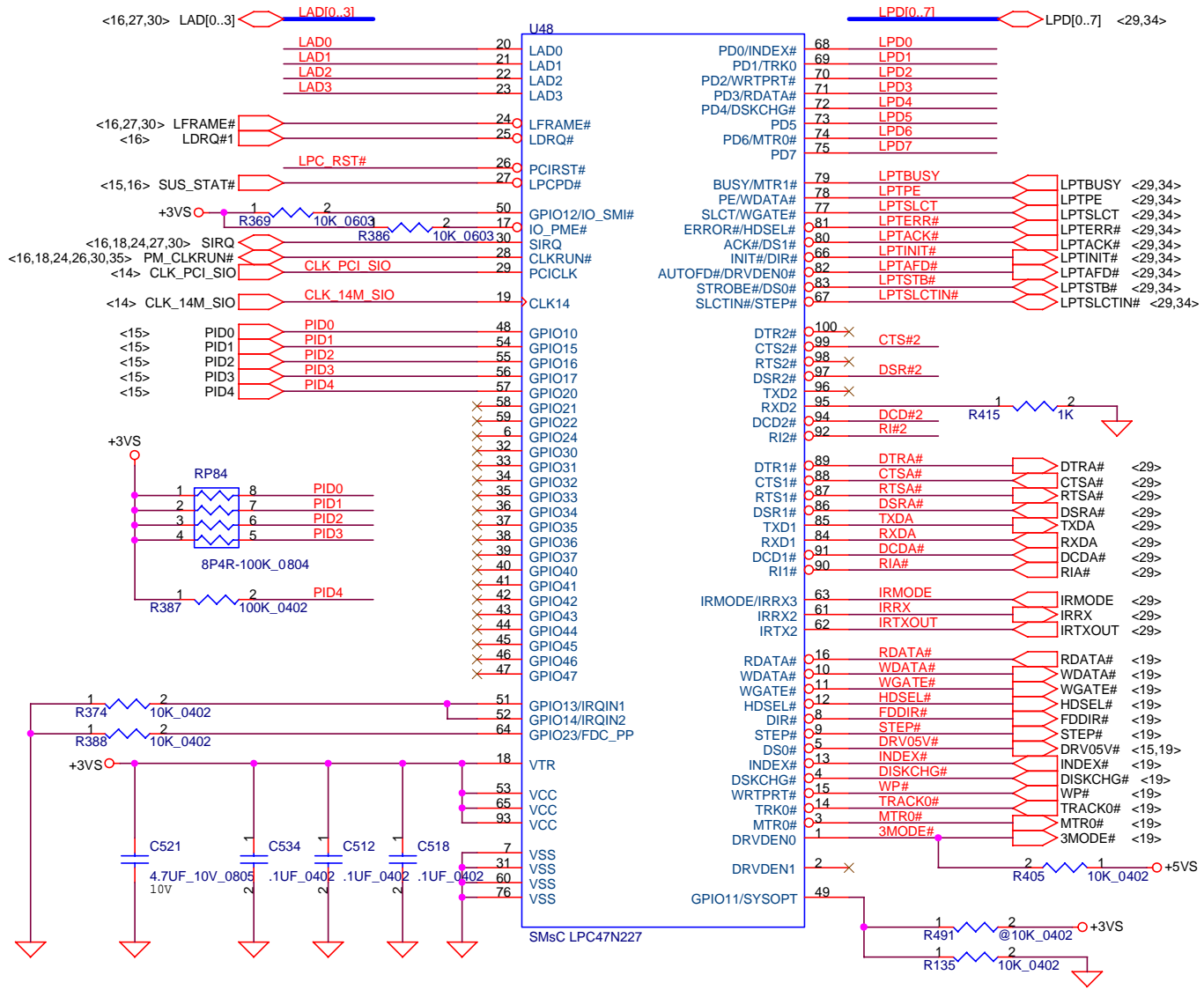
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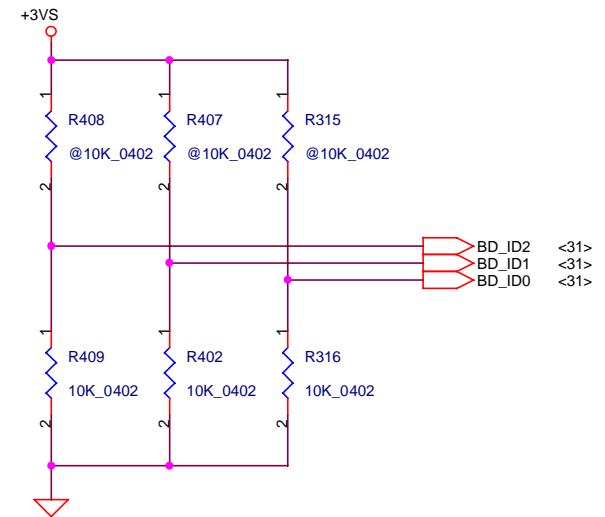
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SUPER I/O SMC FDC47N227

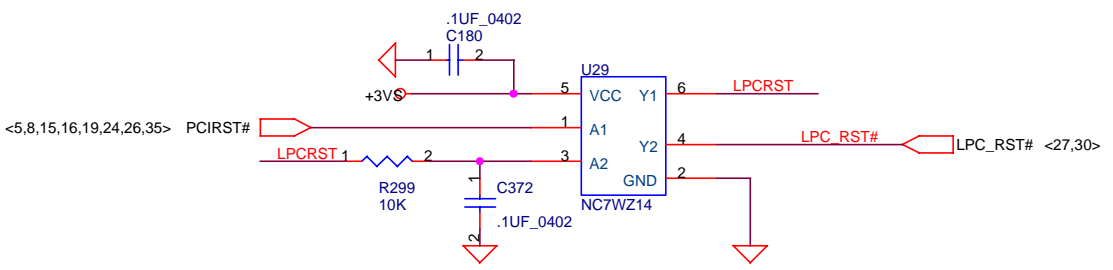
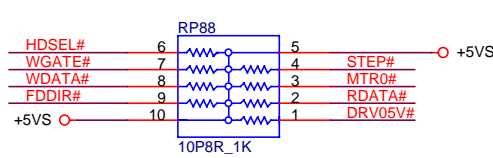
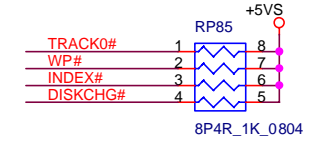
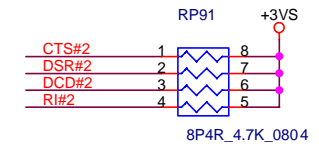


Base I/O Address
 0 = 02Eh
 * 1 = 04Eh

BOARD ID



	BD_ID2	BD_ID1	BD_ID0
SST	0	0	0
PT	0	0	1
ST	0	1	0
QT	0	1	1



Compal Electronics, Inc.

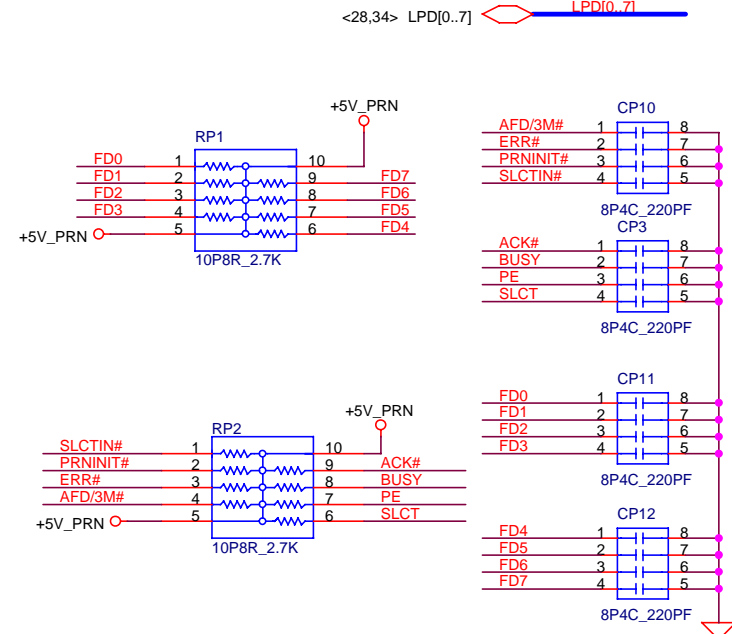
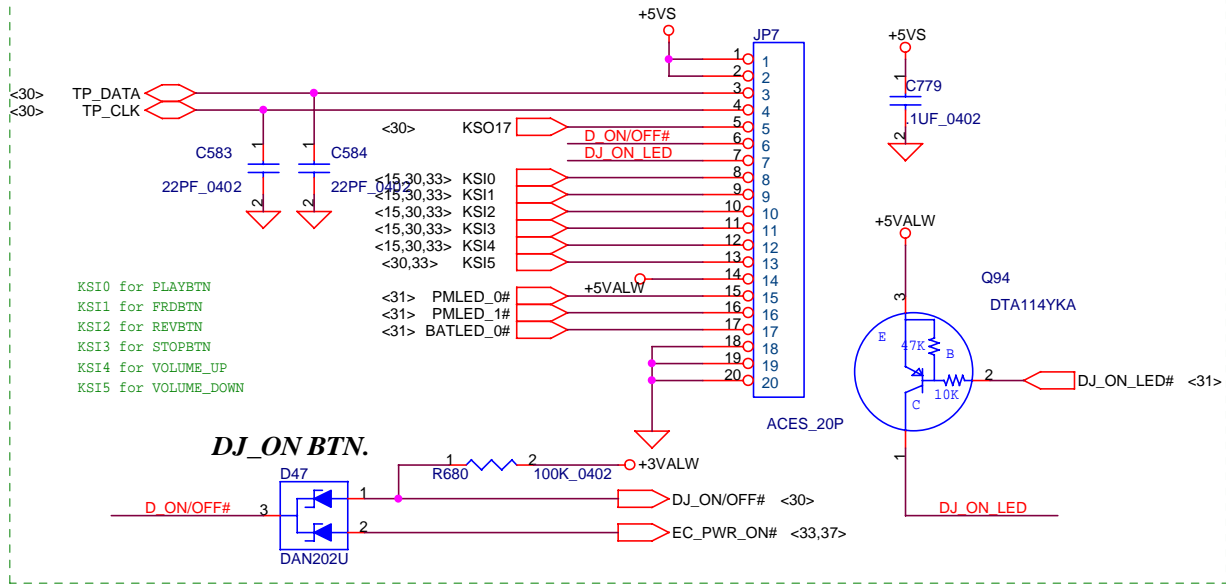
Title: SCHEMATIC, M/B LA-1511

Size: Document Number 401224

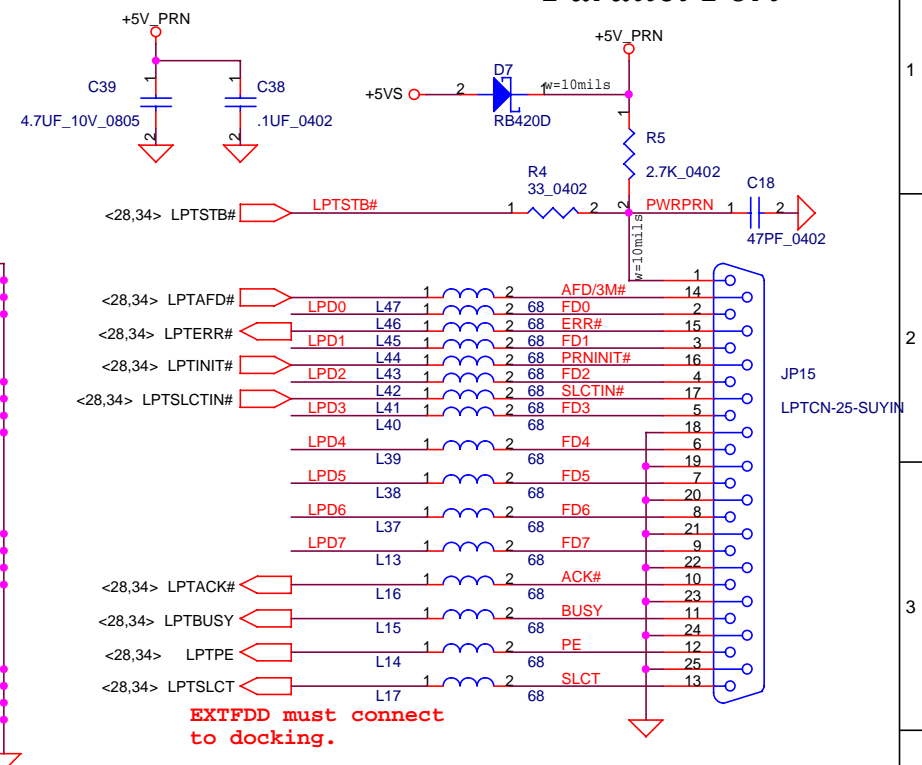
Rev: 0B

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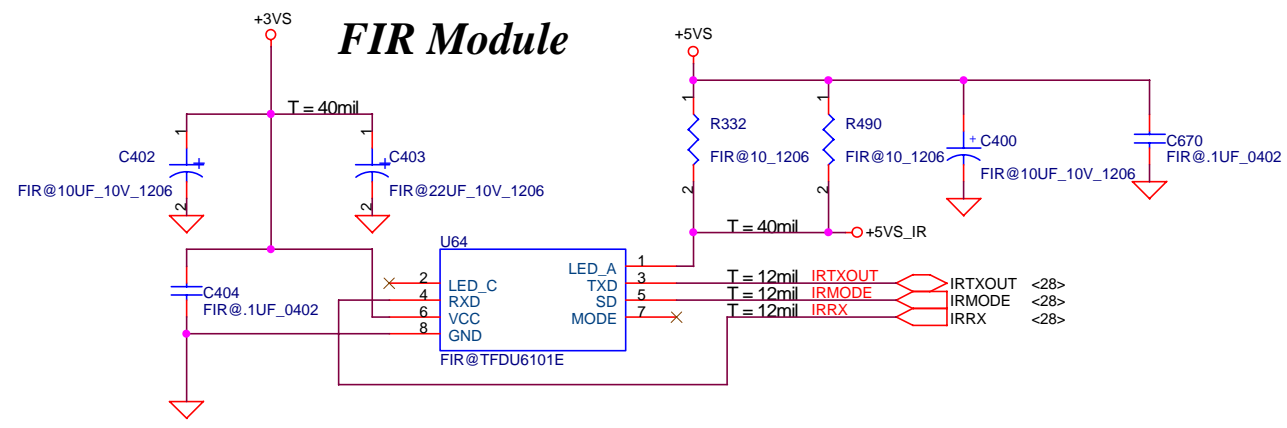
Touch Pad & Status LED Conn.



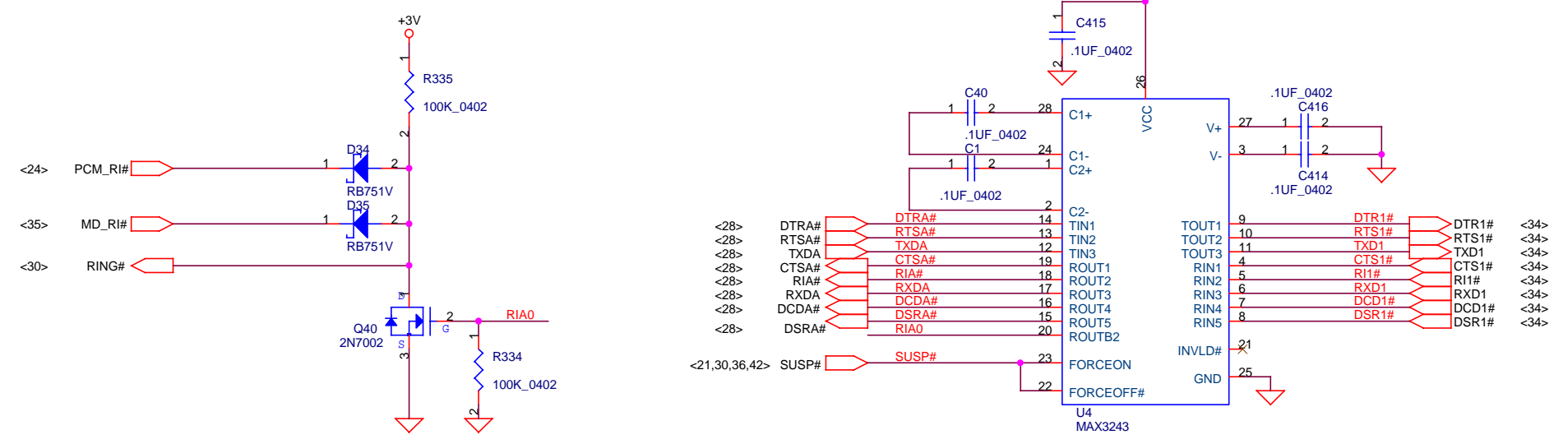
Parallel Port



FIR Module

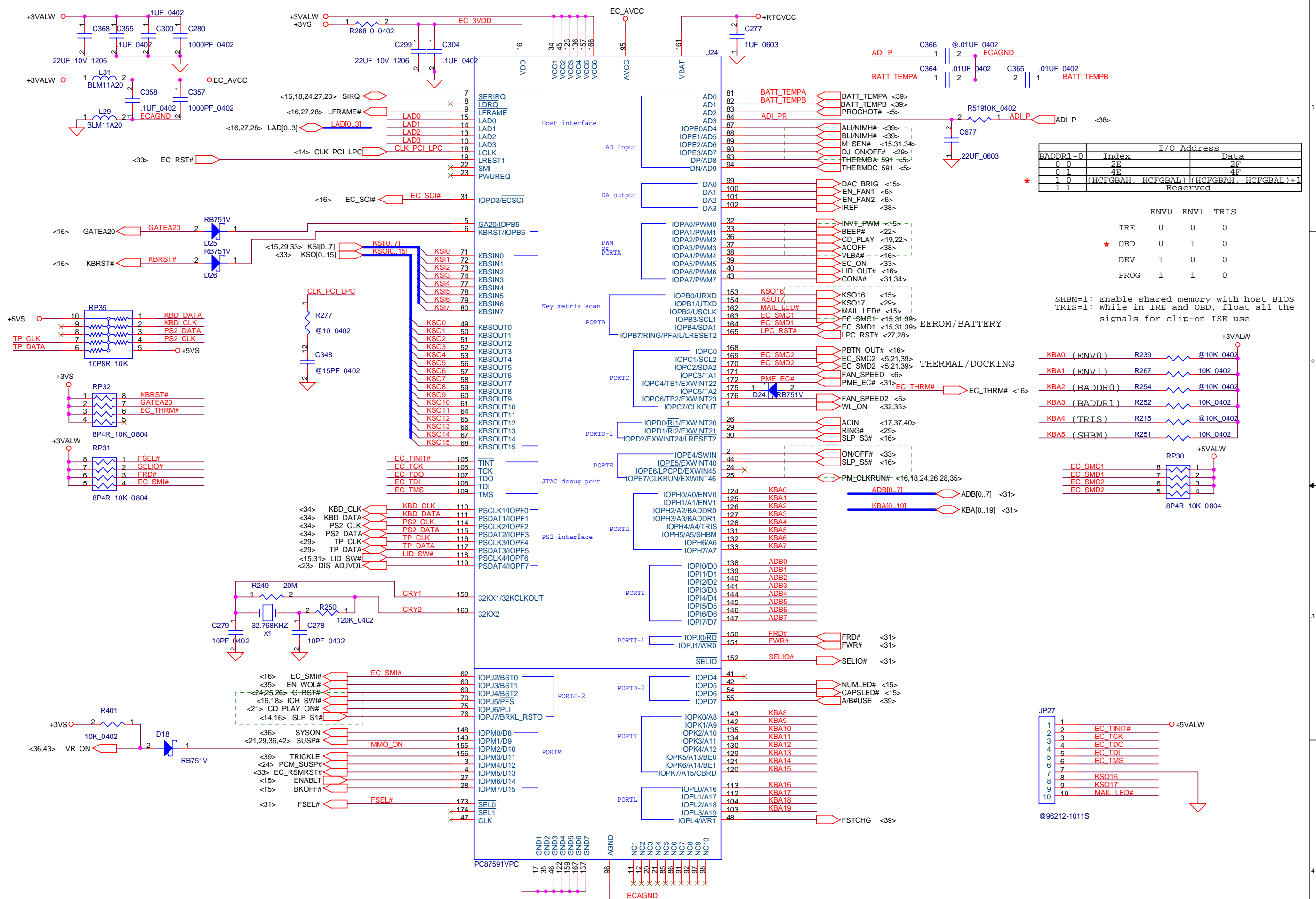


Serial Port



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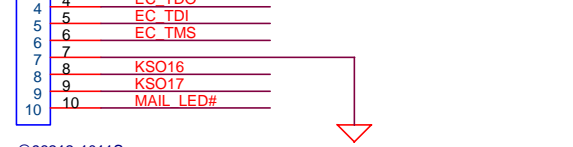
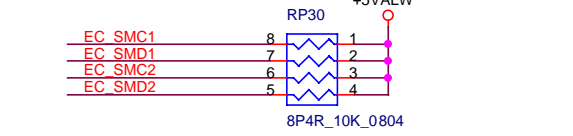
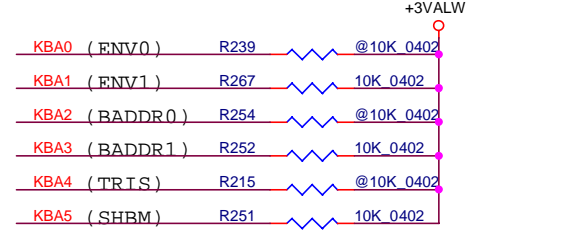
Compal Electronics, Inc.		
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I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL) (HCFGBAH, HCFGBAL)+1	
1 1	Reserved	

	ENV0	ENV1	TRIS
IRE	0	0	0
* OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

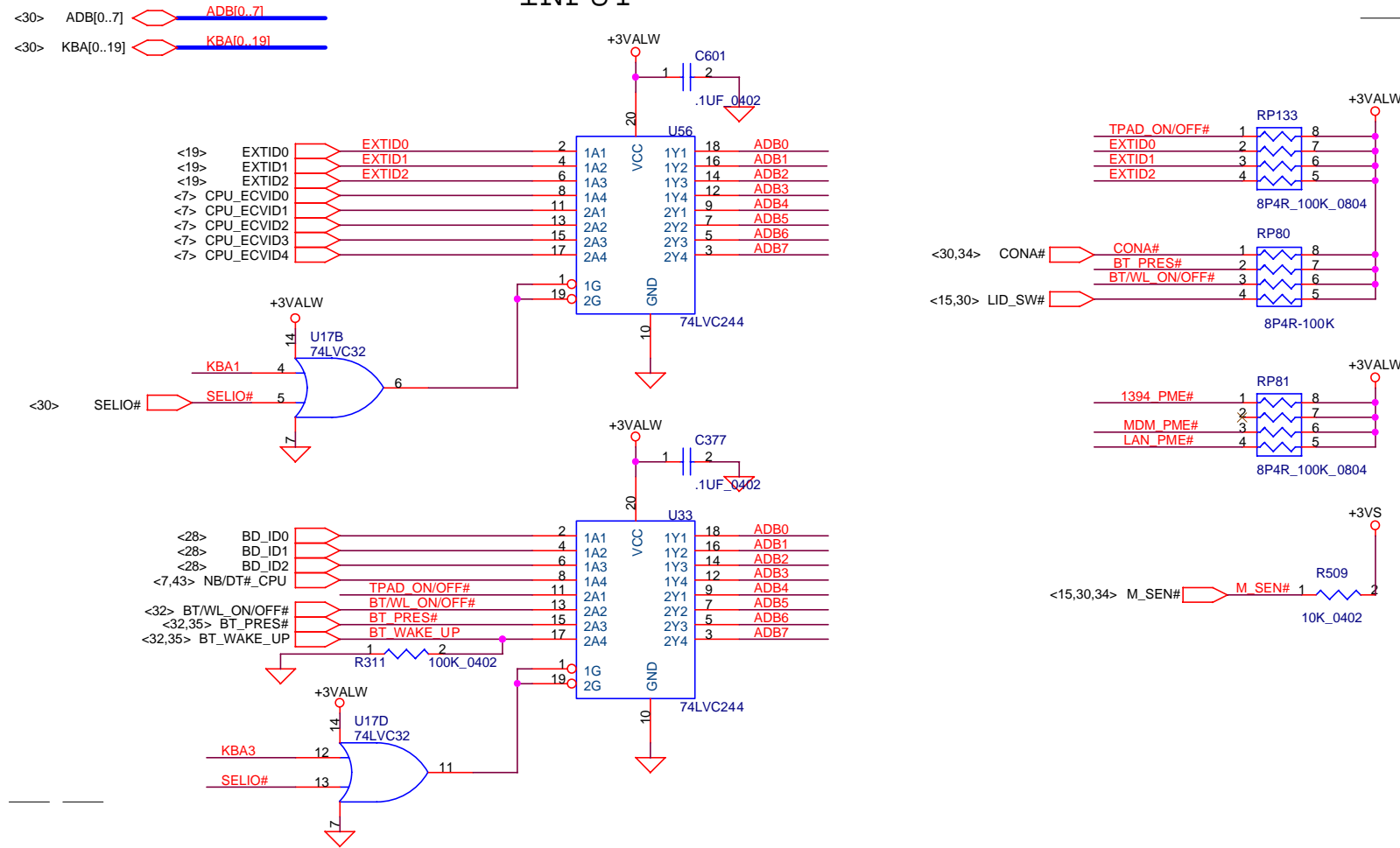
SHBM=1: Enable shared memory with host BIOS
 TRIS=1: While in IRE and OBD, float all the signals for clip-on ISE use



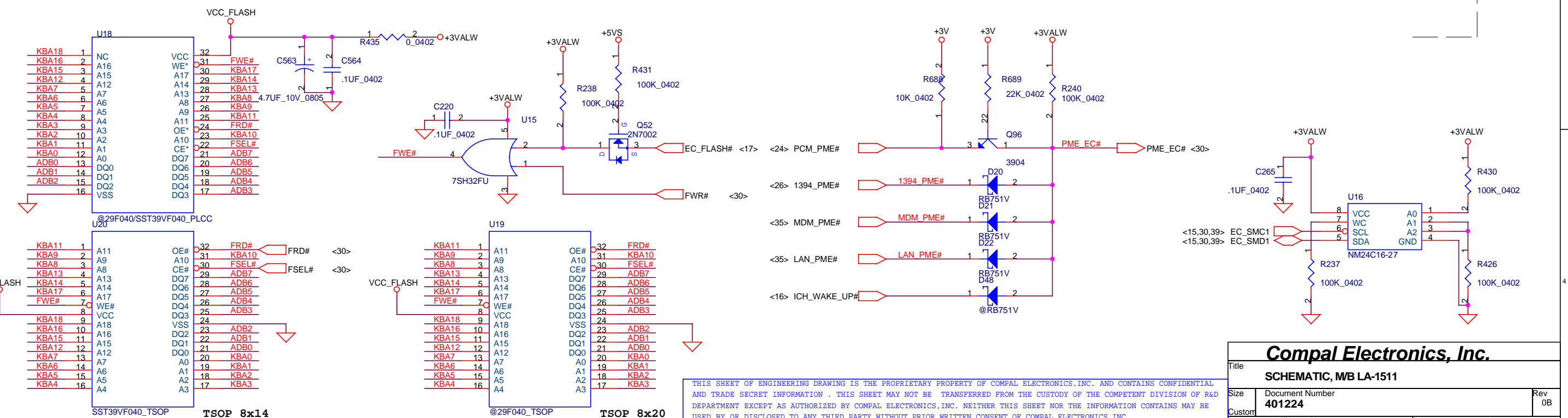
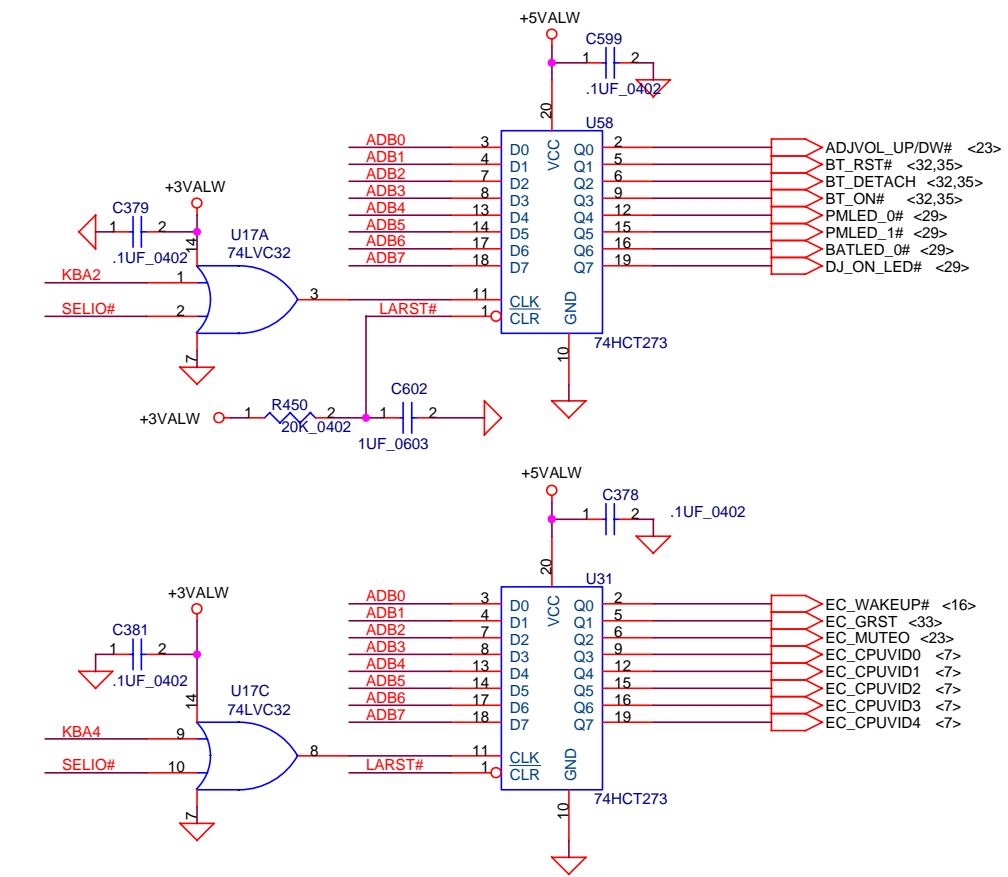
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Schematic, M/B LA-1511		
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INPUT



OUTPUT

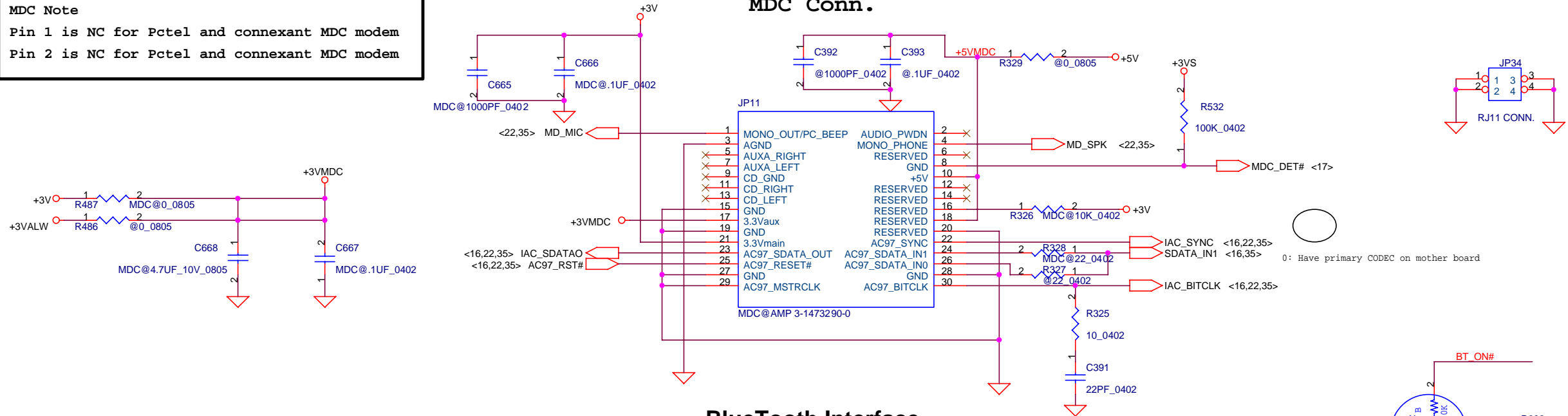


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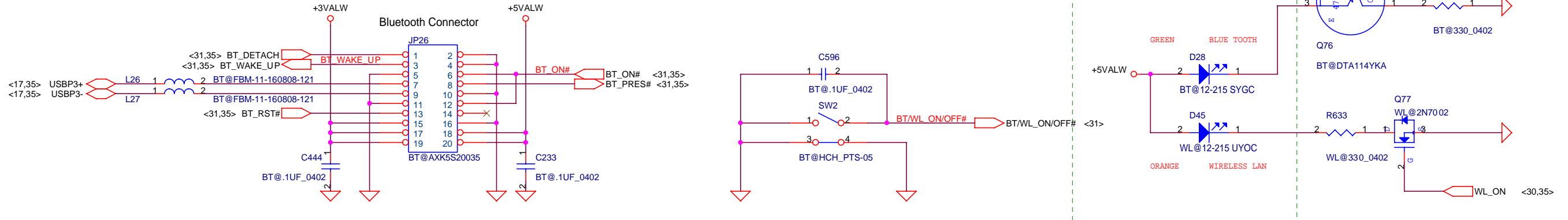
Compal Electronics, Inc.		
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MDC Note
 Pin 1 is NC for Pctel and connexant MDC modem
 Pin 2 is NC for Pctel and connexant MDC modem

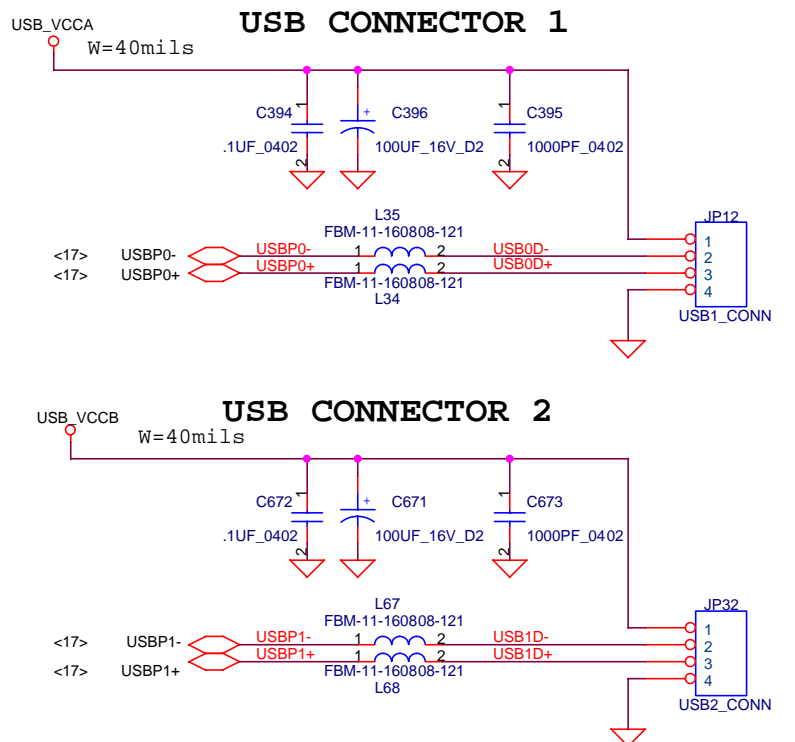
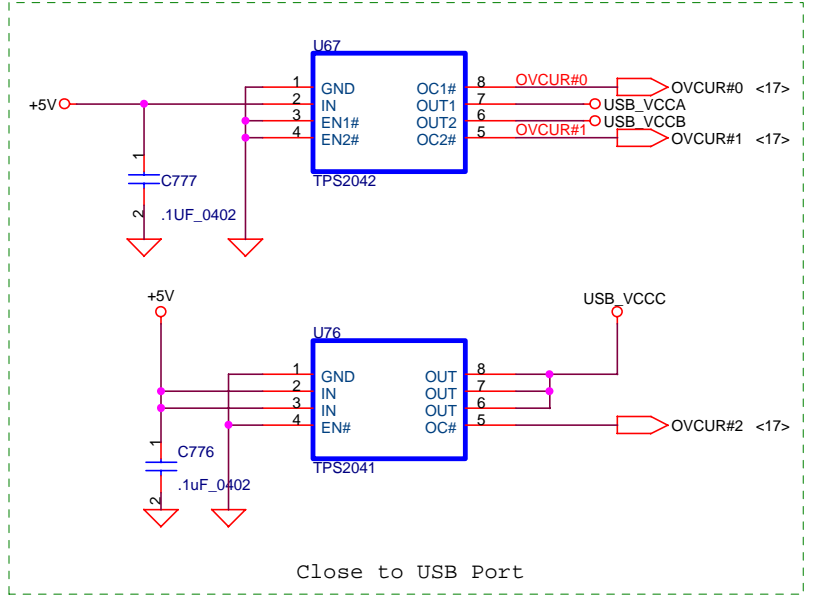
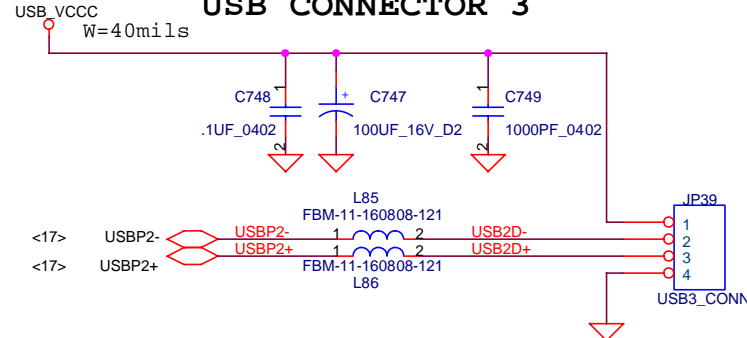
MDC Conn.



BlueTooth Interface



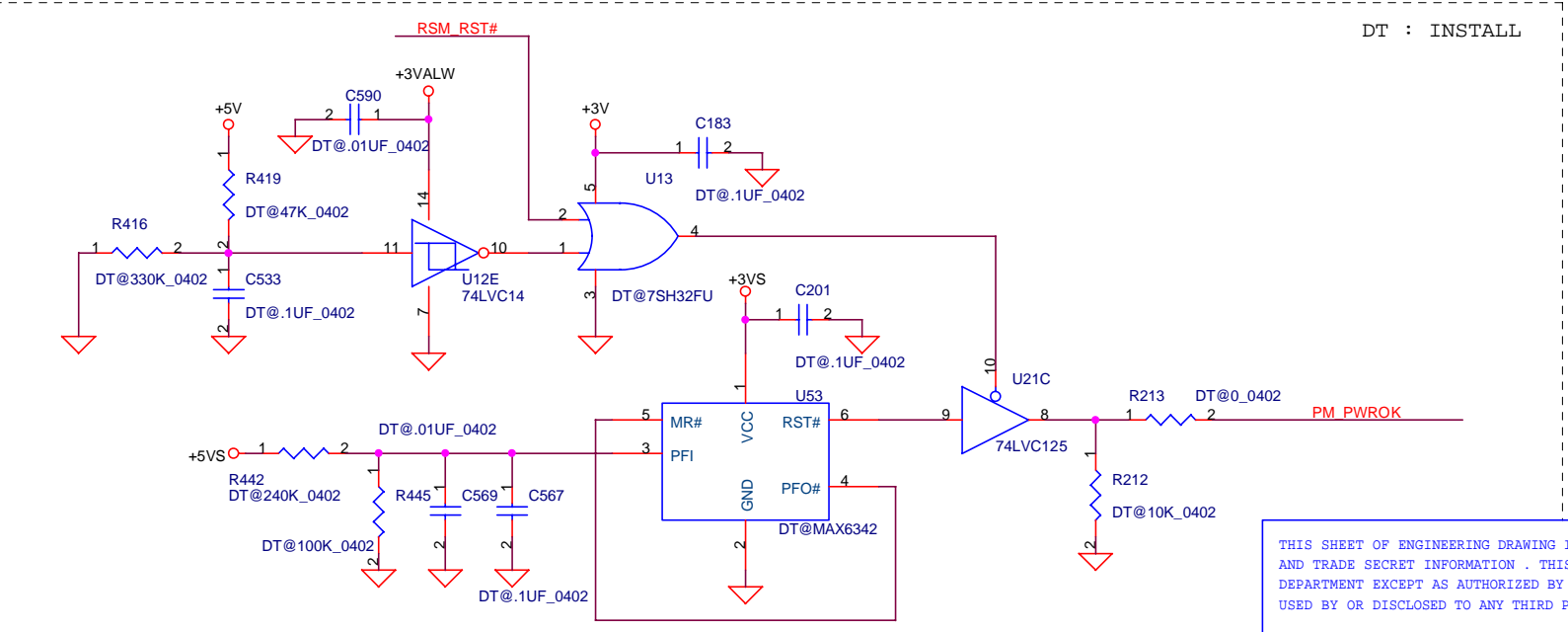
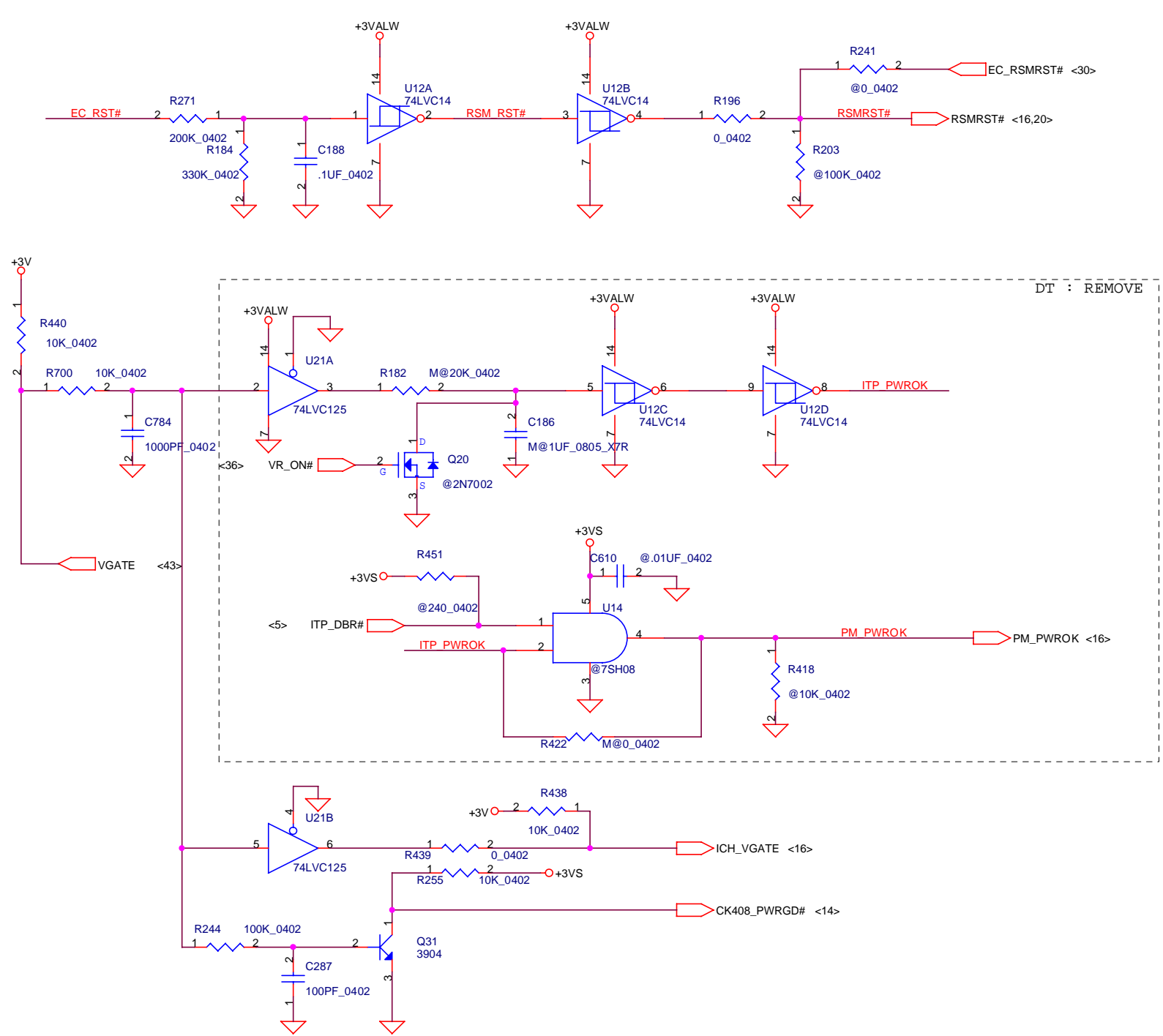
USB CONNECTOR 3



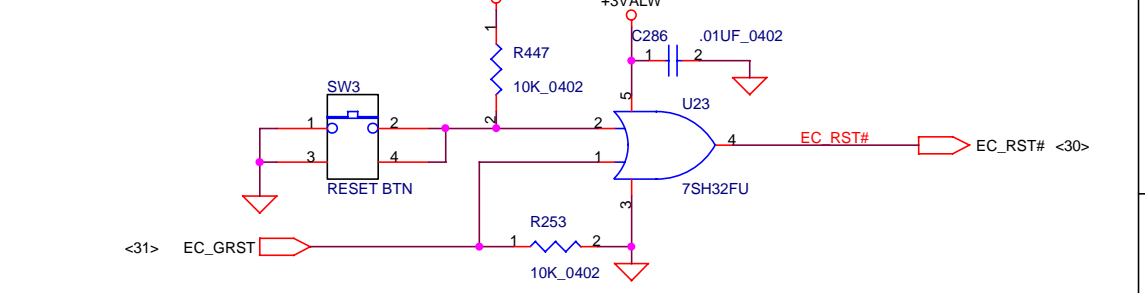
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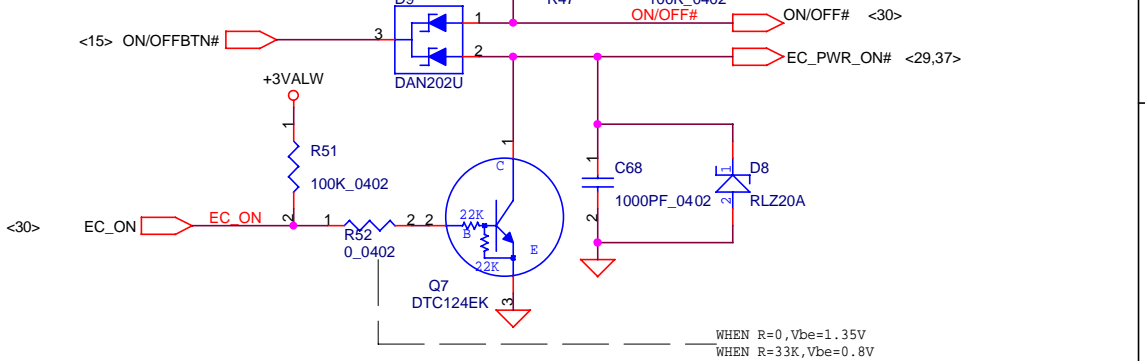
Power ON Circuit



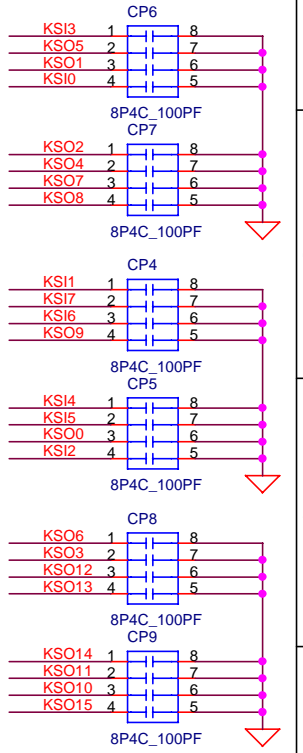
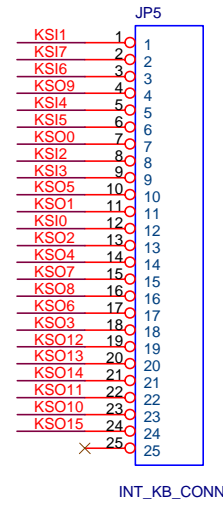
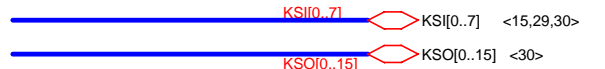
Reset Button



Power BTN



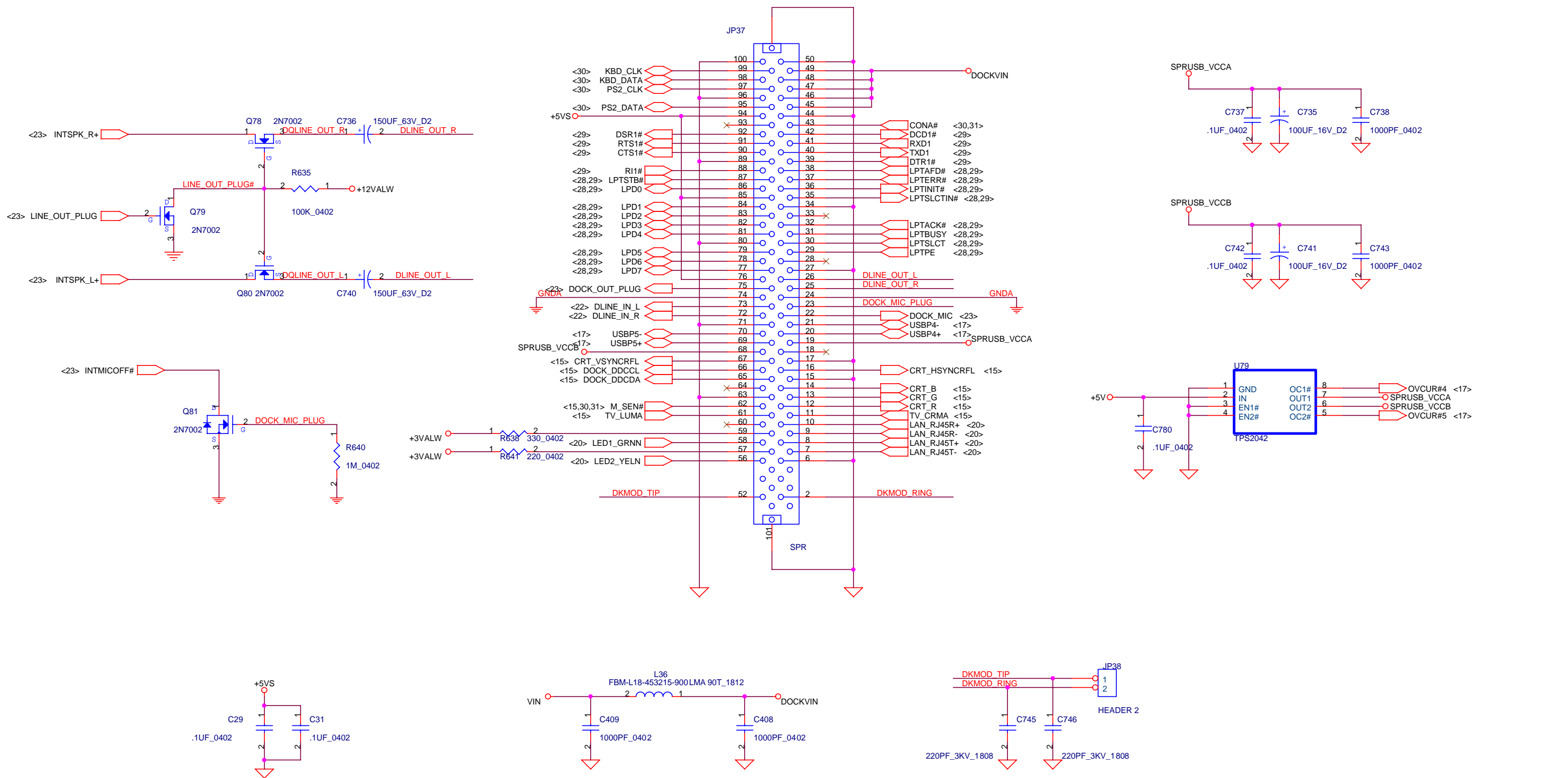
INT_KBD CONN.



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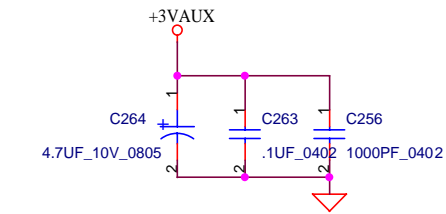
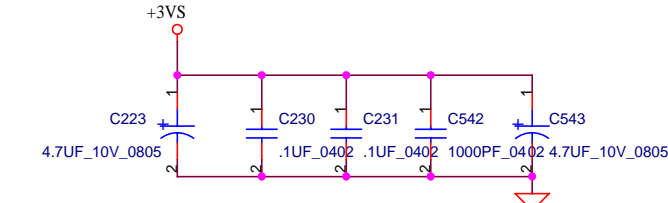
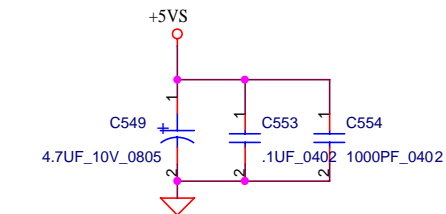
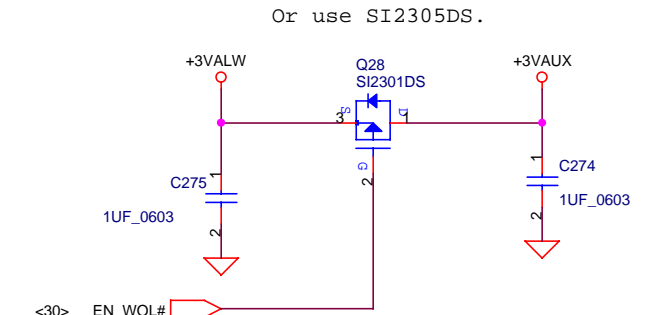
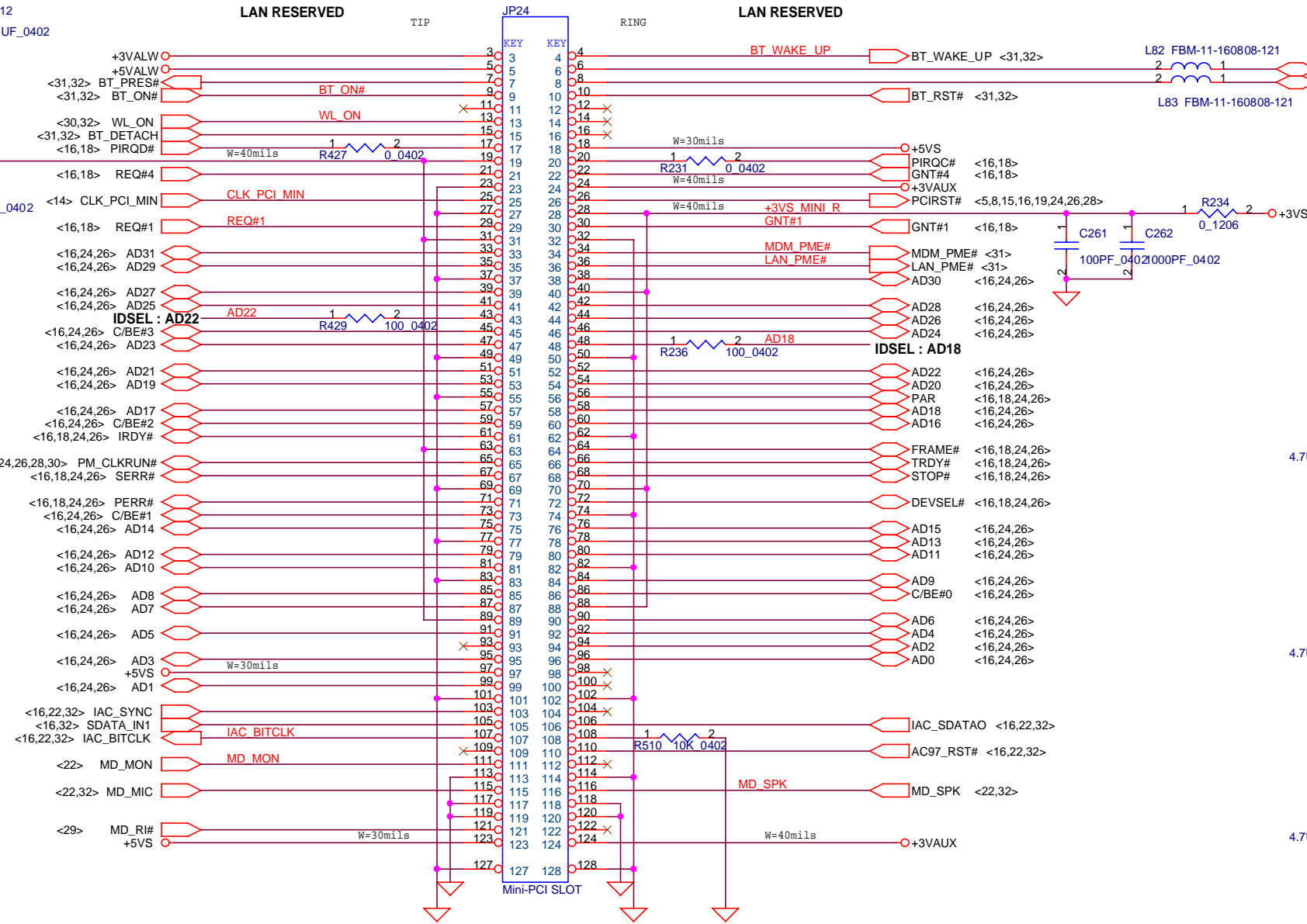
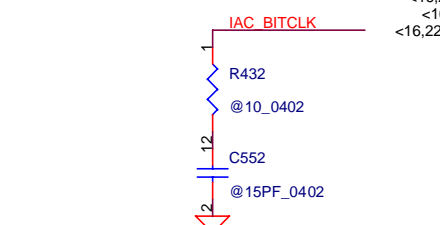
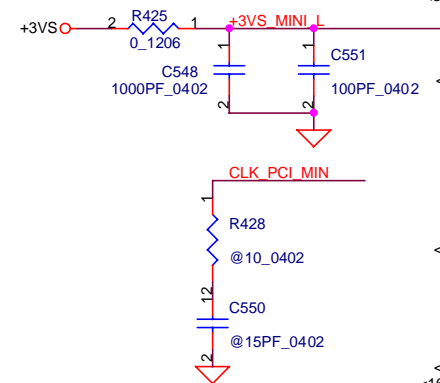
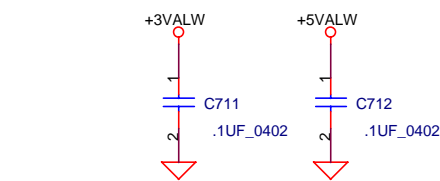
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DOCKING 204 PIN



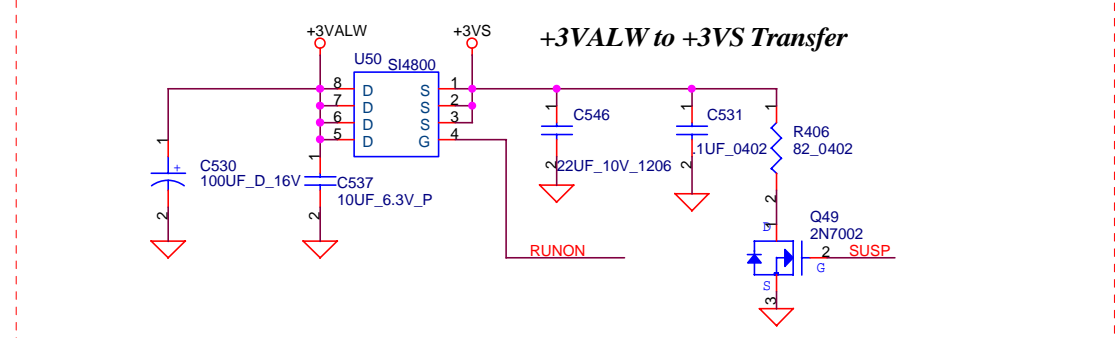
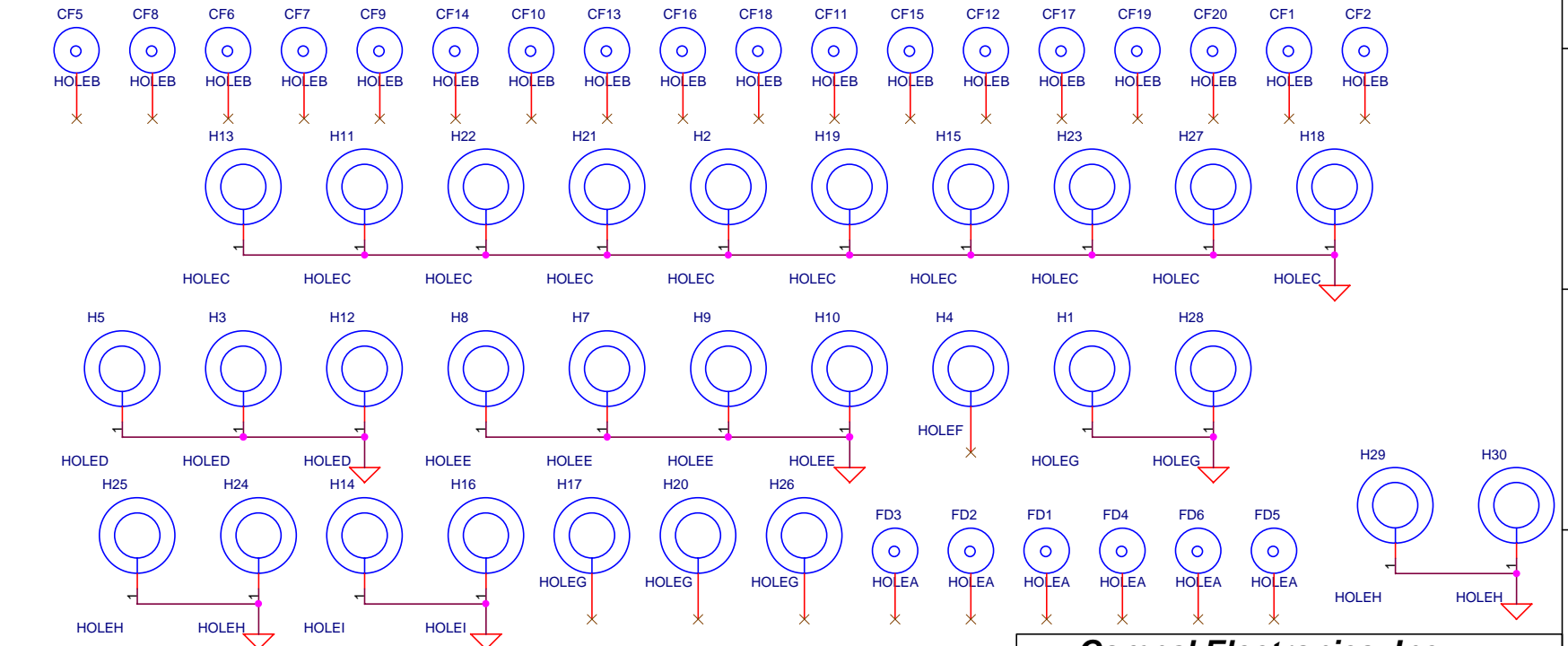
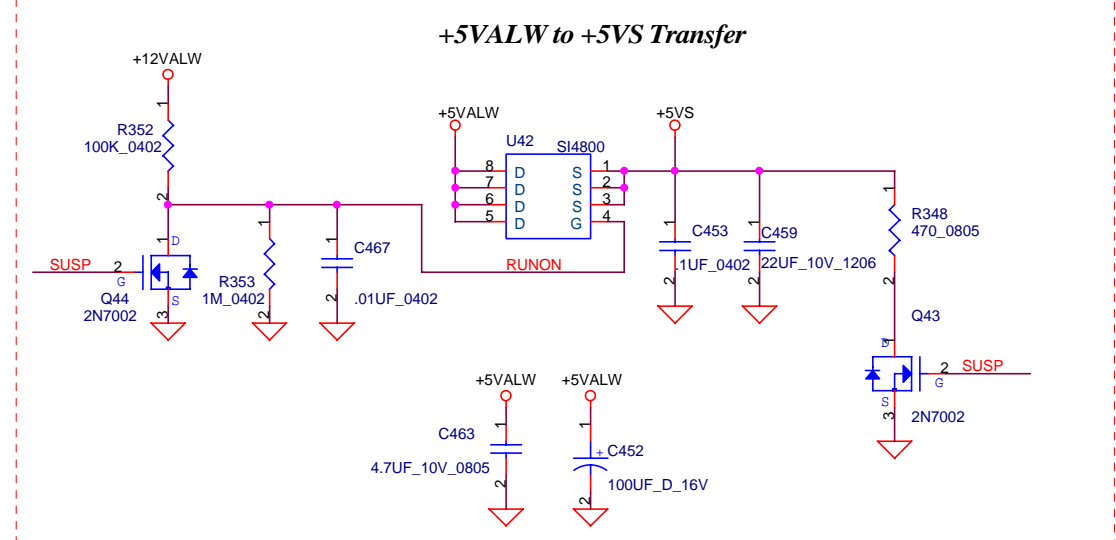
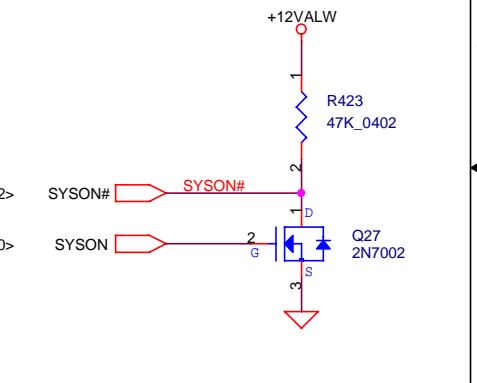
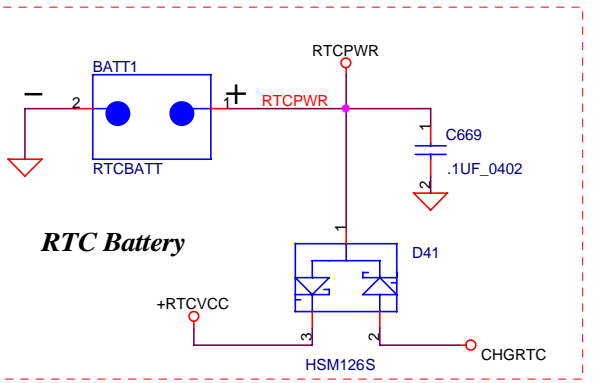
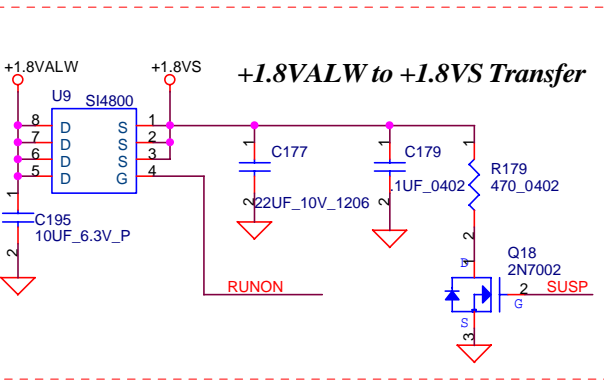
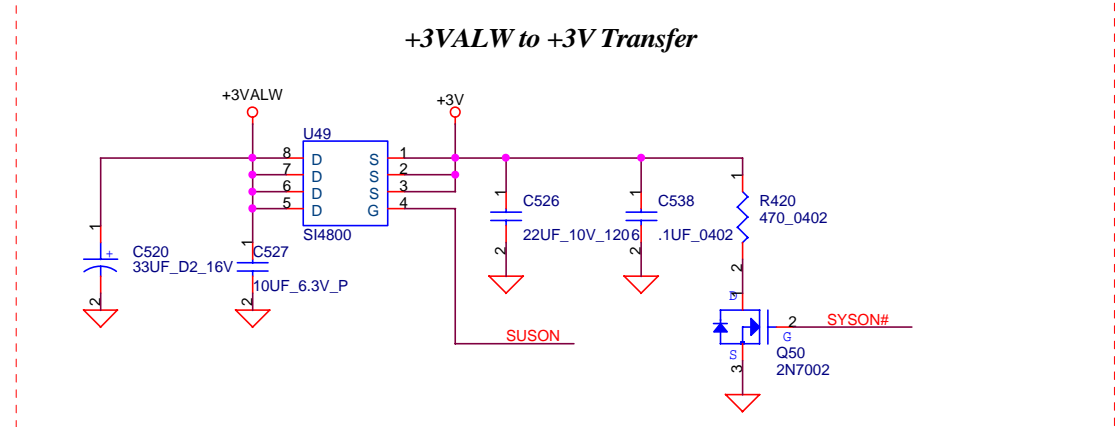
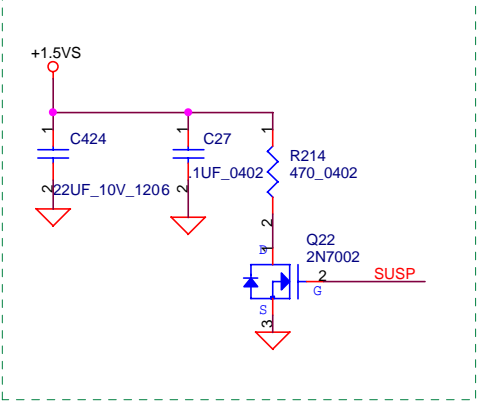
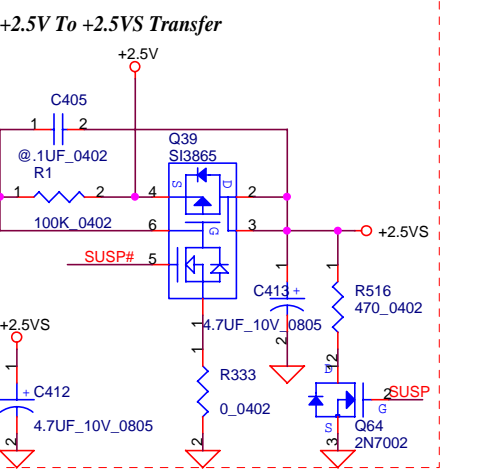
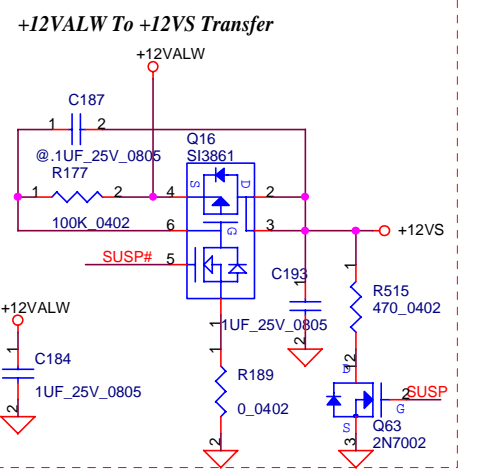
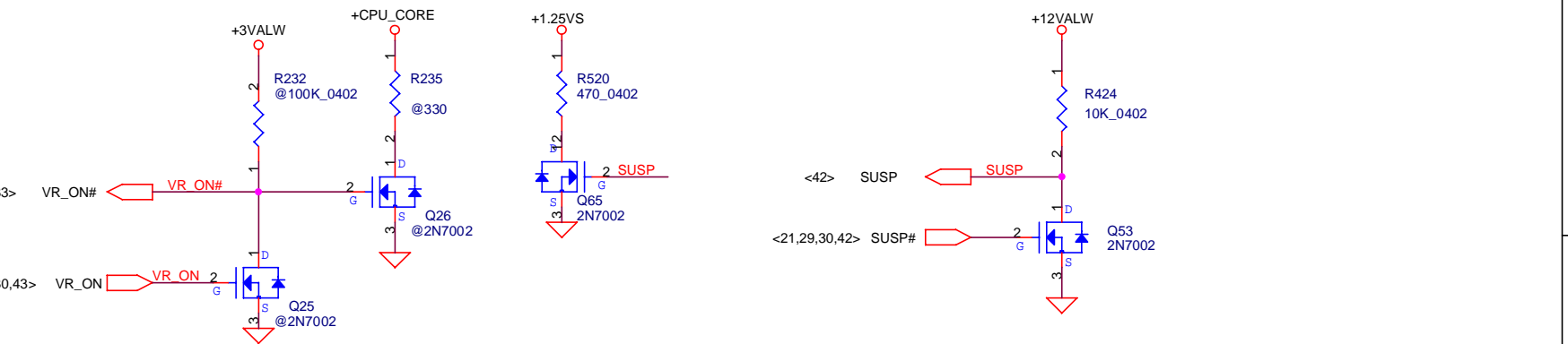
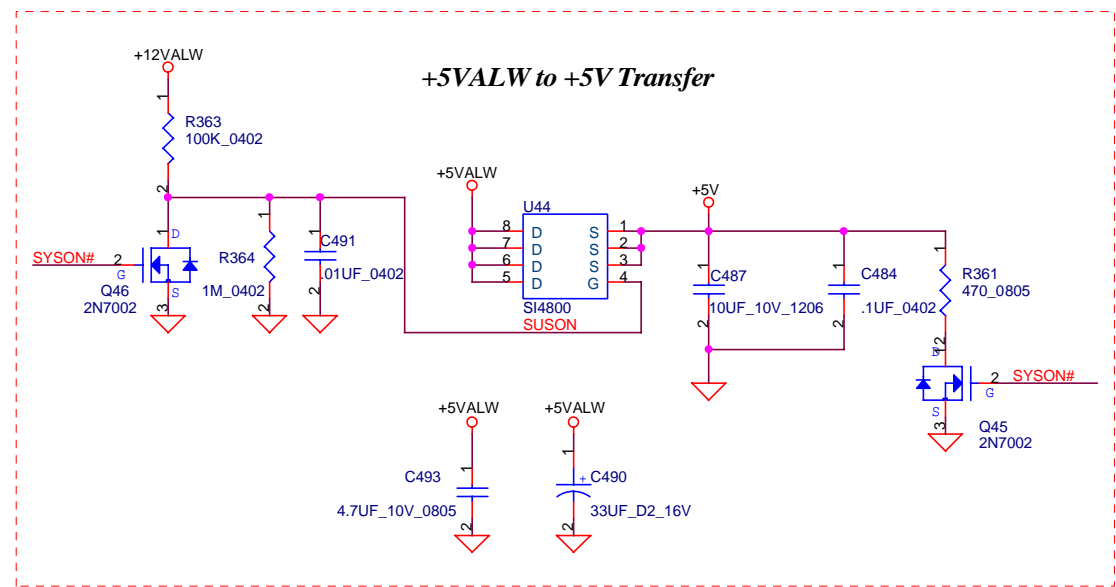
Compal Electronics, Inc.		
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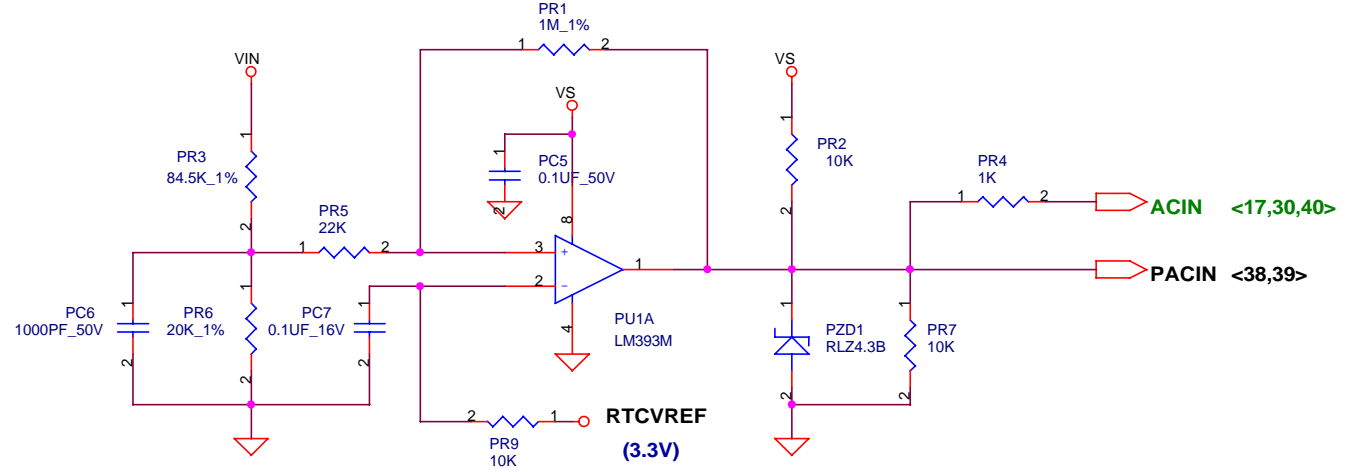
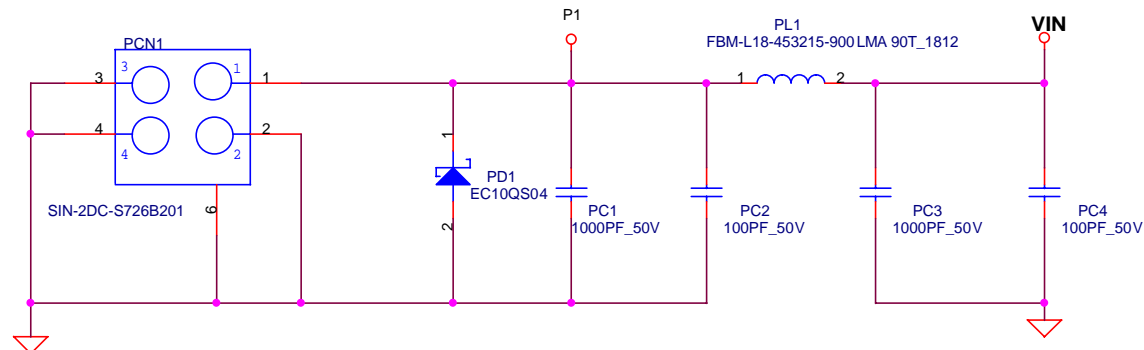
Compal Electronics, Inc.		
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Vin Detector
 High 18.784 17.901 17.077 V
 Low 17.877 17.043 16.195 V

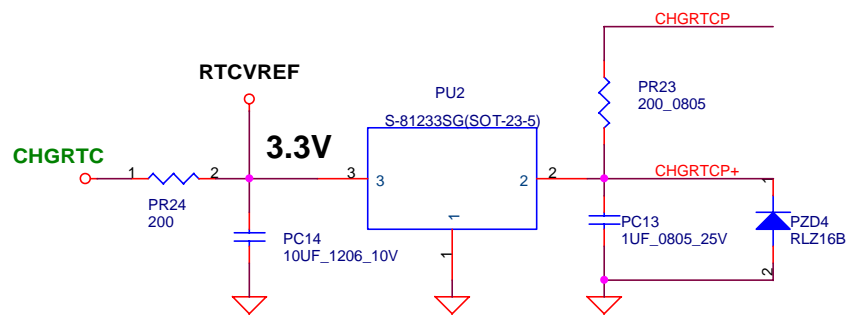
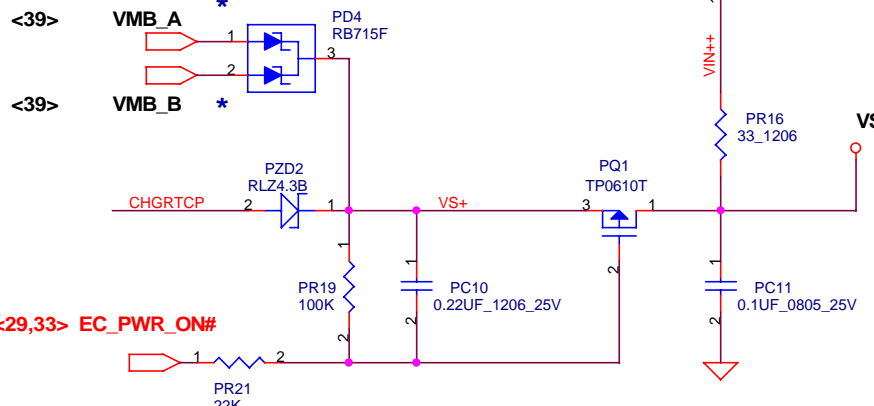
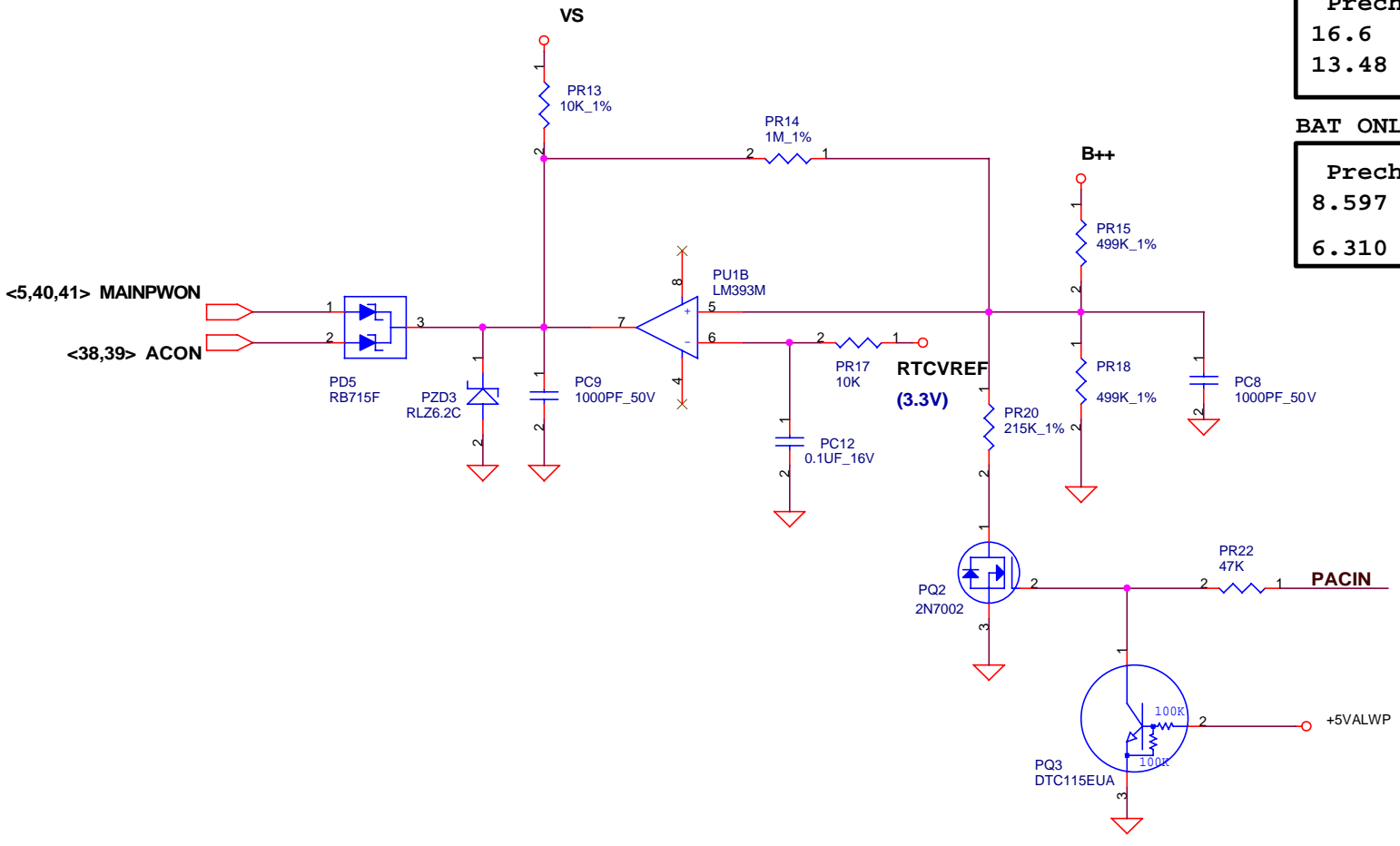
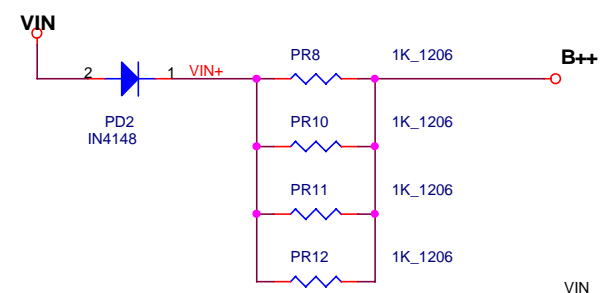


ACIN

Precharge detector		
16.6	15.9	15.2
13.48	12.93	12.09

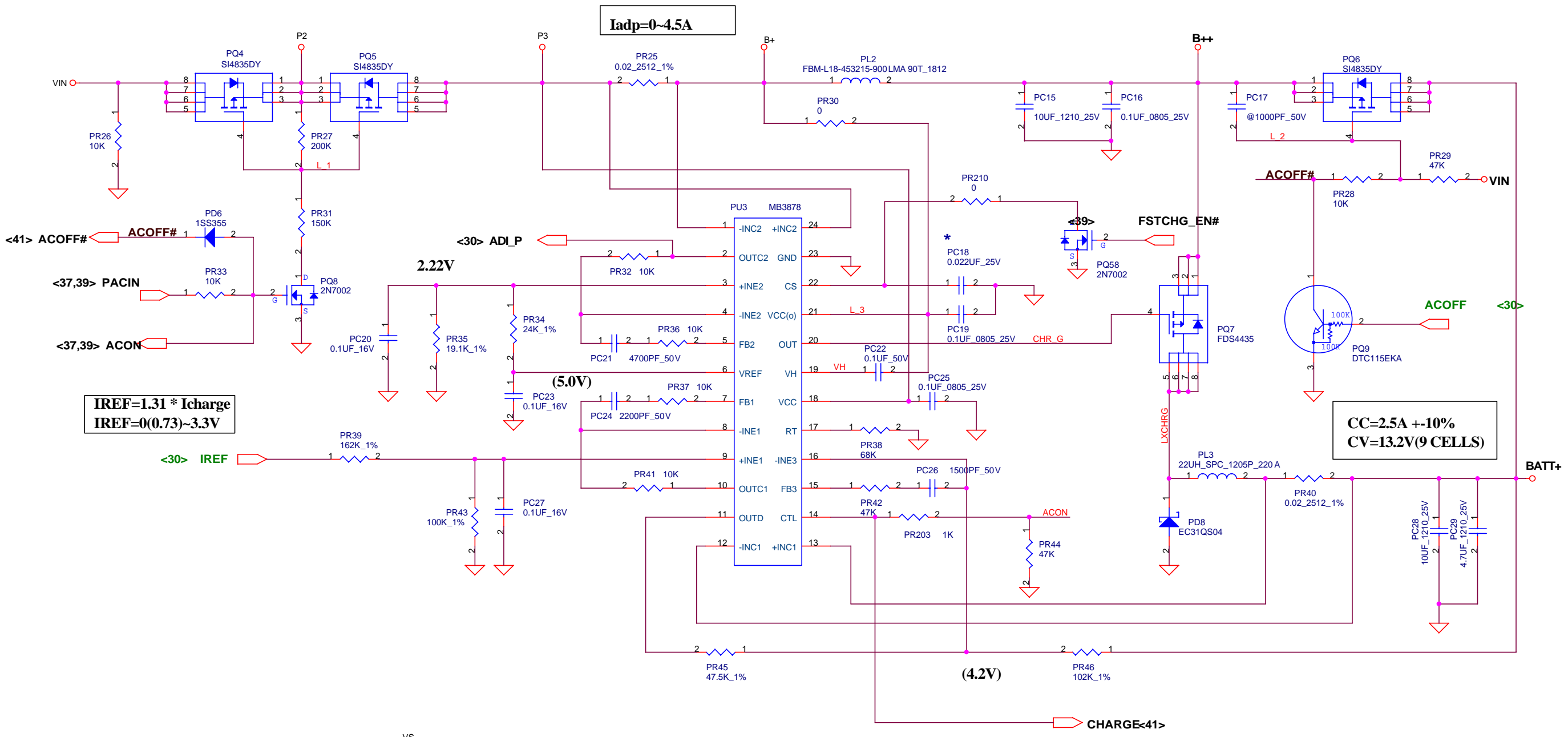
BAT ONLY

Precharge detector		
8.597	8.247	7.904
6.310	6.101	5.683



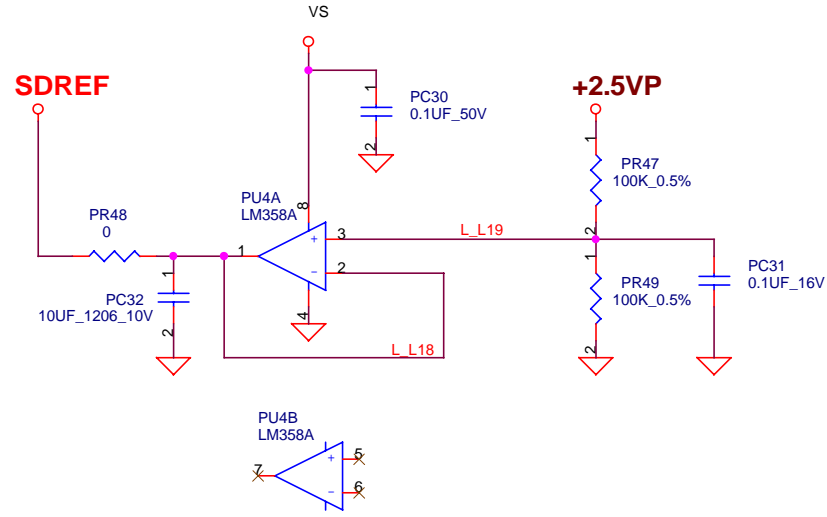
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Compal Electronics, Inc.
 Title: **SCHEMATIC, M/B LA-1511**
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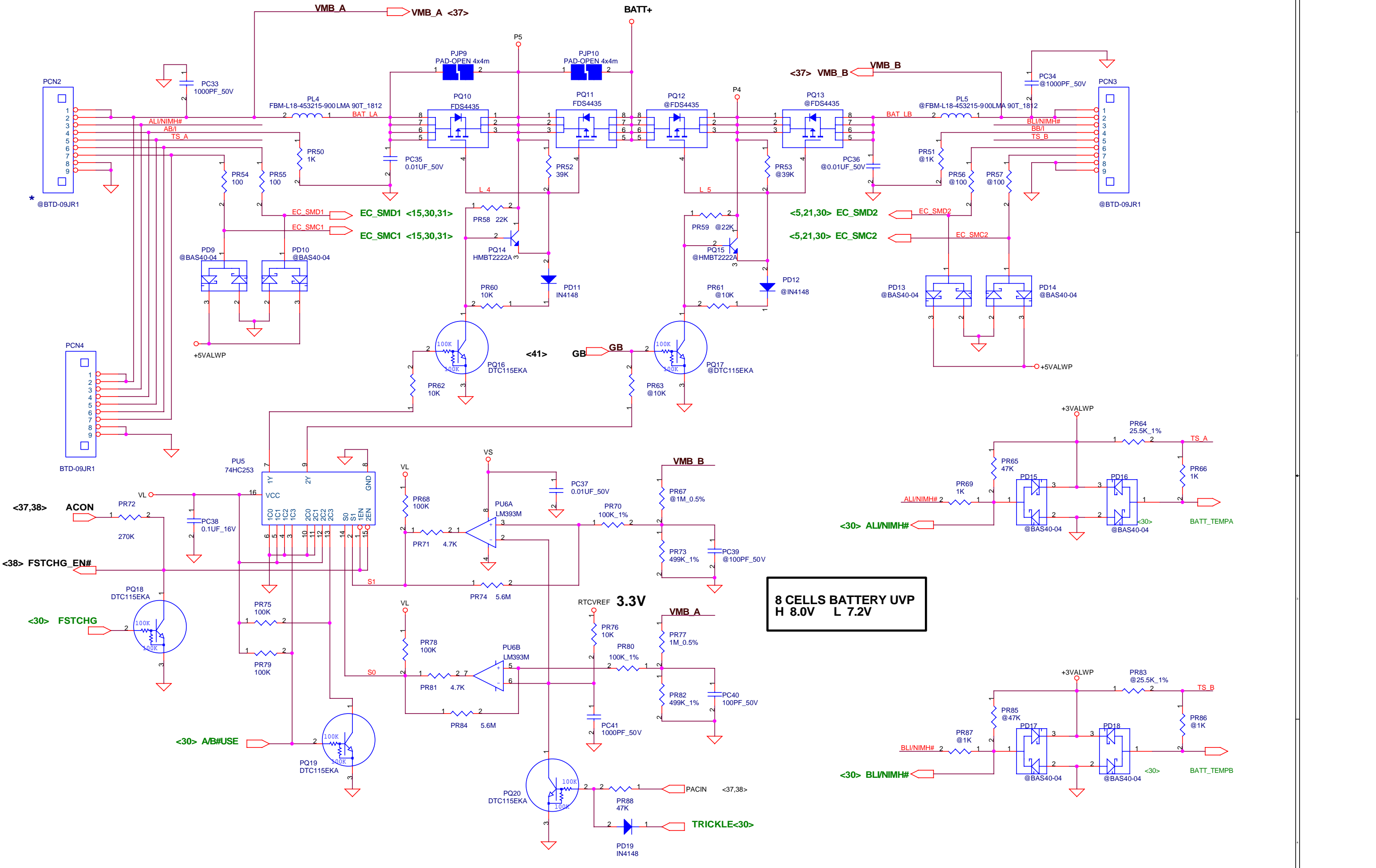
IREF=1.31 * Icharge
IREF=0(0.73)~3.3V

CC=2.5A +-10%
CV=13.2V(9 CELLS)



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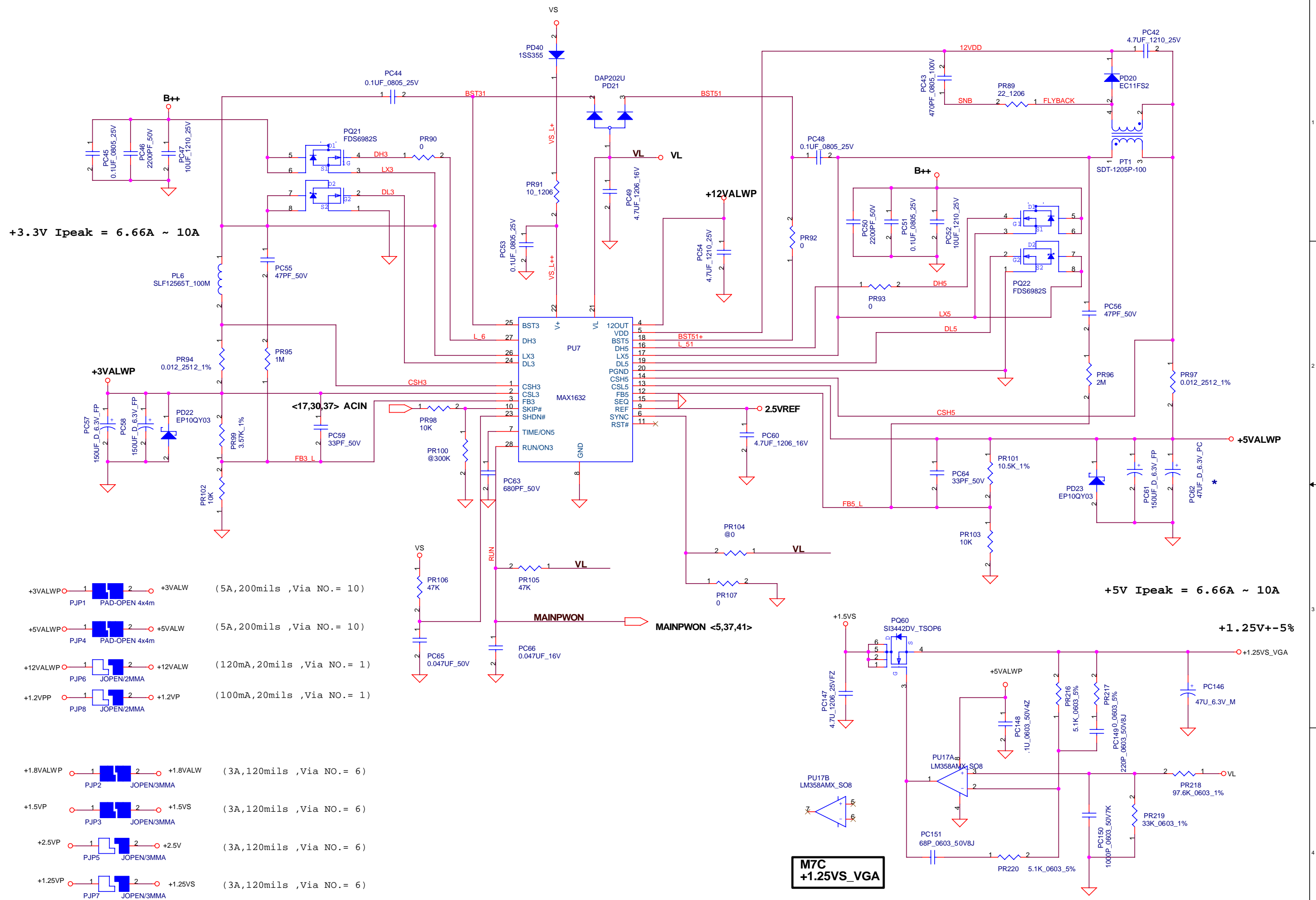
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8 CELLS BATTERY UVP
H 8.0V L 7.2V

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+3.3V Ipeak = 6.66A ~ 10A

+5V Ipeak = 6.66A ~ 10A

M7C
+1.25VS_VGA

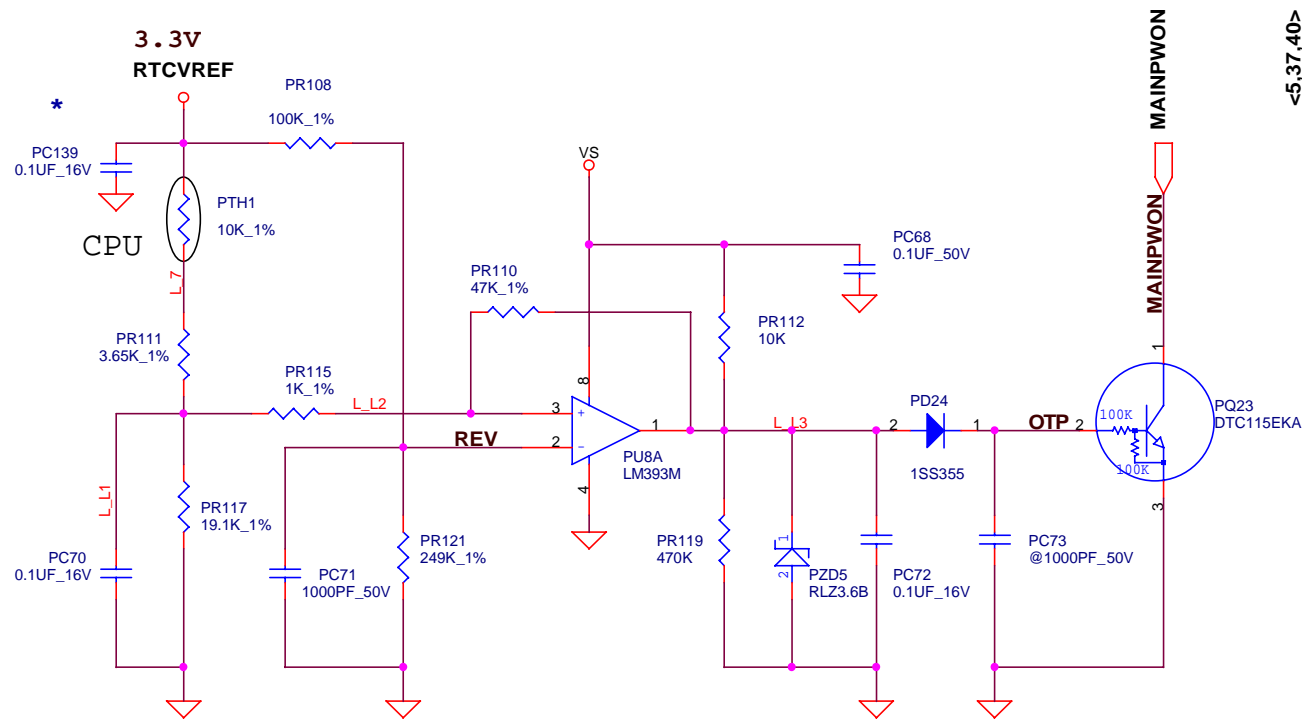
- +3VALWP (1) (2) (5A, 200mils, Via NO.= 10)
PJP1 PAD-OPEN 4x4m
- +5VALWP (1) (2) (5A, 200mils, Via NO.= 10)
PJP4 PAD-OPEN 4x4m
- +12VALWP (1) (2) (120mA, 20mils, Via NO.= 1)
PJP6 JOPEN/2MMA
- +1.2VPP (1) (2) (100mA, 20mils, Via NO.= 1)
PJP8 JOPEN/2MMA
- +1.8VALWP (1) (2) (3A, 120mils, Via NO.= 6)
PJP2 JOPEN/3MMA
- +1.5VP (1) (2) (3A, 120mils, Via NO.= 6)
PJP3 JOPEN/3MMA
- +2.5VP (1) (2) (3A, 120mils, Via NO.= 6)
PJP5 JOPEN/3MMA
- +1.25VP (1) (2) (3A, 120mils, Via NO.= 6)
PJP7 JOPEN/3MMA
- +1.25VS (1) (2) (3A, 120mils, Via NO.= 6)
PJP11 JOPEN/3MMA

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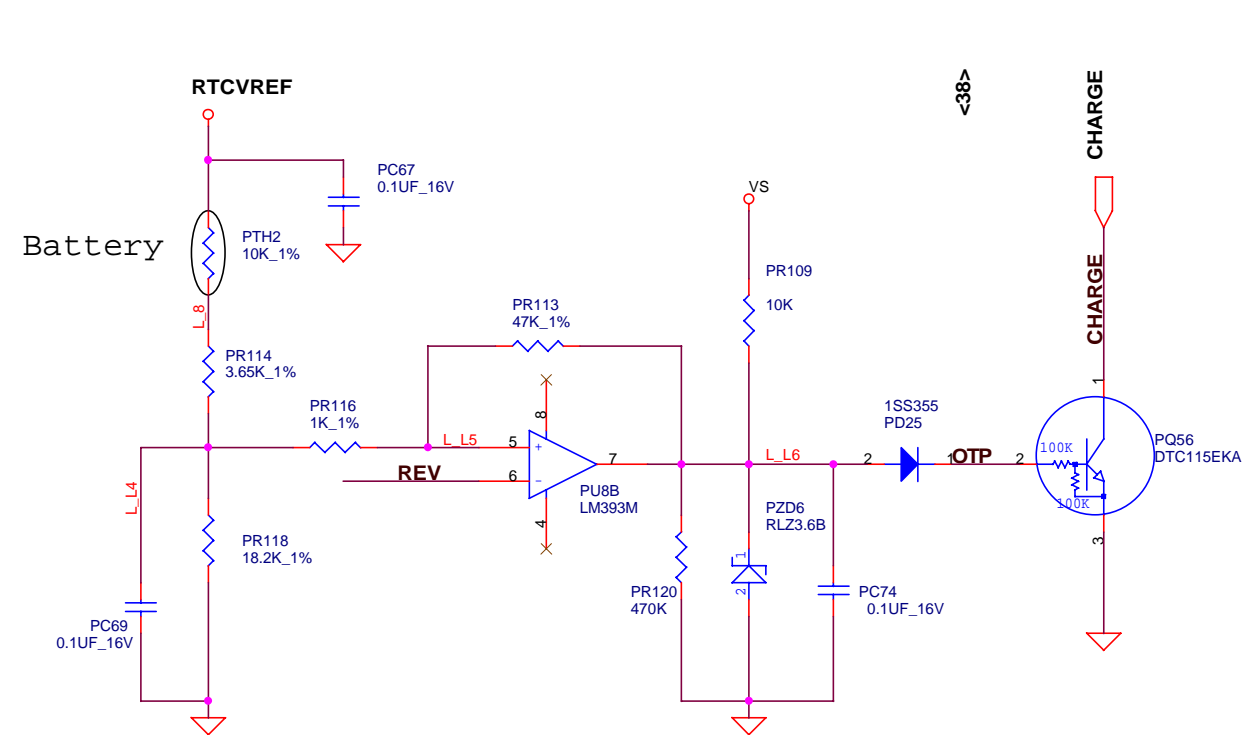
PH1 under CPU botten side :

CPU thermal protection at 90(91)+-3 degree C
 Recovery at 50(51)+-3 degree C

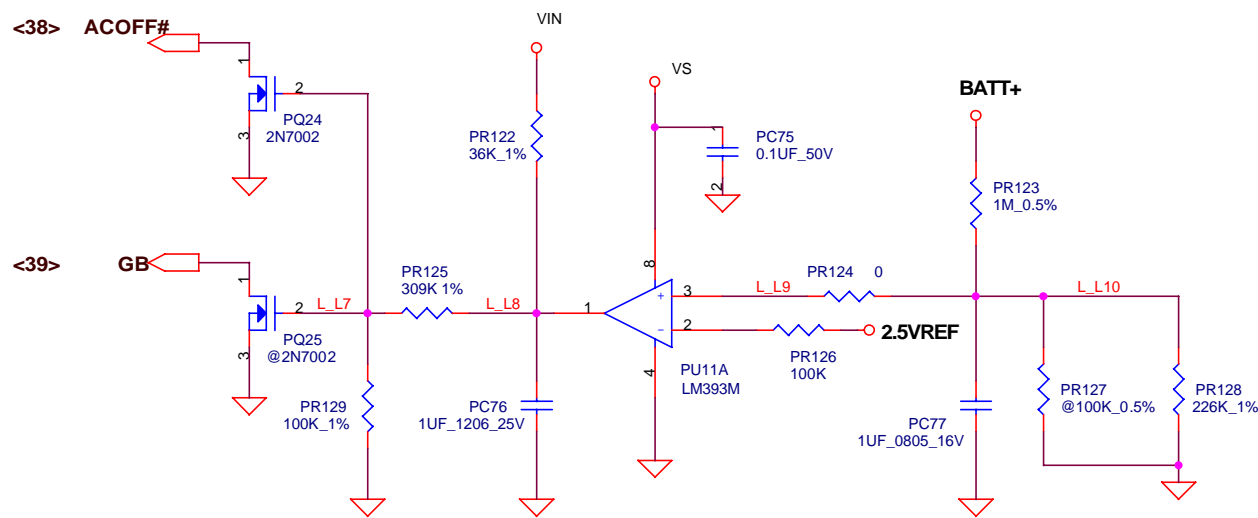


PH2 near main Battery CONN :

BAT. thermal protection at 85(86)+-3 degree C
 Recovery at 50(51)+-3 degree C

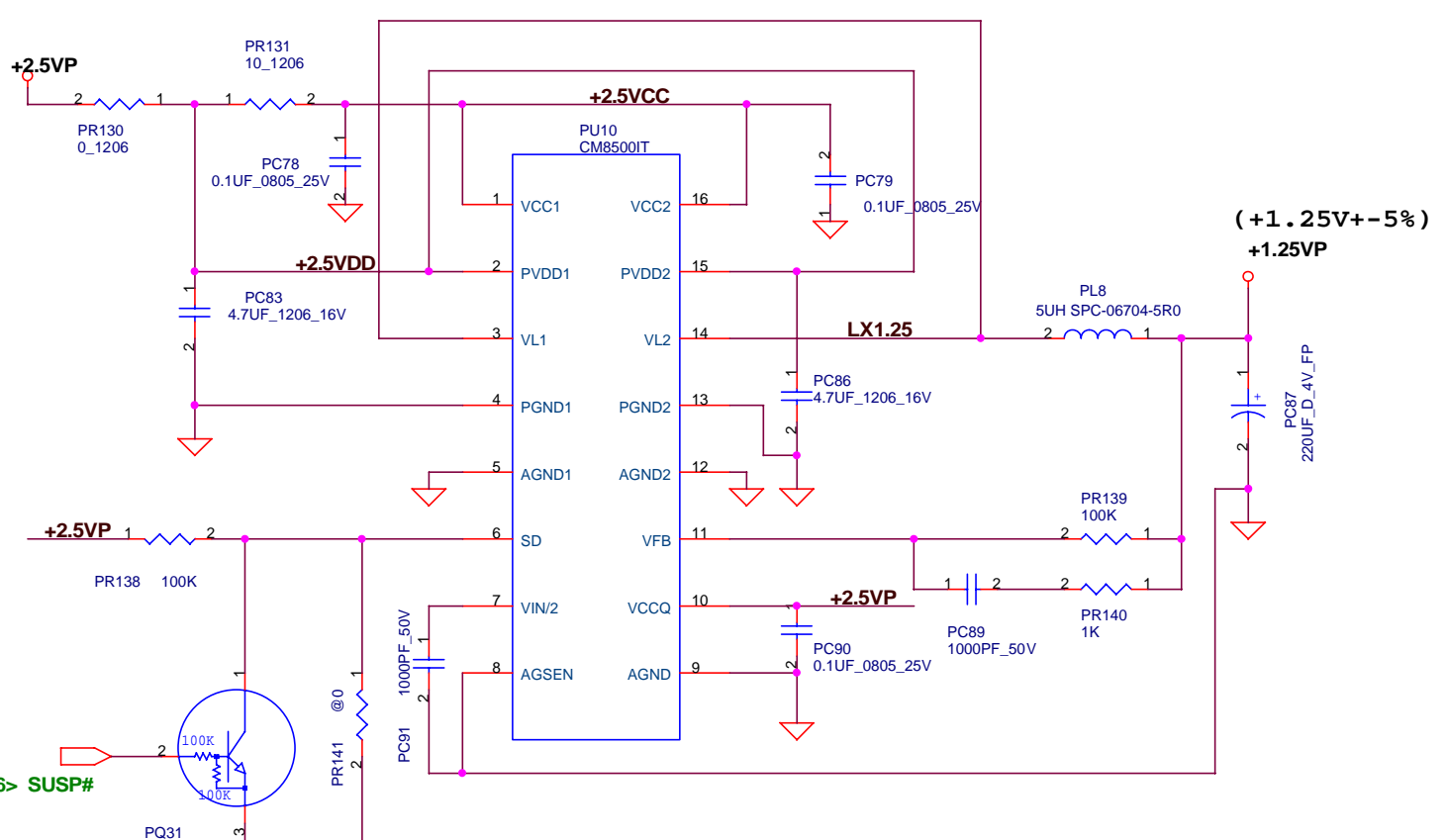
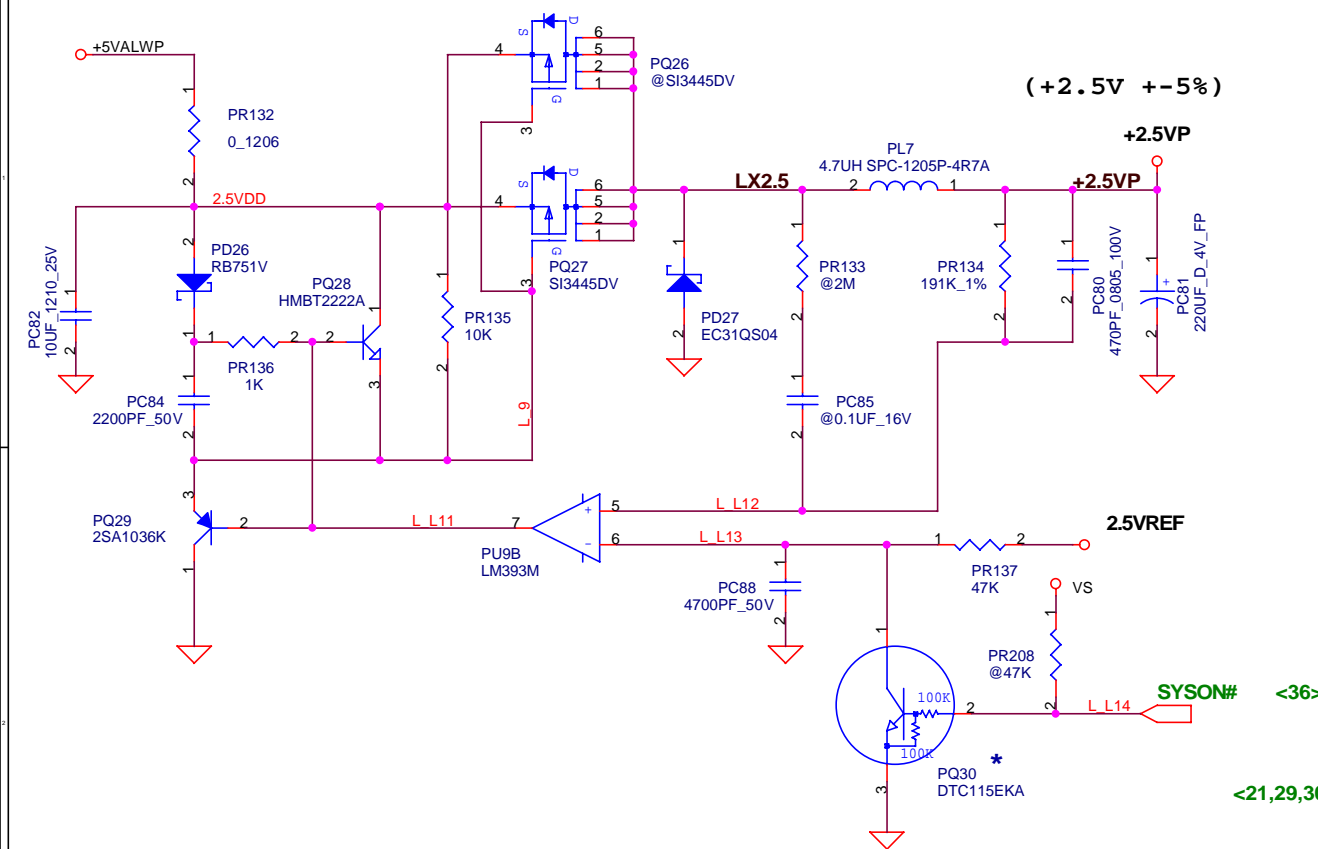


BATTERY Charger OVP : 13.56V

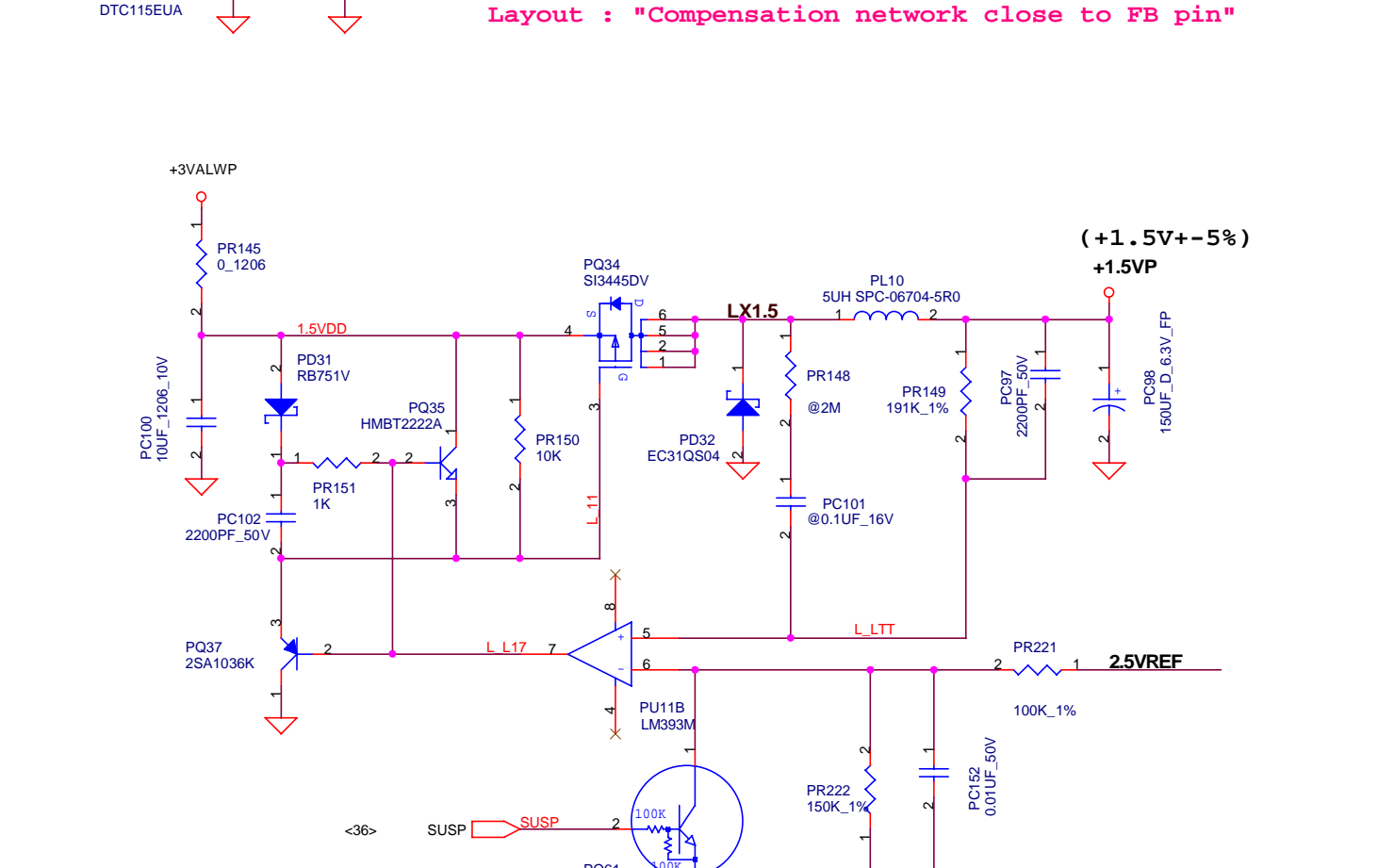
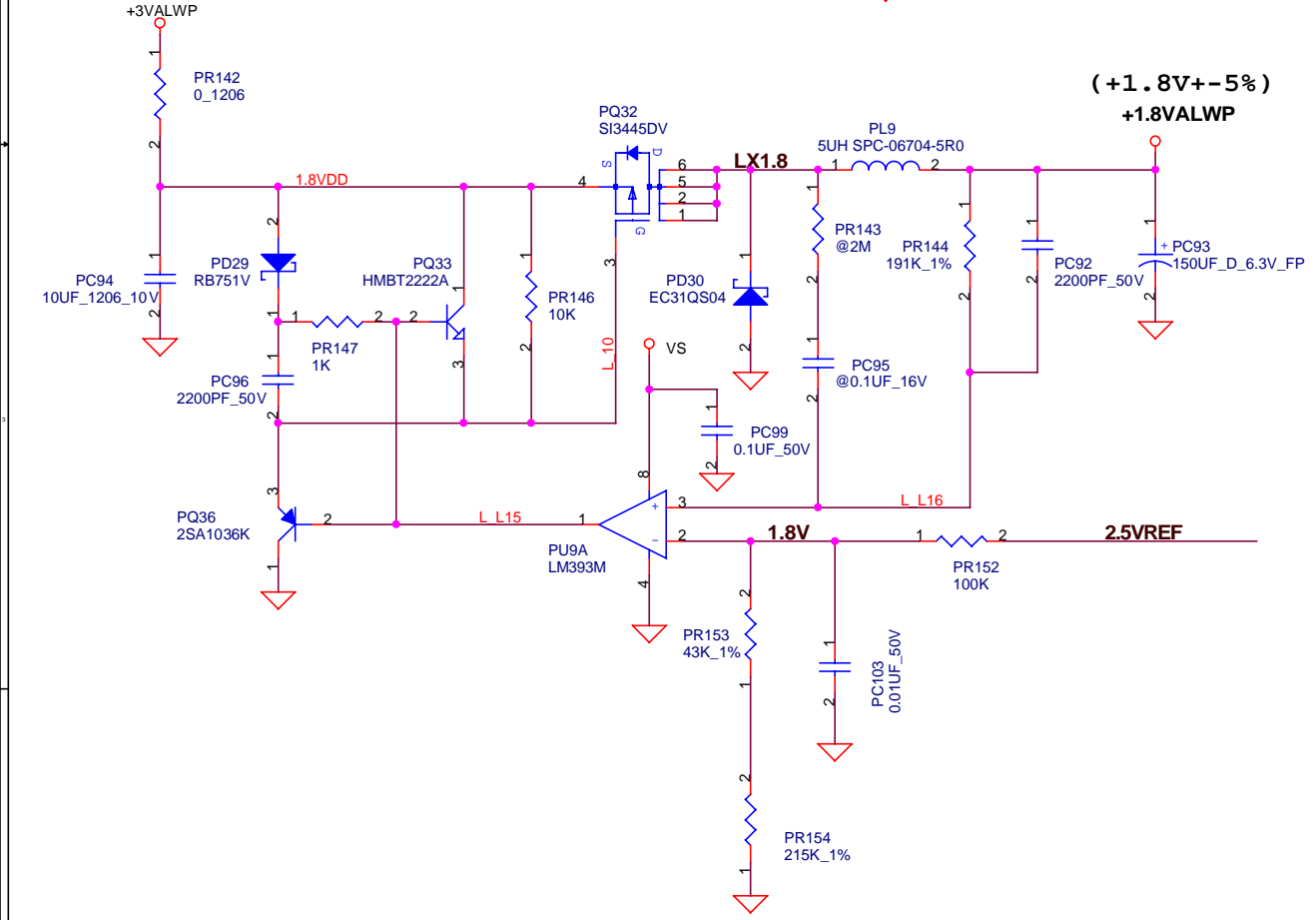


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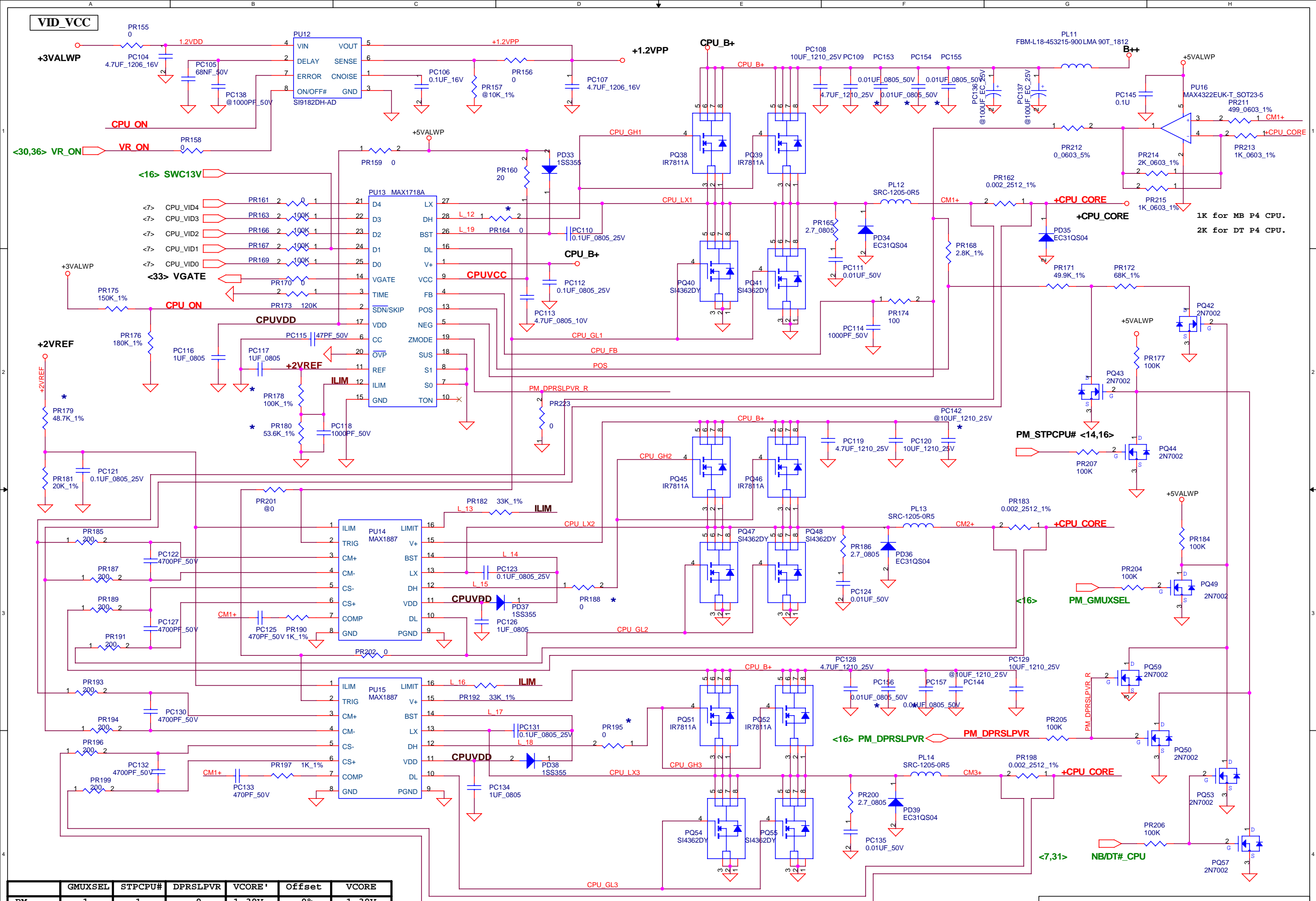
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VID_VCC



	GMUXSEL	STPCPU#	DPRSLPVR	VCORE'	Offset	VCORE
PM	1	1	0	1.30V	0%	1.30V
PM D-S	1	0	0	1.2309V	4.62%	1.2309V
BM	0	1	0	1.20V	2.0%	1.176V
BM D-S	0	0	0	1.144V	4.62%	1.144V
Deeper	X	0	1	1.0V	0%	1.0V

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