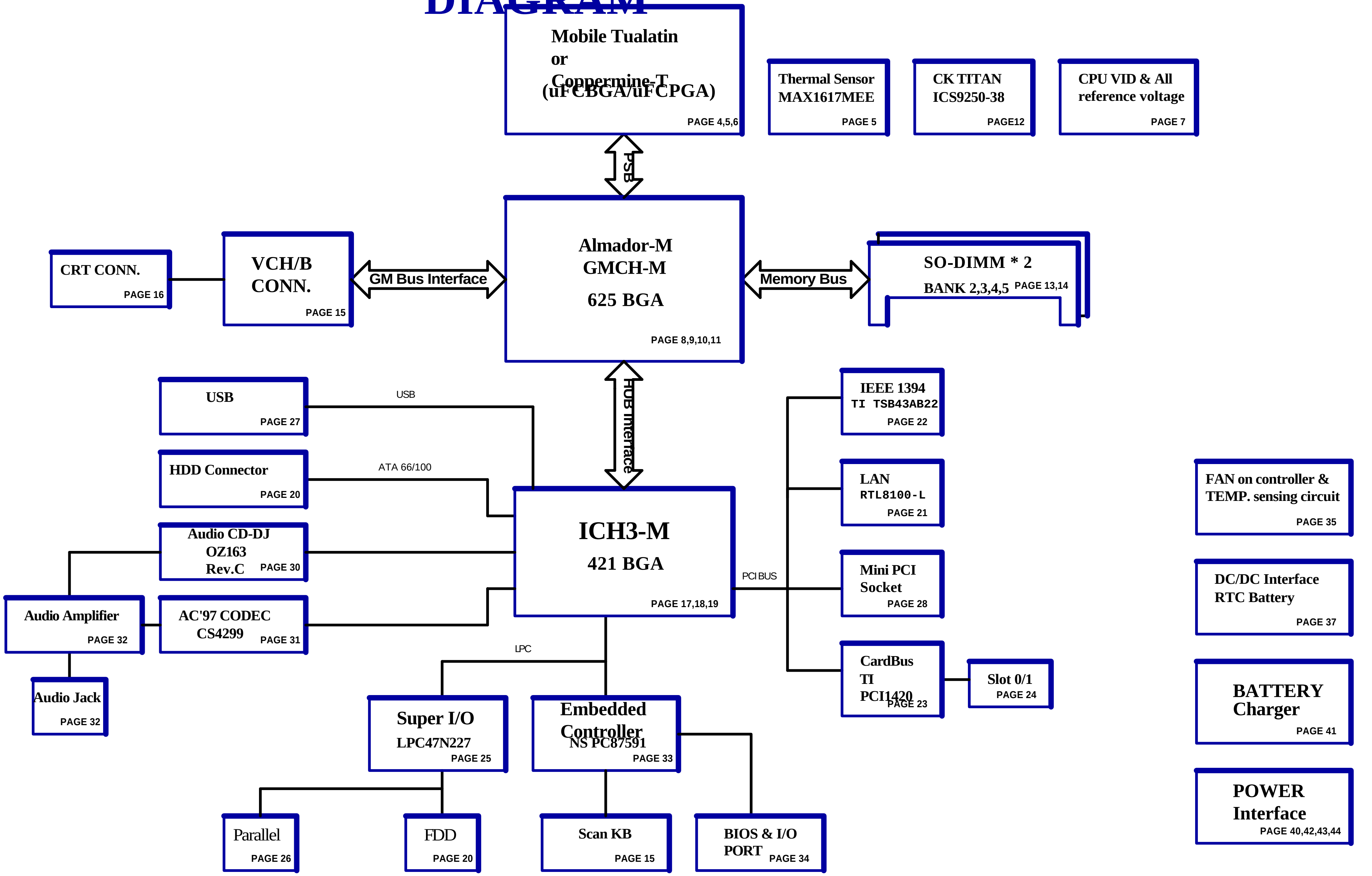
ACL05 LA-1371 Schematics Document

REV 1.0

INTEL Coppermine-T or Tualatin CPU uFCBGA/uFCPGA

Almador-M(830MG) + ICH3-M + VCH Chipset

ACL05 BLOCK DIAGRAM



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_H_CORE	Core voltage for CPU	ON	OFF	OFF
+VTT	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+1.8V	1.8V power rail	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12VS	12V switched power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
VCH CONN.			PIRQA
IEEE 1394	AD16	0	PIRQA
CardBus	AD20	2	PIRQA/PIRQB
LAN	AD17	3	PIRQB
Mini-PCI	AD18	1/4	PIRQC/PIRQD
SD/SM (RESERVE)	AD22		PIRQC/PIRQD

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
(24C04)	1011 000Xb

EC SM Bus2 address

Device	Address
MAX1617MEE	1001 110X b
OZ163	0011 0100 b
Smart Battery	0001 011X b
Docking	0011 011X b
DOT Board	XXXX XXXXb

ICH3-M SM Bus address

Device	Address
Clock Generator (ICS9238-50)	1101 0000
SDRAM Select (74HC4052)	1010 0000
CPU Voltage VID select (F3565)	0110 111Xb

PIR

REV 0.1

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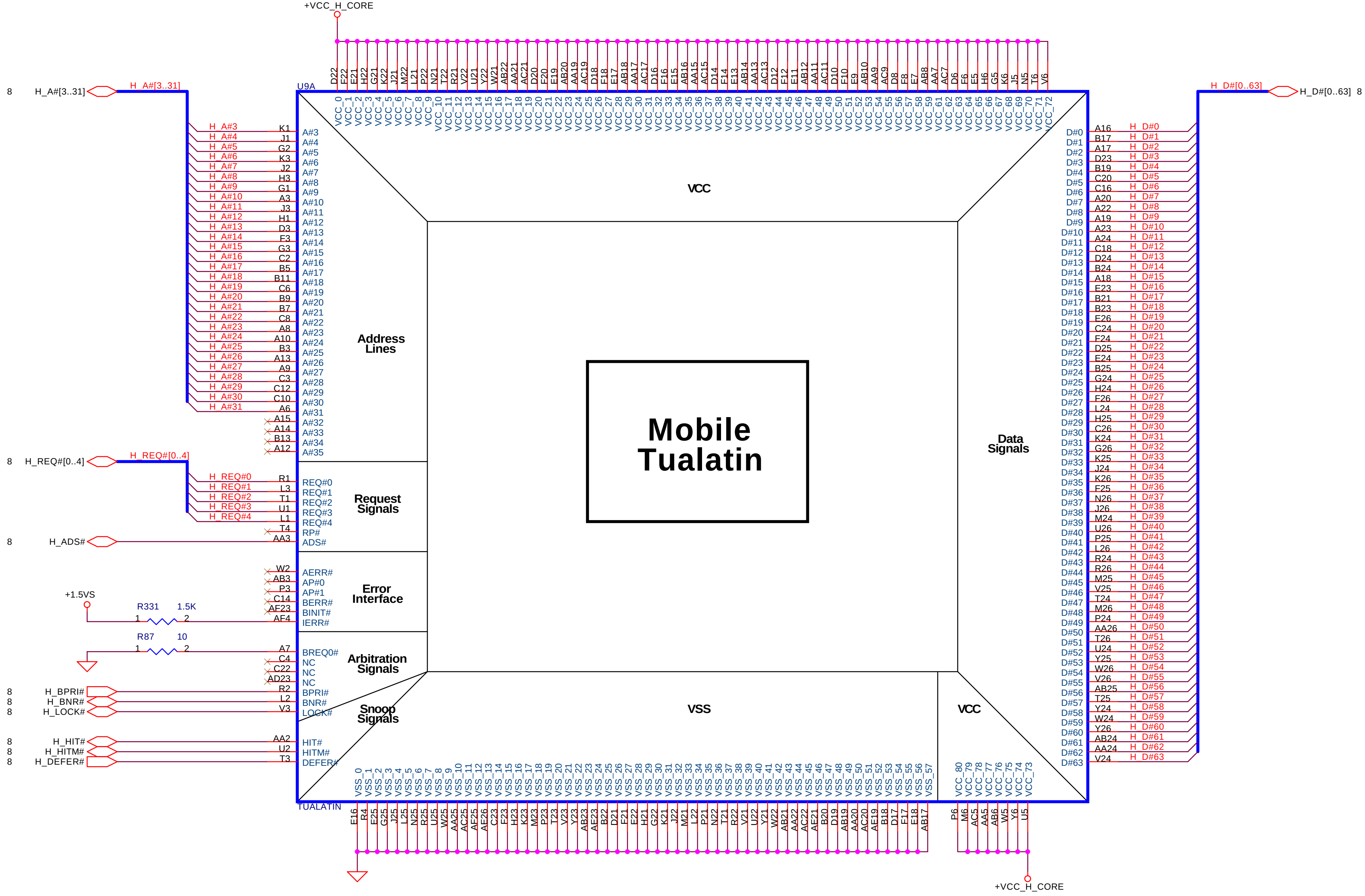

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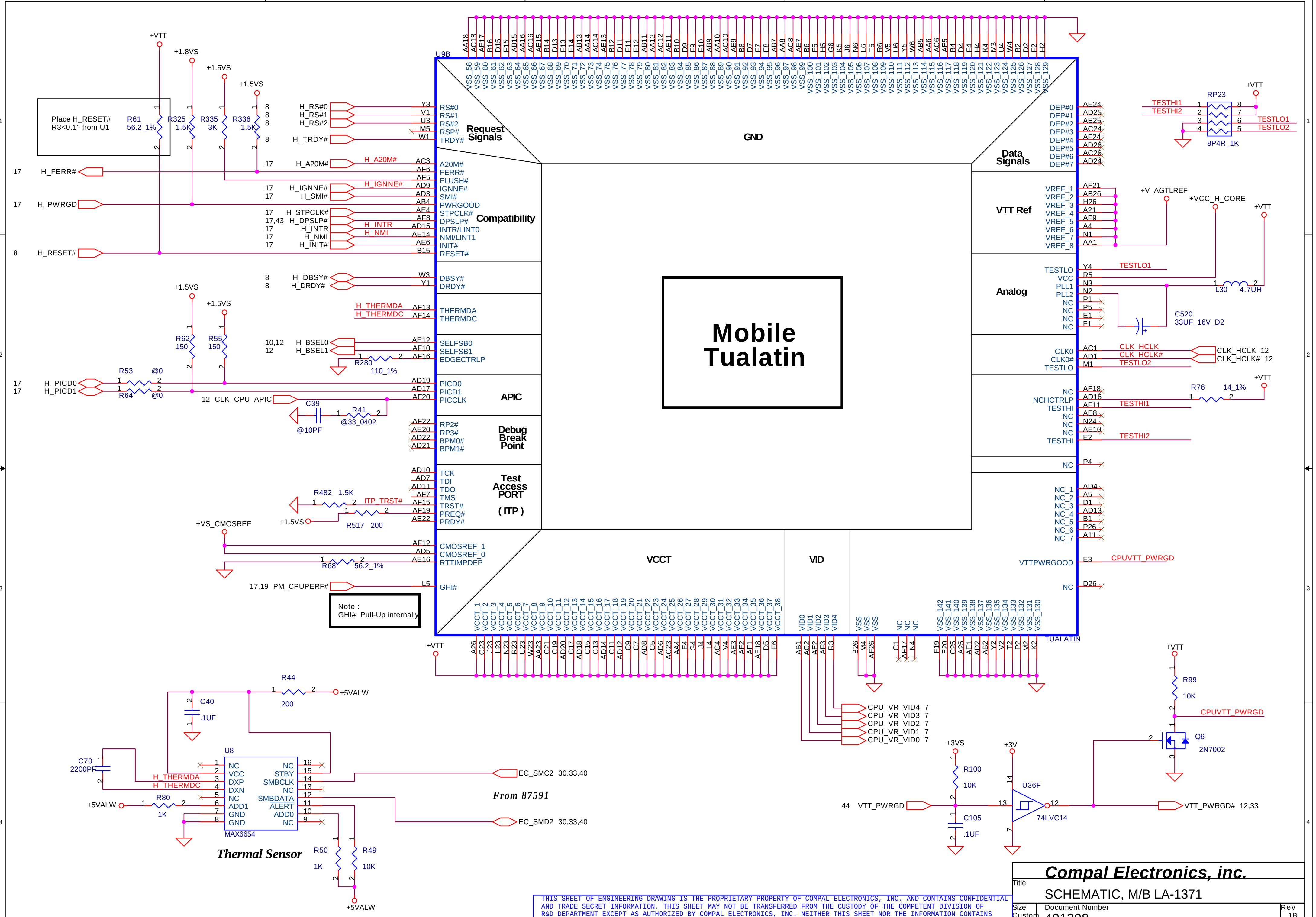

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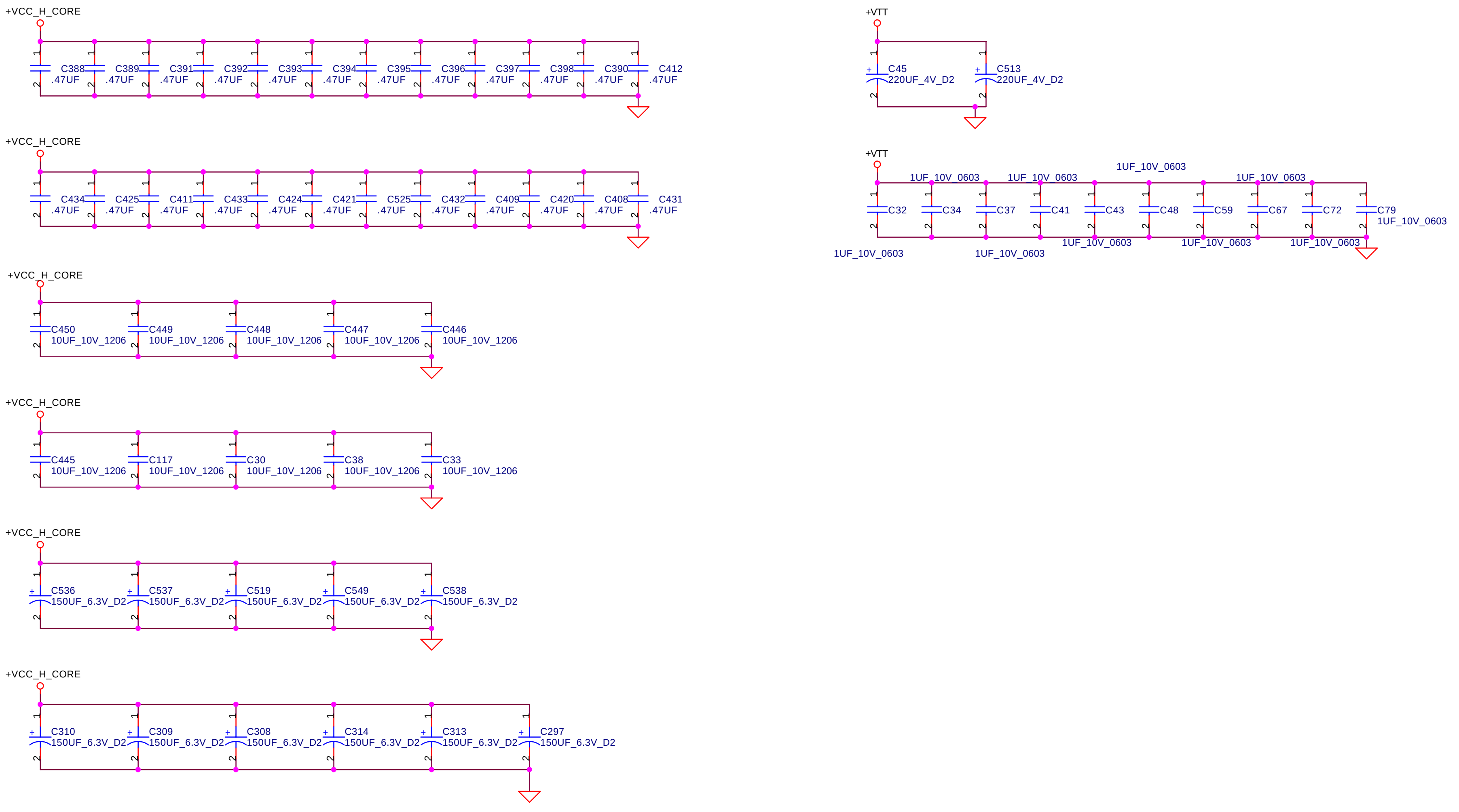
Layout note :

Place close to CPU, Use 2~3 vias per PAD.
Place .47uF caps underneath balls on solder side
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.

Layout note :

Place close to CPU,
Use 2 vias per PAD.



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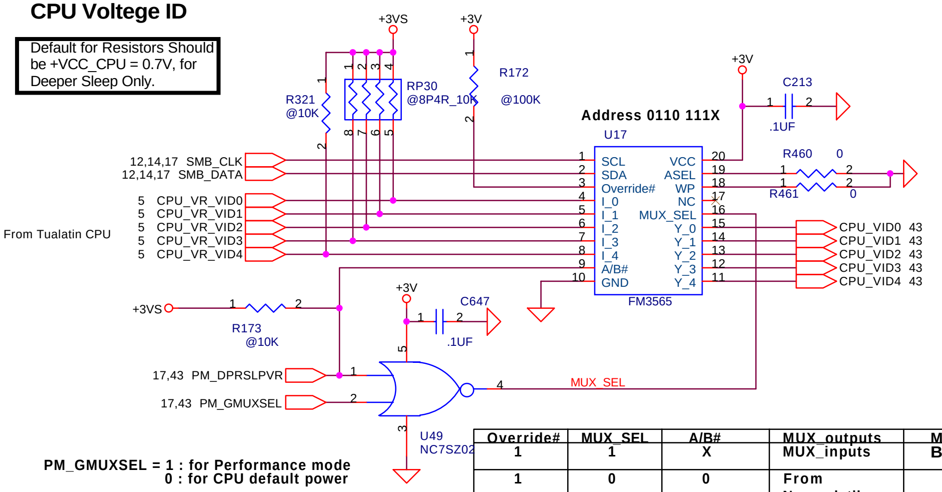
CPU Voltege ID

Default for Resistors Should be +VCC_CPU = 0.7V, for Deeper Sleep Only.



PM_GMUXSEL = 1 : for Performance mode
0 : for CPU default power

PM_DPRSLPVR = 1: for Deeper Sleep mode
0 : for Performance mode

Override#	MUX_SEL	A/B#	MUX_outputs	Mode
1	1	X	MUX_inputs	Battery
1	0	0	From Non-volatile register(SOPRB)	Performance
1	0	1	From Non-volatile register(SOPRA)	Deeper sleep

Tualatin

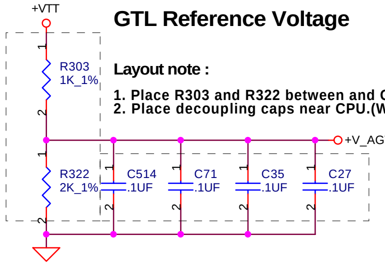
D4	D3	D2	D1	D0	CPU_Core(V)	ES(before MP)
0	0	1	0	1	1.50V	(Performance)
0	1	1	0	0	1.15V	(Battery)
1	0	1	0	1	0.85V	(Deeper Sleep)

D4	D3	D2	D1	D0	CPU_Core(V)	QS(MP)
0	0	1	1	1	1.40V	(Performance)
0	1	1	0	0	1.15V	(Battery)
1	0	1	0	1	0.85V	(Deeper Sleep)

GTL Reference Voltage

Layout note :

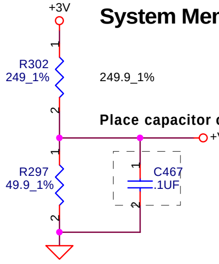
1. Place R303 and R322 between and GMCH and CPU
2. Place decoupling caps near CPU.(Within 500mils)



System Memory Reference

249.9_1%

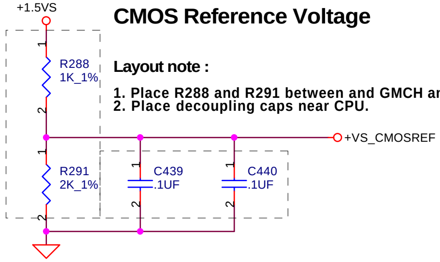
Place capacitor close to GMCH.



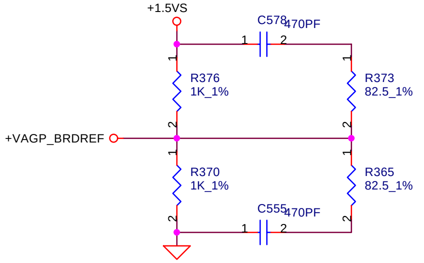
CMOS Reference Voltage

Layout note :

1. Place R288 and R291 between and GMCH and CPU
2. Place decoupling caps near CPU.



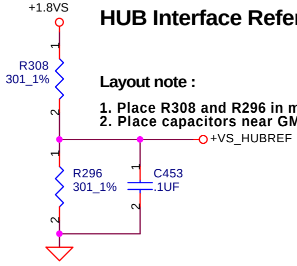
Place Reference Circuit near GMCH



HUB Interface Reference

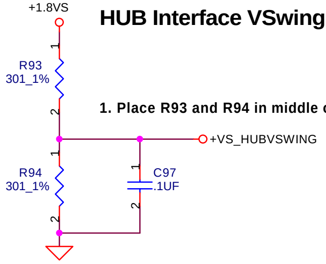
Layout note :

1. Place R308 and R296 in middle of Bus.
2. Place capacitors near GMCH.

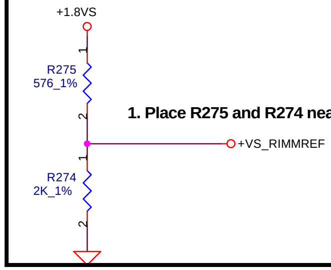


HUB Interface VSwing Voltage

1. Place R93 and R94 in middle of Bus.



1. Place R275 and R274 near GMCH.



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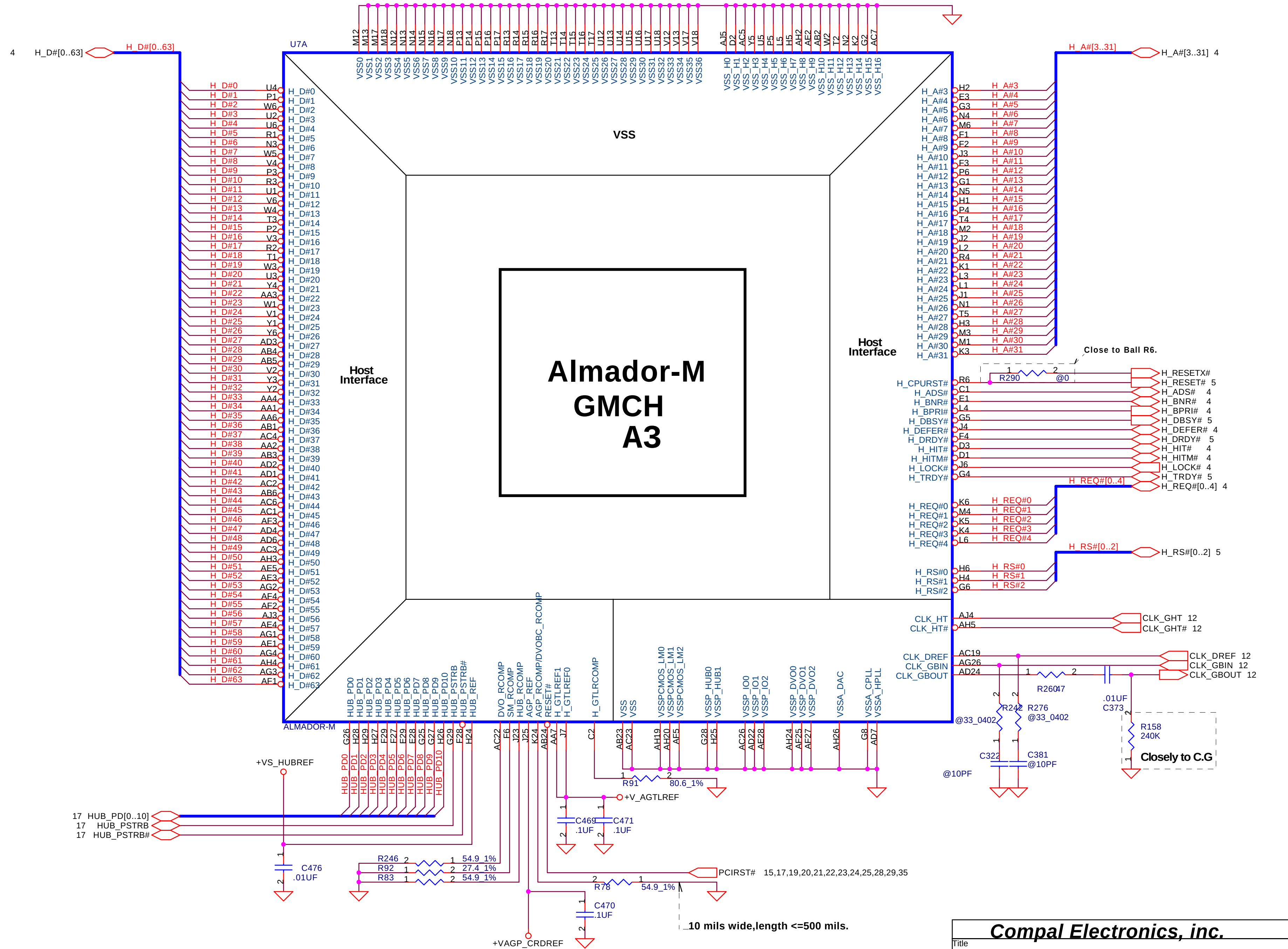

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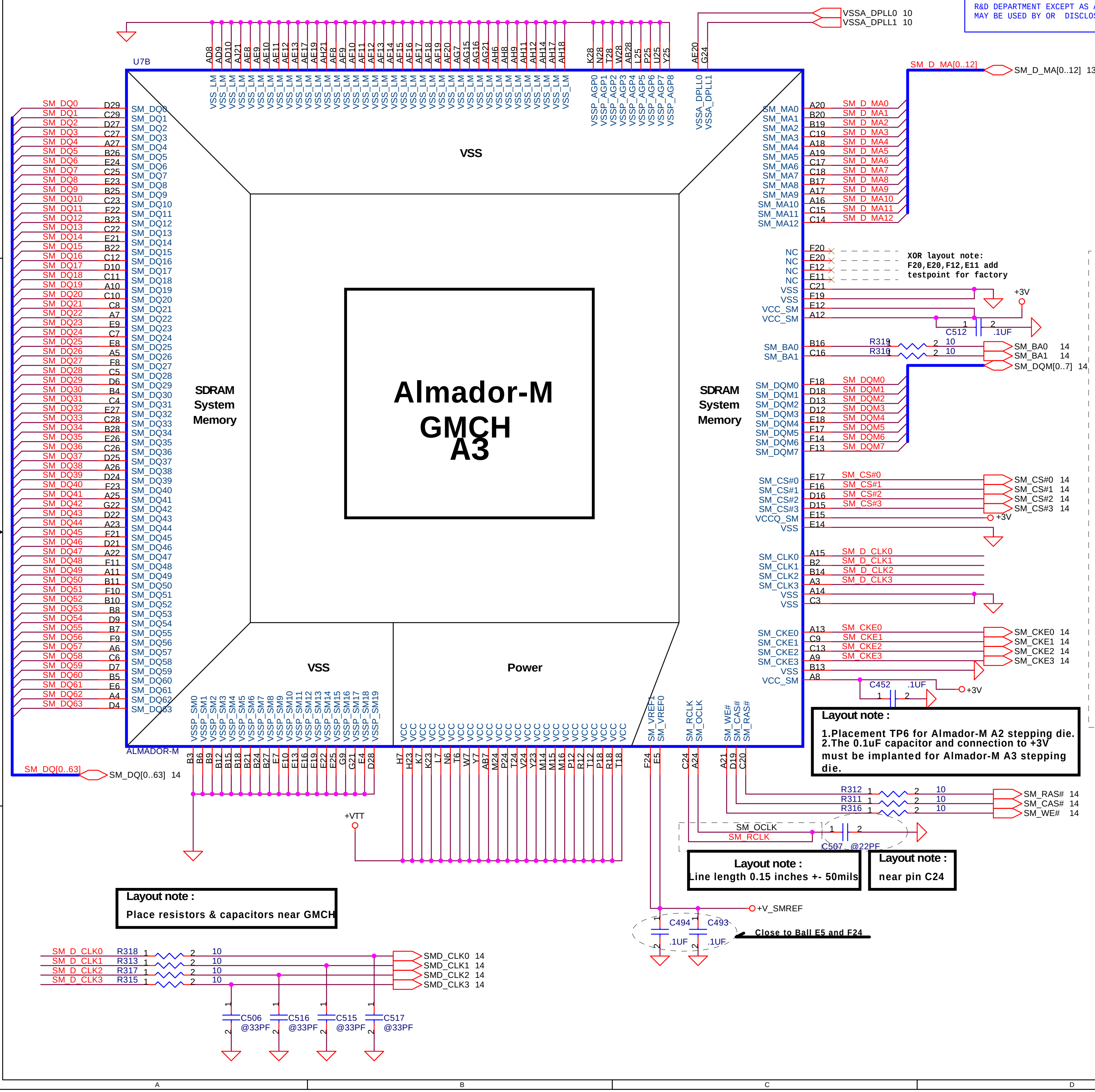

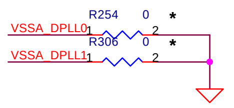

For Almador-M A3 stepping requirement.

The table below provides a summary of the ballout changes to the Almador-M chip.

Table 4-1 Ballout Changes

Ball#.	New Signal Name.	Old Signal Name.
A8.	VCC_SM.	SM_CKE5.
A12.	VCC_SM.	SM_ECC7.
E12.	VCC_SM.	SM_ECC6.
G10.	VCC_SM.	VCCQ_SM.
F7.	VCCQ_SM.	VCC_SM.
G19.	VCCQ_SM.	VCC_SM.
E15.	VCCQ_SM.	SM_CS4.
F15.	VCCQ_SM.	VCC_SM.
A14.	VSS.	SM_CLK4.
B13.	VSS.	SM_CKE4.
C3.	VSS.	SM_CLK5.
C21.	VSS.	SM_ECC4.
E14.	VSS.	SM_CS5.
F19.	VSS.	SM_ECC5.
E11.	NC.	SM_ECC3.
E20.	NC.	SM_ECC1.
F12.	NC.	SM_ECC2.
F20.	NC.	SM_ECC0.

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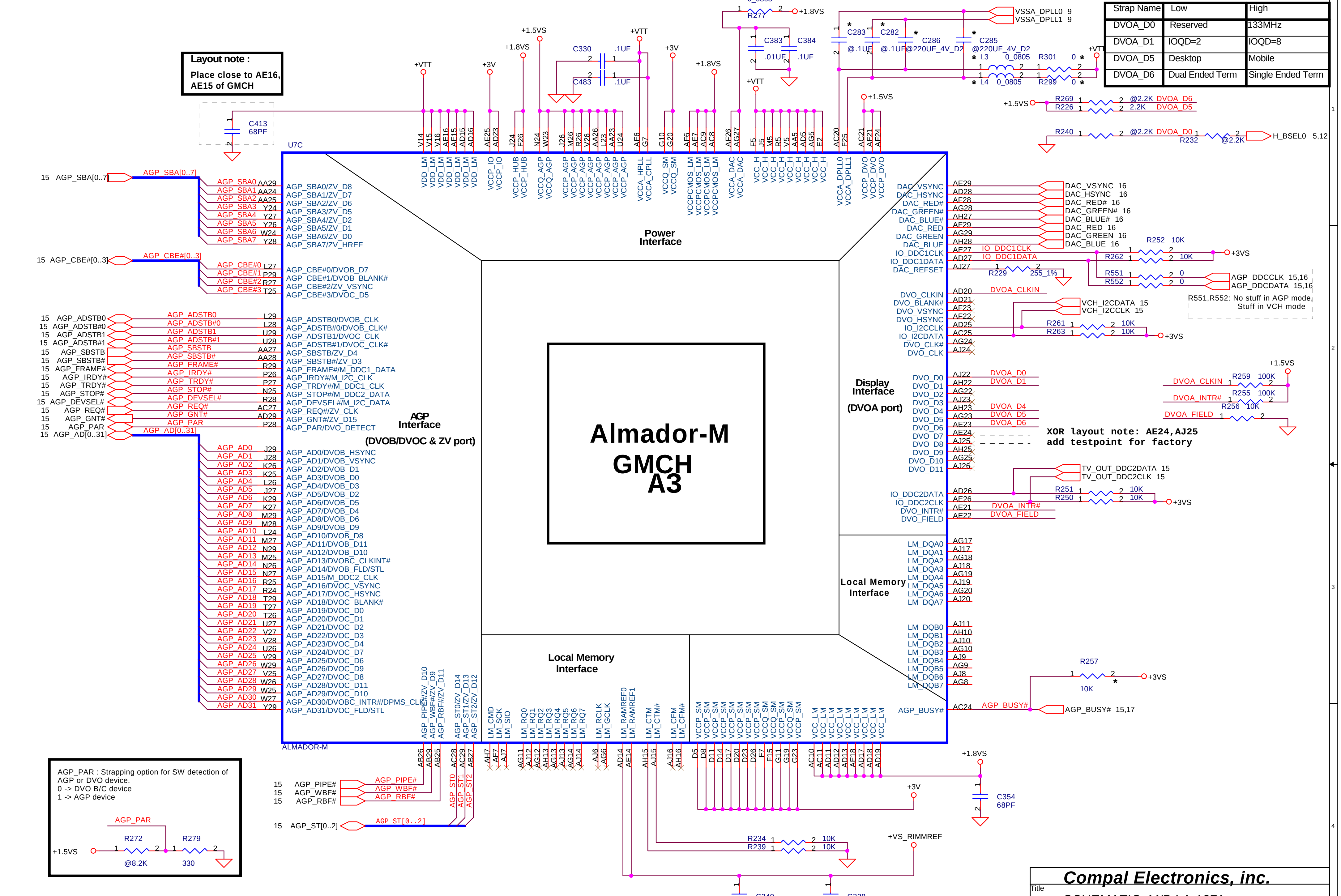

Strap Name	Low	High
DVOA_D0	Reserved	133MHz
DVOA_D1	IOQD=2	IOQD=8
DVOA_D5	Desktop	Mobile
DVOA_D6	Dual Ended Term	Single Ended Term

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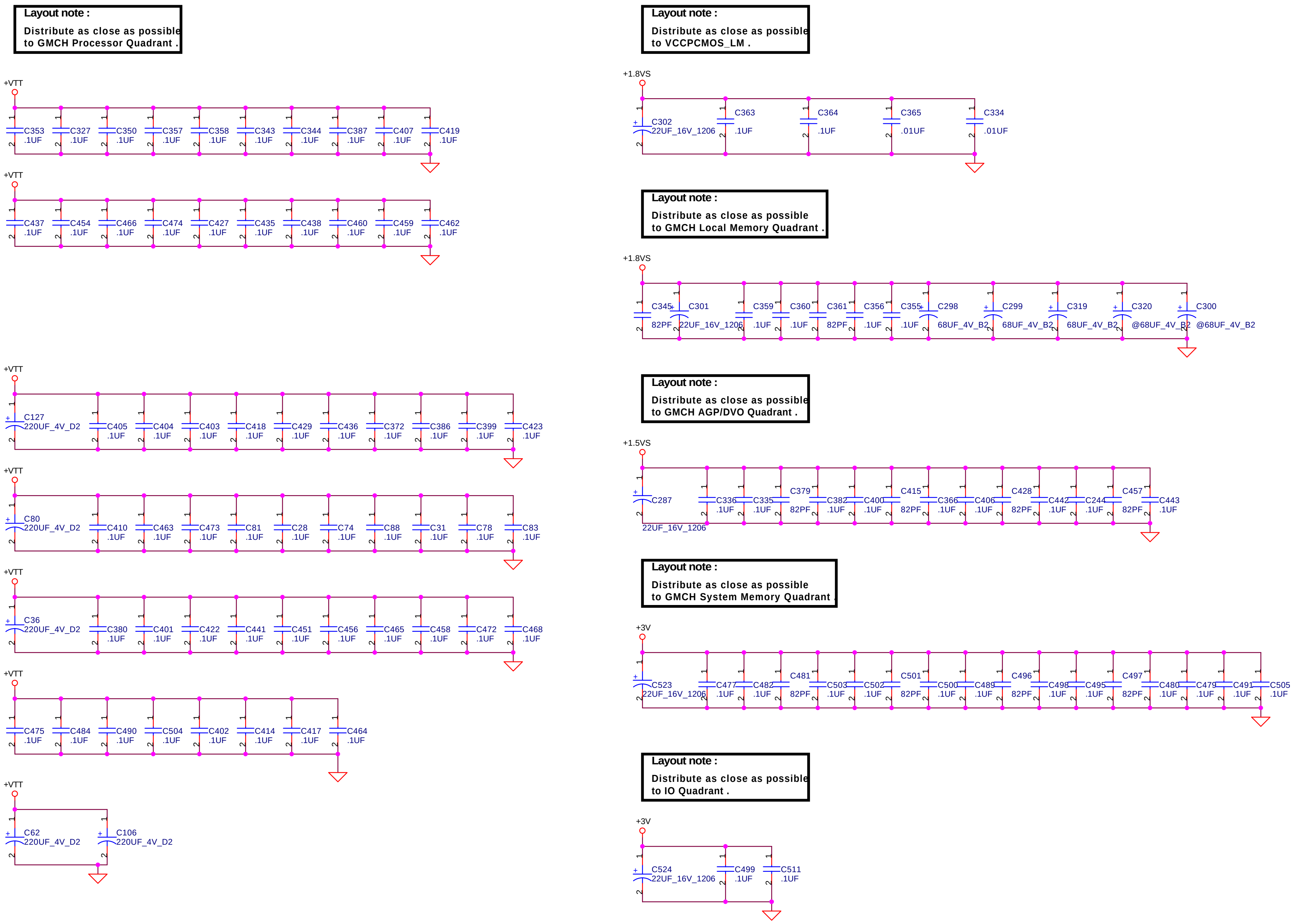

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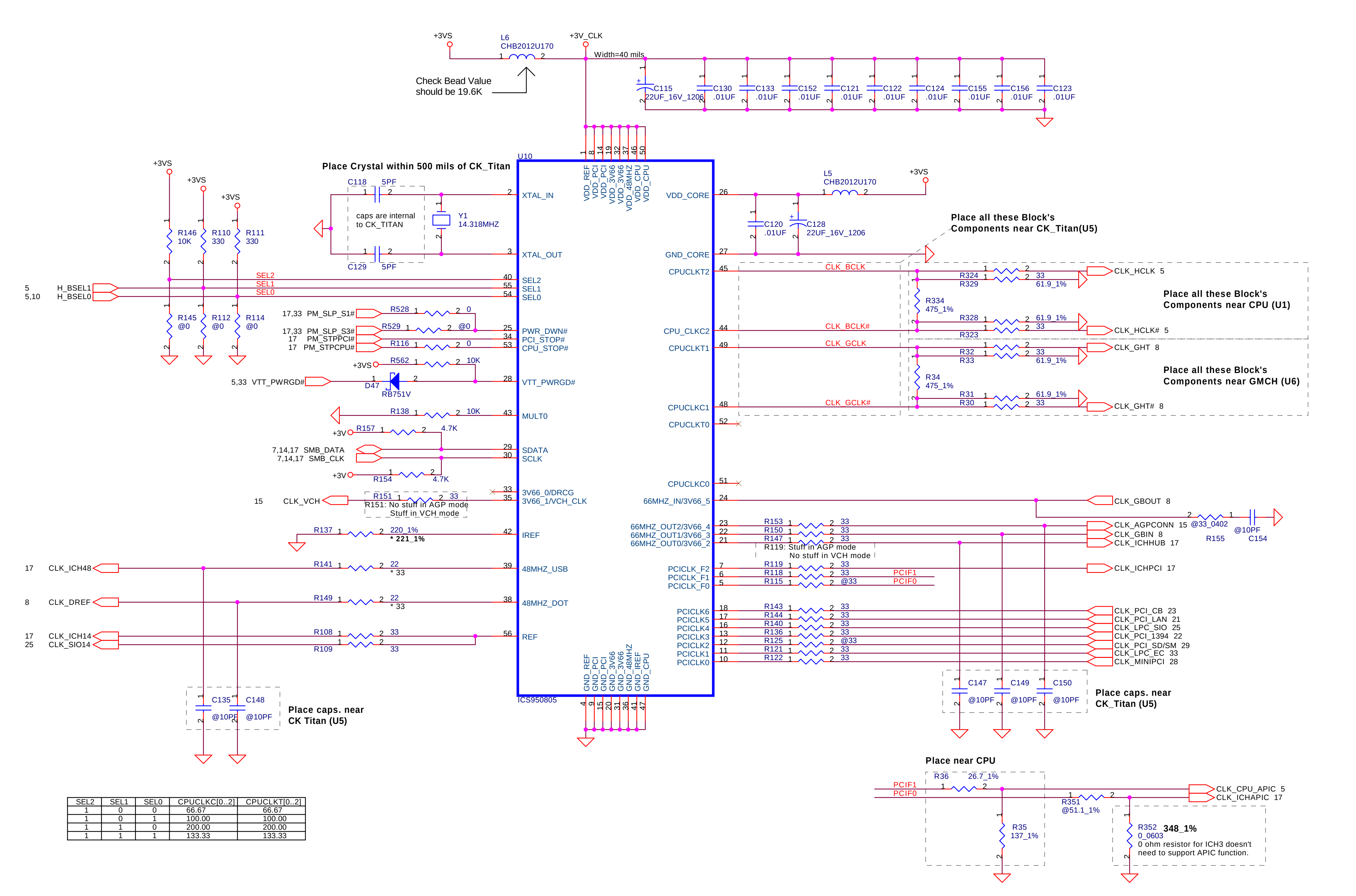

SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
1	0	0	66.67	66.67
1	0	1	100.00	100.00
1	1	0	200.00	200.00
1	1	1	133.33	133.33

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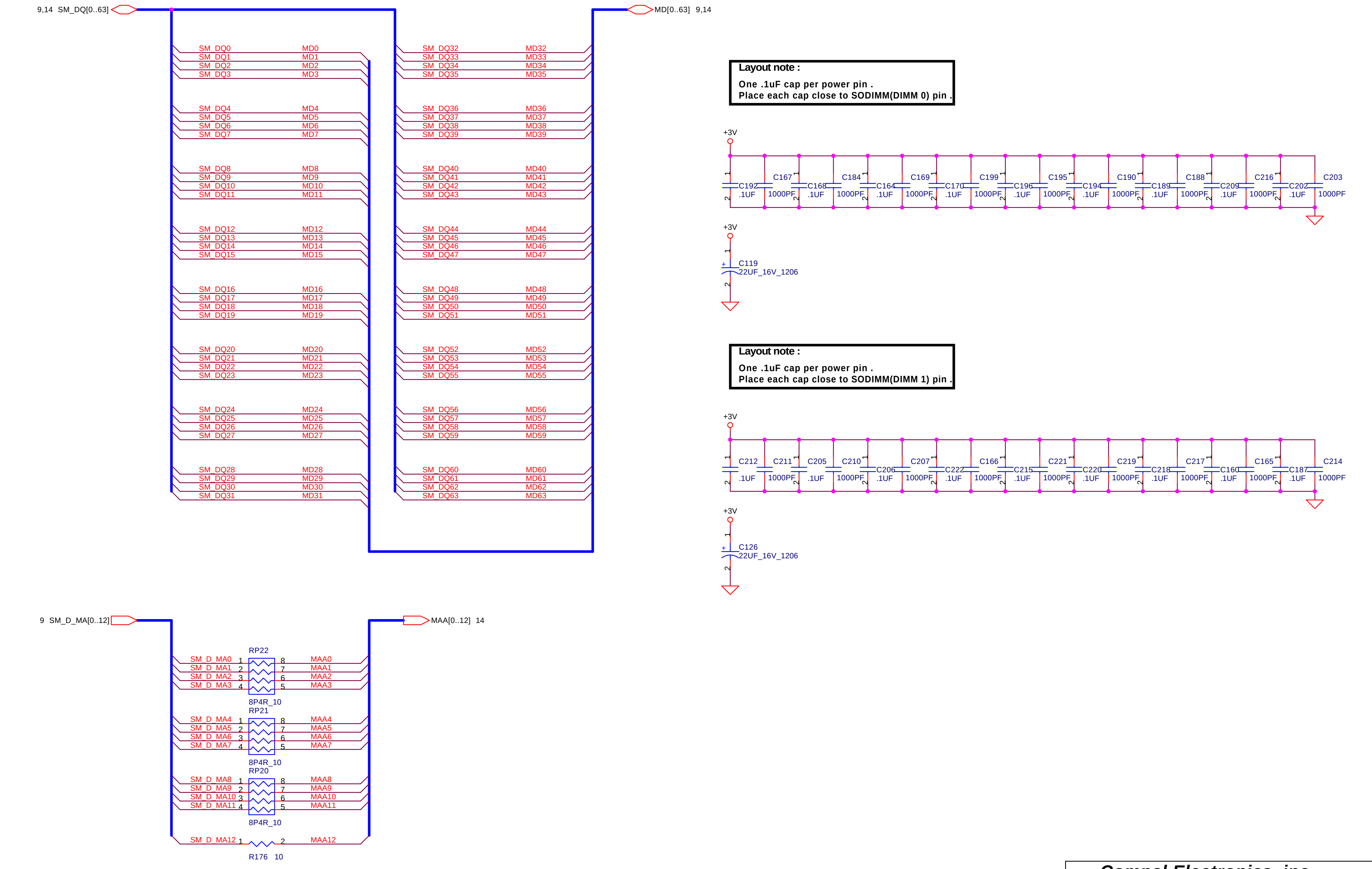

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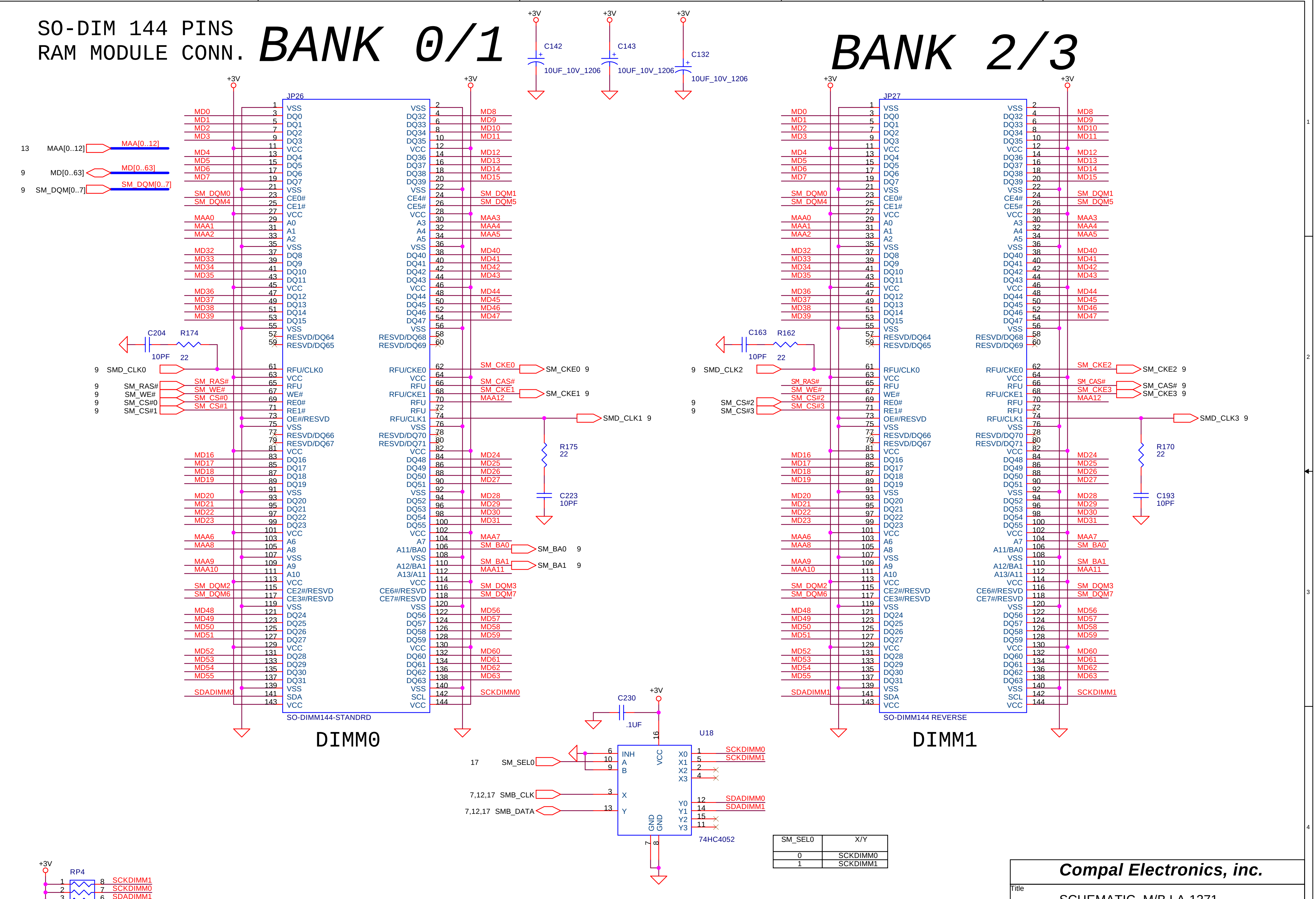

SM_SEL0	X/Y
0	SCKDIMM0
1	SCKDIMM1

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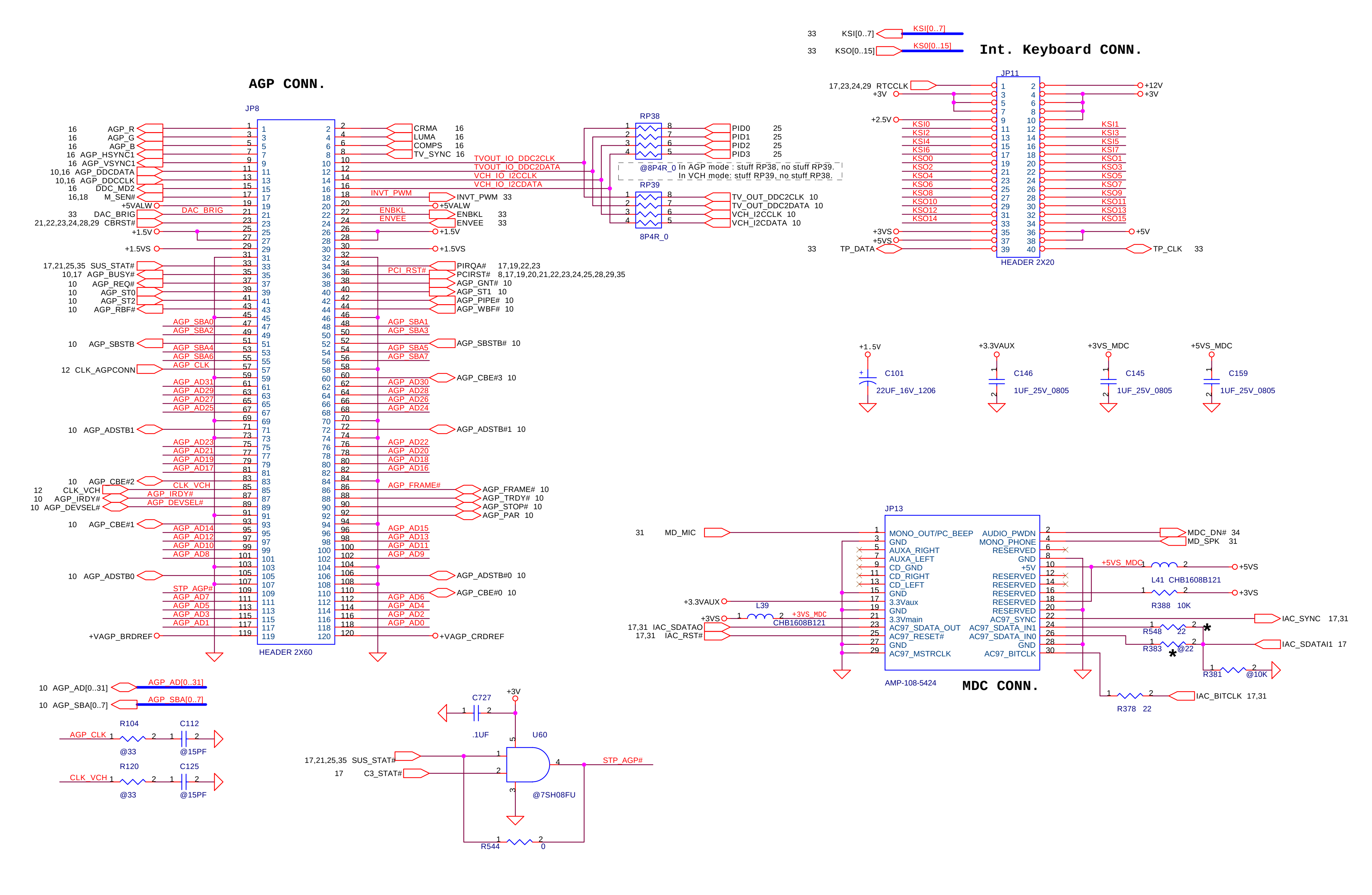

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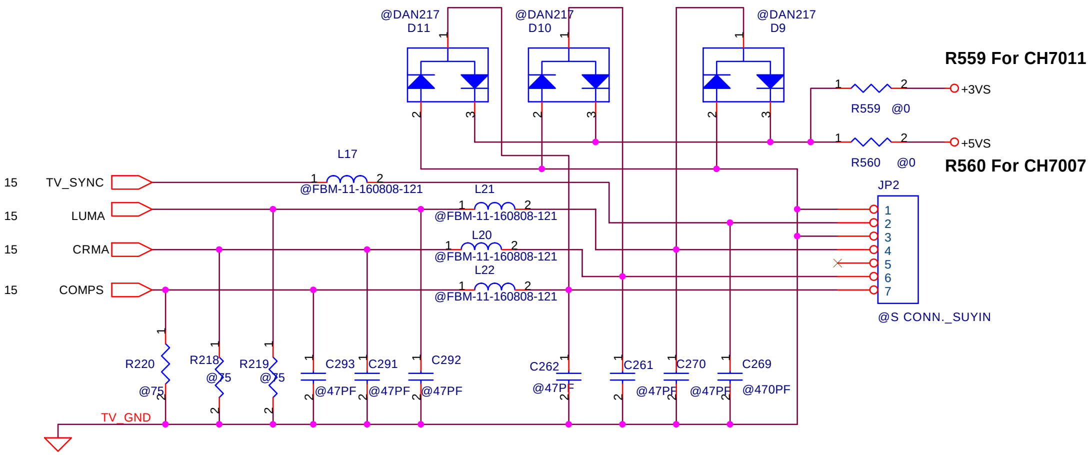
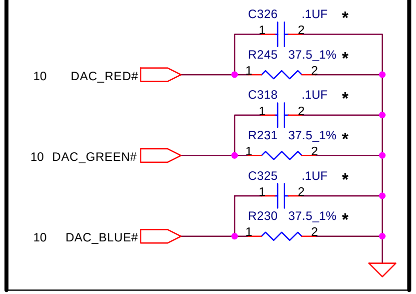
TV_OUT CONN.



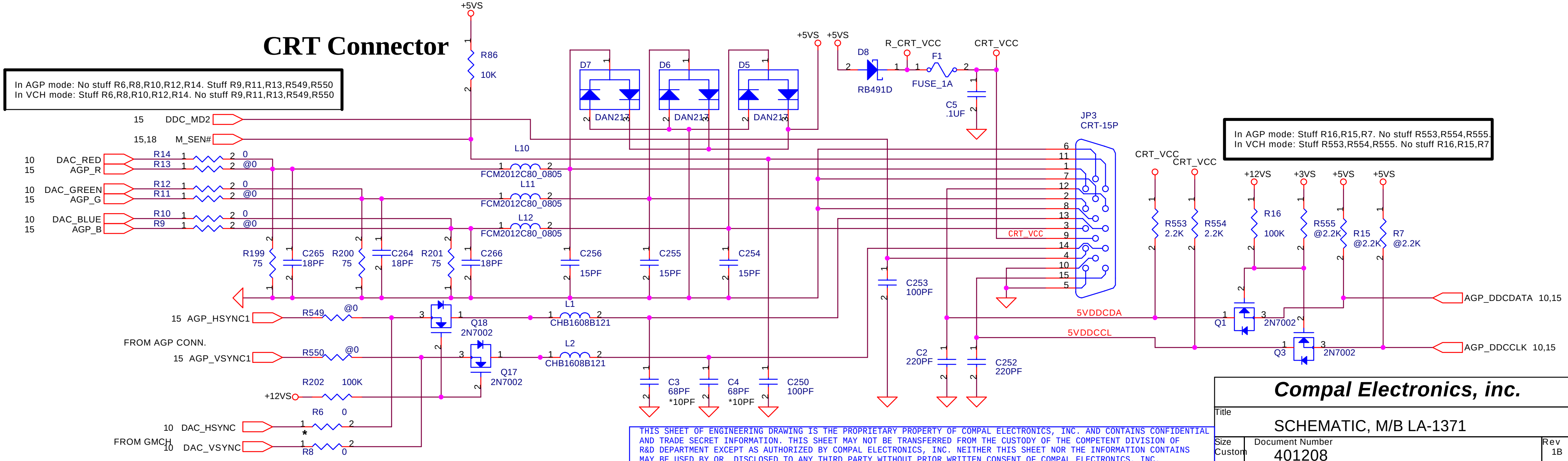
In AGP mode: No stuff C326,R245,C318,R231,C325,R230.
In VCH mode: Stuff C326,R245,C318,R231,C325,R230



CRT Connector

In AGP mode: No stuff R6,R8,R10,R12,R14. Stuff R9,R11,R13,R549,R550
In VCH mode: Stuff R6,R8,R10,R12,R14. No stuff R9,R11,R13,R549,R550

In AGP mode: Stuff R16,R15,R7. No stuff R553,R554,R555.
In VCH mode: Stuff R553,R554,R555. No stuff R16,R15,R7



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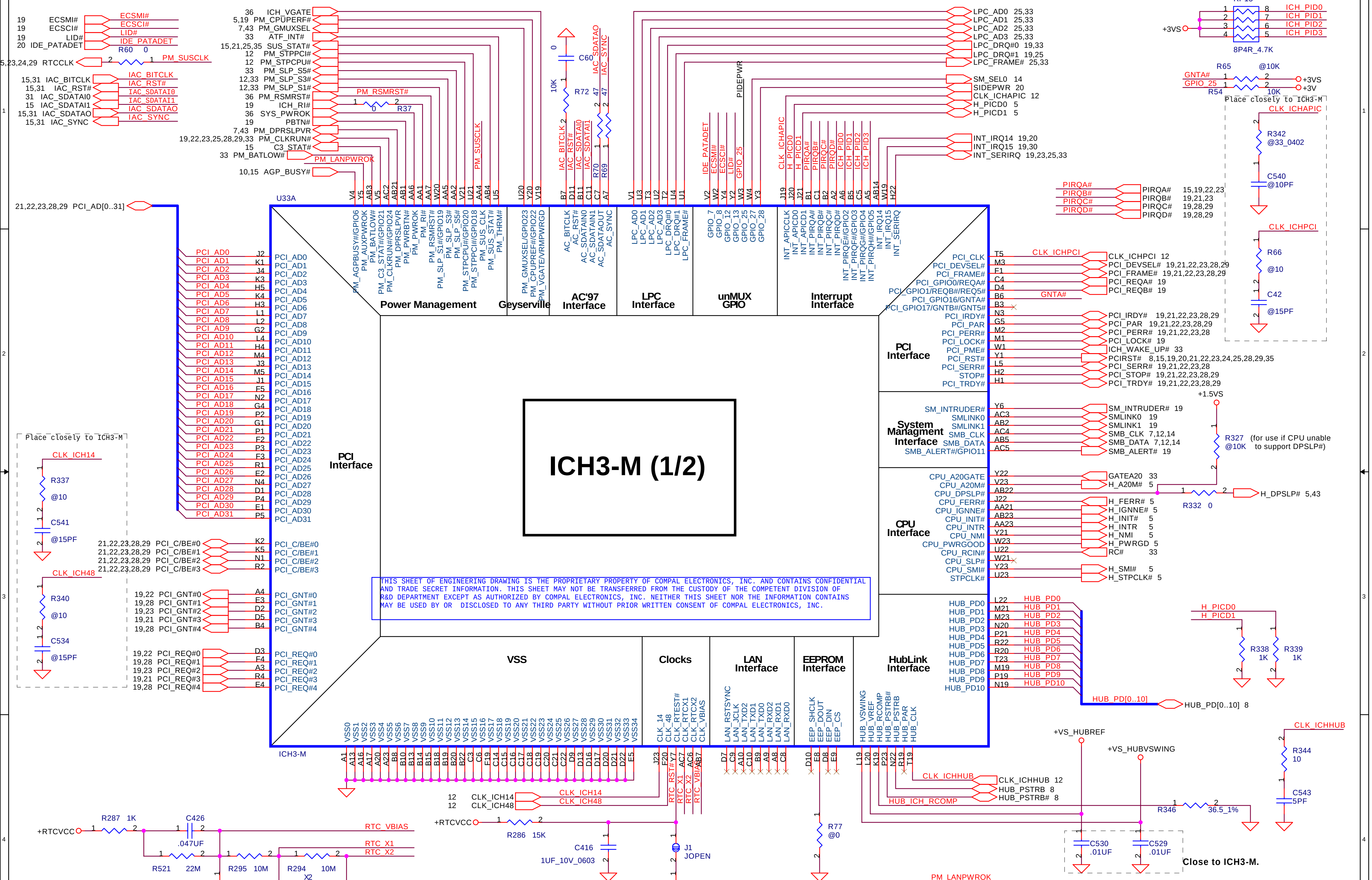

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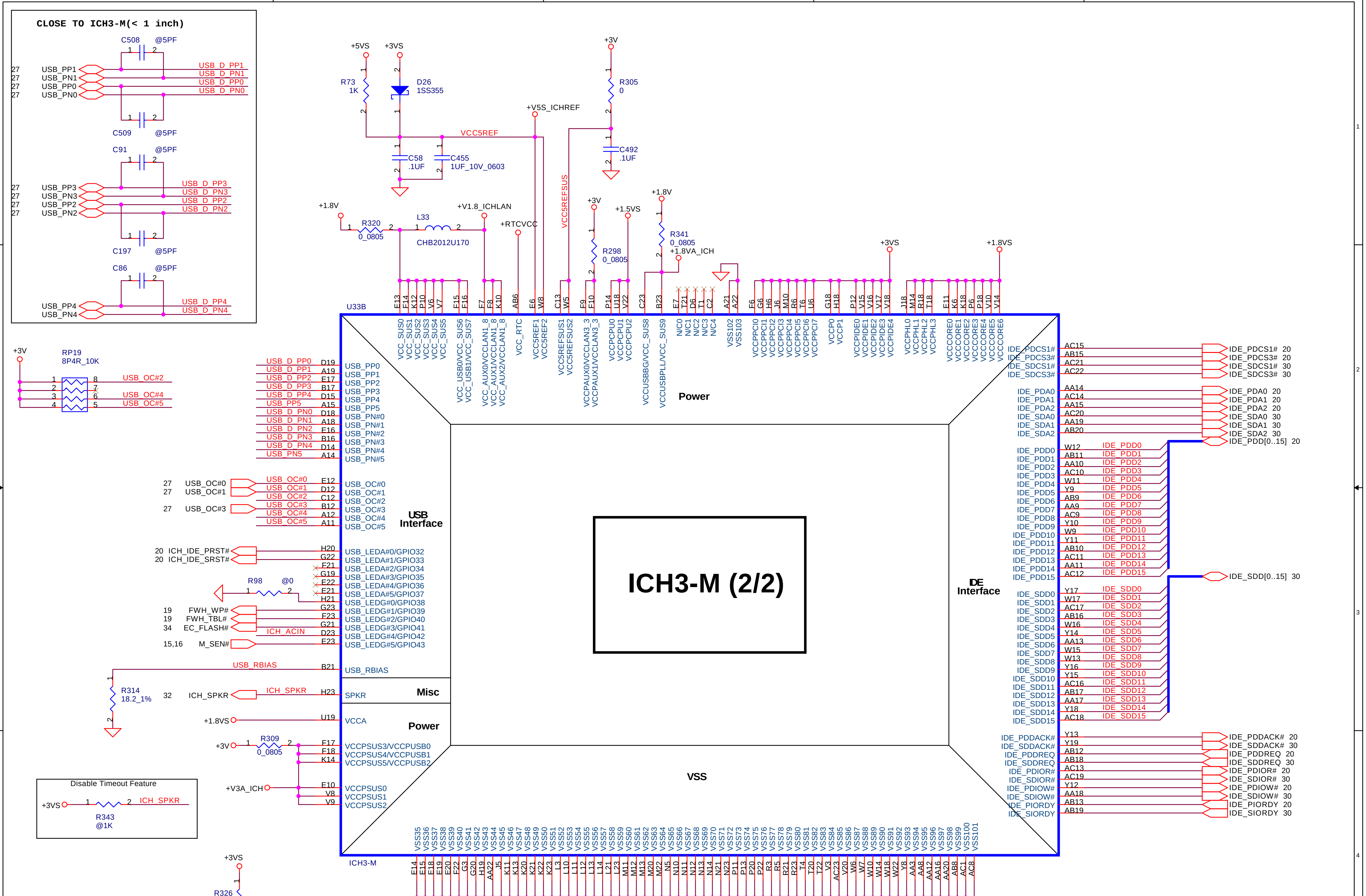

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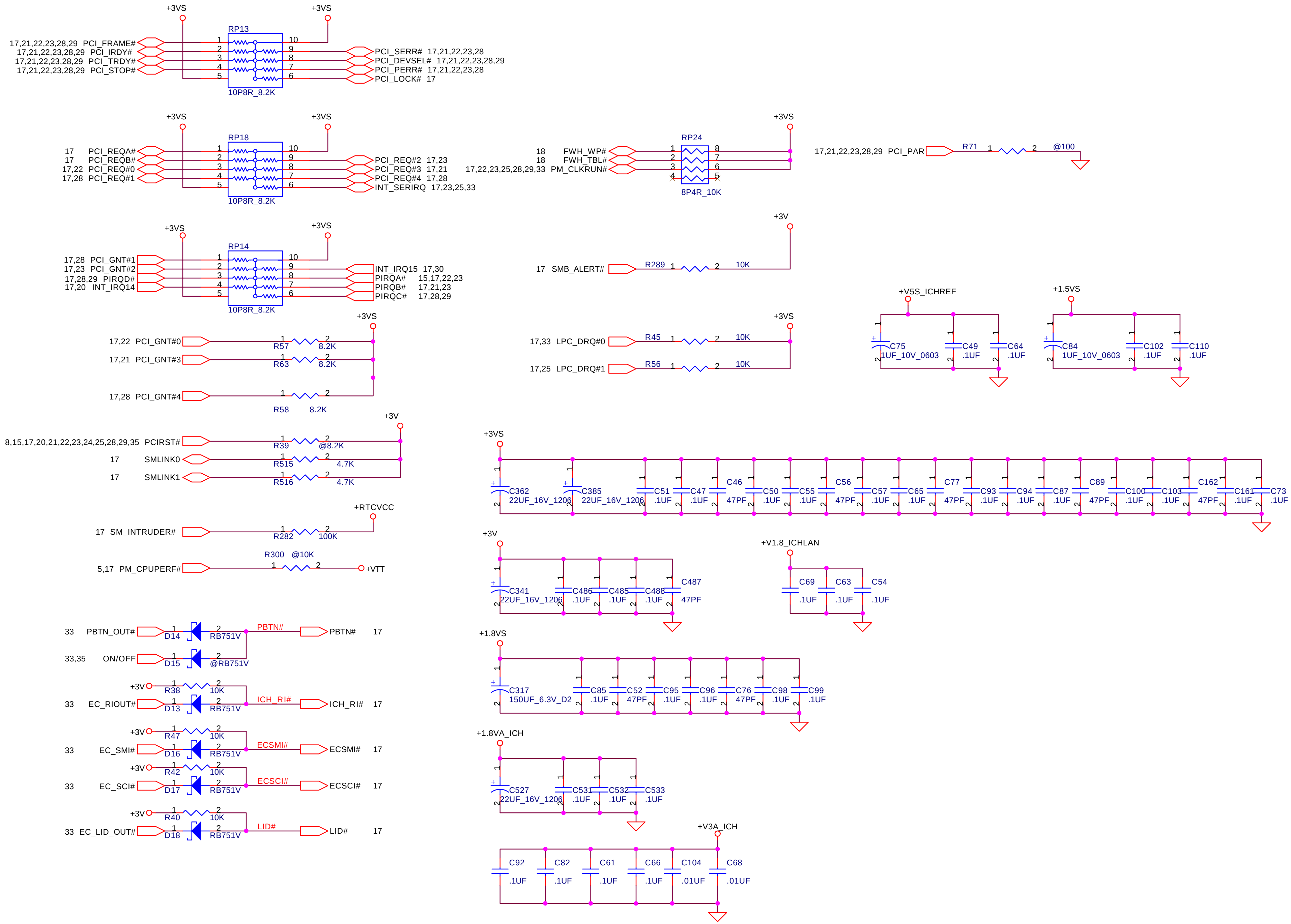

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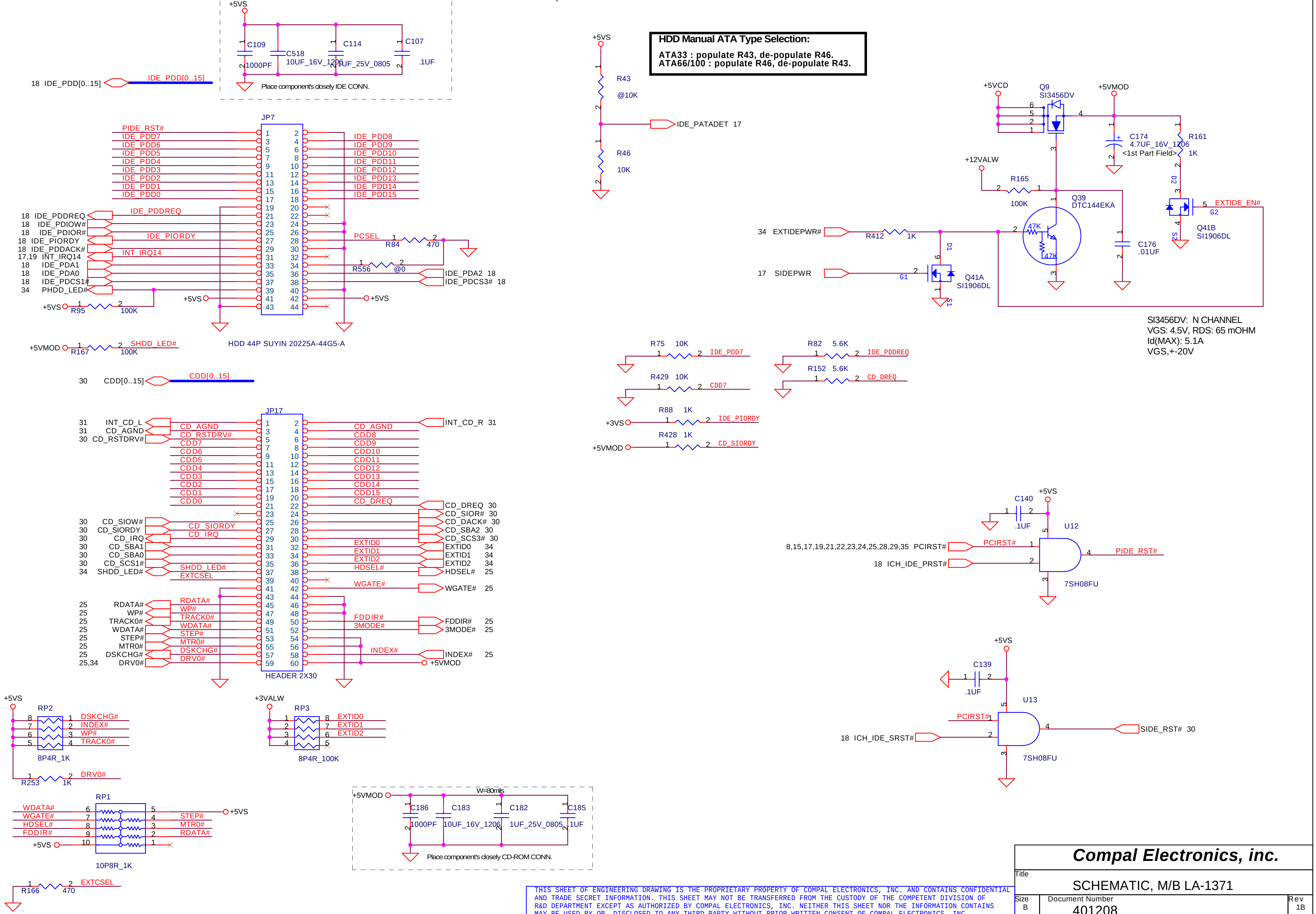
IDE,CD-ROM Module CONN.



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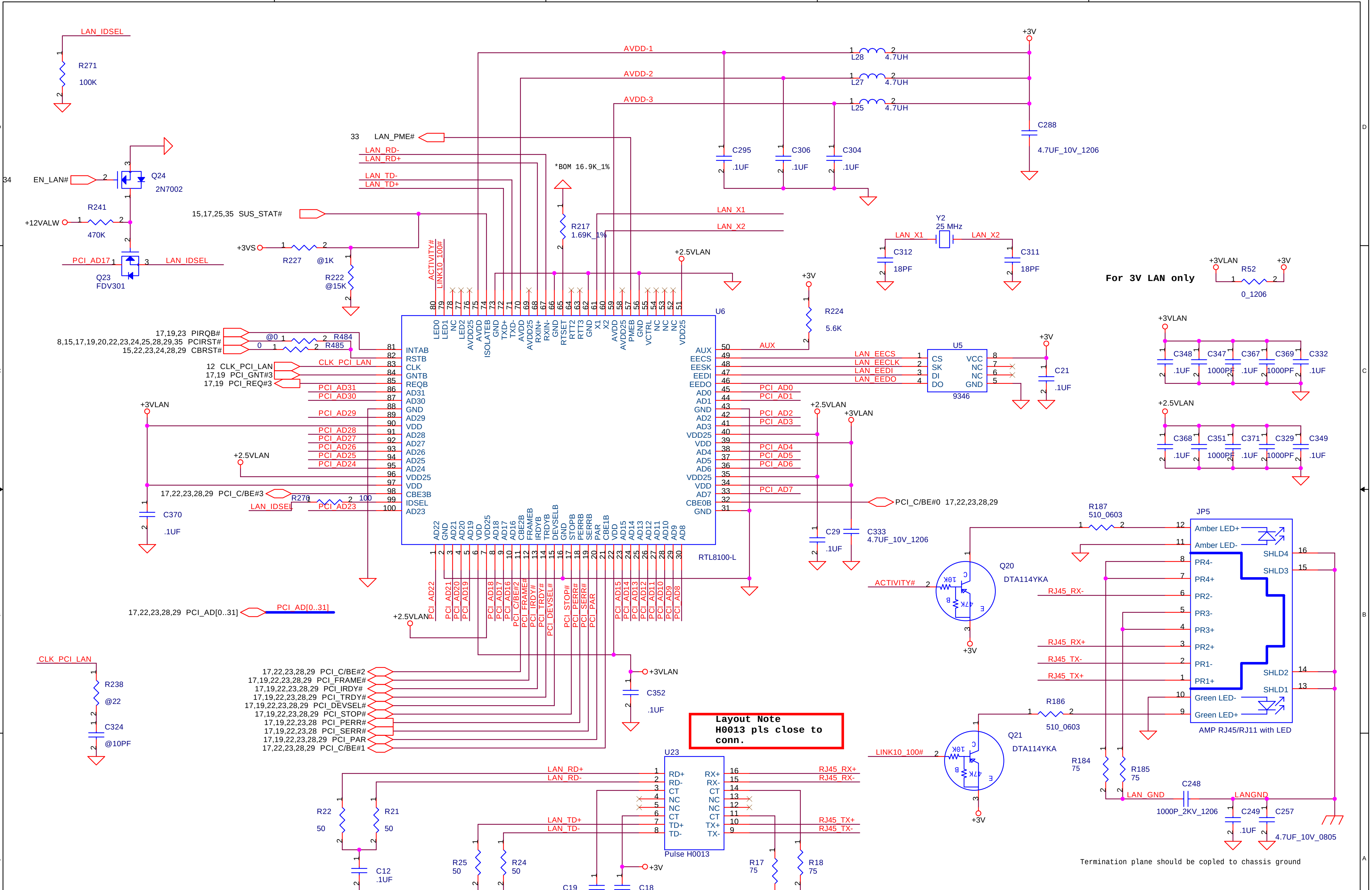

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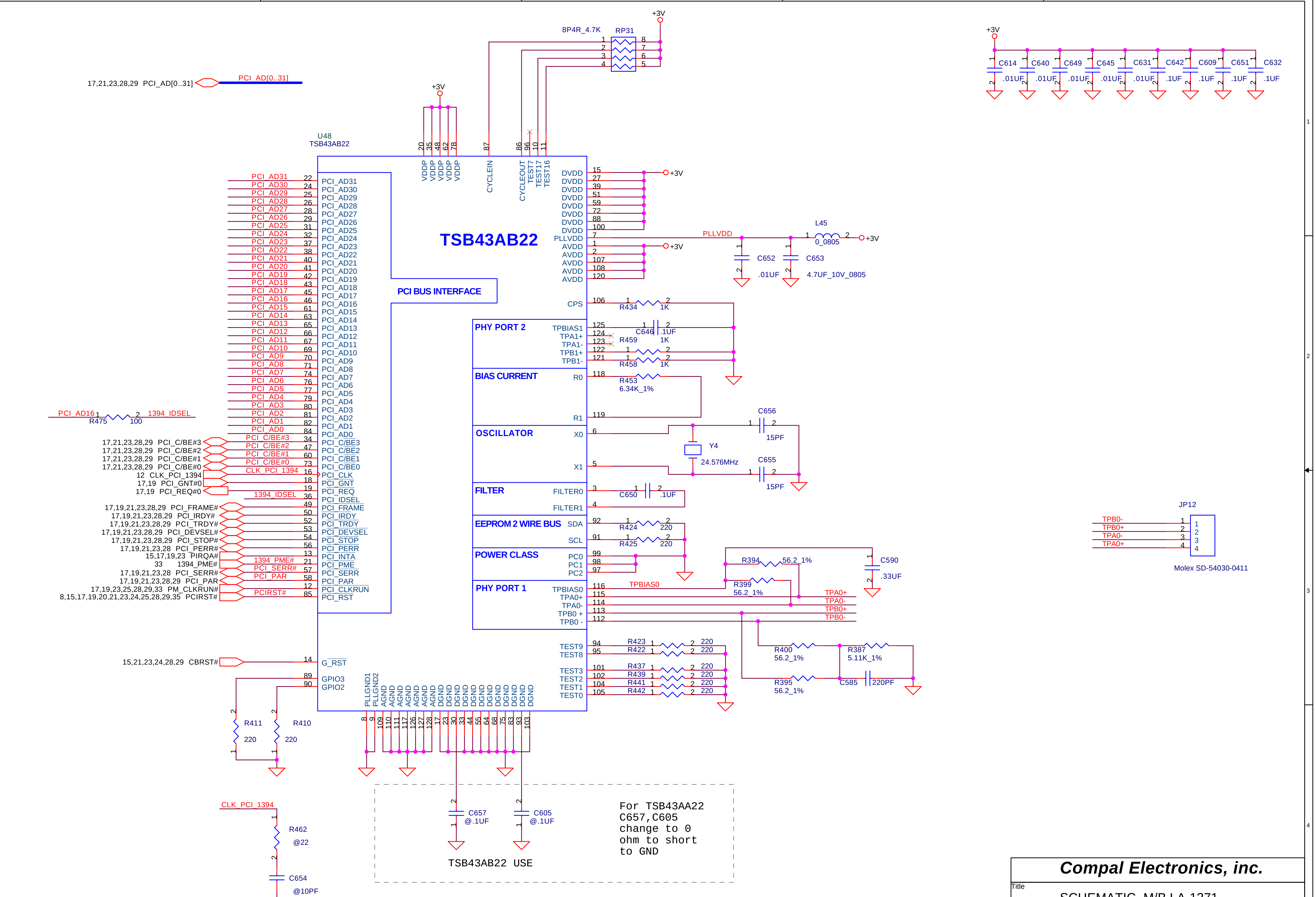

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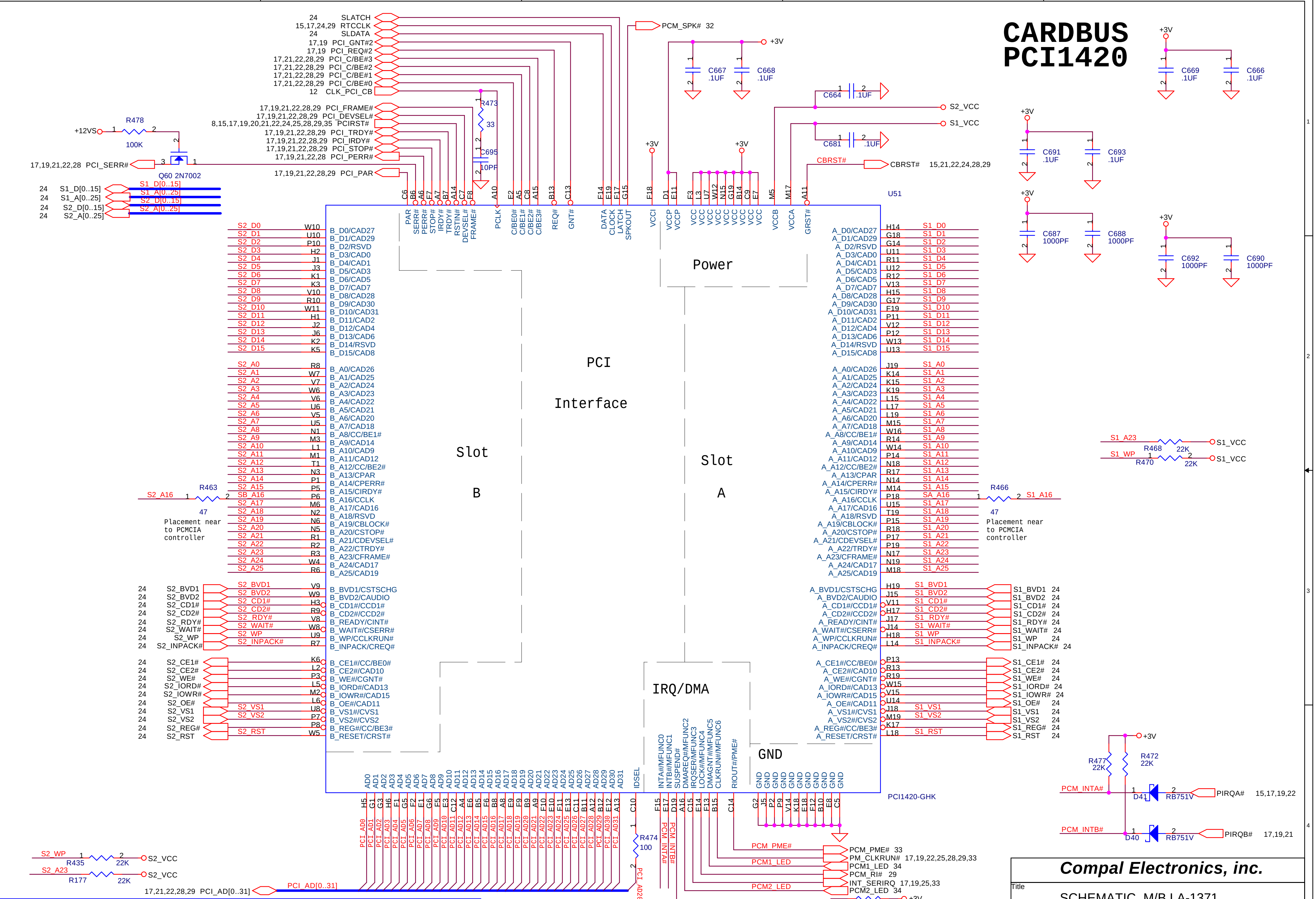

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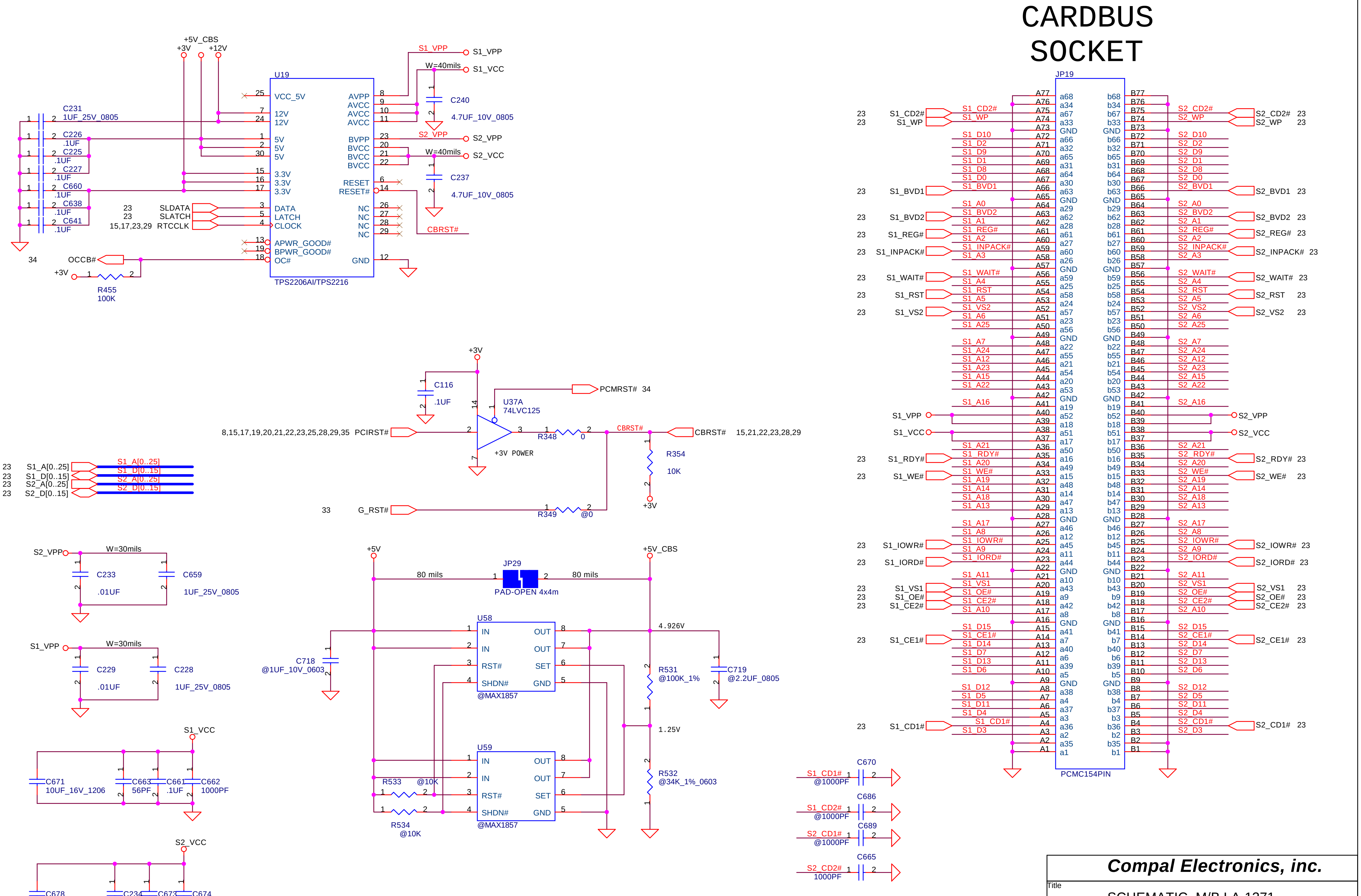
PCMCIA POWER CTRL.



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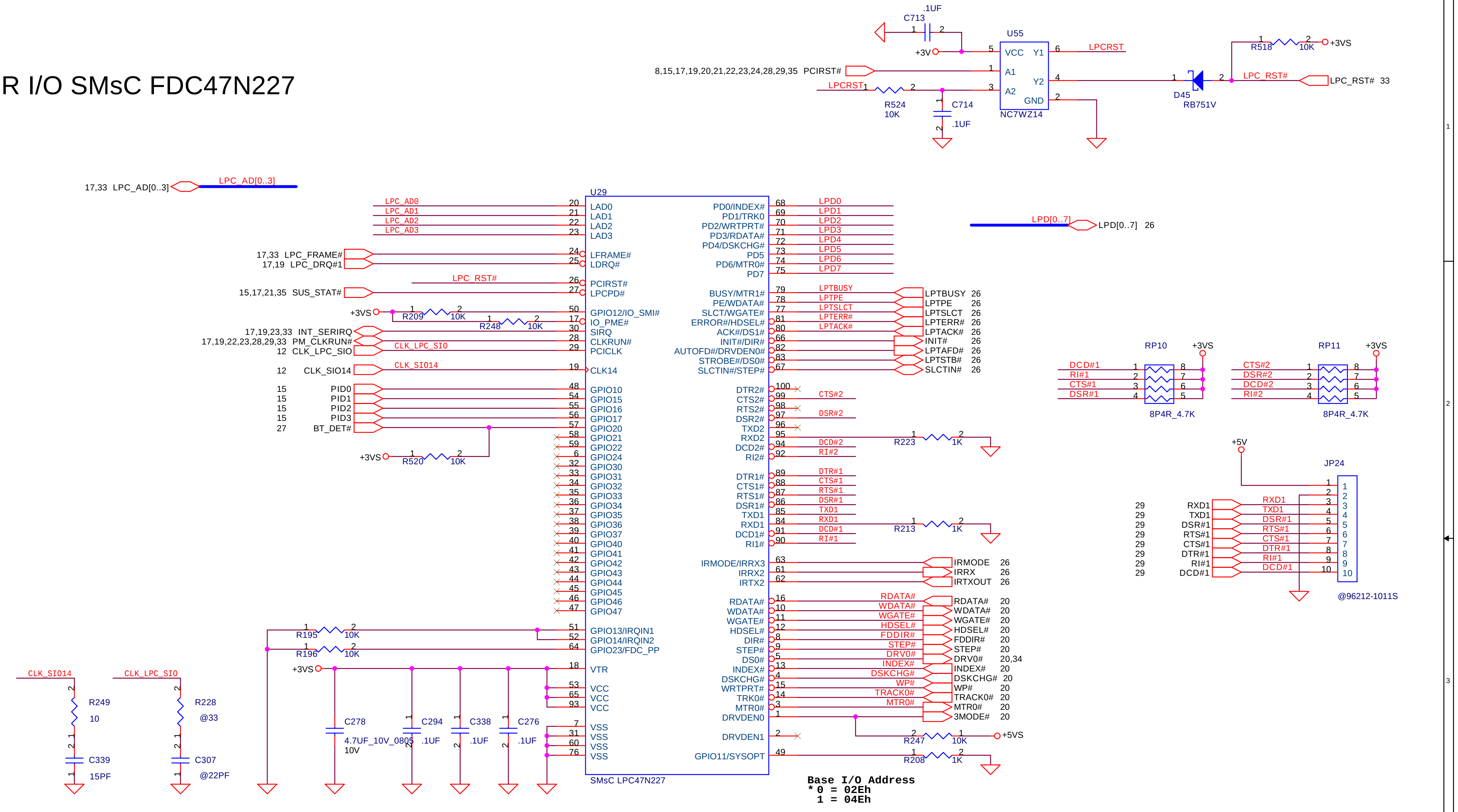
SUPER I/O SMsC FDC47N227



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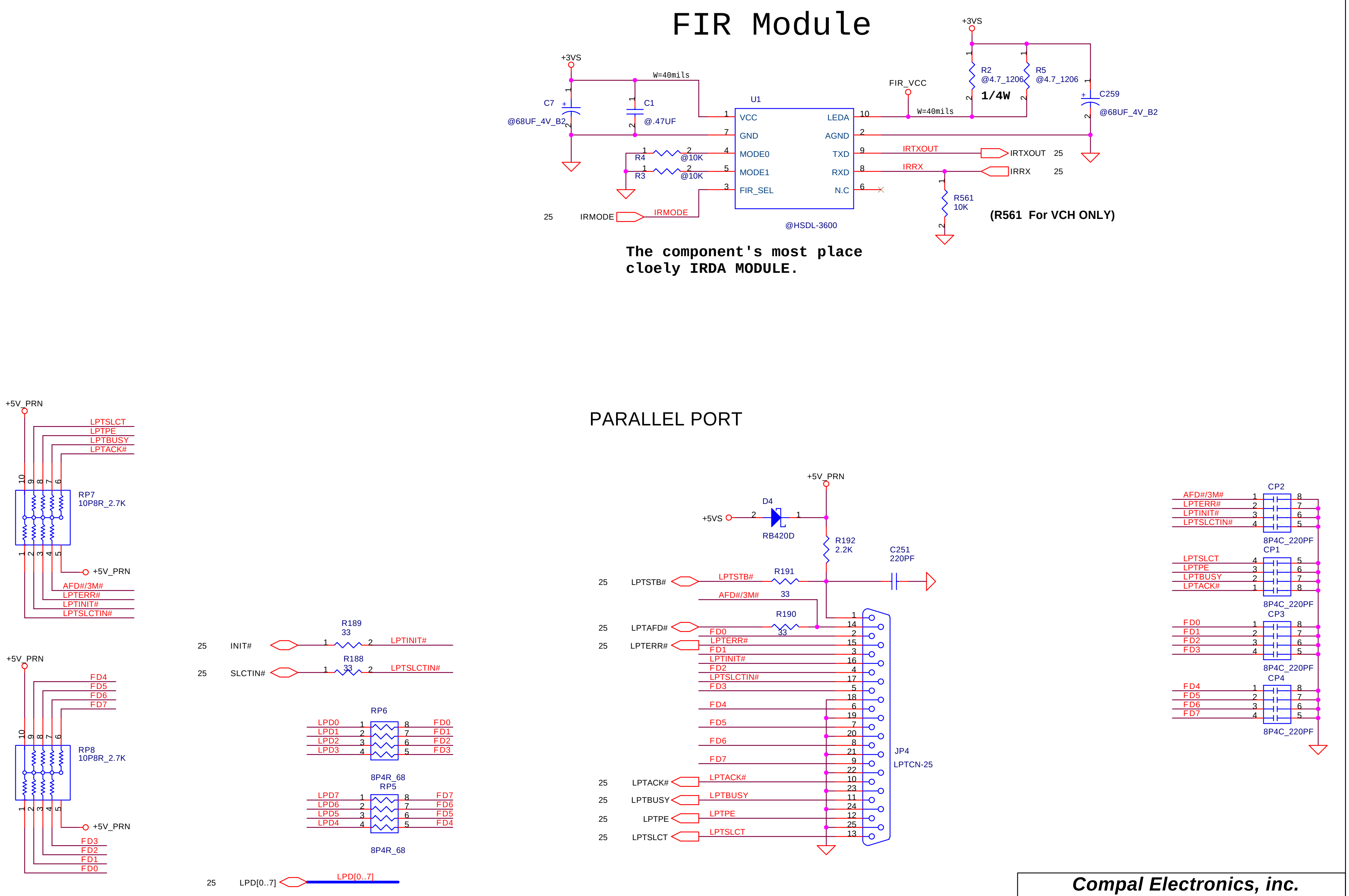

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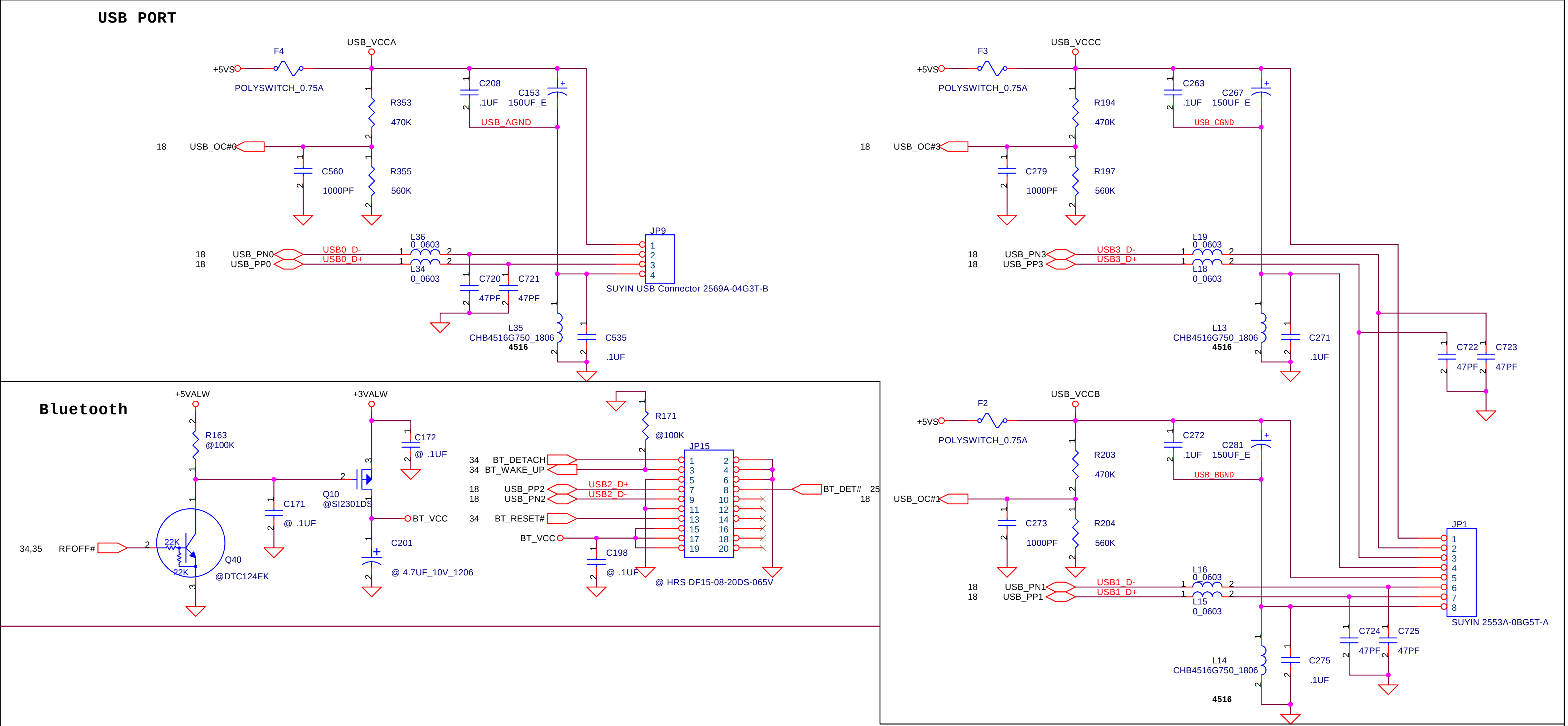

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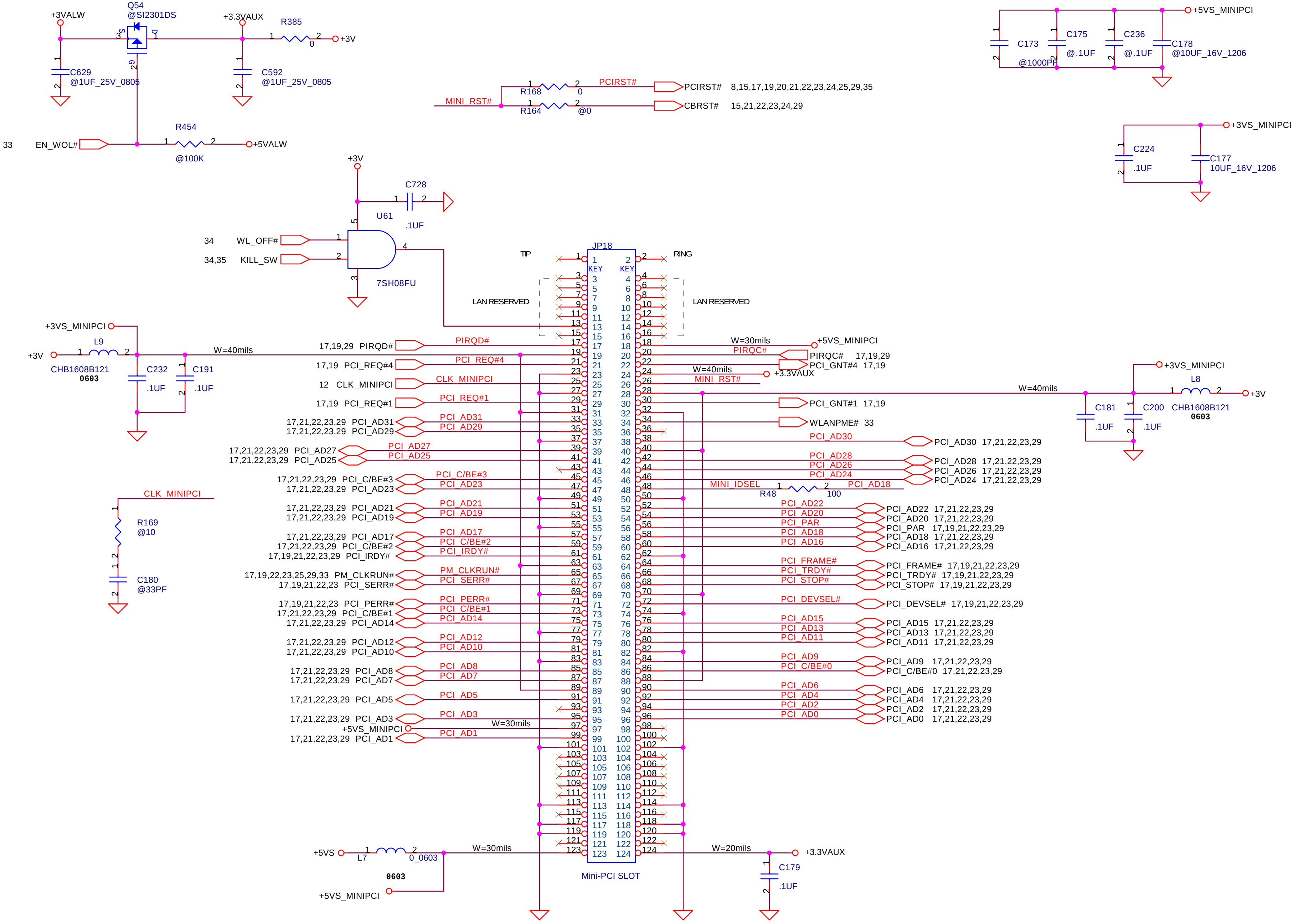

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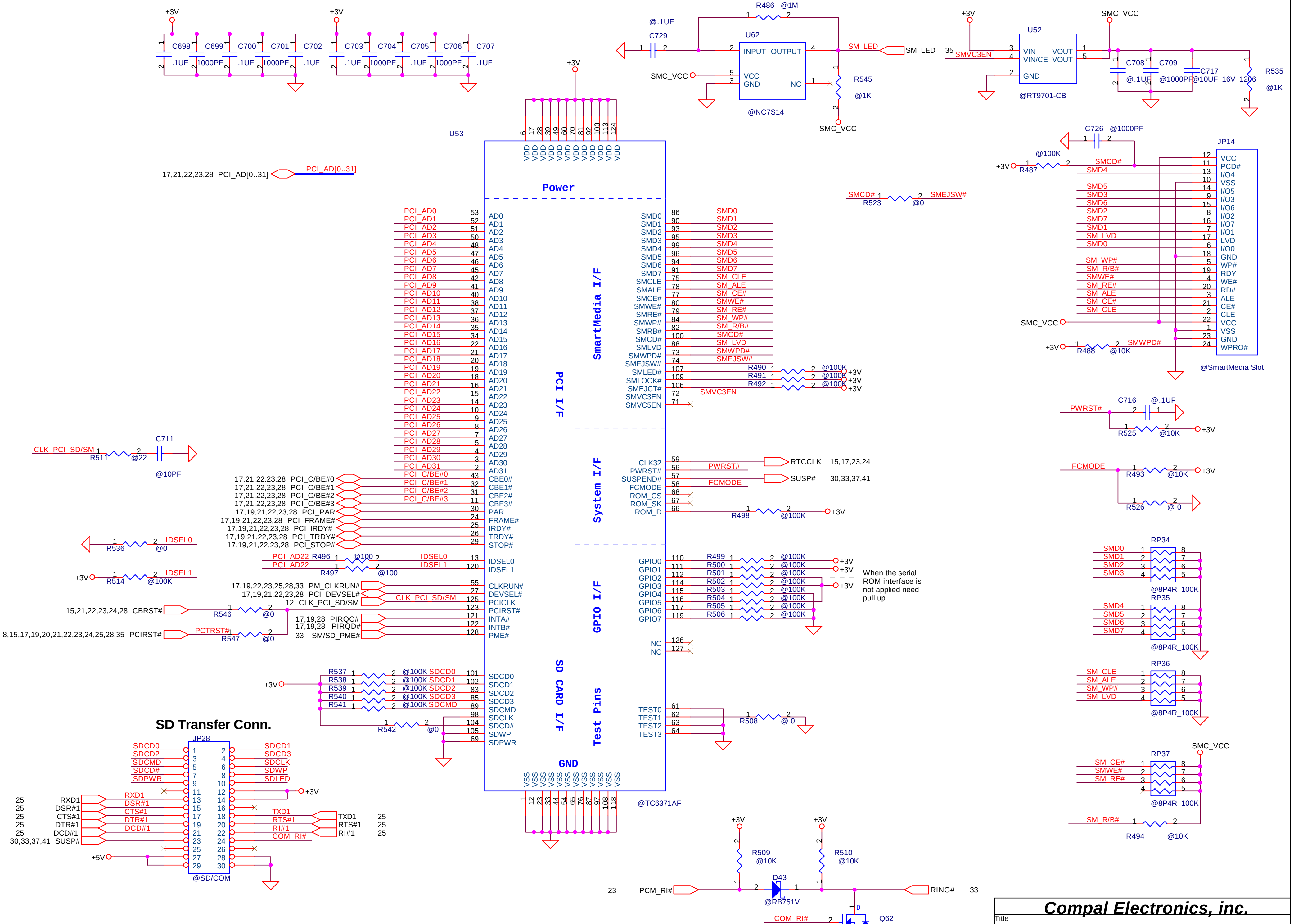

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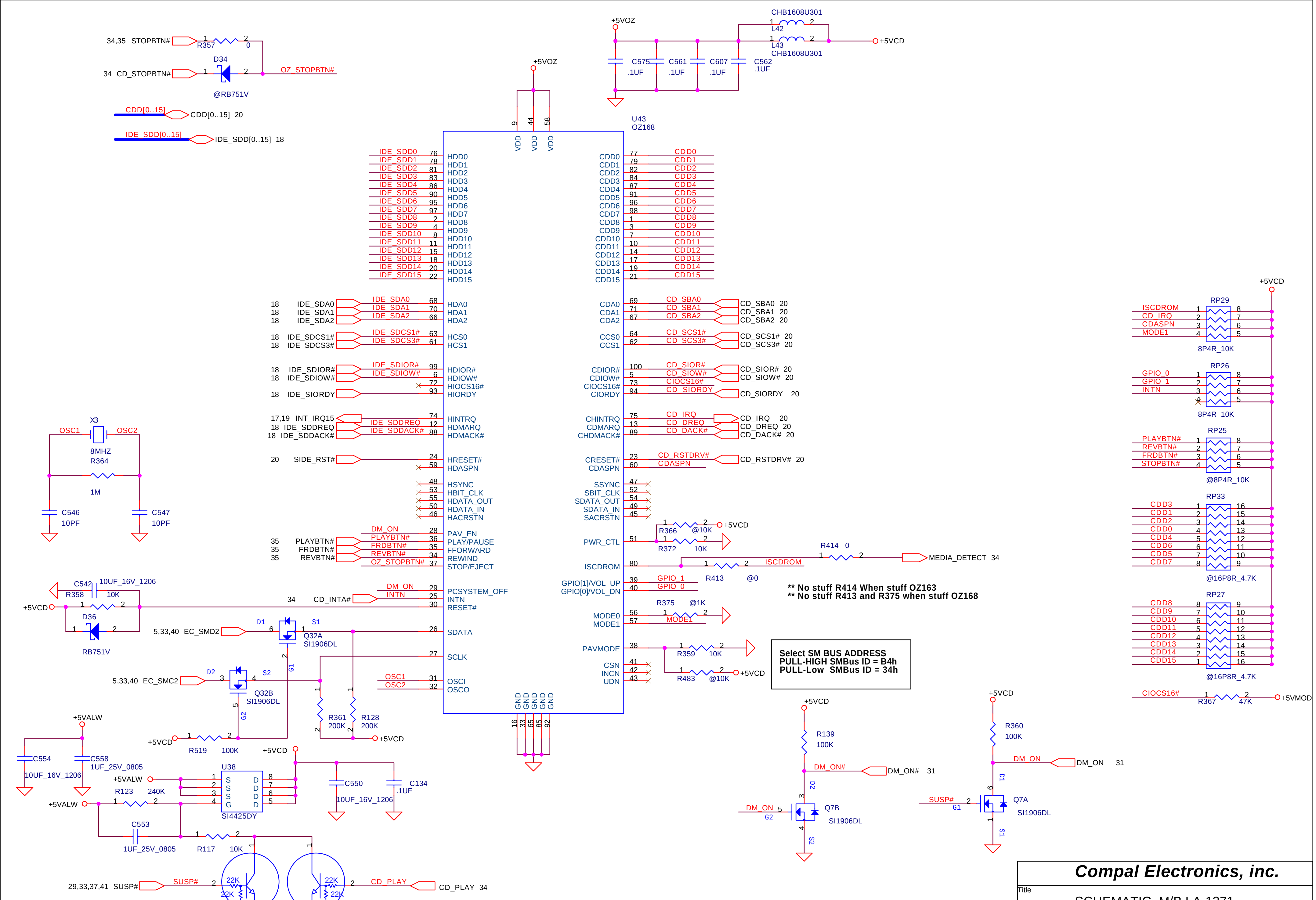

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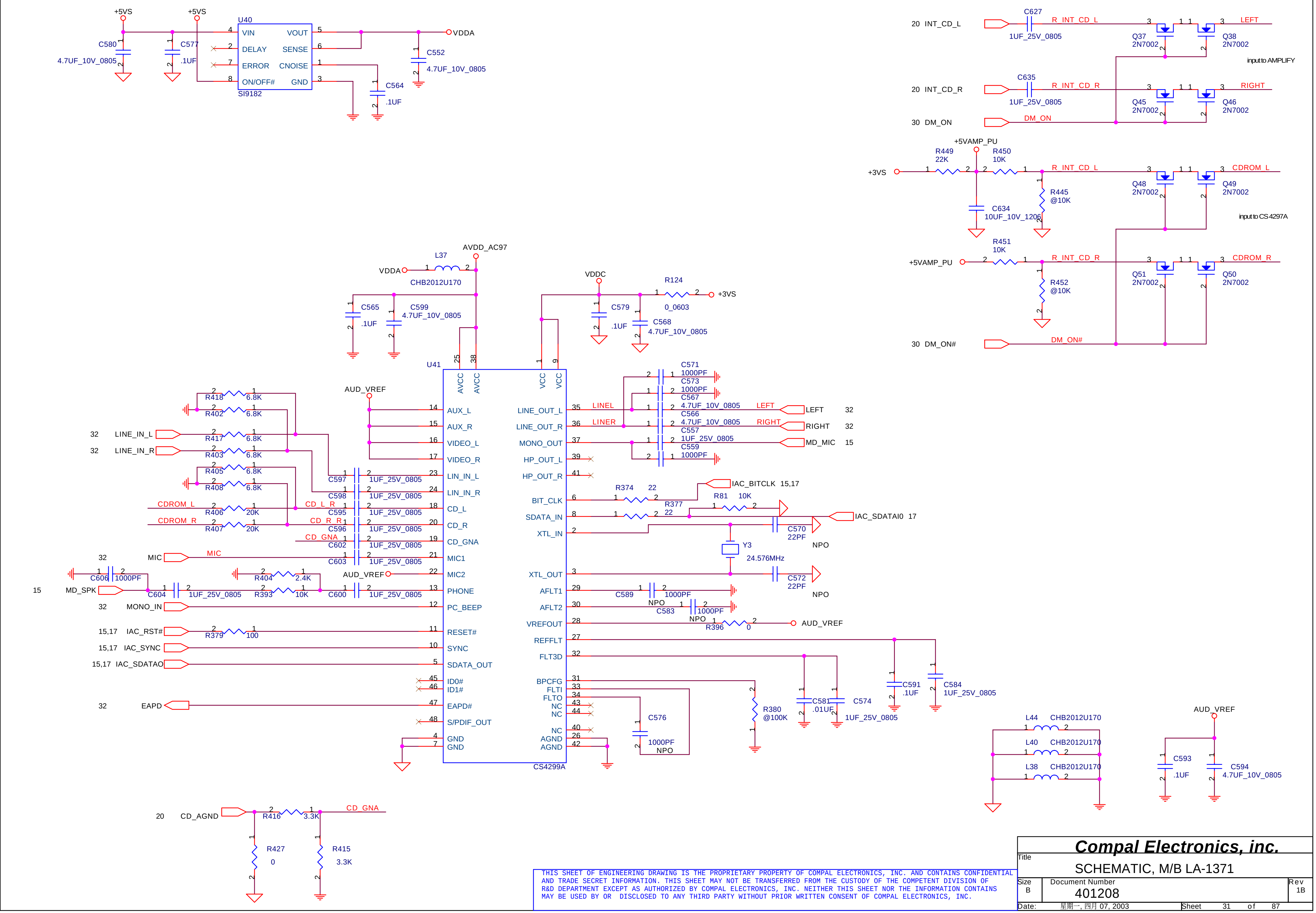
AC97 Codec



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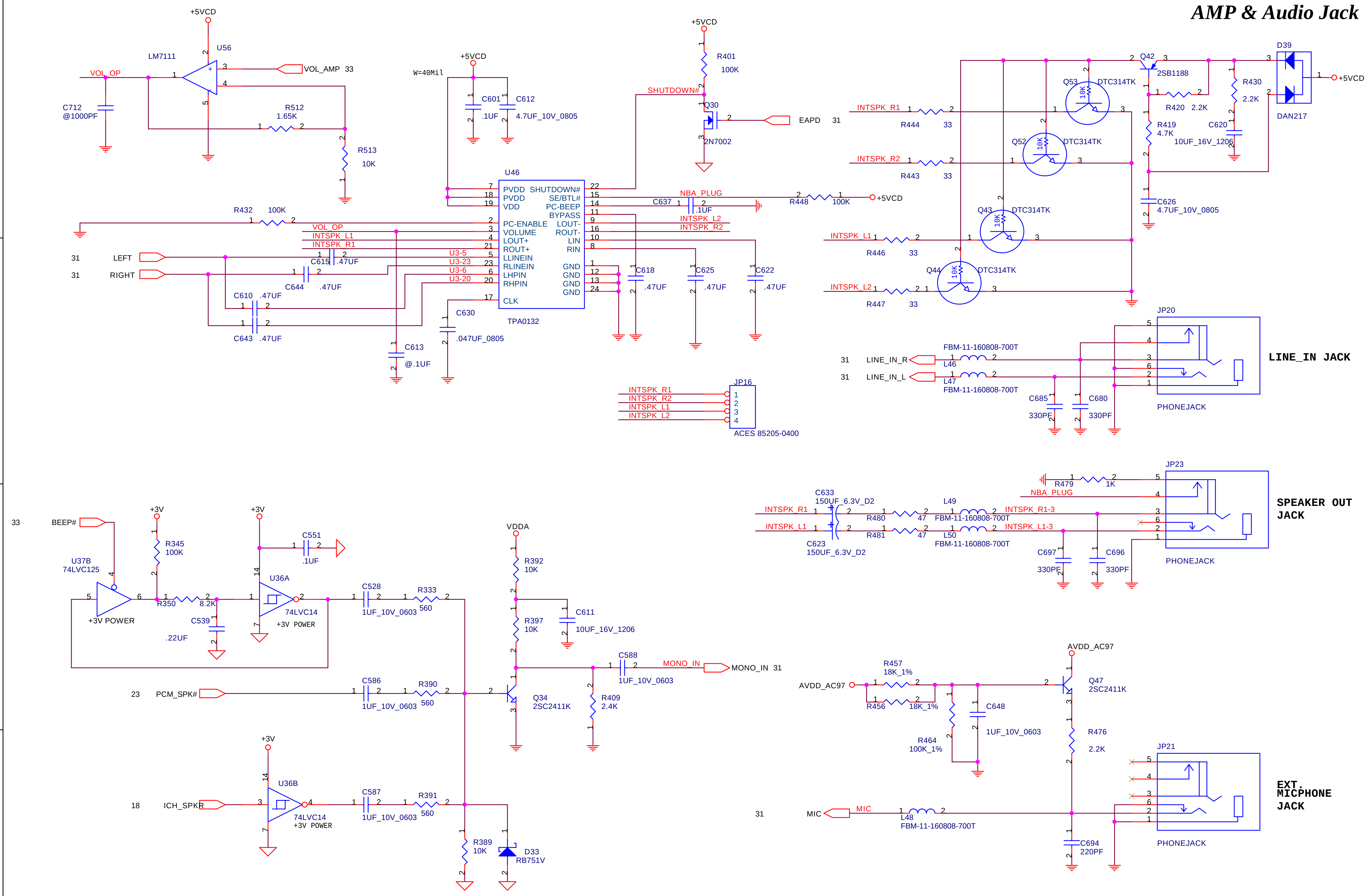
AMP & Audio Jack



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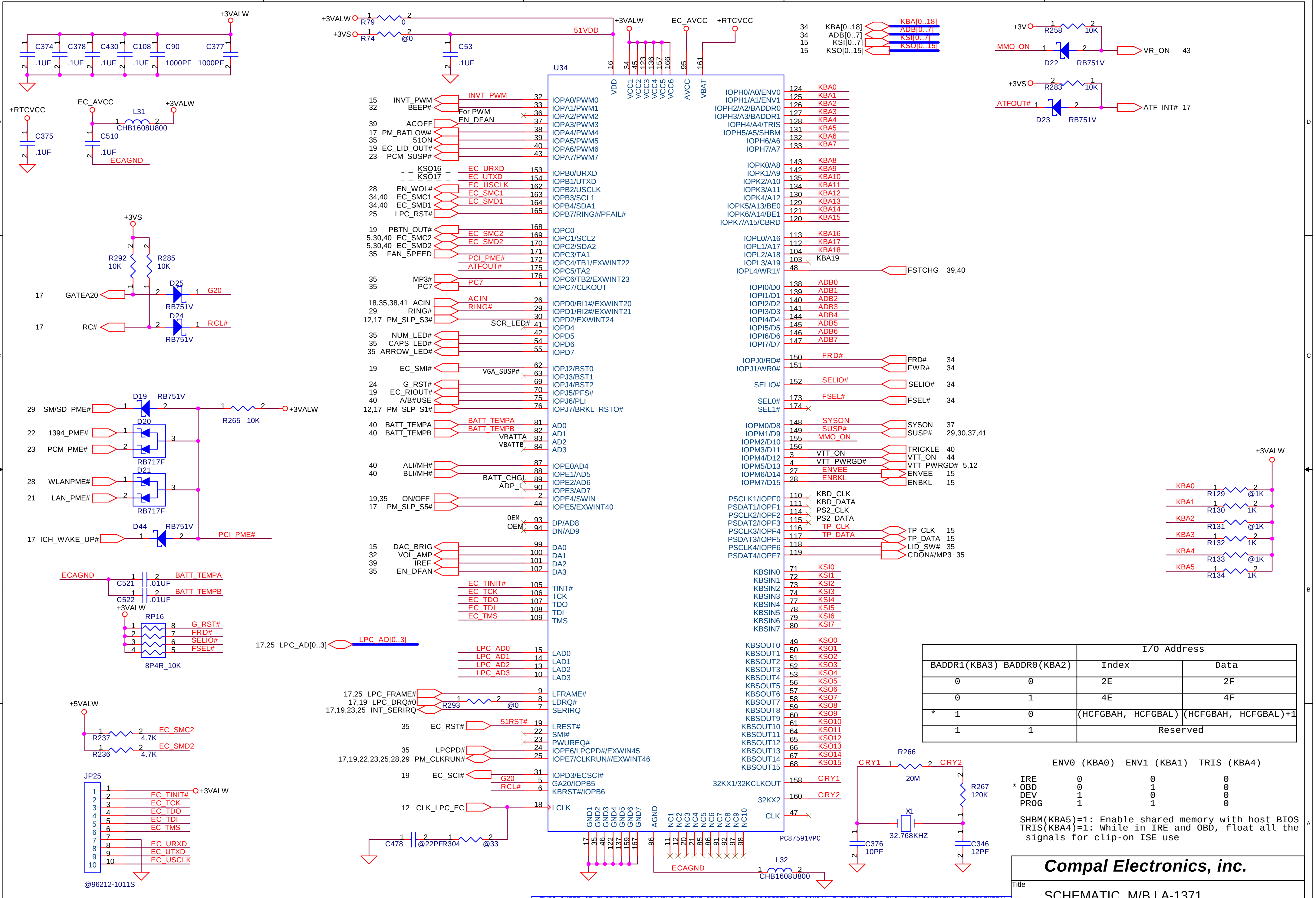

BADDR1(KBA3)	BADDR0(KBA2)	I/O Address Index	I/O Address Data
0	0	2E	2F
0	1	4E	4F
* 1	0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1	1	Reserved	

	ENV0 (KBA0)	ENV1 (KBA1)	TRIS (KBA4)
IRE	0	0	0
* OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

SHBM(KBA5)=1: Enable shared memory with host BIOS
TRIS(KBA4)=1: While in IRE and OBD, float all the signals for clip-on ISE use

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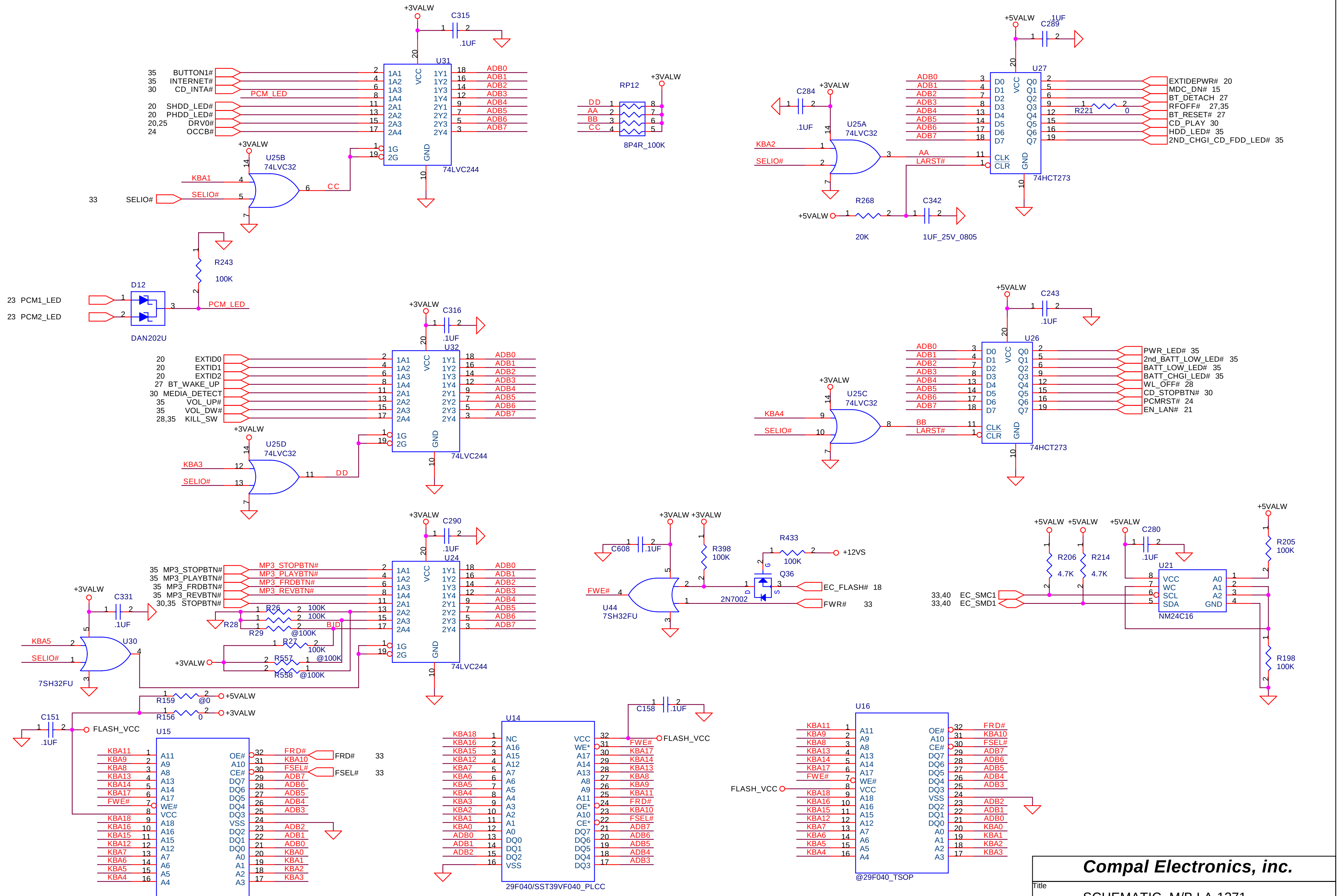

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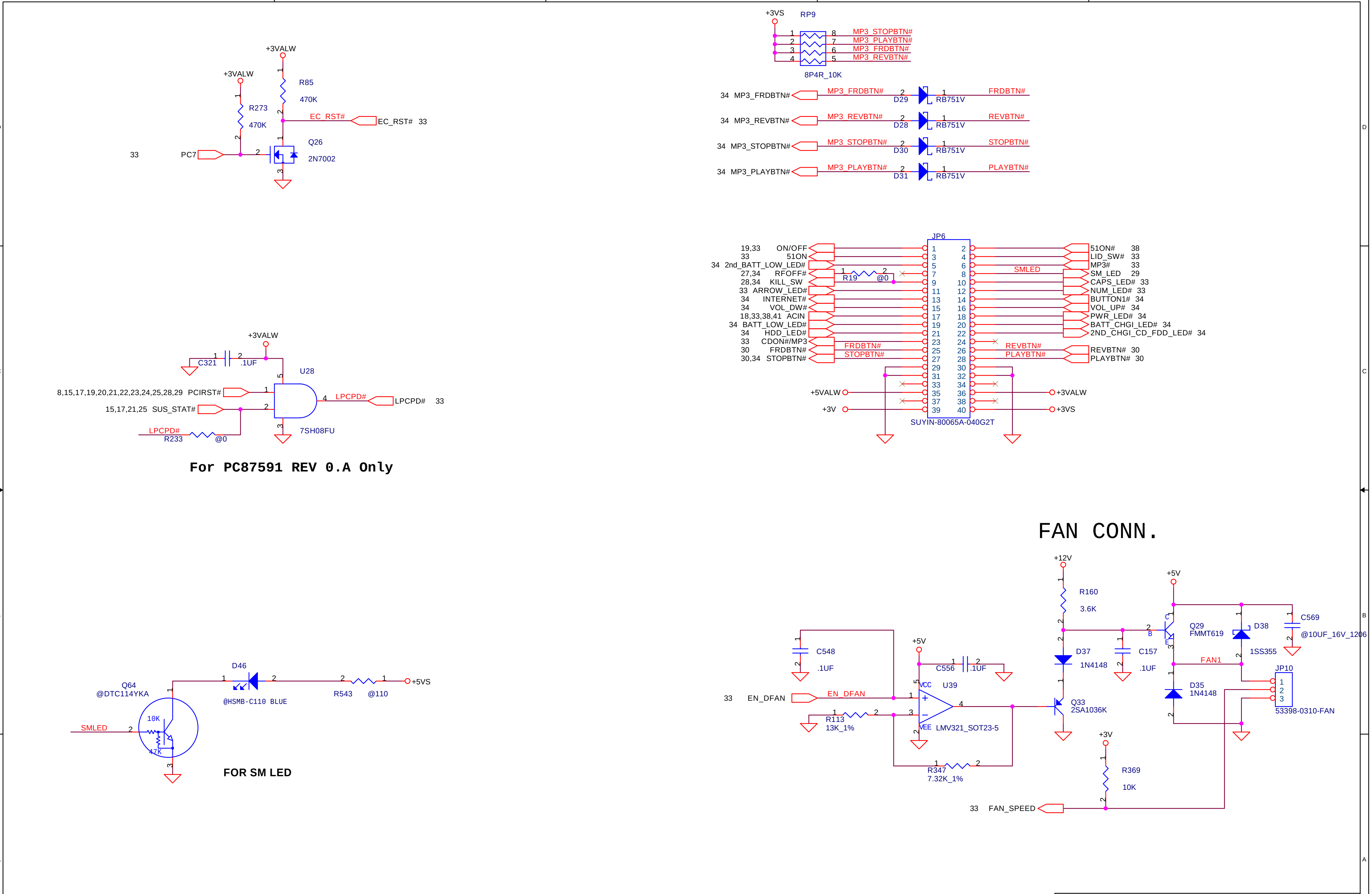

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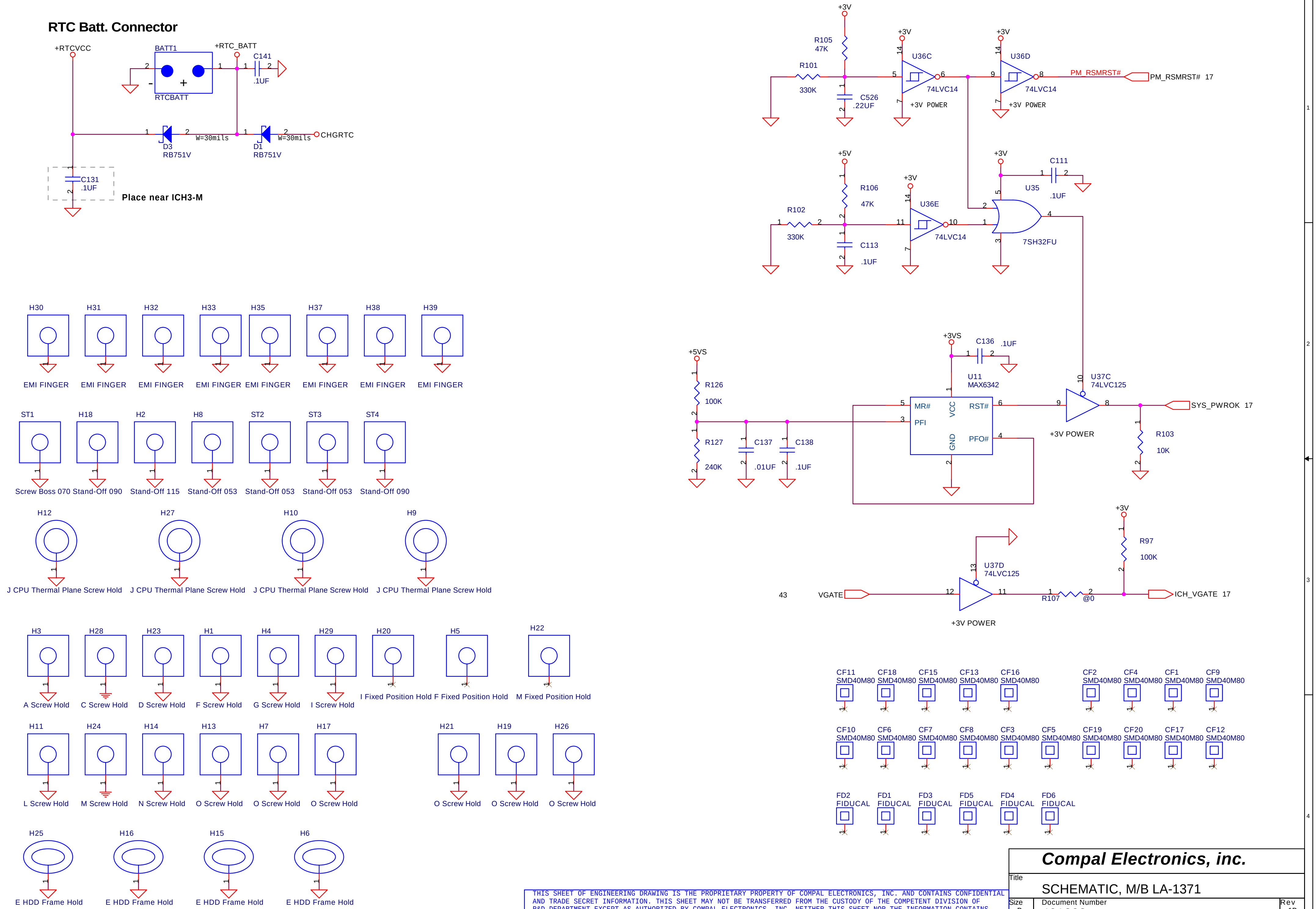

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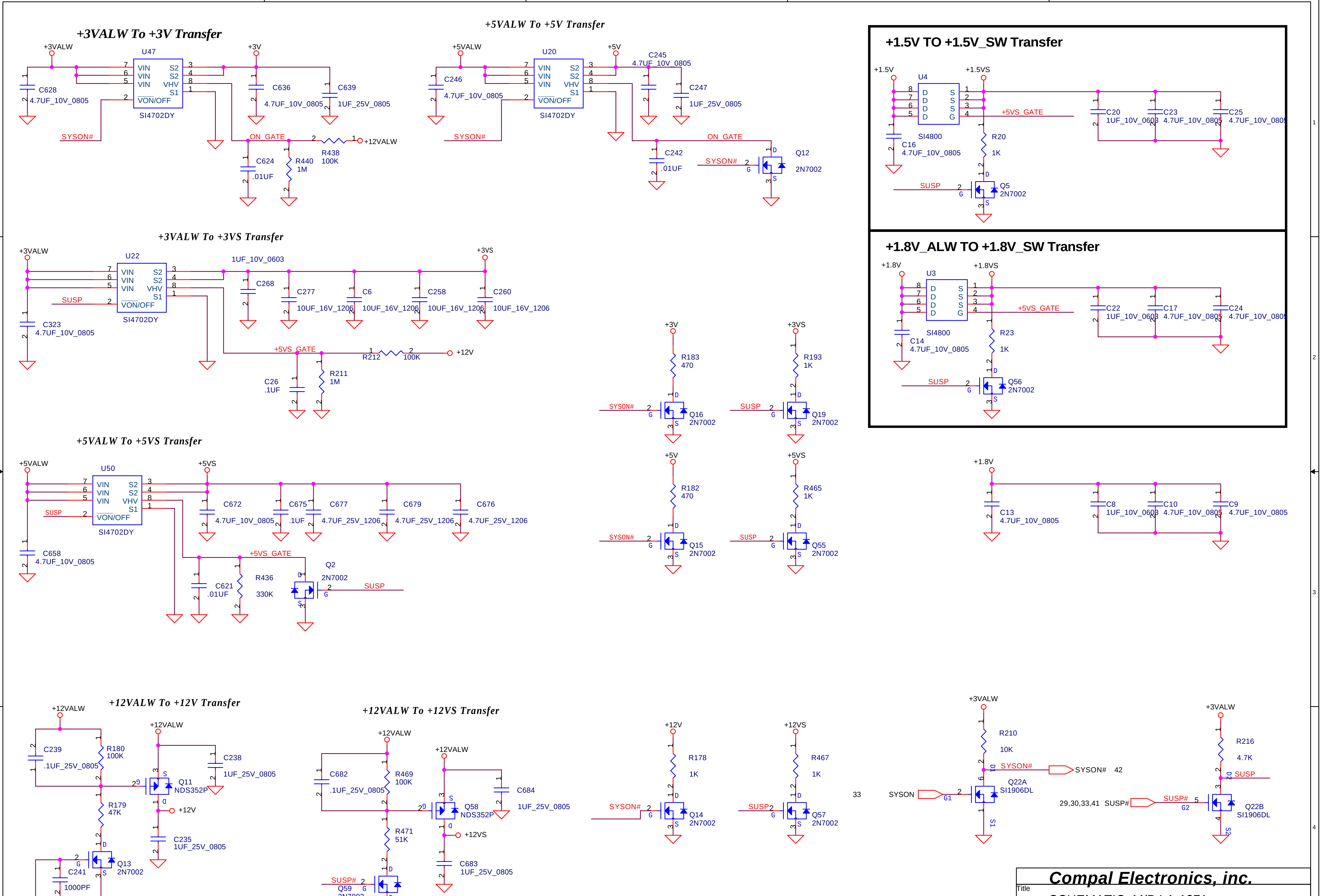

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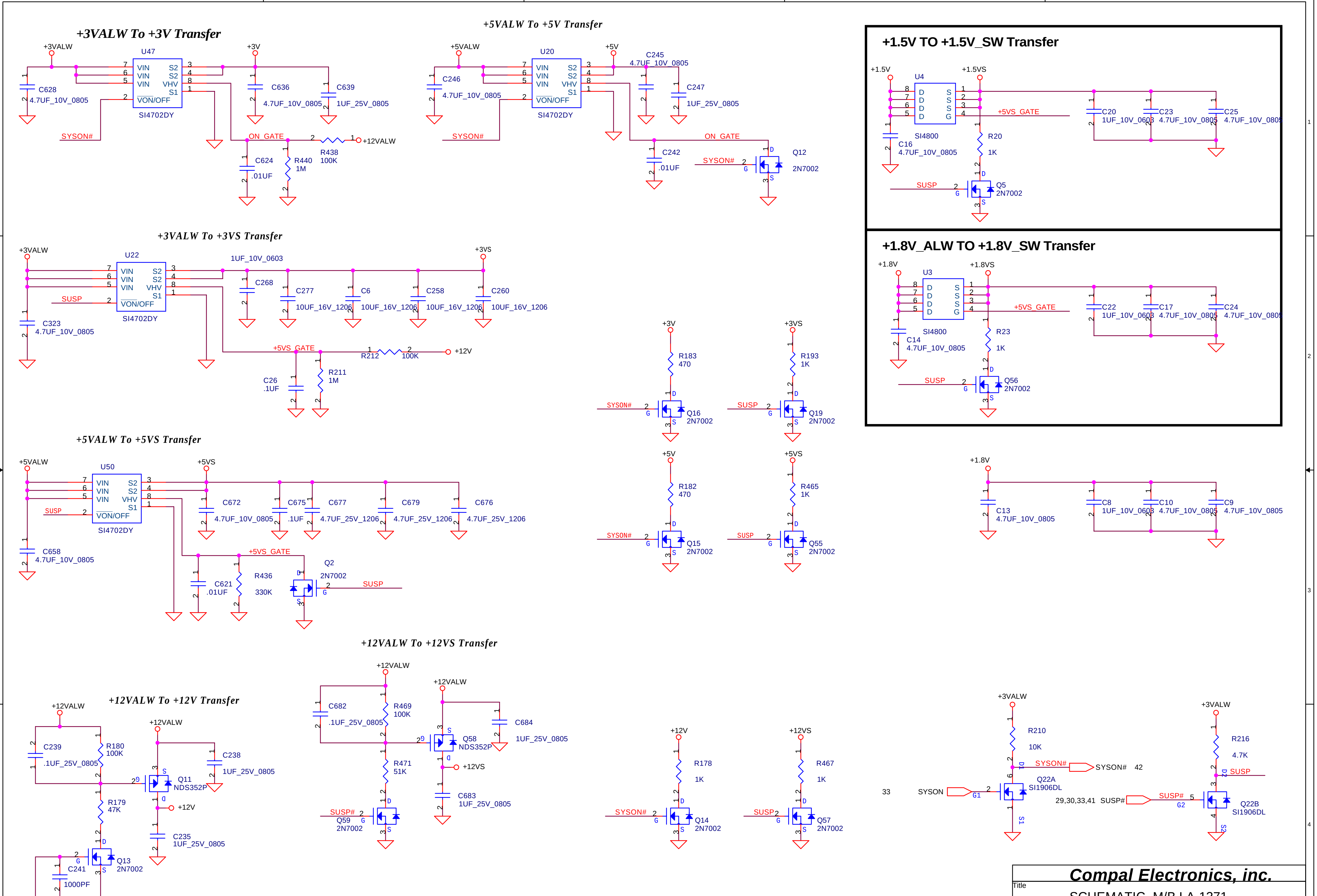

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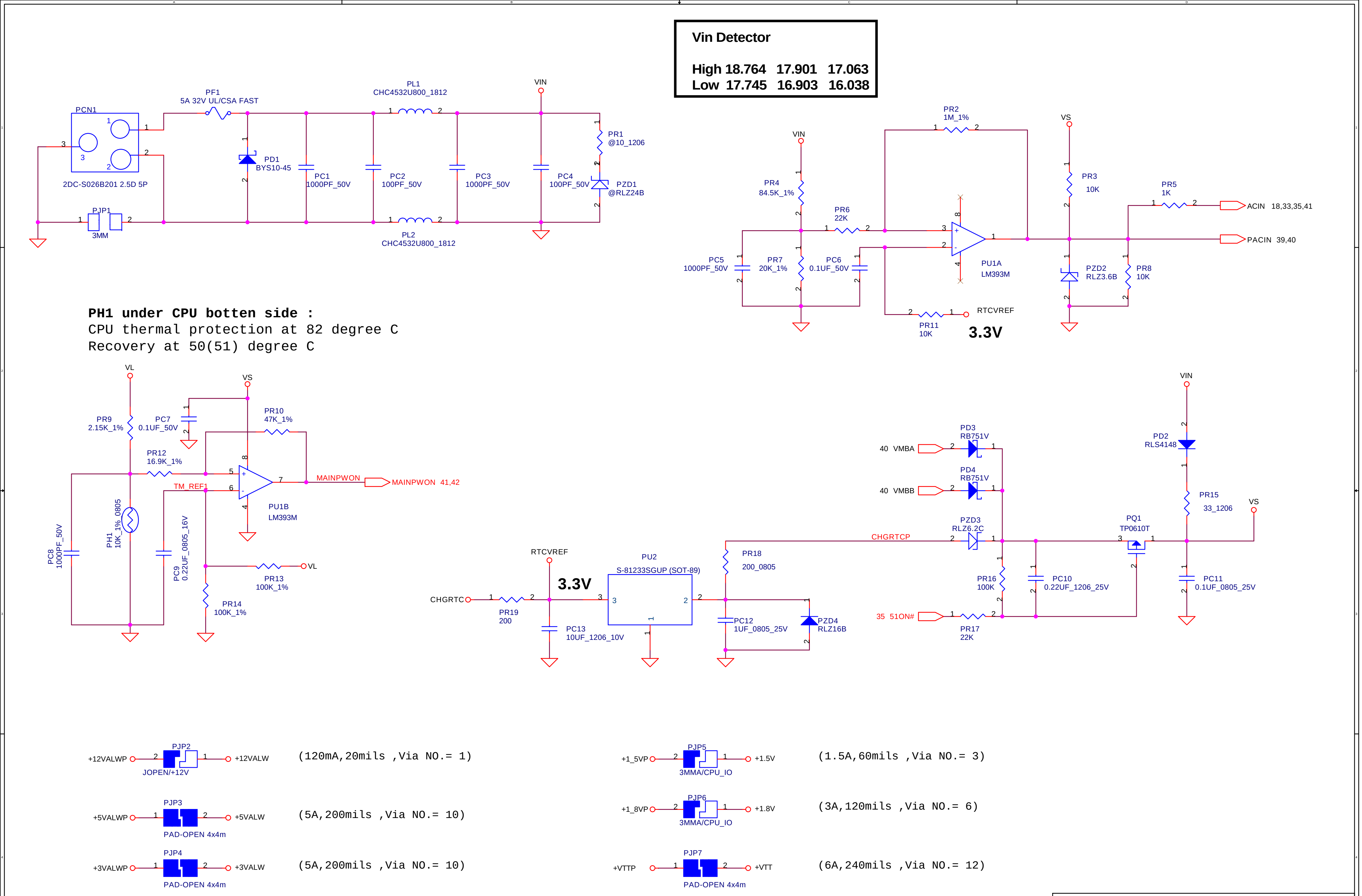

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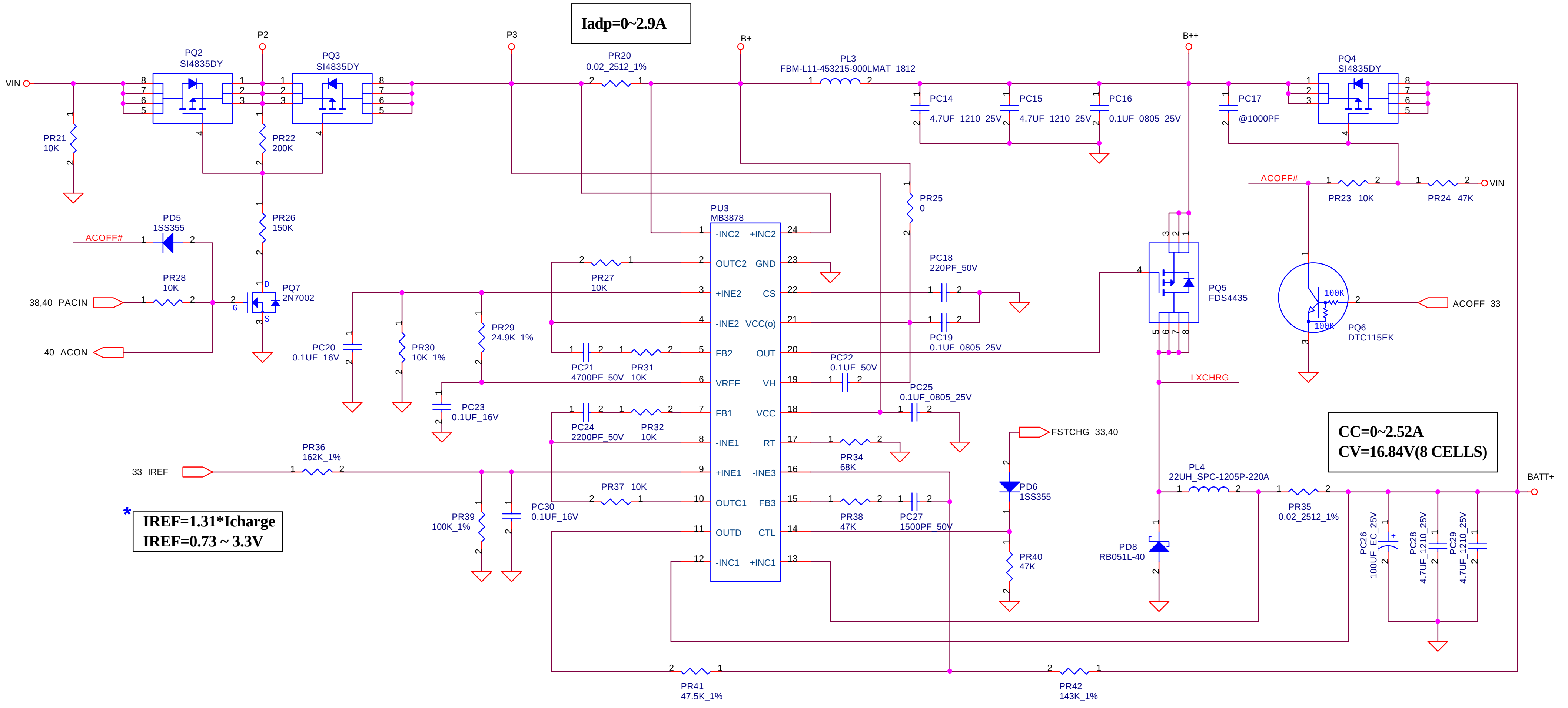

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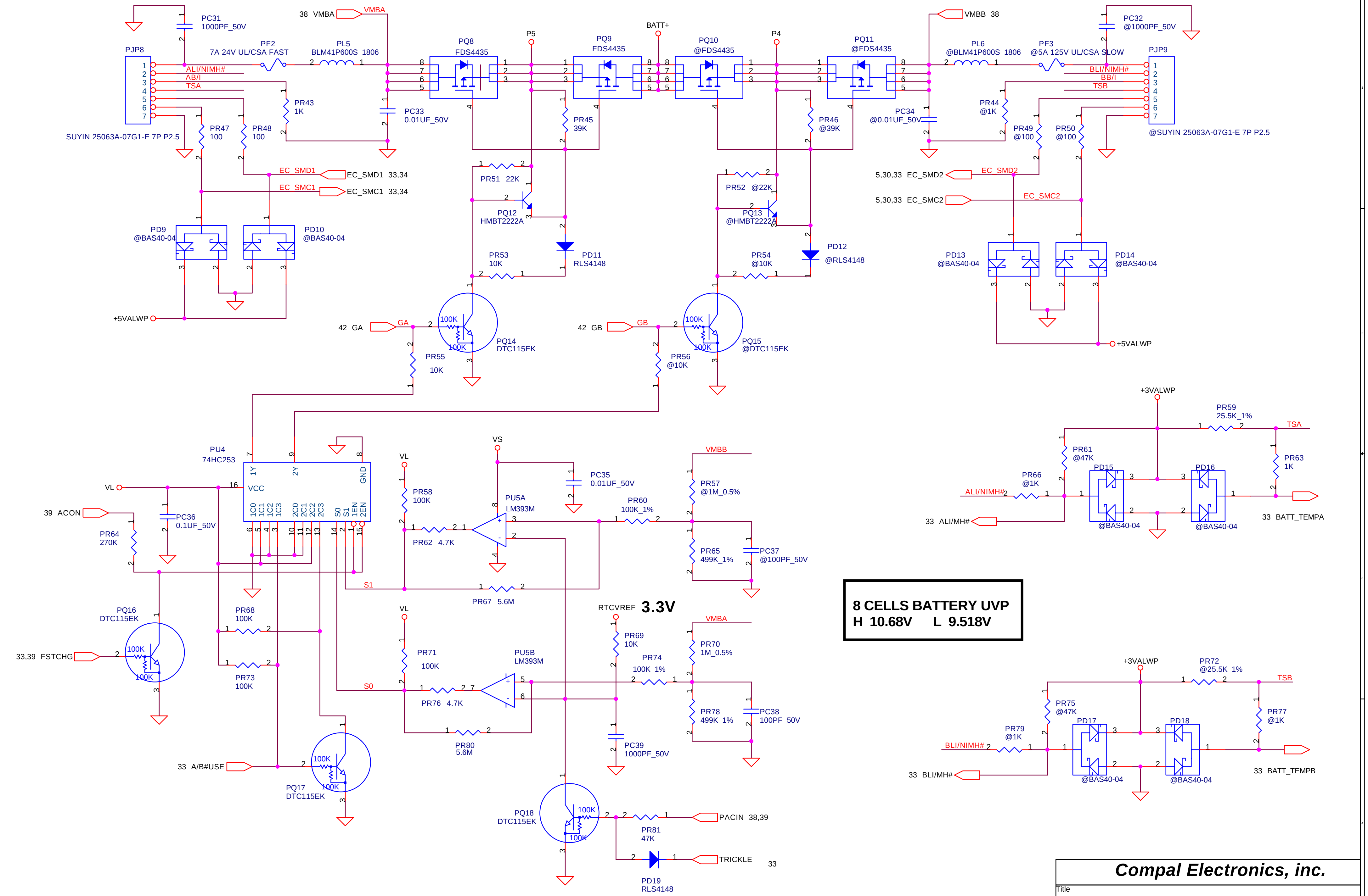

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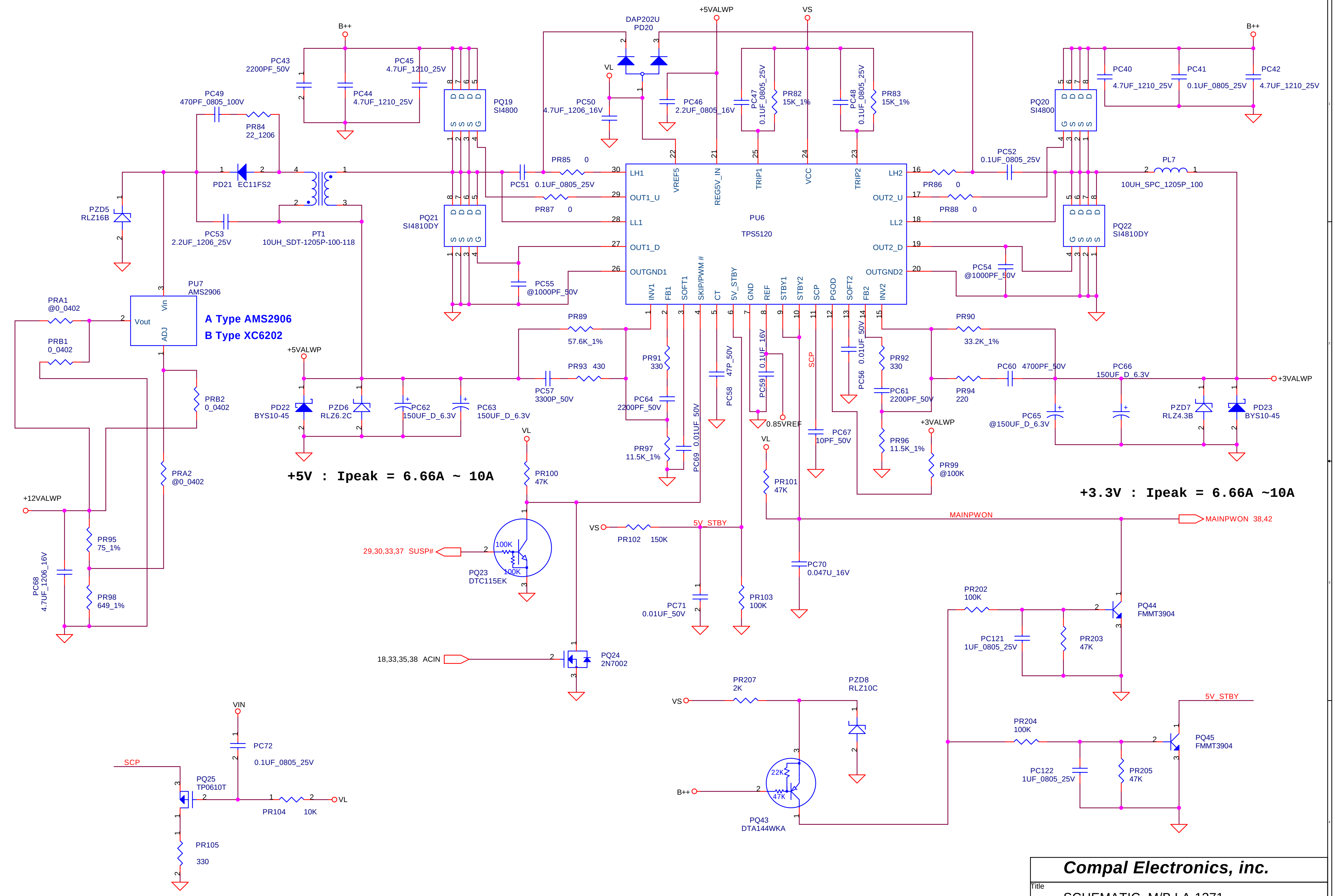

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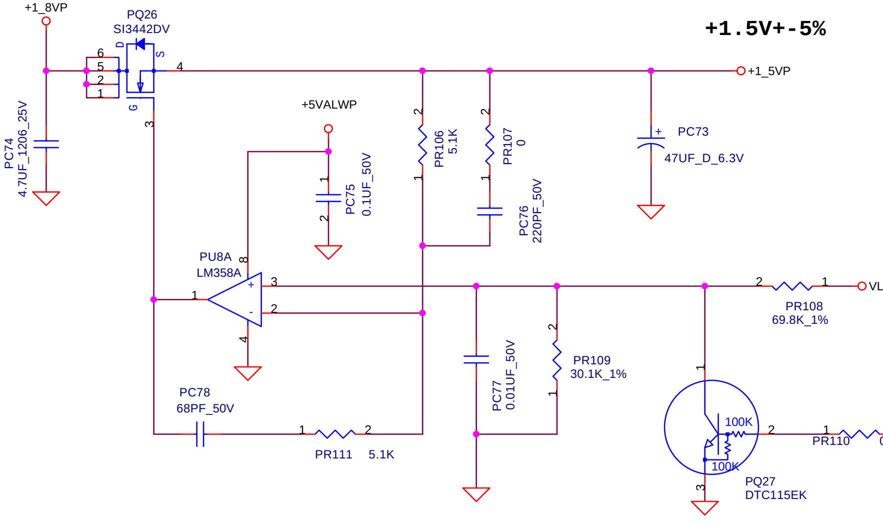
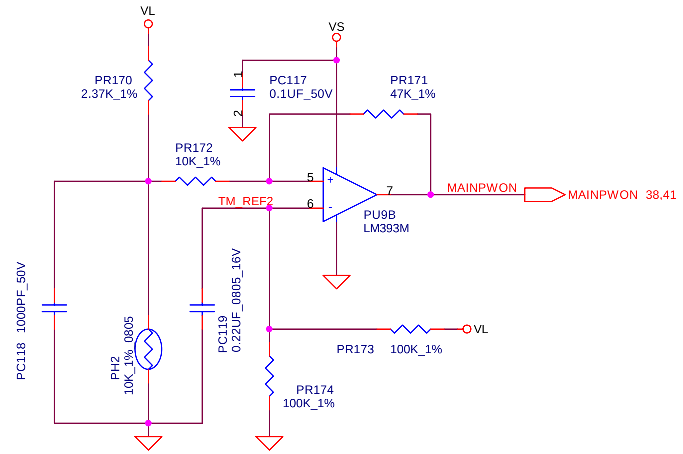
+1.5V+-5%



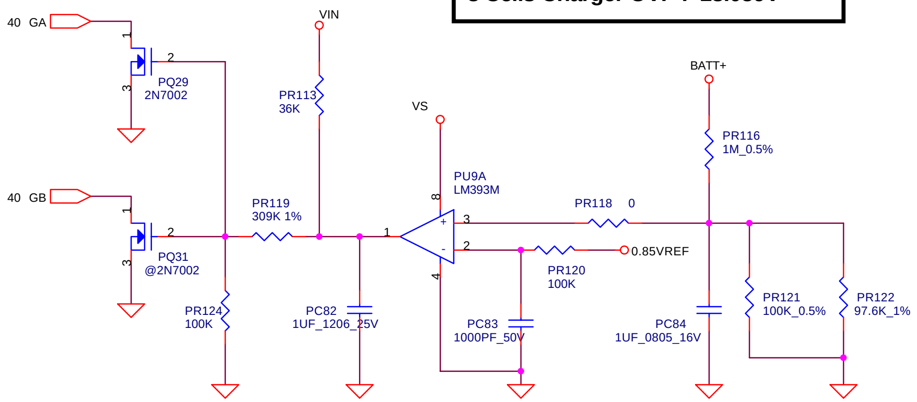
PH2 near main Battery CONN :

BAT. thermal protection at 73 degree C

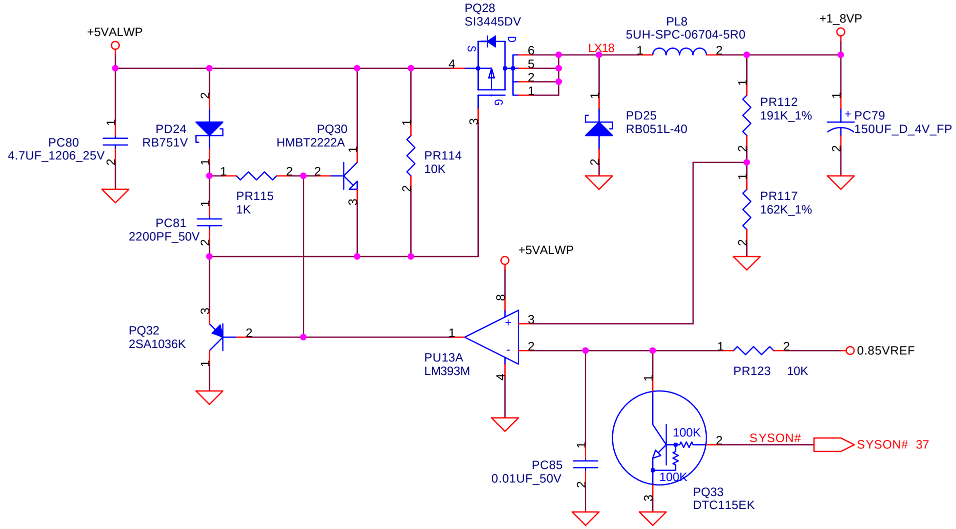
Recovery at 50(51) degree C



8 Cells Charger OVP : 18.059V



+1.8V+-5%



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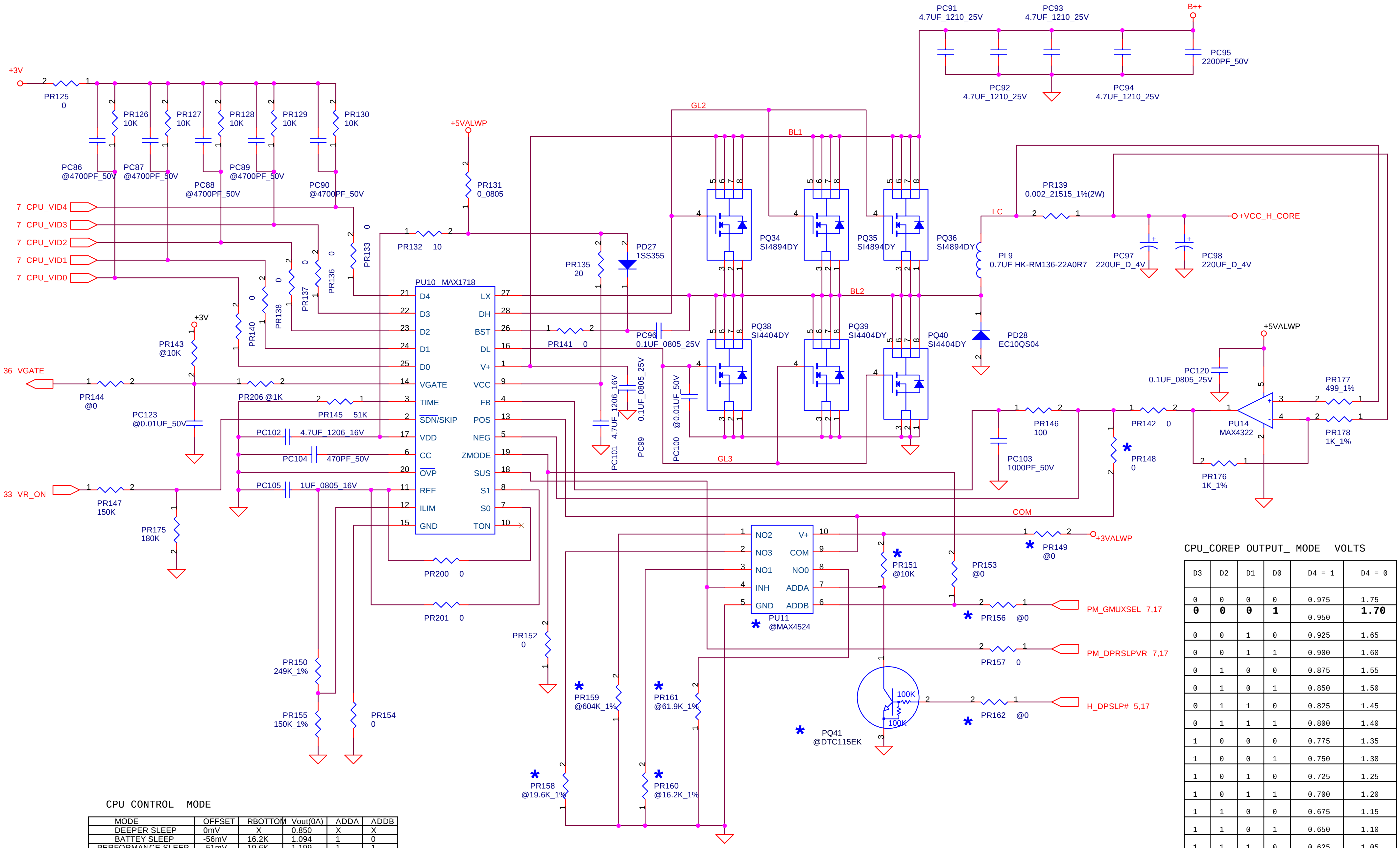

CPU_COREP OUTPUT_ MODE VOLTS

D3	D2	D1	D0	D4 = 1	D4 = 0
0	0	0	0	0.975	1.75
0	**0**	**0**	**1**	0.950	**1.70**
0	0	1	0	0.925	1.65
0	0	1	1	0.900	1.60
0	1	0	0	0.875	1.55
0	1	0	1	0.850	1.50
0	1	1	0	0.825	1.45
0	1	1	1	0.800	1.40
1	0	0	0	0.775	1.35
1	0	0	1	0.750	1.30
1	0	1	0	0.725	1.25
1	0	1	1	0.700	1.20
1	1	0	0	0.675	1.15
1	1	0	1	0.650	1.10
1	1	1	0	0.625	1.05
1	1	1	1	0.600	1.00

CPU CONTROL MODE

MODE	OFFSET	RBOTTOM	Vout(0A)	ADDA	ADDB
DEEPER SLEEP	0mV	X	0.850	X	X
BATTEY SLEEP	-56mV	16.2K	1.094	1	0
PERFORMANCE SLEEP	-51mV	19.6K	1.199	1	1
BATTERY MODE	-16mV	61.9K	1.134	0	0
PERFORMANCE MODE	**-1.8mV**	604K	1.248	0	1

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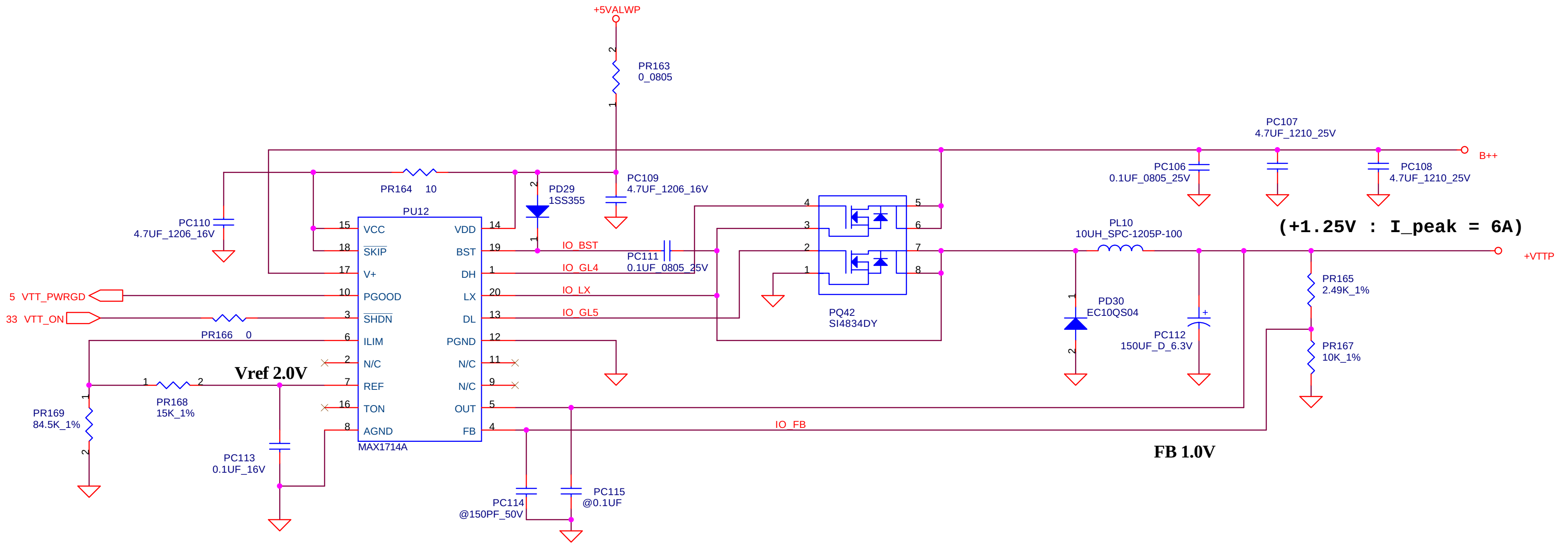

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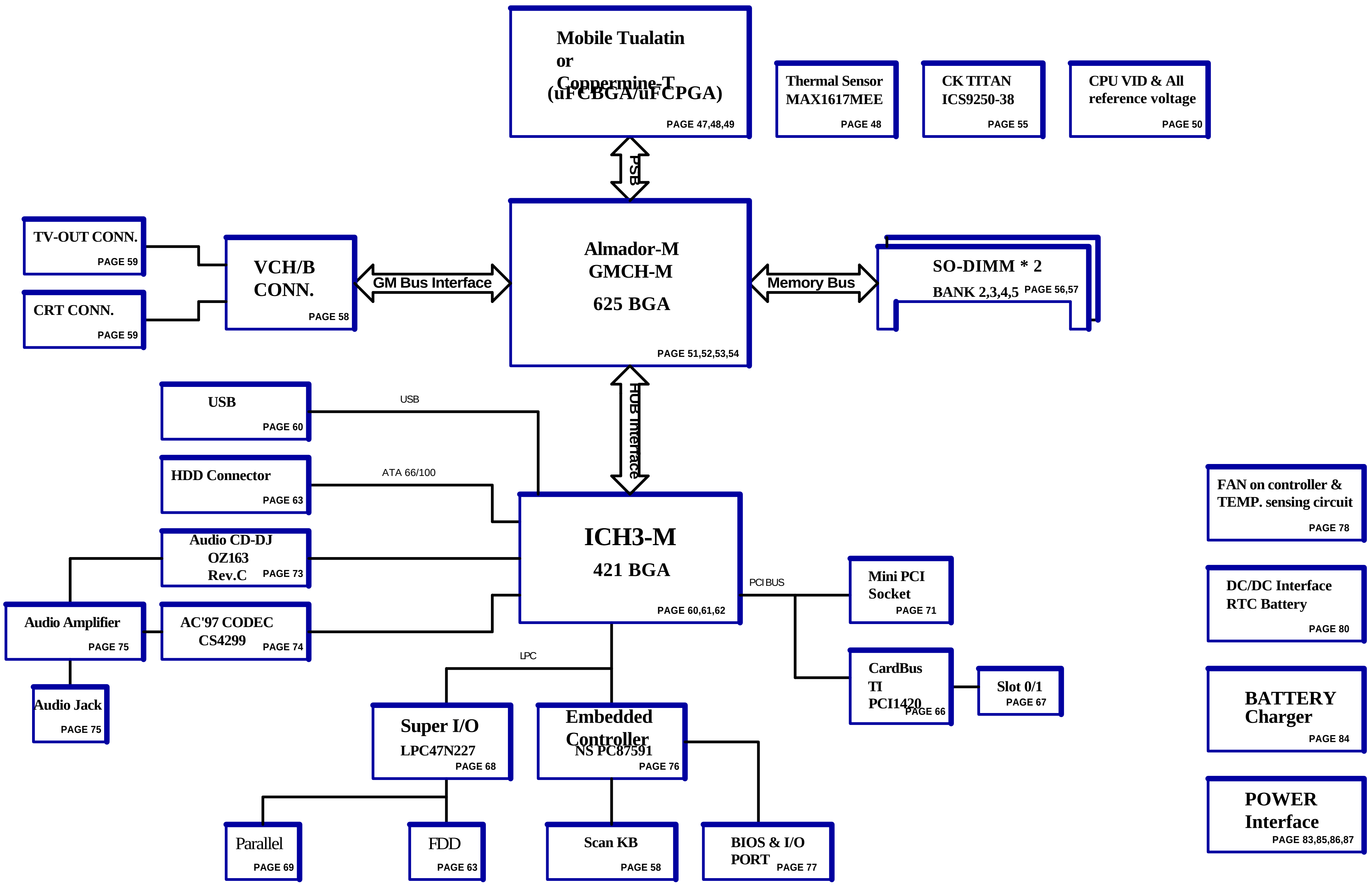
ATW03 BLOCK DIAGRAM



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_H_CORE	Core voltage for CPU	ON	OFF	OFF
+VTT	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+1.8V	1.8V power rail	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12VS	12V switched power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
VCH CONN.			PIRQA
IEEE 1394	AD16	0	PIRQA
CardBus	AD20	2	PIRQA/PIRQB
LAN	AD17	3	PIRQB
Mini-PCI	AD18	1/4	PIRQC/PIRQD
SD/SM (RESERVE)	AD22		PIRQC/PIRQD

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
(24C04)	1011 000Xb

EC SM Bus2 address

Device	Address
MAX1617MEE	1001 110X b
OZ163	0011 0100 b
Smart Battery	0001 011X b
Docking	0011 011X b
DOT Board	XXXX XXXXb

ICH3-M SM Bus address

Device	Address
Clock Generator (ICS9238-50)	1101 0000
SDRAM Select (74HC4052)	1010 0000
CPU Voltage VID select (F3565)	0110 111Xb

PIR

REV 0.1

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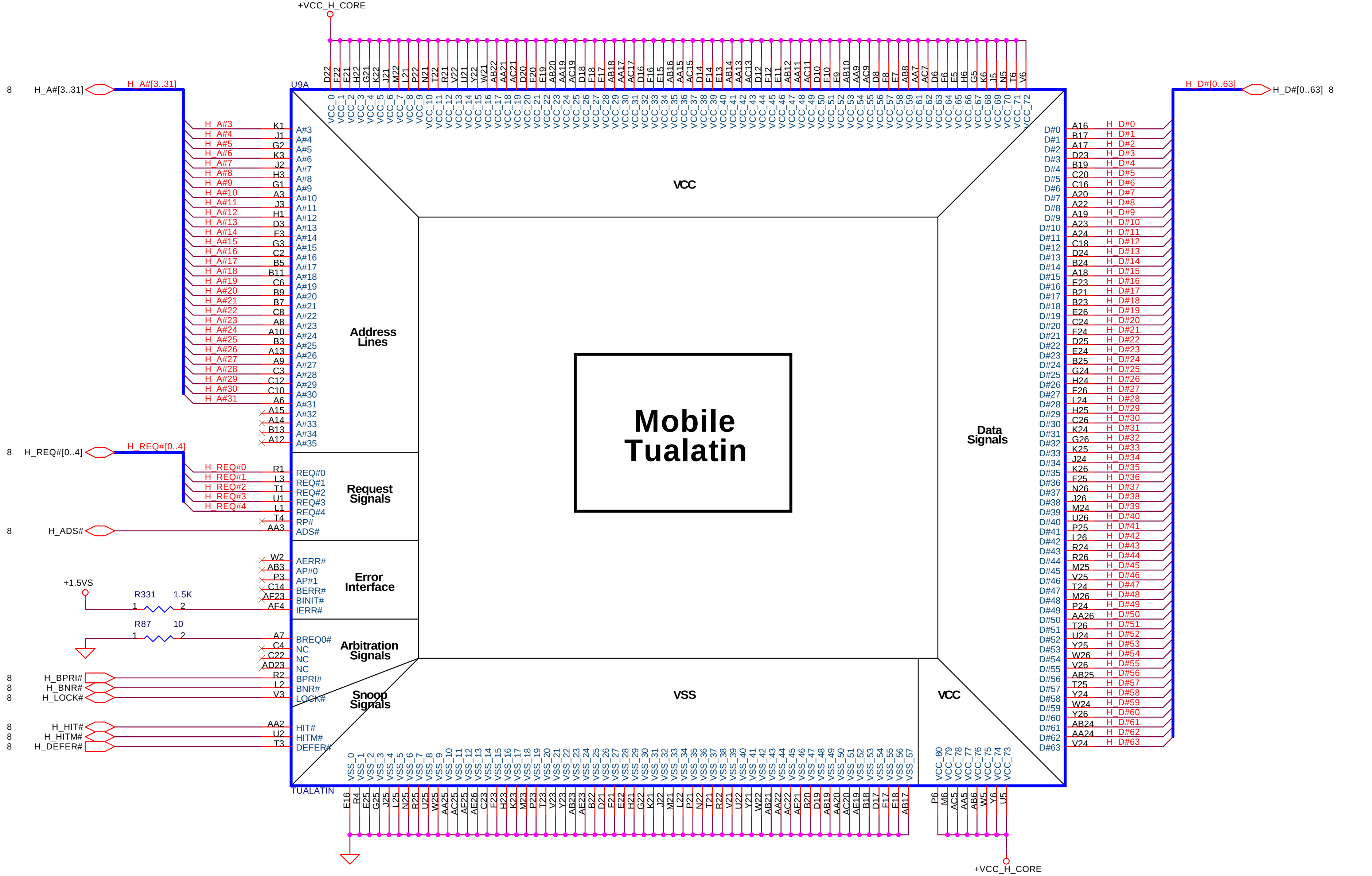

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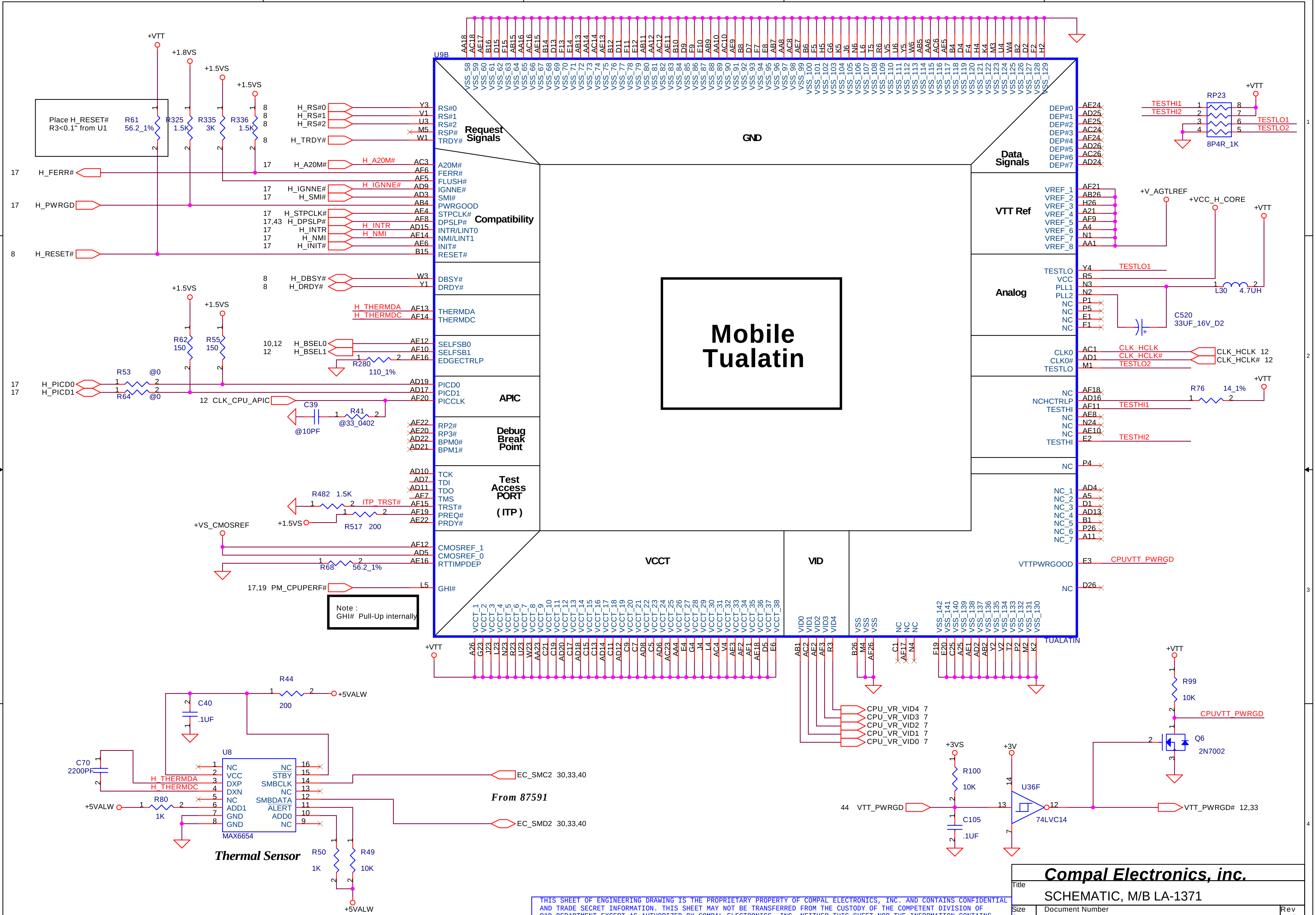

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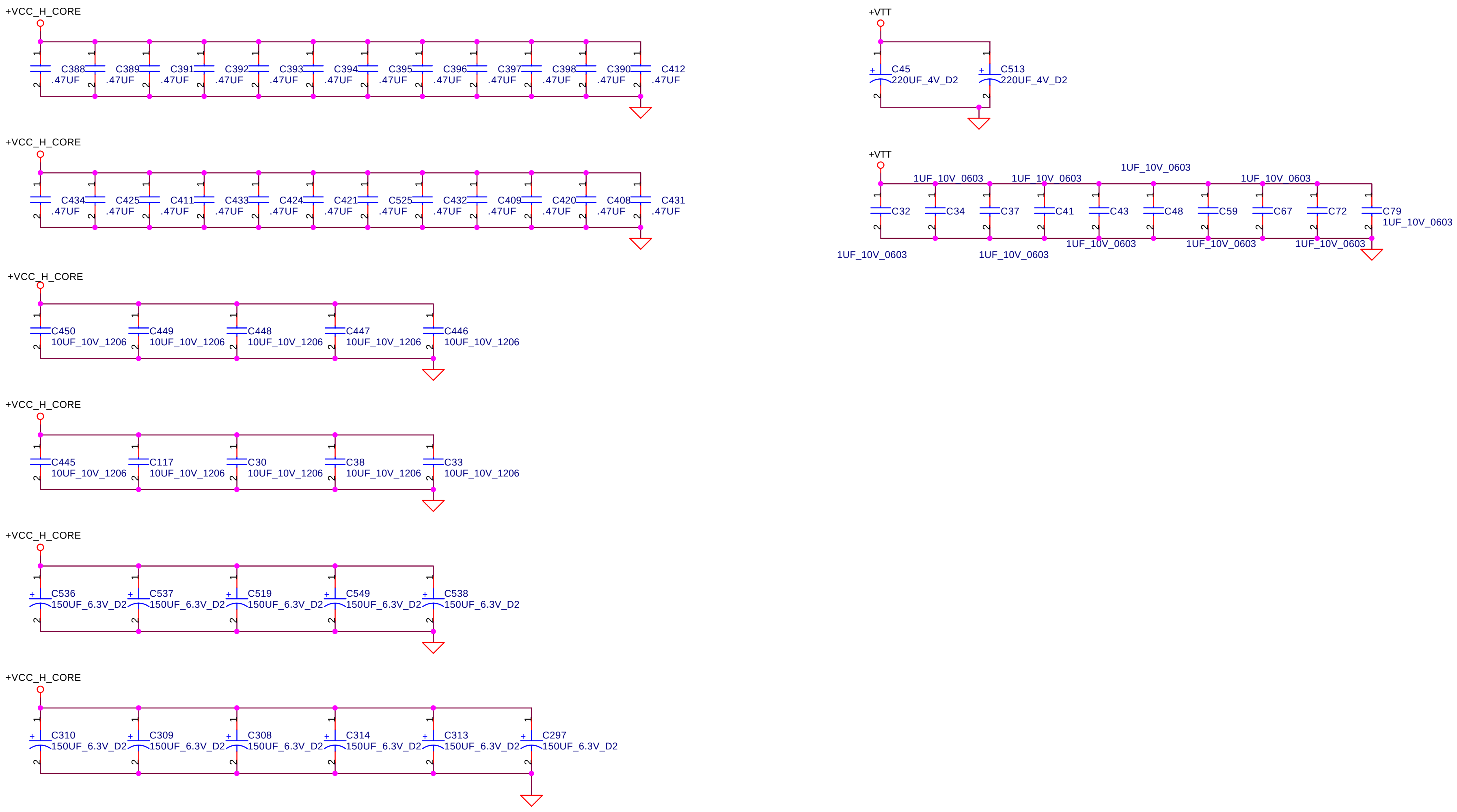
Layout note :

Place close to CPU, Use 2~3 vias per PAD.
Place .47uF caps underneath balls on solder side
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.

Layout note :

Place close to CPU,
Use 2 vias per PAD.



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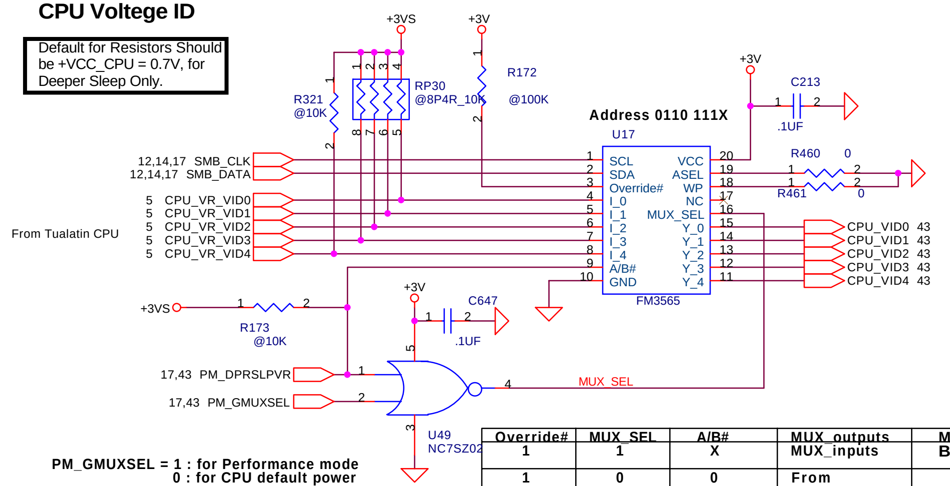
CPU Voltege ID

Default for Resistors Should be +VCC_CPU = 0.7V, for Deeper Sleep Only.



PM_GMUXSEL = 1 : for Performance mode
0 : for CPU default power

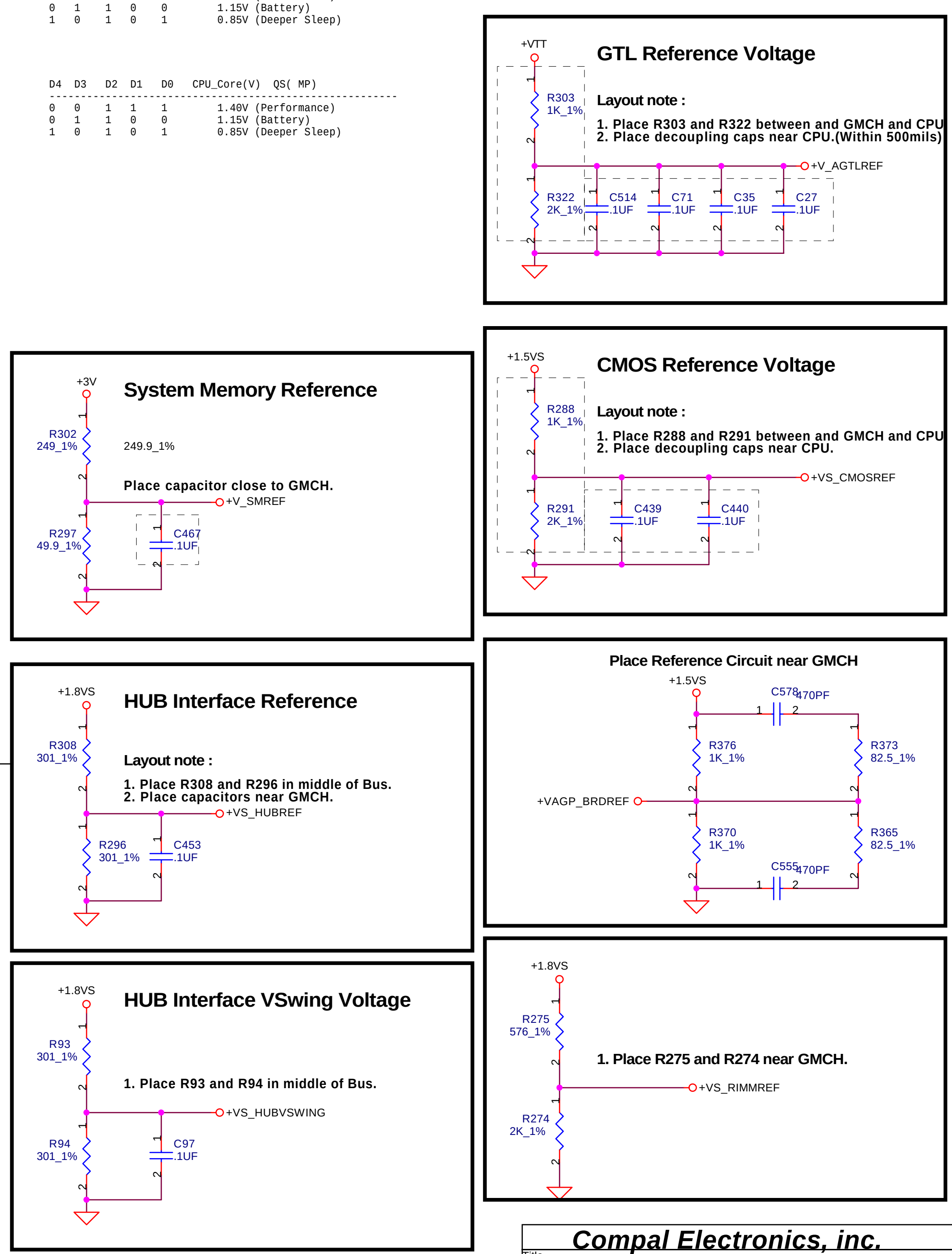
PM_DPRSLPVR = 1: for Deeper Sleep mode
0 : for Performance mode

Override#	MUX_SEL	A/B#	MUX_outputs	Mode
1	1	X	MUX_inputs	Battery
1	0	0	From Non-volatile register(SOPRB)	Performance
1	0	1	From Non-volatile register(SOPRA)	Deeper sleep

Tualatin

D4	D3	D2	D1	D0	CPU_Core(V)	ES(before MP)
0	0	1	0	1	1.50V	(Performance)
0	1	1	0	0	1.15V	(Battery)
1	0	1	0	1	0.85V	(Deeper Sleep)

D4	D3	D2	D1	D0	CPU_Core(V)	QS(MP)
0	0	1	1	1	1.40V	(Performance)
0	1	1	0	0	1.15V	(Battery)
1	0	1	0	1	0.85V	(Deeper Sleep)



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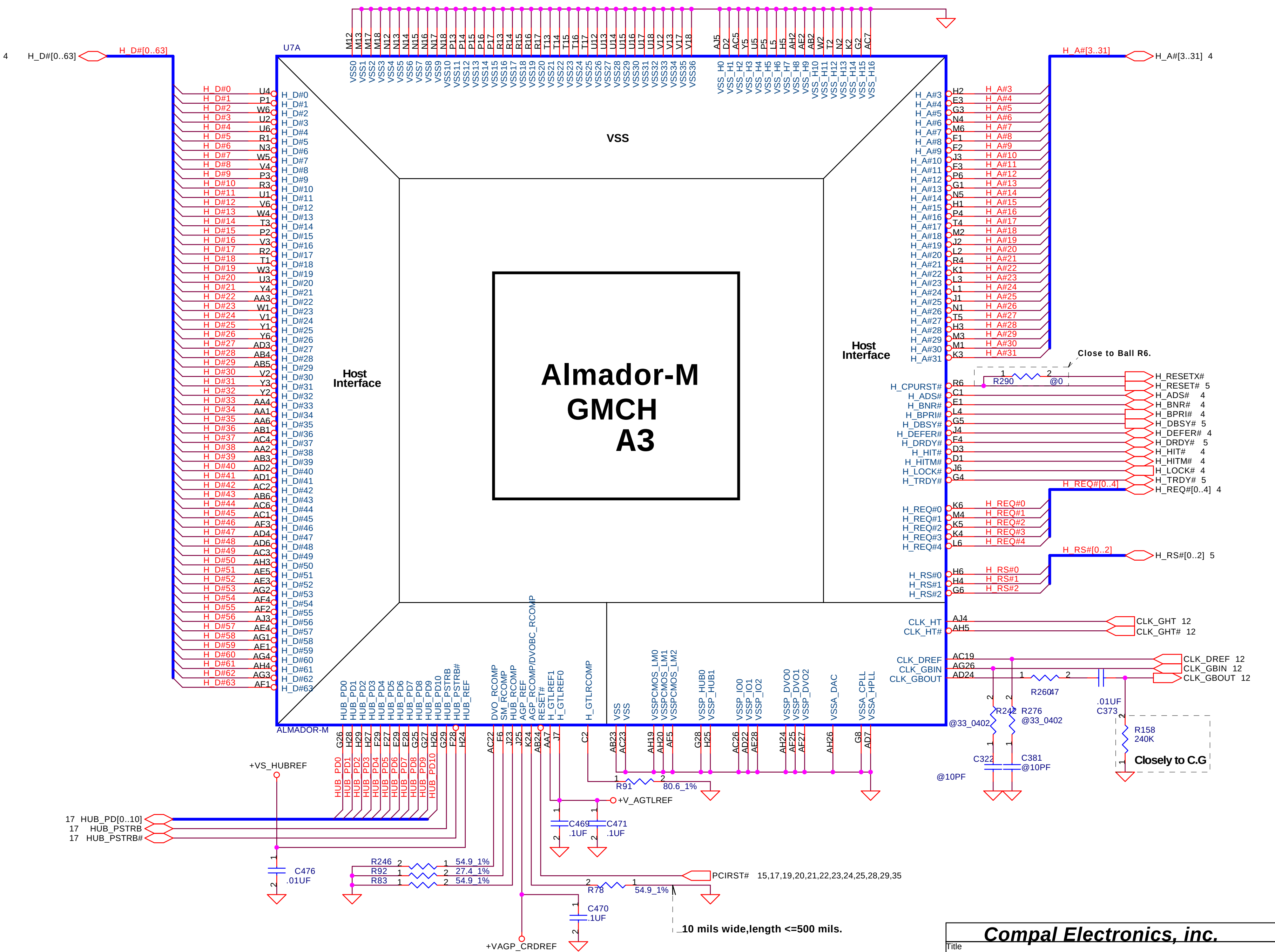

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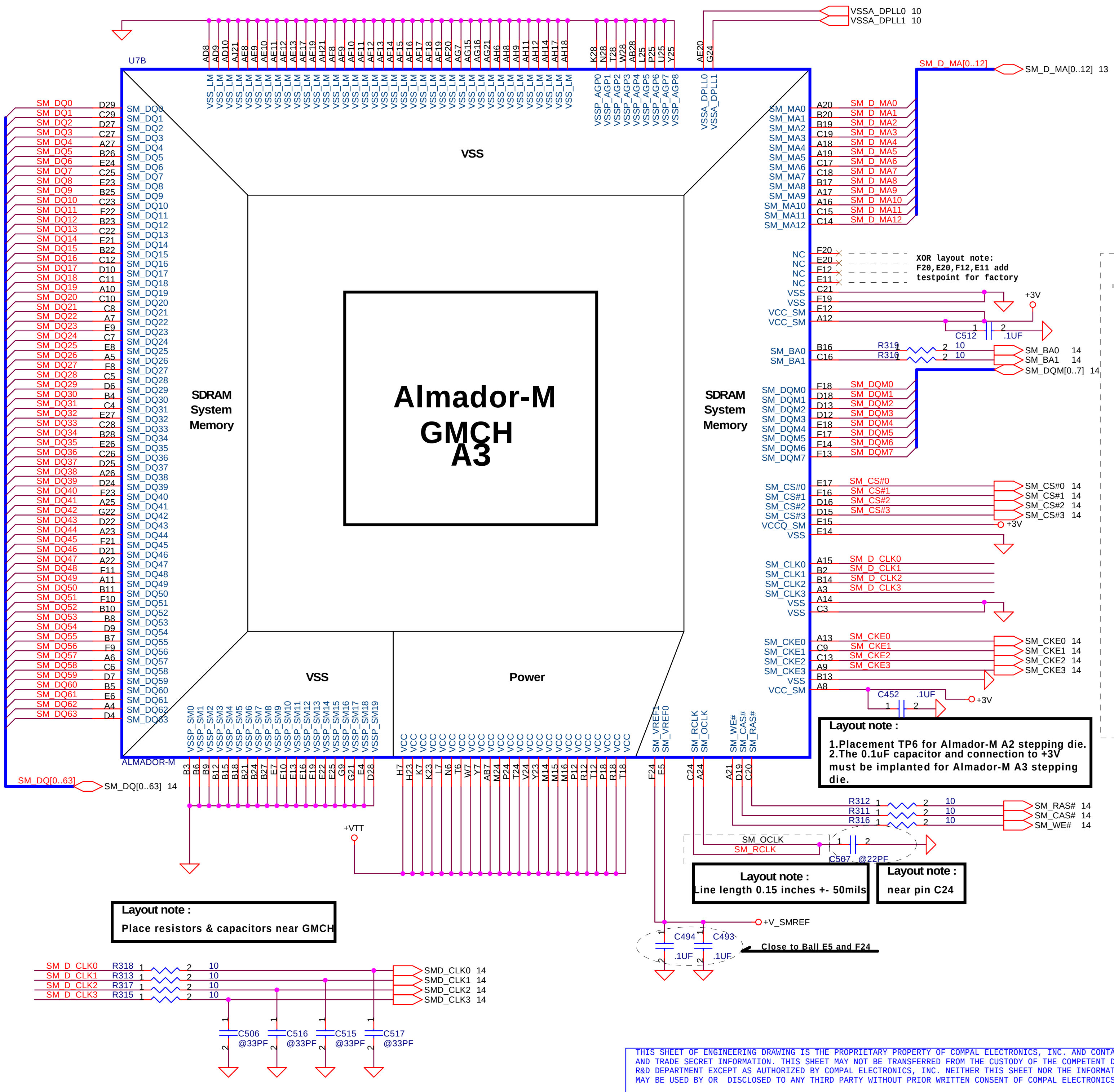

For Almador-M A3 stepping requirement.

The table below provides a summary of the ballout changes to the Almador-M chip

Table 4-1 Ballout Changes

Ball#	New Signal Name	Old Signal Name
A8	VCC_SM	SM_CKE5
A12	VCC_SM	SM_ECC7
E12	VCC_SM	SM_ECC6
D10	VCC_SM	VCCQ_SM
F7	VCCQ_SM	VCC_SM
D19	VCCQ_SM	VCC_SM
E15	VCCQ_SM	SM_CS4
F15	VCCQ_SM	VCC_SM
A14	VSS	SM_CLK4
B13	VSS	SM_CKE4
C3	VSS	SM_CLK5
C21	VSS	SM_ECC4
E14	VSS	SM_CS5
F19	VSS	SM_ECC5
E11	NC	SM_ECC3
E20	NC	SM_ECC1
F12	NC	SM_ECC2
F20	NC	SM_ECC0

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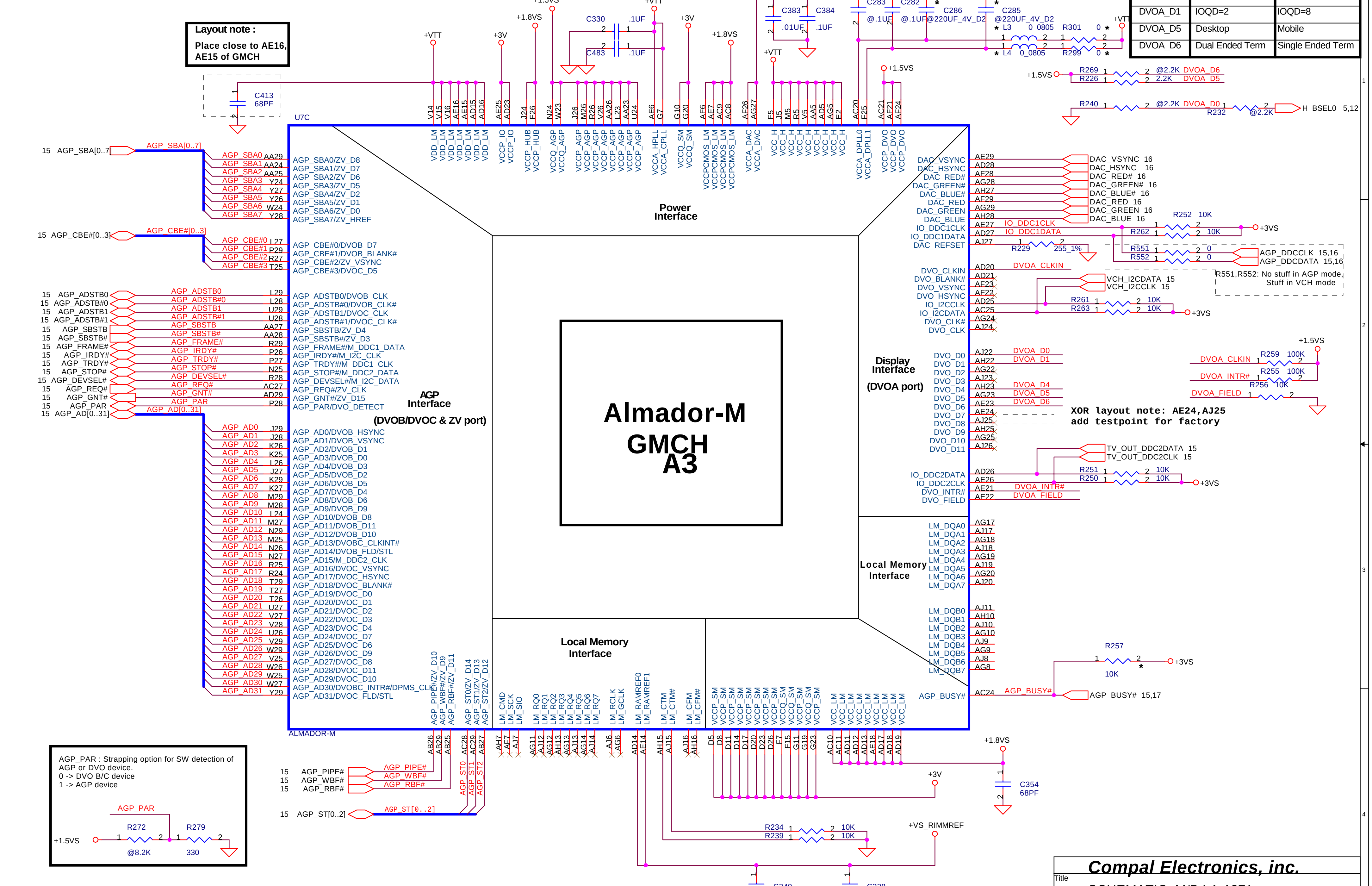
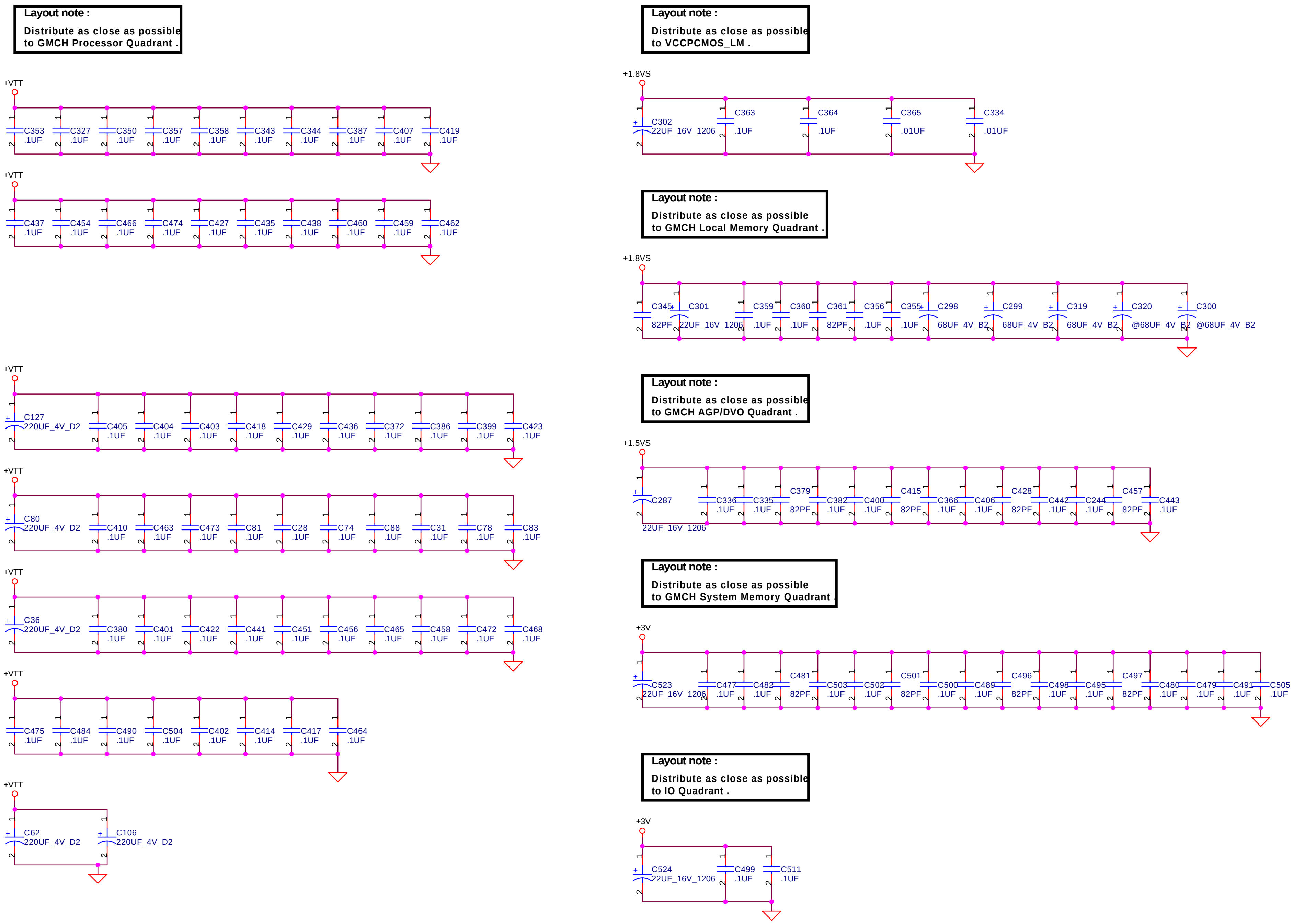
Strap Name	Low	High
DVOA_D0	Reserved	133MHz
DVOA_D1	IOQD=2	IOQD=8
DVOA_D5	Desktop	Mobile
DVOA_D6	Dual Ended Term	Single Ended Term





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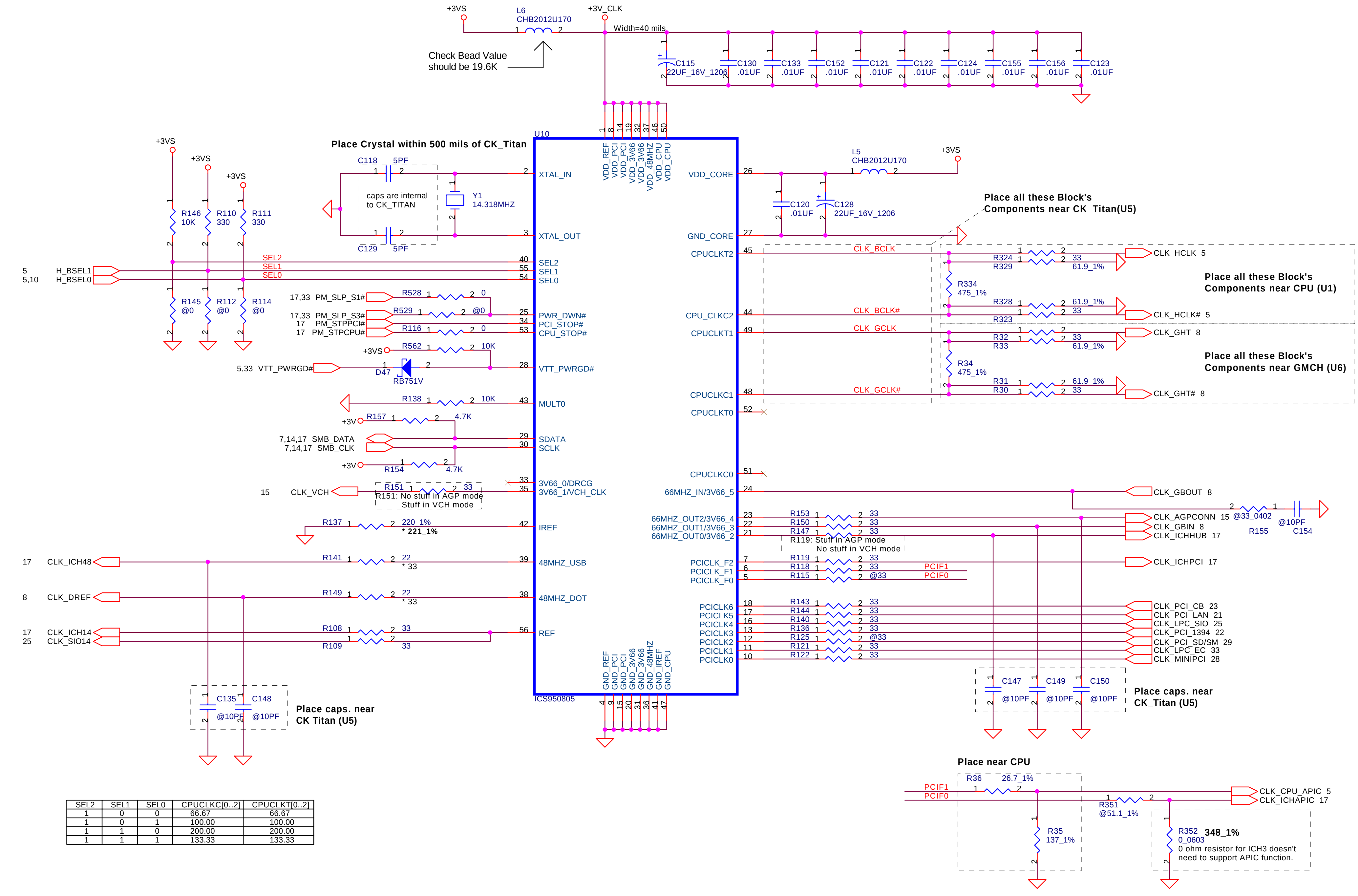

SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
1	0	0	66.67	66.67
1	0	1	100.00	100.00
1	1	0	200.00	200.00
1	1	1	133.33	133.33

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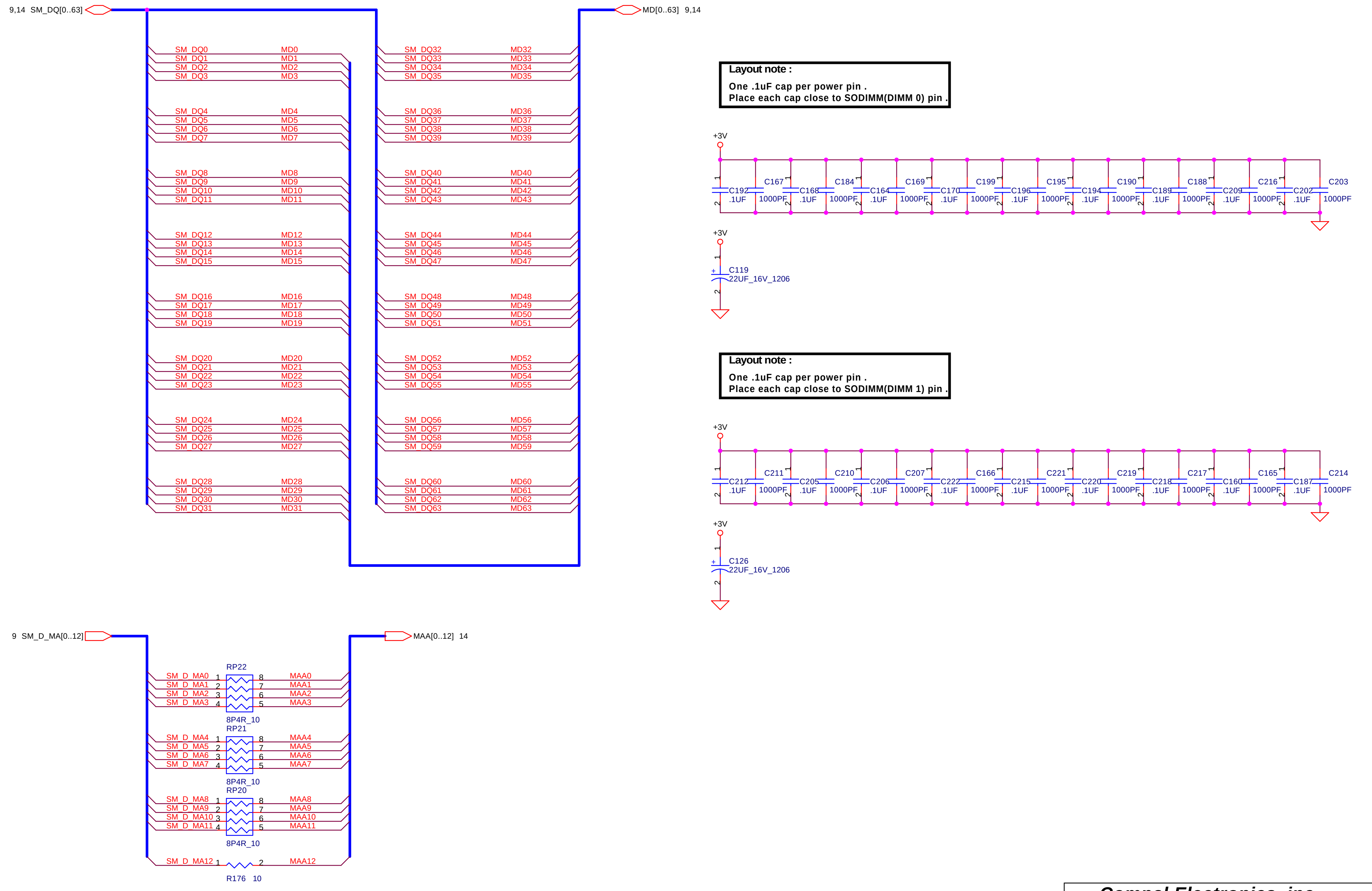

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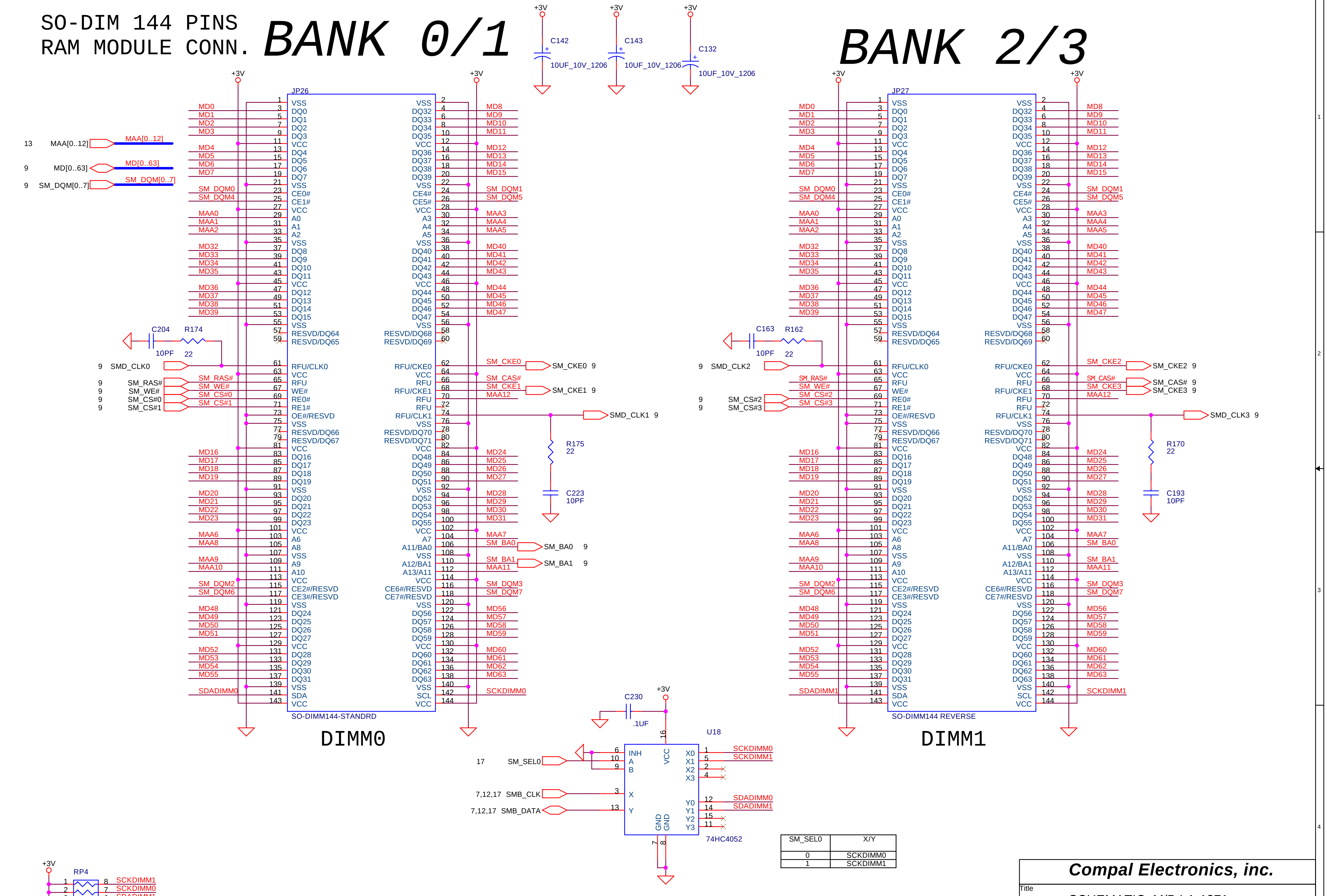

SM_SEL0	X/Y
0	SCKDIMM0
1	SCKDIMM1

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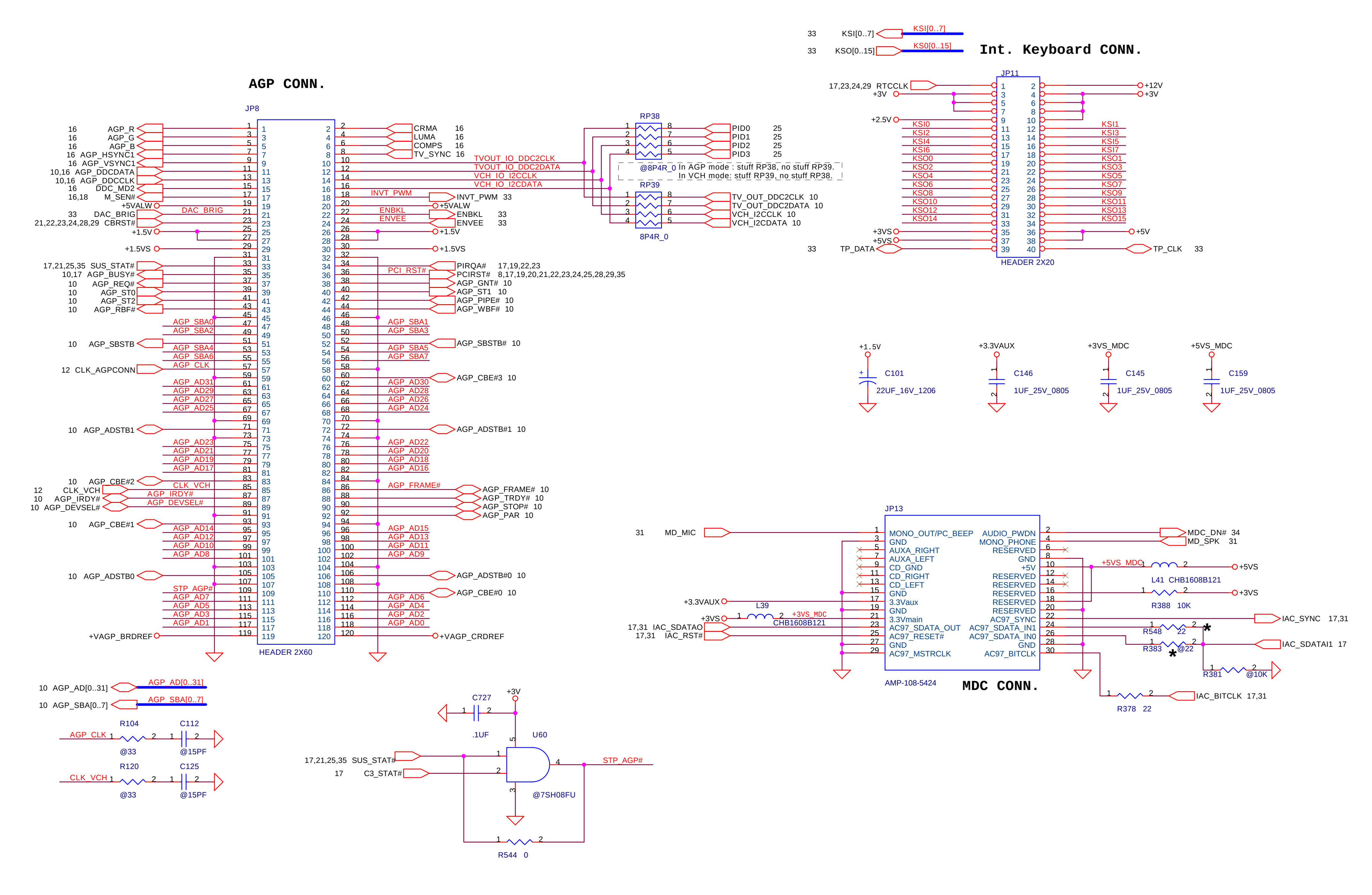

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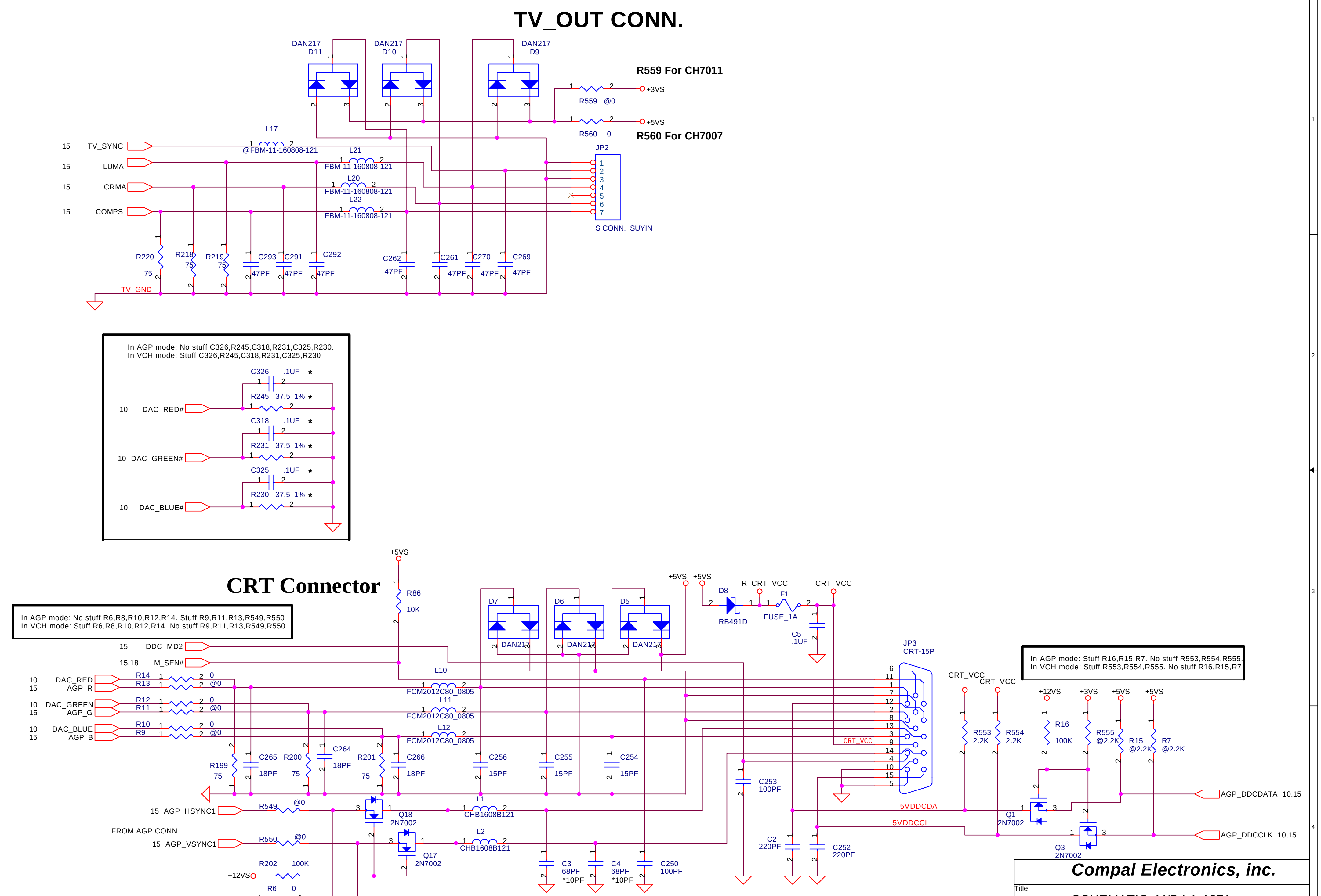

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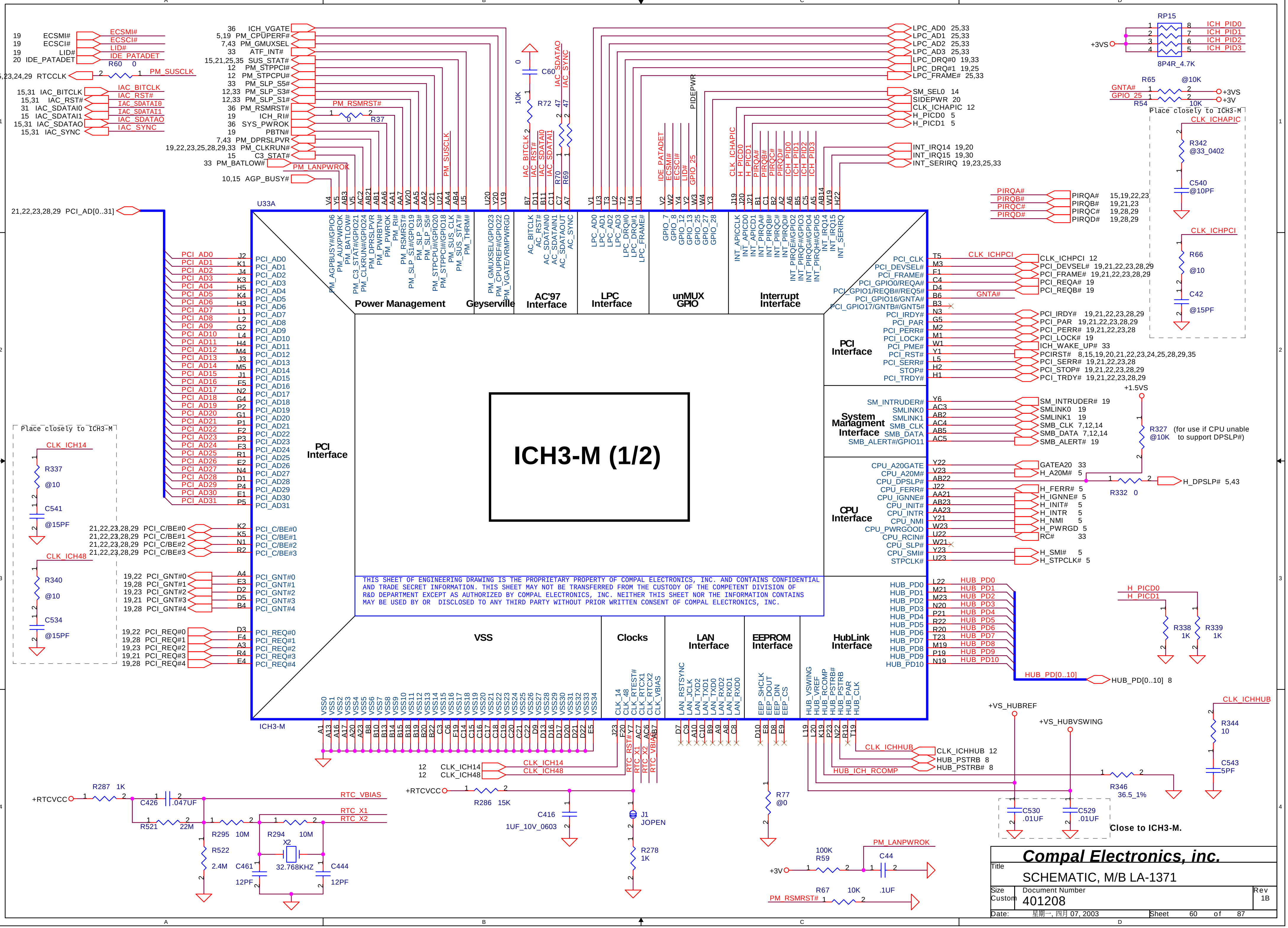

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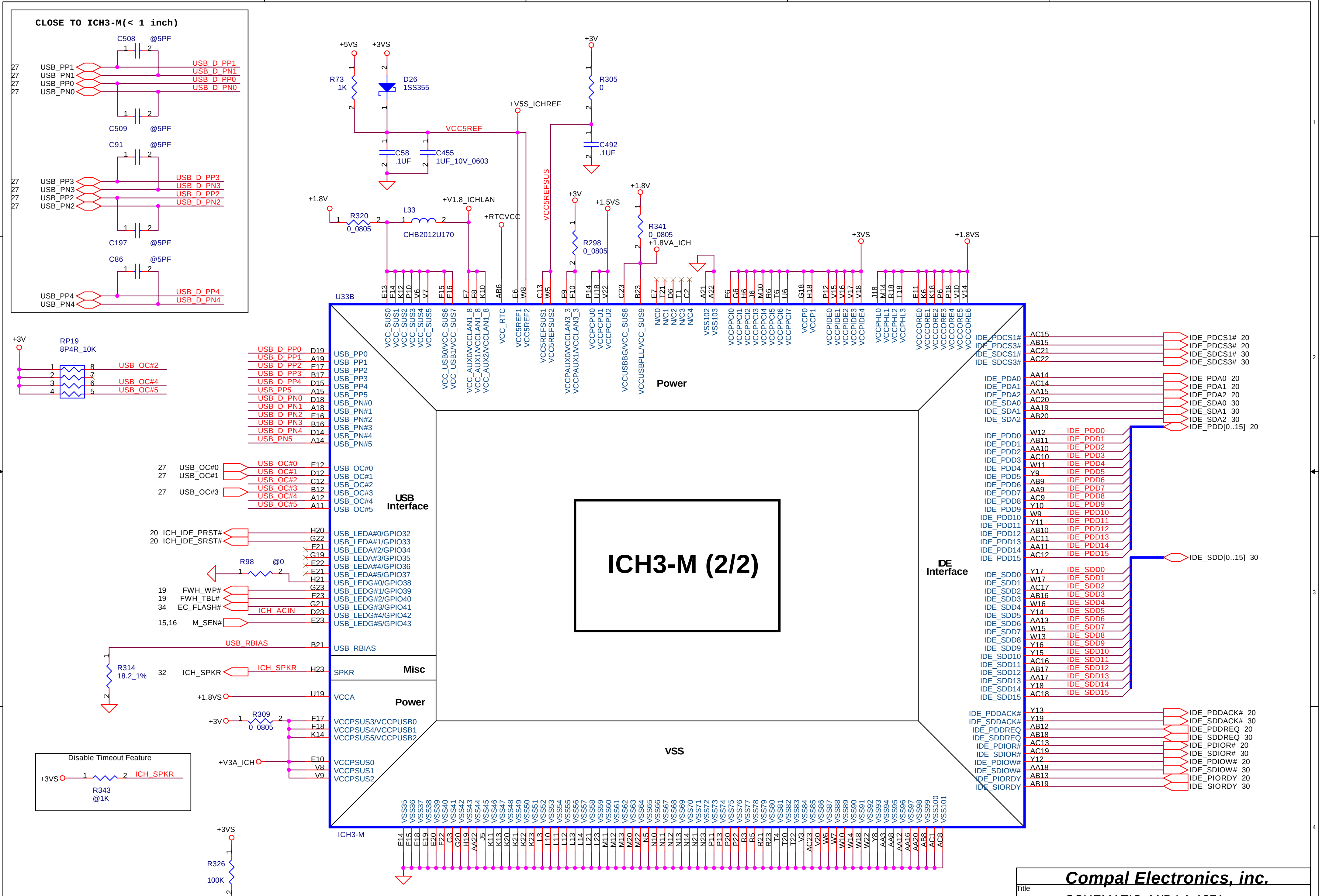

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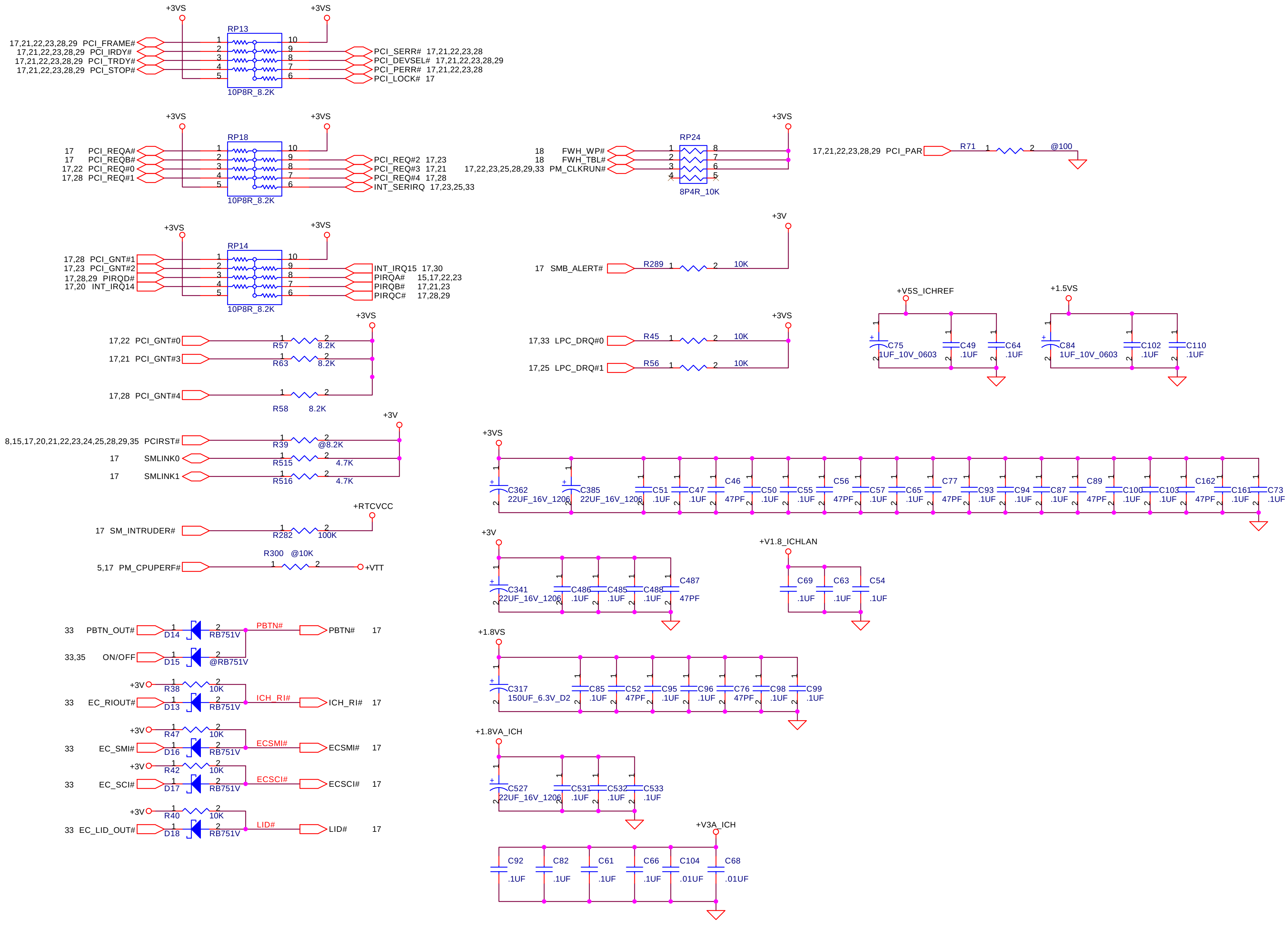

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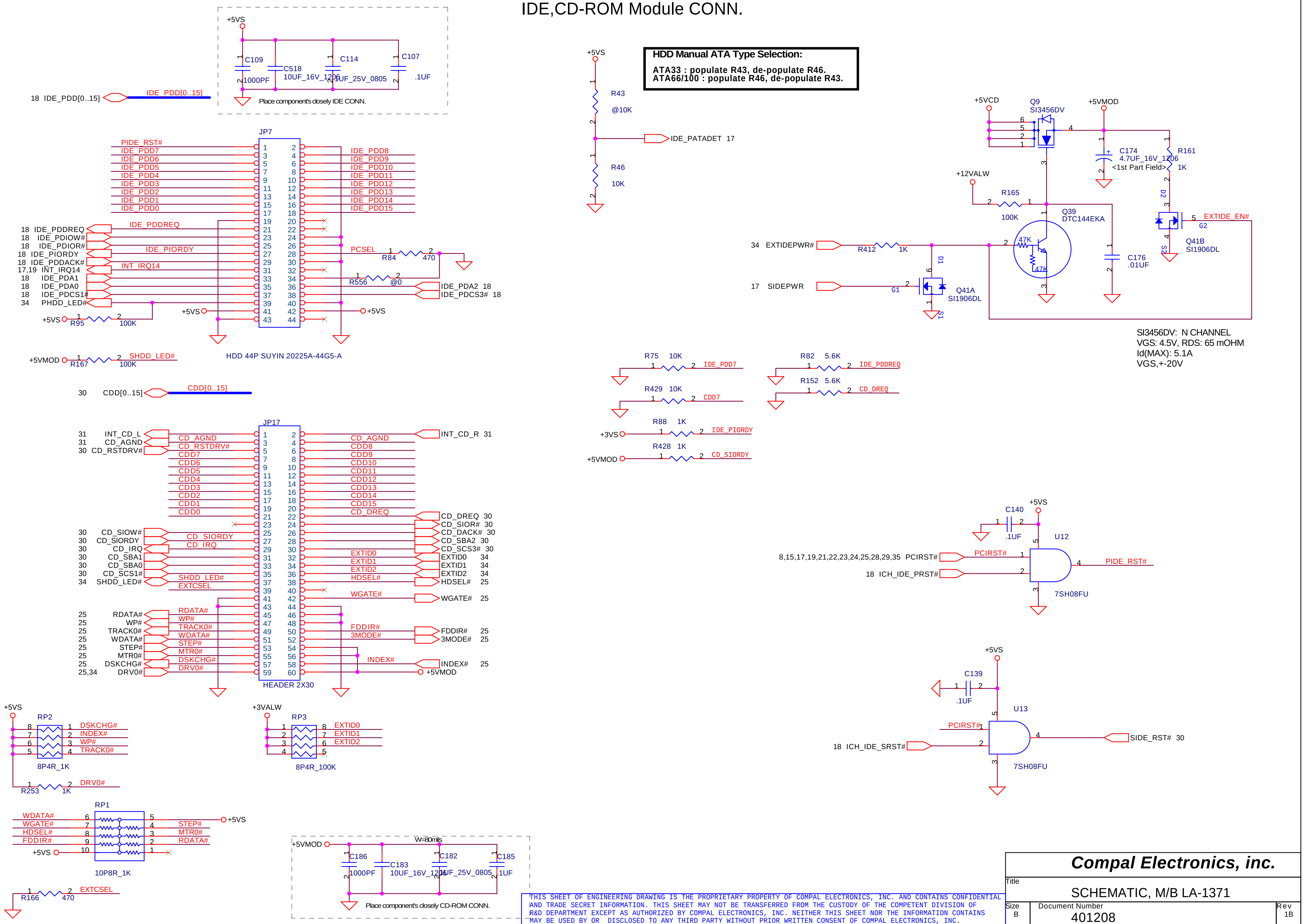
IDE,CD-ROM Module CONN.



HDD Manual ATA Type Selection:

ATA33 : populate R43, de-populate R46.
ATA66/100 : populate R46, de-populate R43.

SI3456DV: N CHANNEL
VGS: 4.5V, RDS: 65 mOHM
Id(MAX): 5.1A
VGS,+-20V

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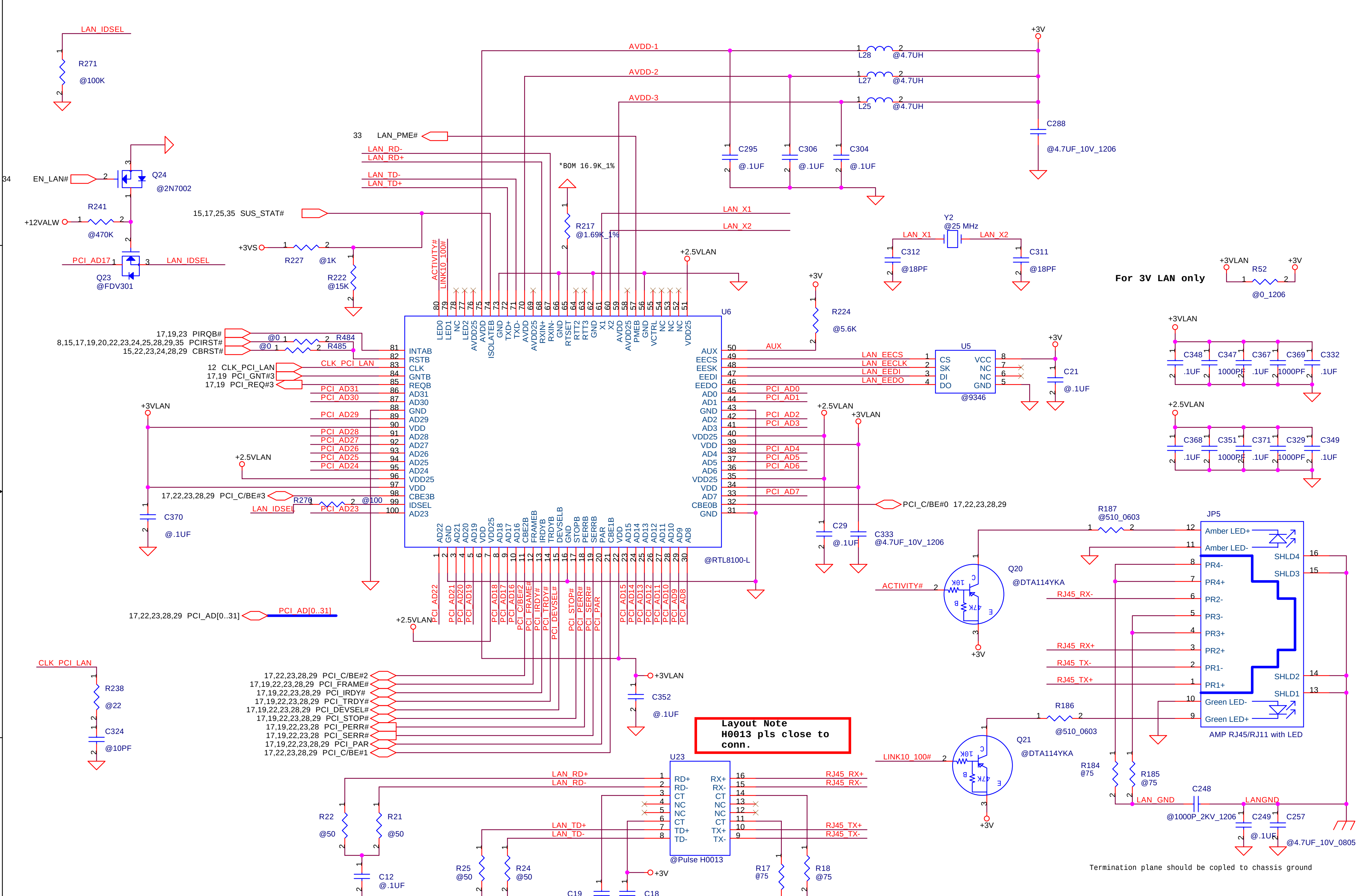

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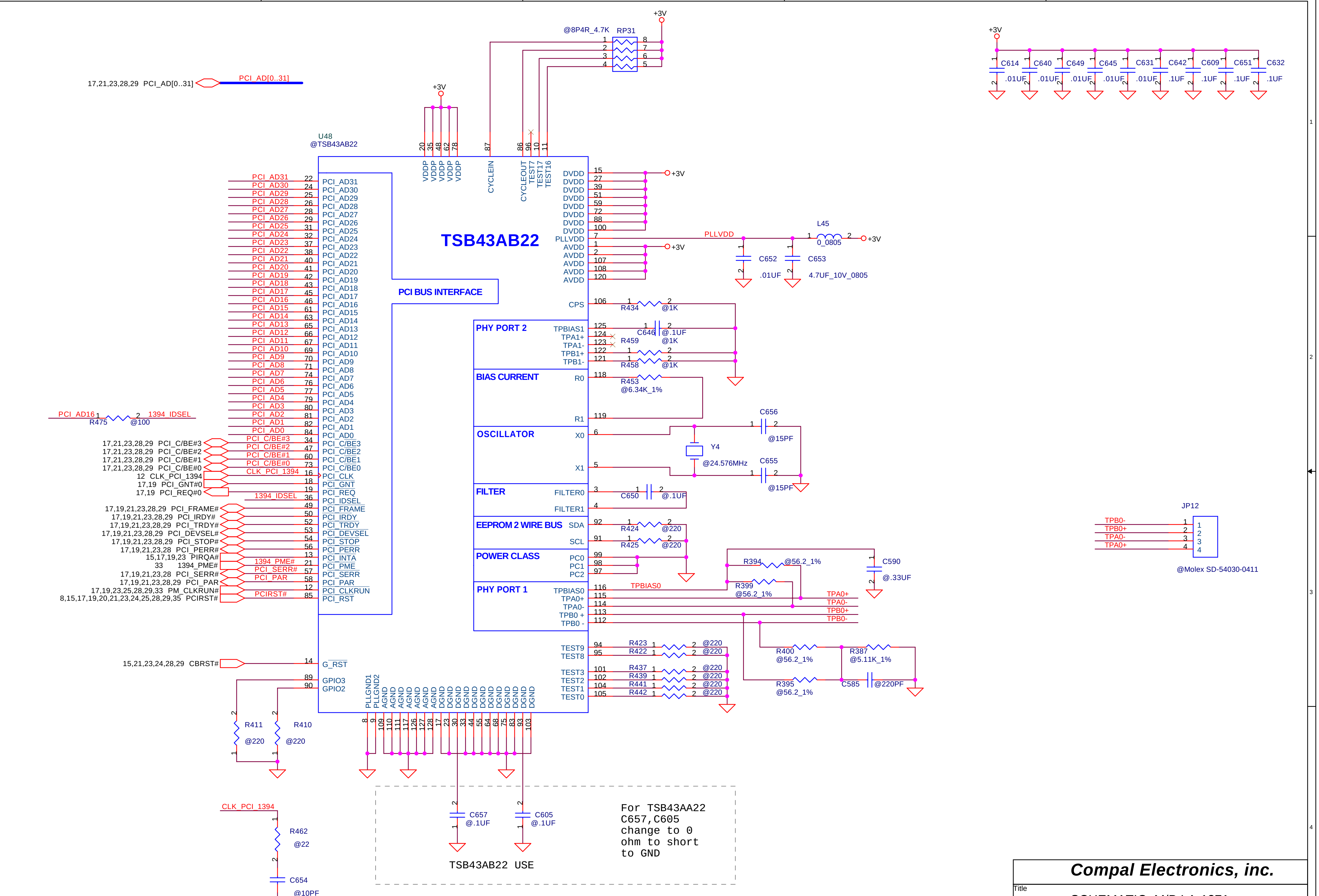

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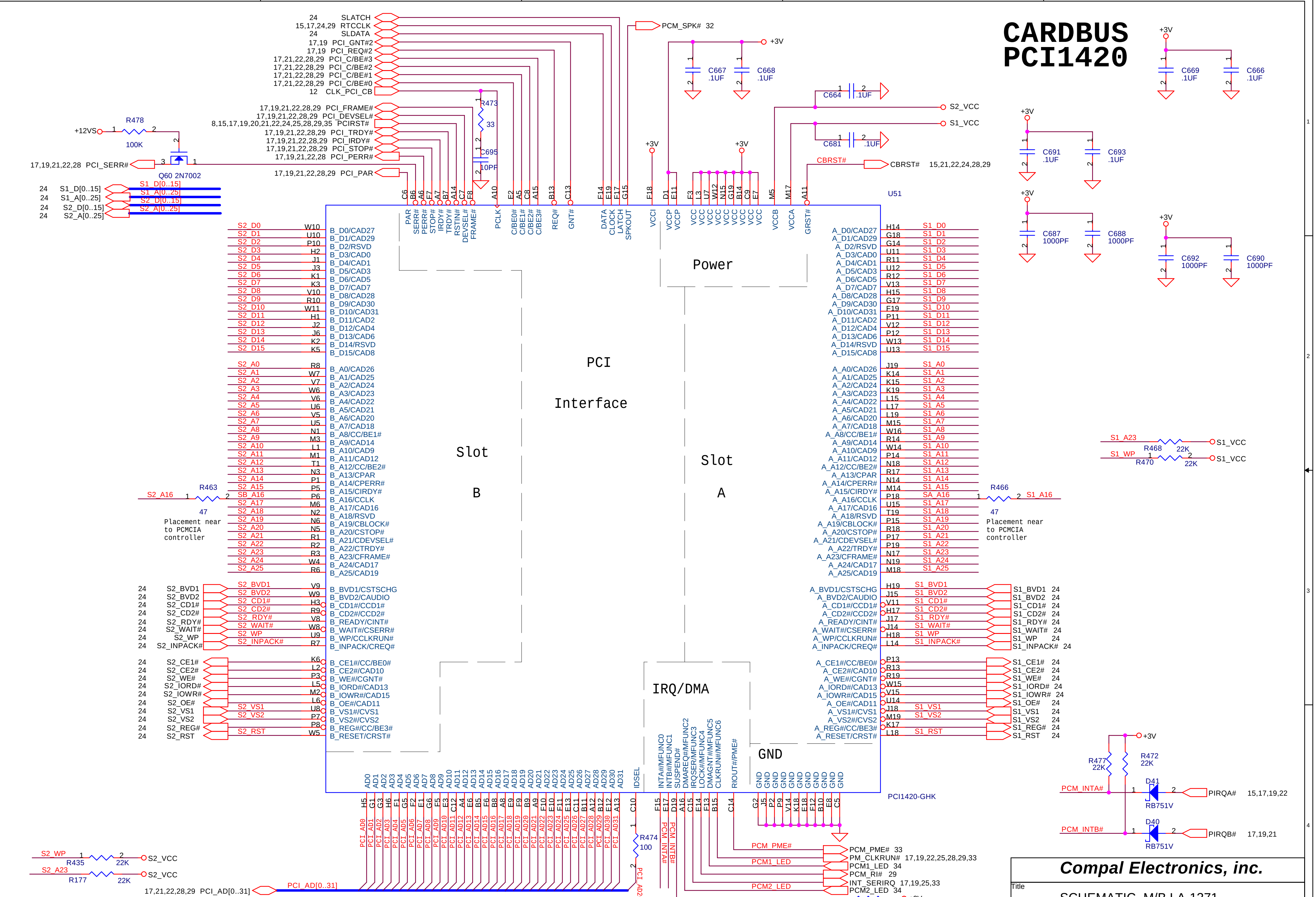

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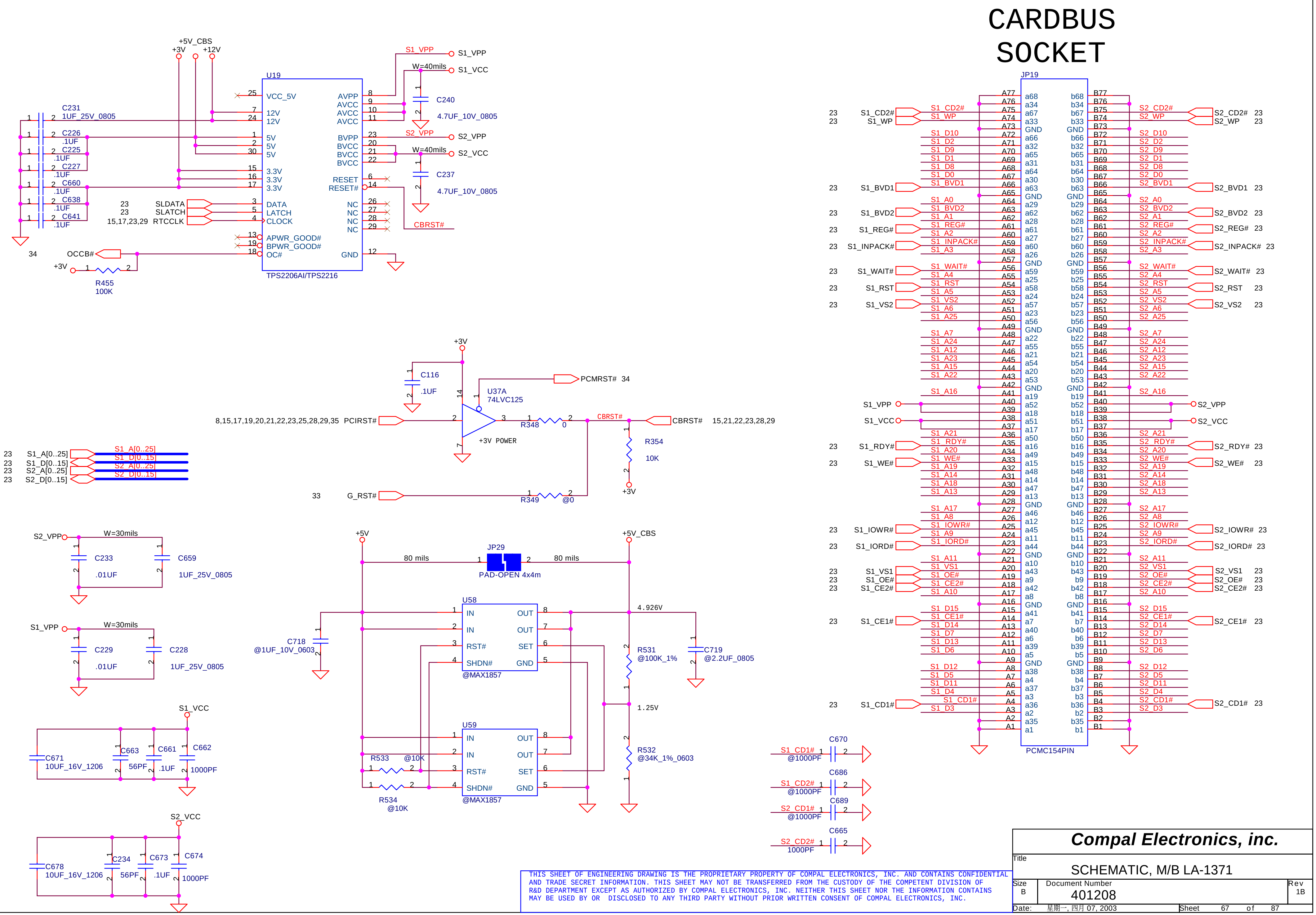
PCMCIA POWER CTRL.



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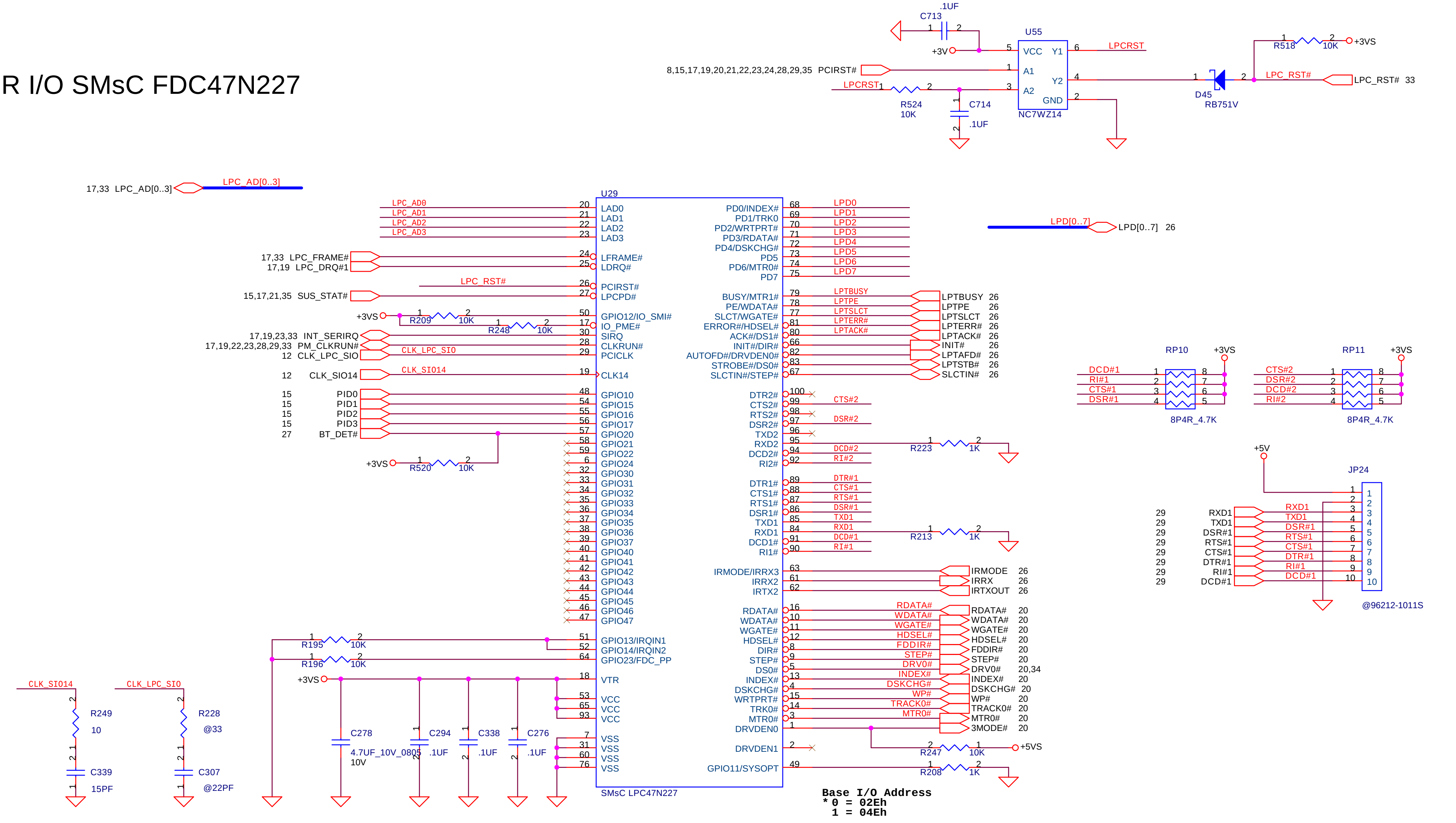
SUPER I/O SMsC FDC47N227



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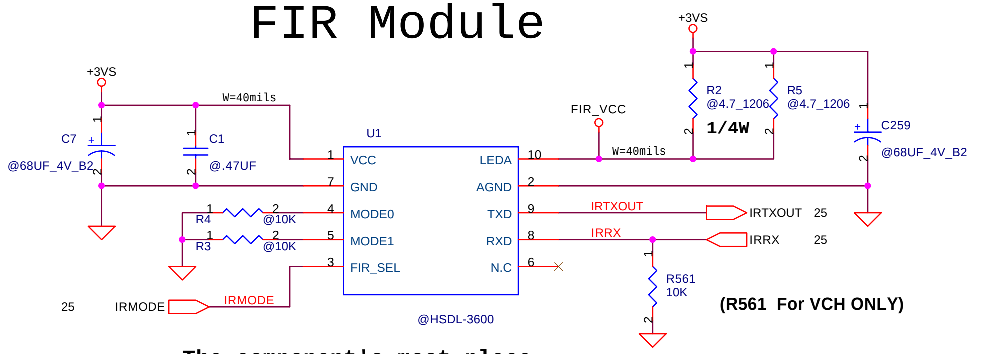
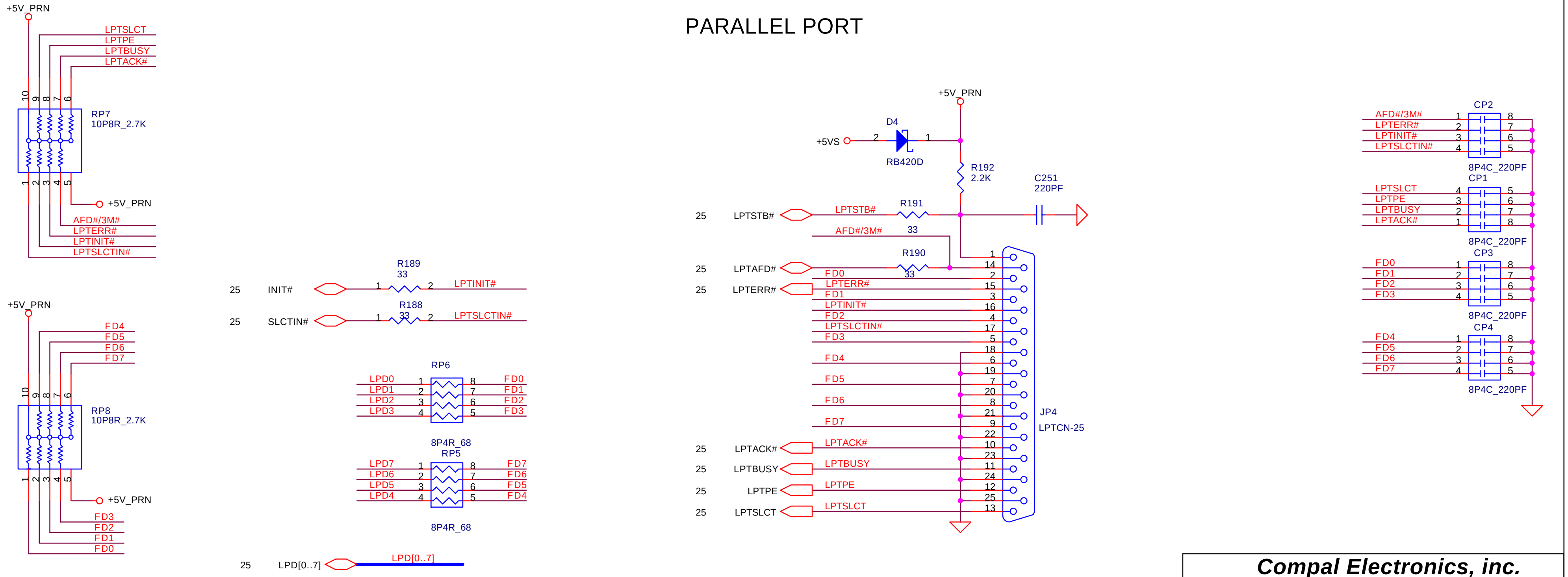
FIR Module



The component's most place cloely IRDA MODULE.

PARALLEL PORT



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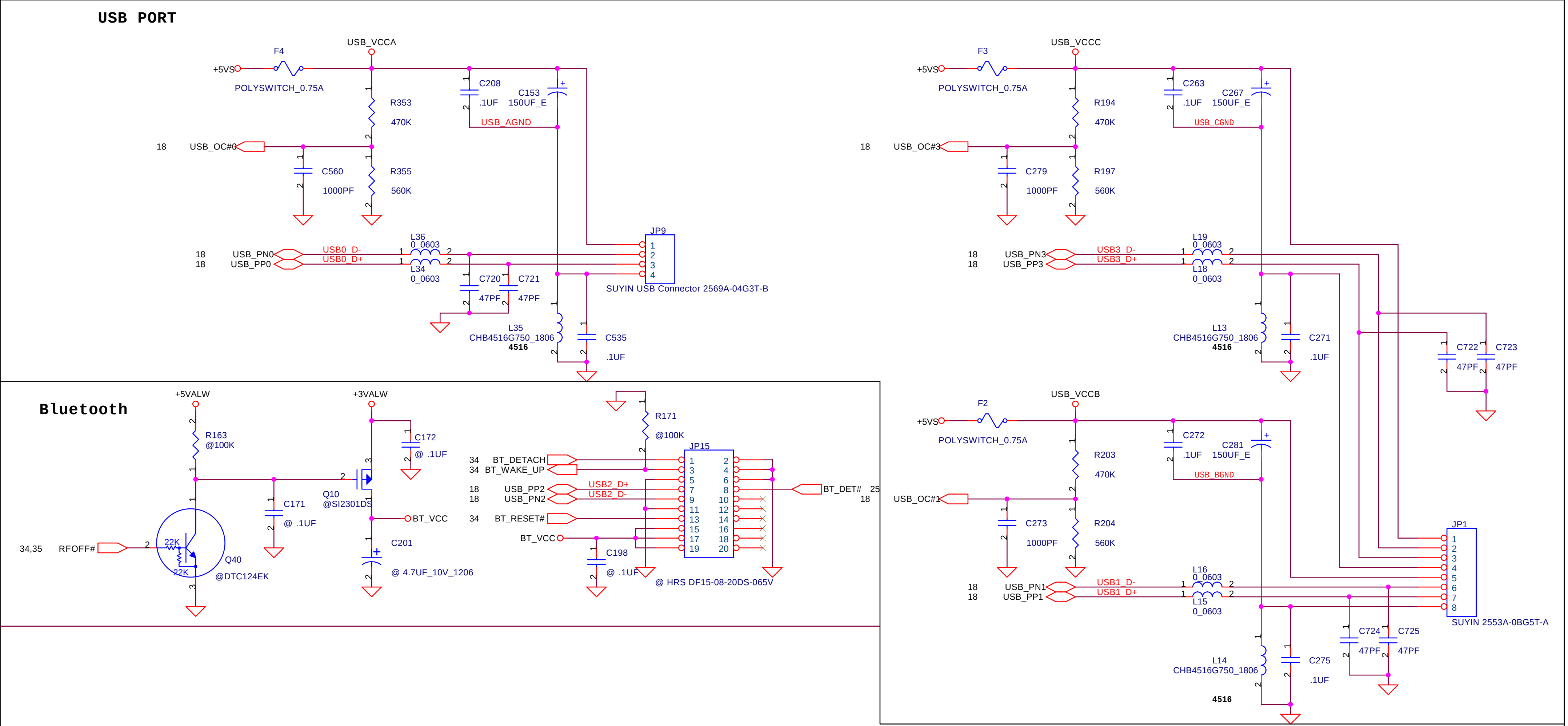

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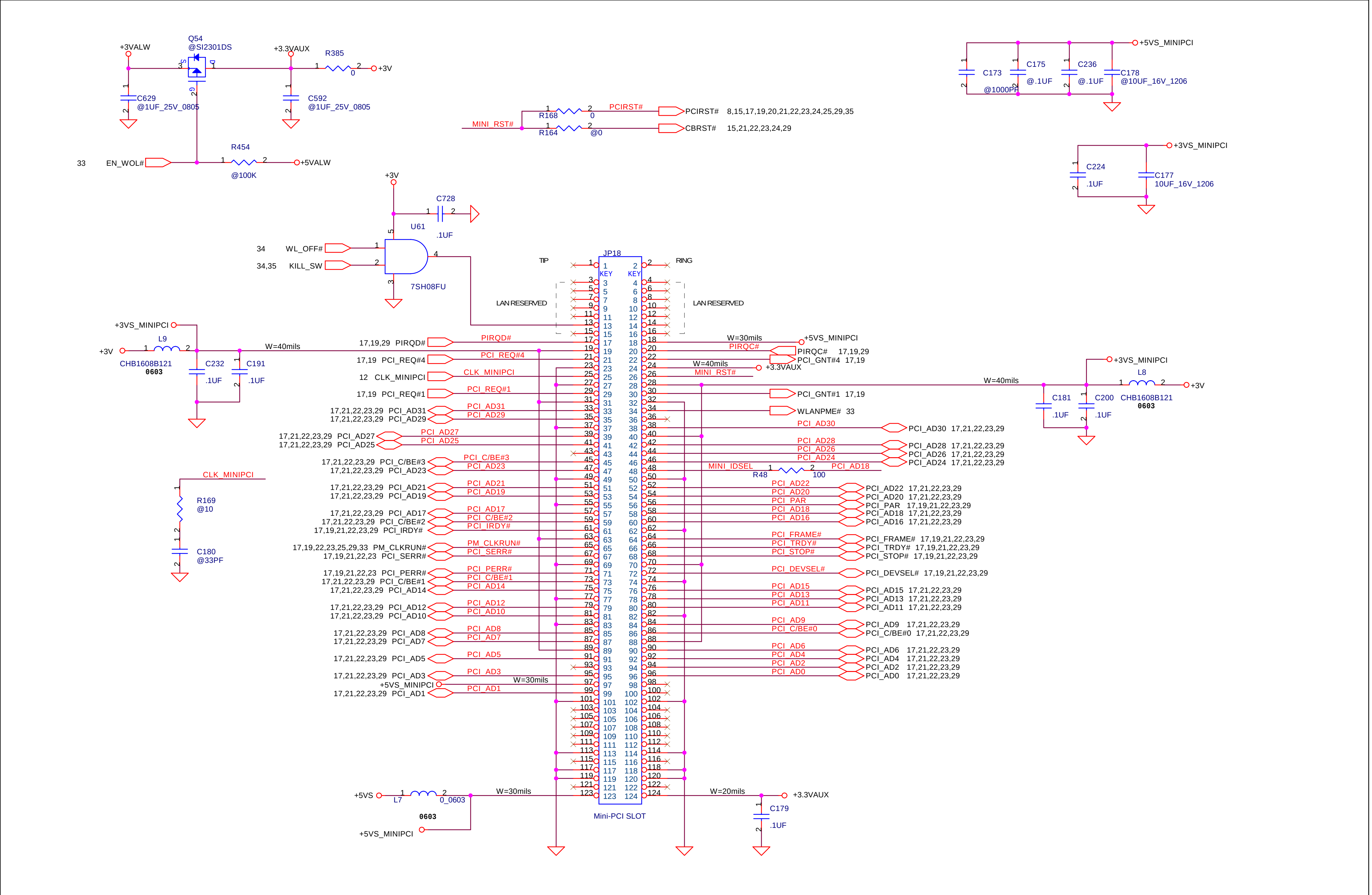

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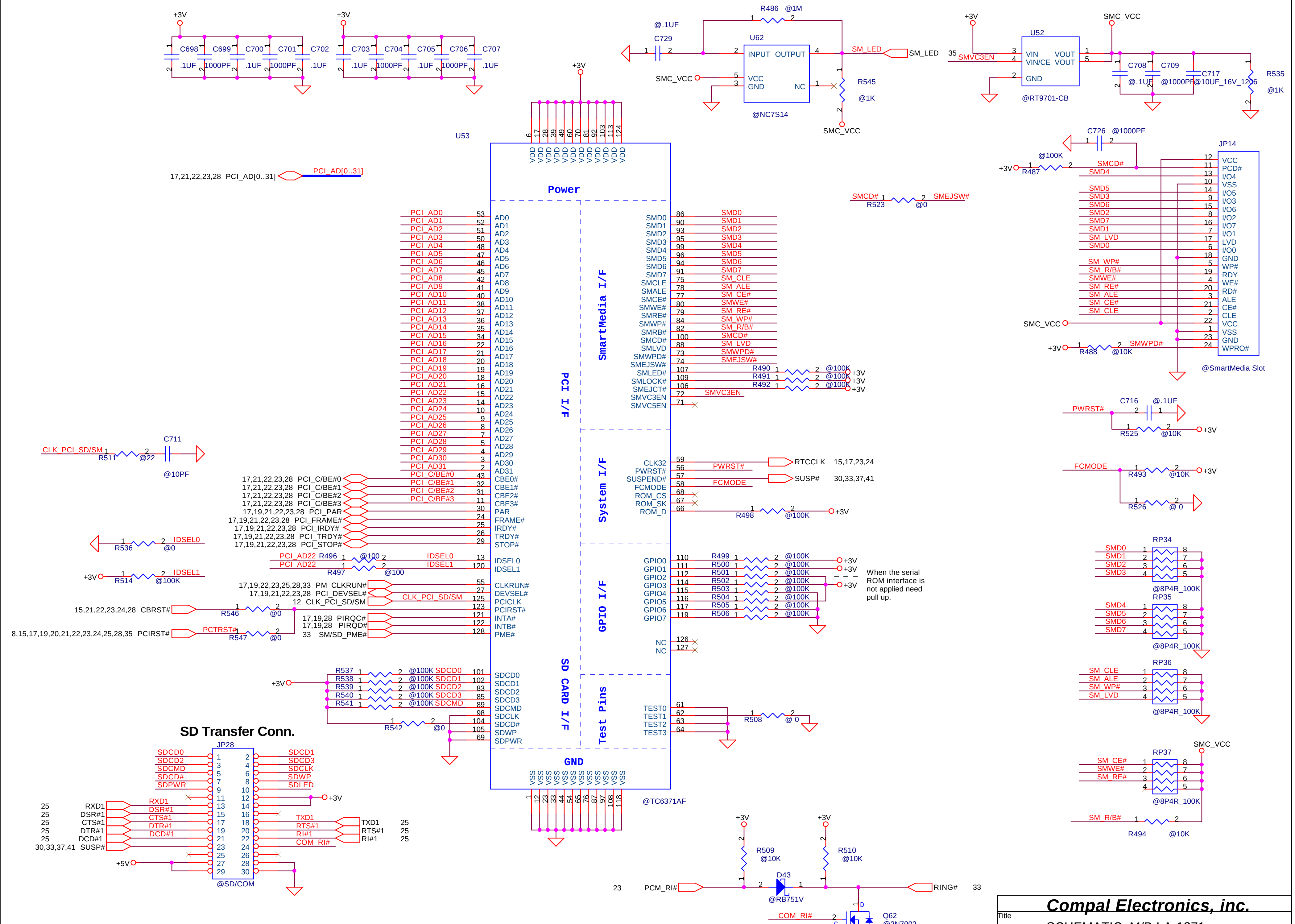

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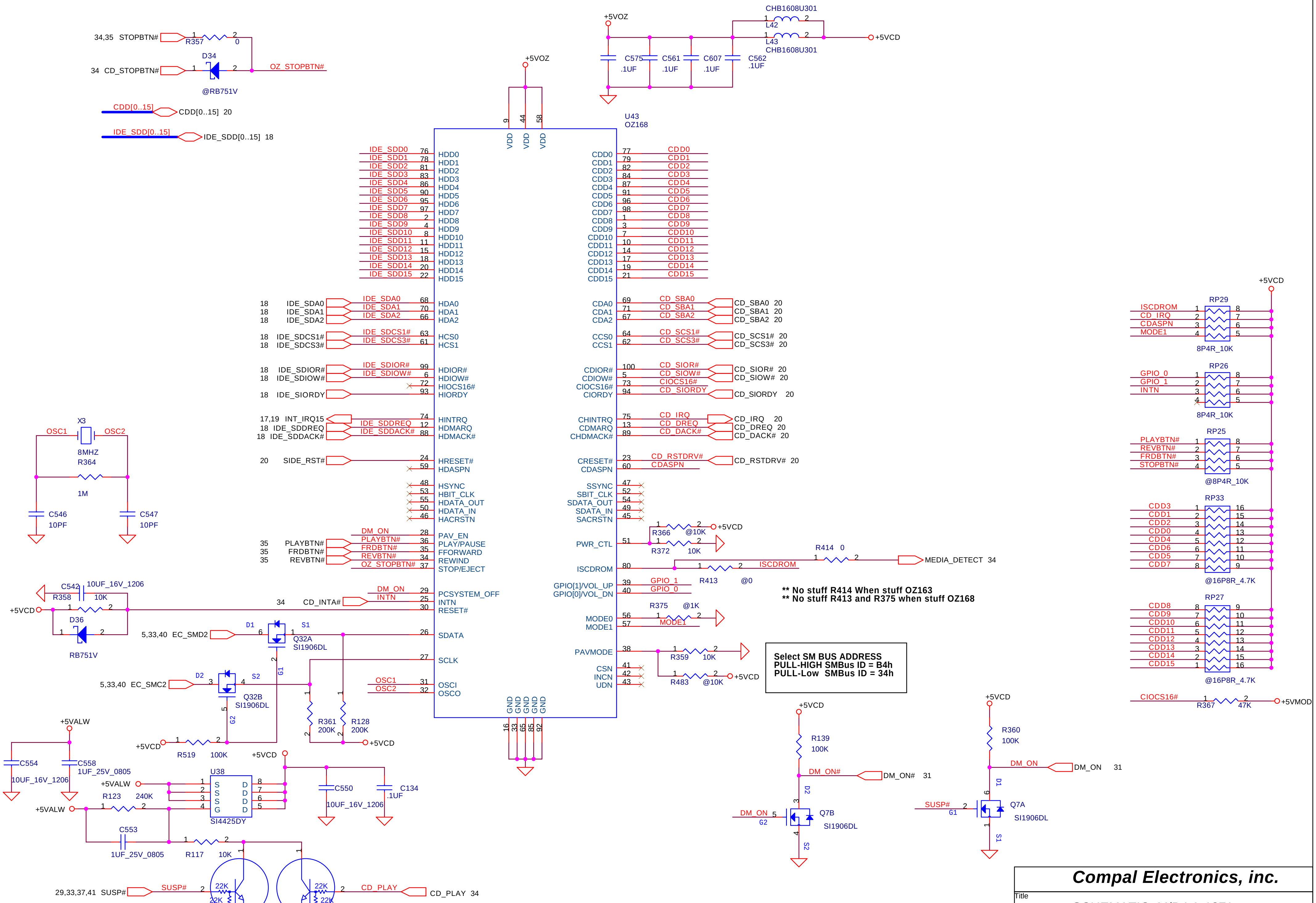

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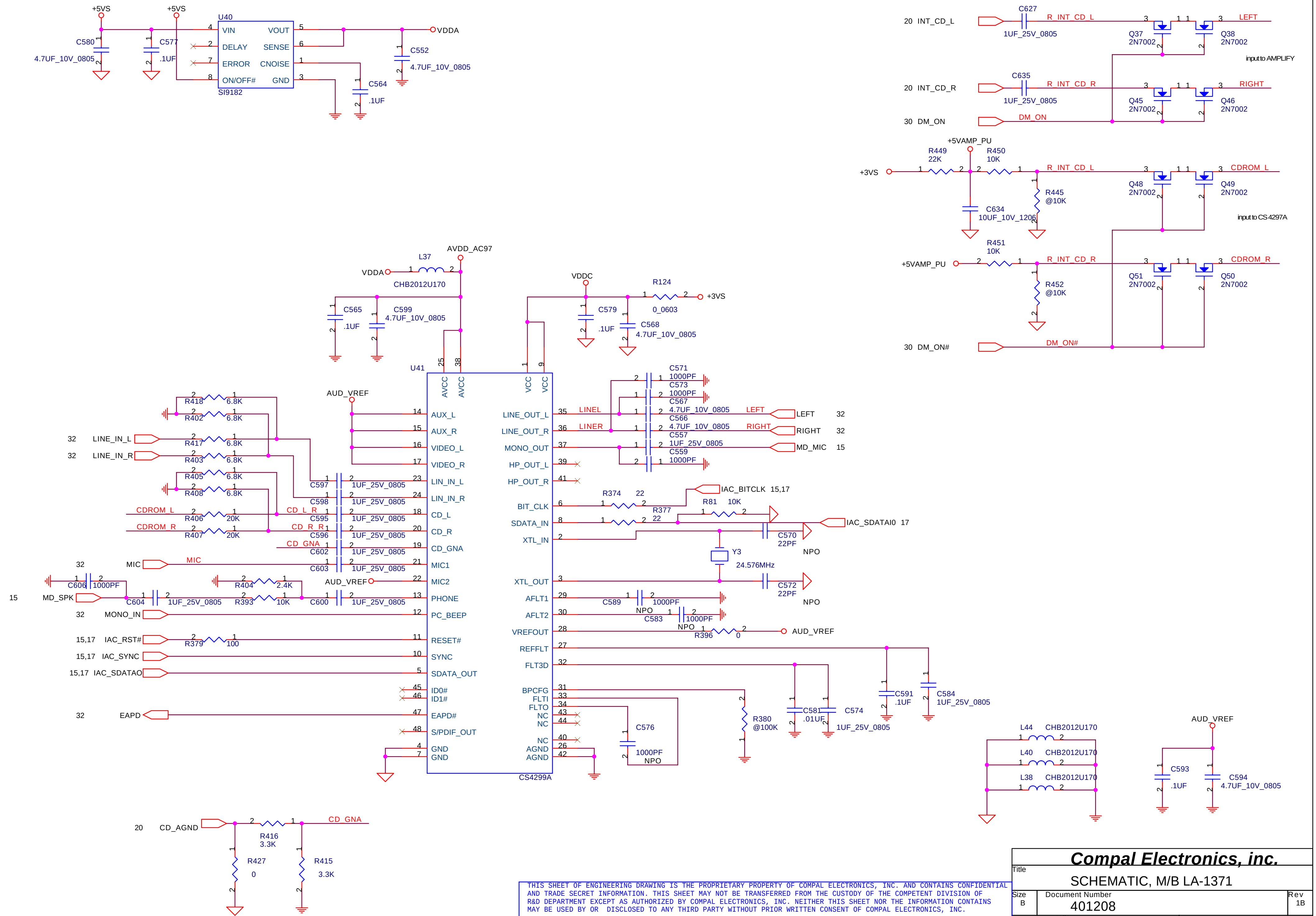
AC97 Codec



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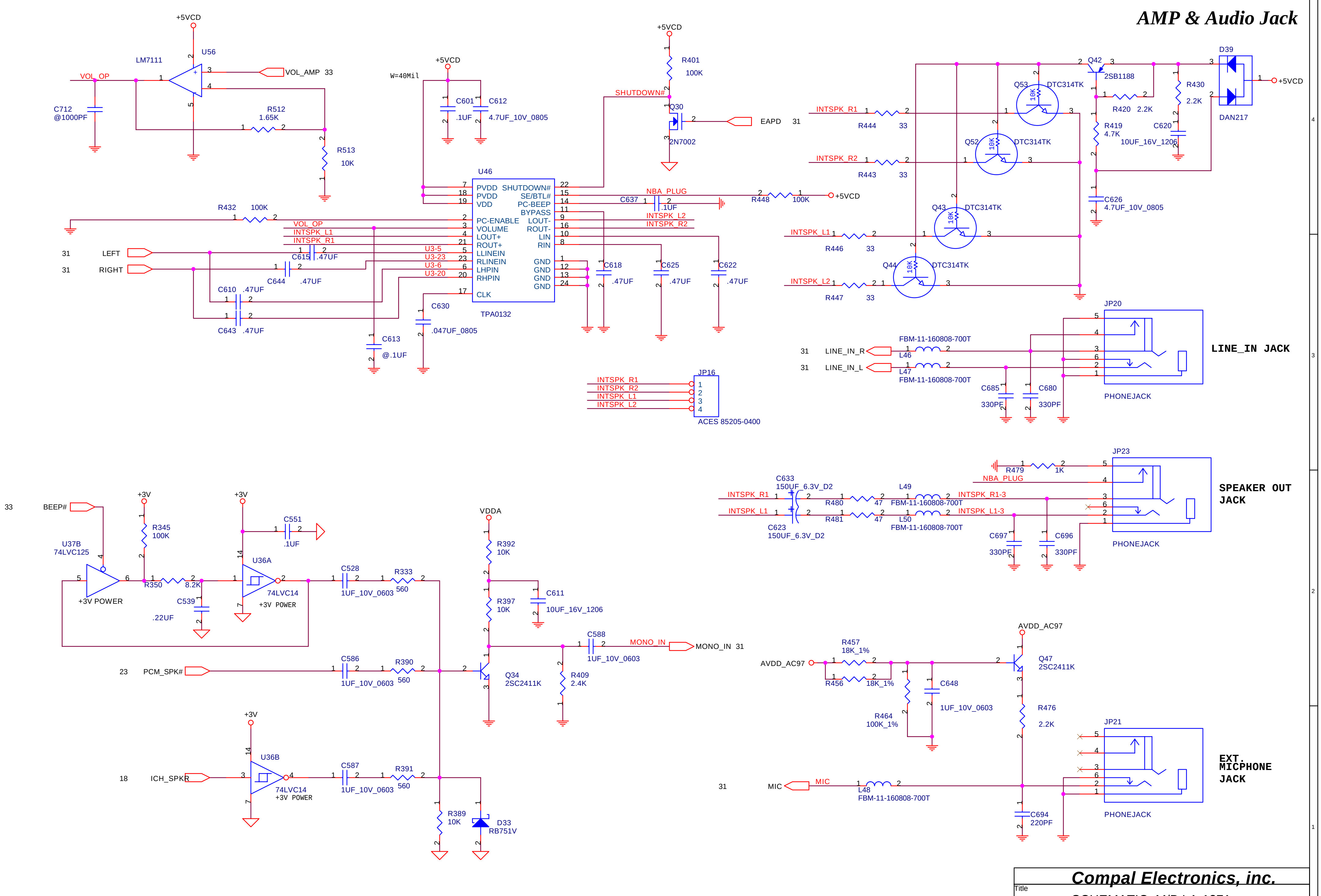
AMP & Audio Jack



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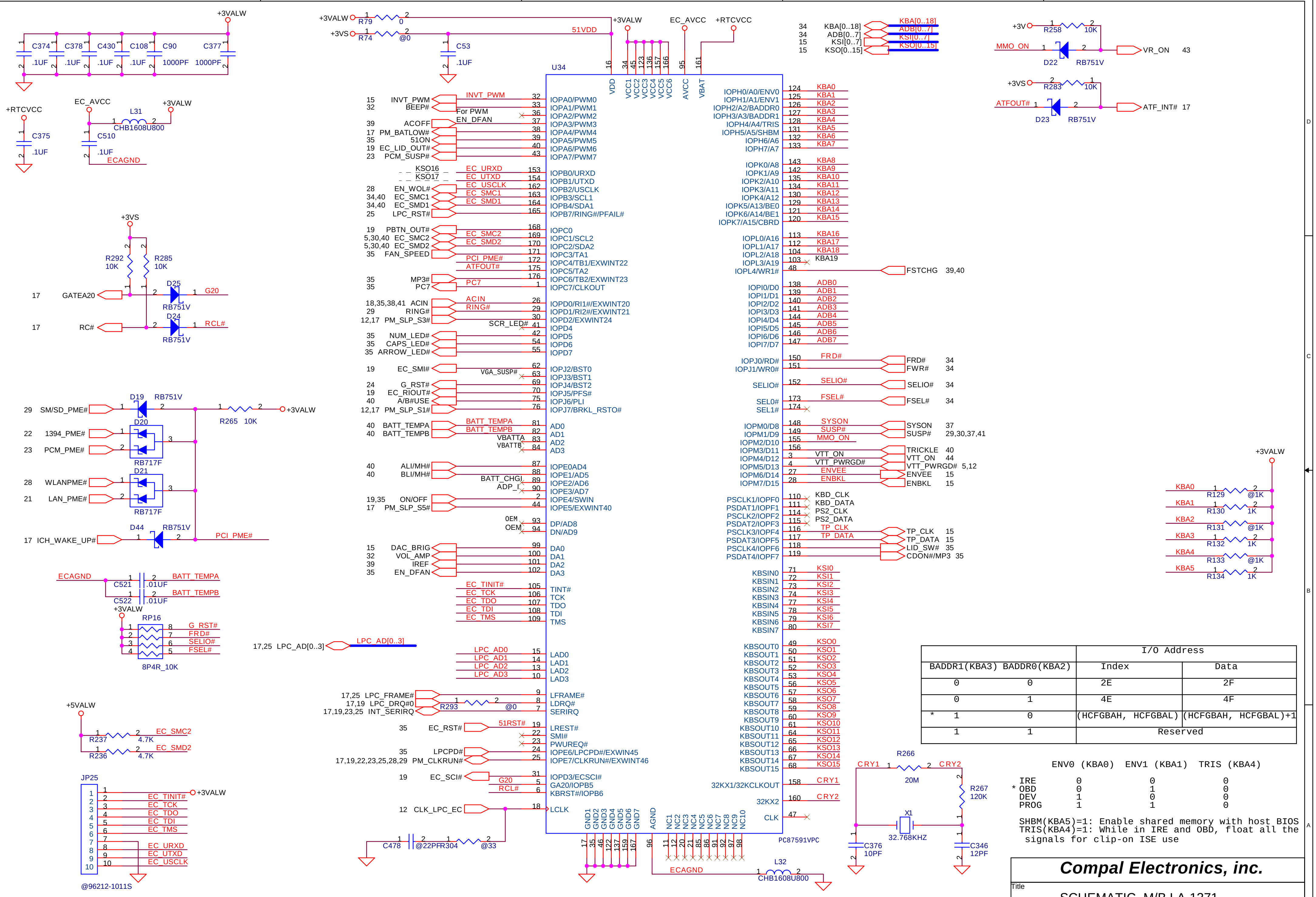

BADDR1(KBA3)	BADDR0(KBA2)	I/O Address Index	I/O Address Data
0	0	2E	2F
0	1	4E	4F
* 1	0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1	1	Reserved	

	ENV0 (KBA0)	ENV1 (KBA1)	TRIS (KBA4)
IRE	0	0	0
* OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

SHBM(KBA5)=1: Enable shared memory with host BIOS
TRIS(KBA4)=1: While in IRE and OBD, float all the signals for clip-on ISE use

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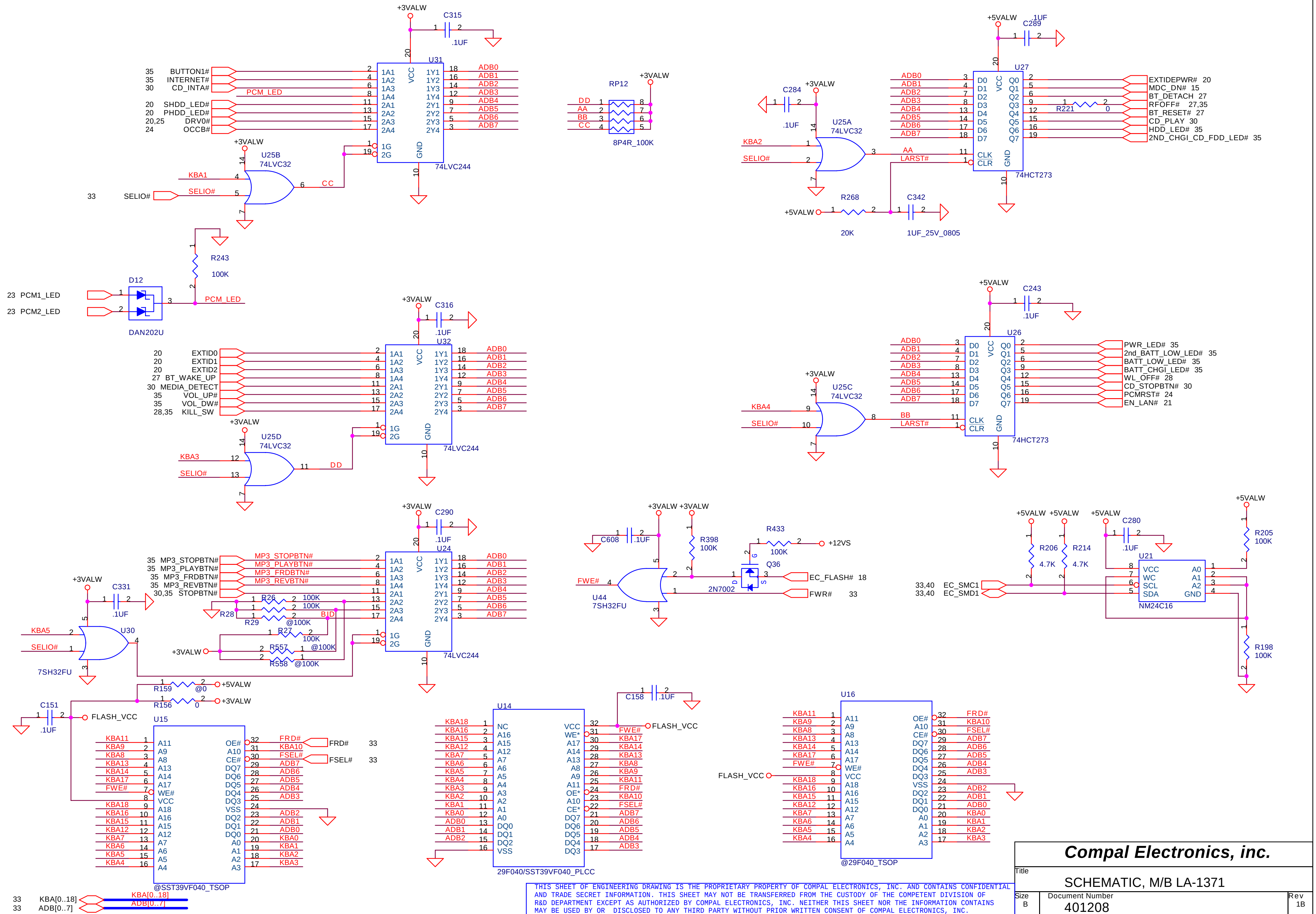

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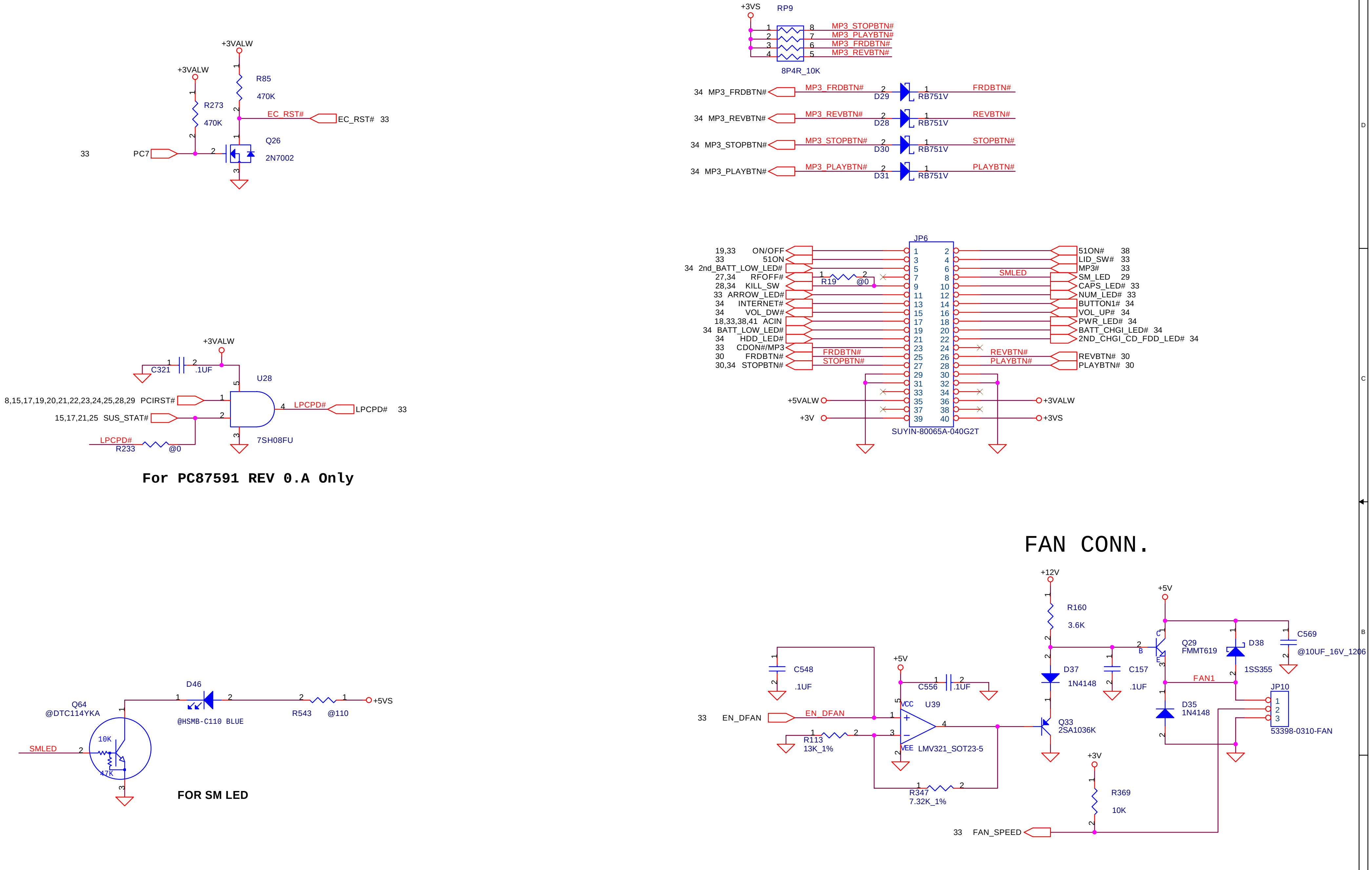

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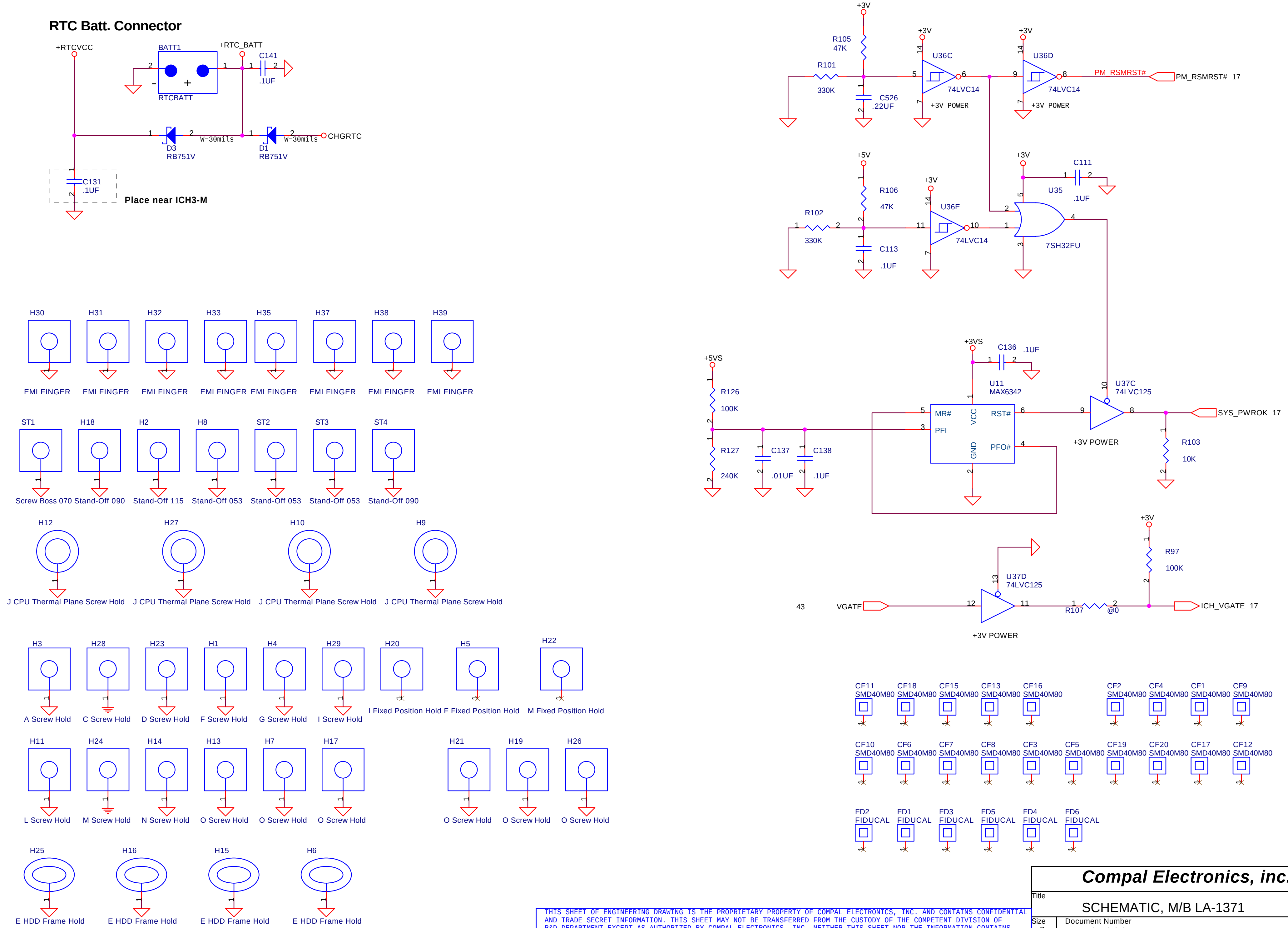

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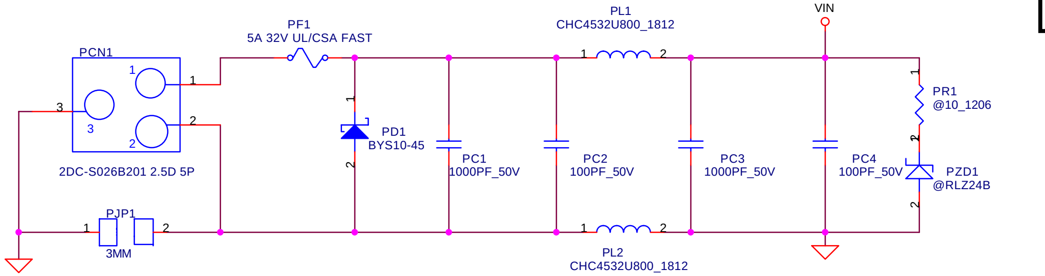
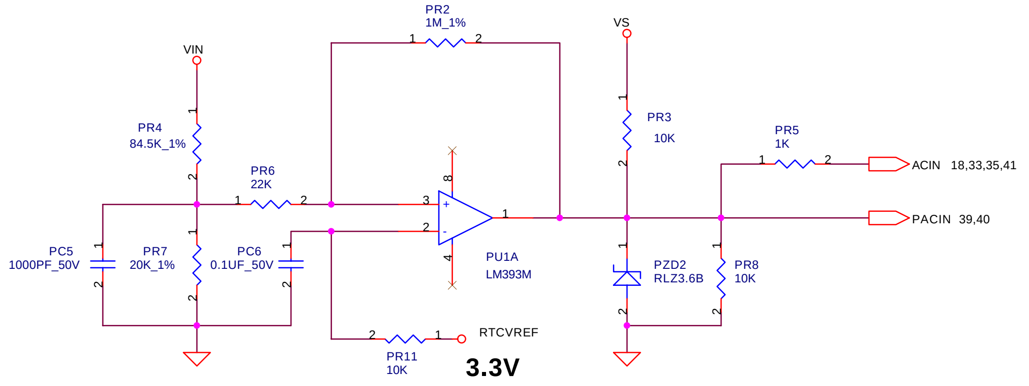
Vin Detector

High	18.764	17.901	17.063
Low	17.745	16.903	16.038

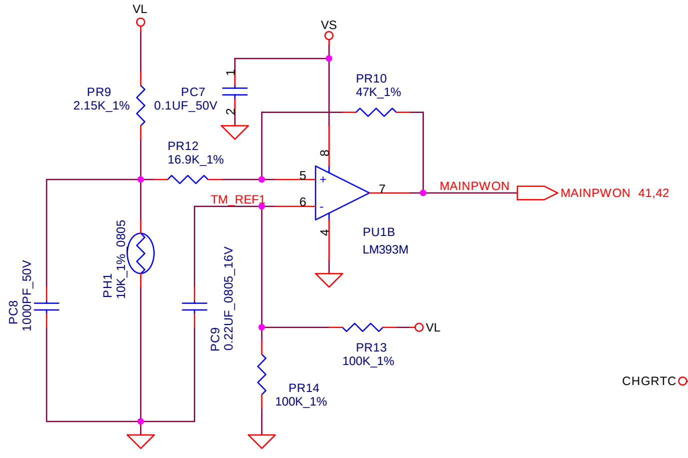


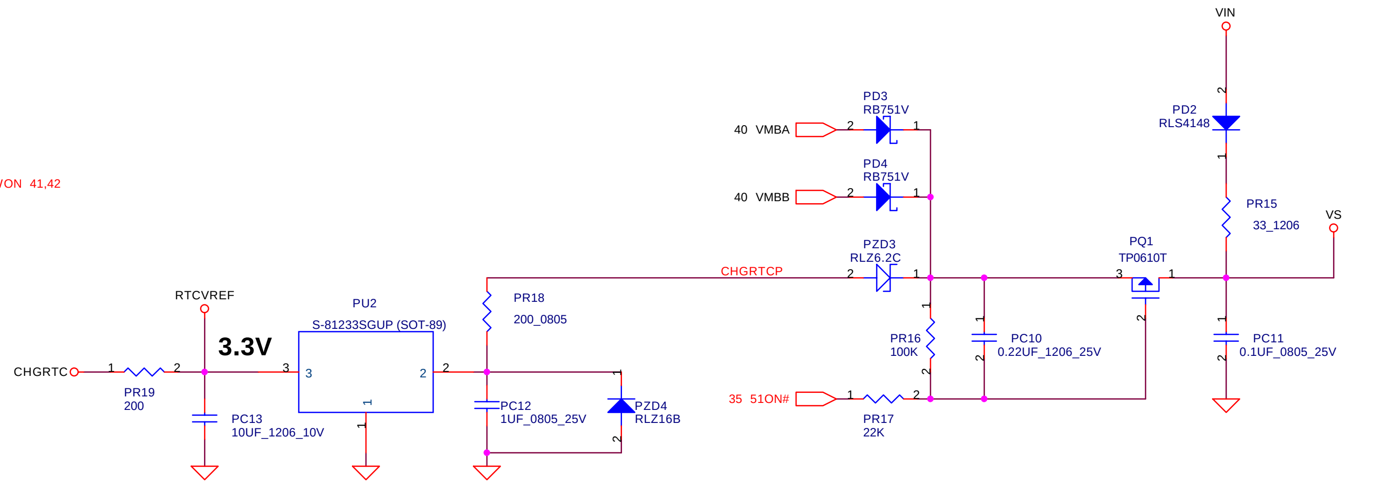


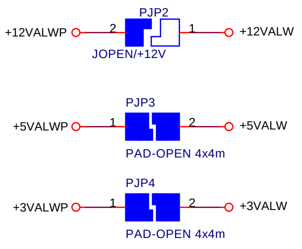
PH1 under CPU botten side :

CPU thermal protection at 82 degree C

Recovery at 50(51) degree C



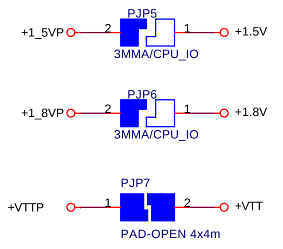




(120mA,20mils ,Via NO.= 1)

(5A,200mils ,Via NO.= 10)

(5A,200mils ,Via NO.= 10)



(1.5A,60mils ,Via NO.= 3)

(3A,120mils ,Via NO.= 6)

(6A,240mils ,Via NO.= 12)

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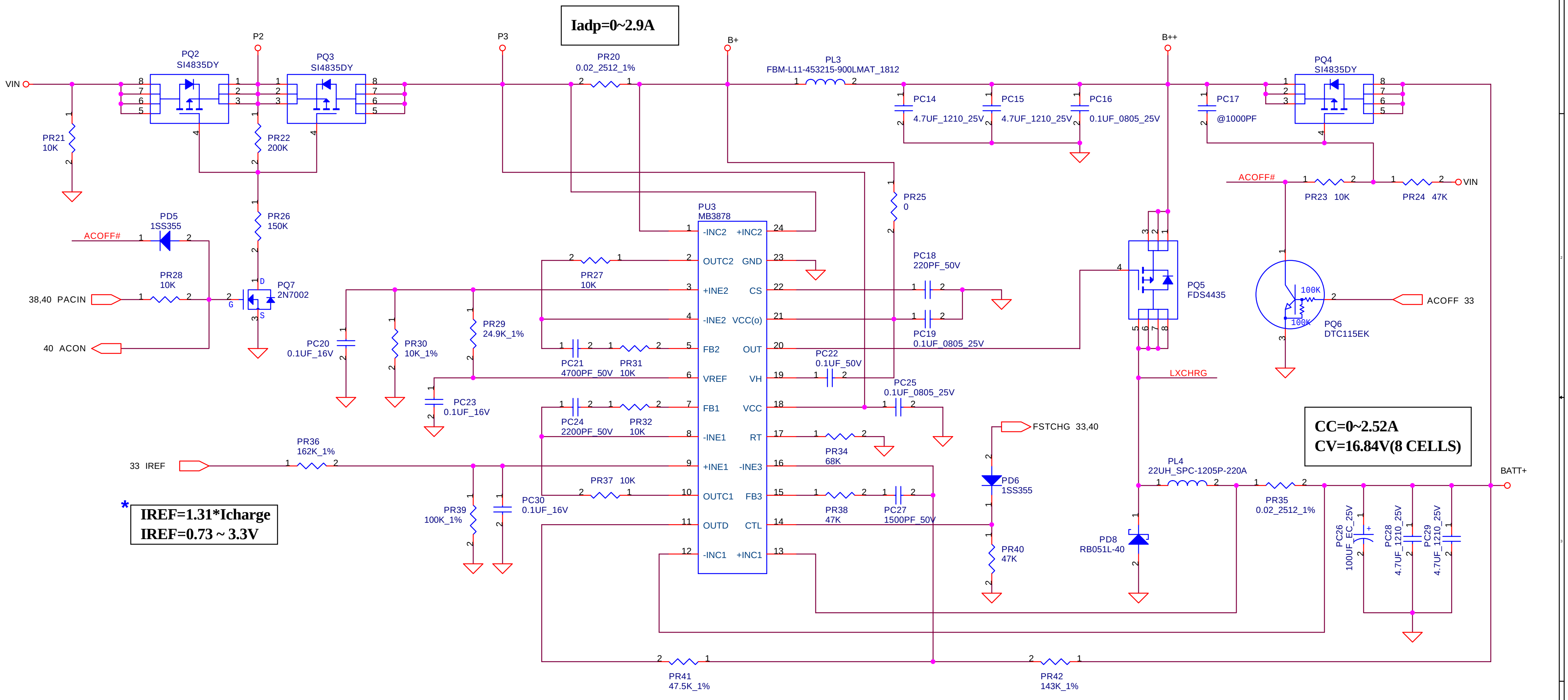

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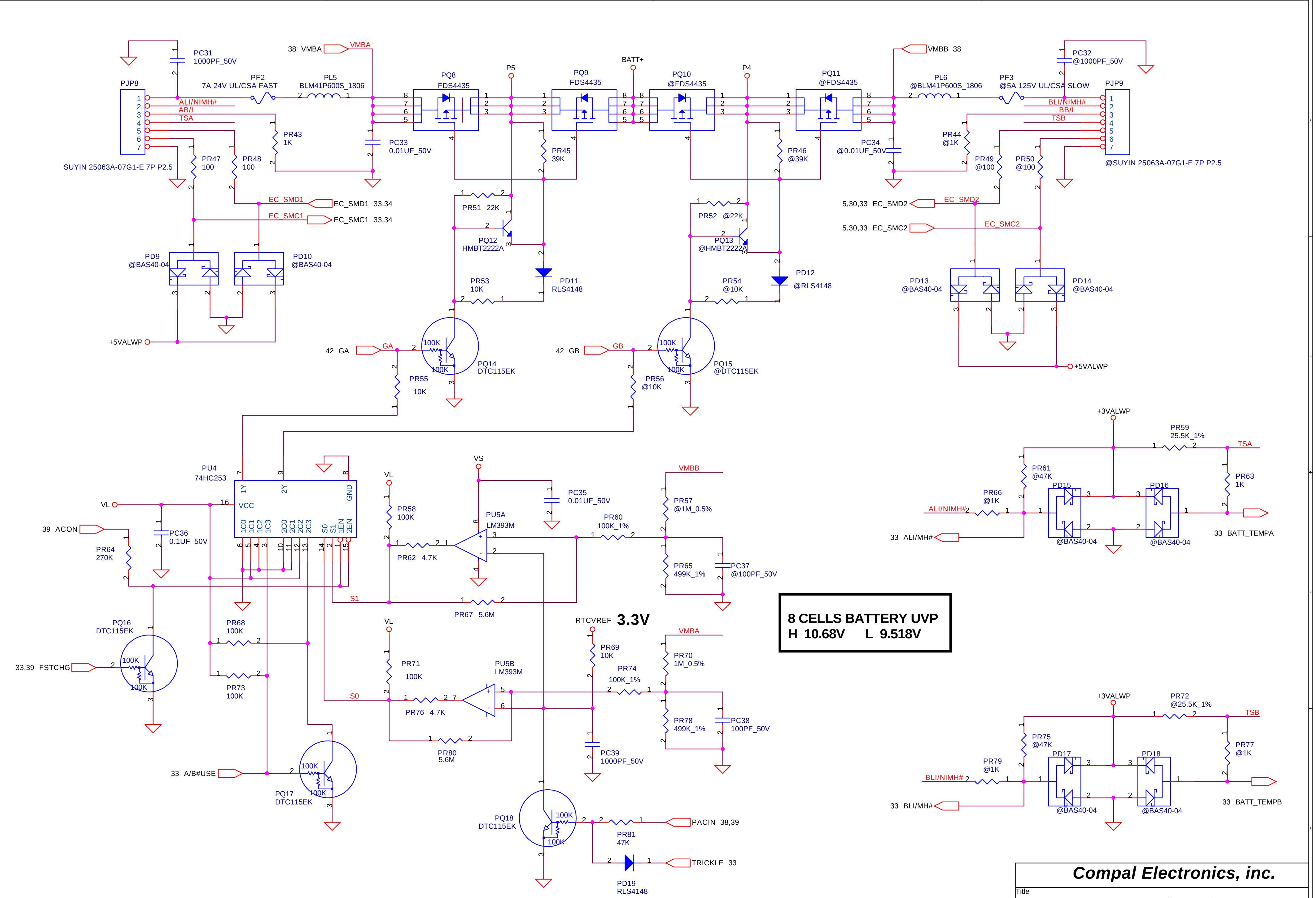

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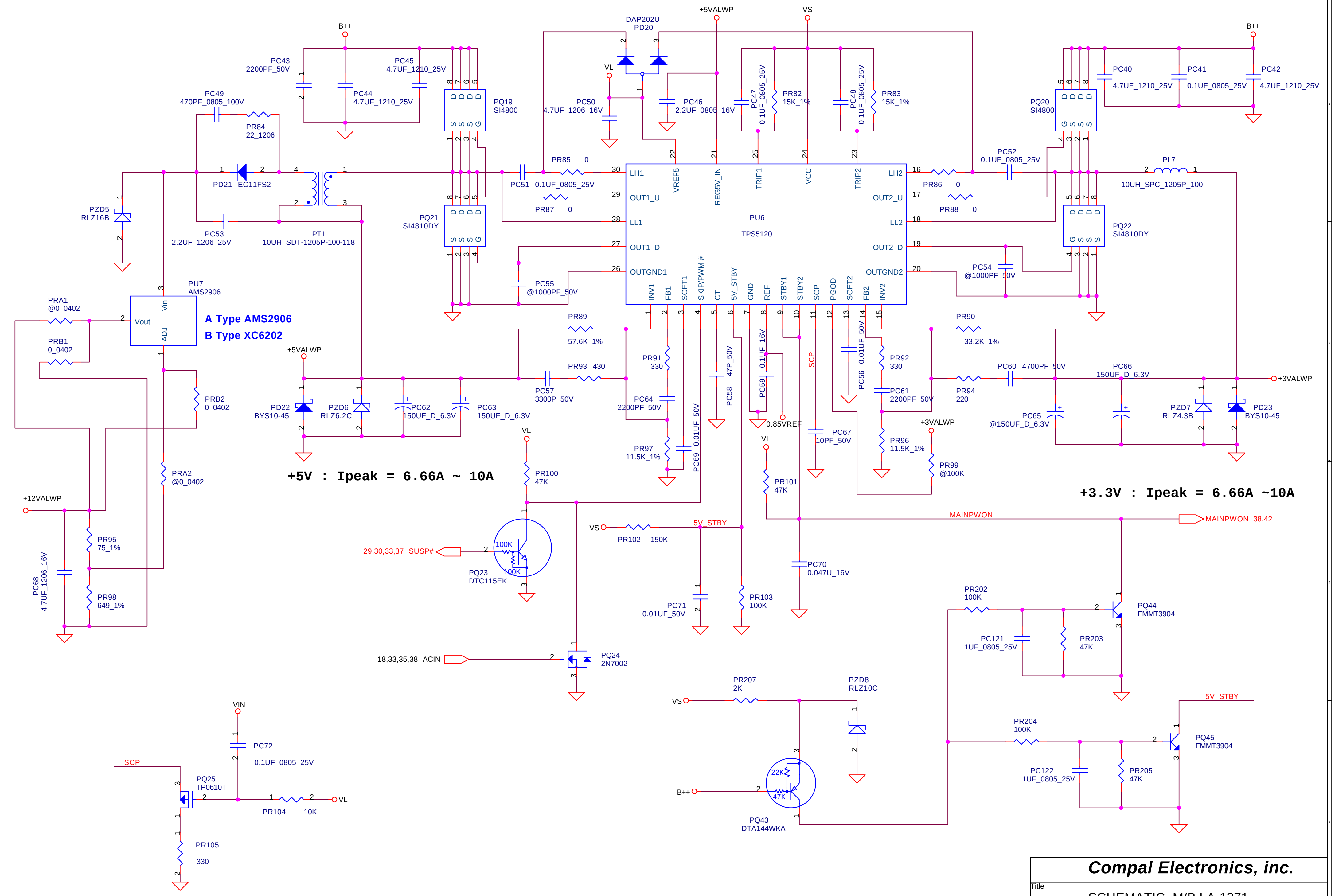

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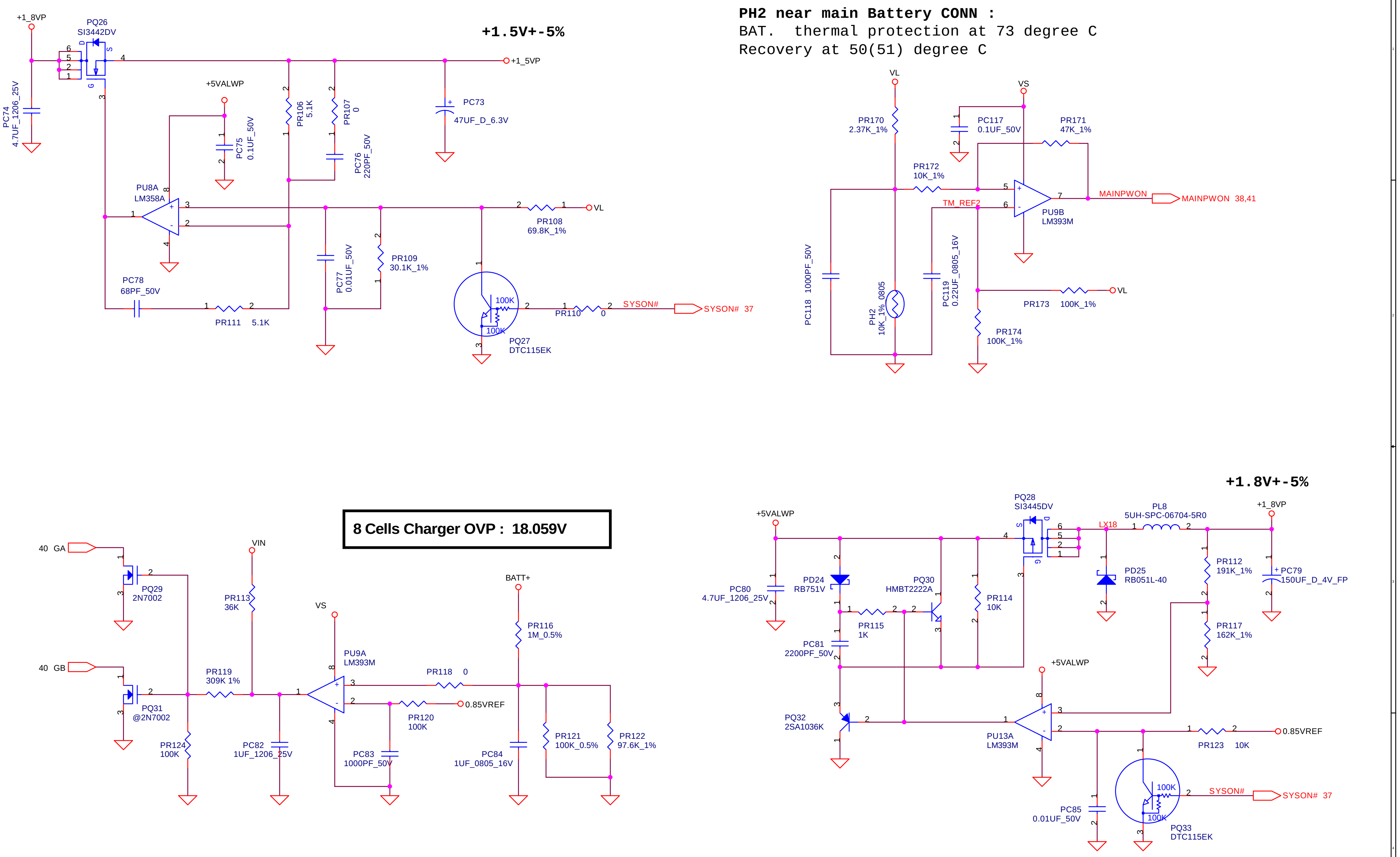

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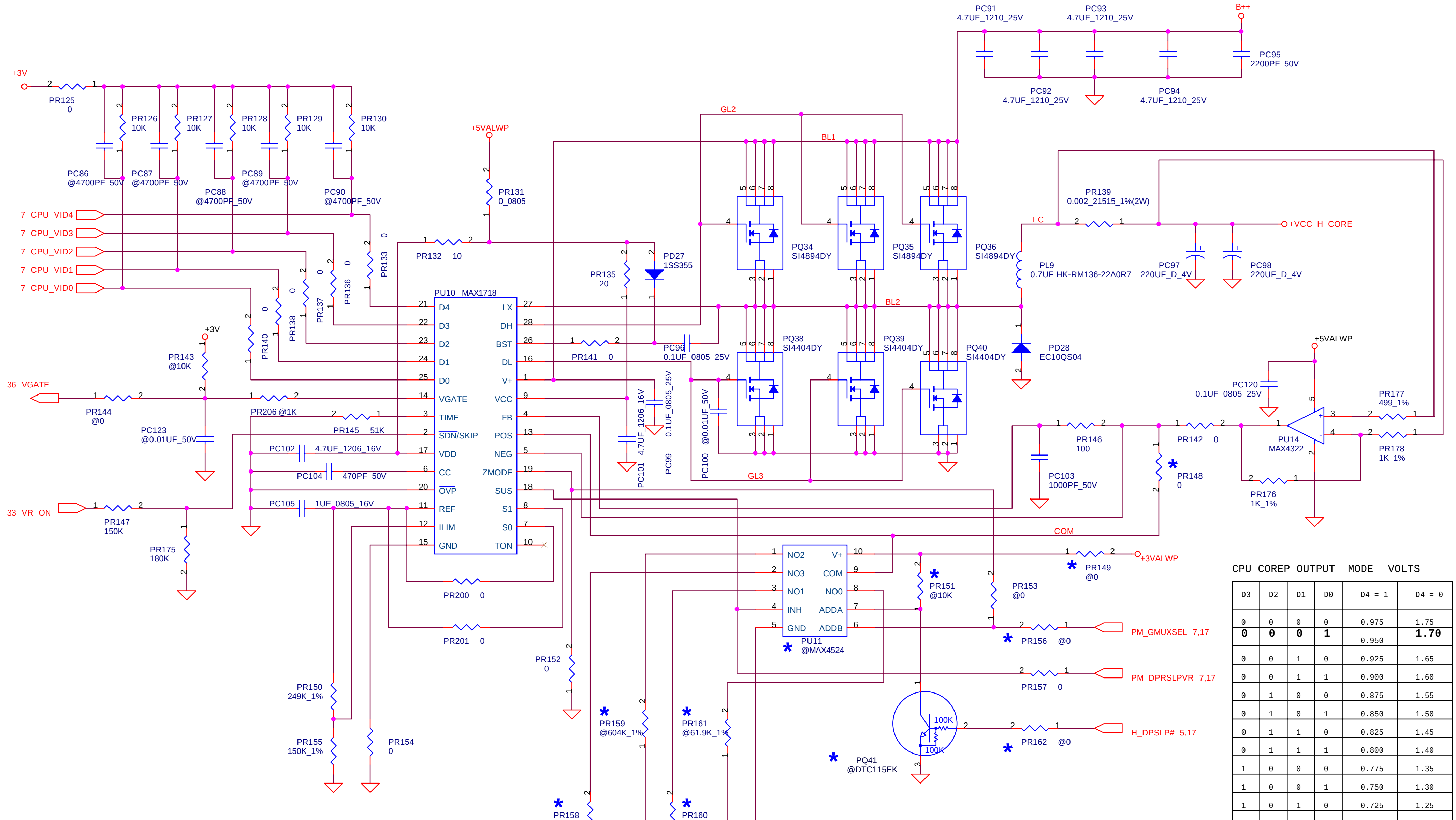

CPU CONTROL MODE

MODE	OFFSET	RBOTTOM	Vout(0A)	ADDA	ADDB
DEEPER SLEEP	0mV	X	0.850	X	X
BATTEY SLEEP	-56mV	16.2K	1.094	1	0
PERFORMANCE SLEEP	-51mV	19.6K	1.199	1	1
BATTERY MODE	-16mV	61.9K	1.134	0	0
PERFORMANCE MODE	**-1.8mV**	604K	1.248	0	1

CPU_COREP OUTPUT_ MODE VOLTS

D3	D2	D1	D0	D4 = 1	D4 = 0
0	0	0	0	0.975	1.75
0	**0**	**0**	**1**	0.950	**1.70**
0	0	1	0	0.925	1.65
0	0	1	1	0.900	1.60
0	1	0	0	0.875	1.55
0	1	0	1	0.850	1.50
0	1	1	0	0.825	1.45
0	1	1	1	0.800	1.40
1	0	0	0	0.775	1.35
1	0	0	1	0.750	1.30
1	0	1	0	0.725	1.25
1	0	1	1	0.700	1.20
1	1	0	0	0.675	1.15
1	1	0	1	0.650	1.10
1	1	1	0	0.625	1.05
1	1	1	1	0.600	1.00

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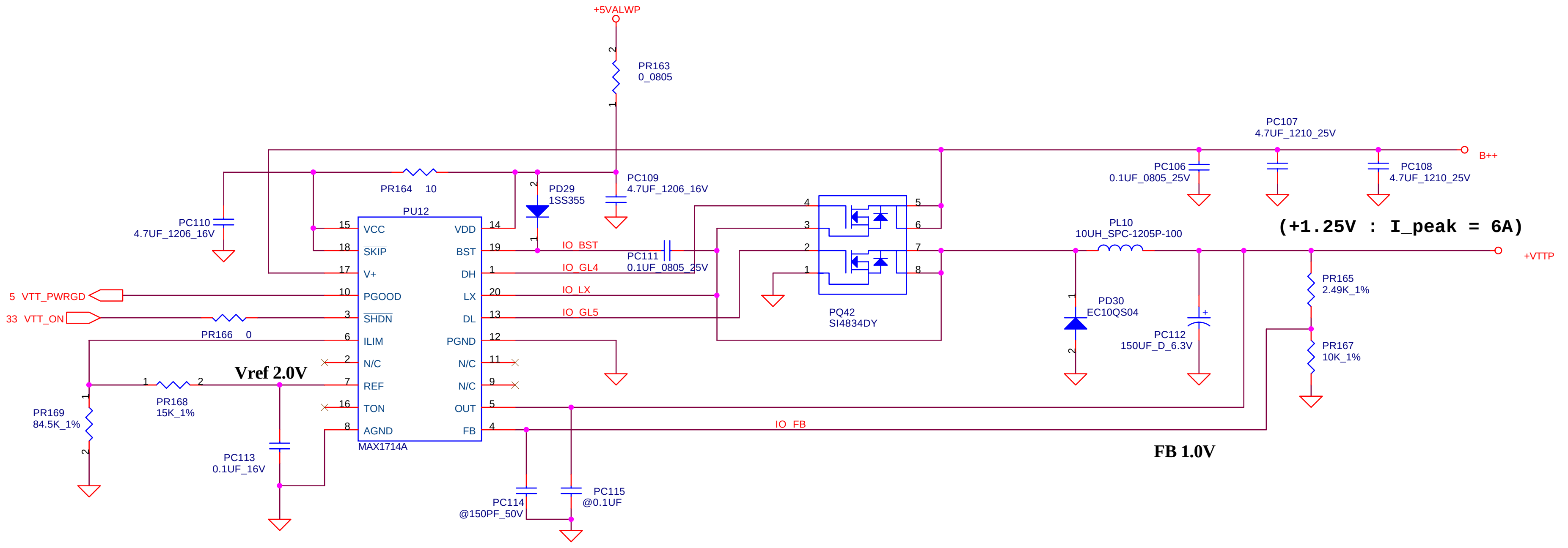

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