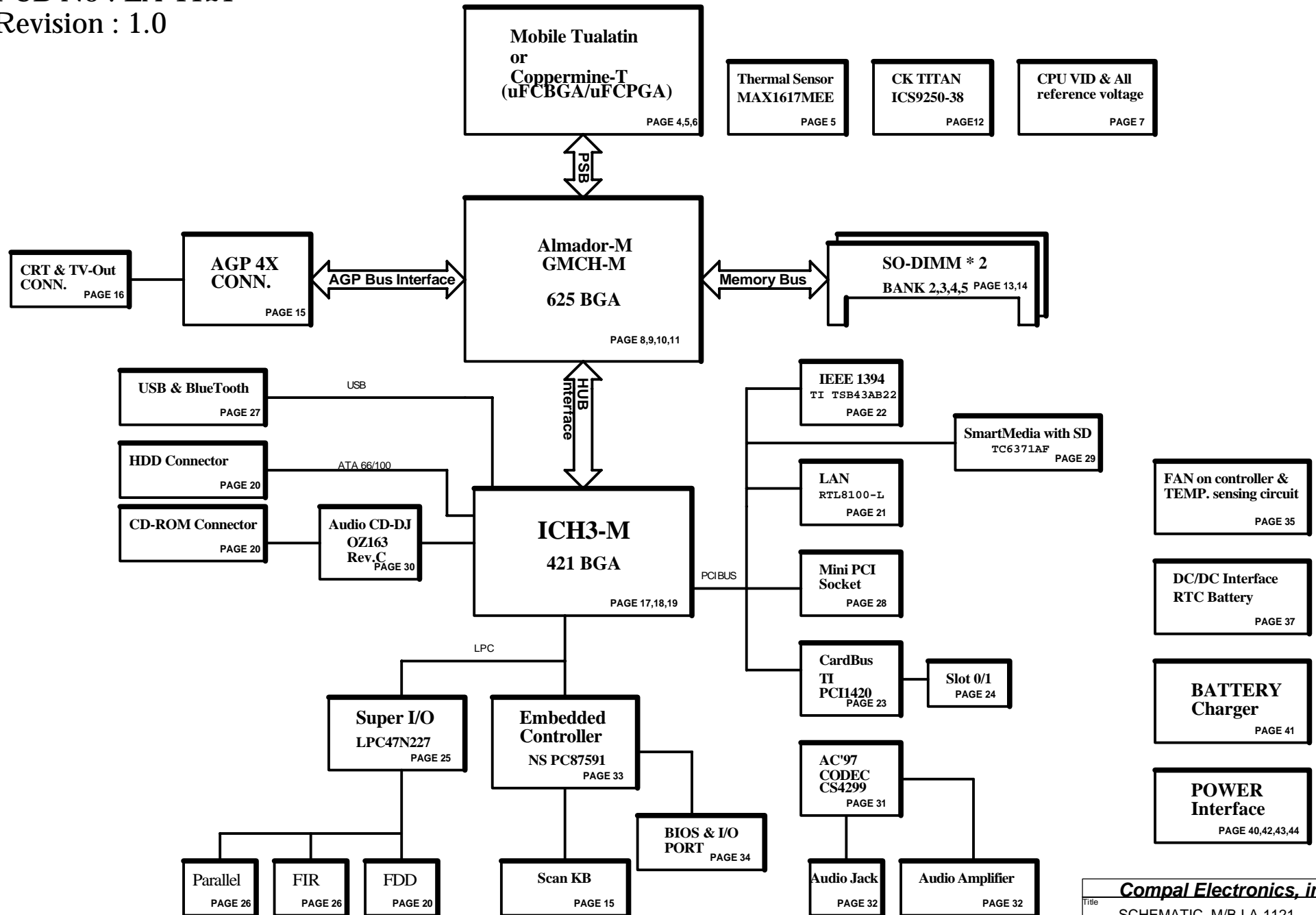


Model Name : 888M3  
 PCB No : LA-1121  
 Revision : 1.0

# BLOCK DIAGRAM

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Title	SCHEMATIC, M/B LA-1121	
Size	Document Number	Rev
Custom	401191 (FOR ATL02 / ACL00)	1C
Date:	星期一, 十一月 27, 2001	Sheet 2 of 87

## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_H_CORE	Core voltage for CPU	ON	OFF	OFF
+VTT	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+1.8V	1.8V power rail	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12VS	12V switched power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
AGP 4X CONN.			PIRQA
IEEE 1394	AD16	0	PIRQA
CardBus	AD20	2	PIRQA/PIRQB
LAN	AD17	3	PIRQB
Mini-PCI	AD18	1/4	PIRQC/PIRQD
SD/SM	AD22		PIRQC/PIRQD

## EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	MAX1617MEE	1001 110X b
EEPROM(24C16/02)	1010 000X b	OZ163	0011 0100 b
(24C04)	1011 000Xb	Smart Battery	0001 011X b
		Docking	0011 011X b
		DOT Board	XXXX XXXXb

## ICH3-M SM Bus address

Device	Address
Clock Generator ( ICS9238-50)	1101 0000
SDRAM Select ( 74HC4052 )	1010 0000
CPU Voltage VID select ( F3565 )	0110 111Xb

## PIR

### REV 0.2

Date	Page	Description
5/8	29	Modification toshiba SM+SD function
5/8	32	Modification audio volume control function
5/8	42	ADD system thermal protection
5/14	33	DEL R244 ,Add D44

### REV 0.3

Date	Page	Description
5/23	5	U8 Vcc plane modify to +5VALW
5/23	18	DEL R90,R89,R281
5/23	32	R448 change gnd to +5VCD, R479 change +5VCD to gnd.
5/23	37	U2.4 link to U20.8
5/23	30	Add R519.
5/23	5	U9.AF19 add R517 link to +1.5VS
5/23	25	Modify LPC_RST# timing. Add U55,D45,R518.
5/31	27	JP15.8 connector to U29.57
5/31	25	ADD R520, Add net name BT_DET# to U29.57
5/31	34	Modify net name ANT_SW to WL_OFF#, ADD R221
5/31	28	Modify net name RFOFF# to WL_OFF#
5/31	35	DEL R19

### REV 0.4

Date	Page	Description
7/3	16	Del L23,R14,R12,R10,R6,R8
7/3	27	ADD C720,C721,C722,C723,C724,C725
7/3	29	IDSEL0 change to PCI_AD26. INTA#/INTB# change to PIRQC#/PIRQD#
7/10	24	Add U58,U59,R531,R532,R533,R534,C718,C719
7/17	29	Del SD function
7/18	29	Change IDSEL to PCI_AD22
7/23	21	DEL C15

### REV 0.5

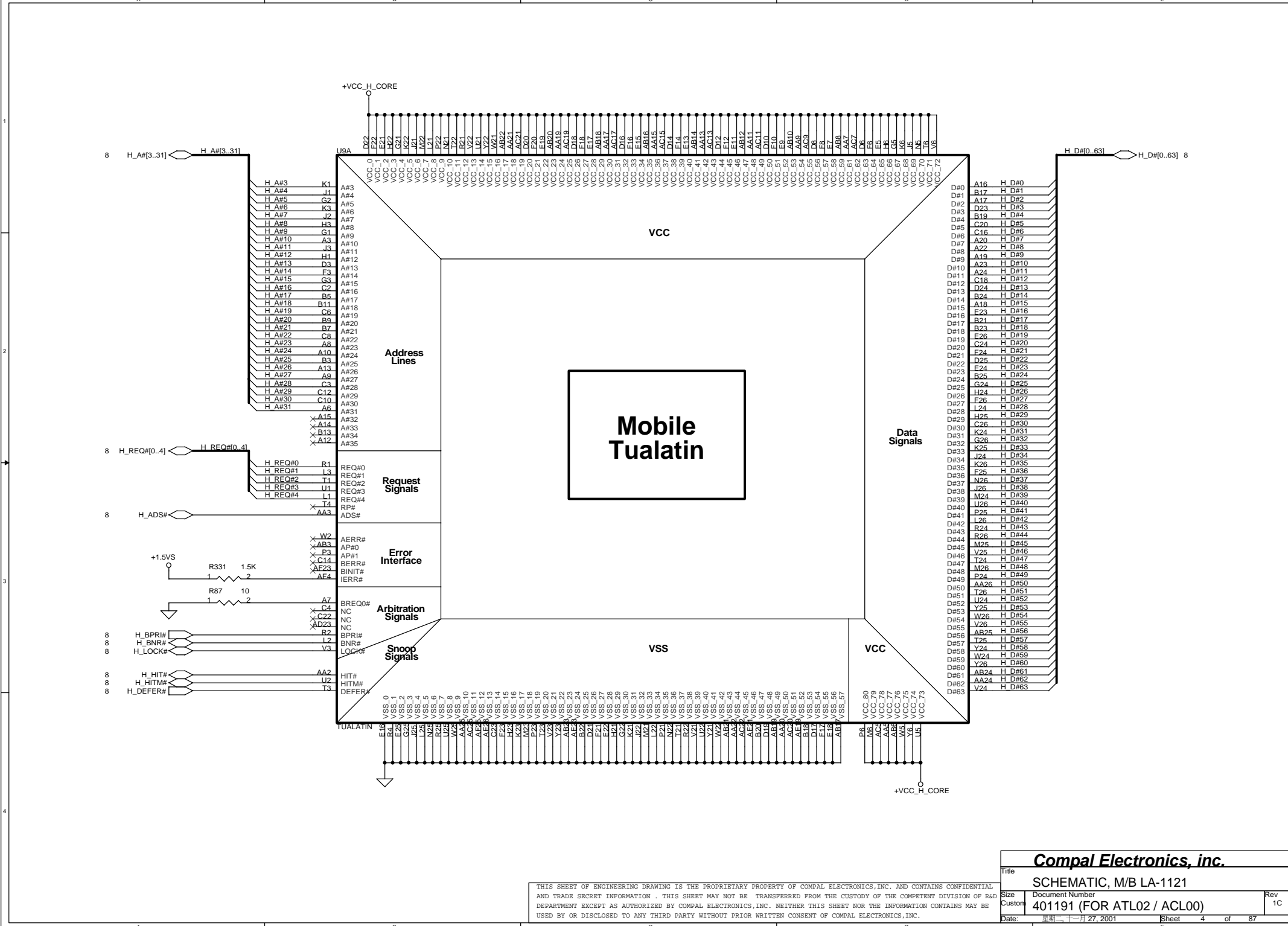
Date	Page	Description
8/13	15	Add R544 reserve for sus_stat# and stp_agp#
8/13	29	Add R545 pull-up signal SM_LED to SMC_VCC.Add@ in U62,C729,R486
8/13	35	Change R543 pull-up form SMC_VCC to +5VS
8/13	29	Add R546,R547 signal PCIRST#,CBRST#
8/13	37	Del U2,Q4,R330
8/16	10	Add Signal TV_out_DDC2CCLK,TV_out_DDC2DATA ,VCH_I2CCLK,VCH_I2CDATA,AGP_DDCCLK,AGP_DDCDATA
8/16	10	Add R551,R552. DEL R225,R235
8/16	15	Add RP38,RP39
8/16	16	Add R553,R554,R555
8/17	34	Del R29, Add R557, R558
8/17	20	Add R556

### REV 1.0

Date	Page	Description
8/31	5	Q6 RESERVE

### REV 1.A

Date	Page	Description
9/6	12	Add D47 and R562

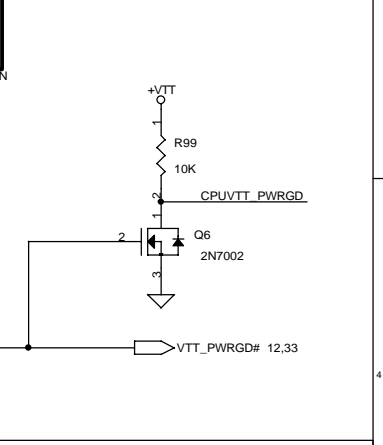
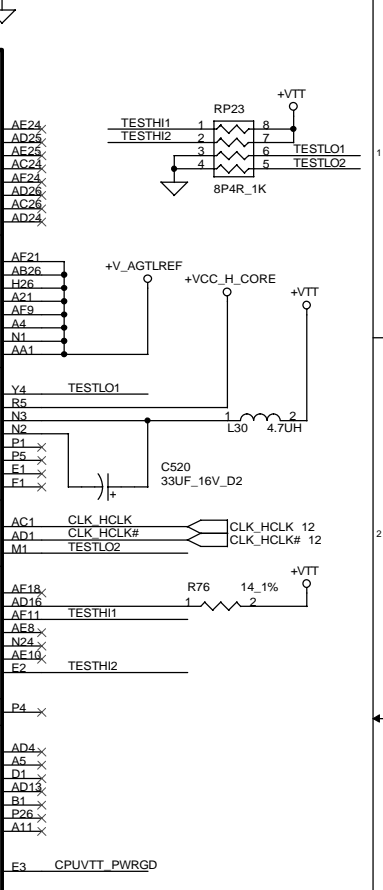
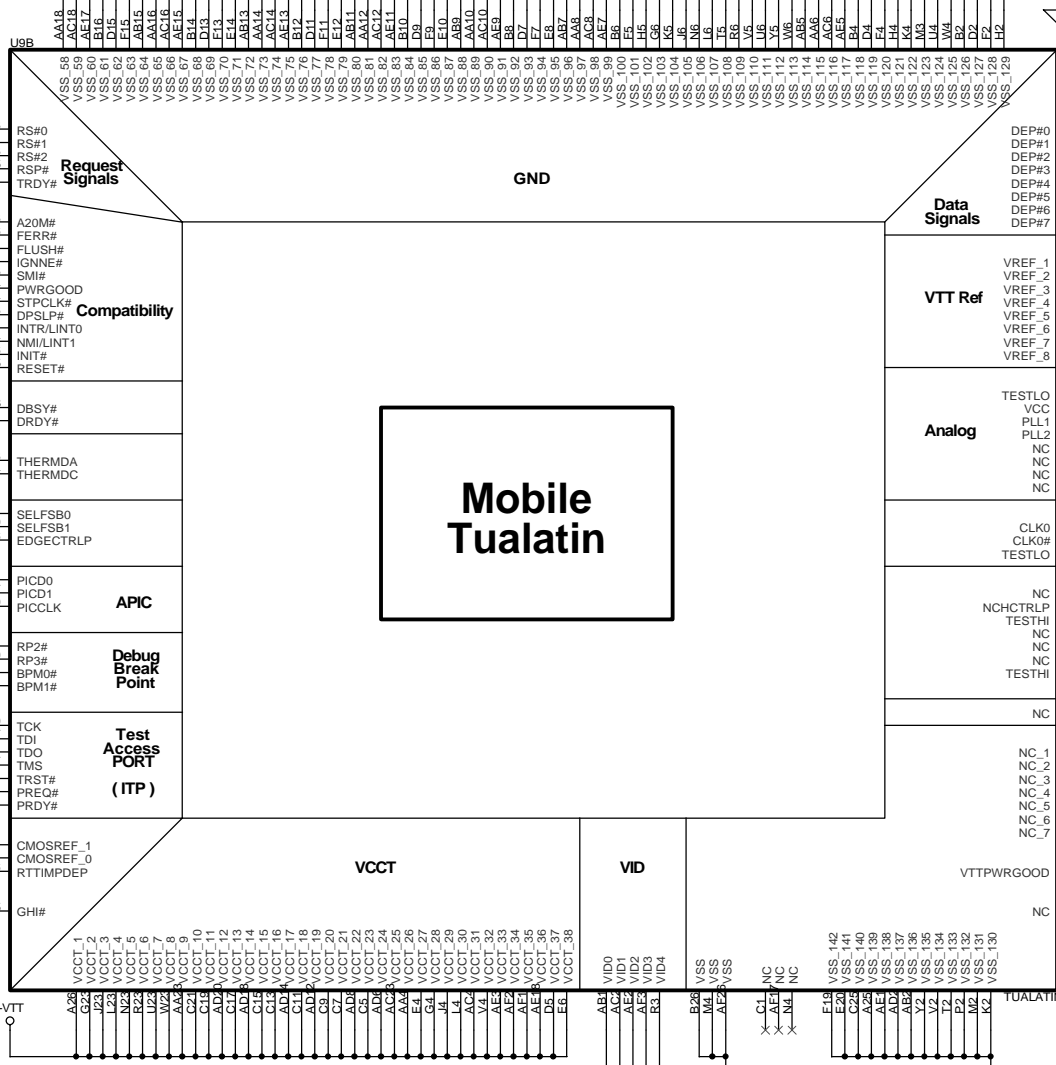
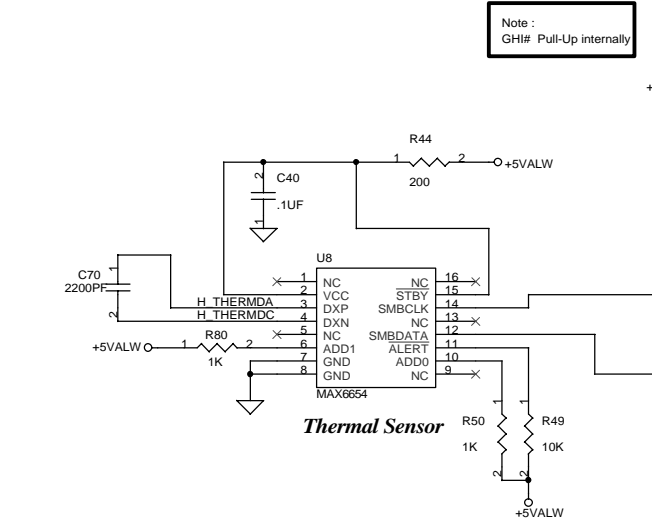
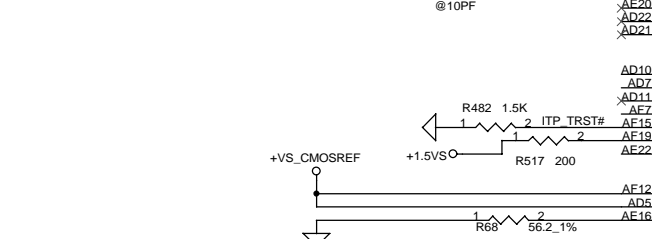
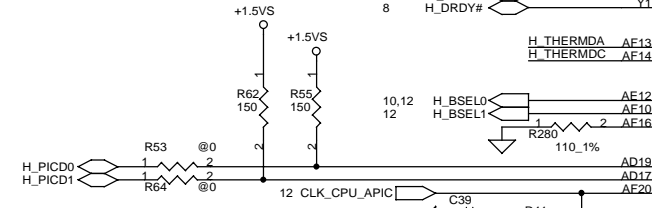
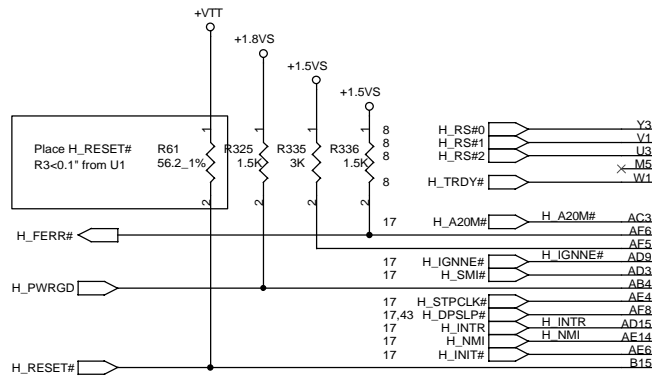


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Size	Document Number			
Custom	401191 (FOR ATL02 / ACL00)	Rev	1C	
Date:	星期一, 十一月 27, 2001	Sheet	4	of 87

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401191 (FOR ATL02 / ACL00)		1C
Size	Custom	Date
		星期一, 十一月 27, 2001
Date		Sheet 5 of 87

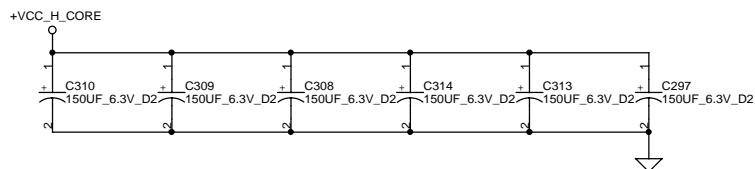
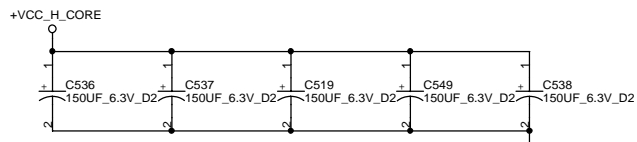
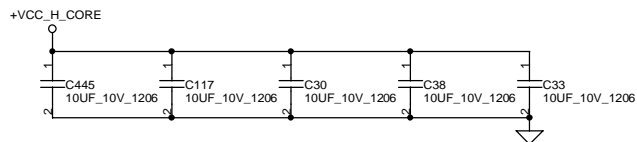
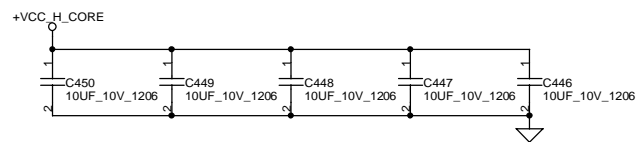
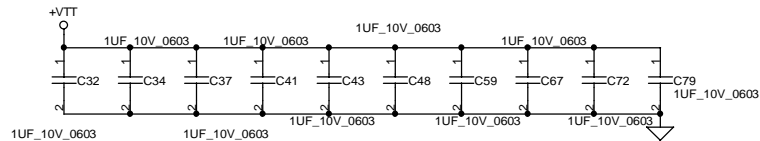
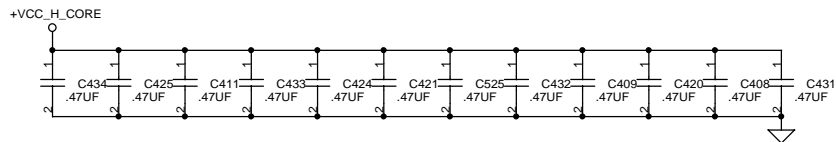
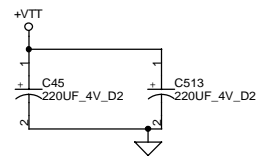
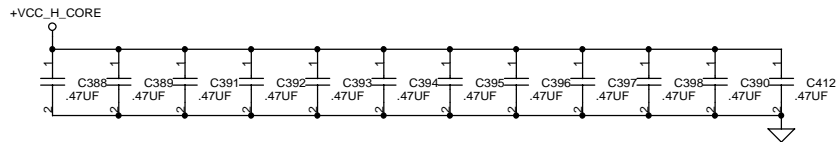
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**Layout note :**

Place close to CPU, Use 2-3 vias per PAD.  
 Place .47uF caps underneath balls on solder side.  
 Place 10uF caps on the peripheral near balls.  
 Use 2-3 vias per PAD.

**Layout note :**

Place close to CPU,  
 Use 2 vias per PAD.

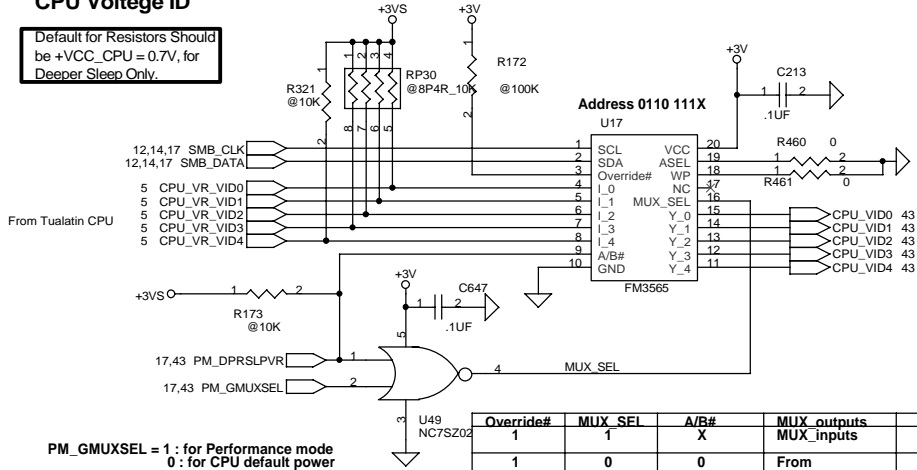


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Title	SCHMATIC, M/B LA-1121
Size	Document Number
Custom	401191 (FOR ATL02 / ACL00)
Date:	星期一, 十一月 27, 2001
Sheet	6 of 87
Rev	1C

### CPU Voltage ID

Default for Resistors Should be +VCC\_CPU = 0.7V, for Deeper Sleep Only.



Override#	MUX_SEL	A/B#	MUX_outputs MUX_inputs	Mode
1	1	X	From Non-volatile register(SOPRB)	Performance
1	0	0	From Non-volatile register(SOPRA)	Deeper sleep

PM\_GMUXSEL = 1 : for Performance mode  
0 : for CPU default power

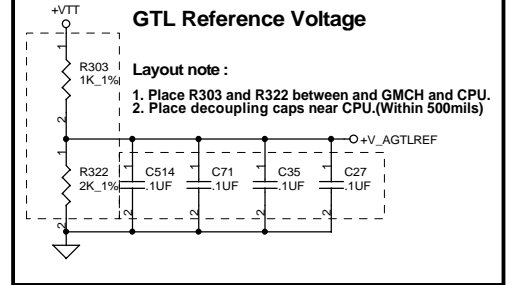
PM\_DPRSLPVR = 1: for Deeper Sleep mode  
0: for Performance mode

### Tualatin

D4	D3	D2	D1	D0	CPU_Core(V)	ES(before MP)
0	0	1	0	1	1.50V (Performance)	
0	1	1	0	0	1.15V (Battery)	
1	0	1	0	1	0.85V (Deeper Sleep)	

D4	D3	D2	D1	D0	CPU_Core(V)	QS( MP)
0	0	1	1	1	1.40V (Performance)	
0	1	1	0	0	1.15V (Battery)	
1	0	1	0	1	0.85V (Deeper Sleep)	

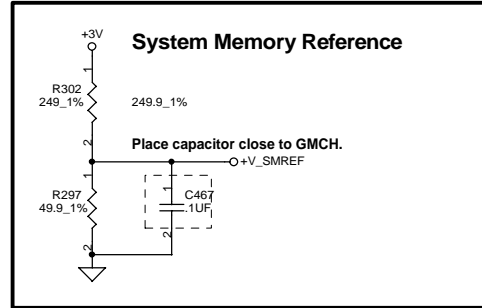
### GTL Reference Voltage



#### Layout note :

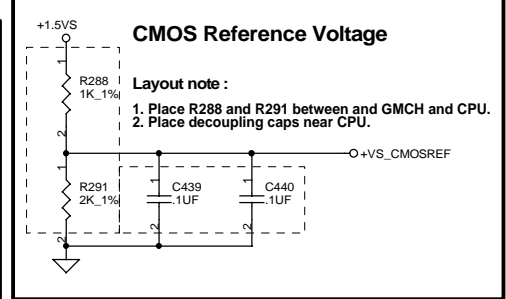
1. Place R303 and R322 between and GMCH and CPU.
2. Place decoupling caps near CPU.(Within 500mils)

### System Memory Reference



#### Place capacitor close to GMCH.

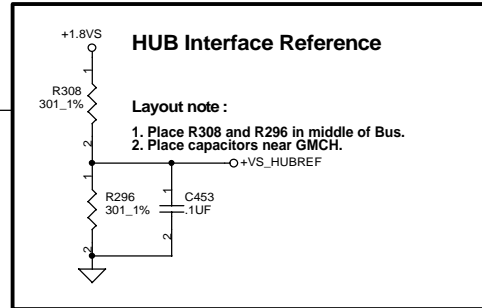
### CMOS Reference Voltage



#### Layout note :

1. Place R288 and R291 between and GMCH and CPU.
2. Place decoupling caps near CPU.

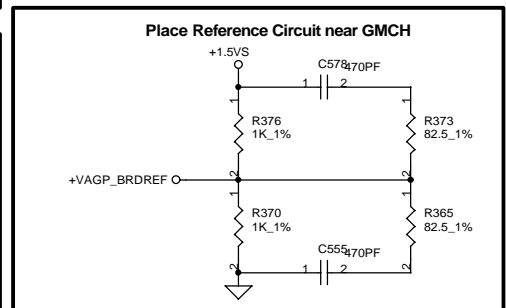
### HUB Interface Reference



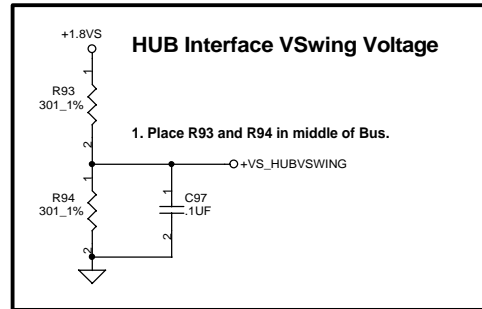
#### Layout note :

1. Place R308 and R296 in middle of Bus.
2. Place capacitors near GMCH.

### Place Reference Circuit near GMCH

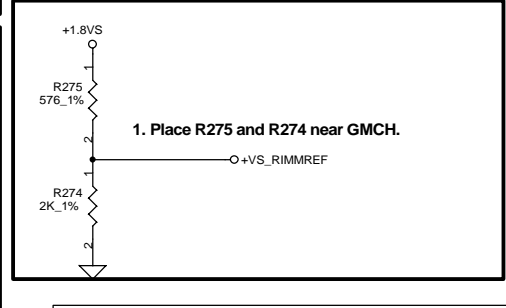


### HUB Interface VSwing Voltage



1. Place R93 and R94 in middle of Bus.

### Place Reference Circuit near GMCH

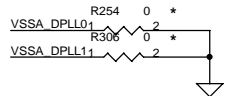
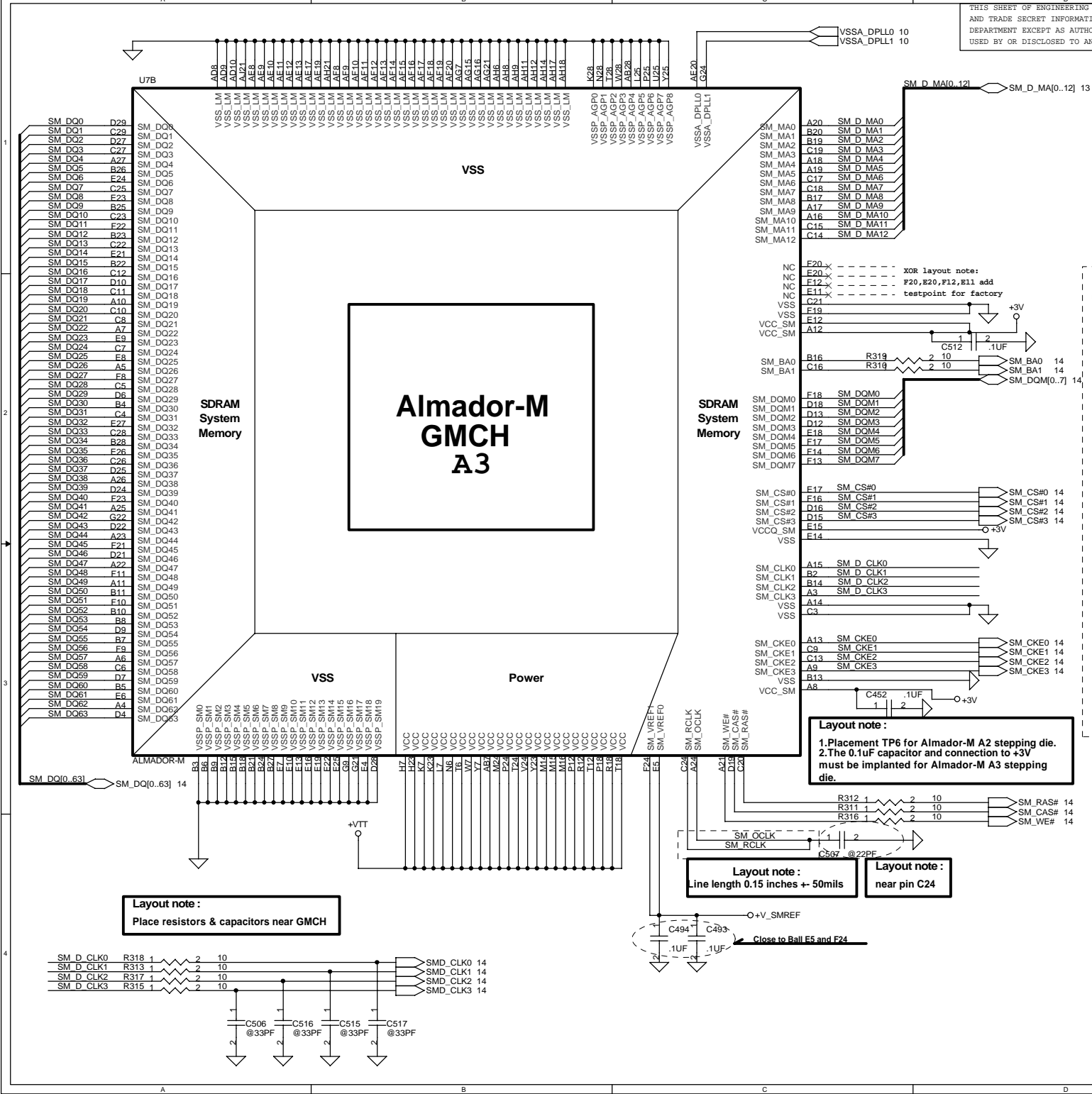


1. Place R275 and R274 near GMCH.

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Title	SCHEMATIC, M/B LA-1121	
Size	Document Number	Rev
Custom	401191 (FOR ATL02 / ACL00)	1C
Date:	星期一, 十一月 27, 2001	Sheet 7 of 87





XOR layout note:  
 F20, F12, E11, E11 add  
 testpoint for factory

**For Almador-M A3 stepping requirement.**  
 The table below provides a summary of the ballout changes to the Almador-M chip

**Table 4-1 Ballout Changes**

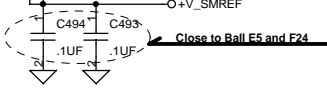
Ball#	New Signal Name	Old Signal Name
A8	VCC_SM	SM_CKE5
A12	VCC_SM	SM_ECC7
E12	VCC_SM	SM_ECC8
G10	VCC_SM	VCCQ_SM
F7	VCCQ_SM	VCC_SM
G19	VCCQ_SM	VCC_SM
E15	VCCQ_SM	SM_CS4
F15	VCCQ_SM	VCC_SM
A14	VSS	SM_CLK4
B13	VSS	SM_CKE4
C3	VSS	SM_CLK5
C21	VSS	SM_ECC4
E14	VSS	SM_CS5
F19	VSS	SM_ECC5
E11	NC	SM_ECC3
E20	NC	SM_ECC1
F12	NC	SM_ECC2
F20	NC	SM_ECC0

**Layout note:**  
 1. Placement TP6 for Almador-M A2 stepping die.  
 2. The 0.1uF capacitor and connection to +3V must be implanted for Almador-M A3 stepping die.

**Layout note:**  
 Line length 0.15 inches +/- 50mils

**Layout note:**  
 near pin C24

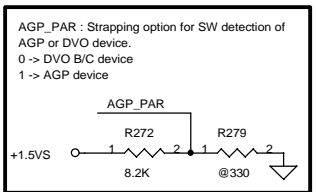
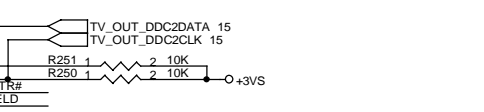
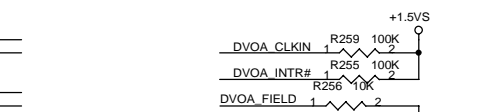
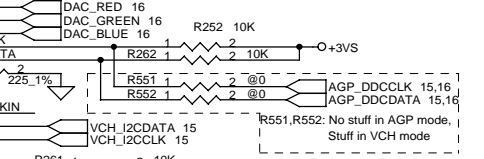
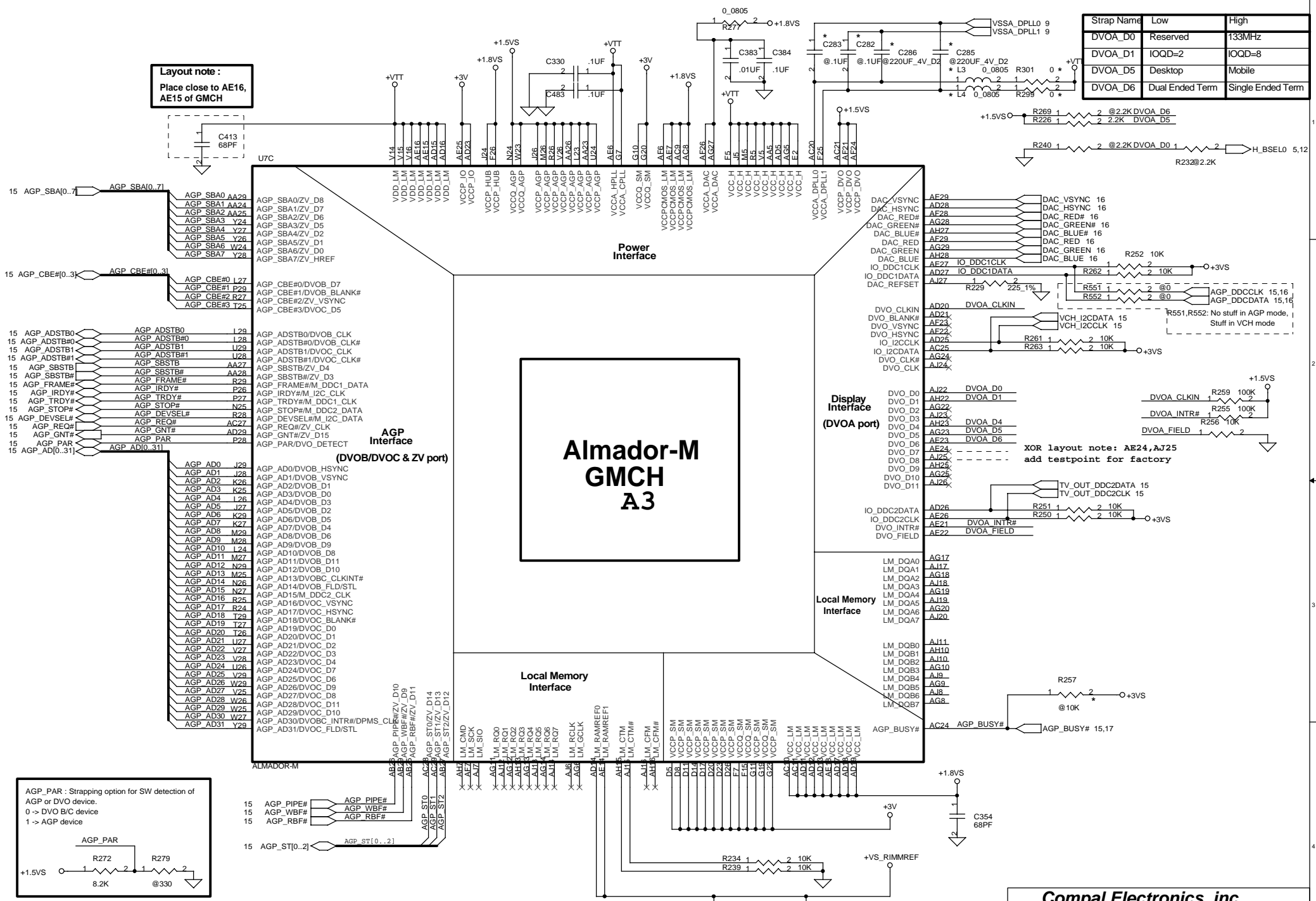
**Layout note:**  
 Place resistors & capacitors near GMCH





**Layout note :**  
Place close to AE16,  
AE15 of GMCH

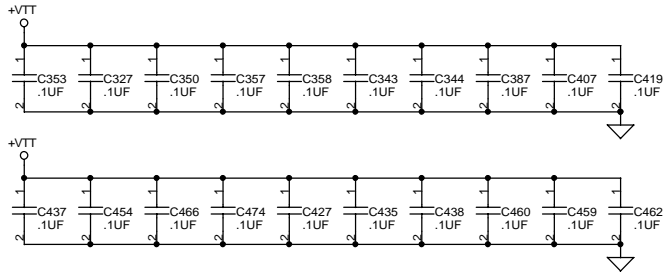
Strap Name	Low	High
DVOA_D0	Reserved	133MHz
DVOA_D1	IOQD=2	IOQD=8
DVOA_D5	Desktop	Mobile
DVOA_D6	Dual Ended Term	Single Ended Term



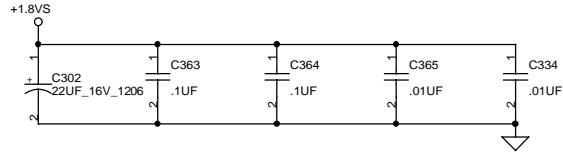
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Title	SCHEMATIC, M/B LA-1121	
Size	Document Number	Rev
Custom	401191 (FOR ATL02 / ACL00)	1C
Date:	星期一, 十一月 27, 2001	Sheet 10 of 87

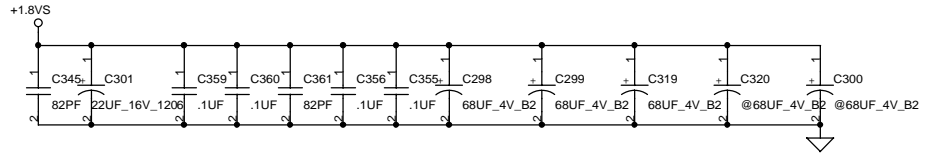
**Layout note :**  
Distribute as close as possible to GMCH Processor Quadrant .



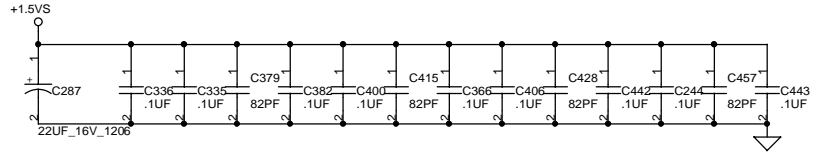
**Layout note :**  
Distribute as close as possible to VCCPCMOS\_LM .



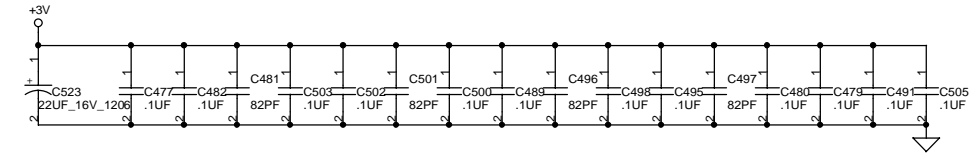
**Layout note :**  
Distribute as close as possible to GMCH Local Memory Quadrant .



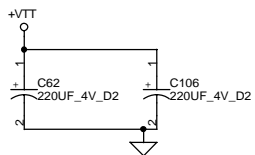
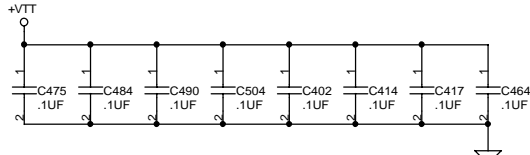
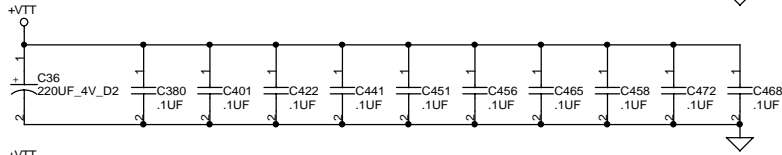
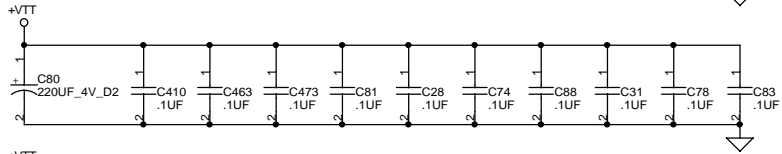
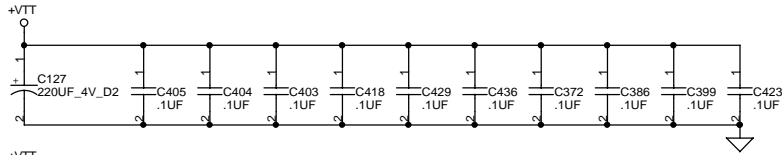
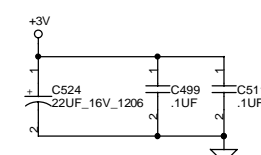
**Layout note :**  
Distribute as close as possible to GMCH AGP/DVO Quadrant .



**Layout note :**  
Distribute as close as possible to GMCH System Memory Quadrant .

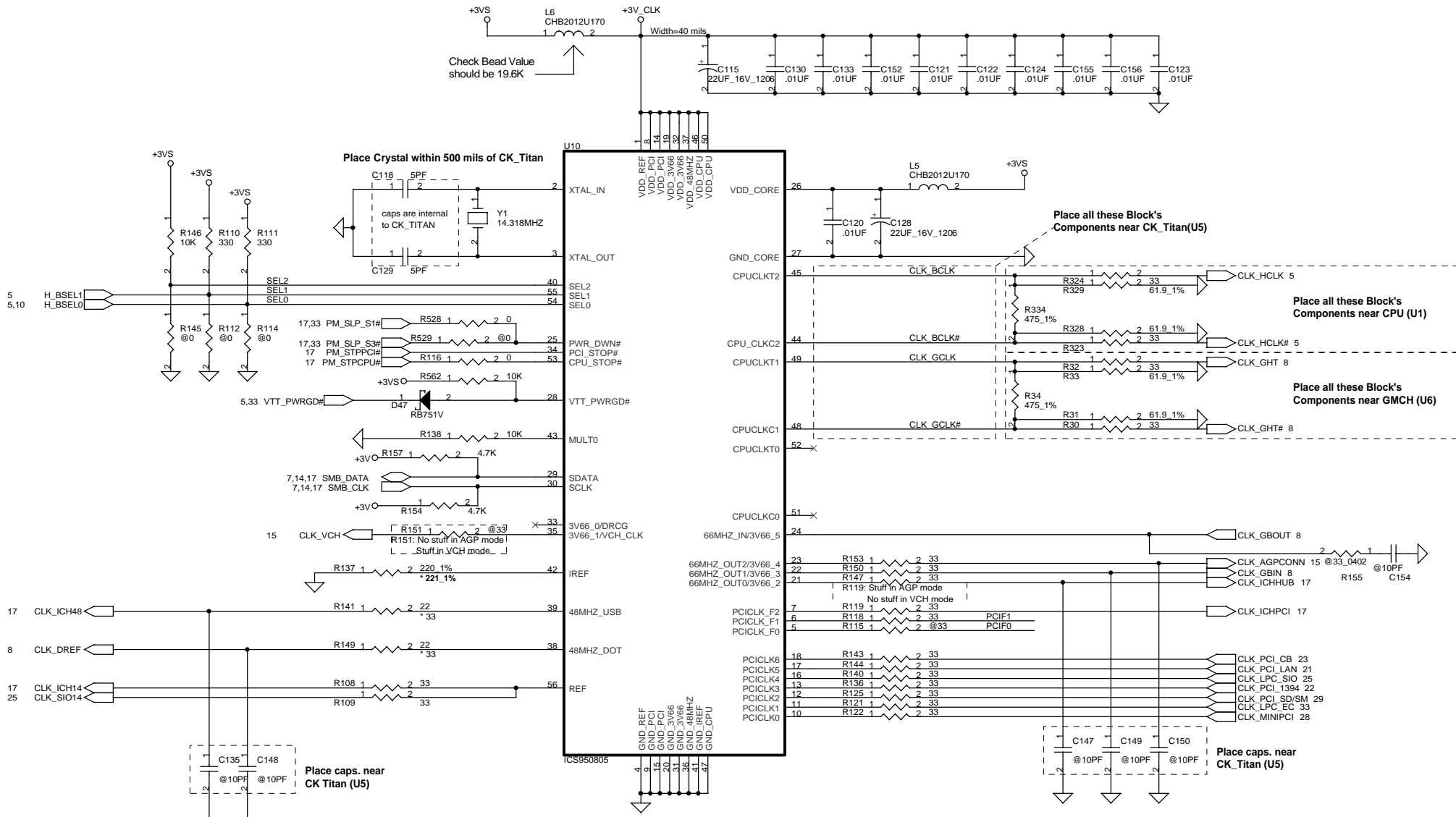


**Layout note :**  
Distribute as close as possible to IO Quadrant .



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Title	SCHEMATIC, M/B LA-1121	
Size	Document Number	Rev
Custom	401191 (FOR ATL02 / ACL00)	1C
Date:	星期一, 十一月 27, 2001	Sheet 11 of 87



SEL2	SEL1	SEL0	CPUCLKC0..2	CPUCLKT0..2
1	0	0	66.67	66.67
1	0	1	100.00	100.00
1	1	0	200.00	200.00
1	1	1	133.33	133.33

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**Title** SCHEMATIC, M/B LA-1121

**Size** Custom

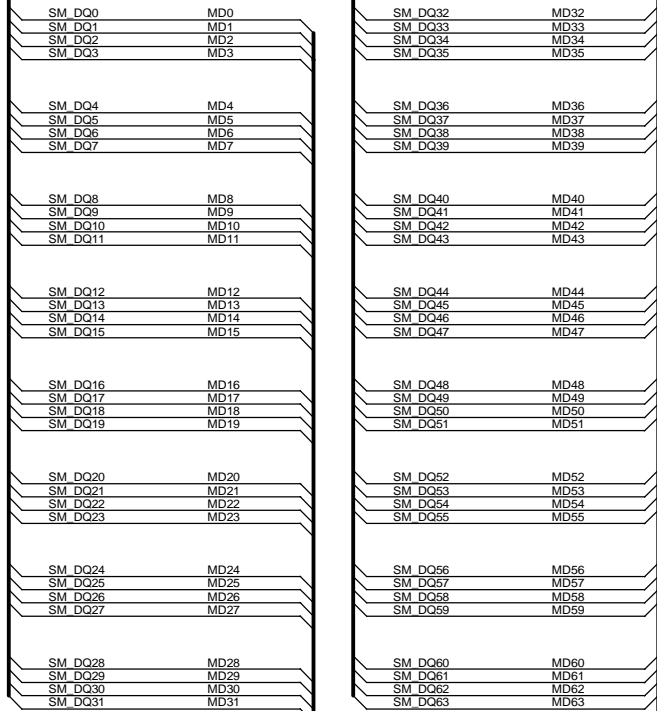
**Document Number** 401191 (FOR ATL02 / ACL00)

**Date** 星期一, 十一月 27, 2001

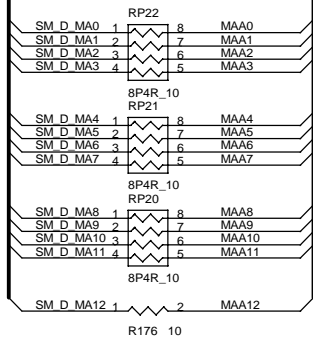
**Sheet** 12 of 87

**Rev** 1C

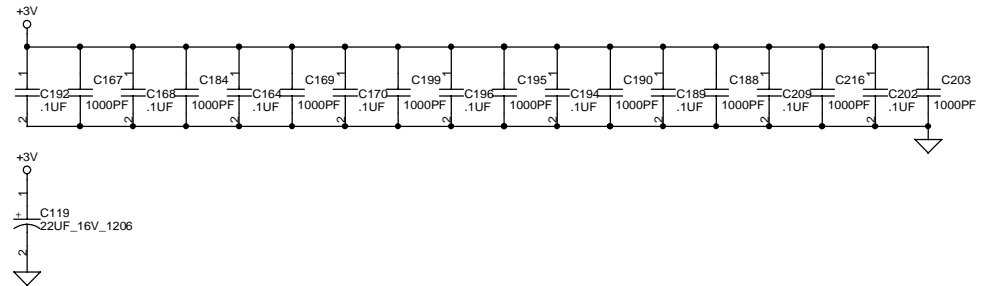
9,14 SM\_DQ[0..63] MD[0..63] 9,14



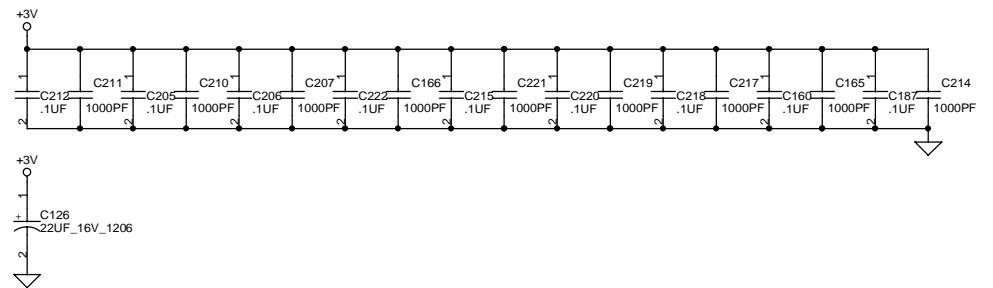
9 SM\_D\_MA[0..12] MAA[0..12] 14



**Layout note :**  
One .1uF cap per power pin .  
Place each cap close to SODIMM(DIMM 0) pin .



**Layout note :**  
One .1uF cap per power pin .  
Place each cap close to SODIMM(DIMM 1) pin .



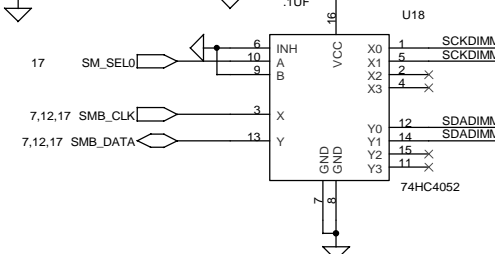
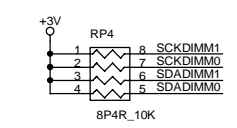
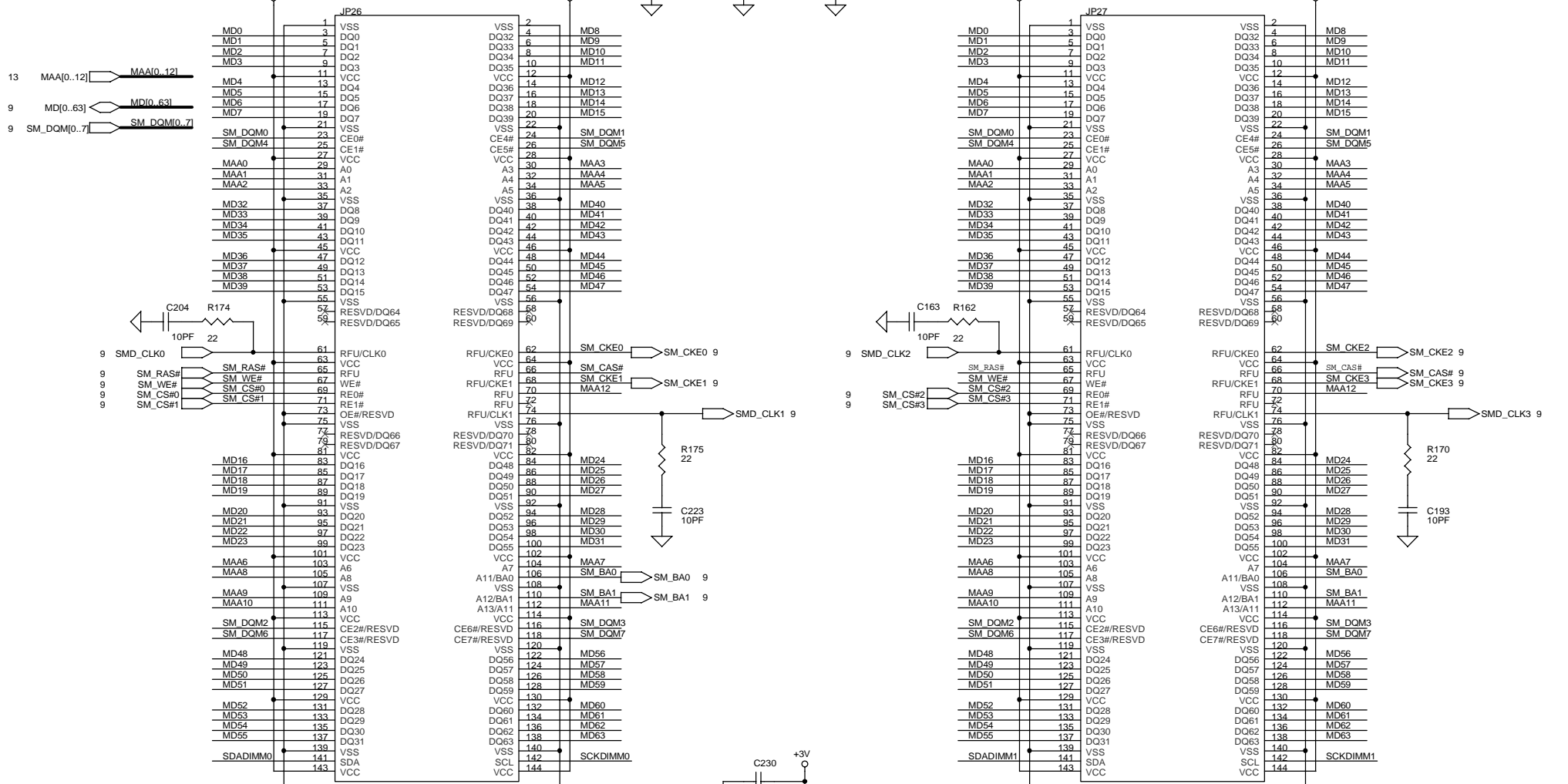
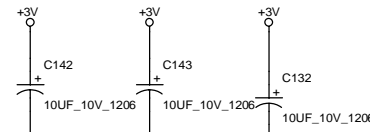
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Title	SCHEMATIC, M/B LA-1121	
Size	Document Number	Rev
Custom	401191 (FOR ATL02 / ACL00)	1C
Date:	星期一, 十一月 27, 2001	Sheet 13 of 87

SO-DIMM 144 PINS  
RAM MODULE CONN.

**BANK 0/1**

**BANK 2/3**



SM_SELO	X/Y
0	SCKDIMM0
1	SCKDIMM1

**Compal Electronics, inc.**

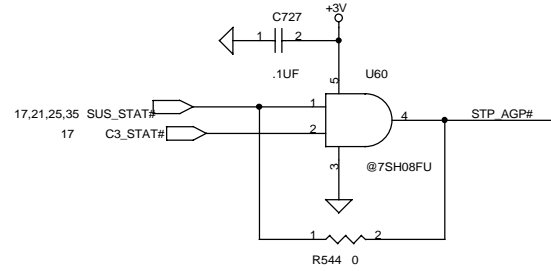
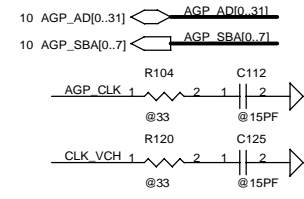
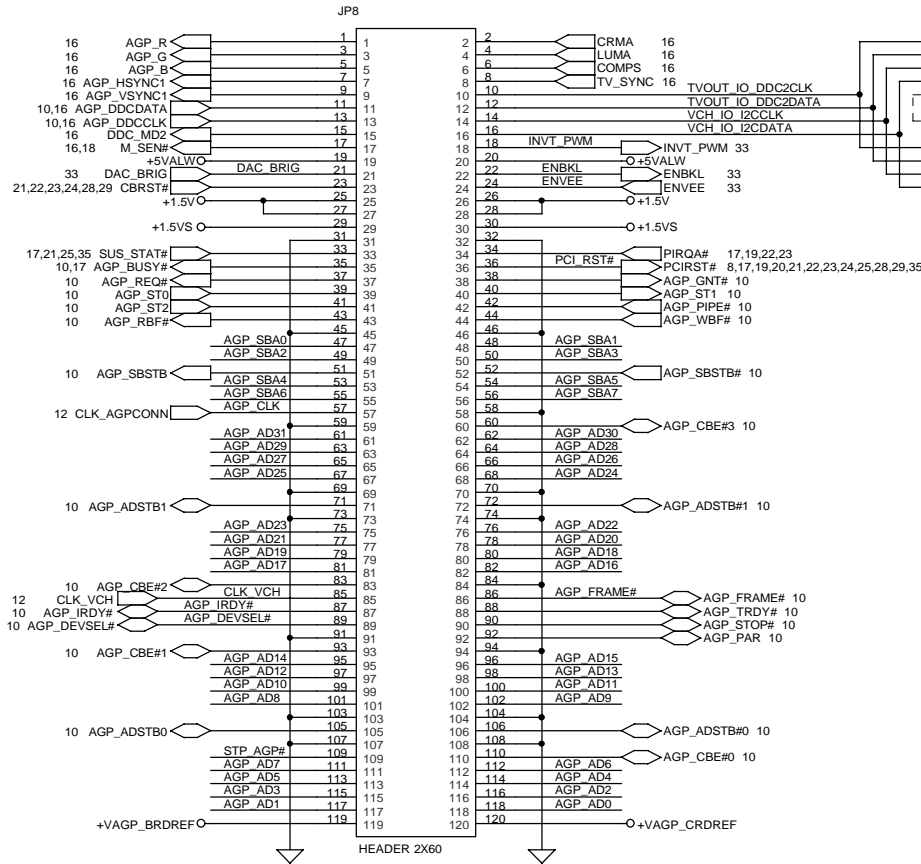
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Document Number  
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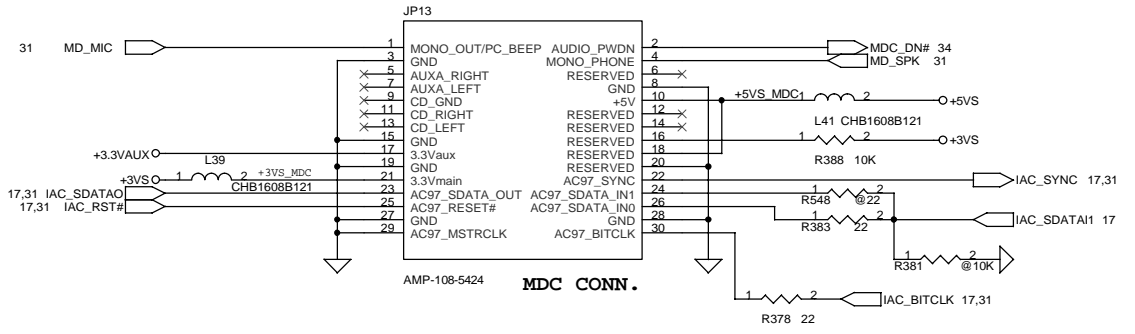
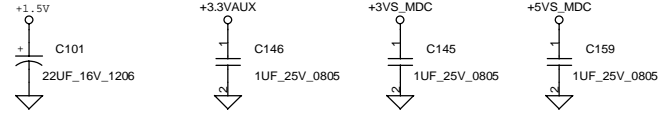
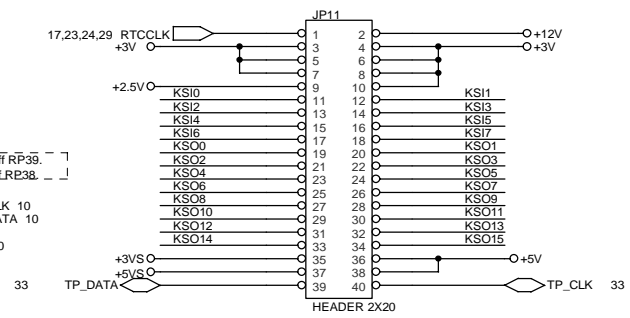
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**AGP CONN.**



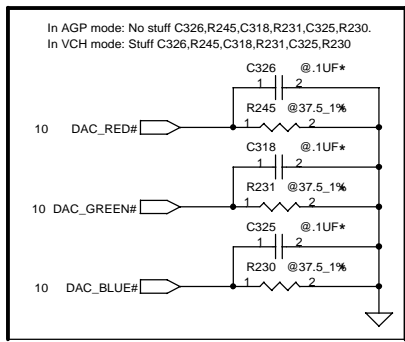
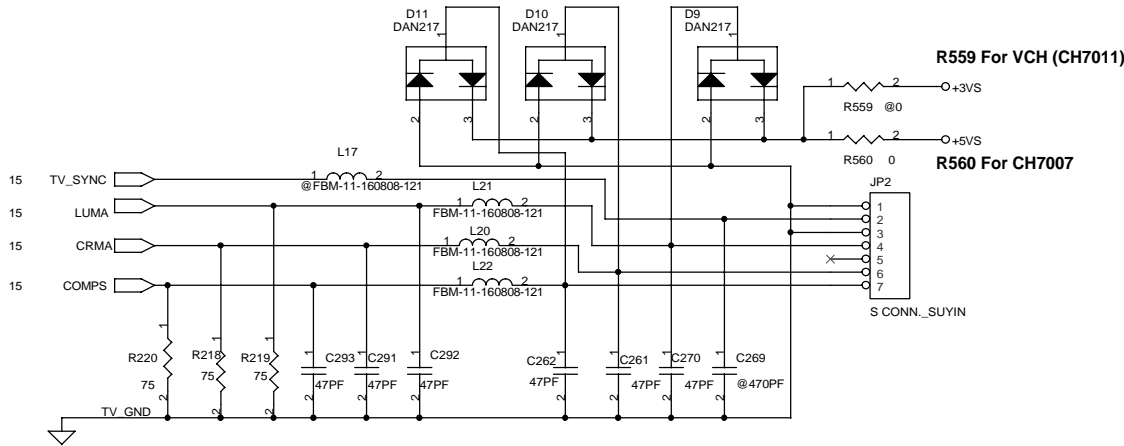
**Int. Keyboard CONN.**



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Title		
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Size	Document Number	Rev
B	401191 (FOR ATL02 / ACL00)	1C
Date:	星期 二, 十一月 27, 2001	Sheet 15 of 87

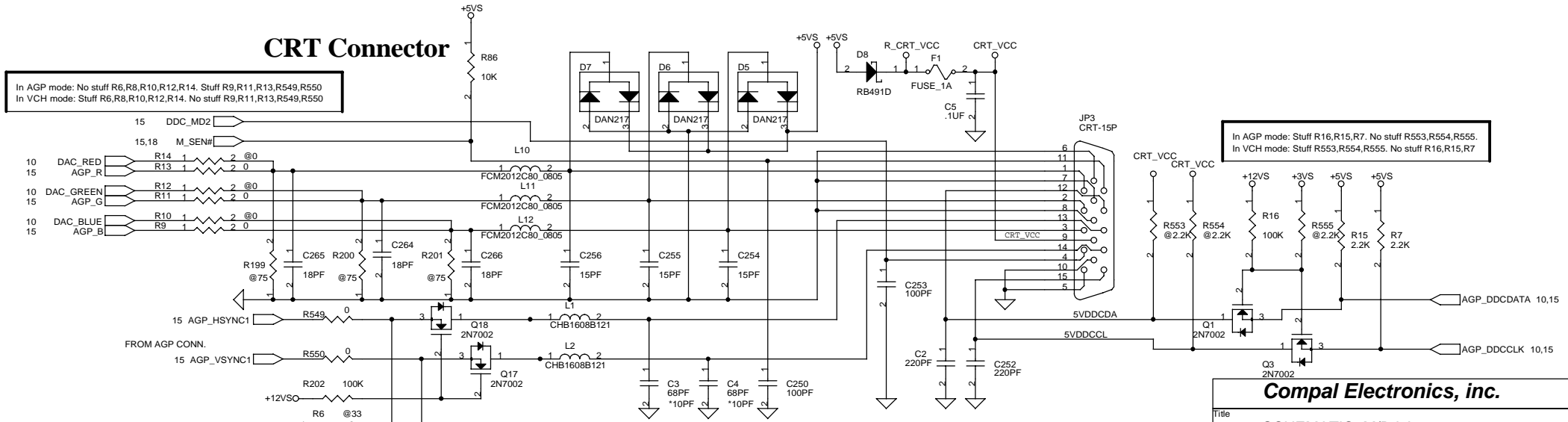
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# TV\_OUT CONN.



# CRT Connector

In AGP mode: No stuff R6,R8,R10,R12,R14. Stuff R9,R11,R13,R549,R550  
In VCH mode: Stuff R6,R8,R10,R12,R14. No stuff R9,R11,R13,R549,R550

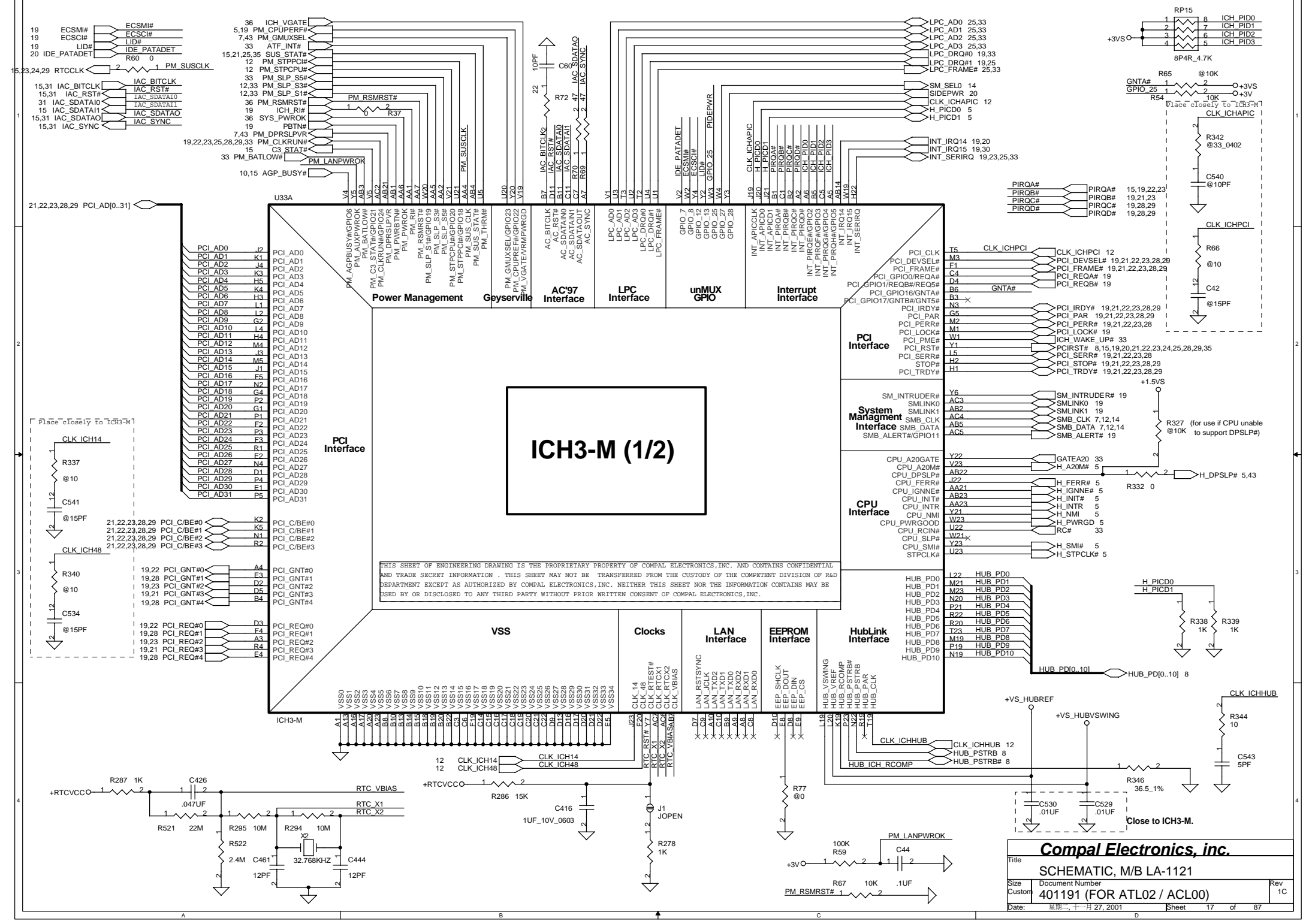


In AGP mode: Stuff R16,R15,R7. No stuff R553,R554,R555.  
In VCH mode: Stuff R553,R554,R555. No stuff R16,R15,R7

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Title	SCHEMATIC, M/B LA-1121	
Size	Document Number	Rev
Custom	401191 (FOR ATLO2 / ACL00)	1C
Date:	星期一, 十一月 27, 2001	Sheet 16 of 87

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**ICH3-M (1/2)**

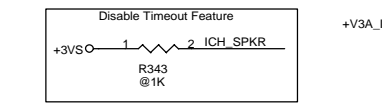
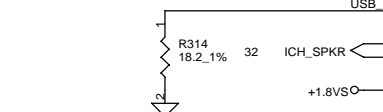
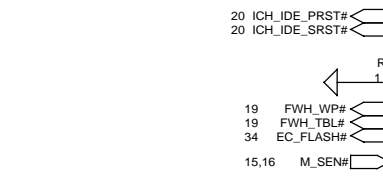
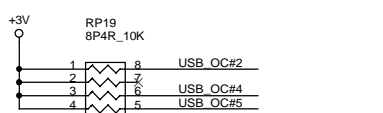
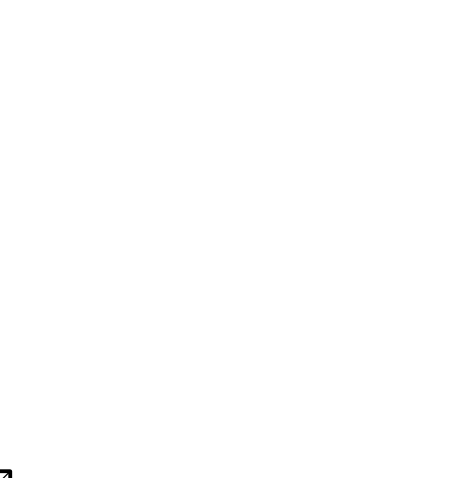
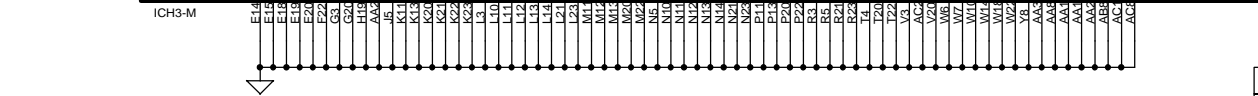
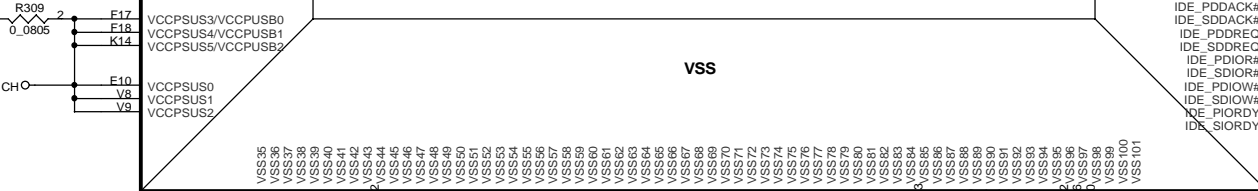
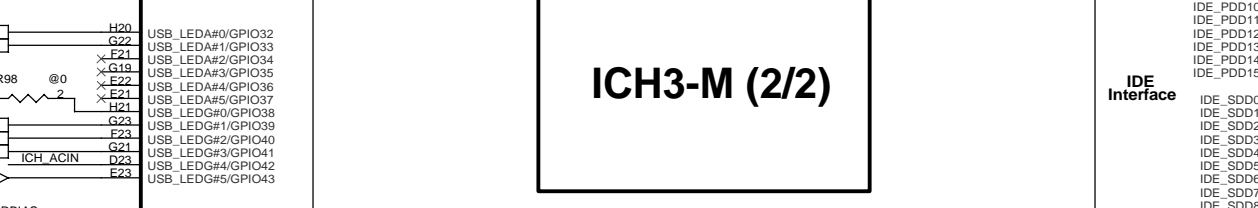
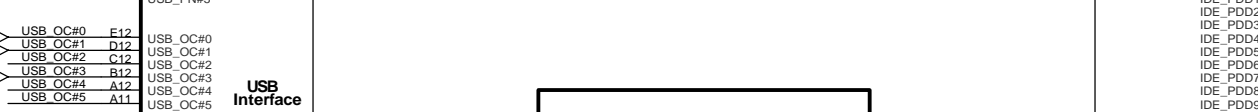
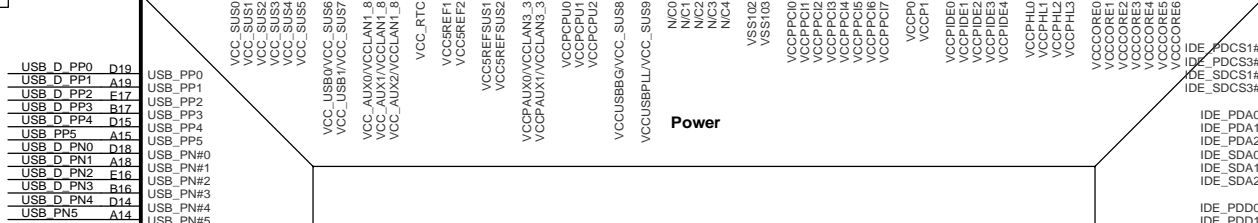
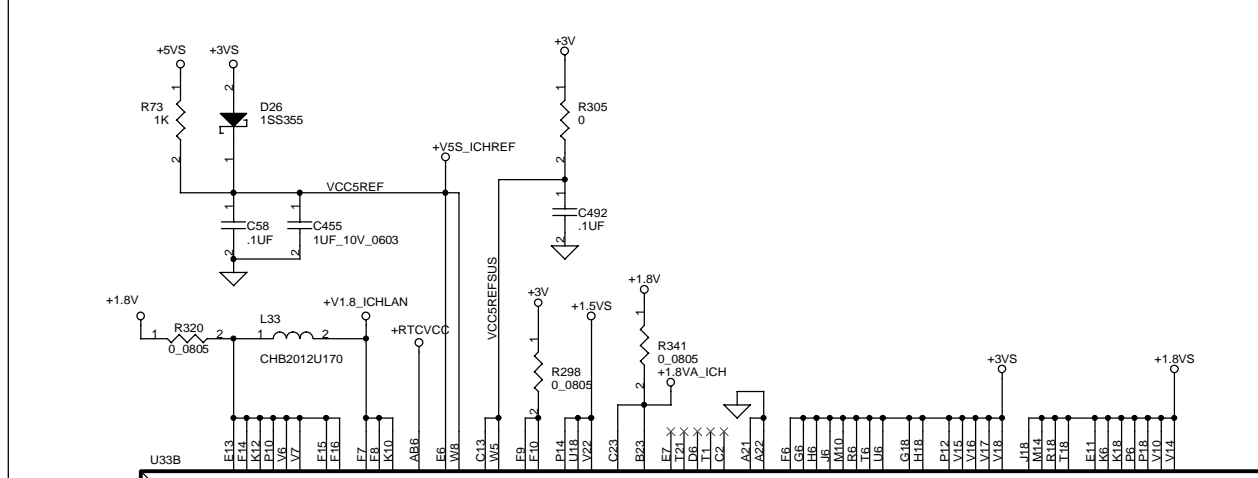
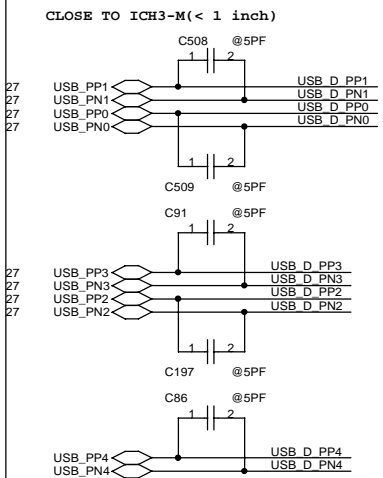
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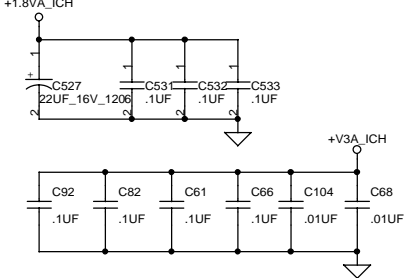
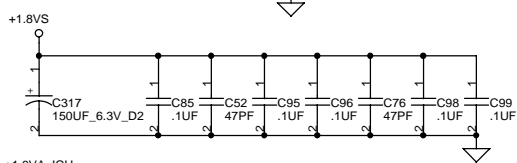
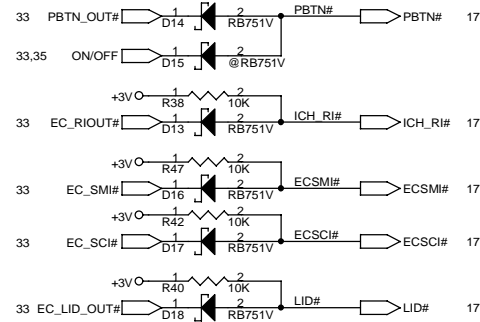
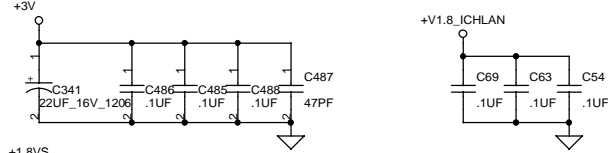
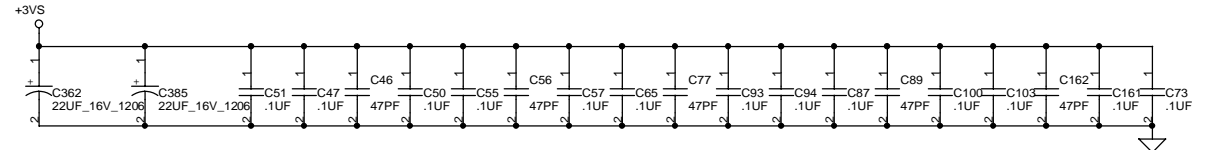
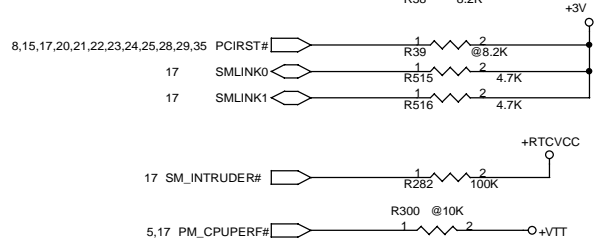
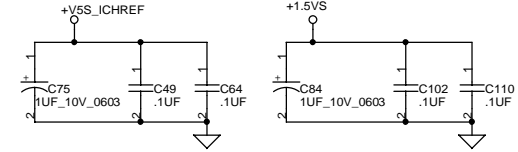
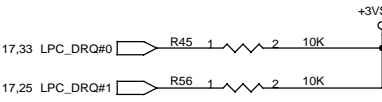
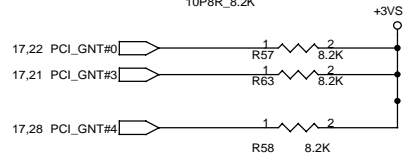
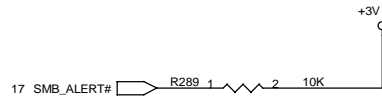
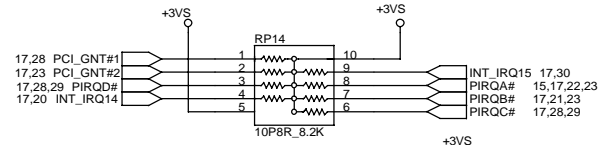
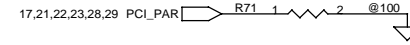
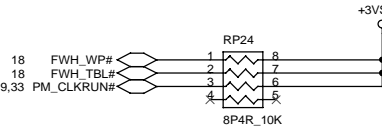
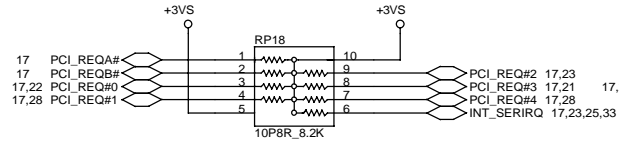
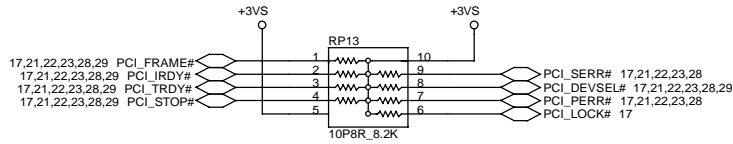
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 Custom: 401191 (FOR ATL02 / ACL00)  
 Date: 星期一, 十一月 27, 2001 Sheet 17 of 87



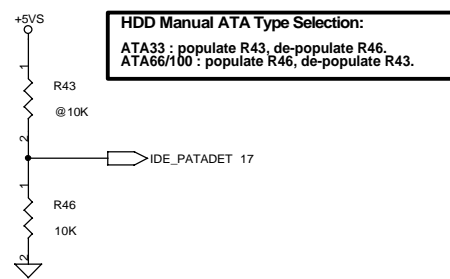
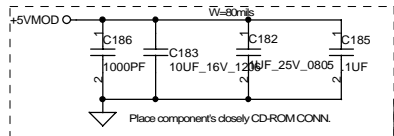
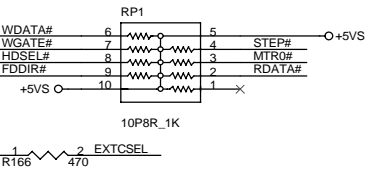
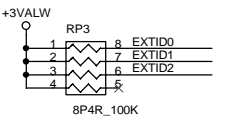
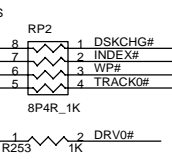
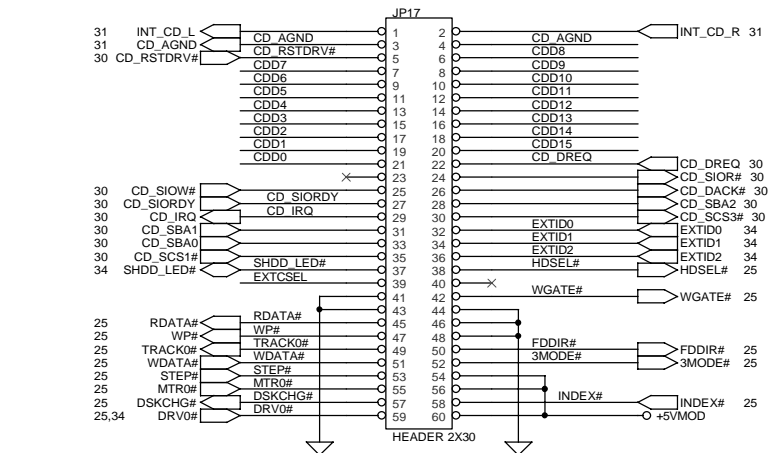
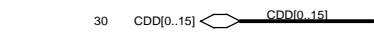
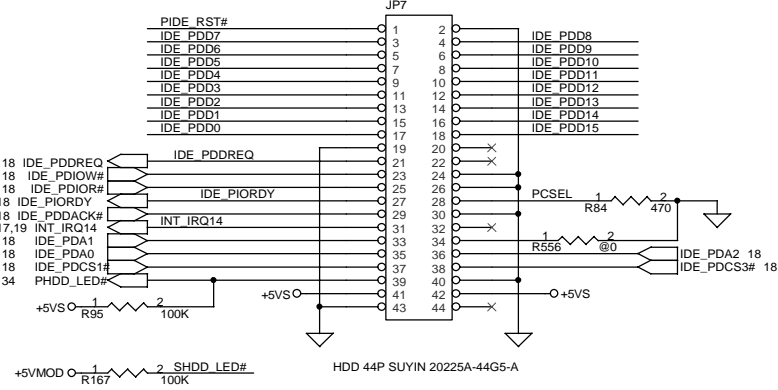
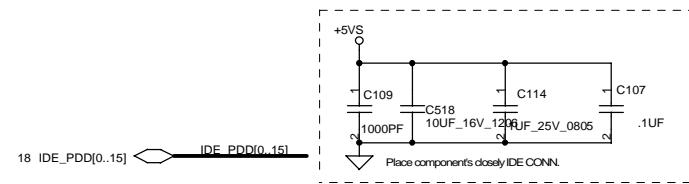




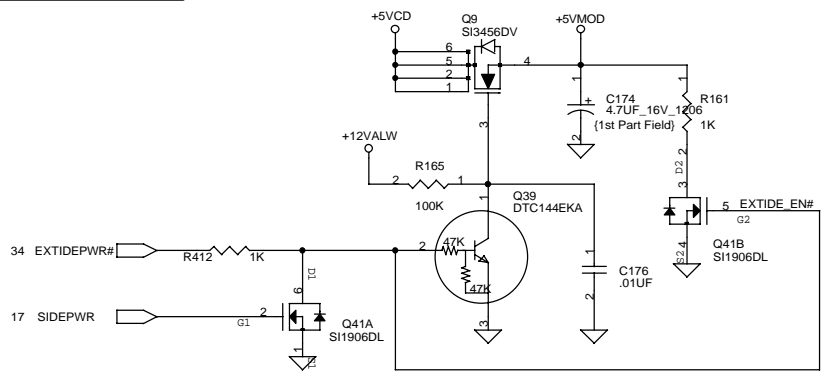
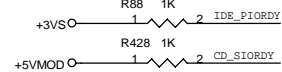
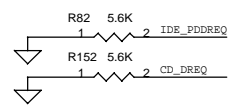
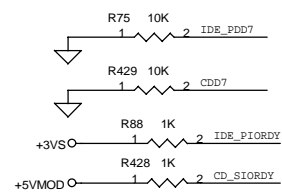
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Title	SCHEMATIC, M/B LA-1121	
Size	Document Number	Rev
Custom	401191 (FOR ATL02 / ACL00)	1C
Date:	星期一, 十一月 27, 2001	Sheet 19 of 87

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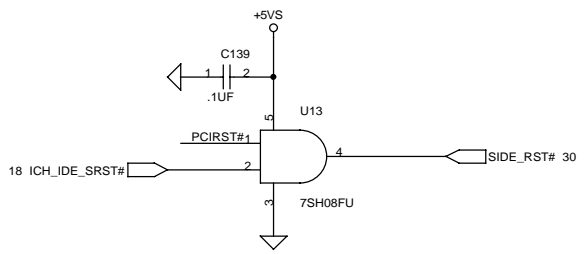
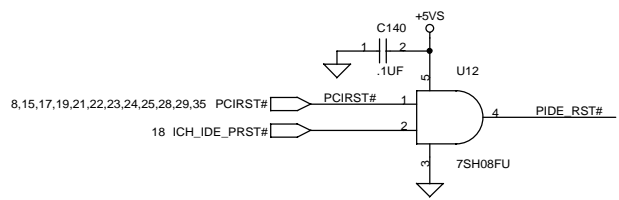
# IDE, CD-ROM Module CONN.



**HDD Manual ATA Type Selection:**  
 ATA33 : populate R43, de-populate R46.  
 ATA66/100 : populate R46, de-populate R43.

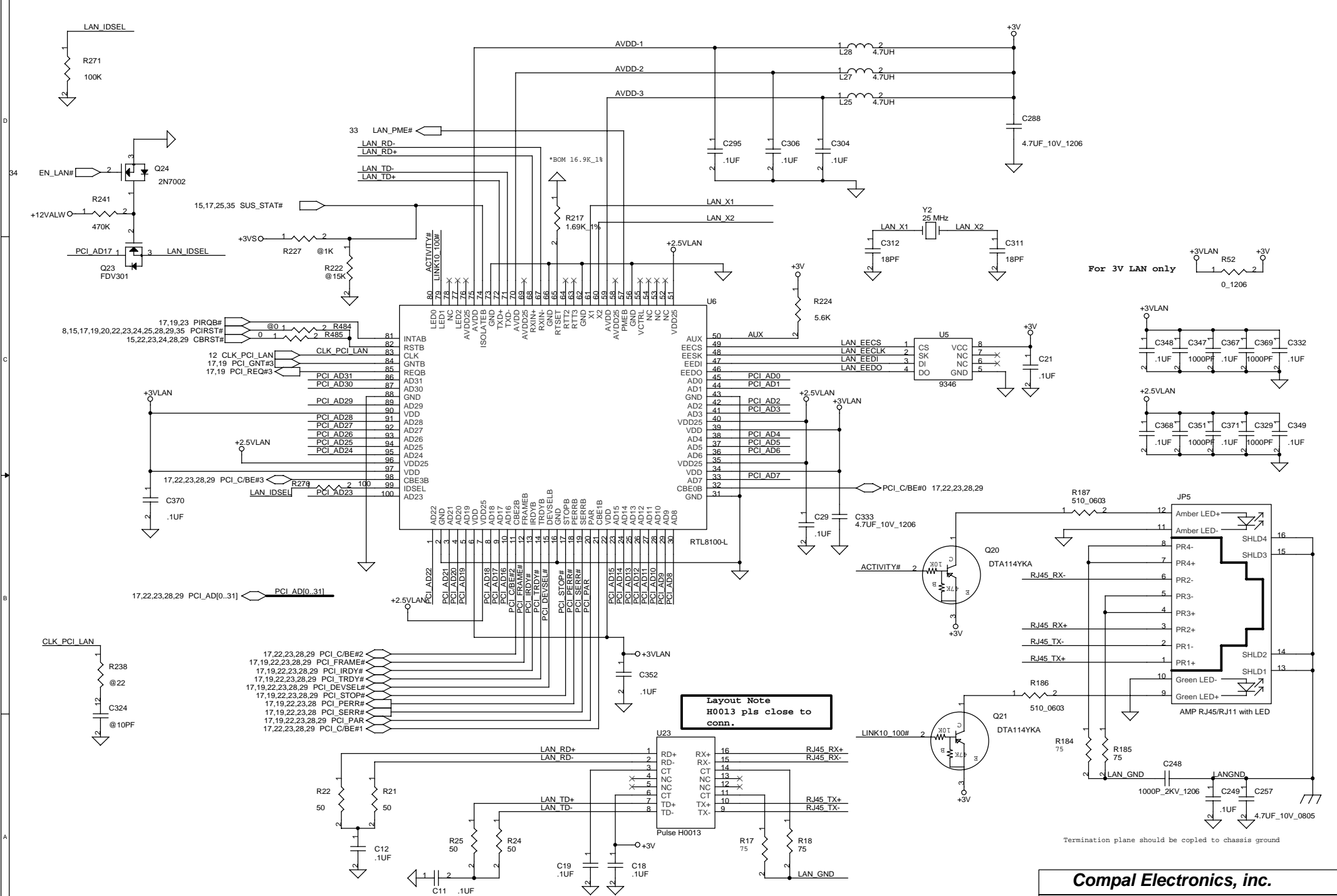


SI3456DV: N CHANNEL  
 VGS: 4.5V, RDS: 65 mOHM  
 Id(MAX): 5.1A  
 VGS,+20V



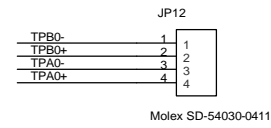
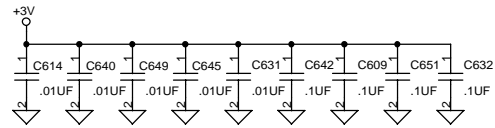
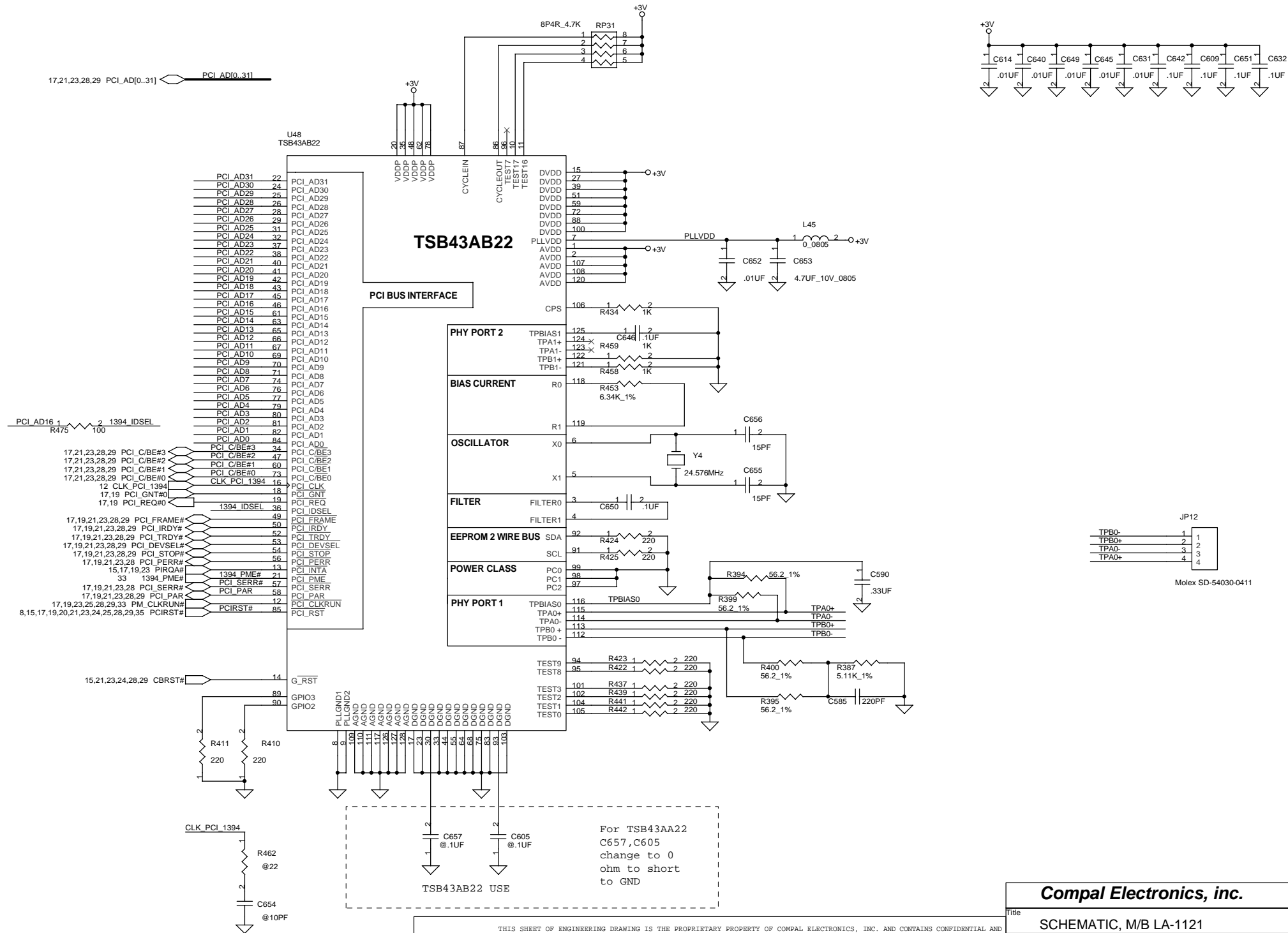
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Date:	星期二, 十一月 27, 2001	Sheet 20 of 87

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For 3V LAN only

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Date:	星期一, 十一月 27, 2001	Sheet 21 of 87



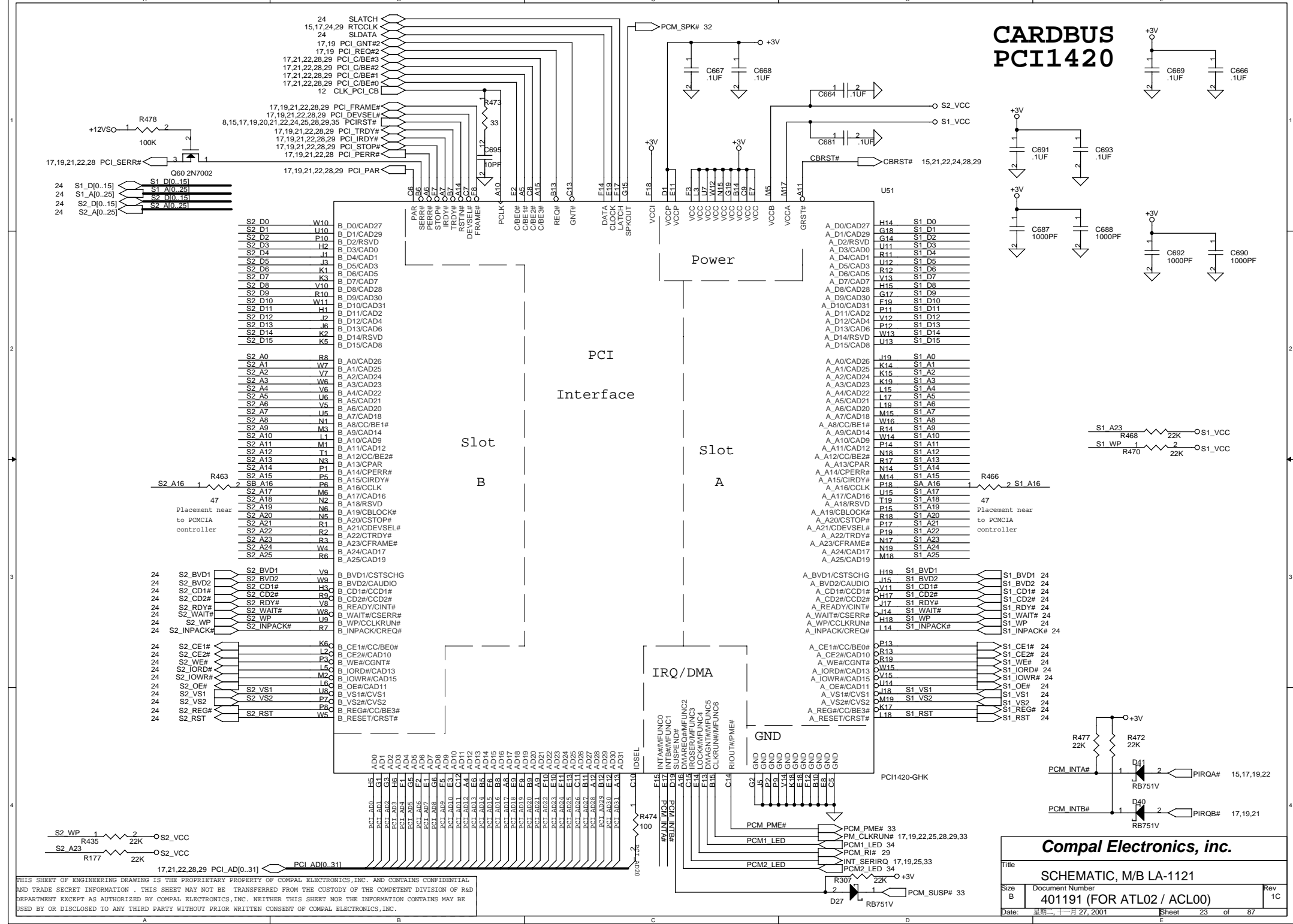
For TSB43AA22  
C657, C605  
change to 0  
ohm to short  
to GND

TSB43AB22 USE

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Size	Document Number	Rev
B	401191 (FOR ATL02 / ACL00)	1C
Date:	星期一, 十一月 27, 2001	Sheet 22 of 87

# CARDBUS PCI1420



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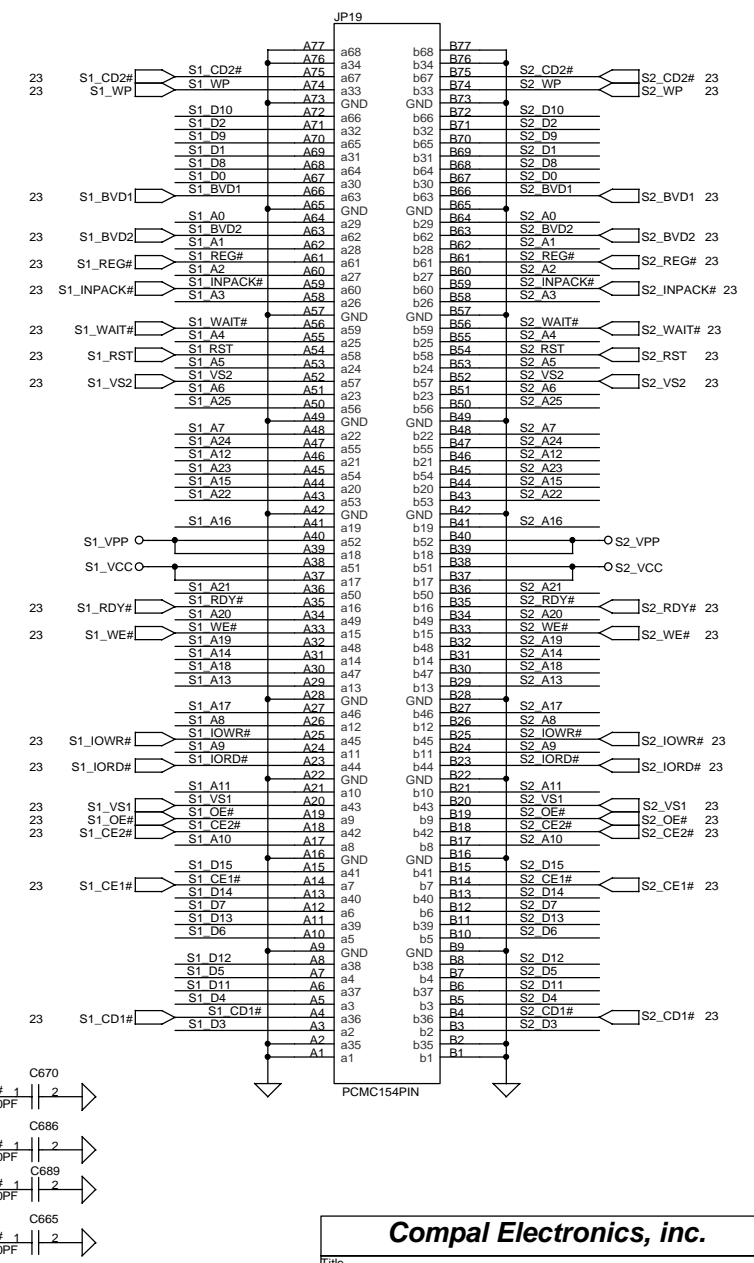
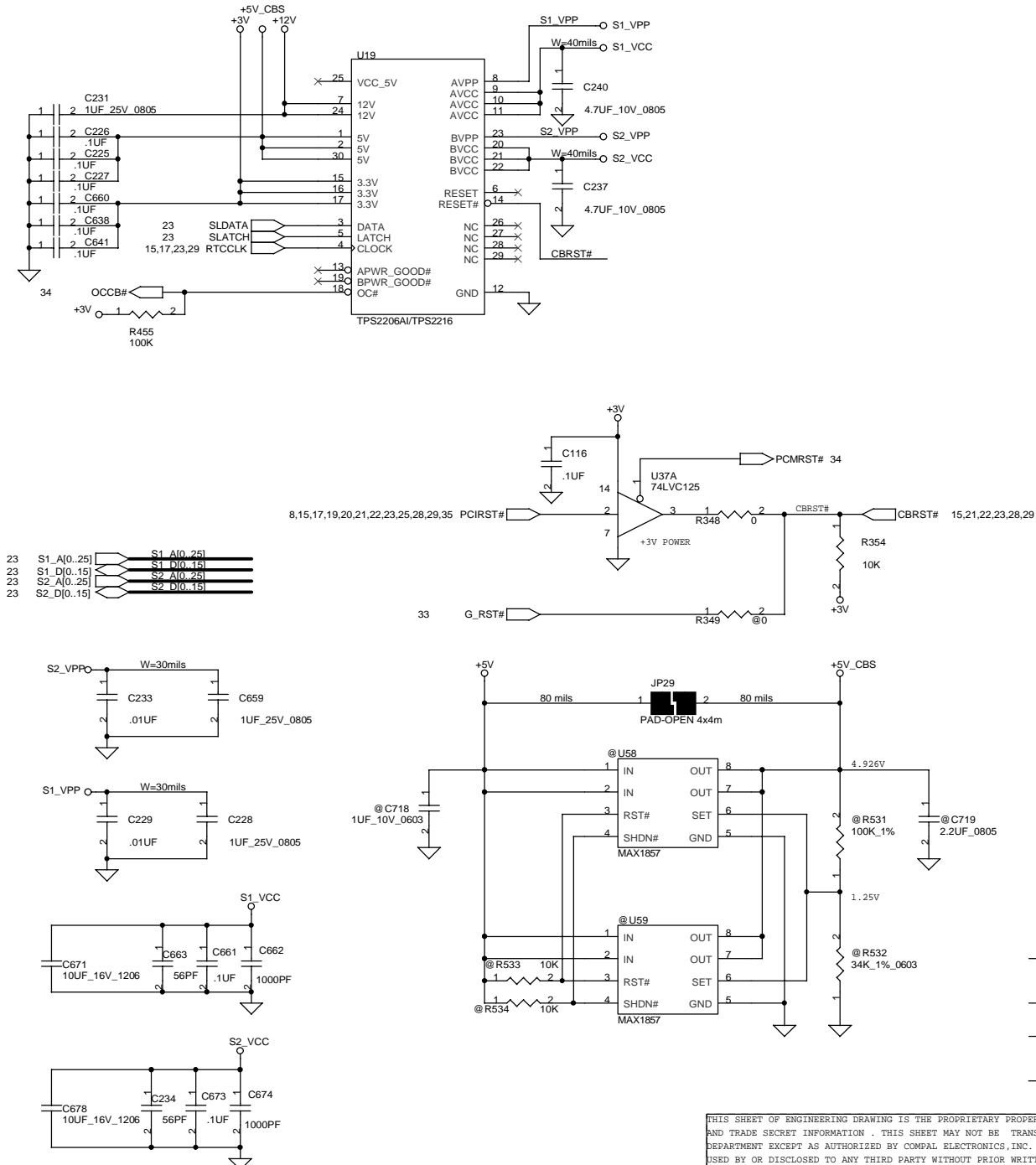
Title: SCHEMATIC, M/B LA-1121

Size: B Document Number: 401191 (FOR ATLO2 / ACL00) Rev: 1C

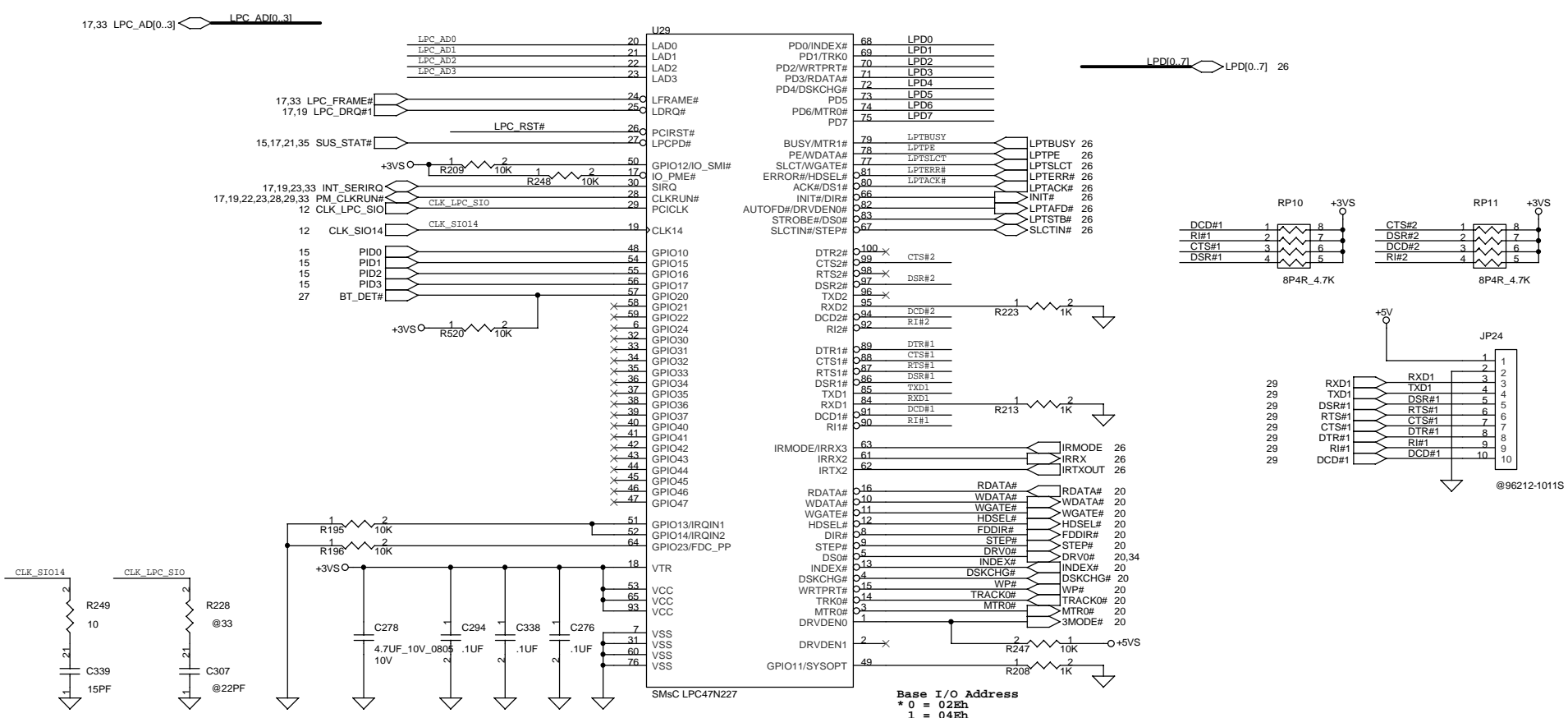
Date: 星期二, 十一月 27, 2001 Sheet: 23 of 87

# PCMCIA POWER CTRL.

# CARDBUS SOCKET



# SUPER I/O SMsC FDC47N227



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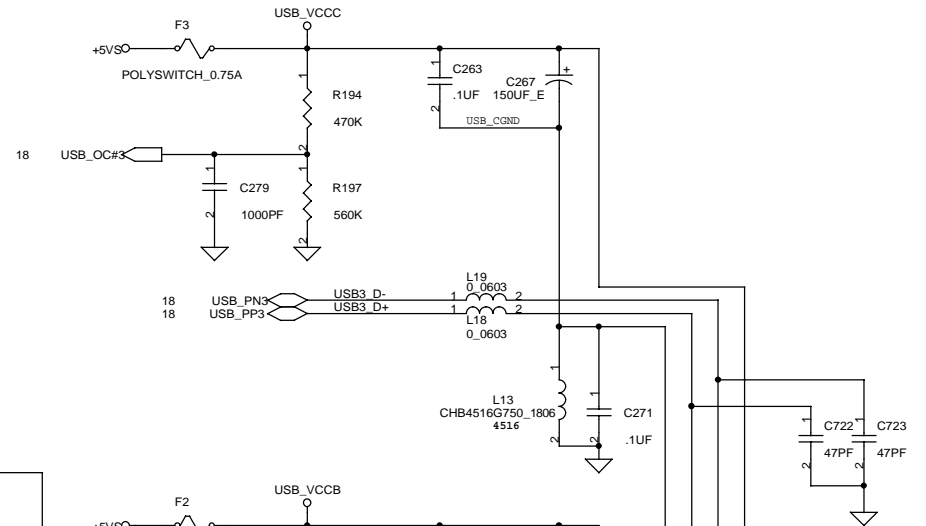
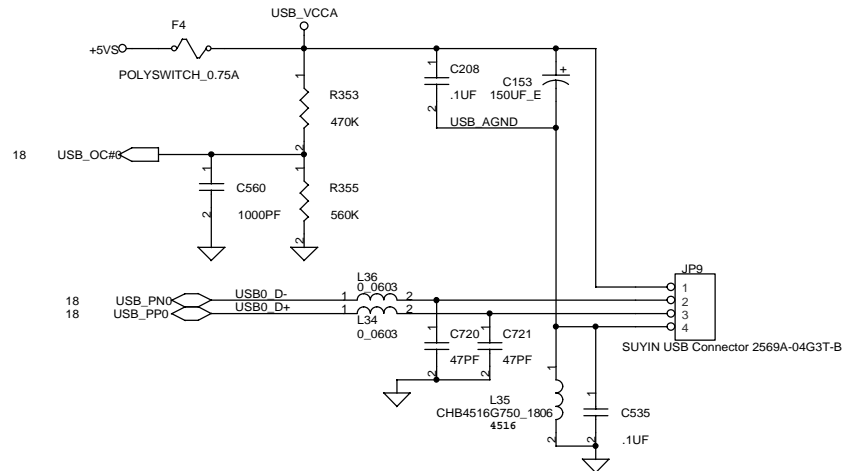
Date: 星期二, 十一月 27, 2001 Sheet 25 of 87

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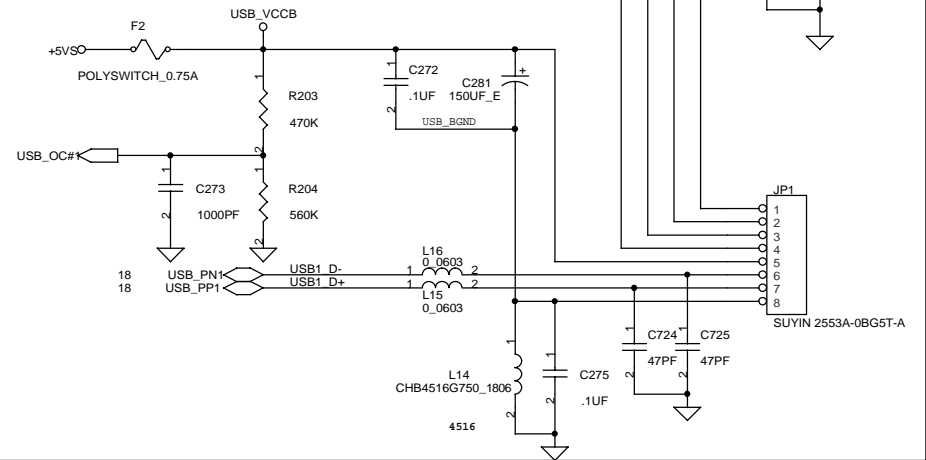
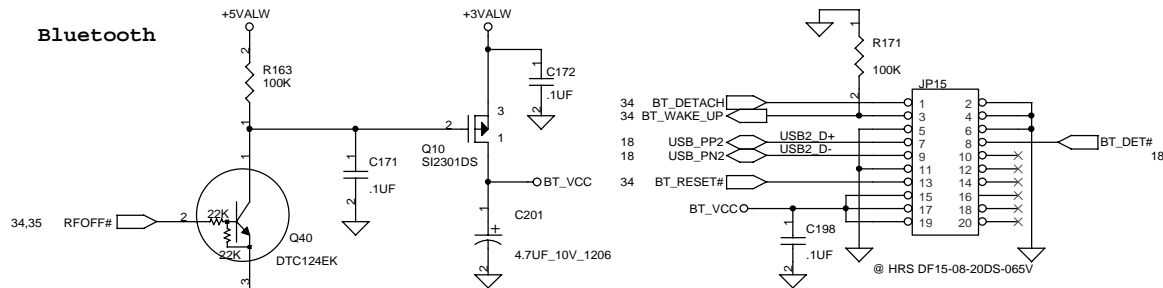




**USB PORT**

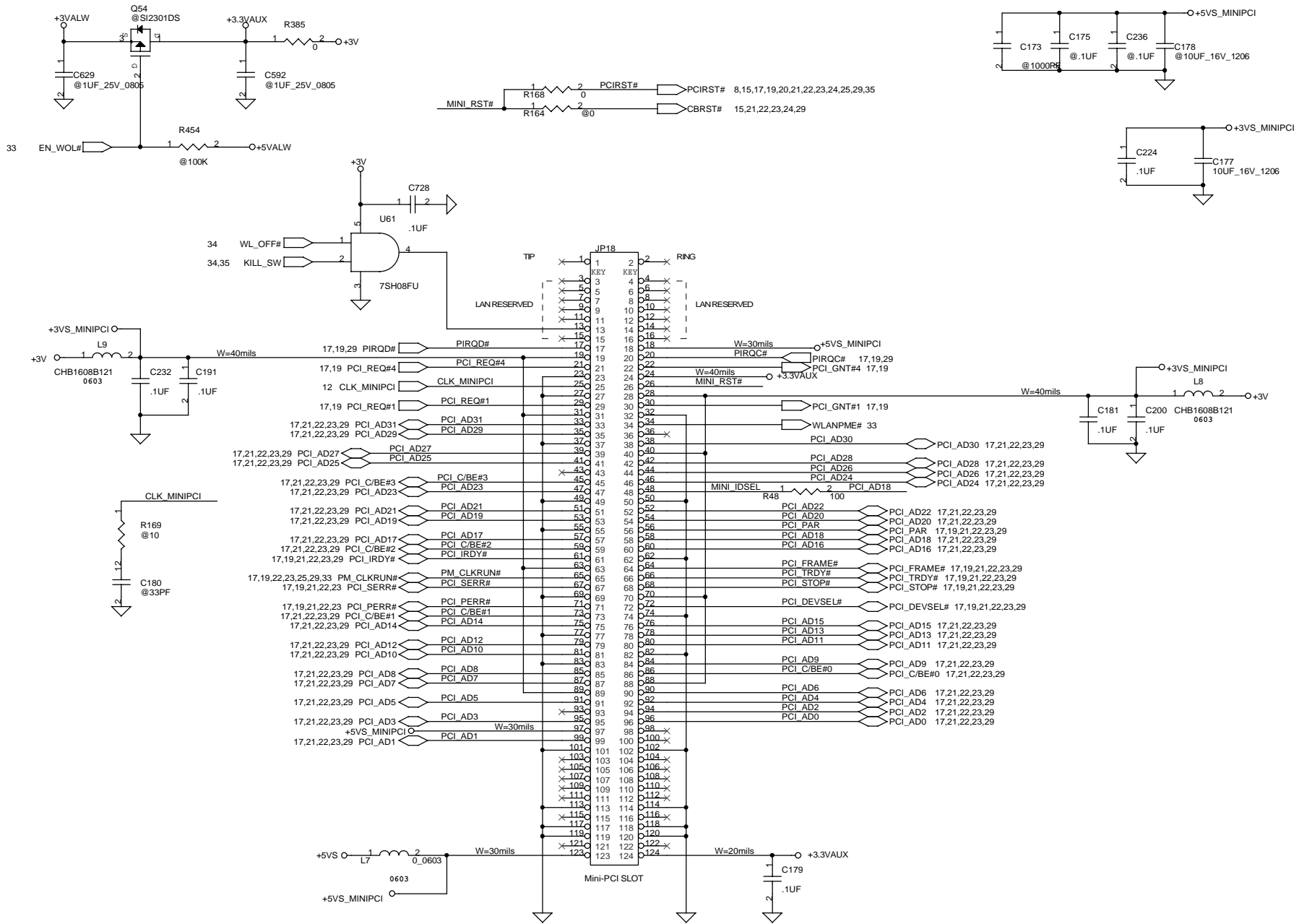


**Bluetooth**

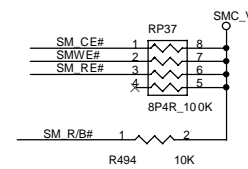
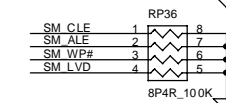
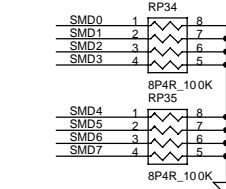
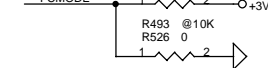
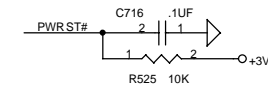
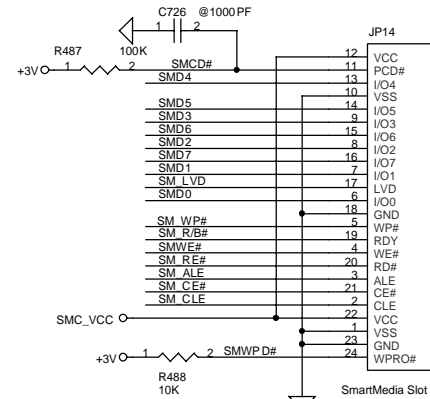
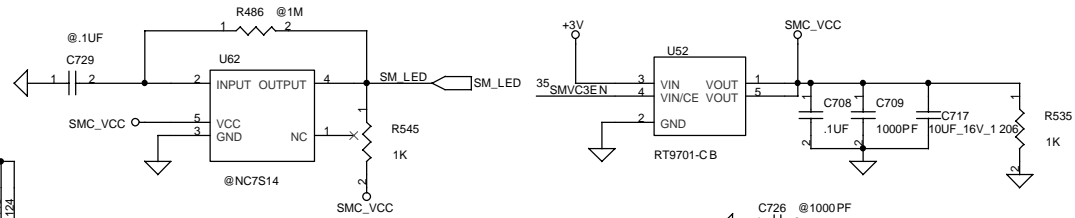
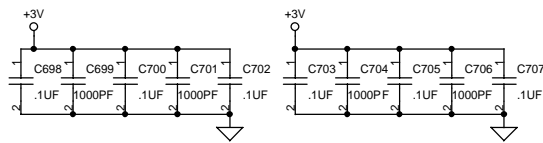


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Size	Document Number	Rev
B	401191 (FOR ATL02 / ACL00)	1C
Date:	星期二, 十一月 27, 2001	Sheet 27 of 87



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17,21,22,23,28 PCI\_AD[0..31] PCI\_AD[0..31]

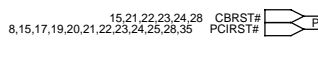
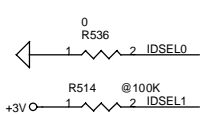
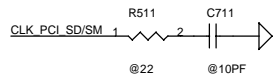
PCI AD0	53	AD0
PCI AD1	52	AD1
PCI AD2	61	AD2
PCI AD3	50	AD3
PCI AD4	48	AD4
PCI AD5	47	AD5
PCI AD6	46	AD6
PCI AD7	45	AD7
PCI AD8	42	AD8
PCI AD9	41	AD9
PCI AD10	40	AD10
PCI AD11	38	AD11
PCI AD12	37	AD12
PCI AD13	36	AD13
PCI AD14	35	AD14
PCI AD15	34	AD15
PCI AD16	22	AD16
PCI AD17	21	AD17
PCI AD18	20	AD18
PCI AD19	19	AD19
PCI AD20	18	AD20
PCI AD21	16	AD21
PCI AD22	15	AD22
PCI AD23	14	AD23
PCI AD24	10	AD24
PCI AD25	9	AD25
PCI AD26	8	AD26
PCI AD27	7	AD27
PCI AD28	5	AD28
PCI AD29	4	AD29
PCI AD30	3	AD30
PCI AD31	2	AD31
PCI C/BE#0	43	CBE0#
PCI C/BE#1	32	CBE1#
PCI C/BE#2	31	CBE2#
PCI C/BE#3	31	CBE3#
PCI PAR	30	PAR
PCI FRAME#	24	FRAME#
PCI LRDY#	25	LRDY#
PCI TRDY#	26	TRDY#
PCI_STOP#	29	STOP#
PCI AD22	R496 1	IDSEL0 130
PCI AD22	R497 1	IDSEL1 120

Power  
SmartMedia I/F  
System I/F  
GPIO I/F  
SD CARD I/F  
Test Pins  
GND

SMD0	86	SMD0
SMD1	83	SMD1
SMD2	93	SMD2
SMD3	95	SMD3
SMD4	99	SMD4
SMD5	96	SMD5
SMD6	94	SMD6
SMD7	91	SMD7
SM CLE	75	SM CLE
SM ALE	78	SM ALE
SM CE#	77	SM CE#
SMWE#	80	SMWE#
SM RE#	79	SM RE#
SM WP#	84	SM WP#
SM R/B#	82	SM R/B#
SMRB#	100	SMRB#
SMCD#	74	SMCD#
SM LVD	88	SM LVD
SMWP D#	73	SMWP D#
SMEJSW#	107	R490 1 2 100K
SMEJSW#	108	R491 1 2 100K +3V
SMEJSW#	106	R492 1 2 100K +3V
SMVC3EN	72	SMVC3EN
SMVC3EN	71	X

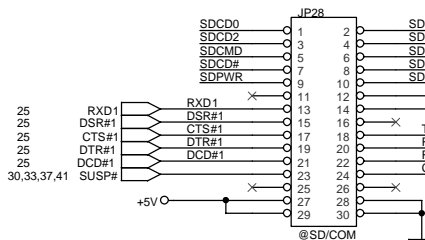
CLK32	PWRST#	RTCCCLK	15,17,23,24
SUSPEND#	FCMODE	SUSP#	30,33,37,41
ROM_CS	X		
ROM_SK	X		
ROM_D	X		
GPI00	R499 1	2 100K	+3V
GPI01	R500 1	2 100K	+3V
GPI02	R501 1	2 100K	+3V
GPI03	R502 1	2 100K	+3V
GPI04	R503 1	2 100K	+3V
GPI05	R504 1	2 100K	+3V
GPI06	R505 1	2 100K	+3V
GPI07	R506 1	2 100K	+3V
NC	X		
NC	X		
TEST0	61	R508 0	
TEST1	62		
TEST2	63		
TEST3	64		

When the serial ROM interface is not applied need pull up.



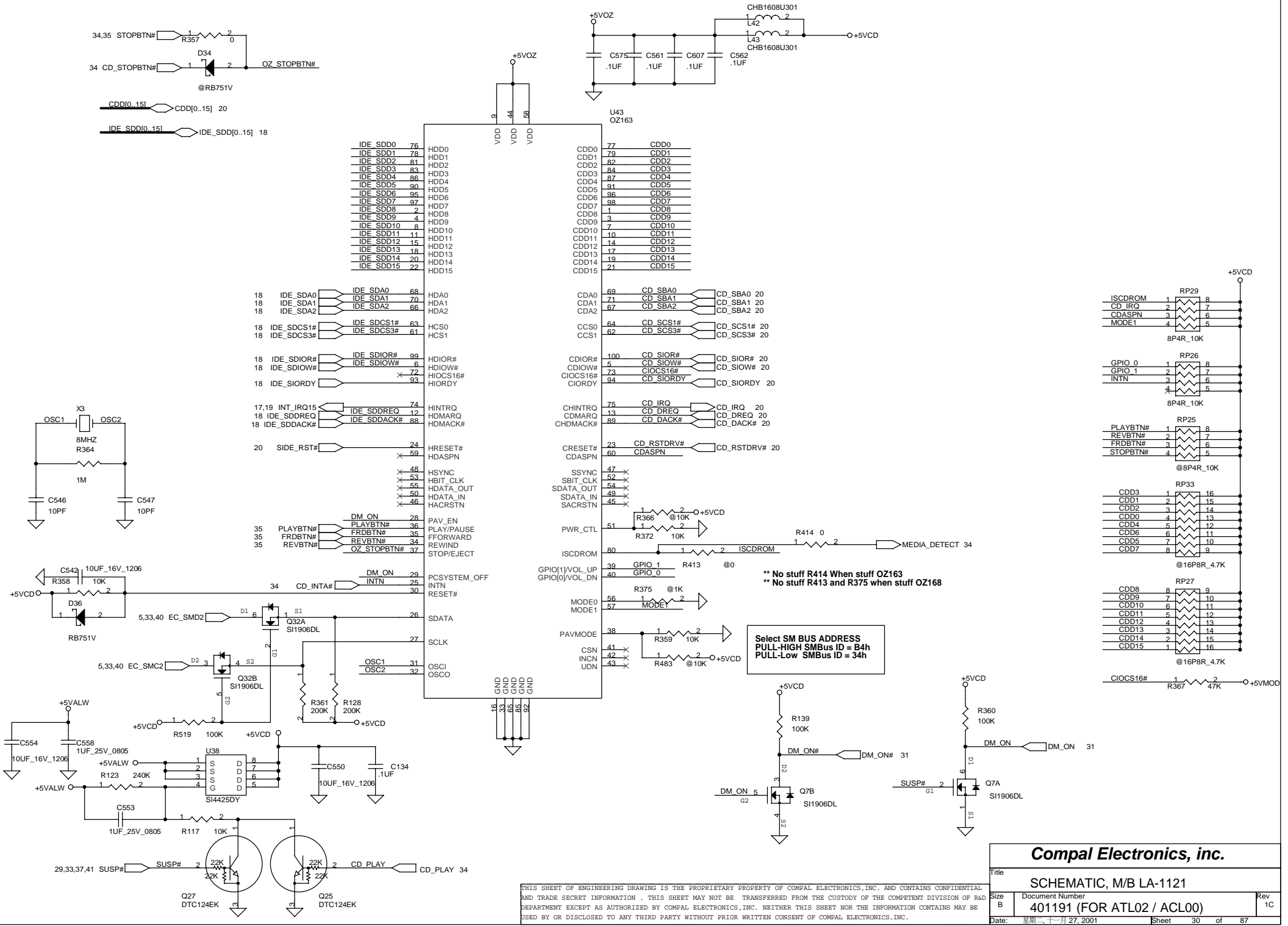
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17,19,21,22,23,28	PCI_DEVSEL#	27	DEVSEL#
17,19,21,22,23,28	CLK_PCI_SD/SM	125	PCICLK
17,19,28	PIROC#	121	PCIRST#
17,19,28	PIROD#	122	INT#
33	SM/SD_PME#	128	PME#
R537 1	2 100K	SDCD0	101
R538 1	2 100K	SDCD1	102
R539 1	2 100K	SDCD2	83
R540 1	2 100K	SDCD3	85
R541 1	2 100K	SDCMD	89
1	2	88	SDCLK
1	2	104	SDPWR
1	2	105	SDPWR
1	2	69	SDPWR

SD Transfer Conn.



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Size B	Document Number 401191 (FOR ATL02 / ACL00)	Rev 1C
Date:	星期一,十一月 27, 2001	Sheet 29 of 87



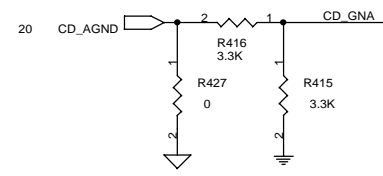
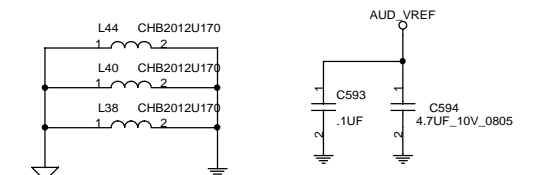
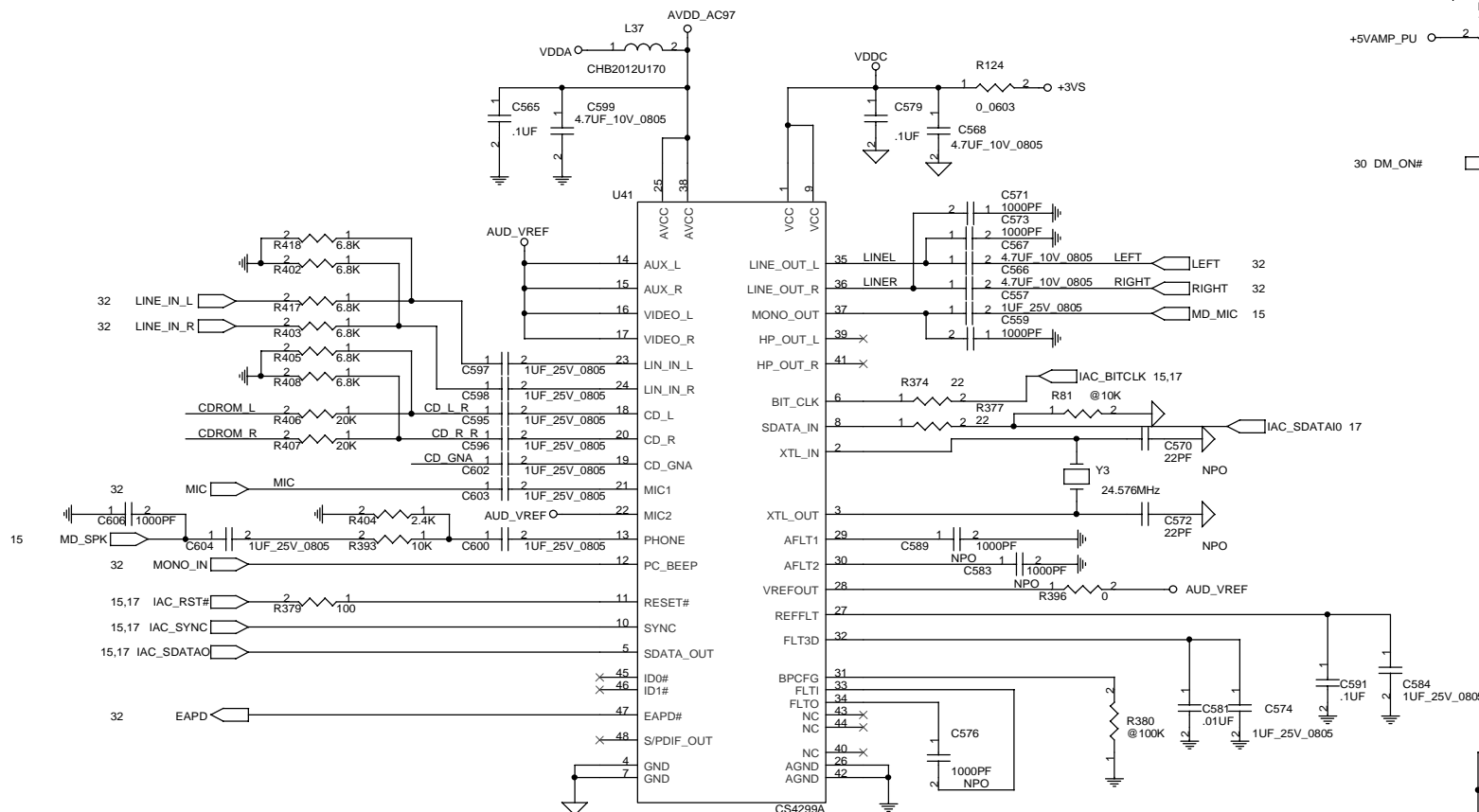
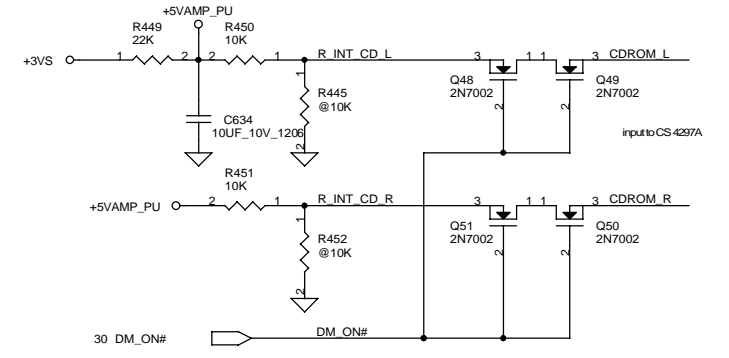
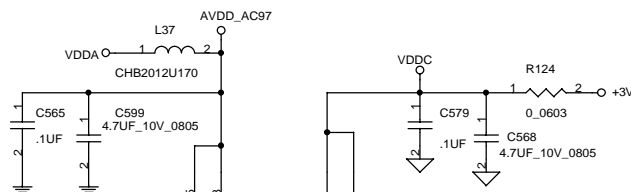
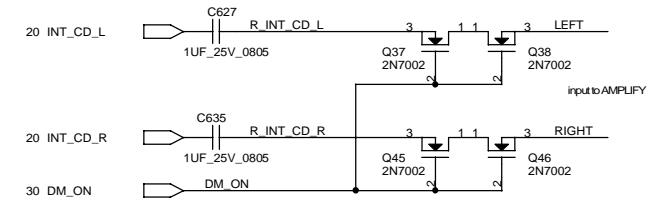
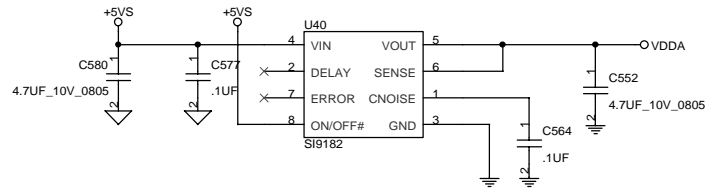
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Size B Document Number 401191 (FOR ATL02 / ACL00) Rev 1C

Date: 星期二, 十一月 27, 2001 Sheet 30 of 87

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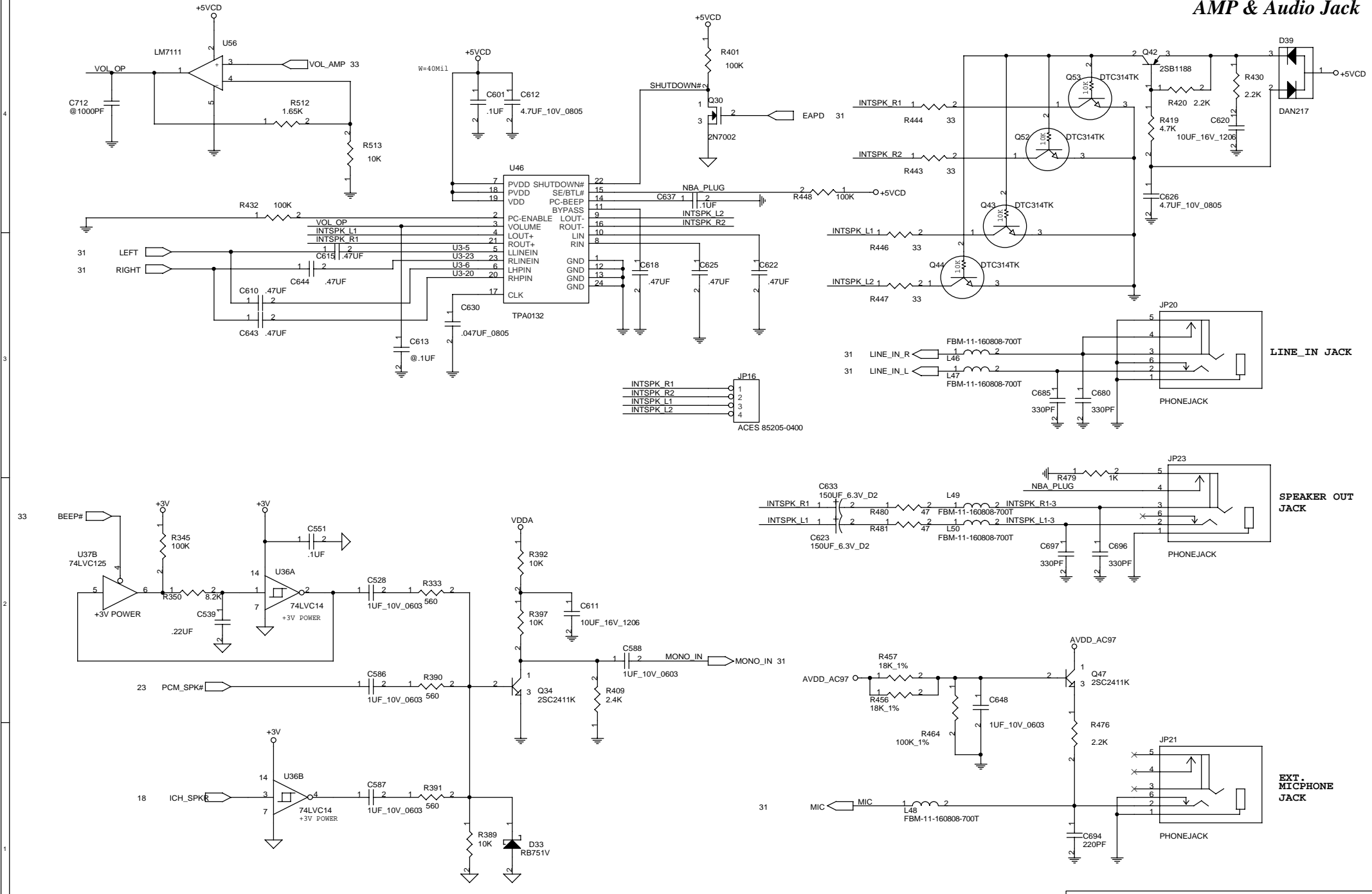


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Title	SCHEMATIC, M/B LA-1121	
Size	Document Number	Rev
B	401191 (FOR ATLO2 / ACL00)	1C
Date:	星期二, 十一月 27, 2001	Sheet 31 of 87

# AMP & Audio Jack



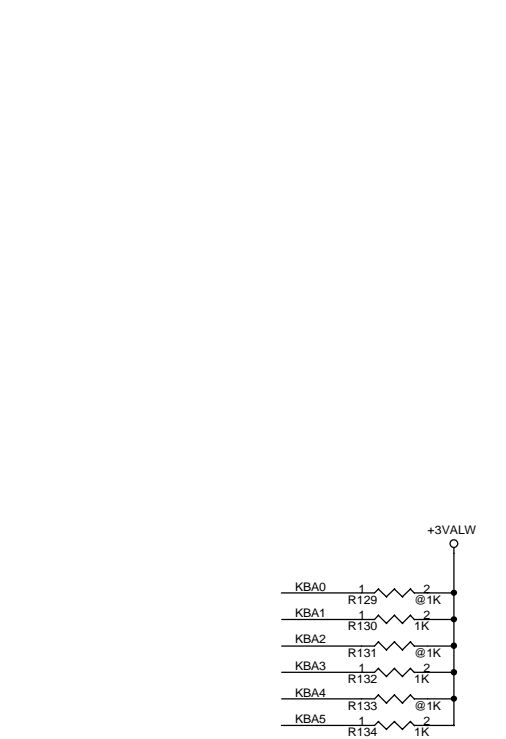
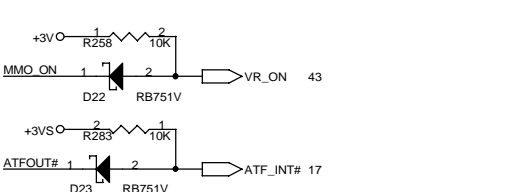
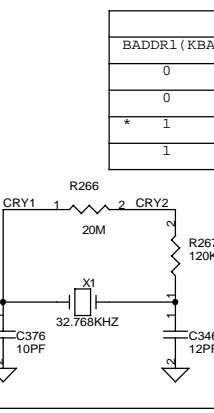
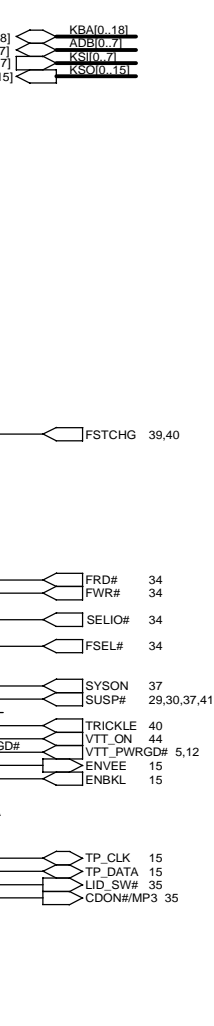
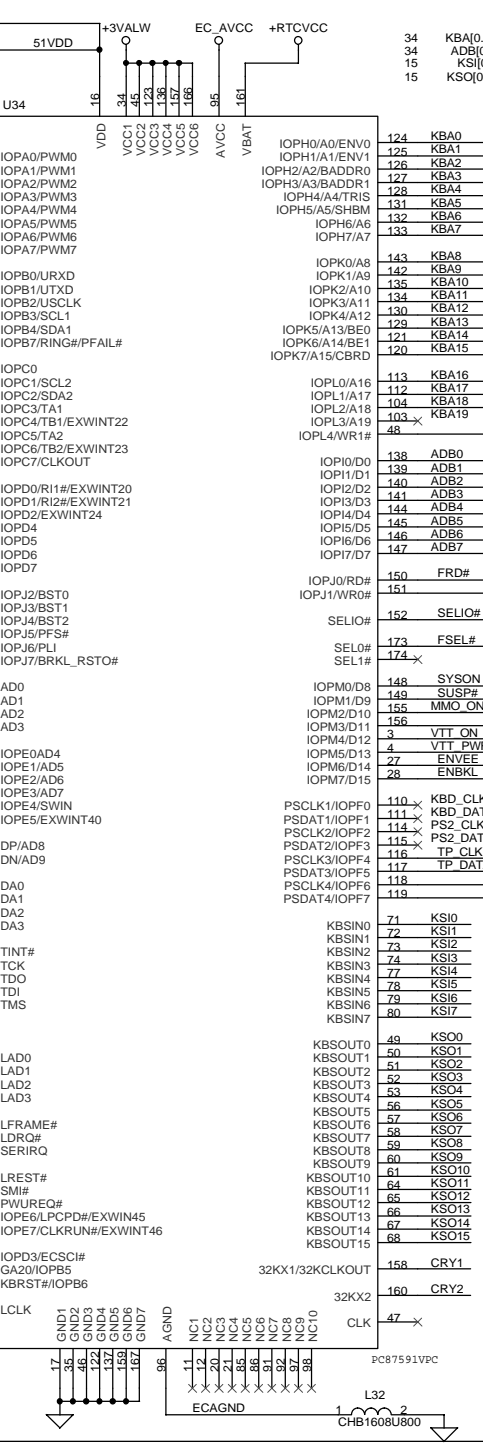
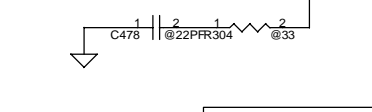
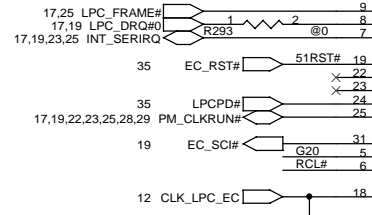
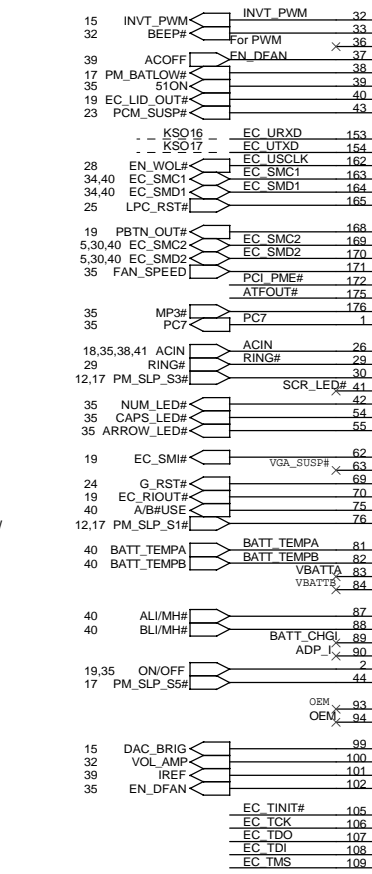
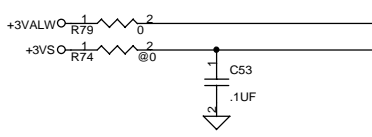
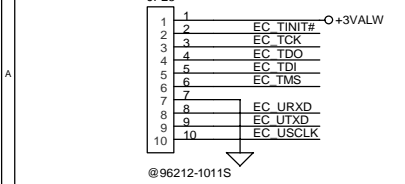
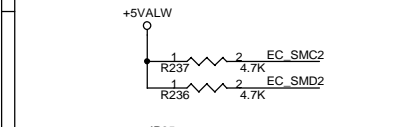
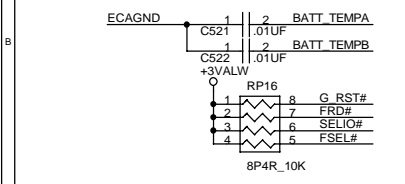
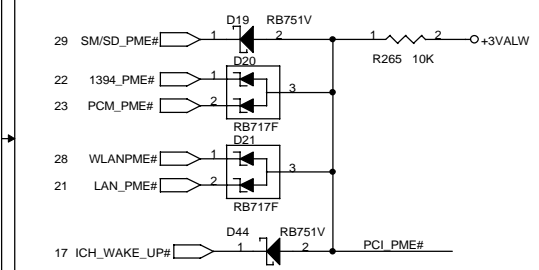
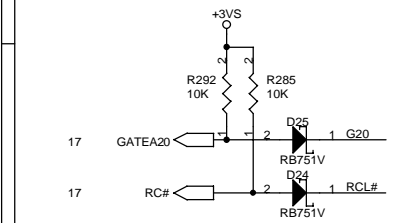
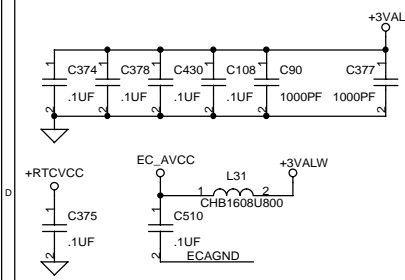
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Document Number 401191 (FOR ATLO2 / ACL00) Rev 1C

Date: 星期一, 十一月 27, 2001 Sheet 32 of 87

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I/O Address			
BADDR1 (KBA3)	BADDR0 (KBA2)	Index	Data
0	0	2E	2F
0	1	4E	4F
* 1	0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1	1	Reserved	

	ENVO (KBA0)	ENV1 (KBA1)	TRIS (KBA4)
IRE	0	0	0
* OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

SHBM(KBA5)=1: Enable shared memory with host BIOS  
 TRIS(KBA4)=1: While in IRE and OBD, float all the signals for clip-on ISE use

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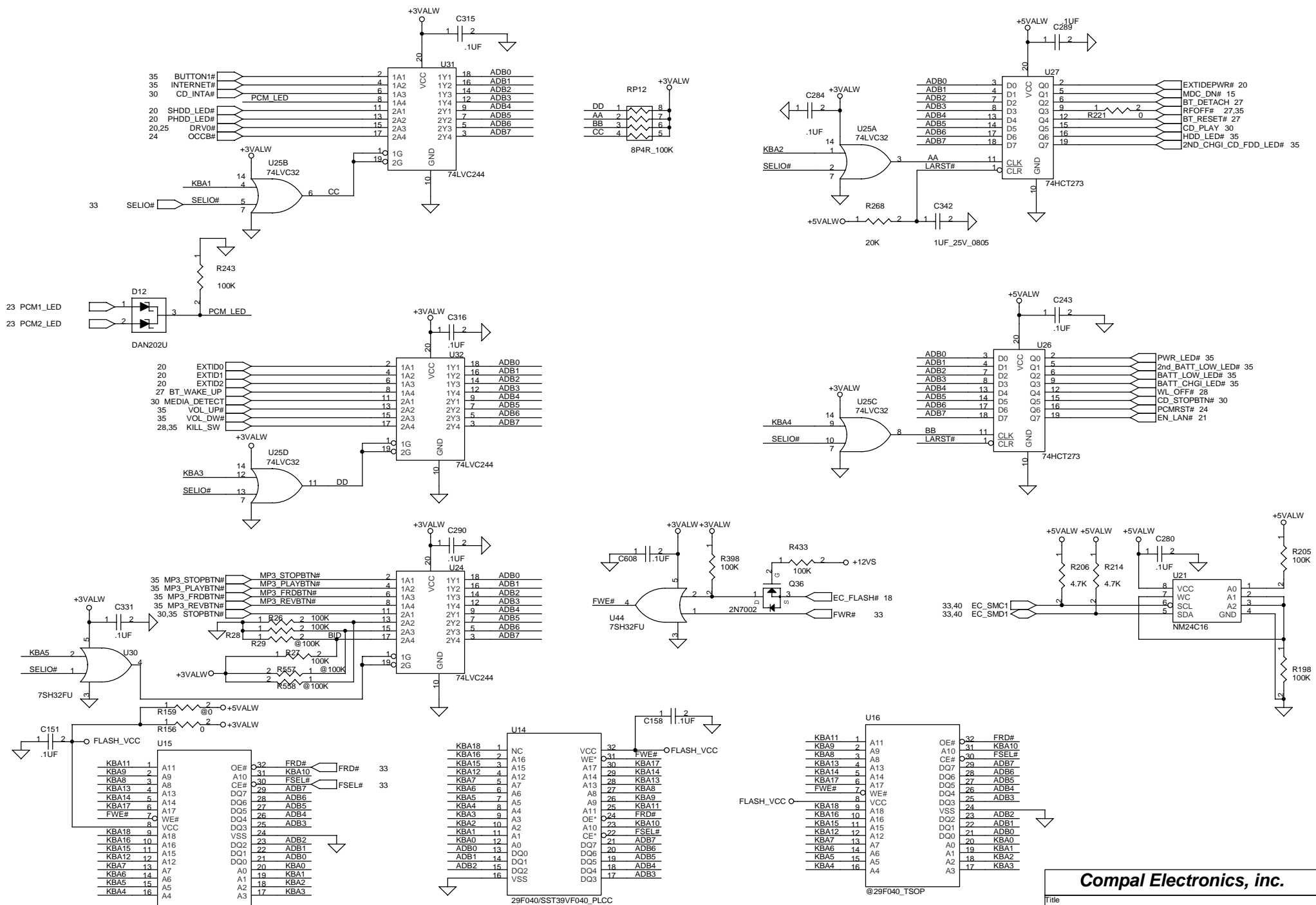
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Size B Document Number 401191 (FOR ATL02 / ACL00) Rev 1C

Date: 星期二, 十一月 27, 2001 Sheet 33 of 87

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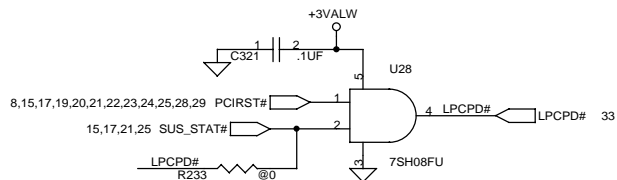
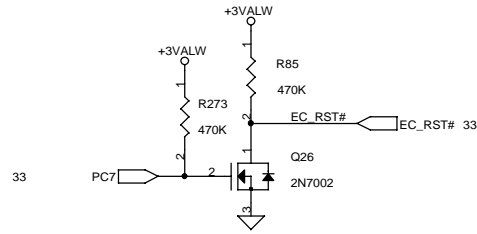




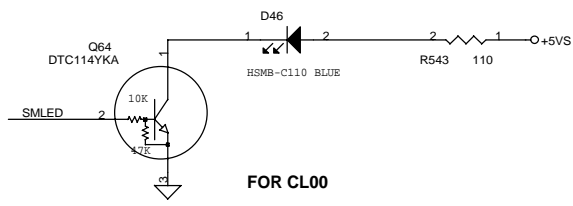
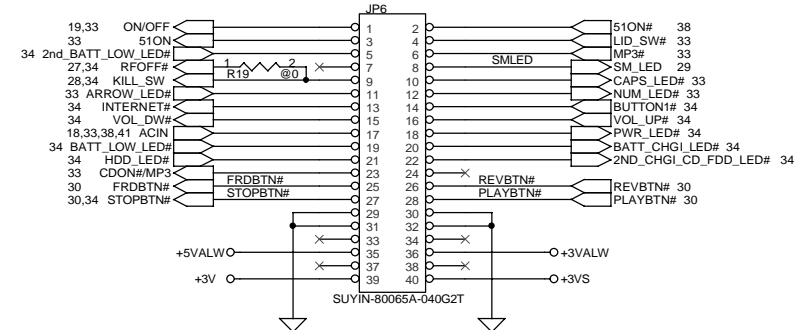
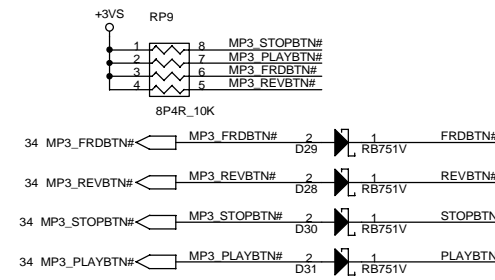
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Title		
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Size	Document Number	Rev
B	401191 (FOR ATL02 / ACL00)	1C
Date:	星期二, 十一月 27, 2001	Sheet 34 of 87

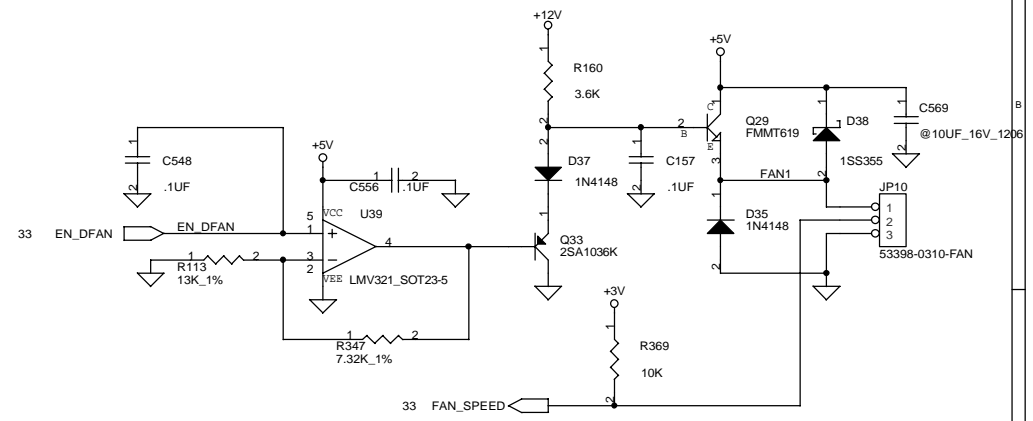


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FOR CL00

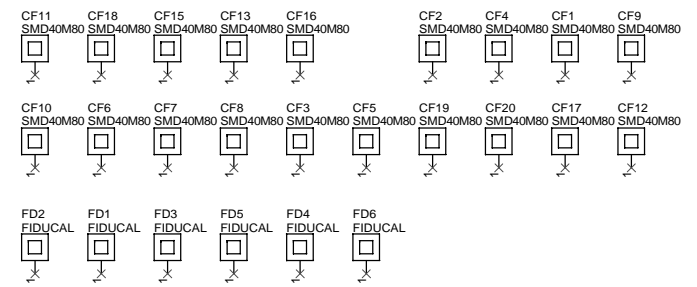
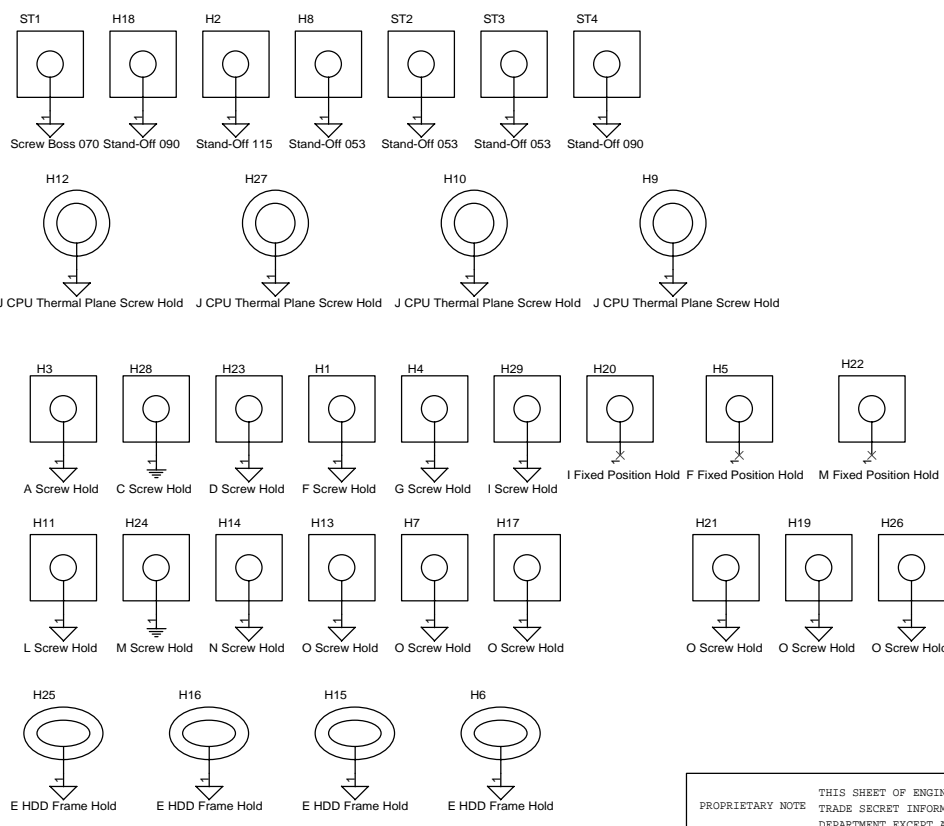
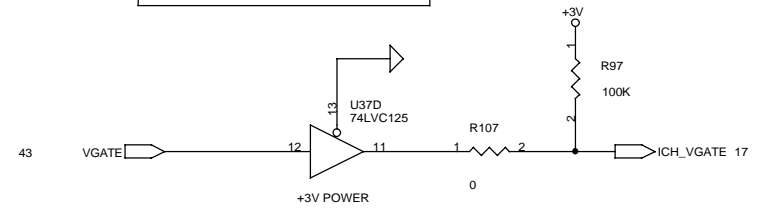
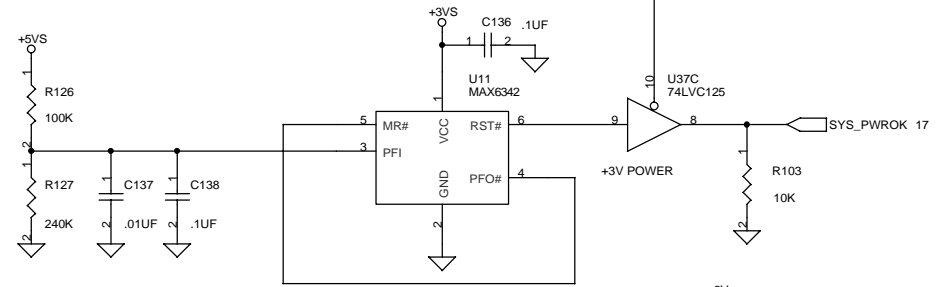
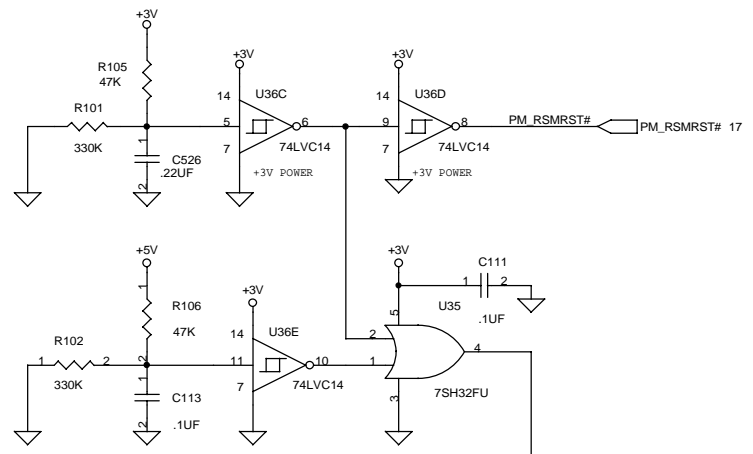
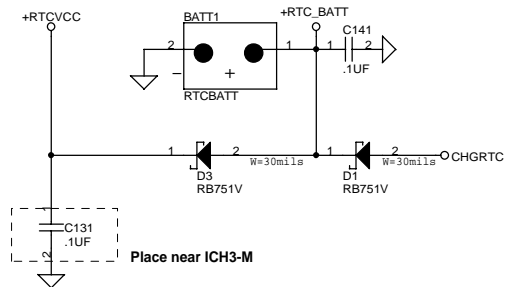
FAN CONN.



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Title	SCHEMATIC, M/B LA-1121	
Size	Document Number	Rev
B	401191 (FOR ATL02 / ACL00)	1C
Date:	星期二, 十一月 27, 2001	Sheet 35 of 87

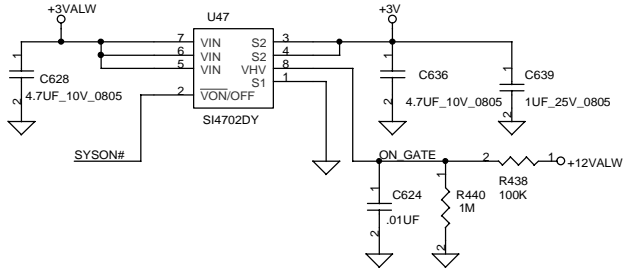
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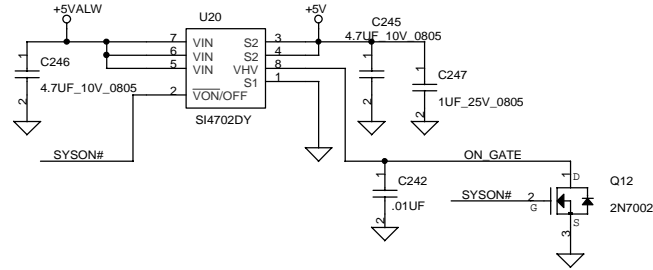
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Title	SCHEMATIC, M/B LA-1121	
Size	Document Number	Rev
B	401191 (FOR ATL02 / ACL00)	1C
Date:	星期二, 十一月 27, 2001	Sheet 36 of 87

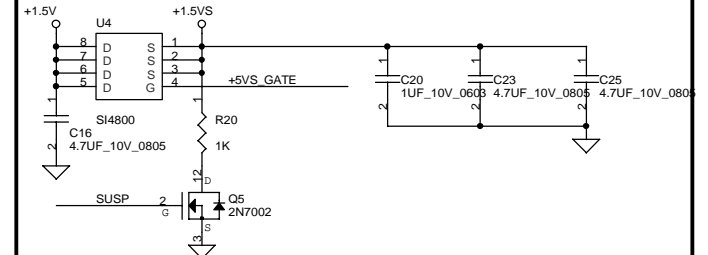
**+3VALW To +3V Transfer**



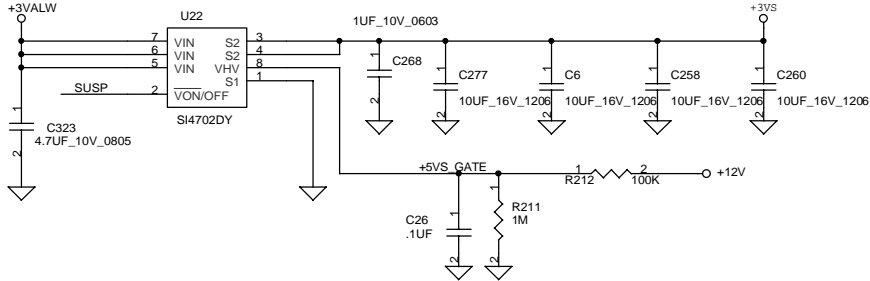
**+5VALW To +5V Transfer**



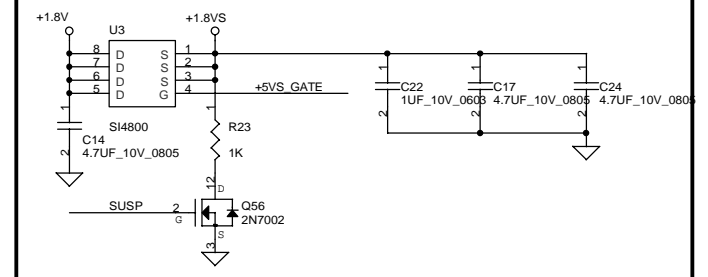
**+1.5V TO +1.5V\_SW Transfer**



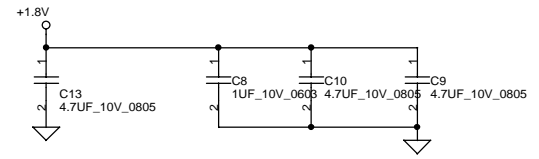
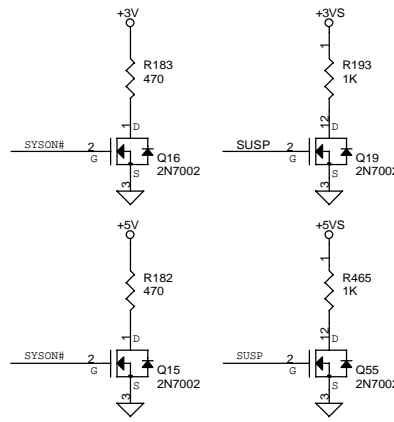
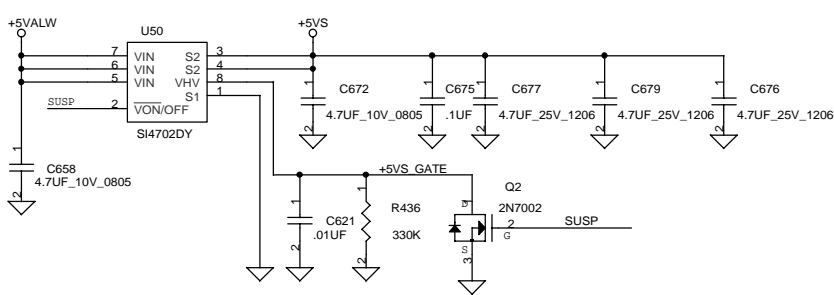
**+3VALW To +3VS Transfer**



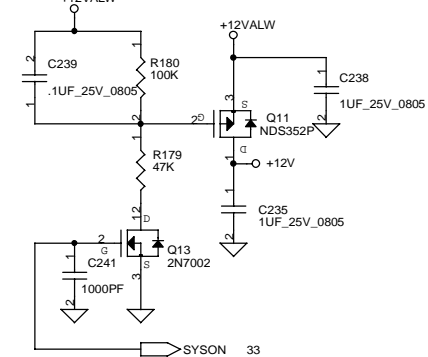
**+1.8V\_ALW TO +1.8V\_SW Transfer**



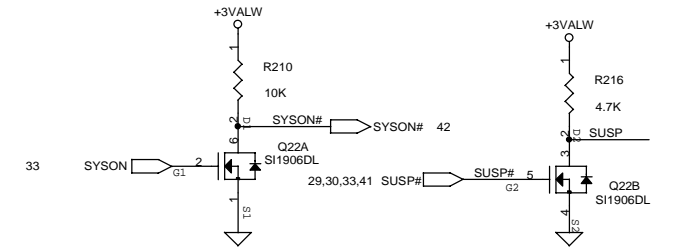
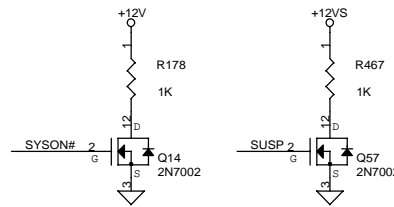
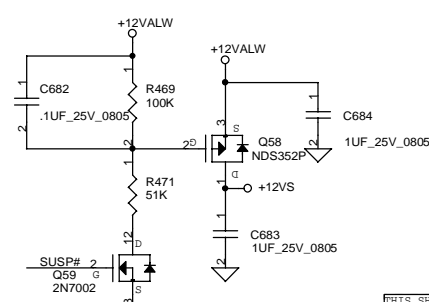
**+5VALW To +5VS Transfer**



**+12VALW To +12V Transfer**



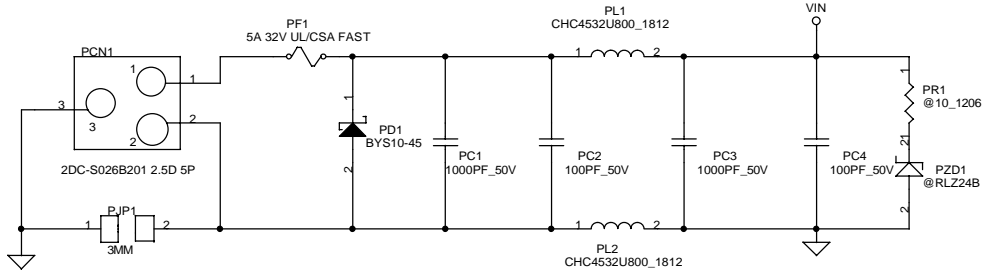
**+12VALW To +12VS Transfer**



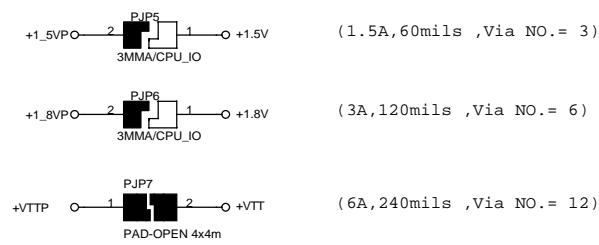
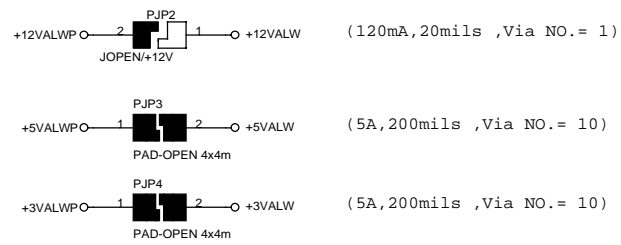
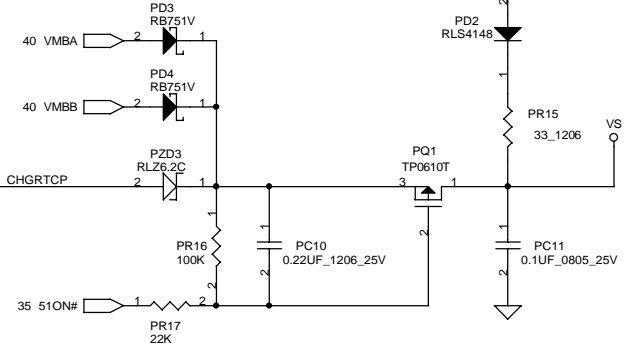
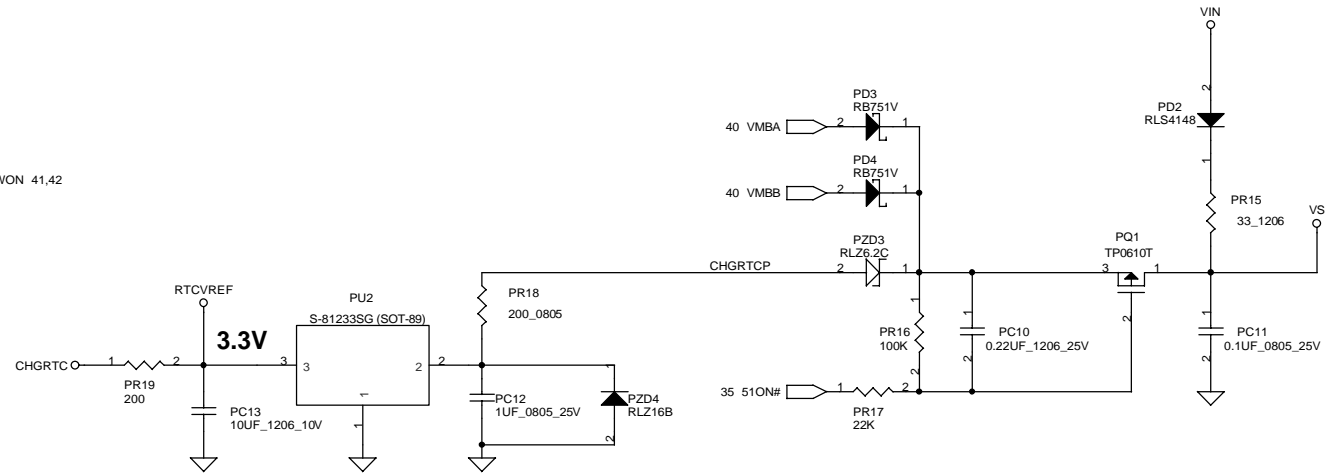
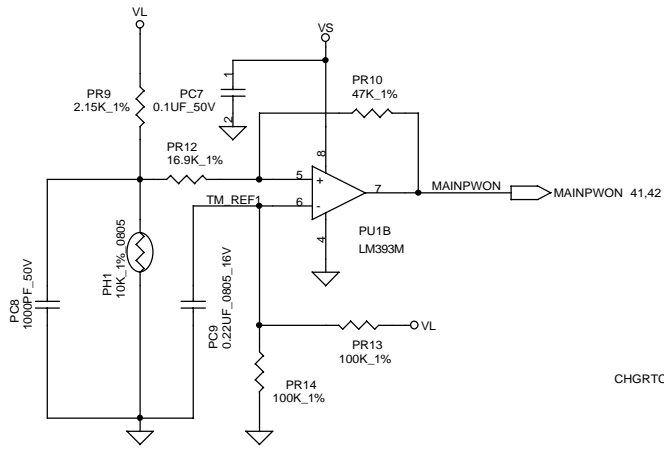
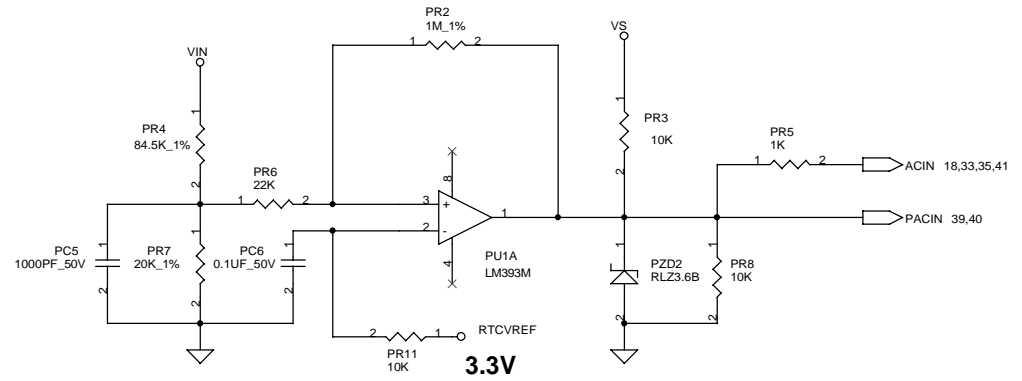
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Title	SCHEMATIC, M/B LA-1121	
Size	Document Number	Rev
Custom	401191 (FOR ATL02 / ACL00)	1C
Date:	星期一, 十一月 27, 2001	Sheet 37 of 87

**Vin Detector**  
**High 18.764 17.901 17.063**  
**Low 17.745 16.903 16.038**

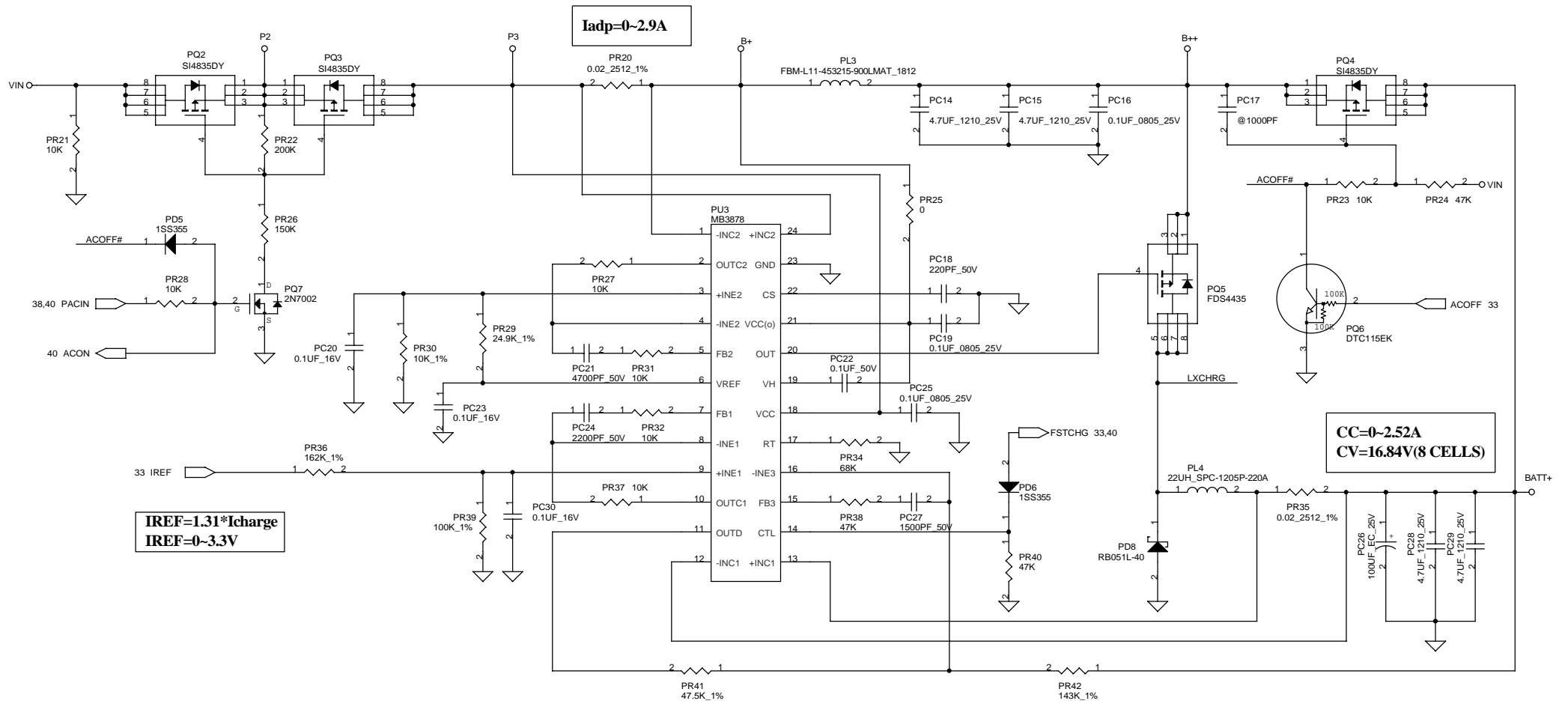


**PH1 under CPU bottom side :**  
 CPU thermal protection at 81(82) degree C  
 Recovery at 50(51) degree C



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Title SCHEMATIC, M/B LA-1121		
Size B	Document Number 401191 (FOR ATL02 / ACL00)	Rev 1C
Date: 星期二, 十一月 27, 2001	Sheet 38	of 87

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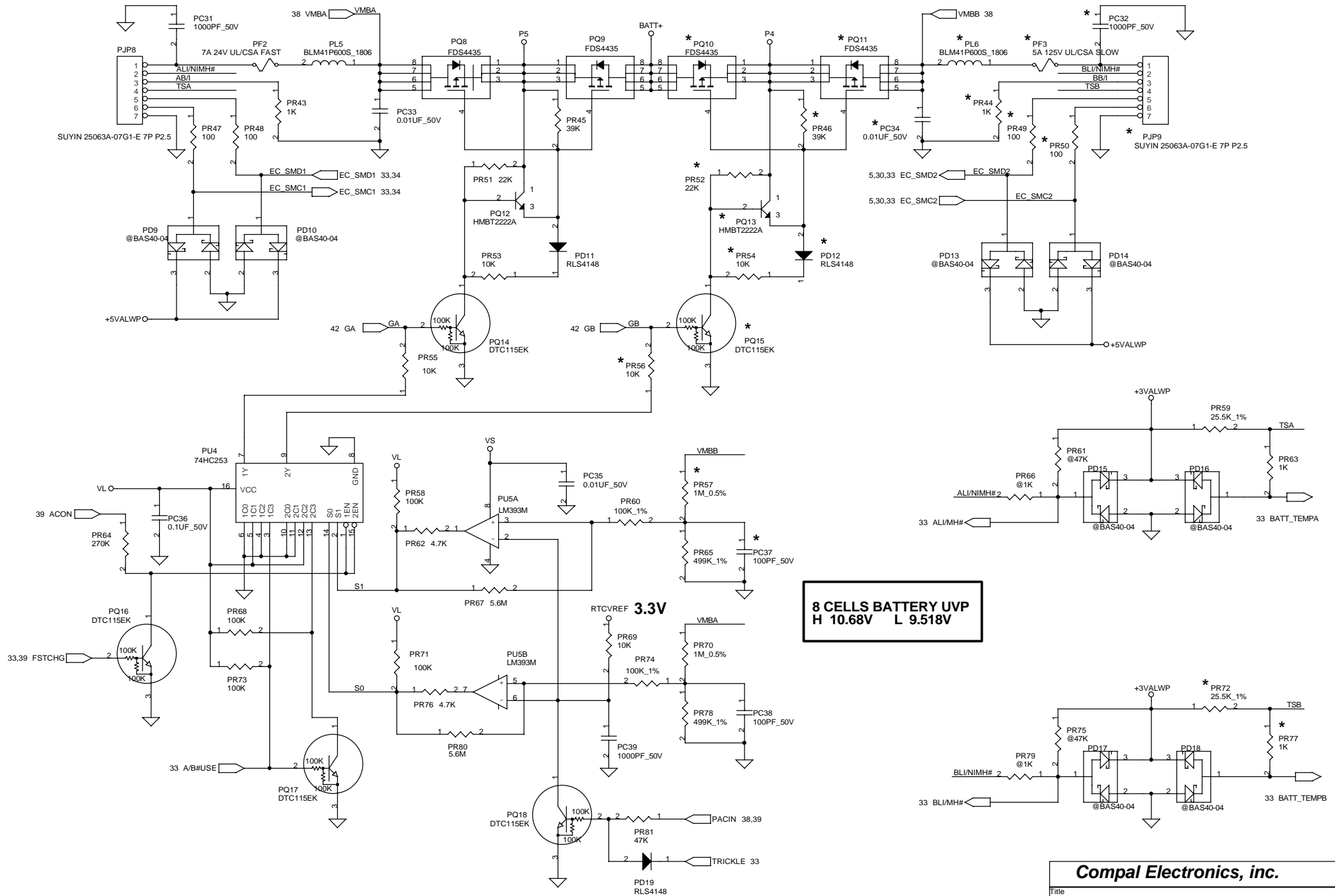


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Title		SCHEMATIC, M/B LA-1121	
Size		Document Number	
<b>B</b>		<b>401191 (FOR ATL02 / ACL00)</b>	Rev
Date:	星期二, 十一月 27, 2001	Sheet	39 of 87

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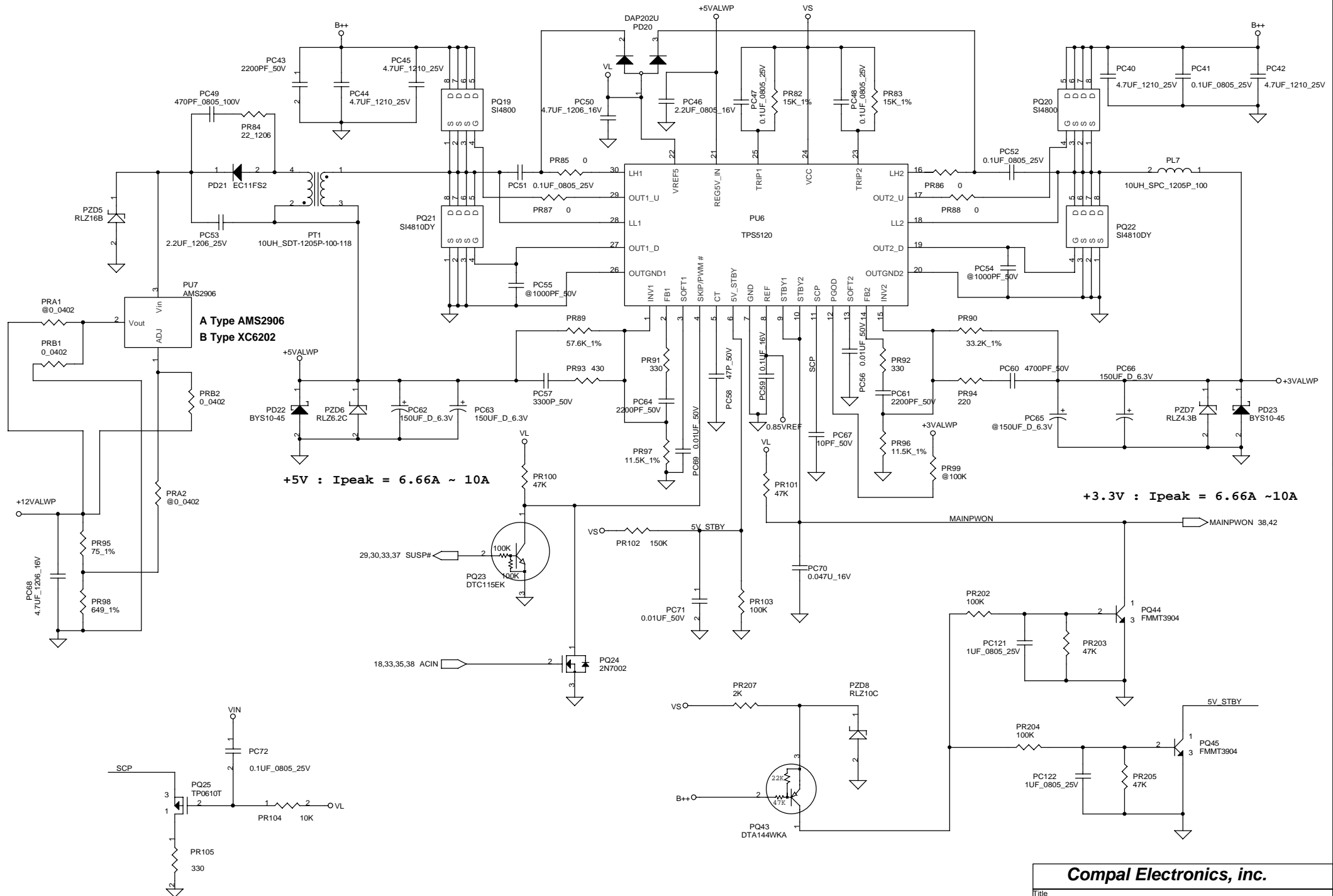
The \* is DEL item only for ACL00



**8 CELLS BATTERY UVP  
H 10.68V L 9.518V**

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Title		
SCHEMATIC, M/B LA-1121		
Size	Document Number	Rev
B	401191 (FOR ATL02 / ACL00)	1C
Date:	星期三, 十一月 27, 2001	Sheet 40 of 87

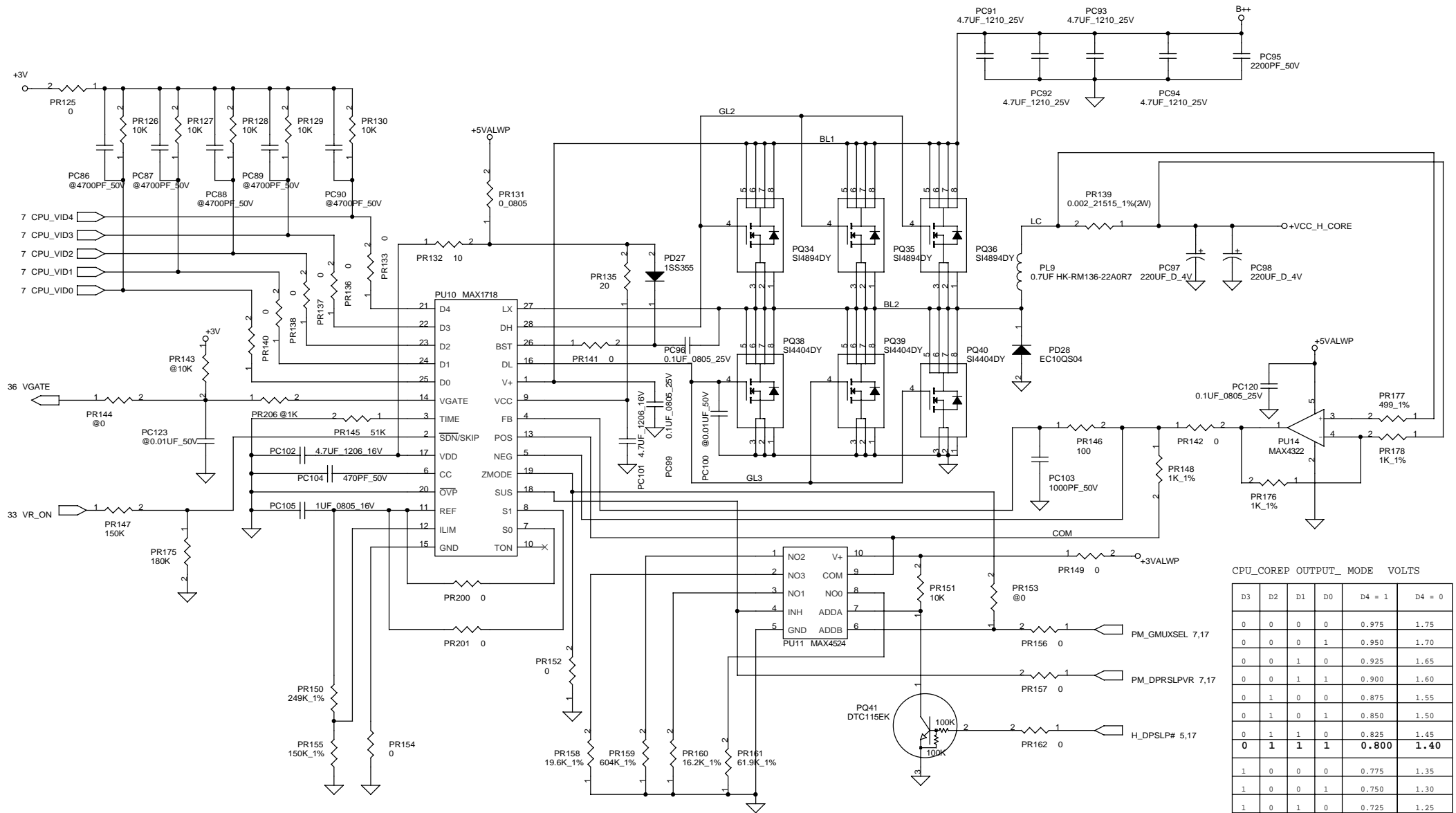


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Title		
SCHEMATIC, M/B LA-1121		
Size	Document Number	Rev
B	401191 (FOR ATL02 / ACL00)	1C
Date:	星期二, 十一月 27, 2001	Sheet 41 of 87

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CPU CONTROL MODE

MODE	OFFSET	RBOTTOM	V <sub>out</sub> (0A)	ADDA	ADDB
DEEPER SLEEP	0mV	X	0.850	X	X
BATTERY SLEEP	-56mV	16.2K	1.094	1	0
PERFORMANCE SLEEP	-51mV	19.6K	1.199	1	1
BATTERY MODE	-16mV	61.9K	1.134	0	0
PERFORMANCE MODE	-1.8mV	604K	1.248	0	1

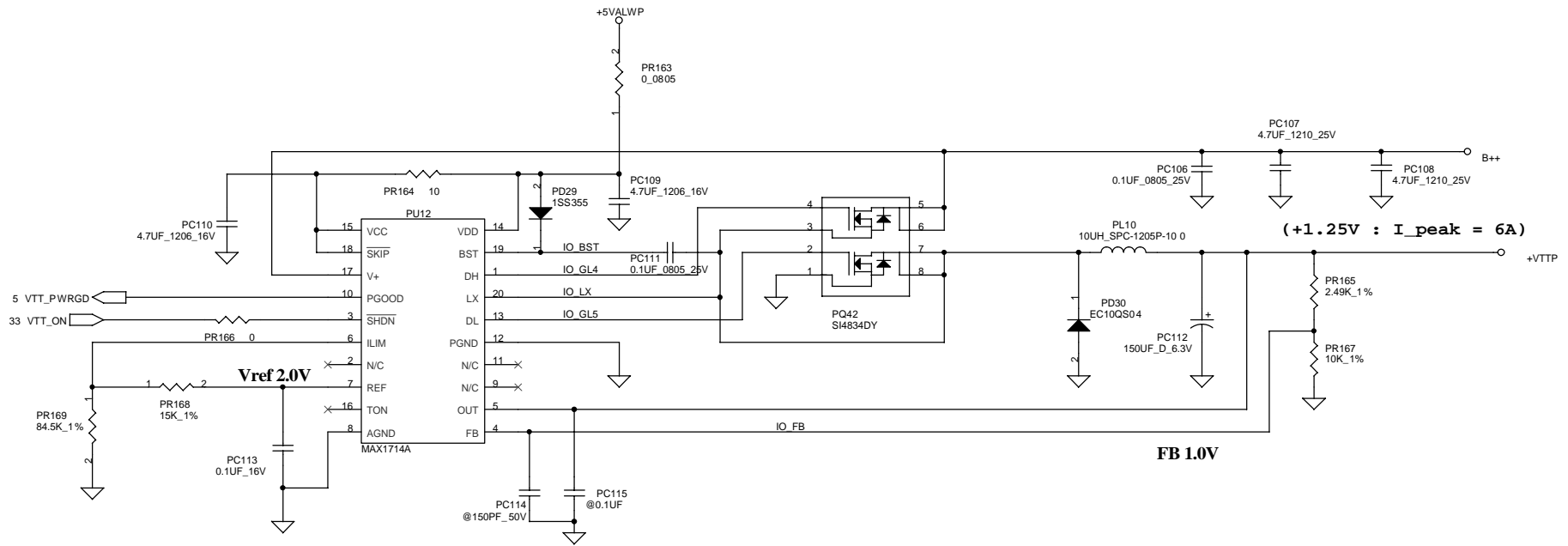
CPU\_COREP OUTPUT\_MODE VOLTS

D3	D2	D1	D0	D4 = 1	D4 = 0
0	0	0	0	0.975	1.75
0	0	0	1	0.950	1.70
0	0	1	0	0.925	1.65
0	0	1	1	0.900	1.60
0	1	0	0	0.875	1.55
0	1	0	1	0.850	1.50
0	1	1	0	0.825	1.45
<b>0</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>0.800</b>	<b>1.40</b>
1	0	0	0	0.775	1.35
1	0	0	1	0.750	1.30
1	0	1	0	0.725	1.25
1	0	1	1	0.700	1.20
<b>1</b>	<b>1</b>	<b>0</b>	<b>0</b>	<b>0.675</b>	<b>1.15</b>
1	1	0	1	0.650	1.10
1	1	1	0	0.625	1.05
1	1	1	1	0.600	1.00

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Title		SCHEMATIC, M/B LA-1121	
Size	B	Document Number	401191 (FOR ATL02 / ACL00)
Date:	星期二, 十一月 27, 2001	Sheet	43 of 87

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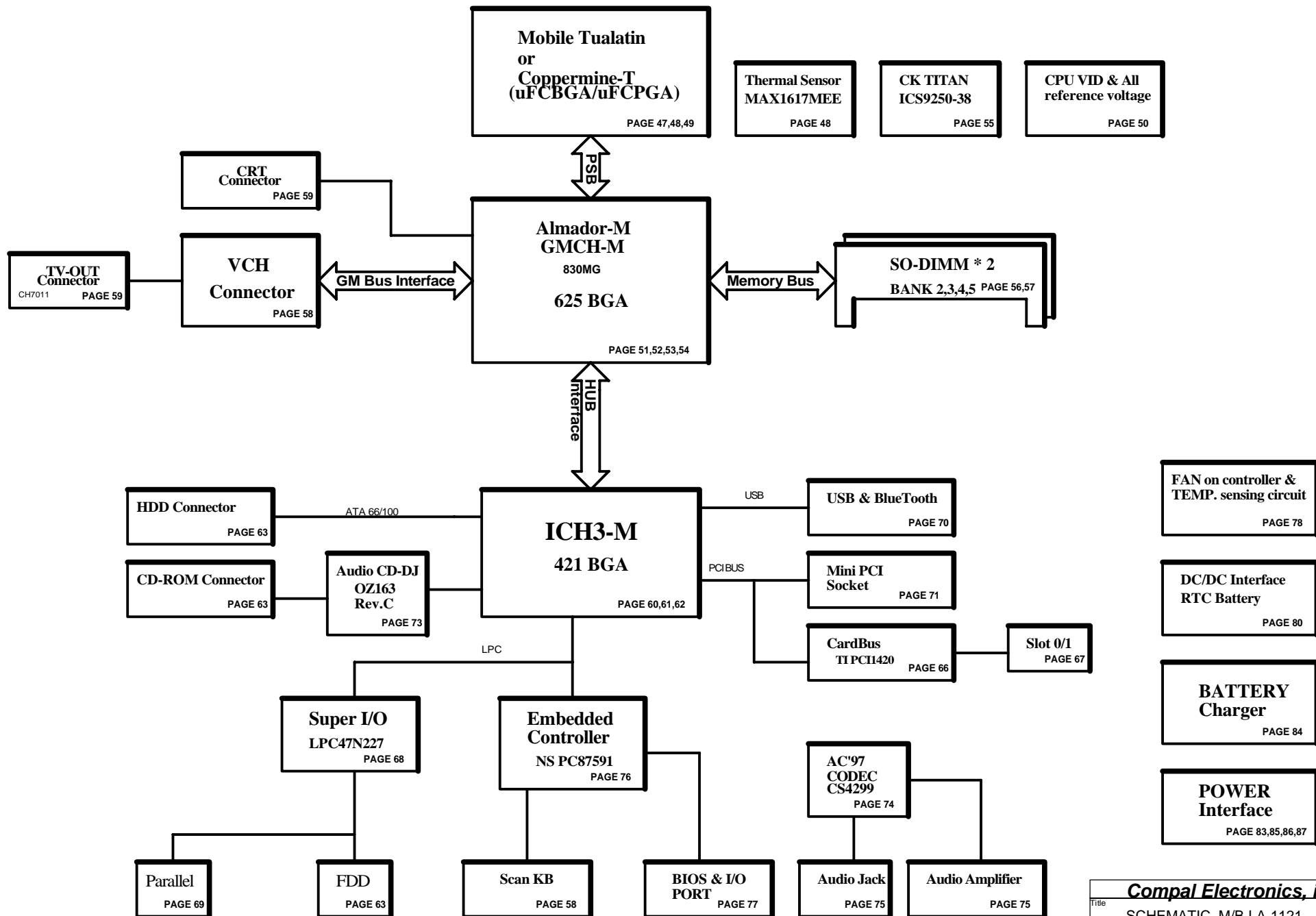
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Title		
SCHEMATIC, M/B LA-1121		
Size	Document Number	Rev
B	401191 (FOR ATL02 / ACL00)	1C
Date:	星期一, 十一月 27, 2001	Sheet 44 of 87

Model Name : ATW01

# BLOCK DIAGRAM

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Title	SCHEMATIC, M/B LA-1121	
Size	Document Number	Rev
Custom	401191 (FOR ATW01)	1C
Date:	星期一, 十一月 27, 2001	Sheet 45 of 87

## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_H_CORE	Core voltage for CPU	ON	OFF	OFF
+VTT	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+1.8V	1.8V power rail	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12VS	12V switched power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA/PIRQB
Mini-PCI	AD18	1/4	PIRQC/PIRQD

## EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
(24C04)	1011 000Xb

## EC SM Bus2 address

Device	Address
MAX1617MEE	1001 110X b
OZ163	0011 0100 b
Smart Battery	0001 011X b
Docking	0011 011X b
DOT Board	XXXX XXXXb

## ICH3-M SM Bus address

Device	Address
Clock Generator ( ICS9238-50)	1101 0000
SDRAM Select ( 74HC4052 )	1010 0000
CPU Voltage VID select ( F3565 )	0110 111Xb

## PIR

REV 0.2

Date	Page	Description
9/6	12	

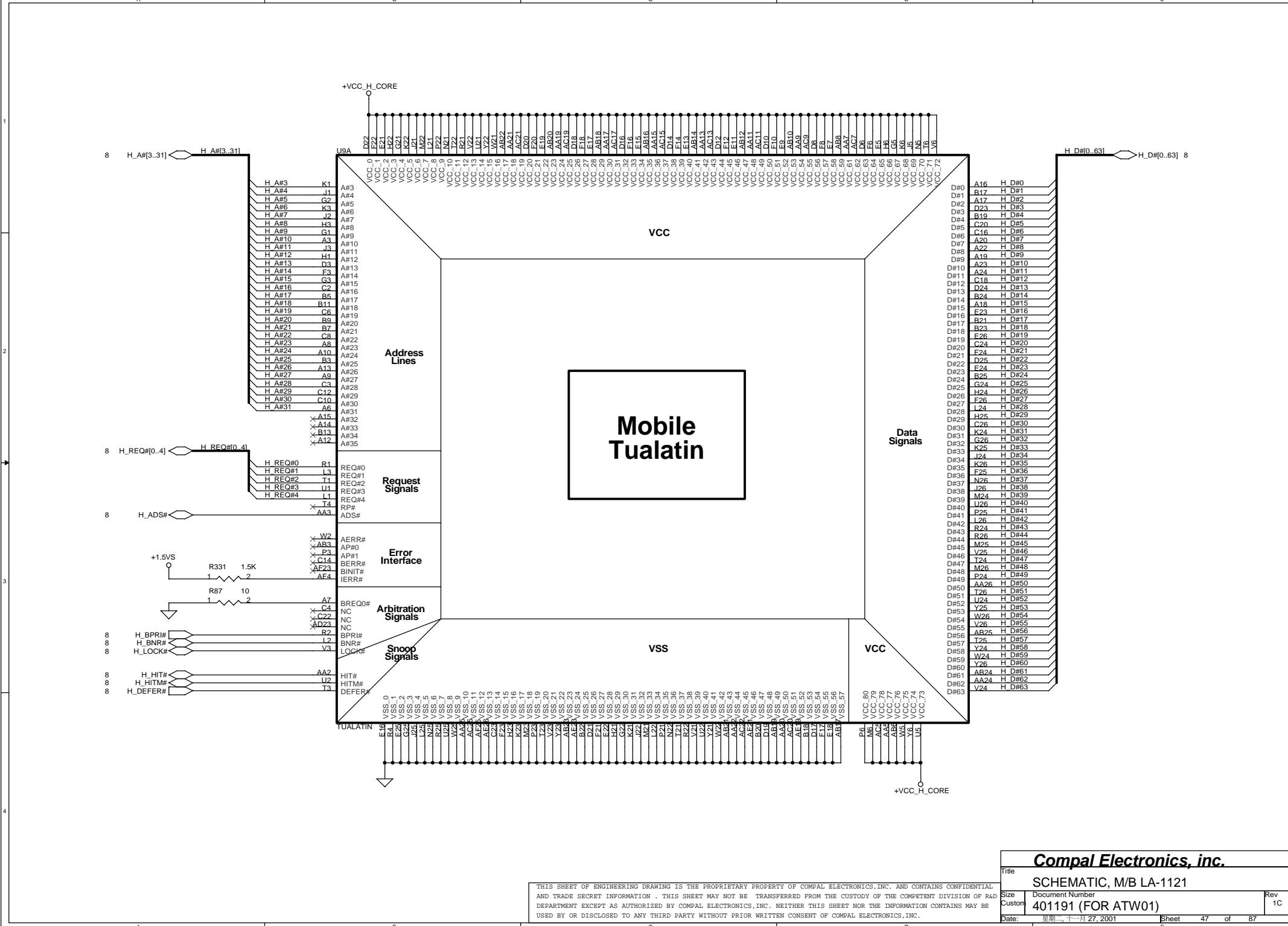
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Title  
SCHEMATIC, M/B LA-1121

Size Custom Document Number  
401191 (FOR ATW01)

Date: 星期 一, 十一月 27, 2001

Sheet 46 of 87 Rev 1C



**Compal Electronics, inc.**

Title: SCHEMATIC, M/B LA-1121

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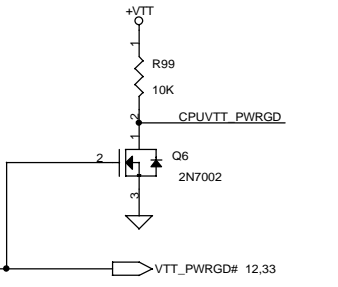
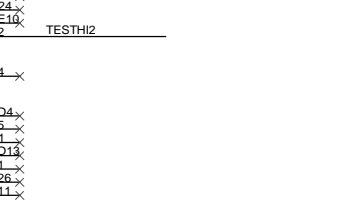
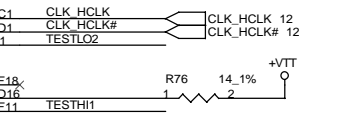
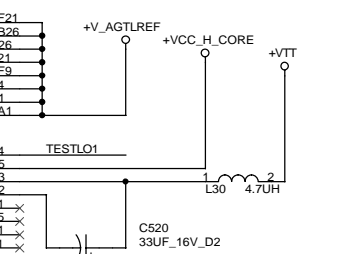
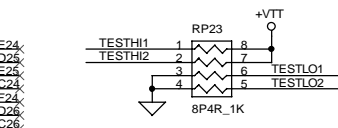
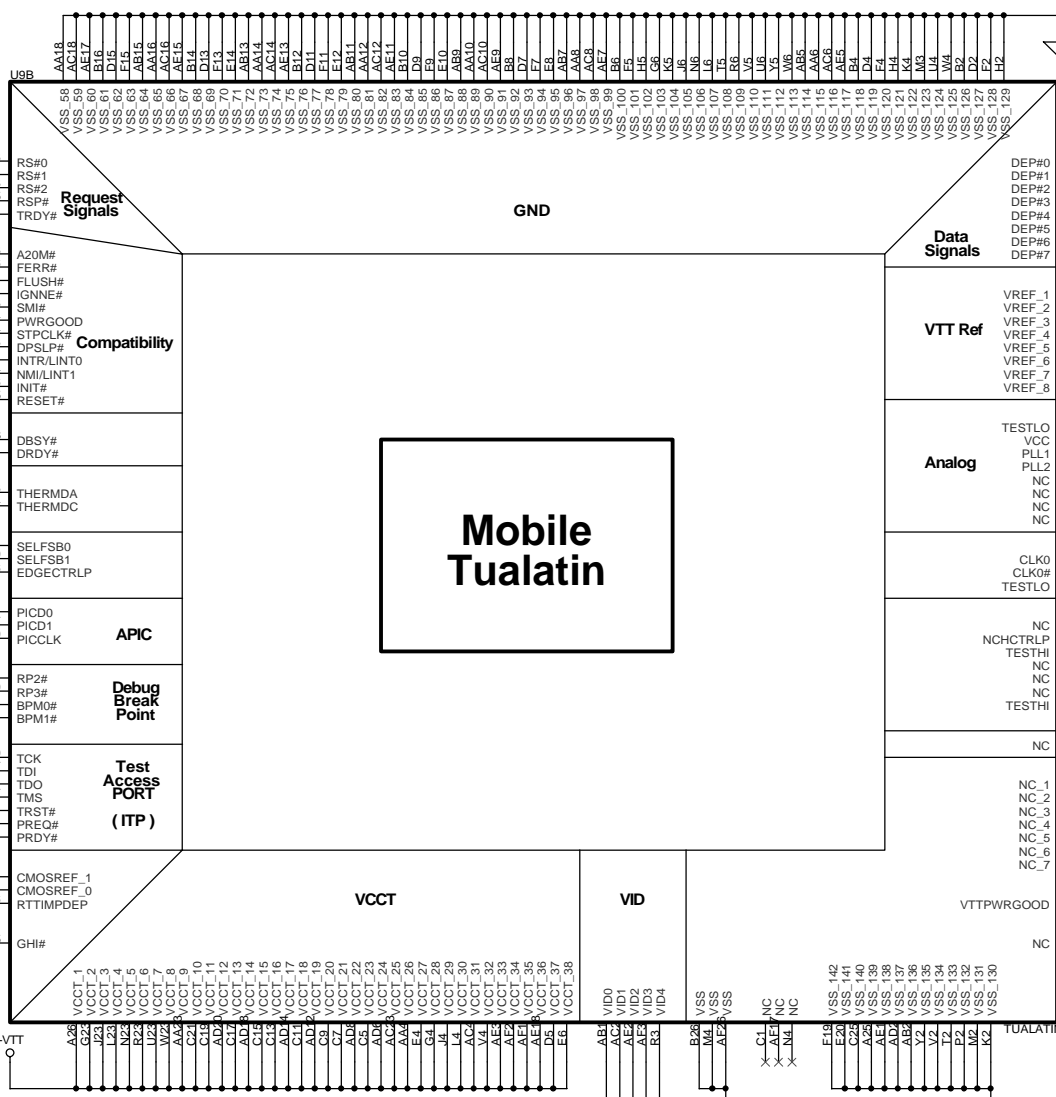
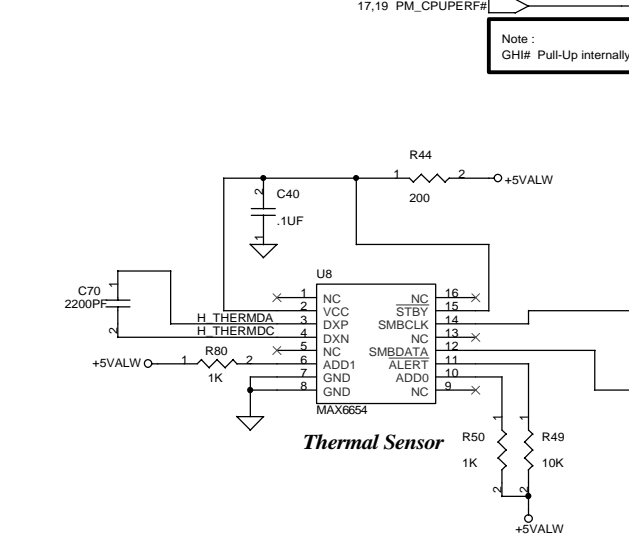
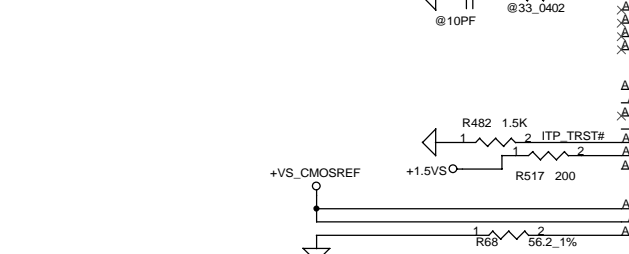
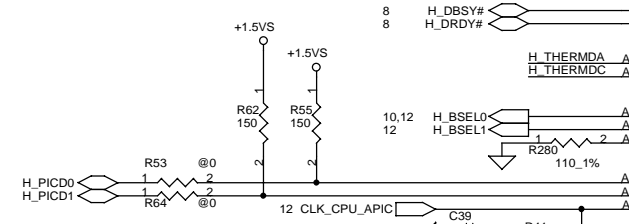
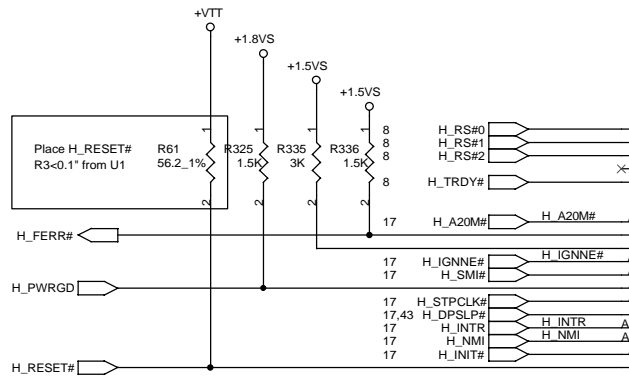
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Date: 星期一, 十一月 27, 2001

Sheet 47 of 87

Rev 1C

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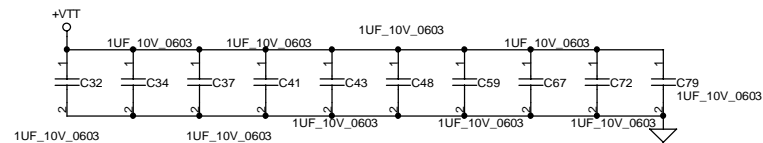
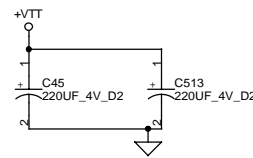
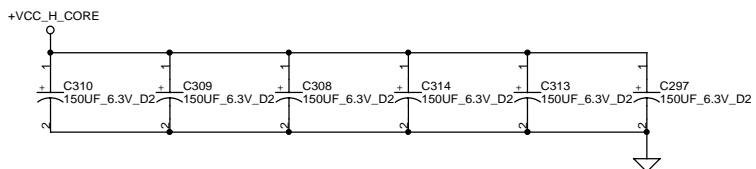
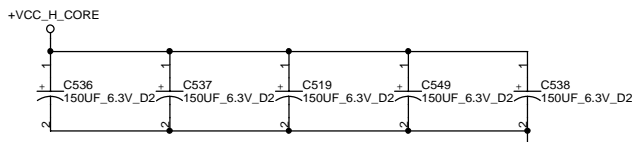
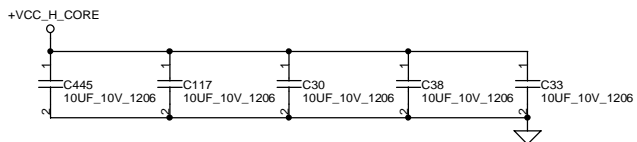
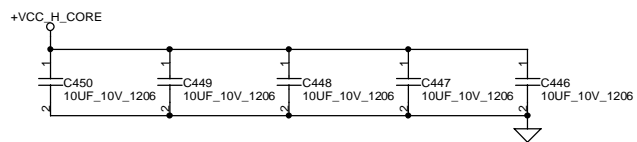
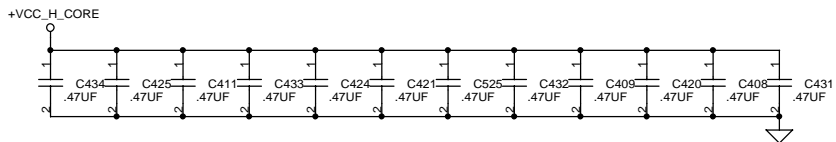
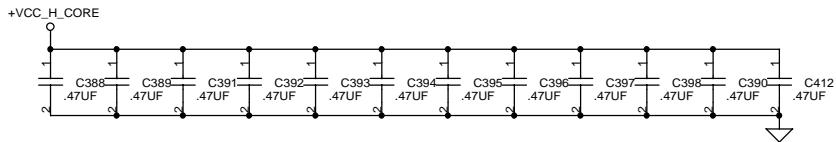


**Layout note :**

Place close to CPU, Use 2-3 vias per PAD.  
 Place .47uF caps underneath balls on solder side.  
 Place 10uF caps on the peripheral near balls.  
 Use 2-3 vias per PAD.

**Layout note :**

Place close to CPU,  
 Use 2 vias per PAD.



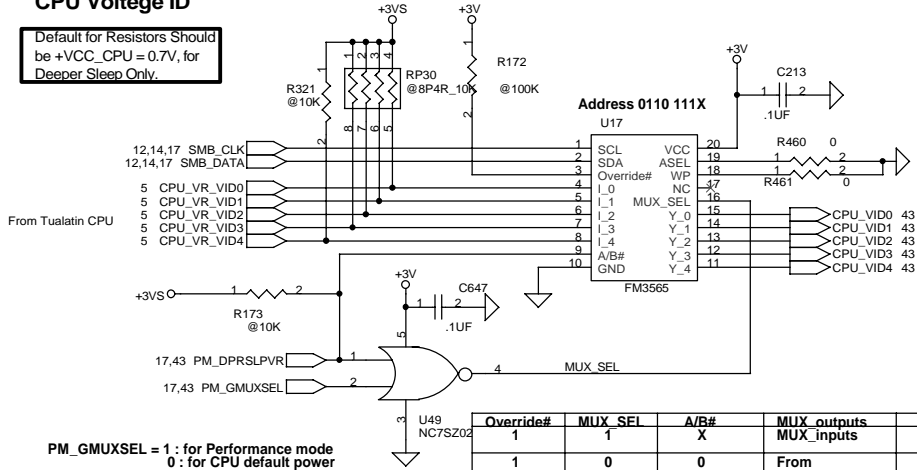
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Title	SCHMATIC, M/B LA-1121
Size	Document Number
Custom	401191 (FOR ATW01)
Date:	Rev 1C
星期 一, 十一月 27, 2001	Sheet 49 of 87



### CPU Voltage ID

Default for Resistors Should be +VCC\_CPU = 0.7V, for Deeper Sleep Only.



PM\_GMUXSEL = 1 : for Performance mode  
0 : for CPU default power

PM\_DPRSLPVR = 1: for Deeper Sleep mode  
0: for Performance mode

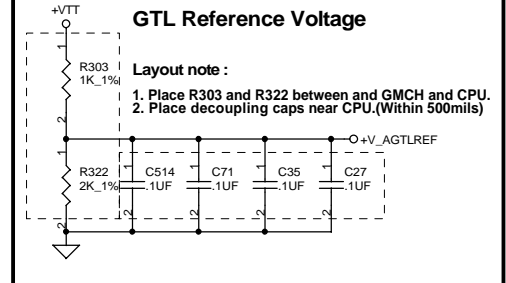
Override#	MUX_SEL	A/B#	MUX_outputs MUX_inputs	Mode
1	1	X	From Non-volatile register(SOPRB)	Performance
1	0	1	From Non-volatile register(SOPRA)	Deeper sleep

### Tualatin

D4	D3	D2	D1	D0	CPU_Core(V)	ES(before MP)
0	0	1	0	1	1.50V (Performance)	
0	1	1	0	0	1.15V (Battery)	
1	0	1	0	1	0.85V (Deeper Sleep)	

D4	D3	D2	D1	D0	CPU_Core(V)	QS( MP)
0	0	1	1	1	1.40V (Performance)	
0	1	1	0	0	1.15V (Battery)	
1	0	1	0	1	0.85V (Deeper Sleep)	

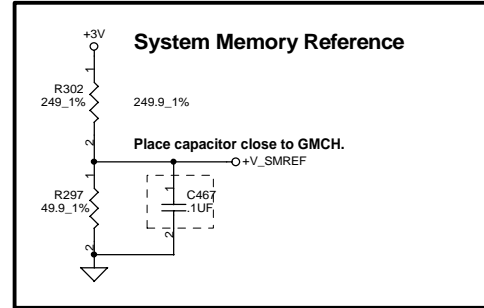
### GTL Reference Voltage



#### Layout note :

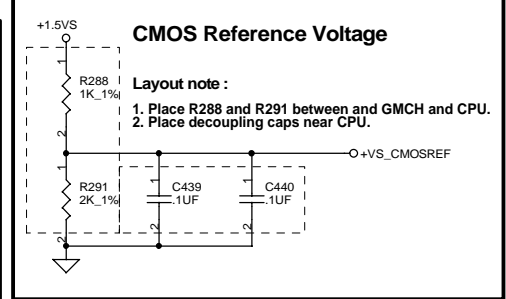
1. Place R303 and R322 between and GMCH and CPU.
2. Place decoupling caps near CPU.(Within 500mils)

### System Memory Reference



#### Place capacitor close to GMCH.

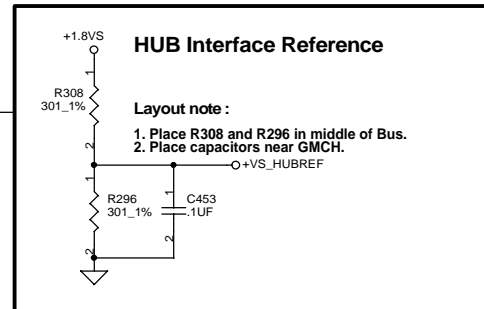
### CMOS Reference Voltage



#### Layout note :

1. Place R288 and R291 between and GMCH and CPU.
2. Place decoupling caps near CPU.

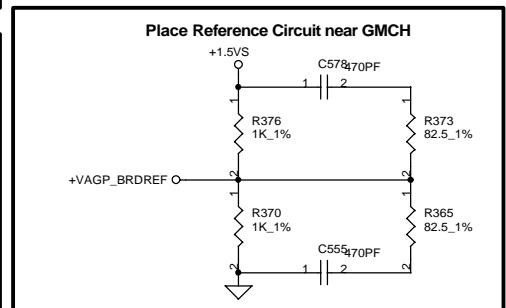
### HUB Interface Reference



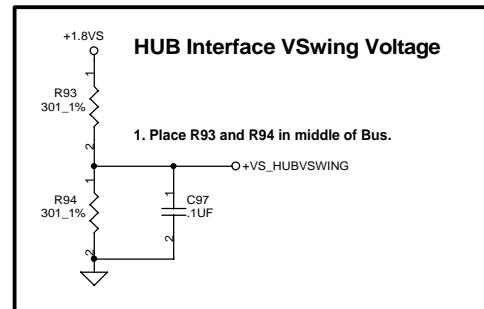
#### Layout note :

1. Place R308 and R296 in middle of Bus.
2. Place capacitors near GMCH.

### Place Reference Circuit near GMCH

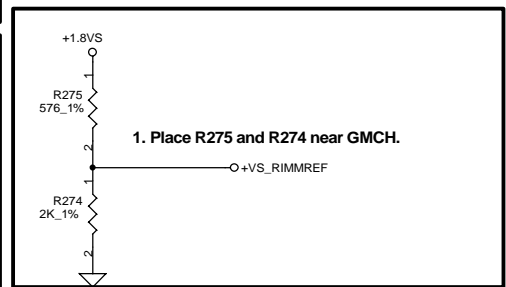


### HUB Interface VSwing Voltage



#### 1. Place R93 and R94 in middle of Bus.

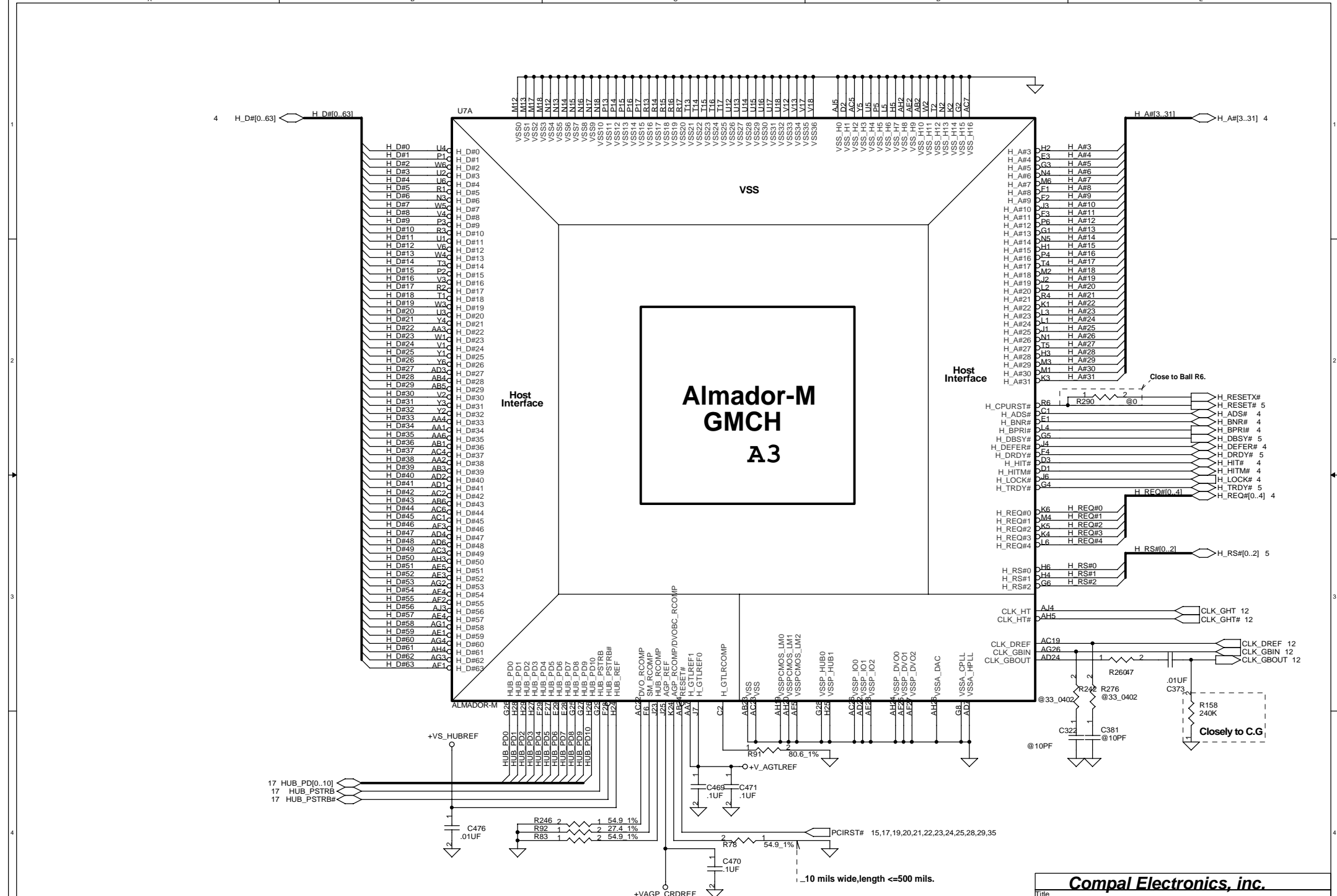
### 1. Place R275 and R274 near GMCH.



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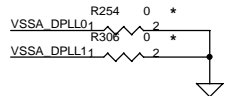
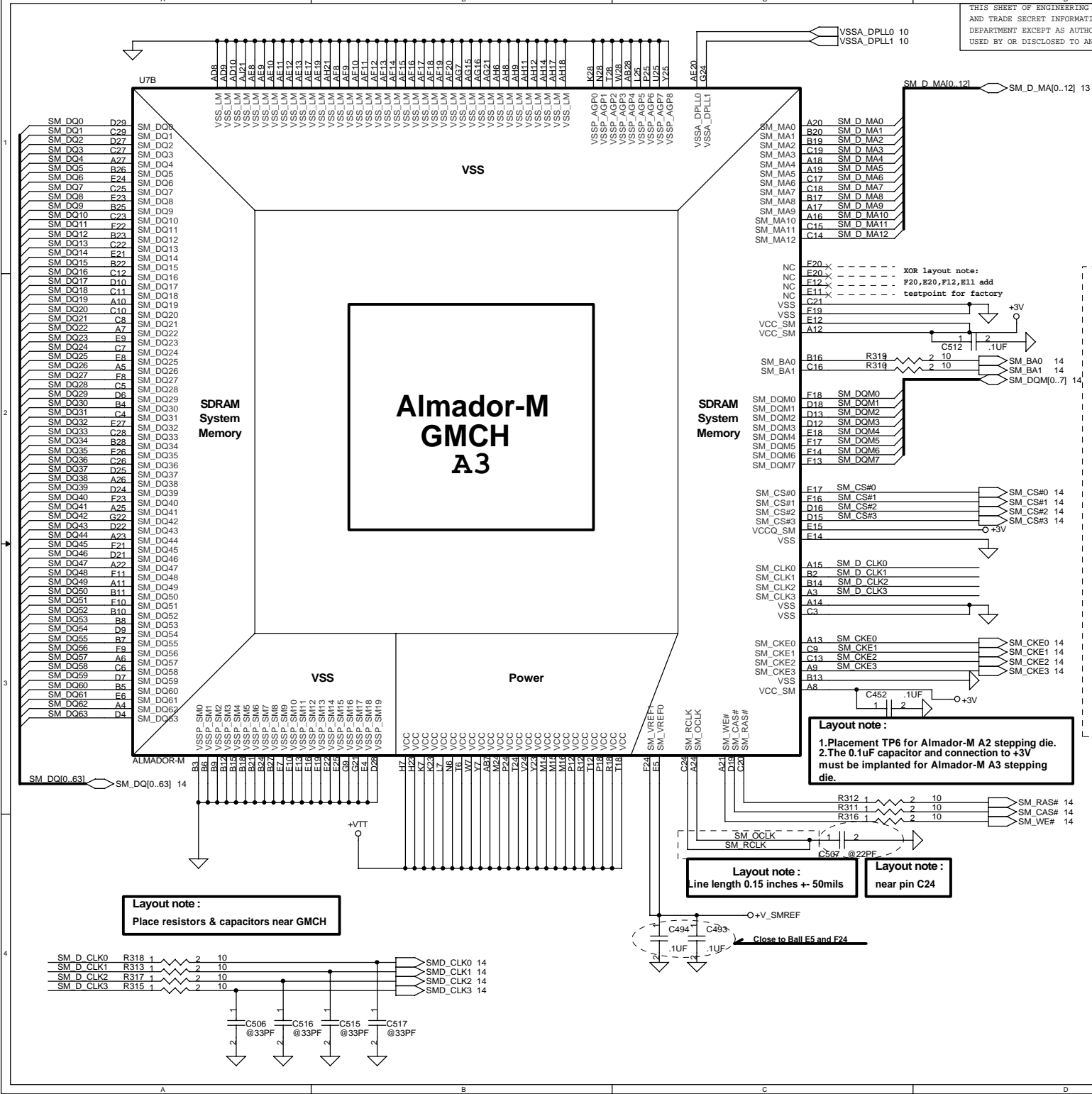
Title	SCHEMATIC, M/B LA-1121	
Size	Document Number	Rev
Custom	401191 (FOR ATW01)	1C
Date:	星期一, 十一月 27, 2001	Sheet 50 of 87

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SCHEMATIC, M/B LA-1121		
Size	Document Number	Rev
Custom	401191 (FOR ATW01)	1C
Date:	星期一, 十一月 27, 2001	Sheet 51 of 87



XOR layout note:  
 F20, F12, E11, E11 add  
 testpoint for factory

For Almador-M A3 stepping requirement.  
 The table below provides a summary of the ballout changes to the Almador-M chip

Table 4-1 Ballout Changes

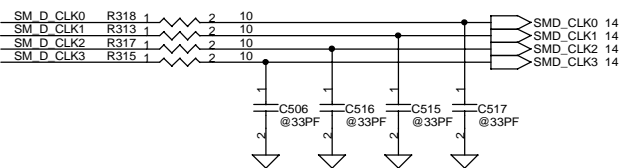
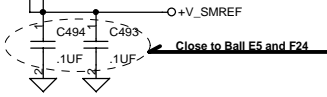
Ball#	New Signal Name	Old Signal Name
A8	VCC_SM	SM_CKES
A12	VCC_SM	SM_ECC7
E12	VCC_SM	SM_ECC8
G10	VCC_SM	VCCQ_SM
F7	VCCQ_SM	VCC_SM
G19	VCCQ_SM	VCC_SM
E15	VCCQ_SM	SM_CS4
F15	VCCQ_SM	VCC_SM
A14	VSS	SM_CLK4
B13	VSS	SM_CKES
C3	VSS	SM_CLK5
C21	VSS	SM_ECC4
E14	VSS	SM_CS5
F19	VSS	SM_ECC5
E11	NC	SM_ECC3
E20	NC	SM_ECC1
F12	NC	SM_ECC2
F20	NC	SM_ECC0

Layout note:  
 1. Placement TP6 for Almador-M A2 stepping die.  
 2. The 0.1uF capacitor and connection to +3V must be implanted for Almador-M A3 stepping die.

Layout note:  
 Line length 0.15 inches +/- 50mils

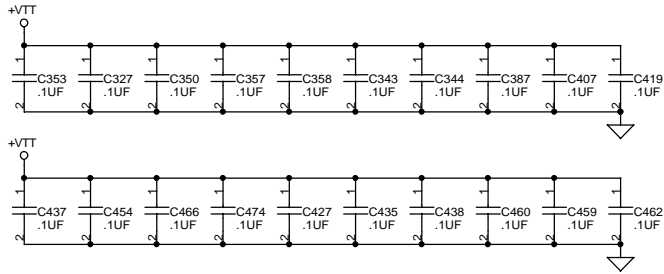
Layout note:  
 near pin C24

Layout note:  
 Place resistors & capacitors near GMCH

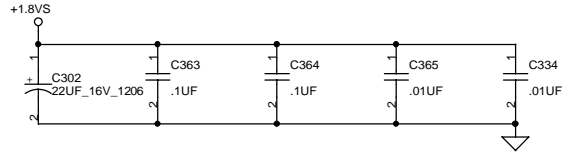




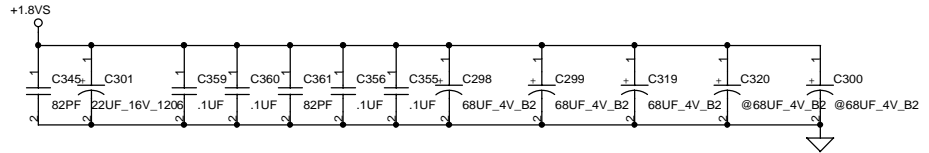
**Layout note :**  
Distribute as close as possible to GMCH Processor Quadrant .



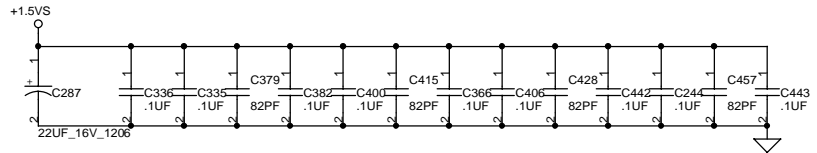
**Layout note :**  
Distribute as close as possible to VCCPCMOS\_LM .



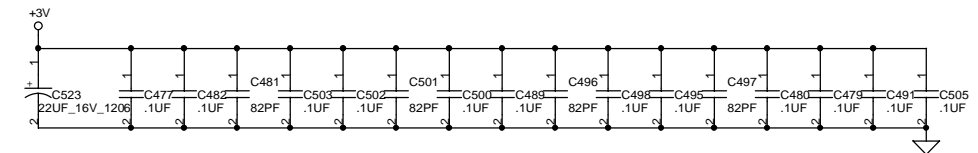
**Layout note :**  
Distribute as close as possible to GMCH Local Memory Quadrant .



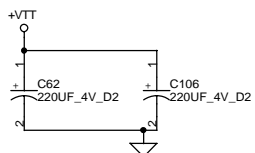
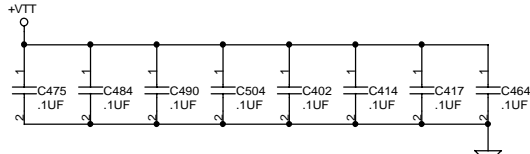
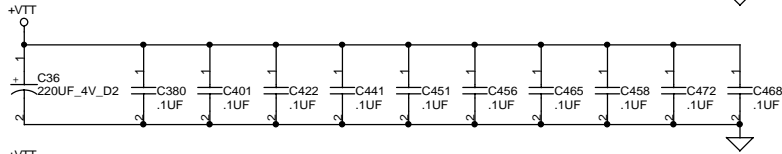
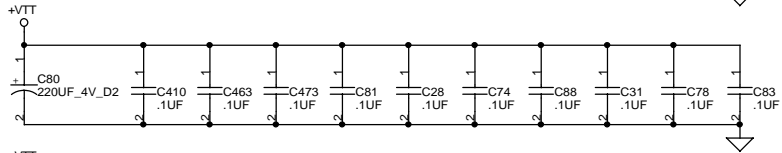
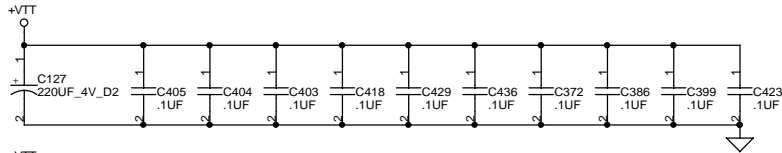
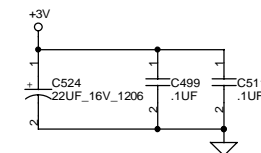
**Layout note :**  
Distribute as close as possible to GMCH AGP/DVO Quadrant .



**Layout note :**  
Distribute as close as possible to GMCH System Memory Quadrant .

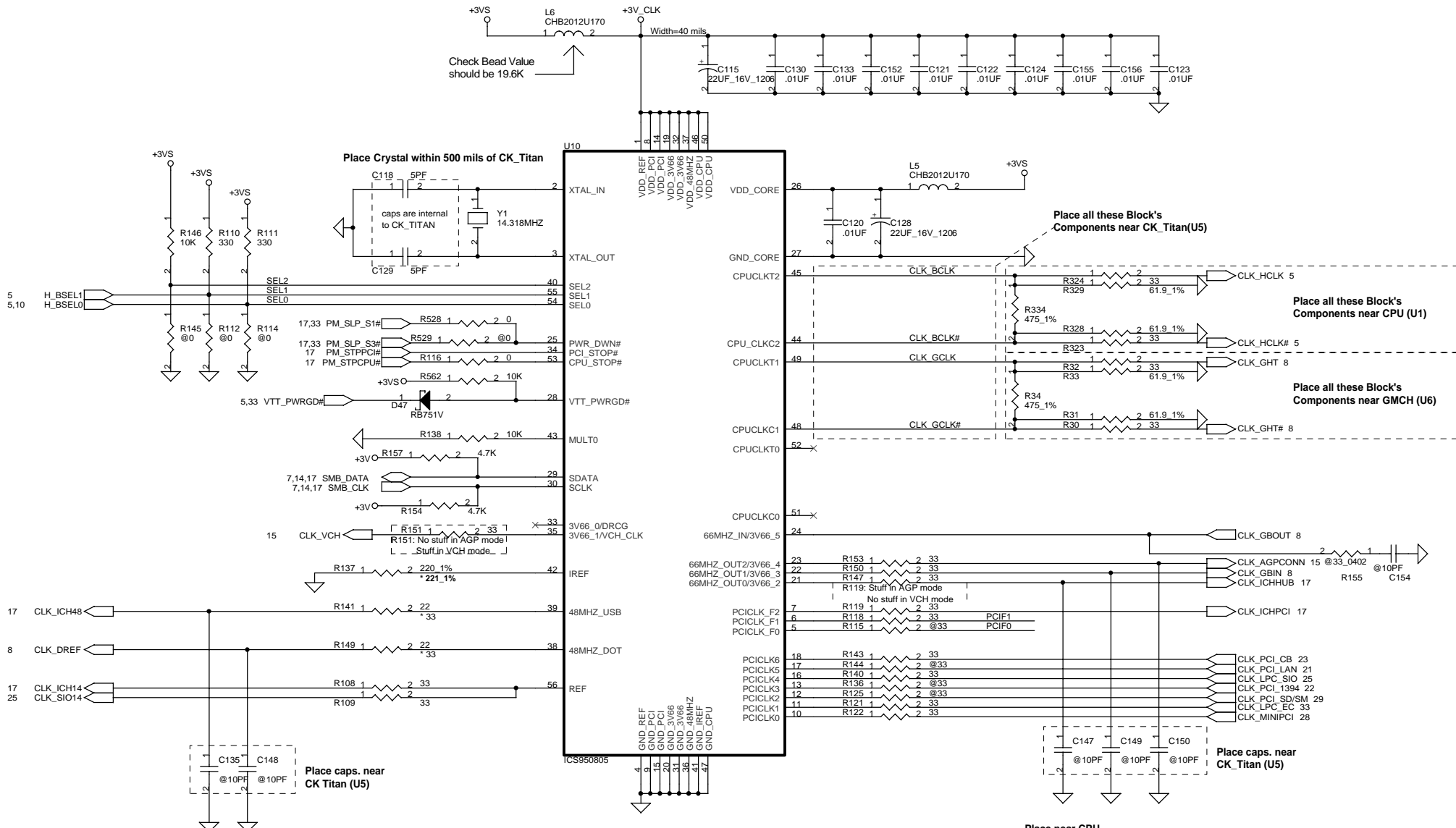


**Layout note :**  
Distribute as close as possible to IO Quadrant .



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Title	SCHEMATIC, M/B LA-1121	
Size	Document Number	Rev
Custom	401191 (FOR ATW01)	1C
Date:	星期一, 十一月 27, 2001	Sheet 54 of 87



SEL2	SEL1	SEL0	CPUCLKC0..2	CPUCLKT0..2
1	0	0	66.67	66.67
1	0	1	100.00	100.00
1	1	0	200.00	200.00
1	1	1	133.33	133.33

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**Size** Custom

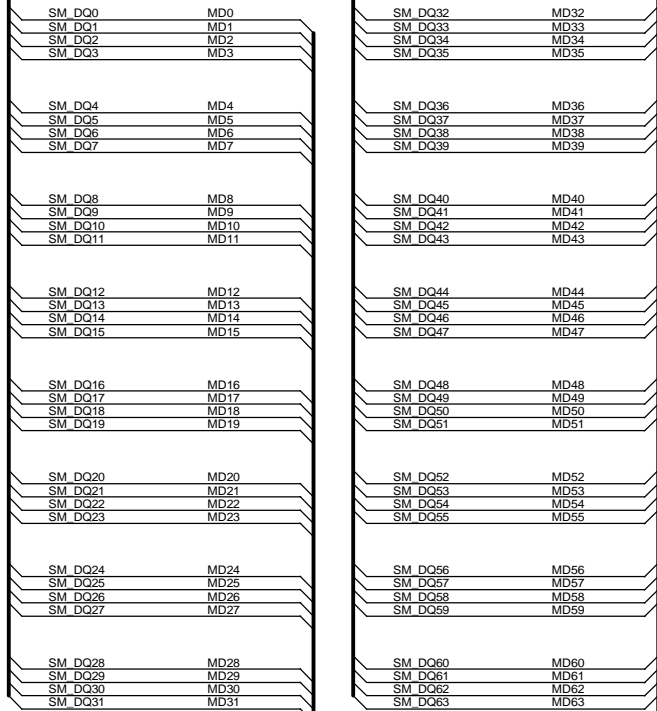
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**Date:** 星期一, 十一月 27, 2001

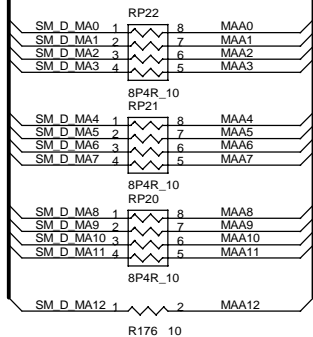
**Rev** 1C

**Sheet** 55 **of** 87

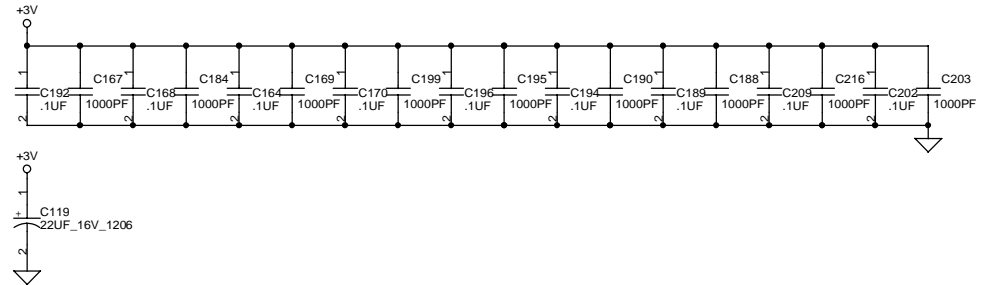
9,14 SM\_DQ[0..63] MD[0..63] 9,14



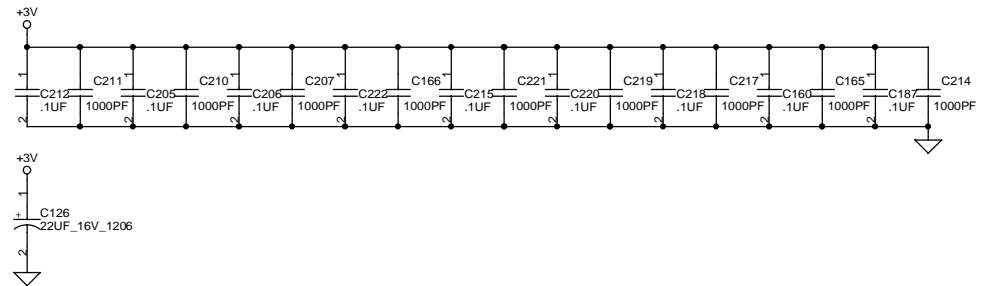
9 SM\_D\_MA[0..12] MAA[0..12] 14



**Layout note :**  
 One .1uF cap per power pin .  
 Place each cap close to SODIMM(DIMM 0) pin .



**Layout note :**  
 One .1uF cap per power pin .  
 Place each cap close to SODIMM(DIMM 1) pin .



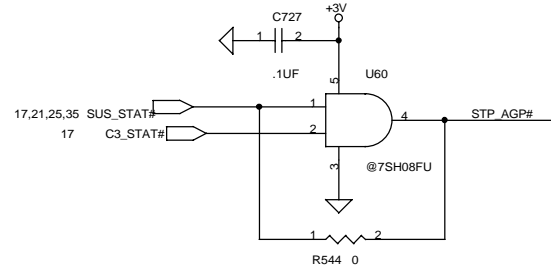
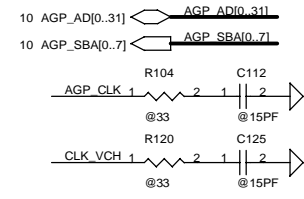
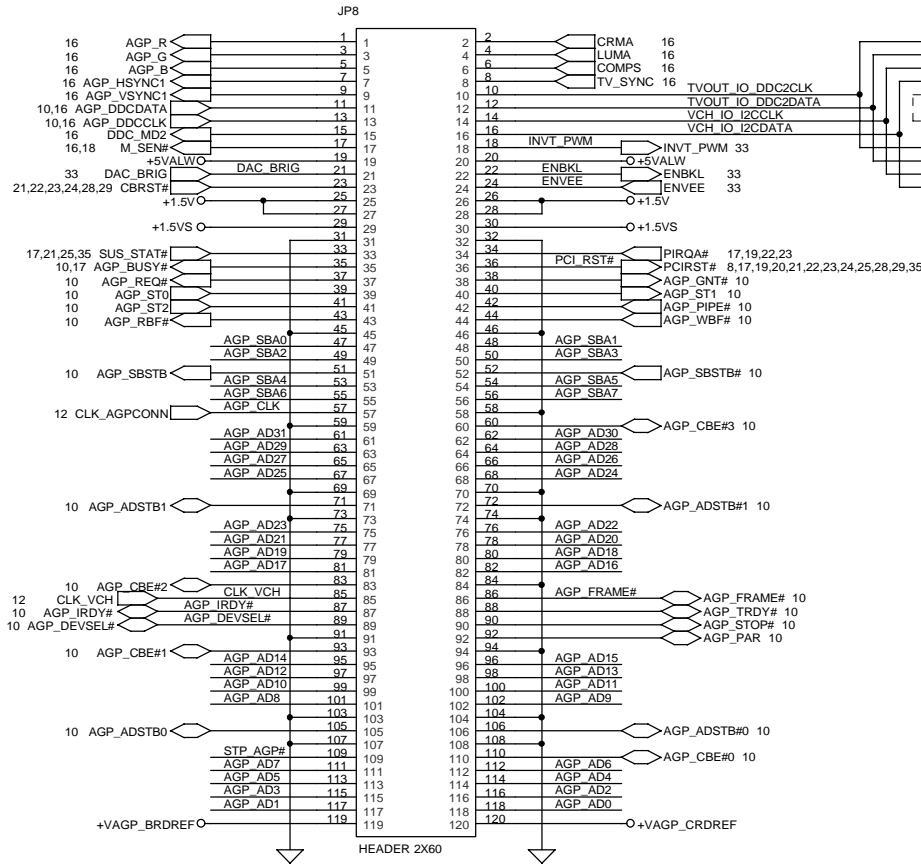
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Title	SCHEMATIC, M/B LA-1121	
Size	Document Number	Rev
Custom	401191 (FOR ATW01)	1C
Date:	星期一, 十一月 27, 2001	Sheet 56 of 87

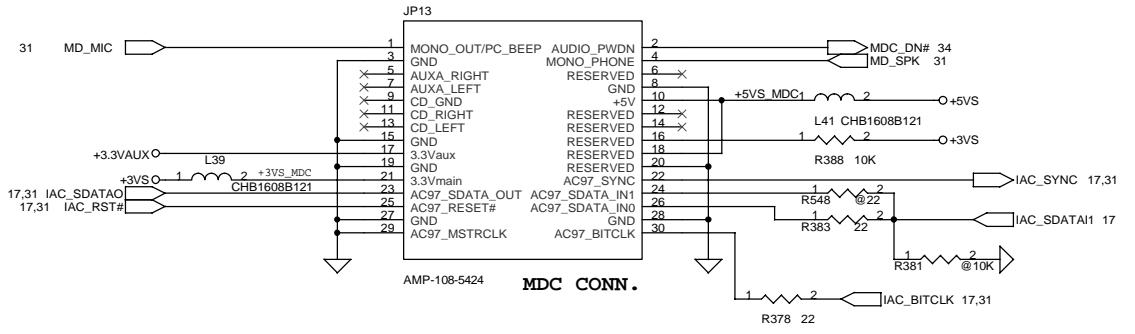
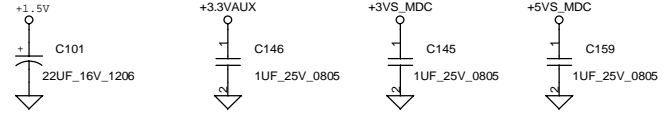
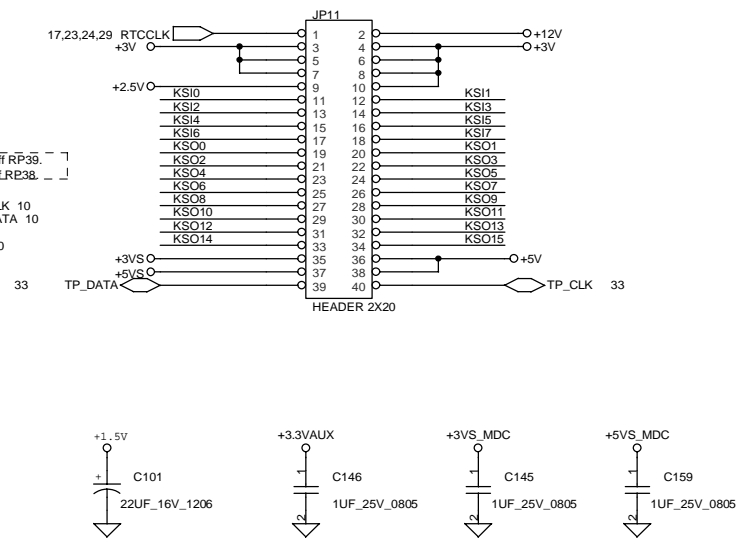




**AGP CONN.**



**Int. Keyboard CONN.**



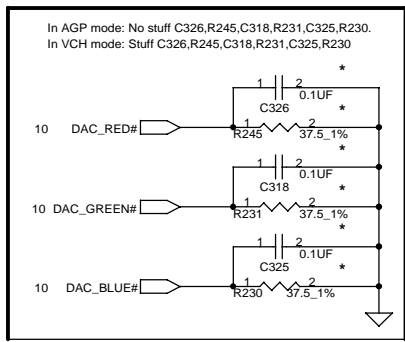
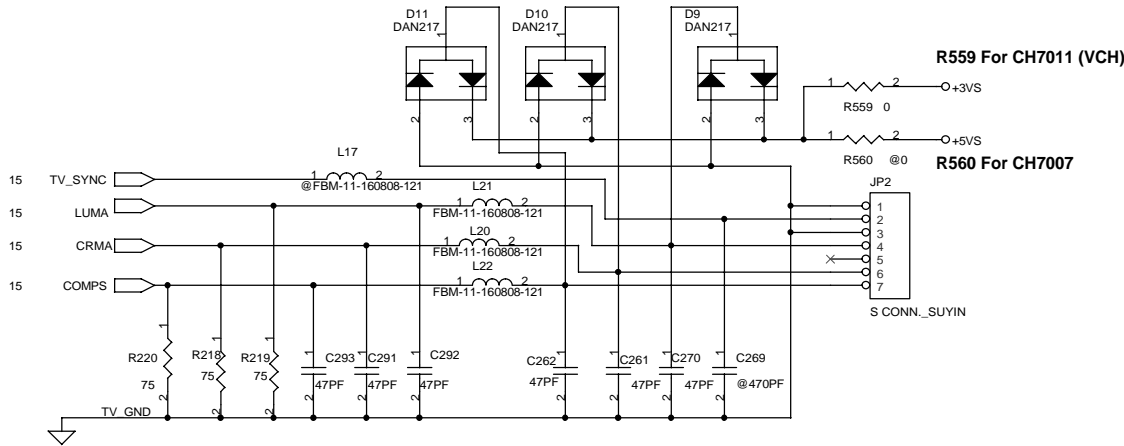
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**SCHMATIC, M/B LA-1121**

Size B Document Number 401191 (FOR ATW01) Rev 1C  
Date: 星期二, 十一月 27, 2001 Sheet 58 of 87

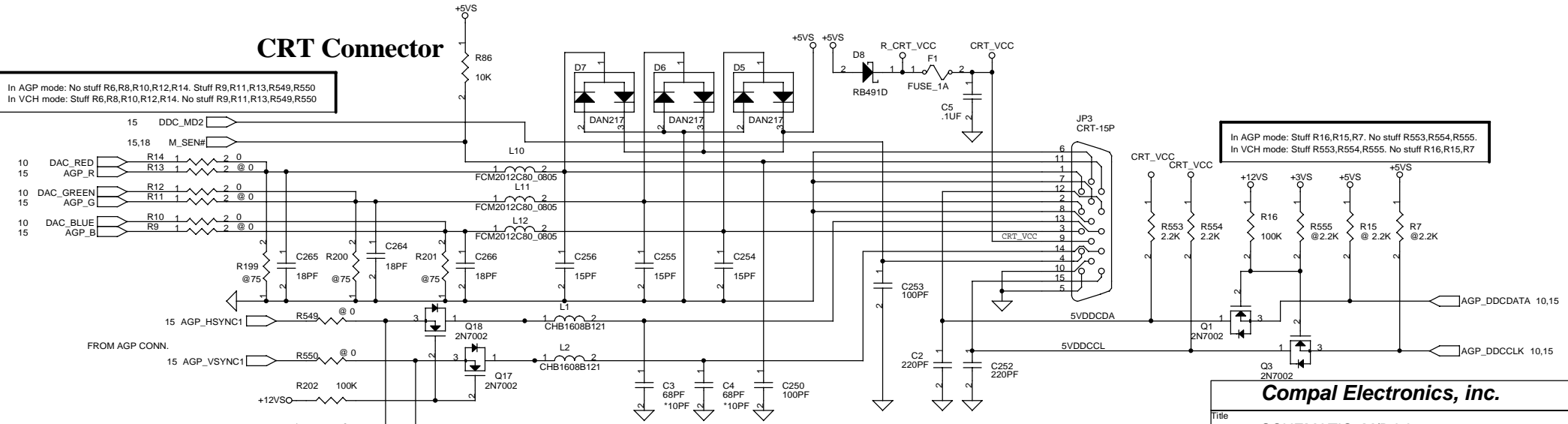
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# TV\_OUT CONN.



# CRT Connector

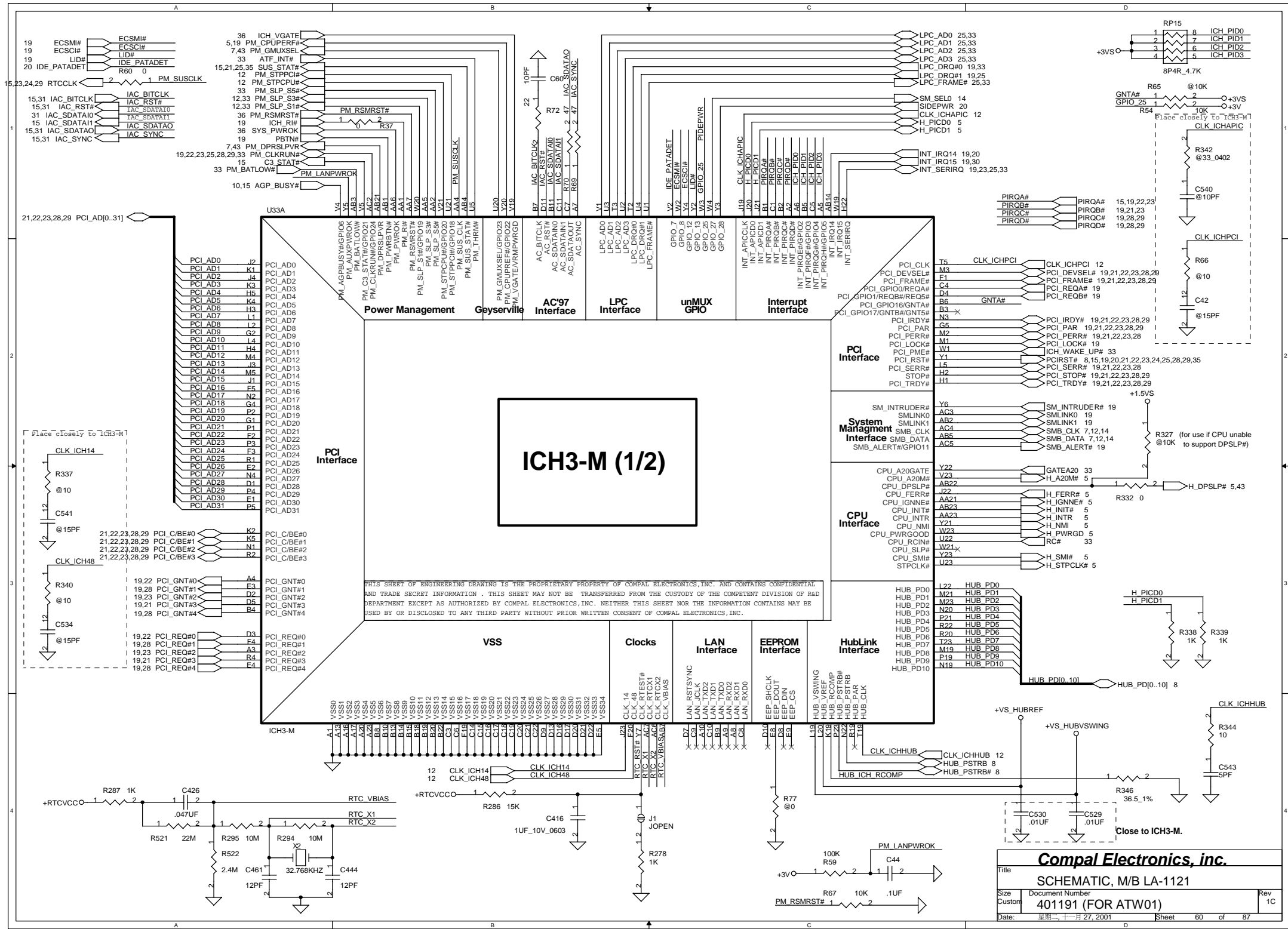
In AGP mode: No stuff R6,R8,R10,R12,R14. Stuff R9,R11,R13,R549,R550  
In VCH mode: Stuff R6,R8,R10,R12,R14. No stuff R9,R11,R13,R549,R550

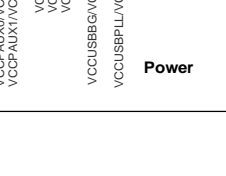
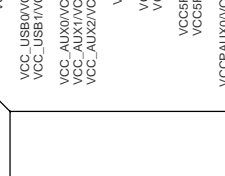
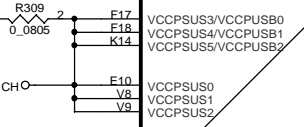
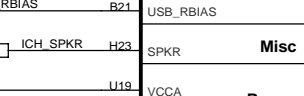
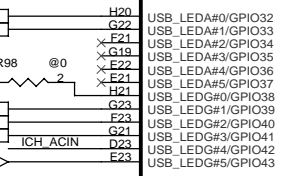
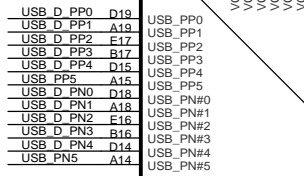
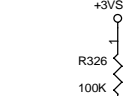
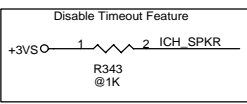
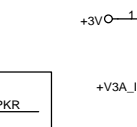
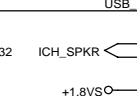
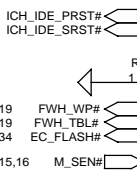
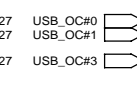
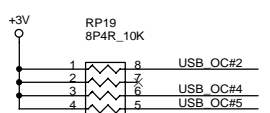
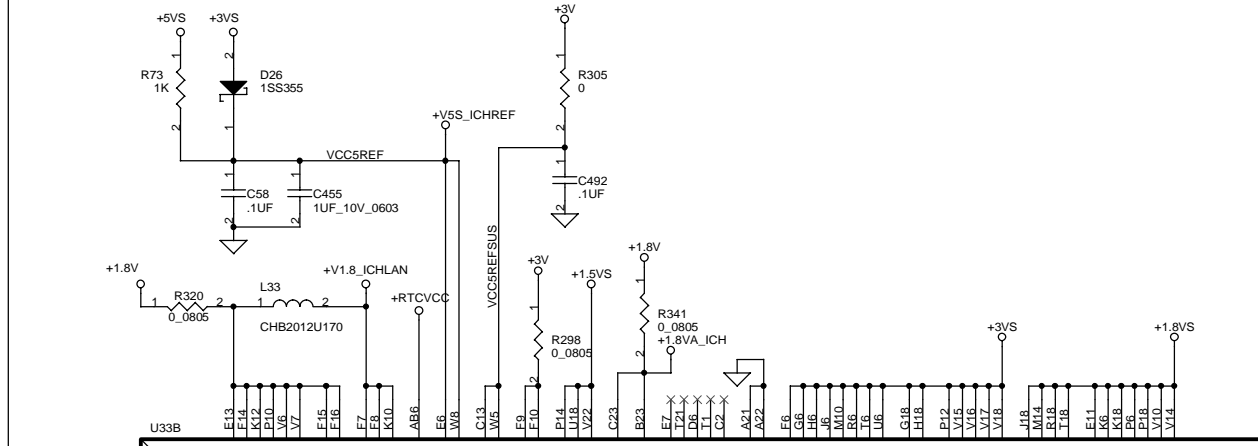
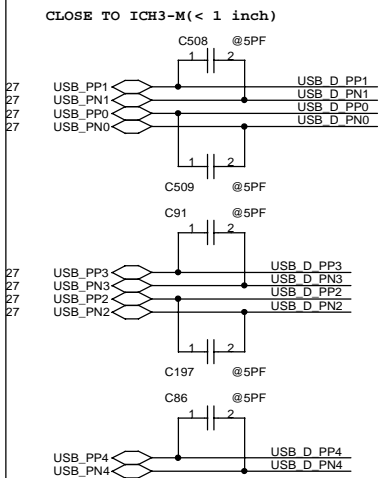


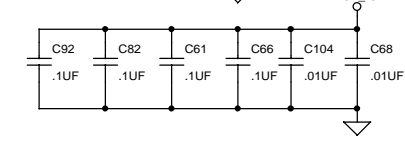
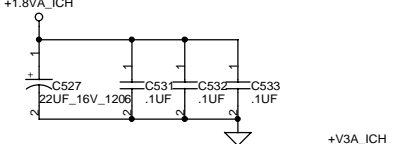
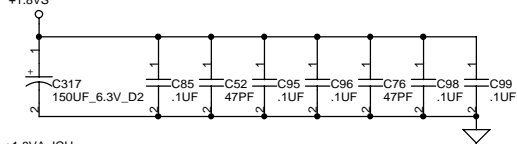
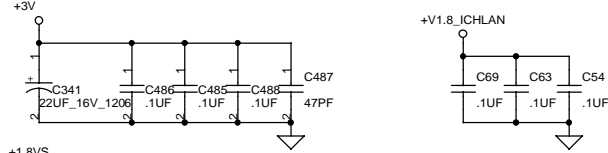
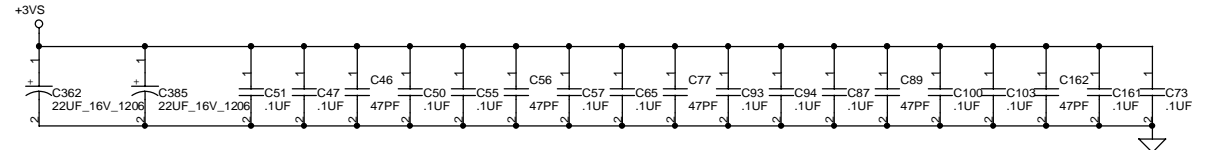
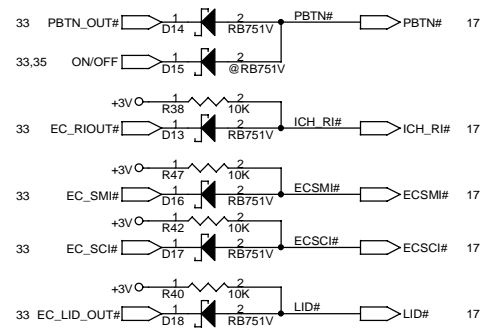
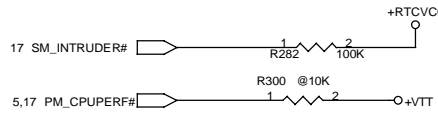
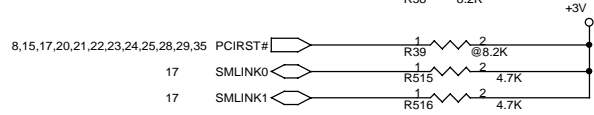
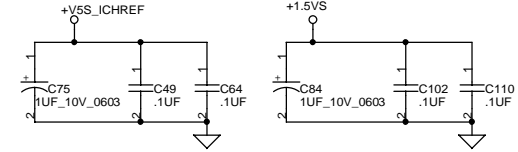
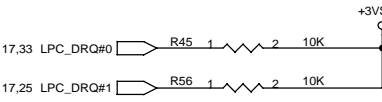
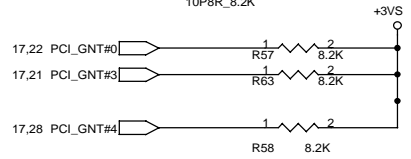
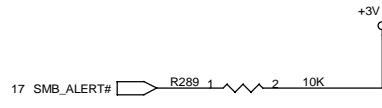
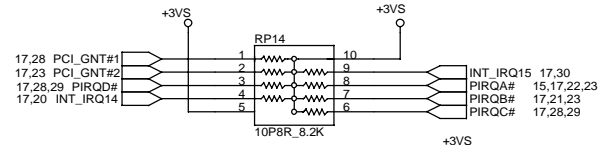
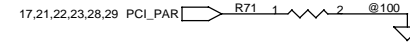
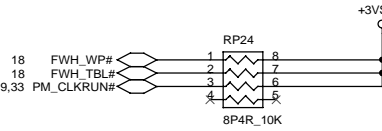
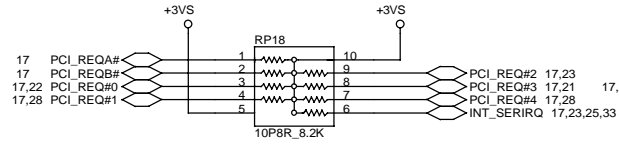
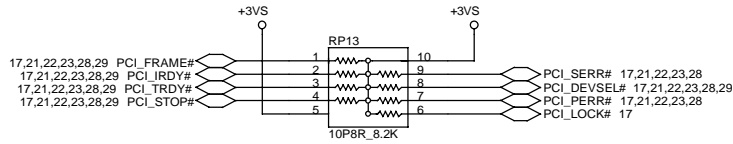
In AGP mode: Stuff R16,R15,R7. No stuff R553,R554,R555.  
In VCH mode: Stuff R553,R554,R555. No stuff R16,R15,R7

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Title	SCHEMATIC, M/B LA-1121	
Size	Custom	Document Number
Date	2001年十一月二十七日	401191 (FOR ATW01)
Sheet	59	of 87
Rev	1C	



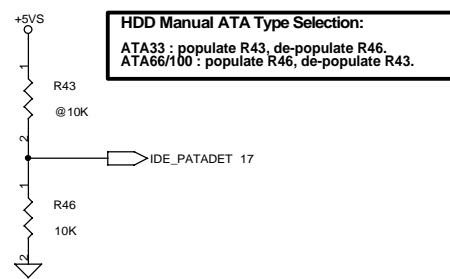
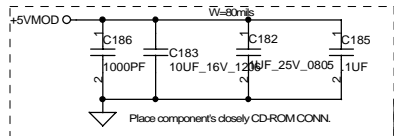
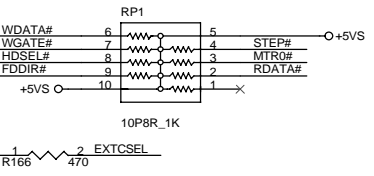
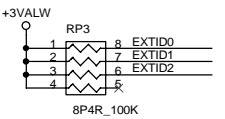
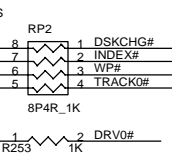
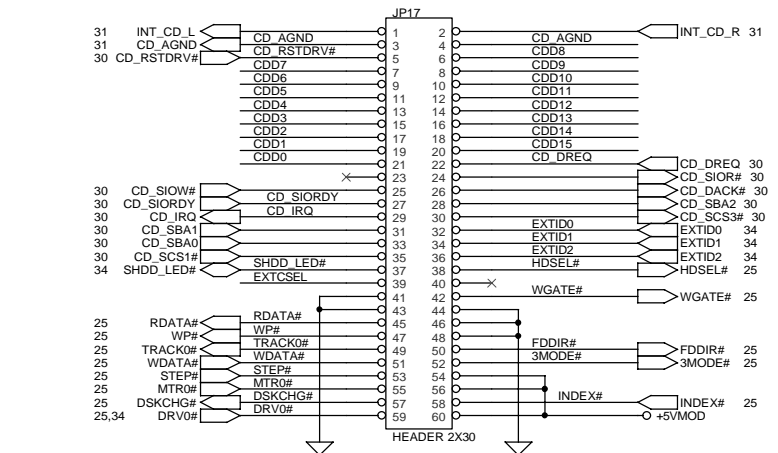
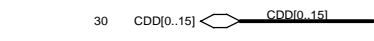
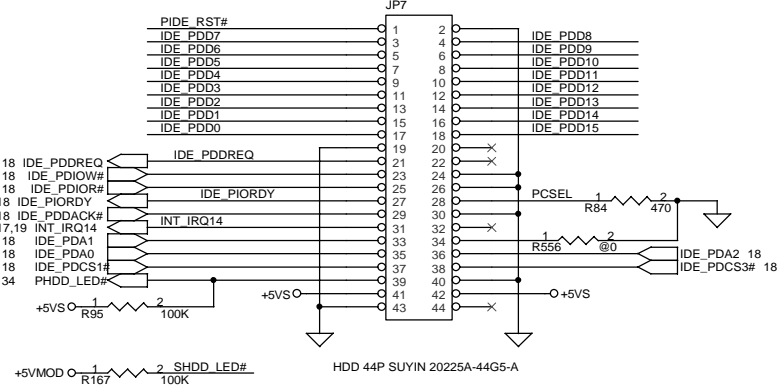
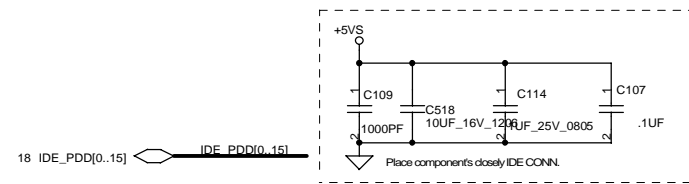




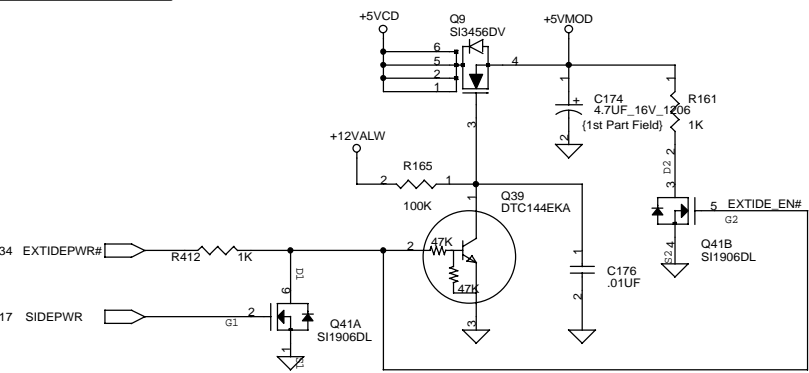
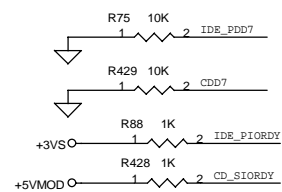
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Title	SCHEMATIC, M/B LA-1121	
Size	Document Number	Rev
Custom	401191 (FOR ATW01)	1C
Date:	星期一, 十一月 27, 2001	Sheet 62 of 87

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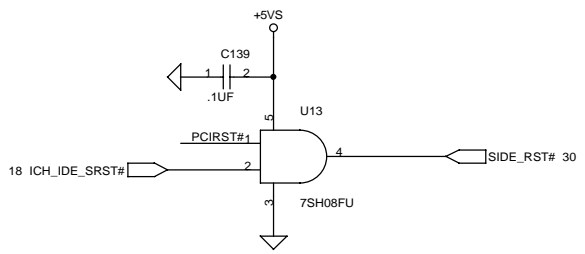
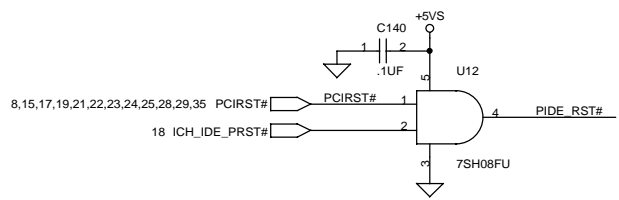
# IDE, CD-ROM Module CONN.



**HDD Manual ATA Type Selection:**  
 ATA33 : populate R43, de-populate R46.  
 ATA66/100 : populate R46, de-populate R43.



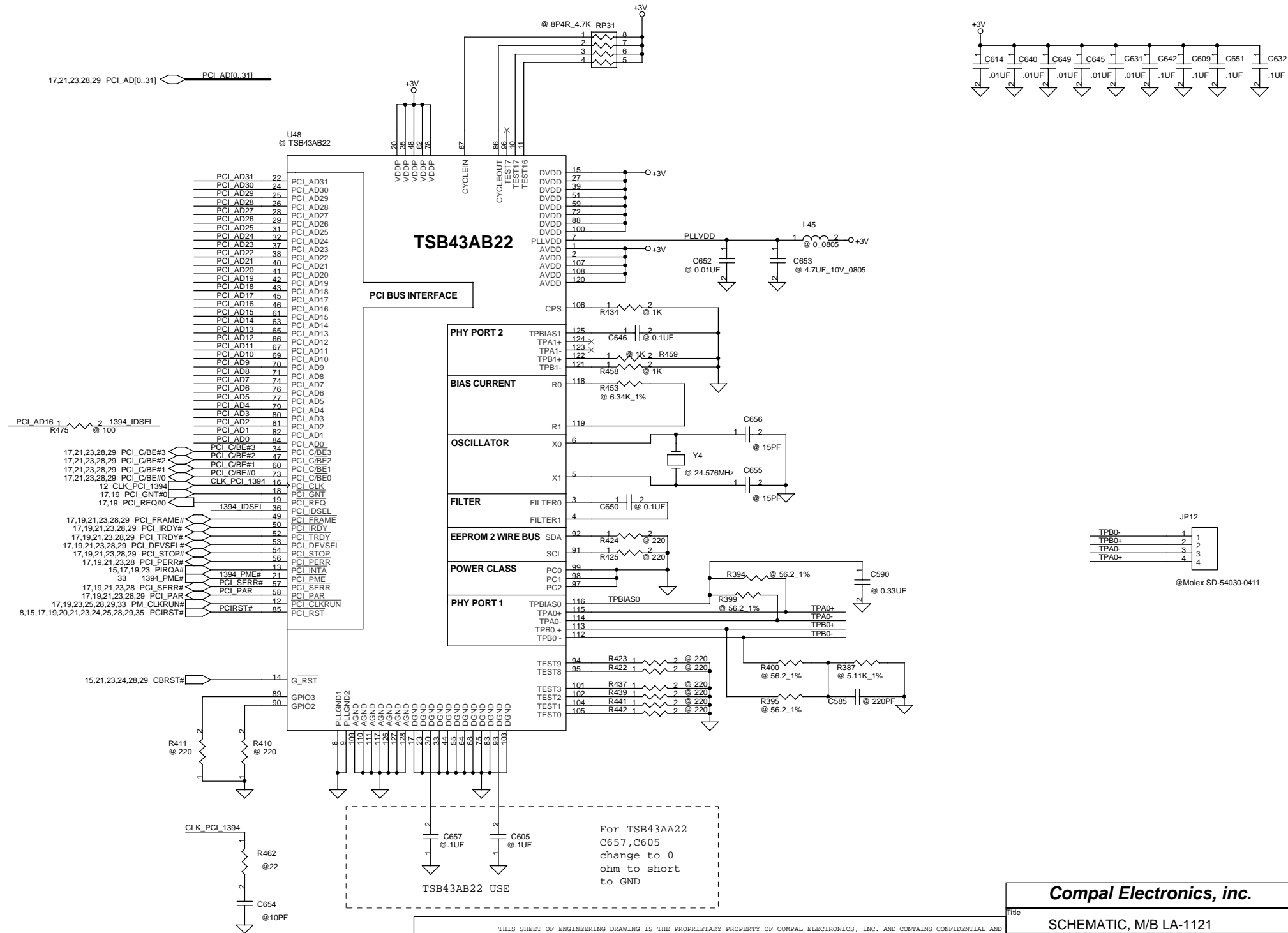
SI3456DV: N CHANNEL  
 VGS: 4.5V, RDS: 65 mOHM  
 Id(MAX): 5.1A  
 VGS,+20V



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Title		
SCHEMATIC, M/B LA-1121		
Size	Document Number	Rev
B	401191 (FOR ATW01)	1C
Date:	星期二, 十一月 27, 2001	Sheet 63 of 87

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Title: SCHEMATIC, M/B LA-1121

Size B Document Number 401191 (FOR ATW01) Rev 1C

Date: 星期一, 十一月 27, 2001 Sheet 65 of 87

For TSB43AA22  
C657, C605  
change to 0  
ohm to short  
to GND

JP12

TPB0-	1
TPB0+	2
TPA0-	3
TPA0+	4

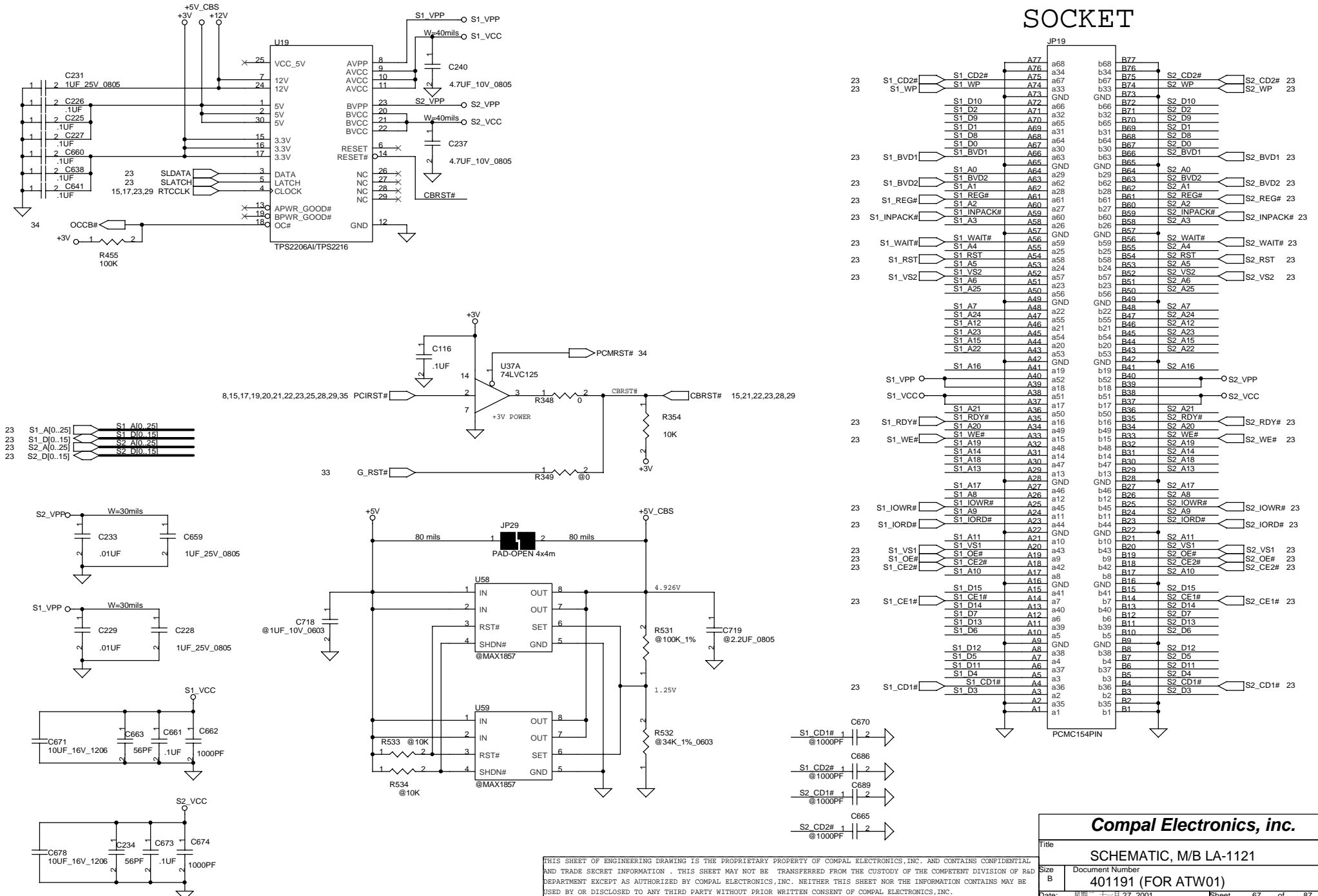
@Molex SD-54030-0411





# PCMCIA POWER CTRL.

# CARDBUS SOCKET



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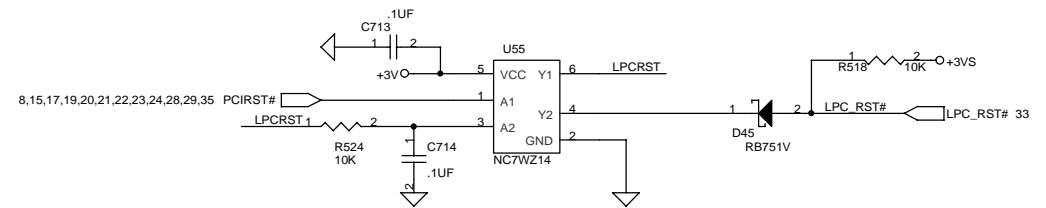
**Compal Electronics, inc.**

Title: SCHEMATIC, M/B LA-1121

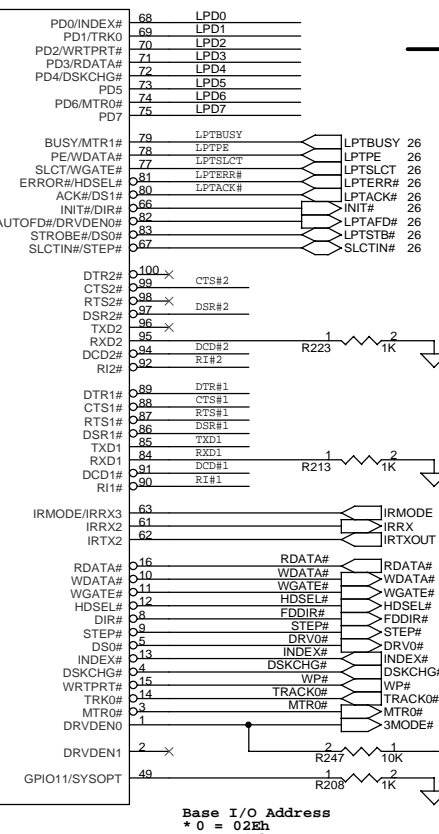
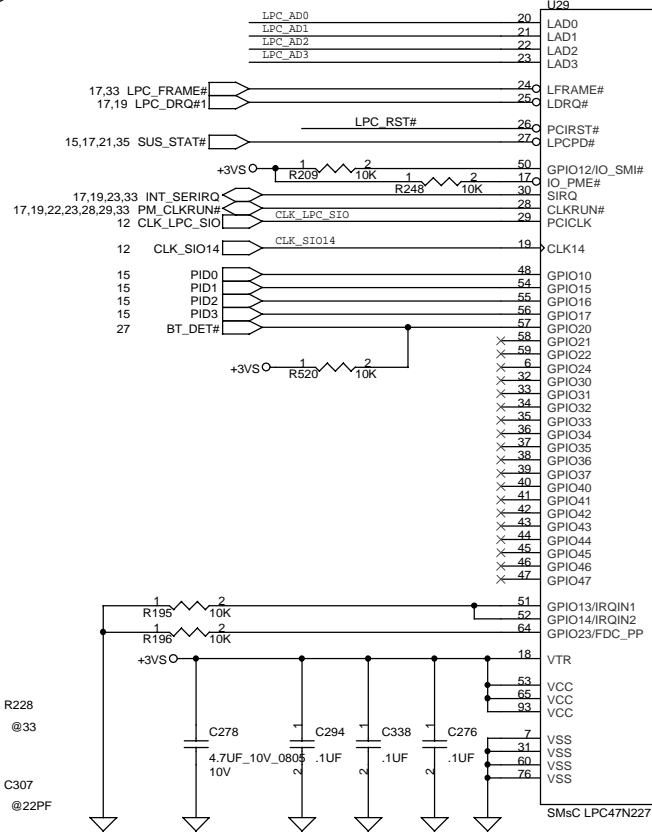
Size B Document Number 401191 (FOR ATW01) Rev 1C

Date: 星期二, 十一月 27, 2001 Sheet 67 of 87

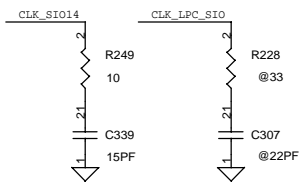
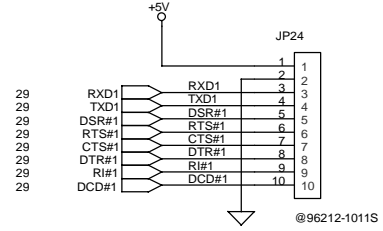
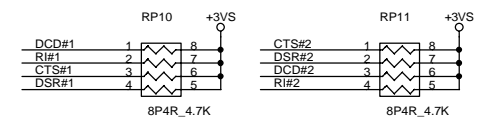
# SUPER I/O SMsC FDC47N227



17.33 LPC\_AD[0..3]  $\hookrightarrow$  LPC\_AD[0..3]



LPC\_I2C[0..7]  $\hookrightarrow$  LPC\_I2C[0..7] 26

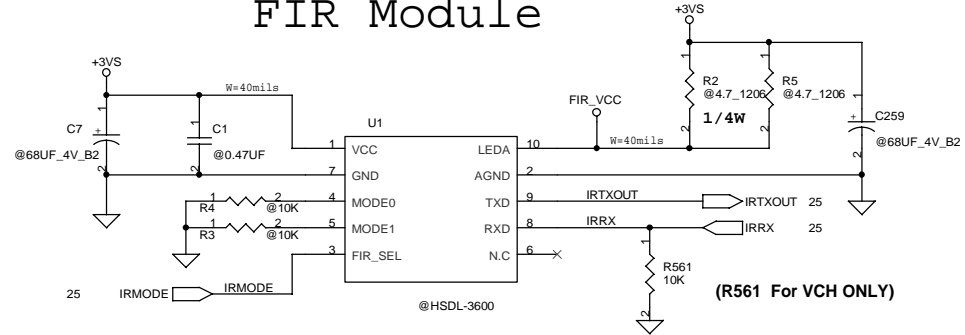


Base I/O Address  
\* 0 = 02Eh  
1 = 04Eh

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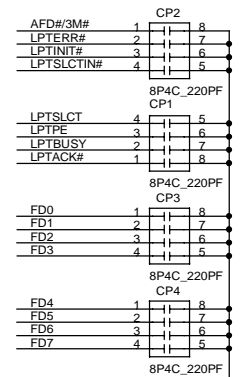
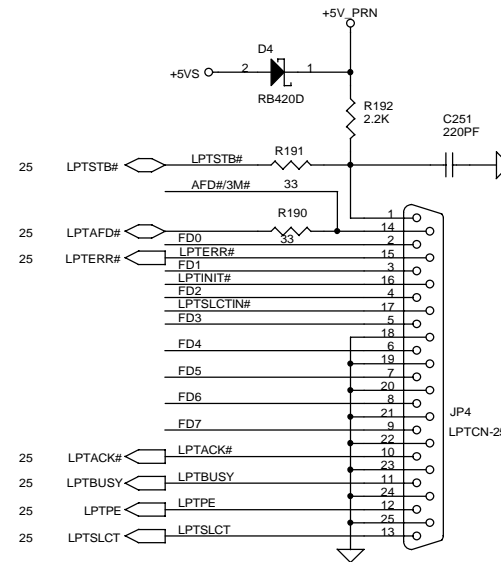
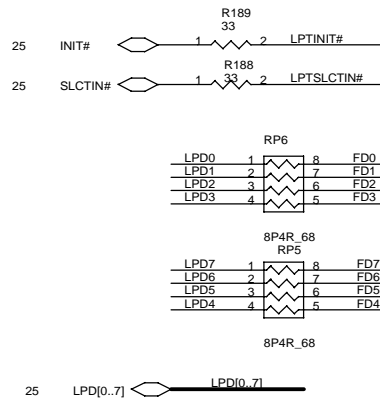
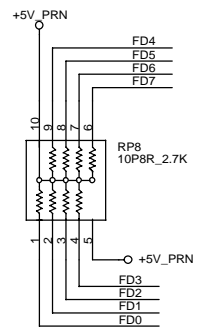
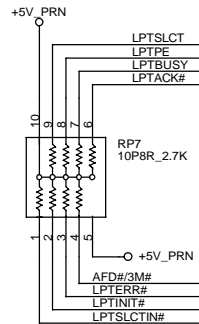
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Title		
SCHEMATIC, M/B LA-1121		
Size	Document Number	Rev
B	401191 (FOR ATW01)	1C
Date:	星期二, 十一月 27, 2001	Sheet 68 of 87

# FIR Module



The component's most place  
cloely IRDA MODULE.

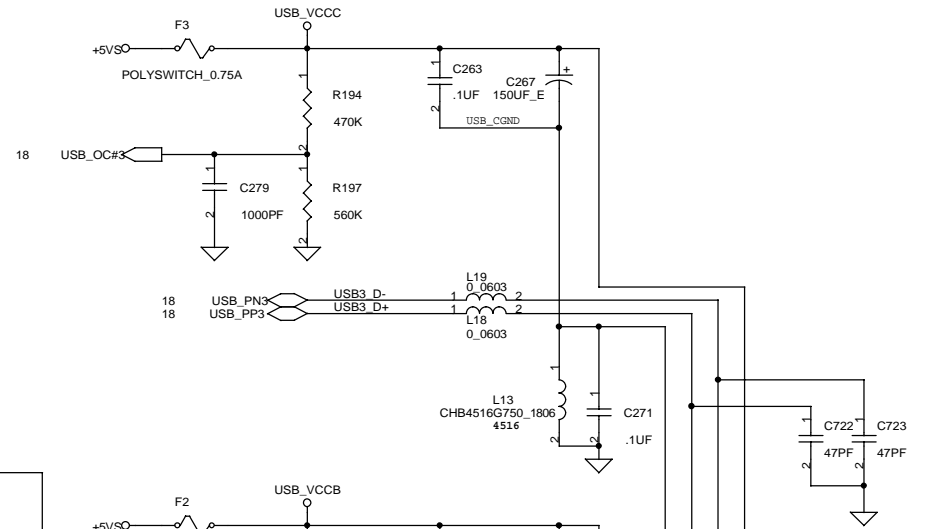
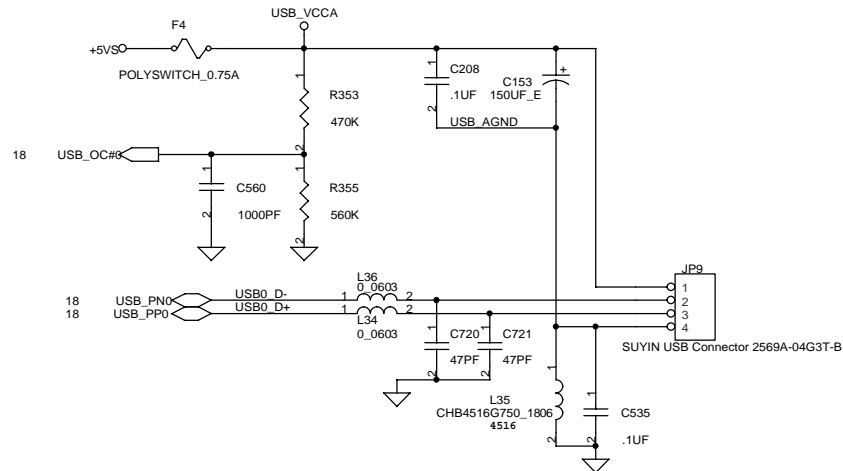
# PARALLEL PORT



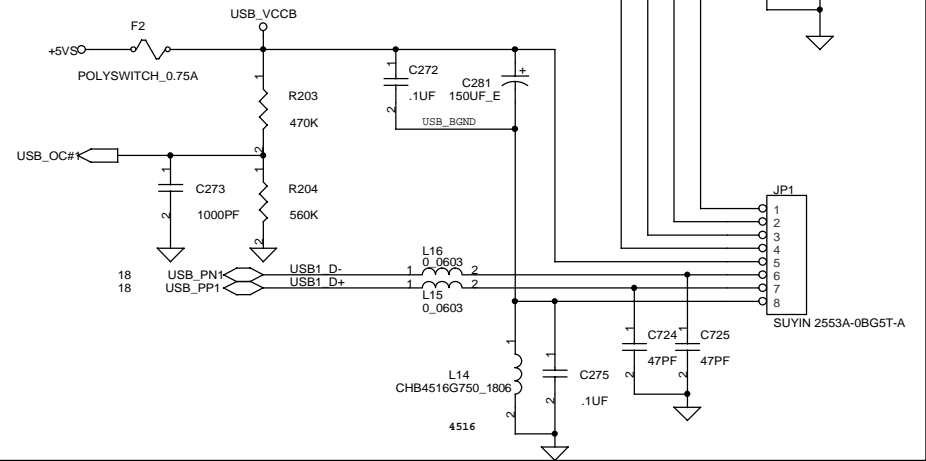
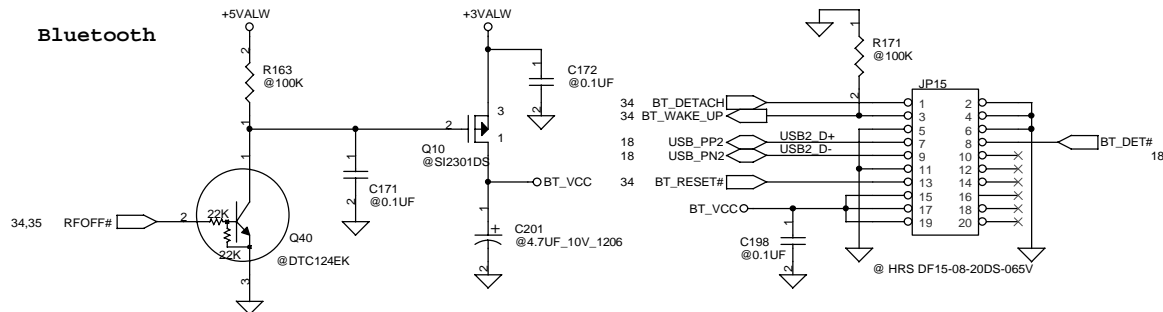
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Title		
SCHEMATIC, M/B LA-1121		
Size	Document Number	Rev
	401191 (FOR ATW01)	1C
Date:	星期二, 十一月 27, 2001	Sheet 69 of 87

**USB PORT**

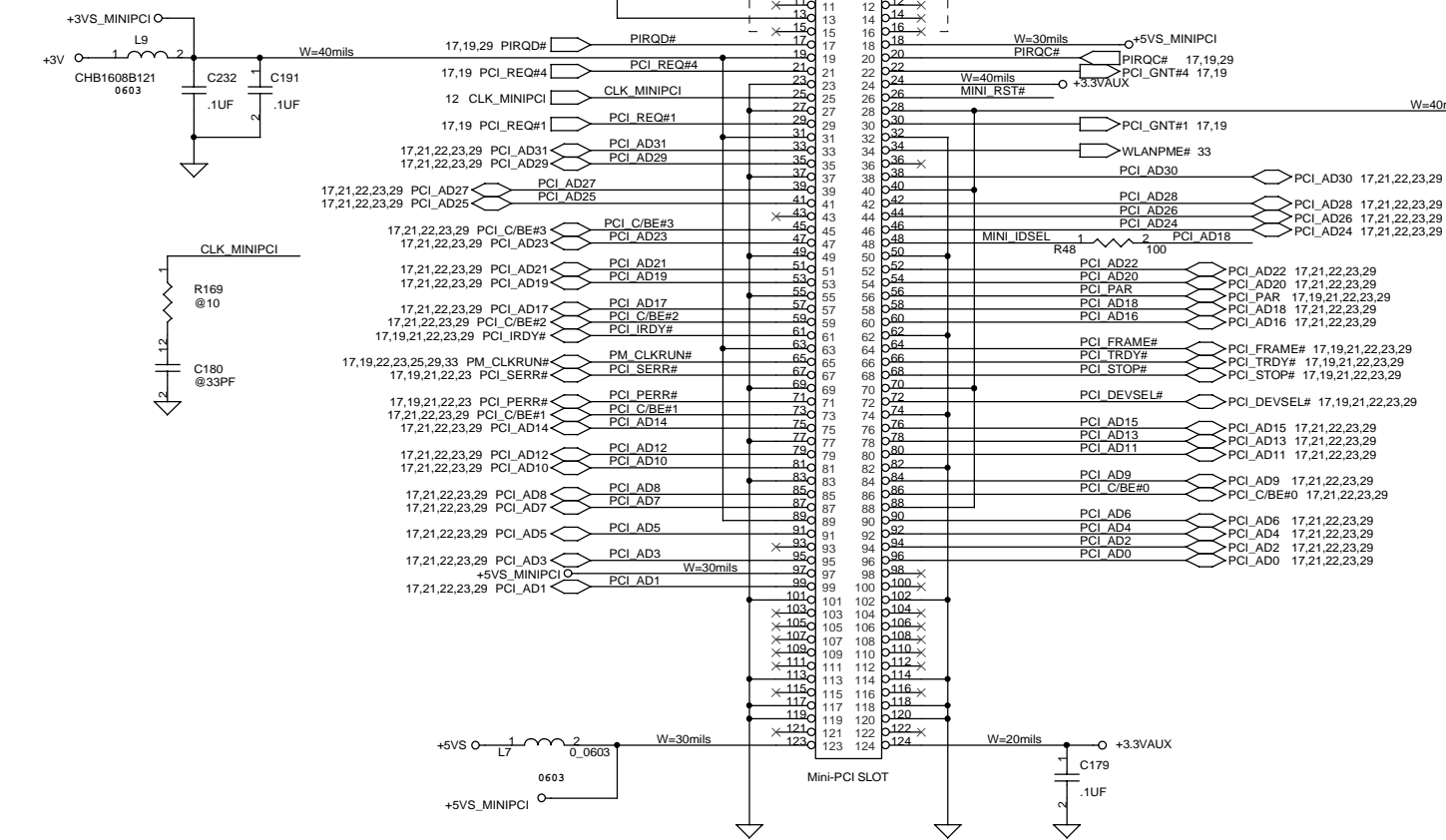
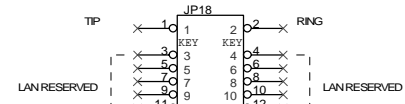
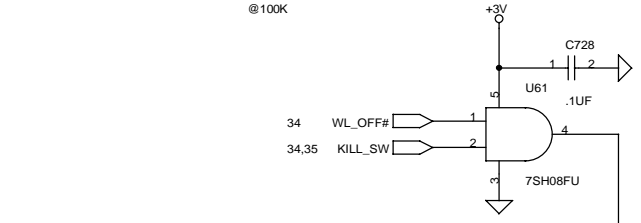
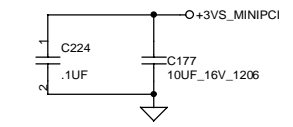
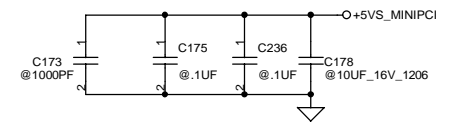
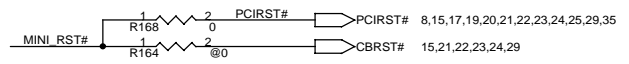
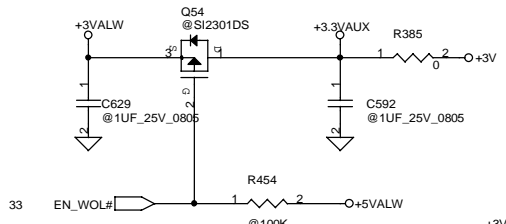


**Bluetooth**

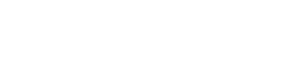
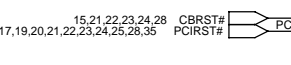
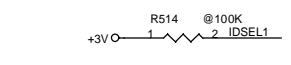
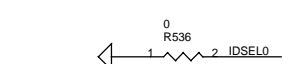
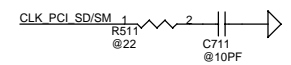
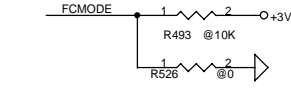
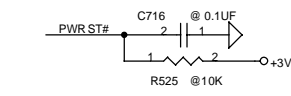
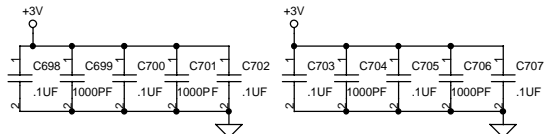


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Title	SCHEMATIC, M/B LA-1121	
Size B	Document Number	Rev 1C
Date:	星期二, 十一月 27, 2001	Sheet 70 of 87



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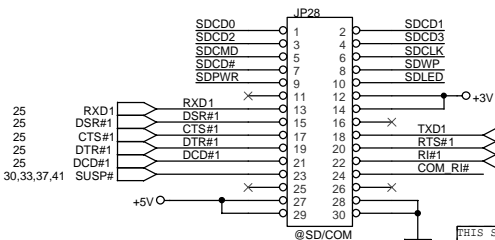
17,21,22,23,28 PCI\_AD[0..31] PCI\_AD[0..31]

17,21,22,23,28 PCI\_C/BE#0  
17,21,22,23,28 PCI\_C/BE#1  
17,21,22,23,28 PCI\_C/BE#2  
17,21,22,23,28 PCI\_C/BE#3  
17,19,21,22,23,28 PCI\_PAR  
17,19,21,22,23,28 PCI\_FRAME#  
17,19,21,22,23,28 PCI\_IRDY#  
17,19,21,22,23,28 PCI\_TRDY#  
17,19,21,22,23,28 PCI\_STOP#

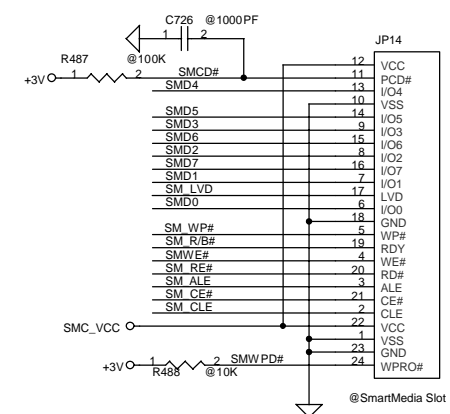
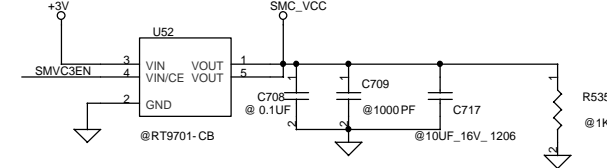
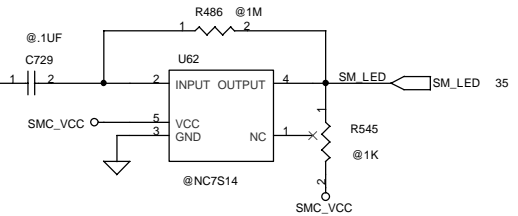
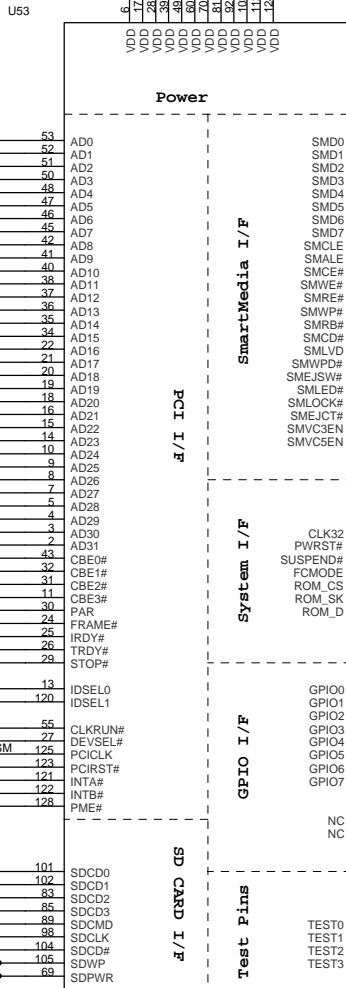
PCI\_AD22 R496 1 2 @100 IDSEL0 13  
PCI\_AD22 R497 1 2 @100 IDSEL1 13  
17,19,22,23,25,28,33 PM\_CLKRUN# 55  
17,19,21,22,23,28 PCI\_DEVSEL# 27  
17,19,21,22,23,28 CLK\_PCI\_SD/SM 125  
17,19,28 PIRQC# 121  
17,19,28 PIRQD# 122  
33 SM/SD\_PME# 128

R537 1 2 @100K SDCD0 101  
R538 1 2 @100K SDCD1 102  
R539 1 2 @100K SDCD2 83  
R540 1 2 @100K SDCD3 85  
R541 1 2 @100K SDCMD 89  
R542 @0 88  
104  
105  
69

**SD Transfer Conn.**



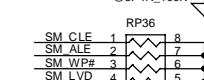
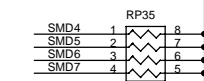
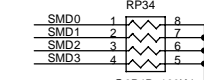
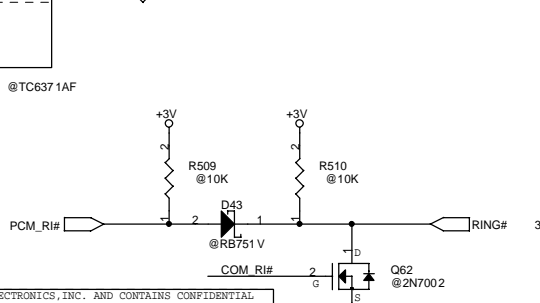
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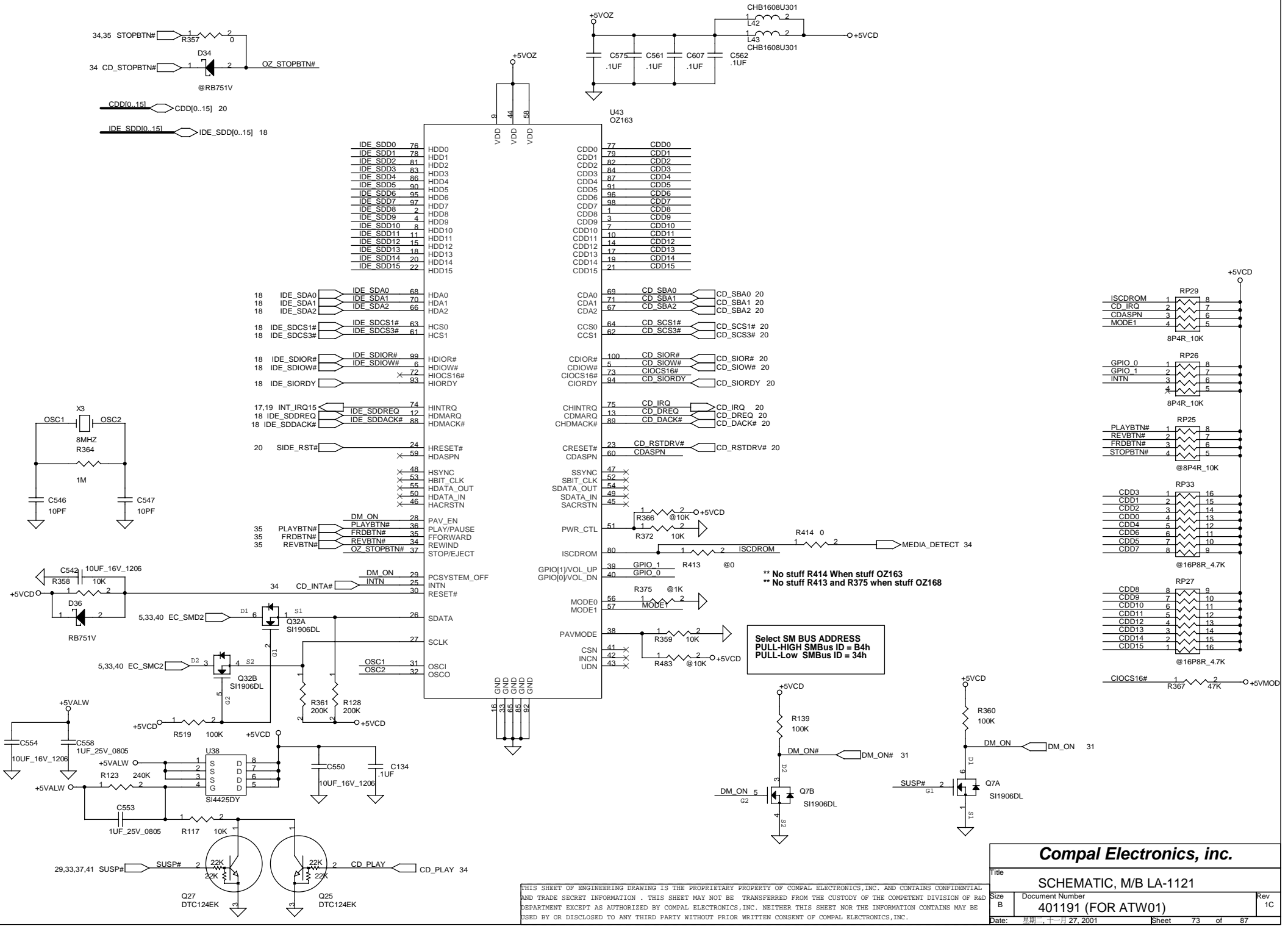
59 PWRST# RTCCLK 15,17,23,24  
56 FCMODE SUSP# 30,33,37,41  
57  
58  
68 ROM\_CS  
67 ROM\_SK  
66

110 R499 1 2 @100K GPIO0 +3V  
111 R500 1 2 @100K GPIO1 +3V  
112 R501 1 2 @100K GPIO2 +3V  
114 R502 1 2 @100K GPIO3 +3V  
115 R503 1 2 @100K GPIO4 +3V  
118 R504 1 2 @100K GPIO5 +3V  
117 R505 1 2 @100K GPIO6 +3V  
119 R506 1 2 @100K GPIO7 +3V

126 NC  
127 NC  
61 TEST0  
62 TEST1  
63 TEST2  
64 TEST3  
R508 @0



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Title <b>SCHEMATIC, M/B LA-1121</b>		
Size B	Document Number <b>401191 (FOR ATW01)</b>	Rev 1C
Date: 星期一, 十一月 27, 2001	Sheet 72	of 87



\*\* No stuff R414 When stuff OZ163  
 \*\* No stuff R413 and R375 when stuff OZ168

Select SM BUS ADDRESS  
 PULL-HIGH SMBus ID = B4h  
 PULL-Low SMBus ID = 34h

**Compal Electronics, inc.**

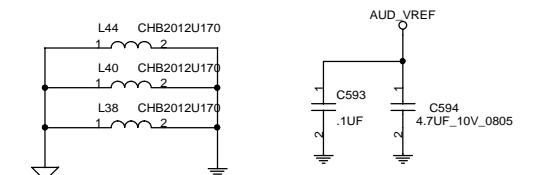
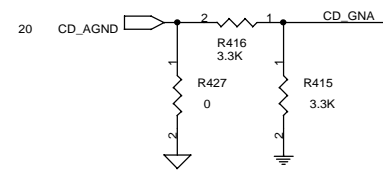
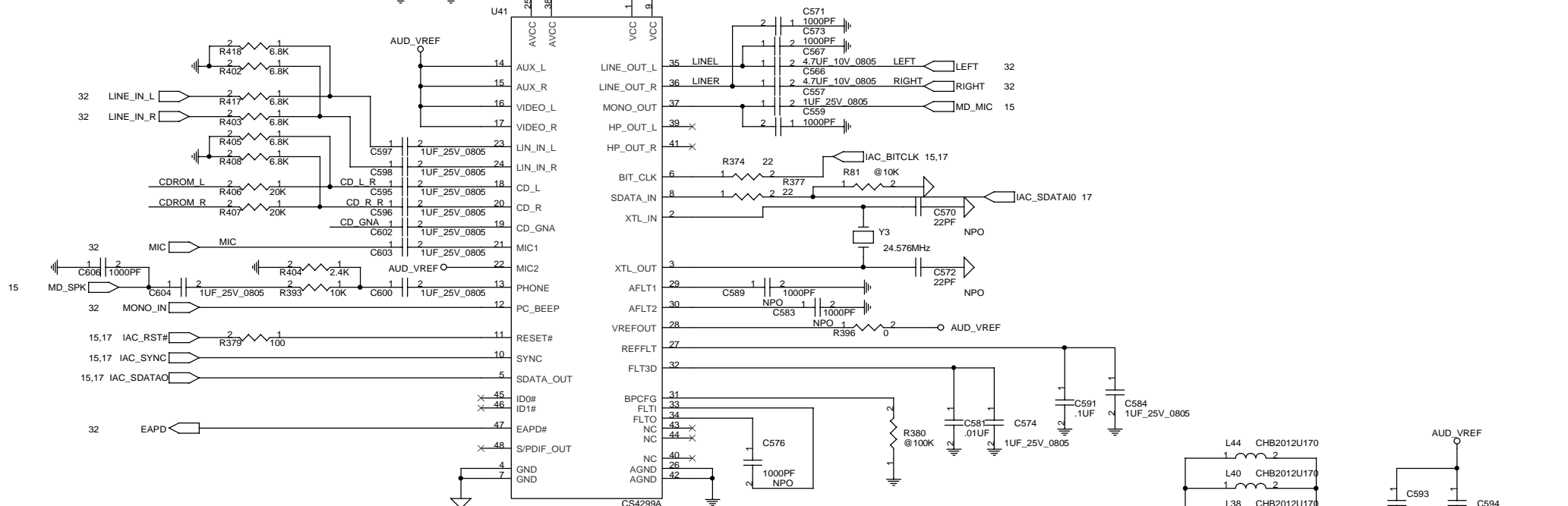
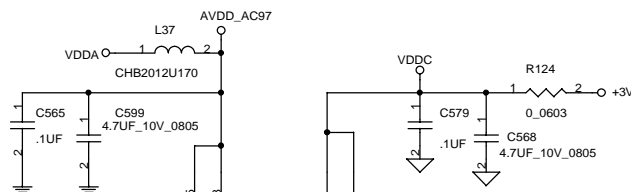
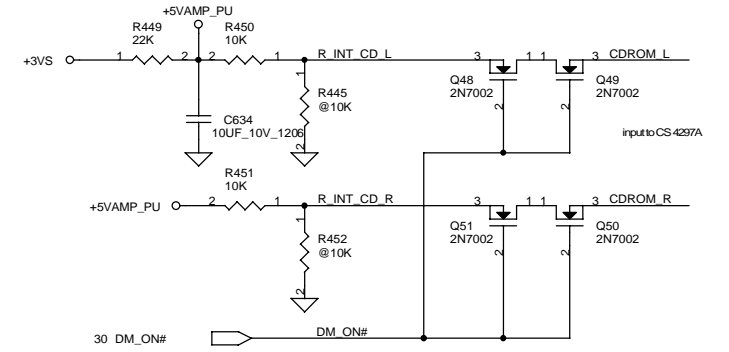
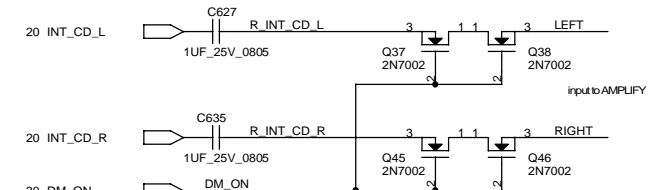
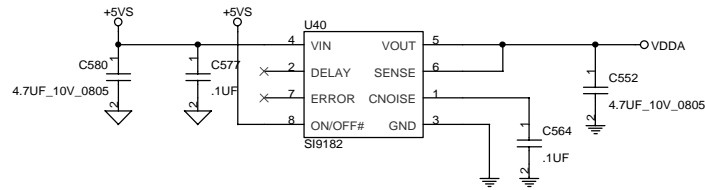
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Size B Document Number 401191 (FOR ATW01) Rev 1C

Date: 星期三, 十一月 27, 2001 Sheet 73 of 87

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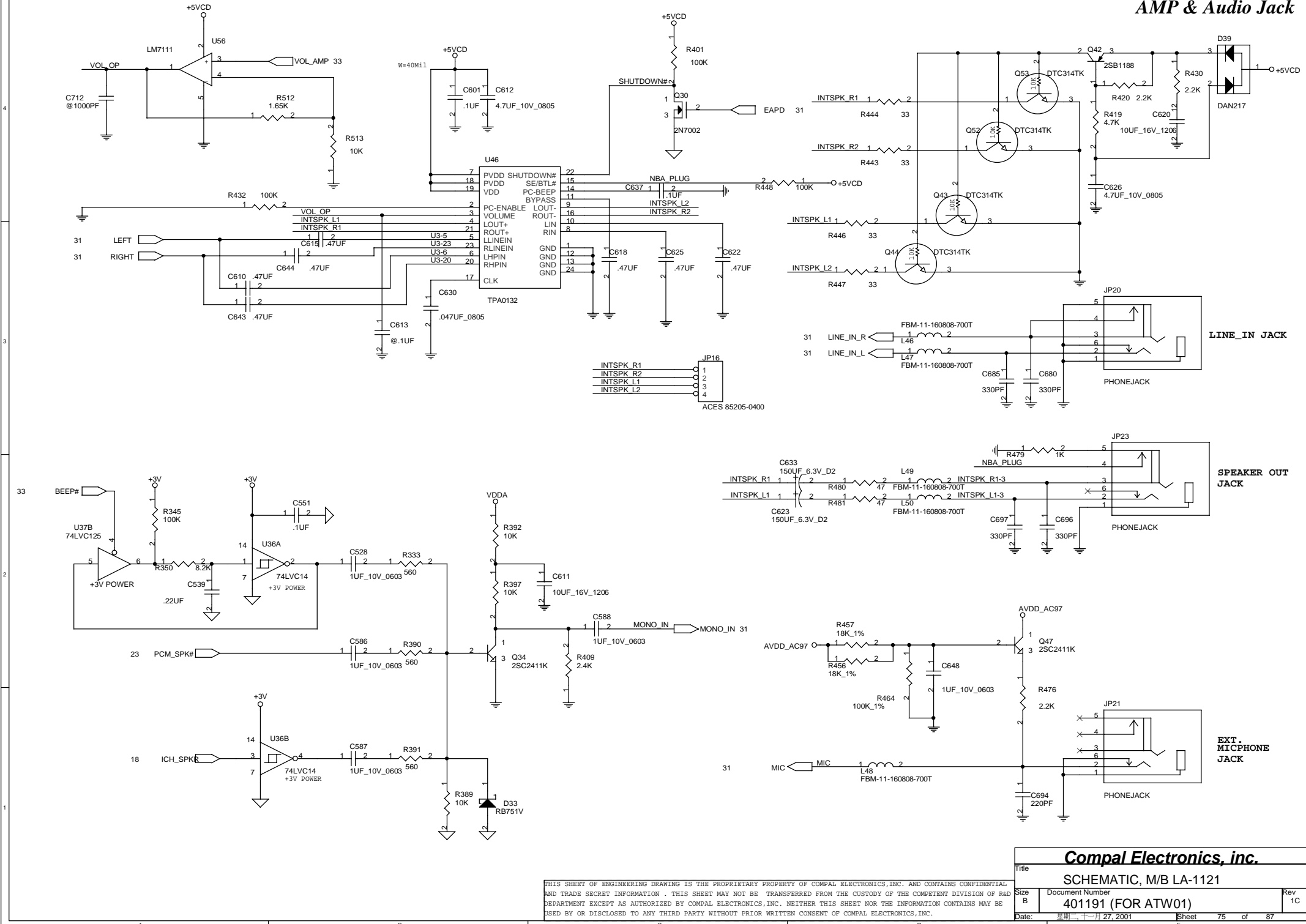




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Title	SCHEMATIC, M/B LA-1121	
Size	Document Number	Rev
B	401191 (FOR ATW01)	1C
Date:	星期二, 十一月 27, 2001	Sheet 74 of 87

# AMP & Audio Jack



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SCHMATIC, M/B LA-1121

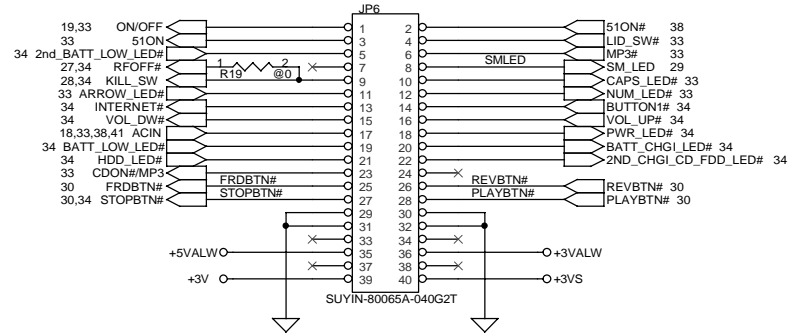
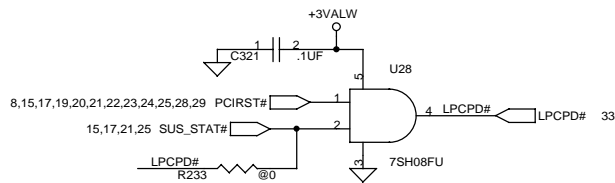
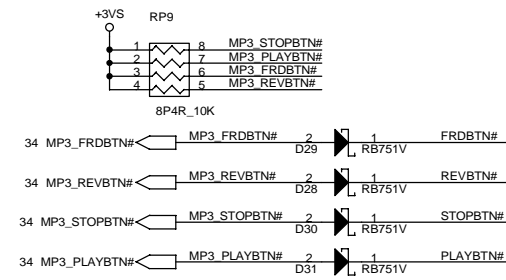
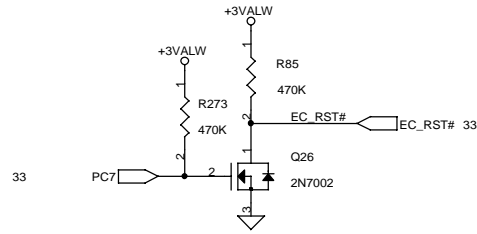
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**401191 (FOR ATW01)**

Date: 星期一, 十一月 27, 2001 Sheet 75 of 87

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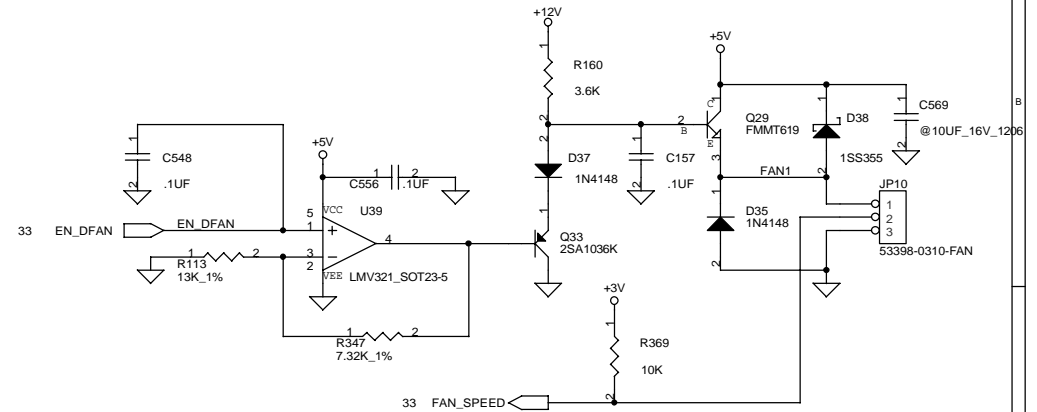






For PC87591 REV 0.A Only

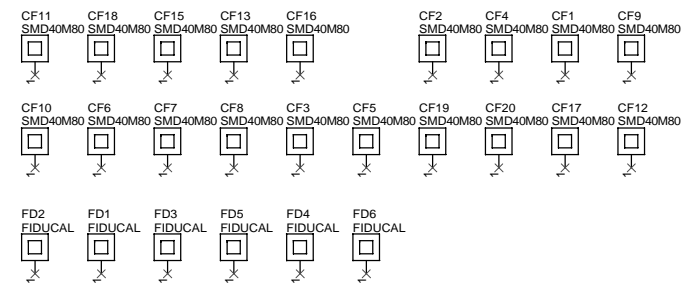
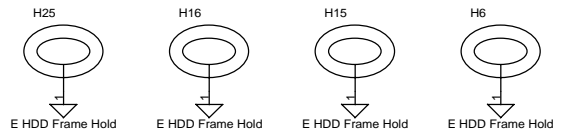
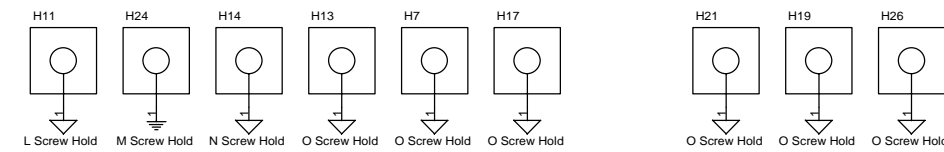
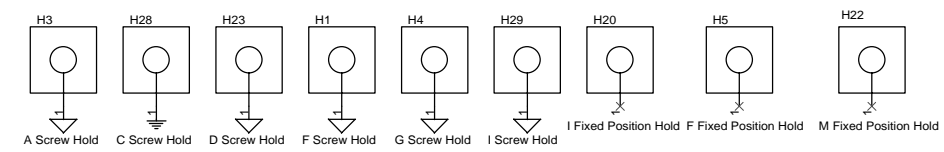
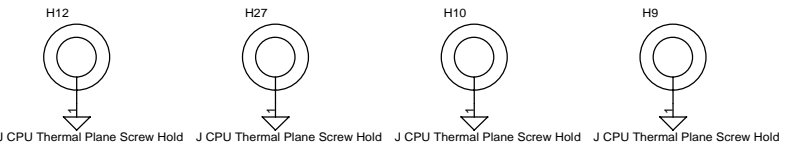
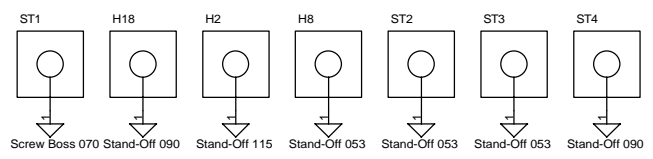
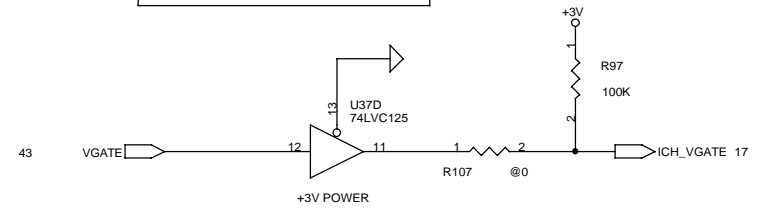
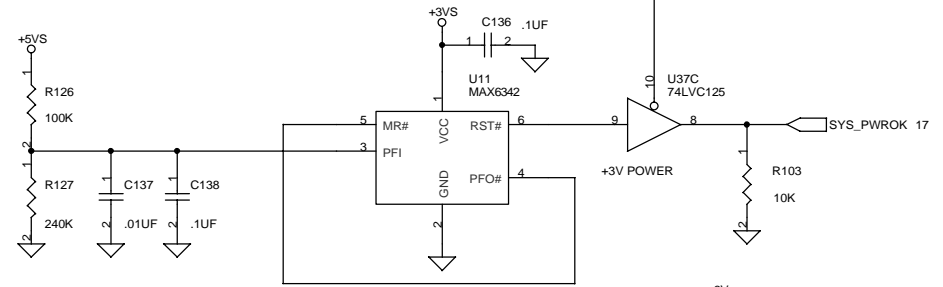
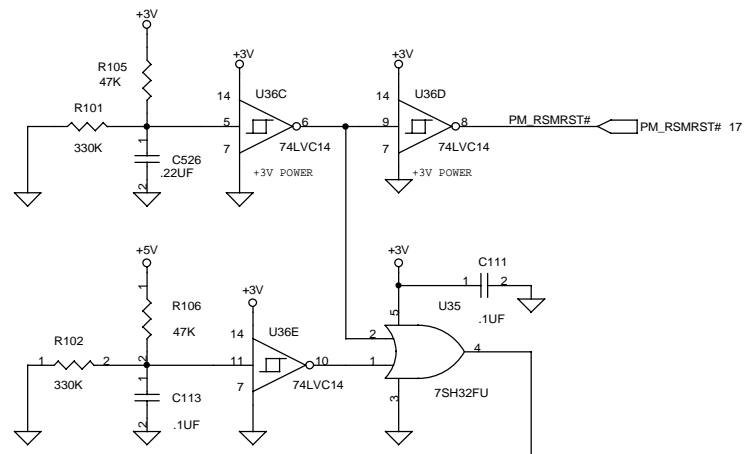
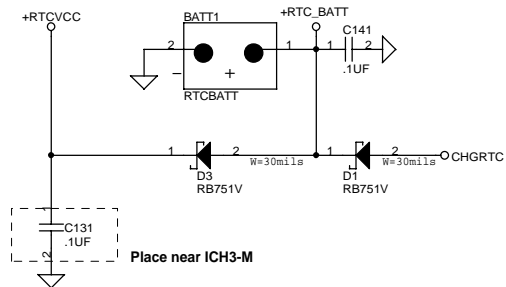
### FAN CONN.



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Title	SCHMATIC, M/B LA-1121
Size	Document Number
B	401191 (FOR ATW01)
Date:	Rev 1C
日期: 十一月 27, 2001	Sheet 78 of 87

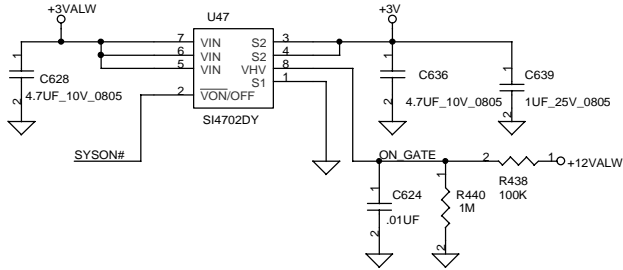
**RTC Batt. Connector**



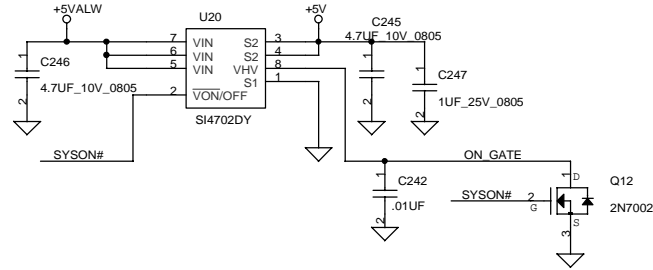
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Title		
SCHEMATIC, M/B LA-1121		
Size	Document Number	Rev
B	401191 (FOR ATW01)	1C
Date:	星期二, 十一月 27, 2001	Sheet 79 of 87

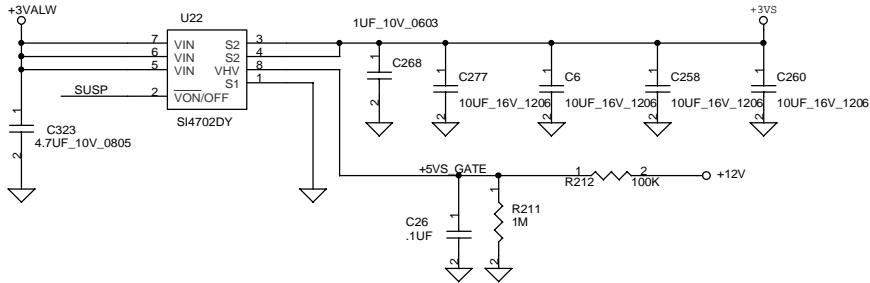
**+3VALW To +3V Transfer**



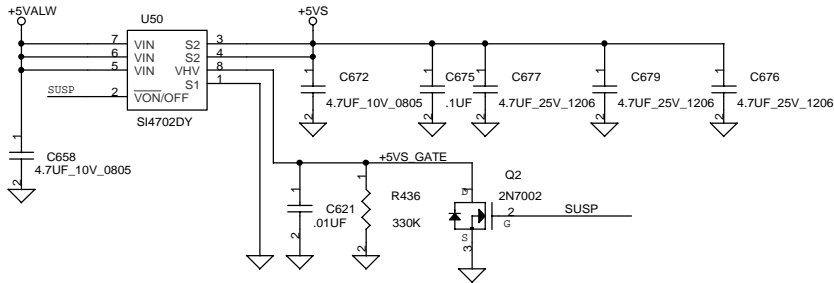
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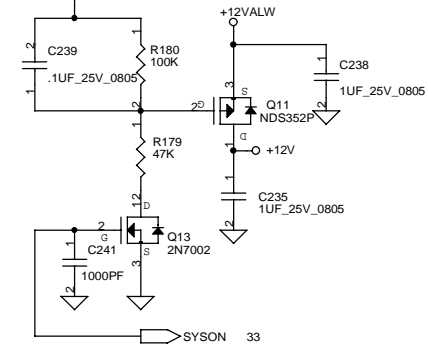
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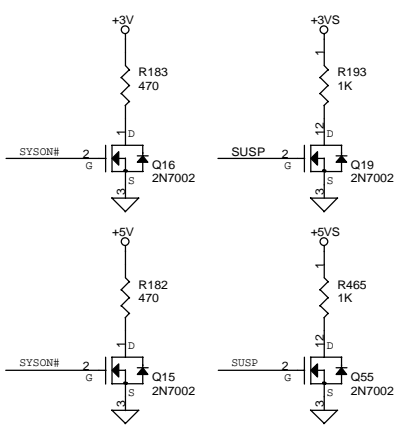
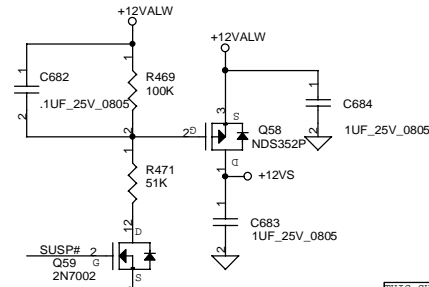
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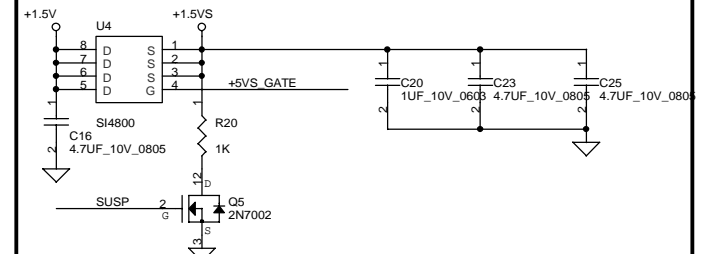
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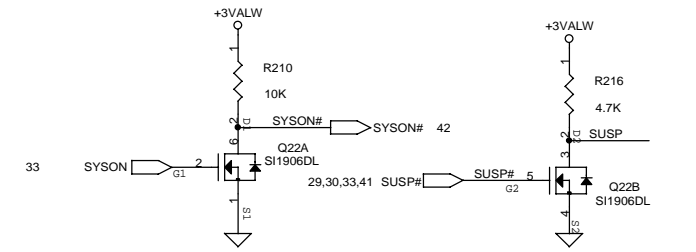
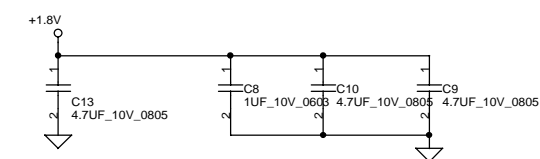
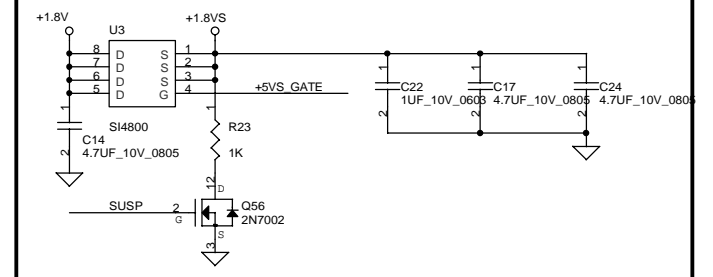
**+12VALW To +12VS Transfer**



**+1.5V TO +1.5V\_SW Transfer**



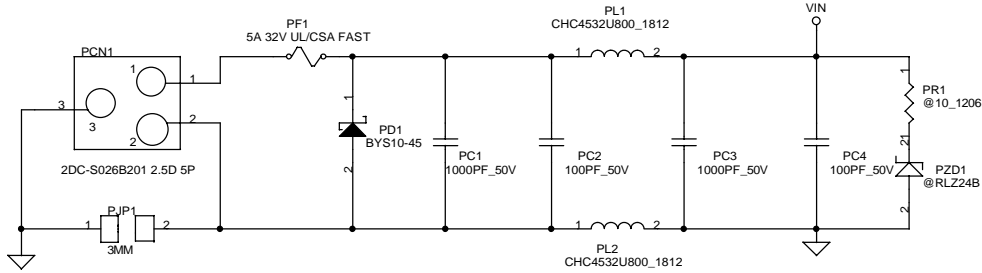
**+1.8V\_ALW TO +1.8V\_SW Transfer**



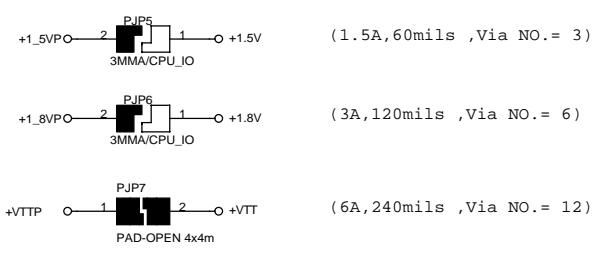
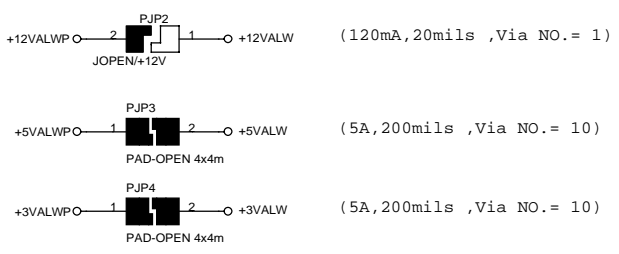
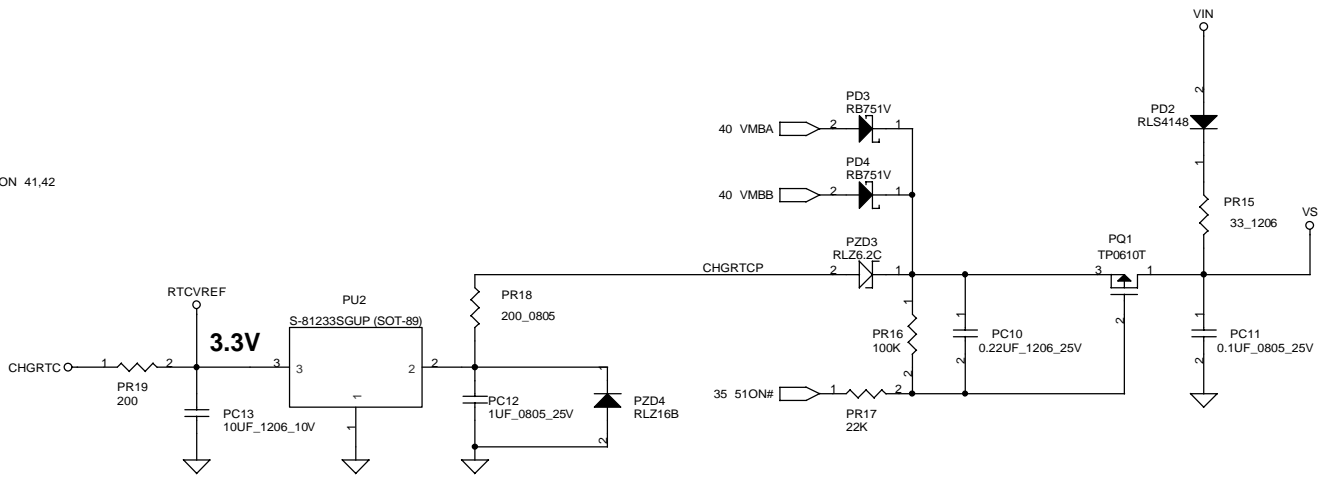
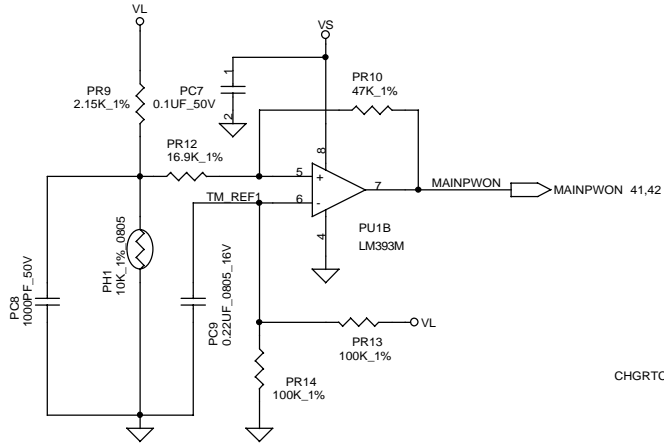
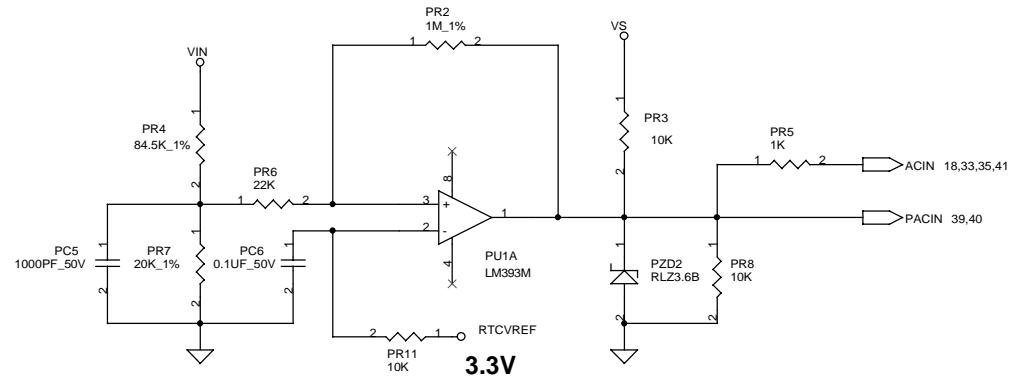
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Title	SCHEMATIC, M/B LA-1121	
Size	Document Number	Rev
Custom	401191 (FOR ATW01)	1C
Date:	星期一, 十一月 27, 2001	Sheet 80 of 87

**Vin Detector**  
**High 18.764 17.901 17.063**  
**Low 17.745 16.903 16.038**



**PH1 under CPU botten side :**  
 CPU thermal protection at 82 degree C  
 Recovery at 50(51) degree C



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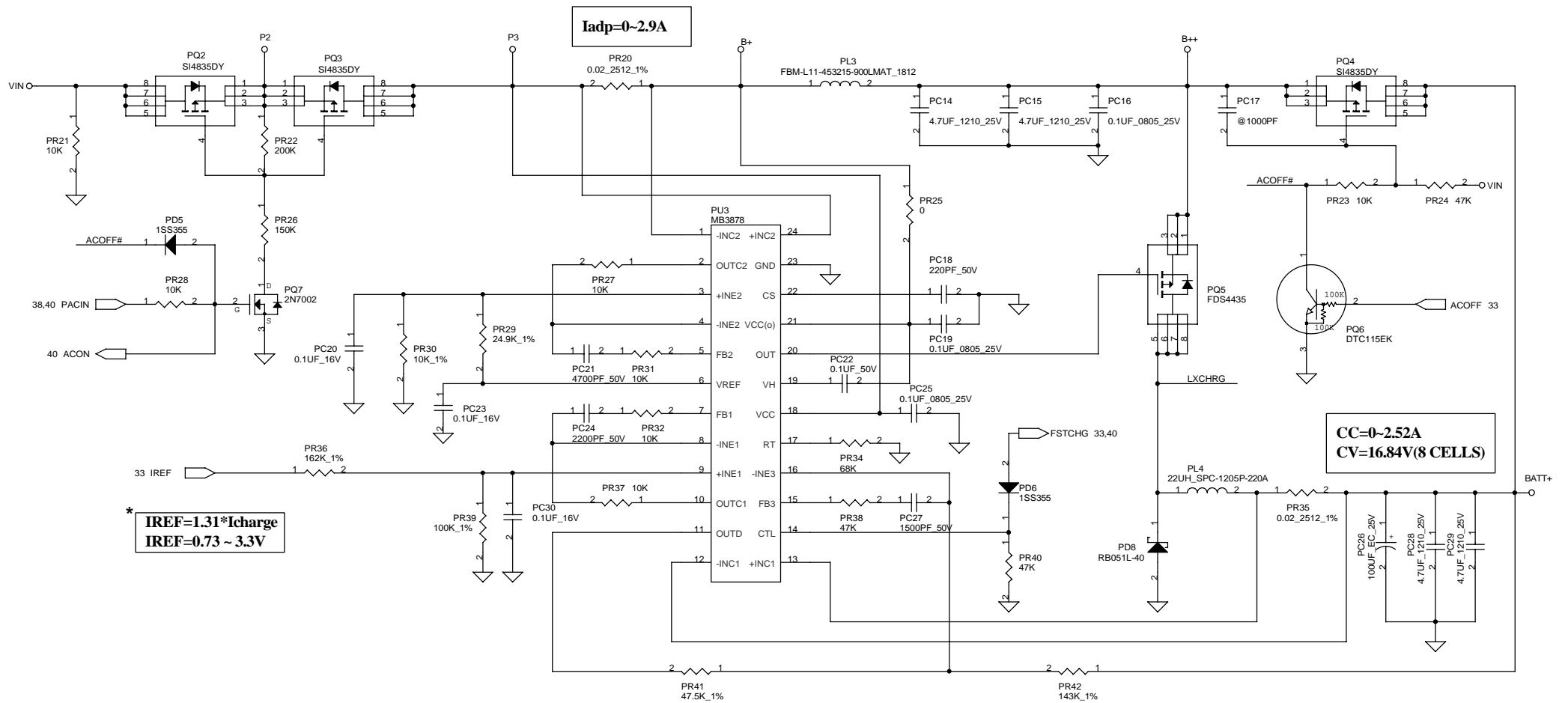
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Size B Document Number 401191 (FOR ATW01) Rev 1C

Date: 星期二, 十一月 27, 2001 Sheet 81 of 87

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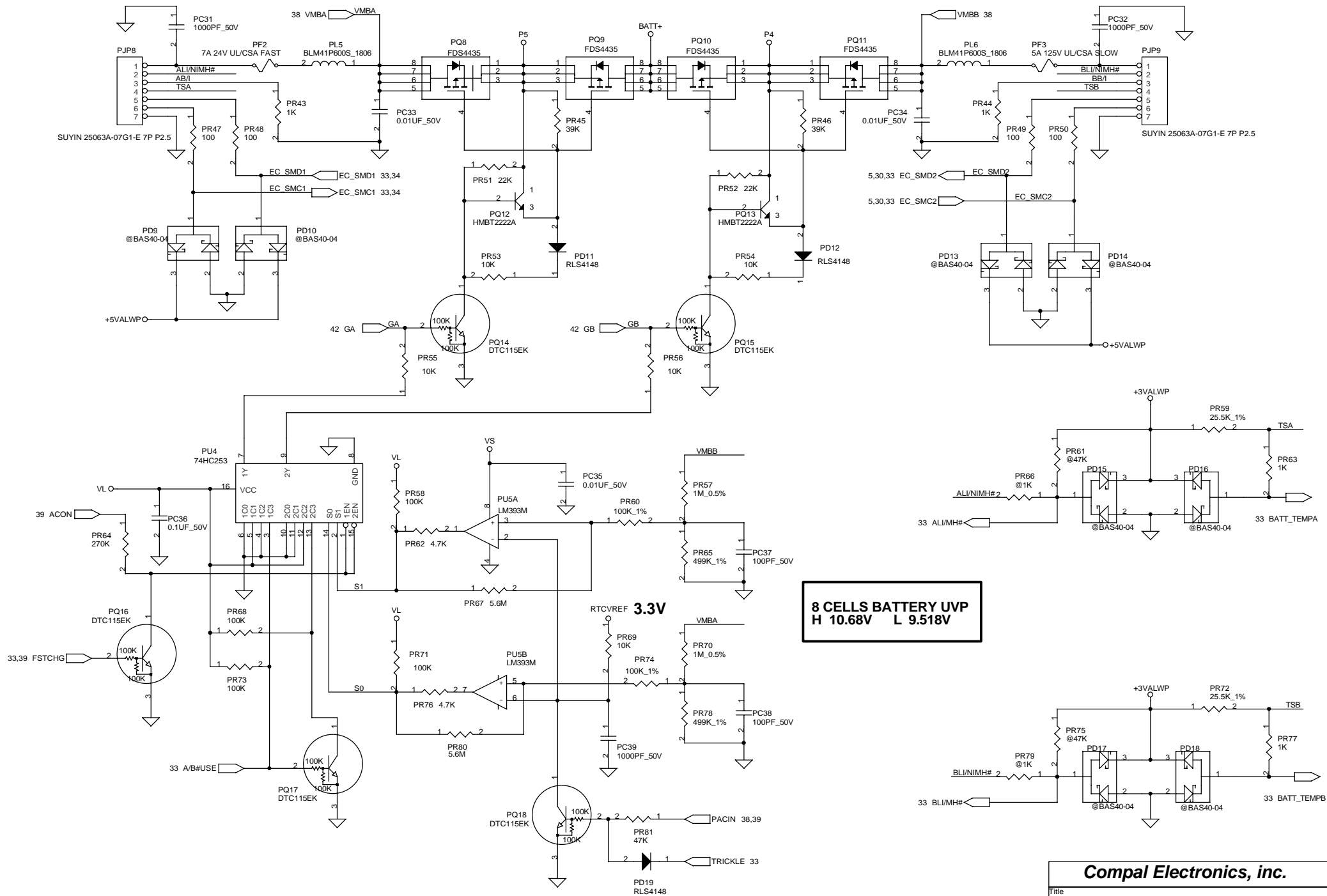


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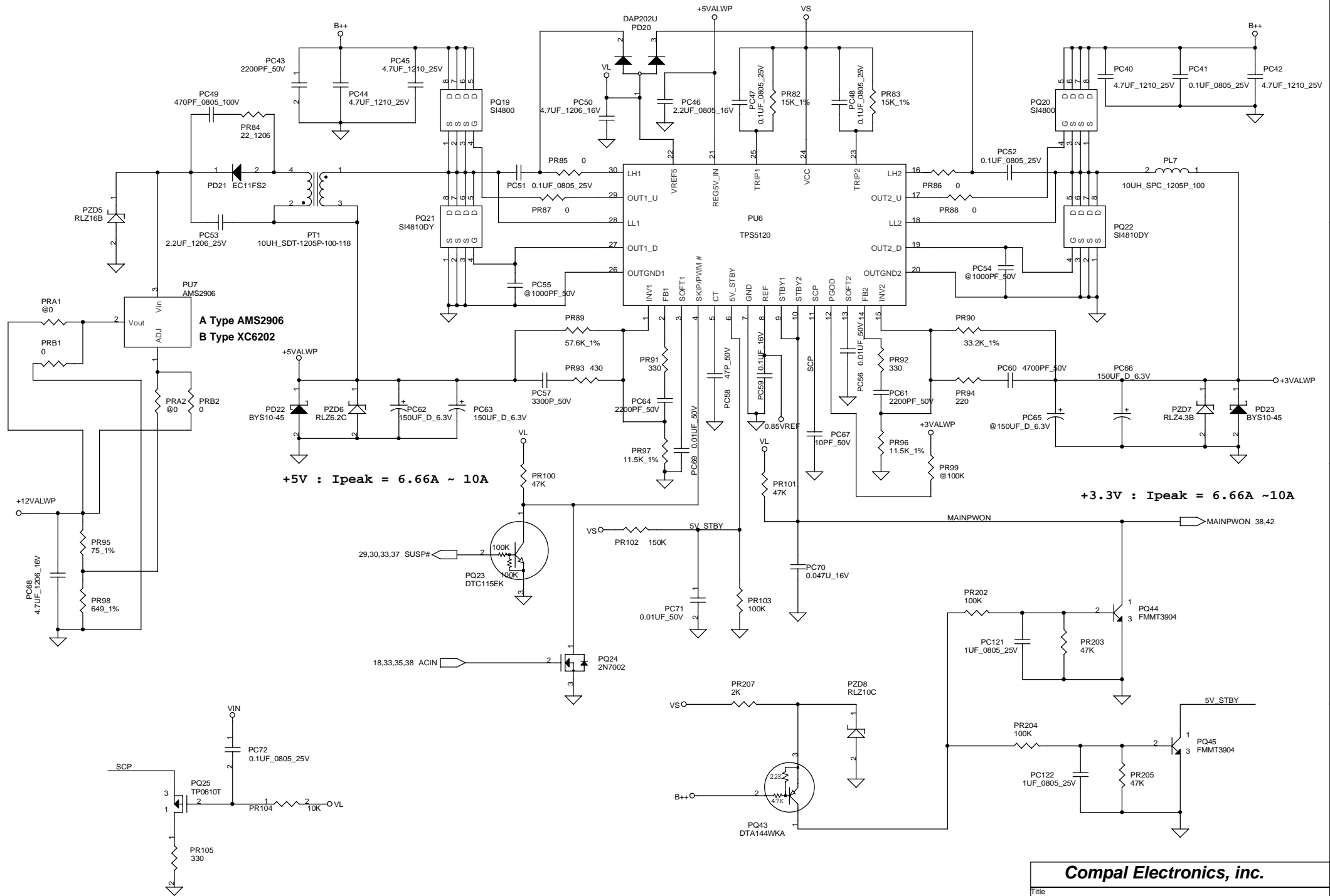
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B	401191 (FOR ATW01)	1C
Date:	星期二, 十一月 27, 2001	Sheet 82 of 87

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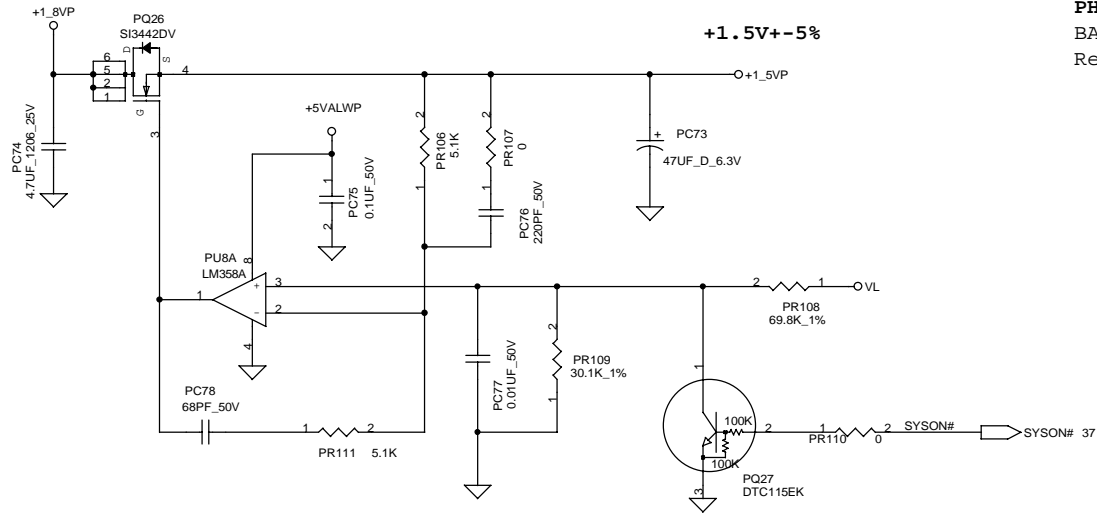
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Title		
SCHEMATIC, M/B LA-1121		
Size	Document Number	Rev
B	401191 (FOR ATW01)	1C
Date:	星期二, 十一月 27, 2001	Sheet 83 of 87



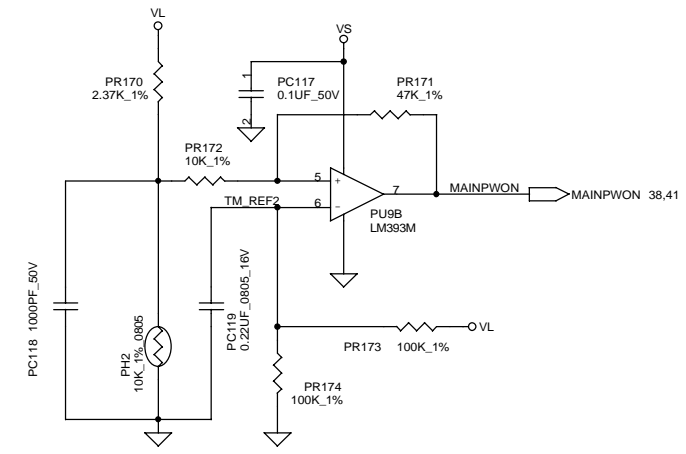
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Title		
SCHEMATIC, M/B LA-1121		
Size	Document Number	Rev
B	401191 (FOR ATW01)	1C
Date:	星期二, 十一月 27, 2001	Sheet 84 of 87

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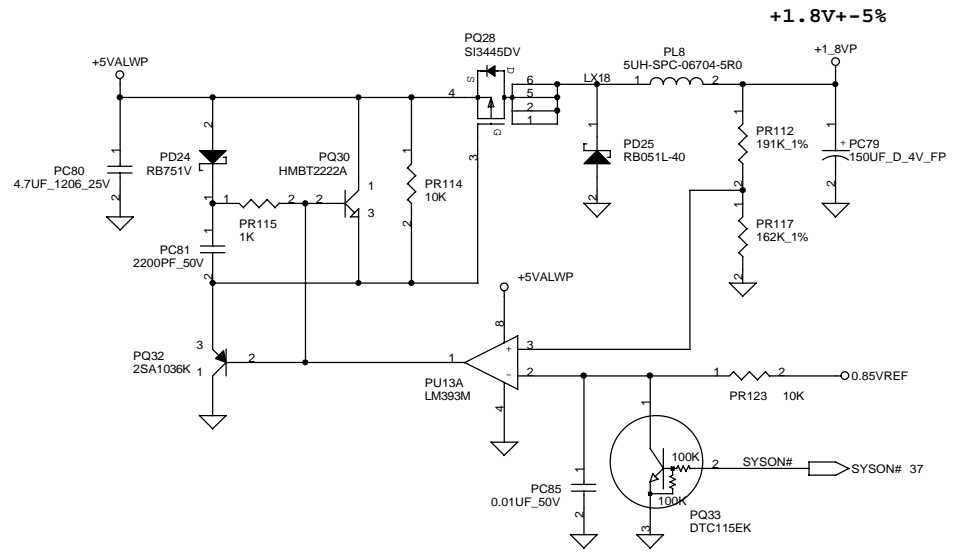
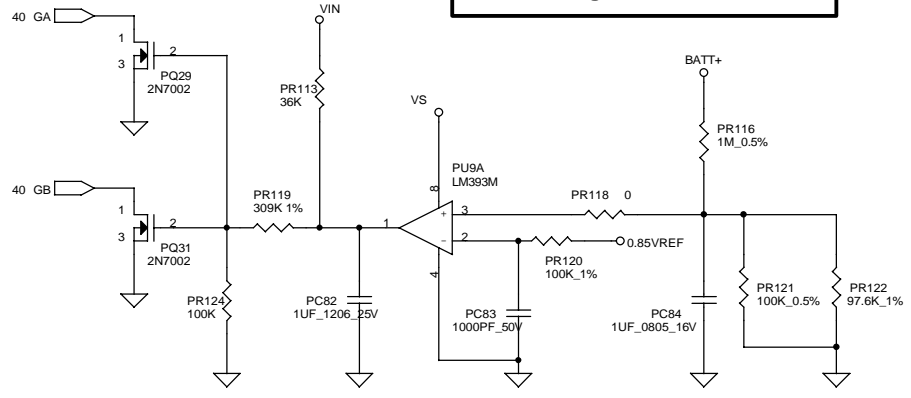


**+1.5V+-5%**

**PH2 near main Battery CONN :**  
 BAT. thermal protection at 73 degree C  
 Recovery at 50(51) degree C



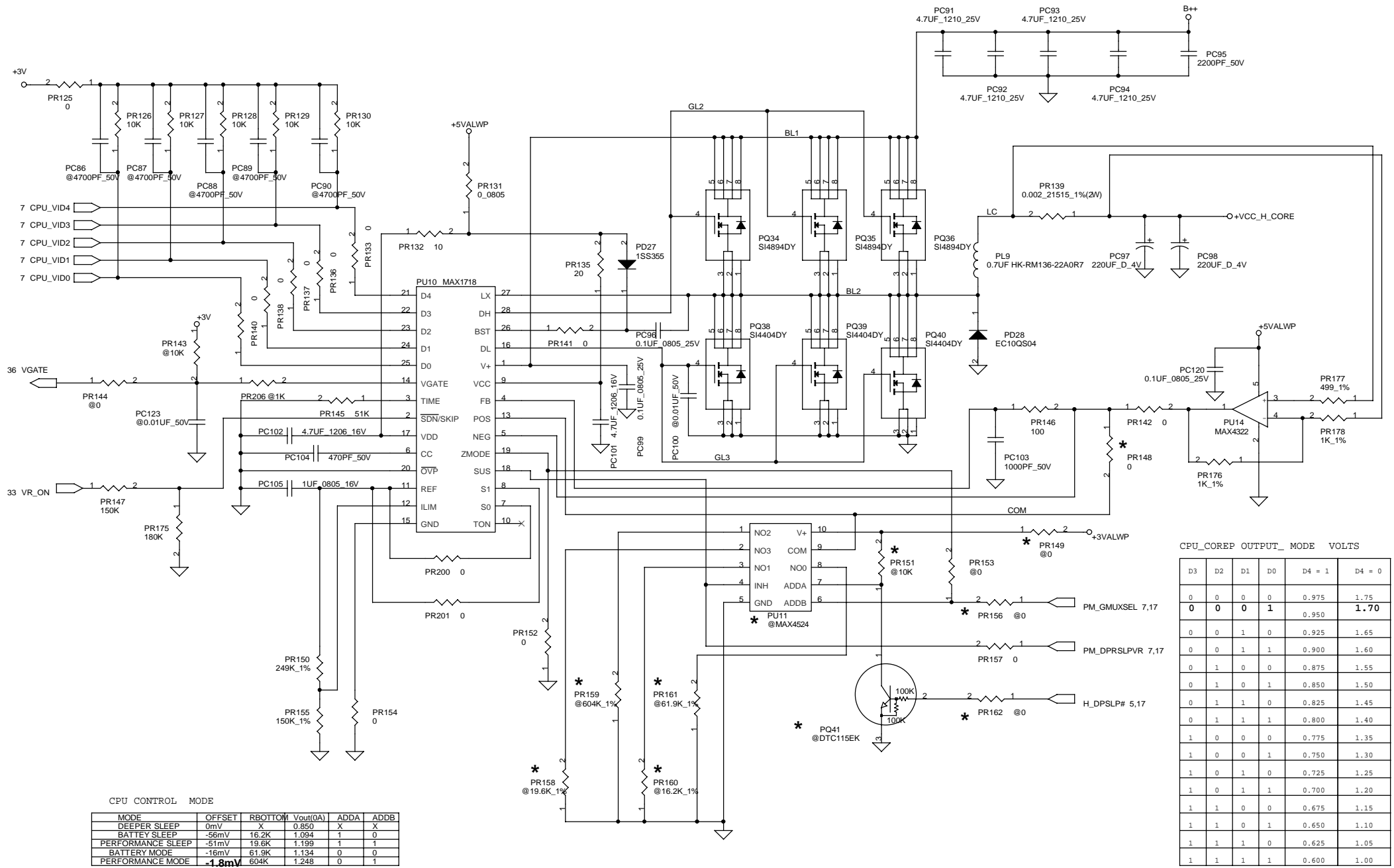
**8 Cells Charger OVP : 18.059V**



**+1.8V+-5%**

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Title		
SCHEMATIC, M/B LA-1121		
Size	Document Number	Rev
B	401191 (FOR ATW01)	1C
Date:	星期一, 十一月 27, 2001	Sheet 85 of 87

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CPU CONTROL MODE

MODE	OFFSET	RBOTTOM	Vout(0A)	ADDA	ADDB
DEEPER SLEEP	0mV	X	0.850	X	X
BATTERY SLEEP	-56mV	16.2K	1.094	1	0
PERFORMANCE SLEEP	-51mV	19.6K	1.199	1	1
BATTERY MODE	-16mV	61.9K	1.134	0	0
PERFORMANCE MODE	<b>-1.8mV</b>	604K	1.248	0	1

CPU\_COREP OUTPUT\_MODE VOLTS

D3	D2	D1	D0	D4 = 1	D4 = 0
0	0	0	0	0.975	1.75
<b>0</b>	<b>0</b>	<b>0</b>	<b>1</b>	0.950	<b>1.70</b>
0	0	1	0	0.925	1.65
0	0	1	1	0.900	1.60
0	1	0	0	0.875	1.55
0	1	0	1	0.850	1.50
0	1	1	0	0.825	1.45
0	1	1	1	0.800	1.40
1	0	0	0	0.775	1.35
1	0	0	1	0.750	1.30
1	0	1	0	0.725	1.25
1	0	1	1	0.700	1.20
1	1	0	0	0.675	1.15
1	1	0	1	0.650	1.10
1	1	1	0	0.625	1.05
1	1	1	1	0.600	1.00

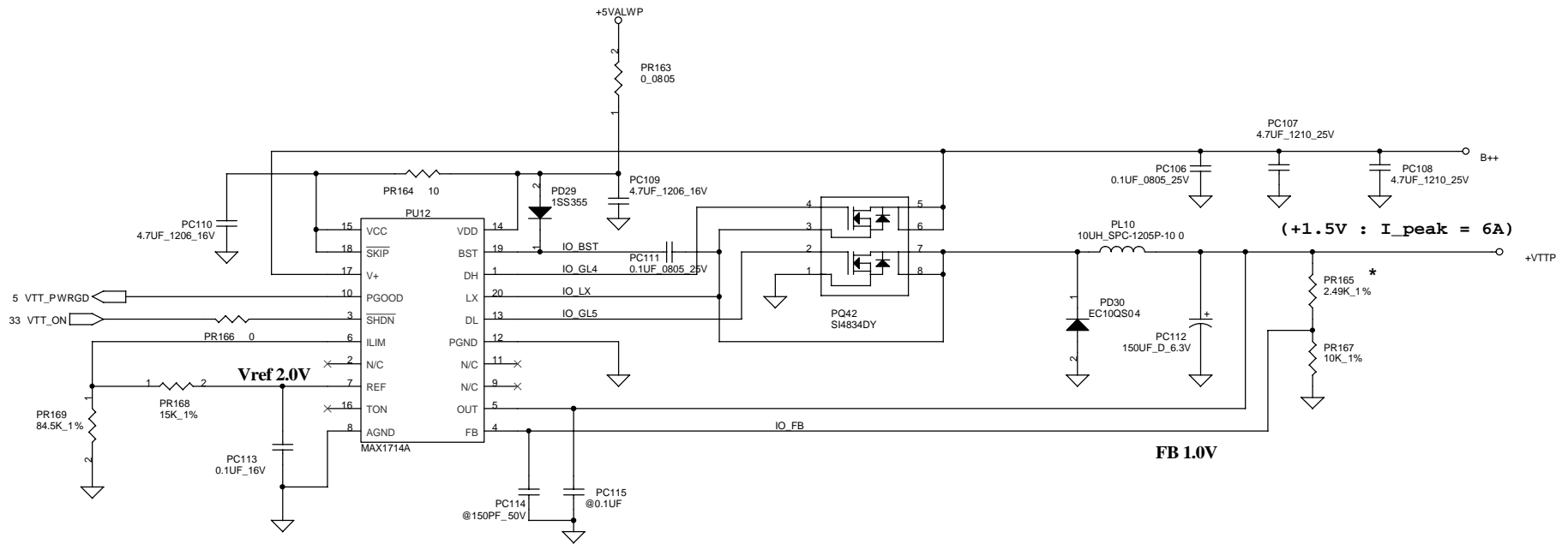
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Title: SCHEMATIC, M/B LA-1121

Size	Document Number	Rev
B	401191 (FOR ATW01)	1C

Date: 星期二, 十一月 27, 2001 Sheet 86 of 87



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