# LCFC Confidential

## AMD 2 Chip M/B Schematics Document

### AMD Kaveri Processor with DDR3L + Bolton FCH

### AMD GPU JET PRO/TOPAZ XT S3

**2013-09-25**

**REV:0.1**

| | | | |
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Title: *Cover Page*

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Date: Monday. December 16. 2013 | Sheet 1 of 52

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Title: **Block Diagram**

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Date: Monday, December 16, 2013 | Sheet 2 of 52

## Voltage Rails ( O --> Means ON , X --> Means OFF )

| power plane / State | B+ | +5VALW<br>+3VALW | +1.5V | +5VS<br>+3VS<br>+1.5VS<br>+VCCSA<br>+1.5s_VCCP<br>+CPU_CORE<br>+VGA_CORE<br>+GFX_CORE<br>+1.8VS<br>+1.05VS<br>+0.75VS<br>+3.3VS_VGA<br>+1.5VS_VGA<br>+1.05VS_VGA |
|---|---|---|---|---|
| S0 | O | O | O | O |
| S3 | O | O | O | X |
| S5 S4/AC Only | O | O | X | X |
| S5 S4/ Battery only | O | X | X | X |
| S5 S4/AC & Battery don't exist | X | X | X | X |

| STATE \ SIGNAL | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V | +VS | Clock |
|---|---|---|---|---|---|---|---|---|
| S0 (Full ON) | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S1 (Power On Suspend) | LOW | HIGH | HIGH | HIGH | ON | ON | ON | LOW |
| S3 (Suspend to RAM) | LOW | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | LOW | LOW | LOW | HIGH | ON | OFF | OFF | OFF |
| S5 (Soft OFF) | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF |

## USB Port Table

| USB 2.0 | USB 3.0 | | Port | 4 External USB Port |
|---|---|---|---|---|
| EHCI1 | xHCI | 1 | 0 | Camera |
| | | 2 | 1 | USB Port (Right Side) |
| | | 3 | 2 | USB Port (Left Side) |
| | | 4 | 3 | |
| | | | 4 | |
| | | | 5 | USB Port (Right Side) |
| | | | 6 | |
| | | | 7 | |
| EHCI2 | | | 8 | |
| | | | 9 | |
| | | | 10 | Mini Card (WLAN) |
| | | | 11 | |
| | | | 12 | |
| | | | 13 | Blue Tooth |

## BOM Structure Table

| BOM Structure | BTO Item |
|---|---|
| @ | Not stuff |
| 100M@ | 100M LAN part |
| 14@ | For 14" part |
| 15@ | For 15" part |
| AOAC@ | AOAC support part |
| GIGA@ | Giga LAN Part |
| JET@ | For AMD Jet GPU part |
| ME@ | ME Part (connector, hole) |
| DIS@ | Discrete GPU SKU part |
| UMA@ | UMA SKU part |
| TS@ | Touch Screen SKU part |
| TPOAZ@ | For AMD Topaz GPU part |
| A10@ | For AMD Kaveri A10 (19W)S IC KAVERI |
| A4@ | For AMD Kaveri A4 (17W)S IC KAVERI |
| EMC@ | EMC componets |

## SMBUS Control Table

| | SOURCE | Main VGA | 2nd VGA | BATT | IT8580E | SODIMM | WLAN WiMAX | Termal Sensor | PCH | CP Module |
|---|---|---|---|---|---|---|---|---|---|---|
| EC_SMB_CK1<br>EC_SMB_DA1 | IT8580E<br>+3VALW | X | X | V<br>+3VALW | X | X | X | X | X | X |
| EC_SMB_CK2<br>EC_SMB_DA2 | IT8580E<br>+3VS | V<br>+3VS | V<br>+3VS | X | X | X | X | V<br>+3VS | V<br>+3V_PCH | X |
| APU_SCLK<br>APU_SDATA | PCH<br>+3V_PCH | X | X | X | X | V<br>+3VS | V<br>+3VS | X | V<br>+3V_PCH | V<br>+3VS |

## PCIE PORT LIST

| Port | Device |
|---|---|
| 1 | LAN |
| 2 | WLAN |
| 3 | |
| 4 | |
| 5 | |
| 6 | |
| 7 | |
| 8 | |

## EC SM Bus1 address

| Device | Address |
|---|---|
| Smart Battery | 0001 011X b |

## EC SM Bus2 address

| Device | Address |
|---|---|
| Thermal Sensor EMC1403-2 | 1001 101X b |
| Master VGA | 0x9E |
| Slave VGA | 0x9C |

## APU SM Bus address

| Device | Address |
|---|---|
| DDR DIMM0 | 1001 000Xb |
| DDR DIMM1 | 1001 010Xb |

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Title: Notes List

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Date: Monday, December 16, 2013 | Sheet 3 of 52

## Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.

It is recommended that the 3.3-V rail ramp up first.

The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 µs before VDDC, VDDCI, and VMEMIO start to ramp up.

The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/µs).

For power down, reversing the ramp-up sequence is recommended.

## CONFIGURATION STRAPS

**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET**

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

| MLPS Bit | Strap Name | Description | RECOMMENDED SETTINGS |
|---|---|---|---|
| PS_0[1]<br>PS_0[2]<br>PS_0[3] | ROM_CONFIG[0]<br>ROM_CONFIG[1]<br>ROM_CONFIG[2] | Define the ROM type when STRAP_BIOS_ROM_EN = 1.<br>Define the primary memory-aperture size when STRAP_BIOS_ROM_EN = 0.<br>100 = 256MB | X |
| PS_0[4] | N/A | Reserved for internal use only. Must be 1 at reset. | 1 |
| PS_0[5] | AUD_PORT_CONN_<br>PINSTRAP[0] | The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs. | 1 |
| PS_1[1] | STRAP_BIF_GEN3_EN_A | 1 = PCIe GEN3 is supported.<br>0 = PCIe GEN3 is not supported. 0= Not support | X |
| PS_1[2] | STRAP_BIF_CLK_PM_EN | 0 = The CLKREQB power management capability is disabled<br>1 = The CLKREQB power management capability is enabled | 0 |
| PS_1[3] | N/A | Reserved for internal use only. Must be 0 at reset. | 0 |
| PS_1[4] | STRAP_TX_CFG_DRV_<br>FULL_SWING | 0 = The transmitter half-swing is enabled<br>1 = The transmitter full-swing is enabled | 1 |
| PS_1[5] | STRAP_TX_DEEMPH_EN | 0 = Tx deemphasis disabled.<br>1 = Tx deemphasis enabled. 1= Enable | X |
| PS_2[1] | N/A | Reserved. | 0 |
| PS_2[2] | N/A | Reserved. | 0 |
| PS_2[3] | STRAP_BIOS_ROM_EN | 0 = Disable the external BIOS ROM device.<br>1 = Enable the external BIOS ROM device. 0= Disable | X |
| PS_2[4] | STRAP_BIF_VGA_DIS | 0 = VGA controller capacity enabled.<br>1 = The device will not be recognized as the system's VGA controller. | 1 |
| PS_2[5] | N/A | Reserved | 1 |
| PS_3[1]<br>PS_3[2]<br>PS_3[3] | BOARD_CONFIG[0]<br>BOARD_CONFIG[1]<br>BOARD_CONFIG[2] | Board configuration related strapping, such as for memory ID<br>000 = Hynix 256M*16 001 = Hynix 128M*16<br>100 = Samsung 256M*16 011 = Samsung 128M*16<br>010 = Micron 256M*16 111 = Micron 128M*16 | X |
| PS_3[4]<br>PS_3[5] | AUD_PORT_CONN_<br>PINSTRAP[1]<br>AUD_PORT_CONN_<br>PINSTRAP[2] | Determines the maximum number of digital display audio endpoints that will be presented to the OS and user.(Combine with PS_0[5])<br>111 = No usable endpoints.<br>110 = One usable endpoint.<br>101 = Two usable endpoints. 111= No usable endpoints.<br>100 = Three usable endpoints.<br>011 = Four usable endpoints.<br>010 = Five usable endpoints.<br>001 = Six usable endpoints.<br>000 = All endpoints are usable. | 11 |

## VRAM ID config

| Memory Type | | VRAM ID PS_3[3:1] | PU resistor RV33 | PD resistor RV36 |
|---|---|---|---|---|
| 128Mx16 | Hynix H5TC2G63FFR-11C | 100 | 4.53K | 4.99K |
| | Micron MT41J128M16JT-093G | 111 | 4.75K | NC |
| | Samsung K4W2G1646Q-BC1A | 110 | 3.4K | 10K |
| 256Mx16 | Hynix H5TC4G63AFR-11C | 000 | NC | 4.75K |
| | Micron MT41J256M16HA-093G | 010 | 4.53K | 2K |
| | Samsung K4W4G1646D-BC1A | 001 | 8.45K | 2K |




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Title: APU PEG/PCIe/UMI

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Title: APU DDRA/B

Size: Custom | Document Number: ACLU7 | Rev: 1.A

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Title: APU Msic

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Date: Monday, December 16, 2013 | Sheet 7 of 52

22u 6.3V *11 @*2 Design Guide
0.22u 10V *2
0.01u 10V *3
180p *3

22u 6.3V *10 @*2 Design Guide
0.22u 10V *3
180p 10V *4

22u 6.3V *3
0.22u 10V *2
180p 10V *2

22u 6.3V *4
0.22u 10V *2
180p 10V *2

4.7u 6.3V *1
0.22u 10V *1
3.3n 10V *1

3.3n need apply PN

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Title: **APU Power**

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Title: APU GND

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Date: Monday, December 16, 2013 | Sheet 9 of 52

# DDR3 SO-DIMM A

# DDR Decoupling

**1uF *4, 10uF *7, 330uF *1**

**Layout Note :**
1. Placed near JDDR3L
2. Place these 4 Caps near Command and Control signals of DIMMA

**Layout Note : Placed near JDDR3L1.Pin203, 204**

**All VREF traces should have 20 mil trace width**

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Title: **DDR3 SO-DIMMA/1**

Size: Custom | Document Number: ACLU7 | Rev: 0.4

Date: Monday, December 16, 2013 | Sheet 10 of 52

# DDR3 SO-DIMM B

## DDR Decoupling

**1uF *4, 10uF *7, 330uF *1**

**Layout Note :**
1. Placed near JDDR3H
2. Place these 4 Caps near Command and Control signals of DIMMA

**Layout Note : Placed near JDDR3H.Pin203, 204**

**CRB: DDRB_SA1 pull low / DDRB_SA0 pull high**
**Edge: DDRB_SA1 pull high / DDRB_SA0 pull low**

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Title: **DDR3 SO-DIMMB/2**

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Date: Monday, December 16, 2013 | Sheet 11 of 52

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Title: FCH PCIe/PCI/LPC/APU/S5+

Size: Custom | Document Number: ACLU7 | Rev: 1.A

Date: Monday, December 16, 2013 | Sheet 12 of 52

Add table on 2013 1001

| BOARD ID Config. | SKU ID | Function | PANEL ID | Function |
|---|---|---|---|---|
| | 0 | UMA@ | 0 | 14@ |
| | 1 | DIS@ | 1 | 15@ |

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Title: FCH SATA/GBE/SPI

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Date: Monday, December 16, 2013 | Sheet 13 of 52

Delete Security EEPROM USROM3 ,unused

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Size: Custom | Document Number: ACLU7 | Rev: 1.A

Date: Monday, December 16, 2013 | Sheet 14 of 52

| | |
|---|---|
| +3VALW | +VDDAN_33_HWM,+VDDAN_33_USB_S,VDDPL_33_SSUSB_S,+VDDPL_33_USB_S |
| +3VS | +VDDPL_33_SATA,+VDDPL_33_PCIE,+VDDPL_33_SYS |
| +1.1VALW | +VDDCR_11_SSUSB_S,+VDDAN_11_SSUSB_S,+VDDAN_11_USB_S, +VDDAN_11_USB_S,+VDDCR_1.1V_USB |
| +1.1VS | +VDDCR_11,+VDDAN_11_CLK,+VDDAN_11_PCIE,+VDDAN_11_SATA, |

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Title: FCH POWER/GND

Size: Custom | Document Number: ACLU7 | Rev: 1.A

Date: Monday, December 16, 2013 | Sheet 15 of 52

## STRAP PINS

| | PCI_CLK1 | PCI_CLK3 | PCI_CLK4 | CLK_PCI_EC | LPC_CLK1 | EC_PWM2 | RTC_CLK |
|---|---|---|---|---|---|---|---|
| PULL HIGH | ALLOW PCIE GEN2 DEFAULT | USE DEBUG STRAPS | NON_FUSION CLOCK MODE | EC ENABLED | CLKGEN ENABLED DEFAULT | LPC ROM | S5 PLUS MODE DISABLED |
| PULL LOW | FORCE PCIE GEN1 | IGNORE DEBUG STRAP DEFAULT | FUSION CLOCK MODE DEFAULT | EC DISABLED DEFAULT | CLKGEN DISABLE | SPI ROM DEFAULT | S5 PLUS MODE ENABLED DEFAULT |

## DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

| | PCI_AD27 | PCI_AD26 | PCI_AD25 | PCI_AD24 | PCI_AD23 |
|---|---|---|---|---|---|
| PULL HIGH | USE PCI PLL DEFAULT | DISABLE ILA AUTORUN DEFAULT | USE FC PLL DEFAULT | USE DEFAULT PCIE STRAPS DEFAULT | DISABLE PCI MEM BOOT DEFAULT |
| PULL LOW | BYPASS PCI PLL | ENABLE ILA AUTORUN | BYPASS FC PLL | USE EEPROM PCIE STRAPS | ENABLE PCI MEM BOOT |

need confirm AD26

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Date: Monday, December 16, 2013 | Sheet 16 of 52

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Title: Topaz & Jet PCIE

Size: Custom | Document Number: ACLU7 | Rev: 1.A

Date: Monday, December 16, 2013 | Sheet 17 of 65

| SVC (GPIO20) | SVD (GPIO15) | Boot Voltage |
|---|---|---|
| 0 | 0 | 1.1V |
| 0 | 1 | 1.0V |
| 1 | 0 | 0.9V(Default) |
| 1 | 1 | 0.8V |

| | Bits5 | Bits4 | Bits3 | Bits2 | Bits1 |
|---|---|---|---|---|---|
| PS0 | 1 | 1 | 0 | 0 | 1 |
| PS1 | 1 | 1 | 0 | 0 | 0 |
| PS2 | 0 | 0 | 0 | 0 | 0 |
| PS3 | 1 | 1 | ? | ? | ? |

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Title: Topaz & Jet GPIO

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Date: Monday, December 16, 2013 | Sheet 18 of 65

| Security Classification | LC Future Center Secret Data | | |
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Title: *Topaz & Jet Core Power*

Size: Custom | Document Number: ACLU7 | Rev: 1.A

Date: Monday, December 16, 2013 | Sheet 19 of 65

| ASIC Ball | Topaz | Jet |
|---|---|---|
| U10,T10<br>AB13,W9<br>AB11,AB12<br>AC11,AC13<br>AC14,Y9,W10 | VDDC | NC |
| AC20 | FB_VDDC | NC |
| AD20 | FB_VSS | NC |
| W1 | FB_VDDCI | NC |
| W3 | FB_VSS | NC |
| AJ11 | GPIO_SVC | NC_SVI2 |
| AK12 | GPIO_SVD | NC_SVI2 |
| AL11 | GPIO_SVT | NC_SVI2 |
| N6 | GPIO_11 | NC_GPIO11 |
| N5 | GPIO_12 | NC_GPIO12 |
| N3 | GPIO_13 | NC_GPIO13 |
| AJ27 | WAKEB | NC_VSYNC |
| T8 | PCC/GPIO_6 | GPIO_6 |
| AA3 | PLL_ANALOG_OUT | NC |
| AA1 | PLL_ANALOG_IN | NC |

| ASIC Ball | Topaz | Jet |
|---|---|---|
| U1 | BP_0 | NC |
| U3 | BP_1 | NC |
| AM26 | DIECRACKMON | NC |
| Y11 | NC | DBG_DATA13 |
| AE9 | NC | DBG_DATA14 |
| L9 | NC | DBG_DATA15 |
| N9 | NC | DBG_DATA16 |
| AE8 | NC | DBG_DATA12 |
| AL9 | NC | DBG_CNTL0 |
| H13,H16,H19,J10<br>J23,J24,J9,K10<br>K23,K24,K9,L11<br>L12,L13,L20,L21<br>L22 | VMEMIO | VDDR1 |
| AA17,AA18<br>AB17,AB18 | VDD_GPIO33 | VDDR3 |
| AA20,AA21<br>AB20,AB21 | VDD_GPIO18 | VDD_CT |

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Title: *Topaz & Jet DP Power/GND*

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|---|---|---|
| Custom | ACLU7 | 1.A |

Date: Monday, December 16, 2013 | Sheet 20 of 65

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Title: *Topaz & Jet MEM Interface*

Size: C | Document Number: ACLU7 | Rev: 1.A

Date: Monday, December 16, 2013 | Sheet 21 of 65

# Memory Partition A - Lower 32 bits

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Title: *Topaz & Jet DDR3 VRAM U*

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Date: Monday, December 16, 2013 | Sheet 22 of 65

# Memory Partition A - Upper 32 bits

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Title: Topaz & Jet DDR3 VRAM L

Size: Custom | Document Number: ACLU7 | Rev: 1.A

Date: Monday, December 16, 2013 | Sheet 23 of 65

## +0.95VS to +0.95VS_VGA

Reserve for GPU/APU share +0.95V

+/- 1.5%

+/- 3% 2A

AON4304
VDS=30V VGS=20V, ID=18A,
Rds=6mohm @ VGS=10V
VGS(th)=2.4V Max

7m OHM is requried ???

AON6414AL
VDS=30V VGS=20V, ID=50A,
Rds=8mohm @ VGS=10V
VGS(th)=2.5V Max

Add 1.35VP to _+1.35VS_VGA on 20130925, RDS on less than 8,need to check, 4A for totally

## +1.35VP TO +1.35VS_VGA

Need OPEN

Check if QV46 need to replaced by LP2301ALT1G_SOT23-3 .

## +1.8VS to +1.8VS_VGA

Reserve for GPU/APU share +1.8V

+/- 2%

+/- 3% 0.5A

36m OHM is requried

AON6414AL
VDS=30V VGS=20V, ID=50A,
Rds=8mohm @ VGS=10V
VGS(th)=2.5V Max

## +3VS to +3VS_VGA

Need OPEN

## GPU Power Discharger

reserve RV167 change to 10 ohm to meet power off sequence on 1202

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Title: Topaz & Jet SWITCH POWER

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Date: Monday, December 16, 2013 | Sheet 24 of 65

# BLANK

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Title

*Topaz & Jet BLANK*

| Size | Document Number | Rev |
|---|---|---|
| Custom | *ACLU7* | 0.4 |

Date: Monday, December 16, 2013 Sheet 25 of 65

## Board ID

| BOARD_ID0 | BOARD_ID1 | BOARD_ID2 | BOARD_ID3 | Description | Stuff Resistor |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | BDW + Jet-LE sku | RC107,RC108,RC109,RC123 |
| 0 | 0 | 1 | 0 | BDW + Topaz-XT sku | RC107,RC108,RC102,RC123 |
| 0 | 1 | 0 | 0 | BDW + N15V-GM sku | RC107,RC101,RC109,RC123 |
| 0 | 1 | 1 | 0 | BDW + N15S-GT sku | RC107,RC101,RC102,RC123 |
| * 1 | 0 | 0 | 0 | HSW + Jet-LE sku | RC100,RC108,RC109,RC123 |
| 1 | 0 | 1 | 0 | HSW + Topaz-XT sku | RC100,RC108,RC102,RC123 |
| 1 | 1 | 0 | 0 | HSW + N15V-GM sku | RC100,RC101,RC109,RC123 |
| 1 | 1 | 1 | 0 | HSW + N15S-GT sku | RC100,RC101,RC102,RC123 |
| 0 | 0 | 0 | 1 | BDW + UMA sku | RC107,RC108,RC109,RC121 |
| 1 | 0 | 0 | 1 | HSW + UMA sku | RC100,RC108,RC109,RC121 |


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Title: Virtual Symbol

Size: C | Document Number: ACLU7 | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 26 of 52

## LCD POWER CIRCUIT

## LED POWER

## CMOS Camera

## Touch Screen

## Touch Screen reserved

Touch Screen

## eDP Conn

add Pull down R14 100k on EC_BKOFF#

## EMI request

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Title: eDP/ CMOS/Touch screen

Size: C | Document Number: ACLU7 | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 27 of 52

***+CRT_VCC_CON and +5VS_HDMI trace width 100 mils***

***For ESD***

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Title: **HDMI_CONN**

Size: Custom | Document Number: ACLU7 | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 28 of 52

# CRT Connector

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Title: CRT_CONN

Size: Custom | Document Number: ACLU7 | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 29 of 52

## ON/OFF switch

## Power Button

*ON/OFF switch*

*Reserved SW5 for debug on 20130926*

## K/B Connector

## TP/B Connector

| For 14" | | For 15" | |
|---|---|---|---|
| 1 | VDD | 1 | VDD |
| 2 | CLK | 2 | CLK |
| 3 | DAT | 3 | DAT |
| 4 | GND | 4 | GND |
| 5 | TP-L | 5 | TP-L |
| 6 | TP-R | 6 | TP-R |

*For 14"*

*For 15"*

## USB I/O Connector

## PWR/B Connector

## Right Side USB2.0 Port X 1 (USB/B)

## LED

*Add LED4,LED5,LED6 for 15"*

*Delete JLED1 on due to both G14 and G15 move LED to MB*

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Title: KBD/PWR/IO/LED/TP Conn

Size: Custom | Document Number: ACL07 | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 30 of 52

# LEFT SIDE USB3.0 PORT X2

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Title: USB 3.0 PORT (LEFT)

Size: Custom | Document Number: ACLU7 | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 31 of 52

# SATA HDD Conn.

# FOR 14" SATA ODD Conn.

# FOR 15" SATA ODD FFC Conn

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Title: HDD/ODD CONN

Size: Custom | Document Number: ACLU7 | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 32 of 52

# Mini-Express Card(WLAN/WiMAX)

Connect CLKREQ_WLAN# and WLAN_CLKREQ_Q# directly and reserve Q11 on 20131004

Change R67 power rail from 3VS to +3VS_WLAN on 20131011

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Title: NGFF-Card / SSD

Size: C | Document Number: ACLU7 | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 33 of 52

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Title: Codec_CX20752

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Date: Monday, December 16, 2013 | Sheet 34 of 52

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Title: LAN_RTL8106E/8111G

Size: Custom | Document Number: ACLU7 | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 35 of 52

# DL1/DL2
# 1'S PN:SC300003M00

Place Close to TL1

Place Close to TL2

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Title: **LAN_Transformer**

Size: B | Document Number: ACLU7 | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 36 of 52

## SMSC thermal sensor placed near DIMM

**Address 1001_101xb**

**REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:**
**Trace width/space:10/10 mil**
**Trace length:<8"**

## *FAN Conn*

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Title: *Thermal sensor/FAN CONN*

Size: Custom | Document Number: ACLU7 | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 37 of 52

## Add Board ID ,please check with Edge

| Vcc | 3.3V +/- 5% | | | | |
|---|---|---|---|---|---|
| RE33 | 100K +/- 1% | | | | |
| Board ID | RE34 | $V_{AD_BID}$ min | $V_{AD_BID}$ typ | $V_{AD_BID}$ max | Phase |
| 0 | 0K +/- 5% | 0 V | 0 V | 0 V | SDV |
| 1 | 8.2K +/- 5% | 0.216 V | 0.250 V | 0.289 V | |
| 2 | 18K +/- 5% | 0.436 V | 0.503 V | 0.538 V | |
| 3 | 33K +/- 5% | 0.712 V | 0.819 V | 0.875 V | |
| 4 | 4.7K +/- 5% | 0.141 V | 0.148 V | 0.155 V | |
| 5 | 24K +/- 5% | 0.612 V | 0.638 V | 0.664 V | |

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Title: EC ITE8586LQFP

Size: Custom | Document Number: AQU7 | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 38 of 52

## Load Switch
## +5VALW To +5VS
## +3VALW To +3VS

**+5VS, C159 --> 1.5ms**
**+3VS, C160 --> 2.5ms**

*VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=18mohm*

**R164 and R165 to adjust 3VALW and 5VALW timing**

***Delete +3VALW To +3VALW_FCH on 20131001***

## Load Switch
## +1.1VALW to +1.1VS

**1.1VS :4A**

**Update Load Switch +1.1VALW to +1.1VS to AON6414AL on 20130926**

***From FCH***

## +VDDIO to +VDDIO_RUN

## For DisCharge

**Short +1.35V_DDR_VDDIOSUS & +1.35V_APU_VDDIO directly on 20130930**

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Title: **DC V TO VS INTERFACE**

Size: C | Document Number: ACLU7 | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 39 of 52

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Title: SCREW

Size: Custom | Document Number: ACLU7 | Rev: 1.A

Date: Monday, December 16, 2013 | Sheet 40 of 52

# AMD Kaveri Platform
## System power on G3 --> S5 --> So

G3
1.+RTCBATT

S5
2.+VIN
3.B+
4.+3VL/+VL
5.ACPRN (BTY Charger to EC)
6.EC_ON (EC to Power IC)
7.FCH_S5 (FCH to EC)
8.S5_1.1_EN (EC to Power IC)
9.+5VALW/+3VALW/+1.1VALW
10.EC_RSMRST# (EC to FCH)

S0
11.ON/OFFBTN# (PBTN to EC)
12.PBTN_OUT# (EC to FCH)
13.PM_SLP_S5# (FCH to EC)
14.PM_SLP_S3# (FCH to EC)
15.SYSON (EC to Power IC)
16.+1.35VS/+0.675VS
17.SUSP# (EC to Power IC)
18.+3VS/+5VS
18.+1.5VS
18.+1.1VS
18.+1.8VS
19.VDDAPWROK (Power IC to EC)
20.APUPWR_EN (EC to VRM)
21.+0.95VS
21.+VDD_VORE/+VDDNB_VORE
22.IMVPPOK (VRM to EC)
23.FCH_PWROK (EC to FCH)
24.APU_PWROK (FCH to APU)
25.PLT_RST (FCH to APU)
26.APU_RESET (FCH to APU)

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Title: Power sequence block

Size: D | Document Number: ACL07 | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 41 of 52

| | | | |
|---|---|---|---|
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Title

*Virtual symbol*

| | | |
|---|---|---|
| Size B | Document Number ACLU7 | Rev 0.1 |
| Date: Monday, December 16, 2013 | Sheet 42 of 52 | |

***PH1 under CPU botten side :***
***CPU thermal protection at 92+-3 degree C***
***Recovery at 56 +-3 degree C***

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Title: ***DCIN / RTC***

Size: Custom | Document Number: G(AMD Beema) | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 43 of 43

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Title: **BATTERY CONN/OTP**

Size: Custom | Document Number: G(AMD Beema) | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 44 of 44

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Title: CHARGER

Size: C | Document Number: G(AMD Beema) | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 45 of 45

| Security Classification | LC Future Center Secret Data | | |
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Title: PWR_3VALW/5VALW

Size: C | Document Number: G(AMD Beema) | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 46 of 46

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Title: +1.35VP/+0.675VSP

Size: Custom | Document Number: AAVE1 | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 47 of 47

Current limit setting pin. The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high respectively.

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Title: +1.35VS_VGA/+1.5VS

Size: C | Document Number: G(AMD Beema) | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 48 of 48

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Title: *+1.1VALWP*

Size: B | Document Number: AAVE1 | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 49 of 49

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Title: +1.05VS/+1.05VS_VGA

Size: B | Document Number: G(AMD Beema) | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 50 of 50

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Title: +VGA_CORE

Size: Custom | Document Number: G(AMD Beema) | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 51 of 51

| SVC | SVD | Boot Voltage |
|---|---|---|
| 0 | 0 | 1.1V |
| 0 | 1 | 1.0V(Default) |
| 1 | 0 | 0.9V |
| 1 | 1 | 0.8V |

| Security Classification | LC Future Center Secret Data | | |
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Title: PWR_CPU Core

Size: D | Document Number: ACL117 | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 52 of 52

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Title: VCCCPUCORE DECOUPLING

Size: B | Document Number: AAVE1 | Rev: 0.1

Date: Monday, December 16, 2013 | Sheet 53 of 53