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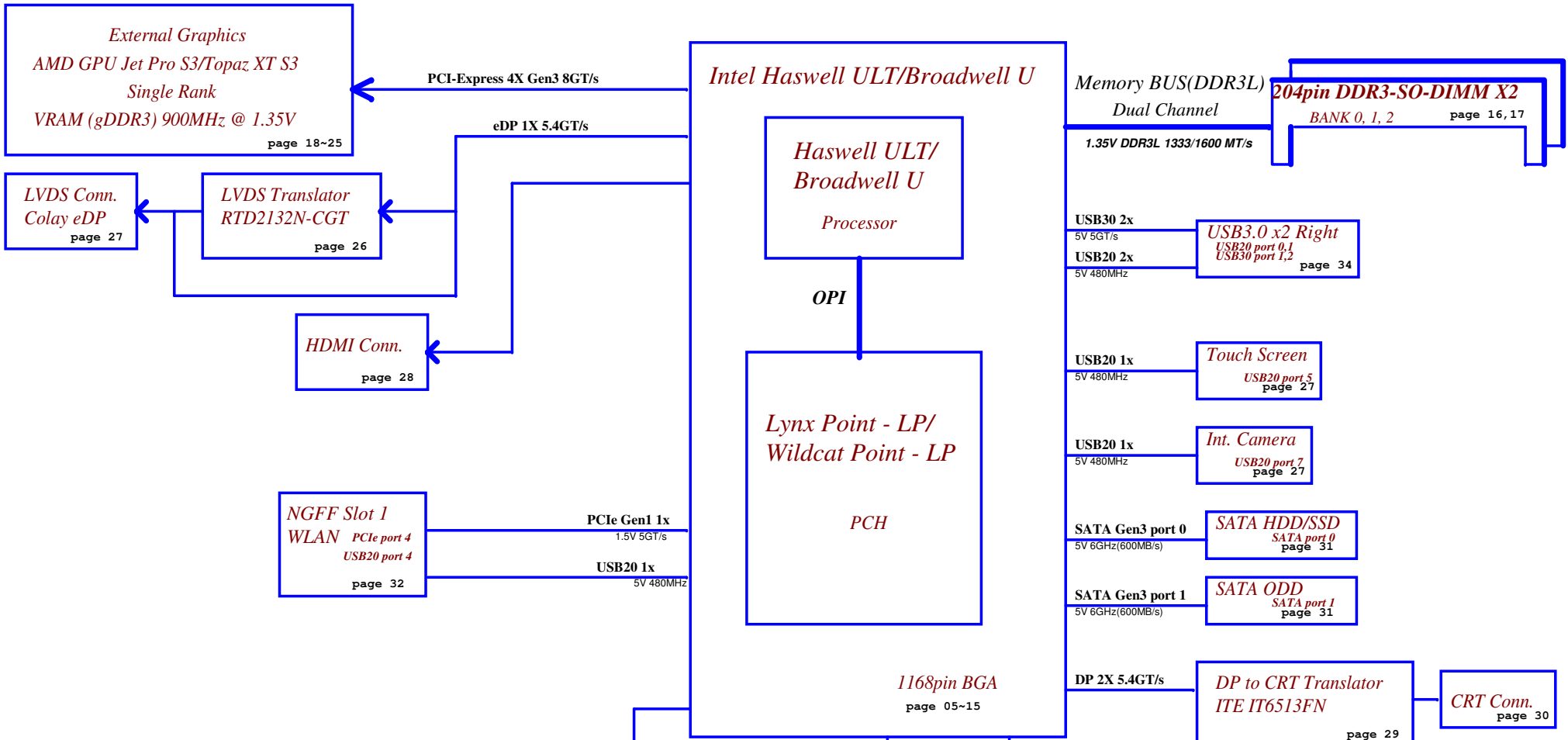
ZSWAA/ZCWAA Schematics Document

Intel Haswell ULT/Broadwell U with DDR3L
 AMD GPU Jet Pro/Topaz XT S3 (Single Rank)

LA-B301P REV 1.0 Schematic

Intel Processor (Haswell ULT/Broadwell U)
 2014-02-10 Rev 1.0

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<small>Date:</small> Monday, February 10, 2014				<small>Sheet</small> 1 of 52	

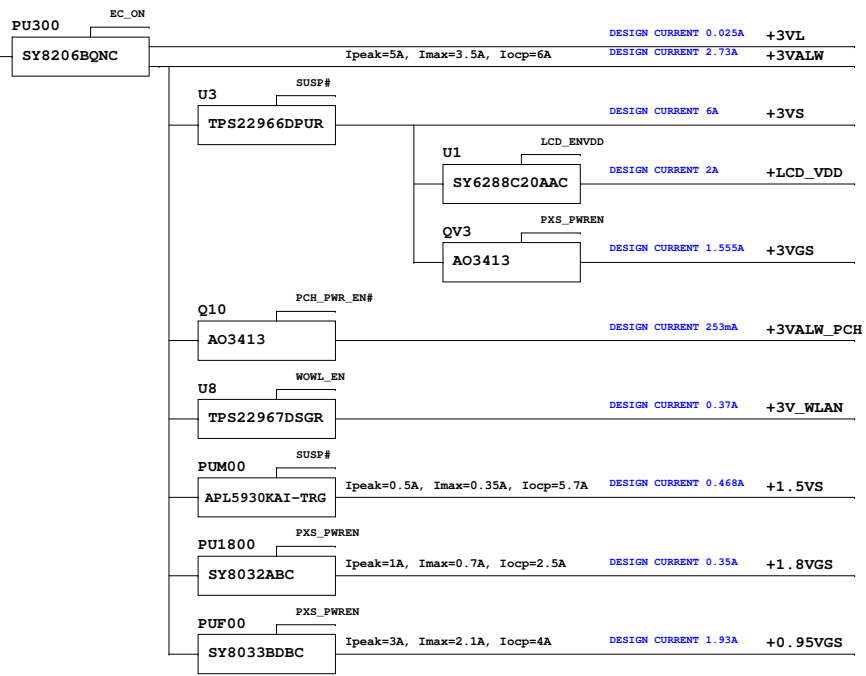
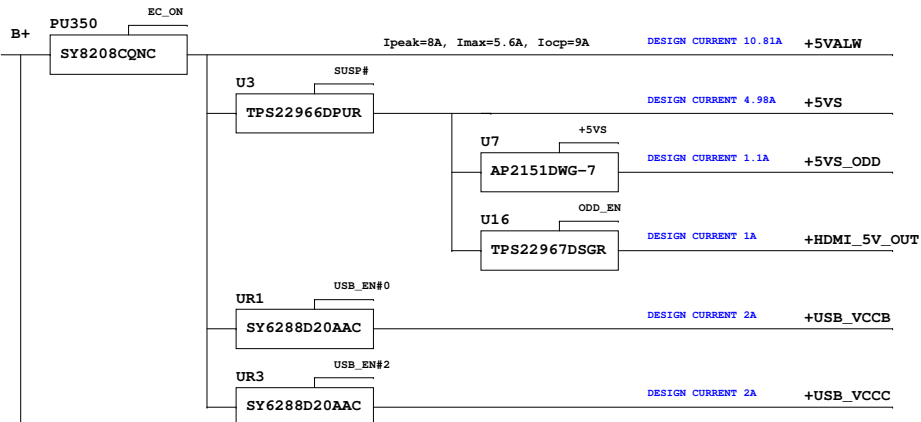


Sub Boards

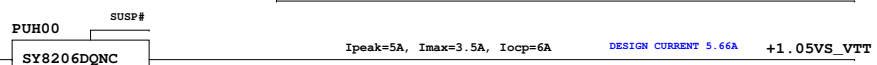
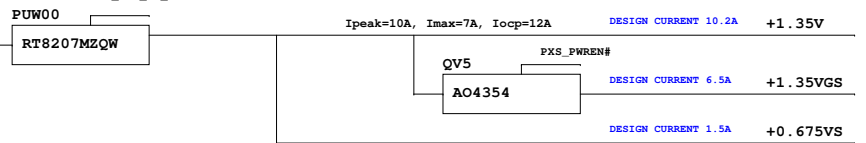
- LS-B301P LED/B page 37
- LS-B302P Power Button/B page 37
- LS-B303P LAN+USB/B Audio Combo Jack page 33
- LS-B304P CardReader/TP/LID B page 37

- RTC CKT. page 7
- DC/DC Interface CKT. page 38
- Power Circuit DC/DC page 39~48
- Power On/Off CKT. page 37

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SYSON: Enable 1.35V
DDR_VTT_PG_CTRL: Enable 0.675VS



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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +1.5VALW	+1.35V	+5VS +3VS +1.5VS +CPU_CORE +VGA_CORE +3VGS +1.8VGS +1.35VGS +0.95VGS +1.05VS_VTT
State						
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	Smart Charger	12 H	0001 0010 b

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VGS	AMD GPU	9E H	1001 1010 b

Power	Device	HEX	Address
-------	--------	-----	---------

Platform	SKU	CPU	PCH	VGA
Intel SharkBay ULT	UMA DIS	Haswell-M ULT Processor	Lynx Point - LP	AMD GPU Jet Pro S3 Topaz XT S3

BTO Option Table

Function	SKU		Processor		GPU		VRAM	Internal Panel		HDMI	Wake On Wireless	
Description	UMA	DIS	HASWELL	BROADWELL	JET	TOPAZ	X76	LVDS	eDP	HDMI	WOWL	NON-WOWL
Explain	UMA	DIS	HASWELL	BROADWELL	JET	TOPAZ	X76	LVDS	eDP	HDMI	WOWL	NON-WOWL
BTO	UMA@	VGA@	HASWELL@	BROADWELL@	JET@	TOPAZ@	X76@	LVDS@	IEDP@	HDMI@	ISCT@	NOISCT@

Function	CPU (R1 PN)					
Description	I3-4005U	I5-4200U	I3-4010U	2990U	I5-4210U	I3-4015U
Explain	SA000072Q70	SA00006SM80	SA00006SXA0	SA00007LM00	SA00007L000	SA00007LN00
BTO	4005UR1@	4200UR1@	4010UR1@	2990UR1@	4210UR1@	4015UR1@

Function	CPU (R3 PN)		
Description	I3-4005U	I5-4200U	I3-4010U
Explain	SA000072Q60	SA00006SM90	SA00006SX90
BTO	4005UR3@	4200UR3@	4010UR3@

Function	ODD		XDP	FIX	Short pad	ESD
Description	ZPODD	Non-ZPODD	XDP	FIX	Short pad	ESD
Explain	Zero Power ODD	Non-Zero Power ODD	XDP	FIX	0 ohm short pad	ESD
BTO	ZPODD@	NONZP@	XDP@	FIX@	Rshort@	ESD@ @ESD@

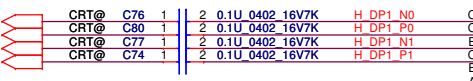
Function	EMI		CAM_EMI		CRT_EMI		TPM_EMI		TOUCH_EMI	
Description	EMI		CAM_EMI		CRT_EMI		TPM_EMI		TOUCH_EMI	
Explain	EMI		CAM_EMI		CRT_EMI		TPM_EMI		TOUCH_EMI	
BTO	EMI@	@EMI@	CAM_EMI@	@CAM_EMI@	CRT_EMI@	@CRT_EMI@	TPM_EMI@	@TPM_EMI@	TOUCH_EMI@	@TOUCH_EMI@

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

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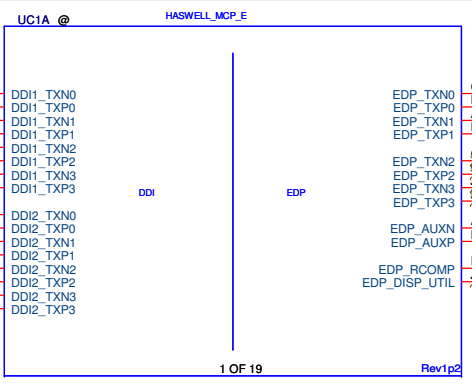
DP to CRT

<29> H_DP1_C_N0
<29> H_DP1_C_P0
<29> H_DP1_C_N1
<29> H_DP1_C_P1



HDMI

<28> H_HDMI_TX2-
<28> H_HDMI_TX2+
<28> H_HDMI_TX1-
<28> H_HDMI_TX1+
<28> H_HDMI_TX0-
<28> H_HDMI_TX0+
<28> H_HDMI_TXC-
<28> H_HDMI_TXC+



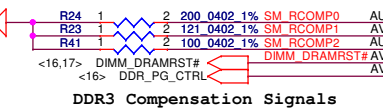
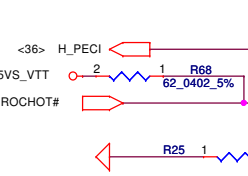
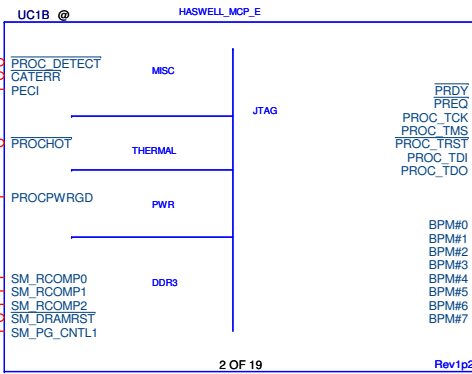
C45 H_EDP_TXN0 <26>
B46 H_EDP_TXP0 <26>
A47 H_EDP_TXN1 <26>
B47 H_EDP_TXP1 <26>

A45 H_EDP_AUXN <26>
B45 H_EDP_AUXP <26>

D20 EDP_COMP R1 1 2 24.9 0402 1% +VCCIOA_OUT
A43

Trace width=20 mils,Spacing=25mil,Max length=100mils

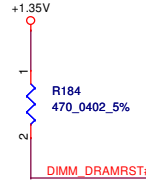
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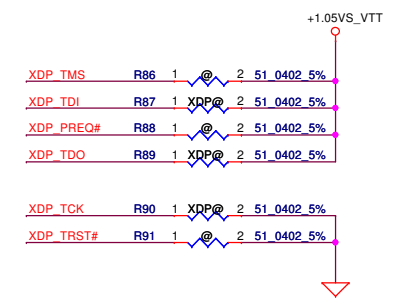
DDR3 Compensation Signals

J62 XDP_PRDY# @ T154
K62 XDP_PREQ#
E60 XDP_TCK
E61 XDP_TMS
E59 XDP_TRST#
F63 XDP_TDI
F62 XDP_TDO

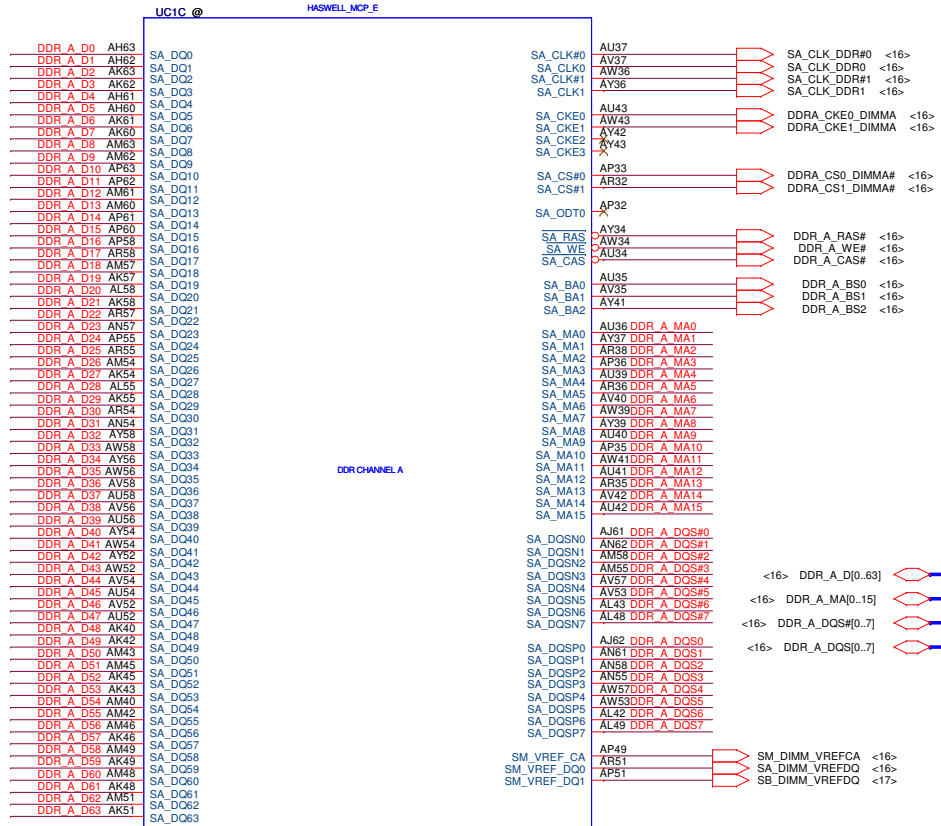
BPM#0 @ T155
H60 BPM#1 @ T156
H61 BPM#2 @ T148
H62 BPM#3 @ T149
K59 BPM#4 @ T150
H63 BPM#5 @ T151
K60 BPM#6 @ T152
J61 BPM#7 @ T153



PU/PD for JTAG signals



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DDR CHANNEL A

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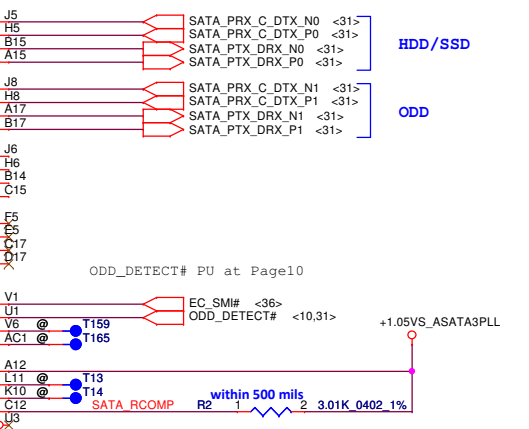
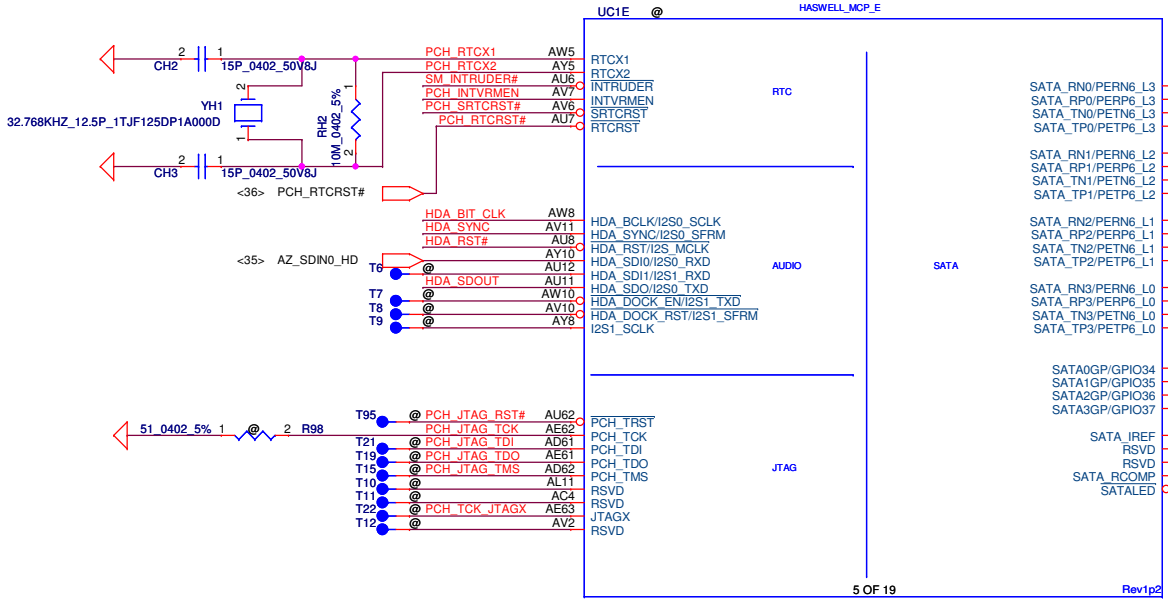
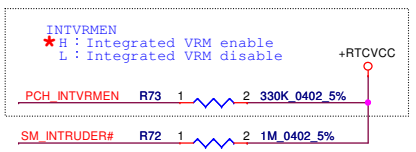
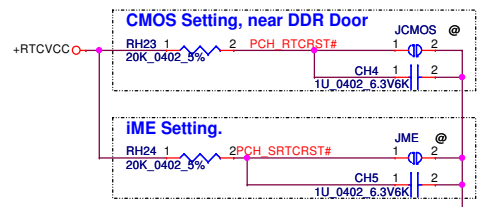


DDR CHANNEL B

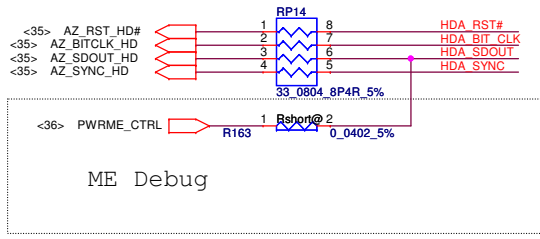
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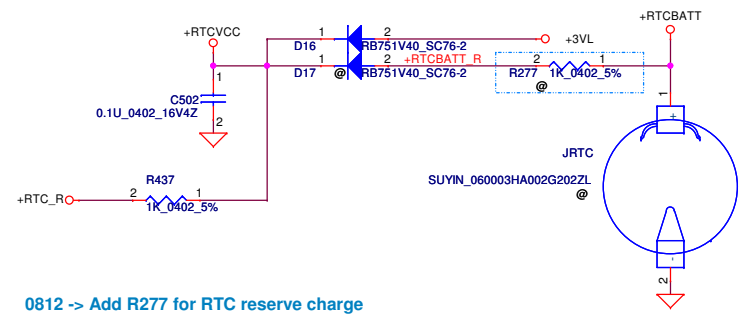
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HDA for AUDIO

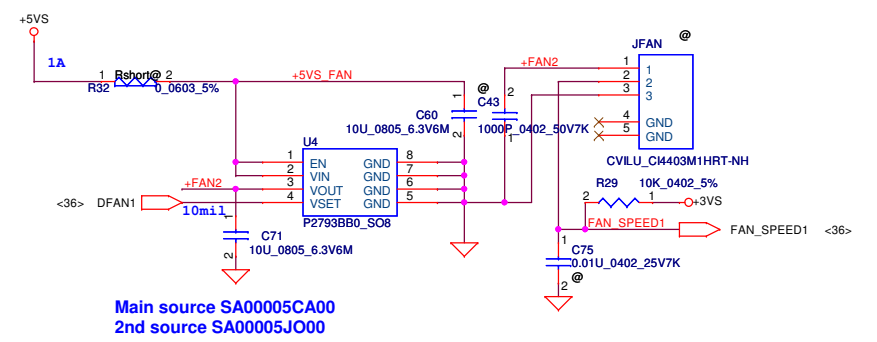


RTC schematic for non-chargeable



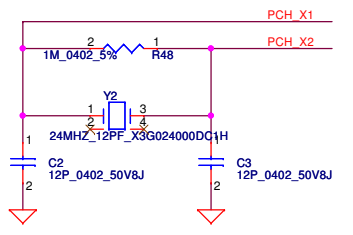
0812 -> Add R277 for RTC reserve charge
 Change D16, D17 P/N from SCS0340L010 to SCS00003500 for X code.

FAN Control Circuit



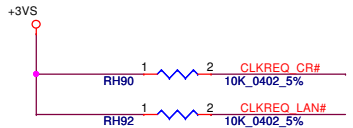
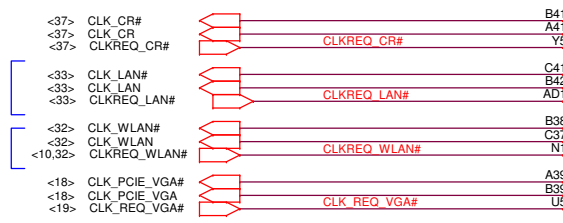
Main source SA00005CA00
 2nd source SA00005JO00

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					HSW MCP(3/11) RTC,SATA,XDP
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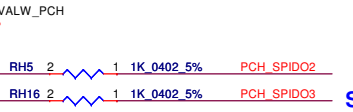
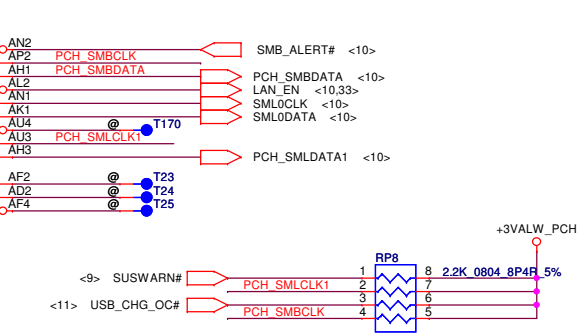
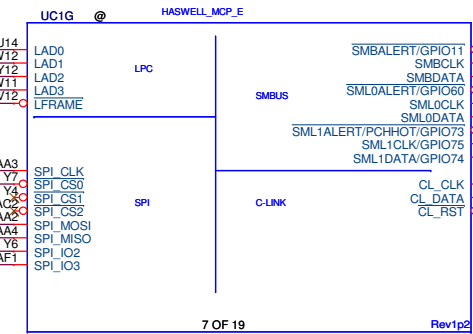
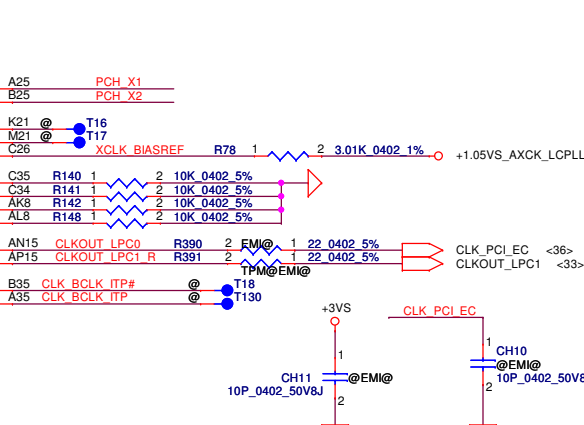
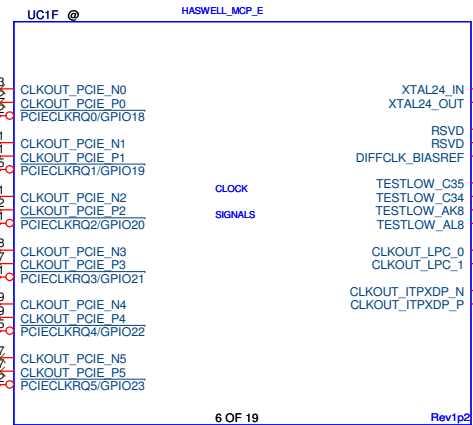
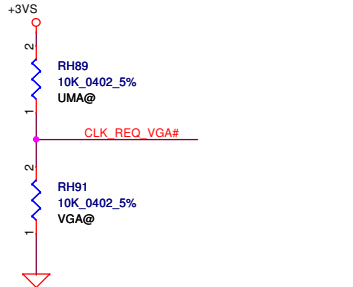


PCIE LAN

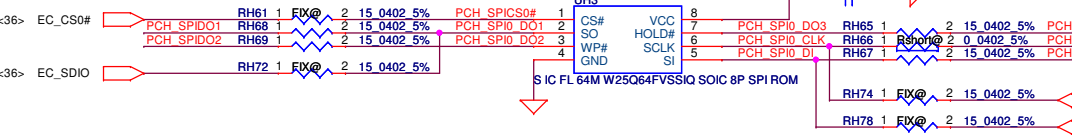
WLAN



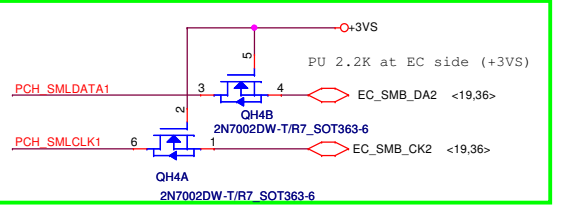
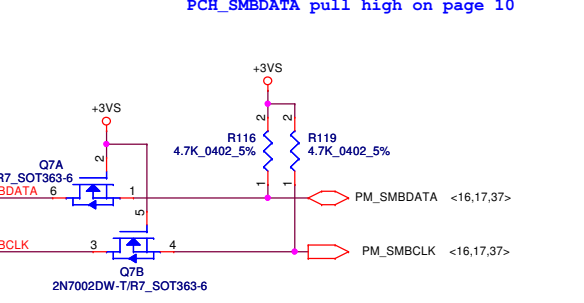
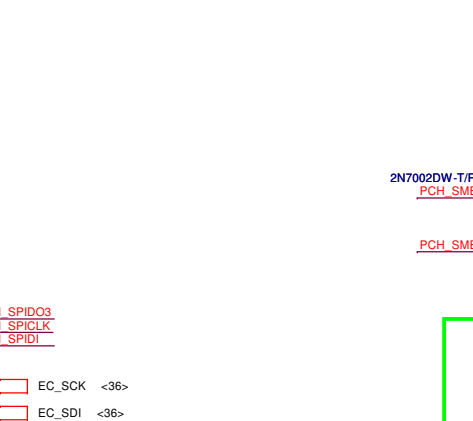
CLKREQ_WLAN# pull high on page 10



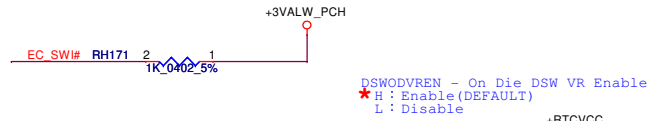
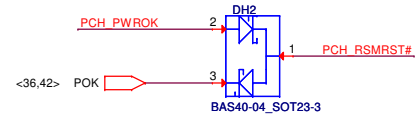
SPI ROM for BIOS & ME & Win8 (8MByte)



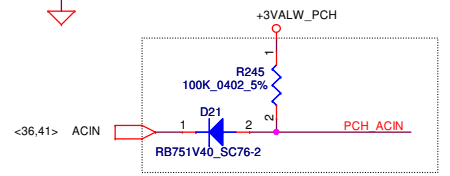
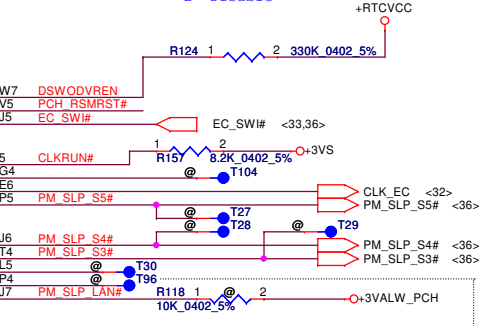
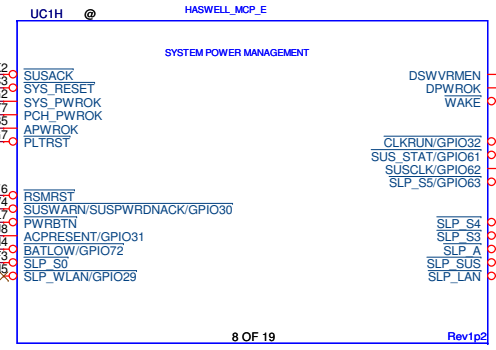
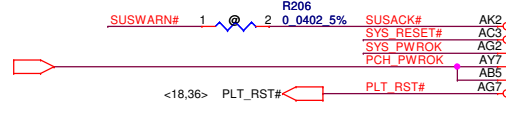
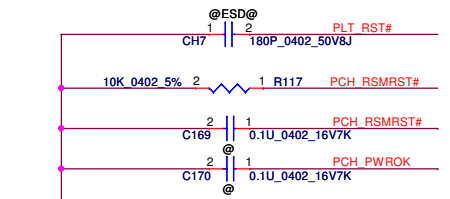
Please place UH3 close to U1 CPU, Please place RH66, RH67, RH68 near UH3



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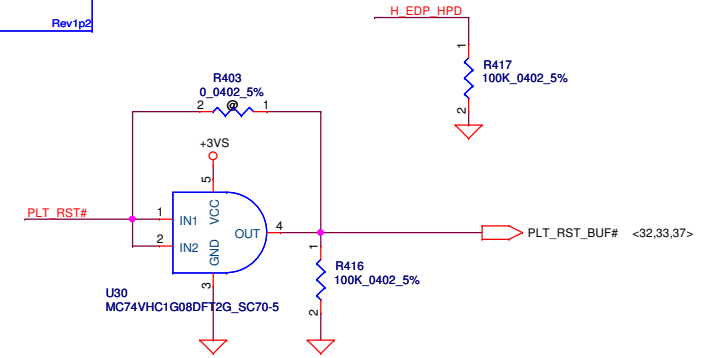
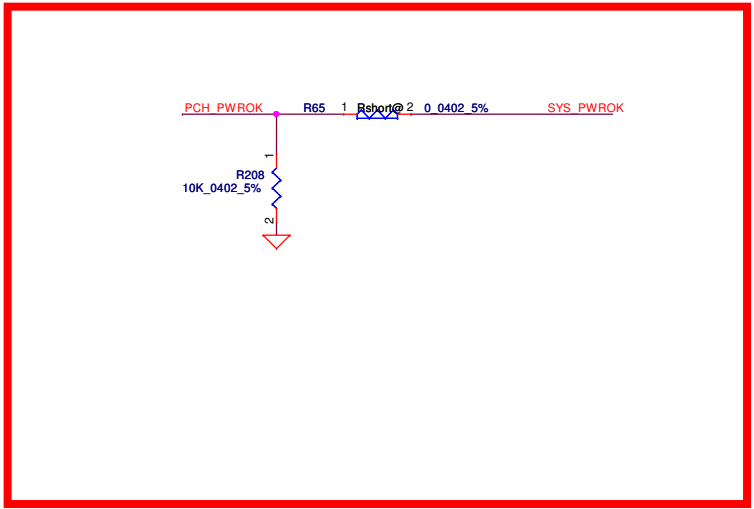
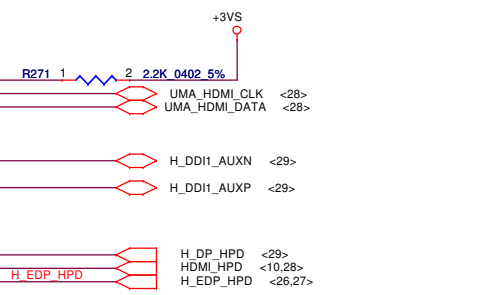
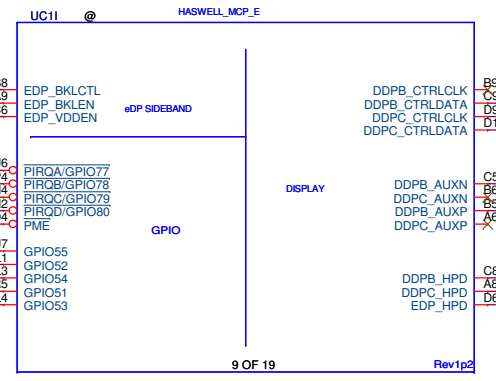
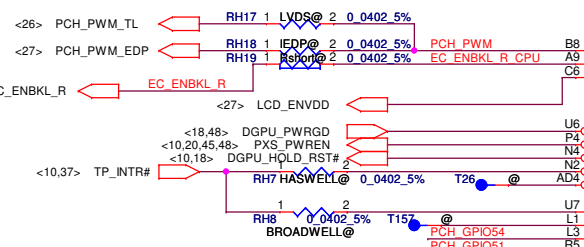
DSWODVREN - On Die DSW VR Enable
 * H : Enable (DEFAULT)
 L : Disable



Note for PCH_ACIN: Deep Sx need use EC GPIO for ACPRESENT function

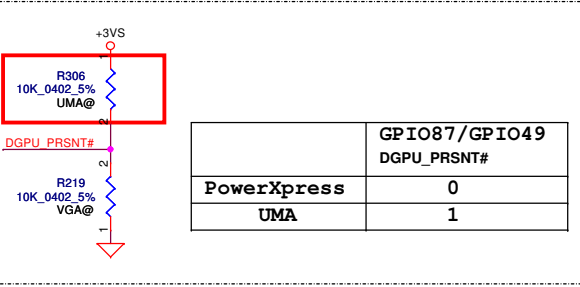
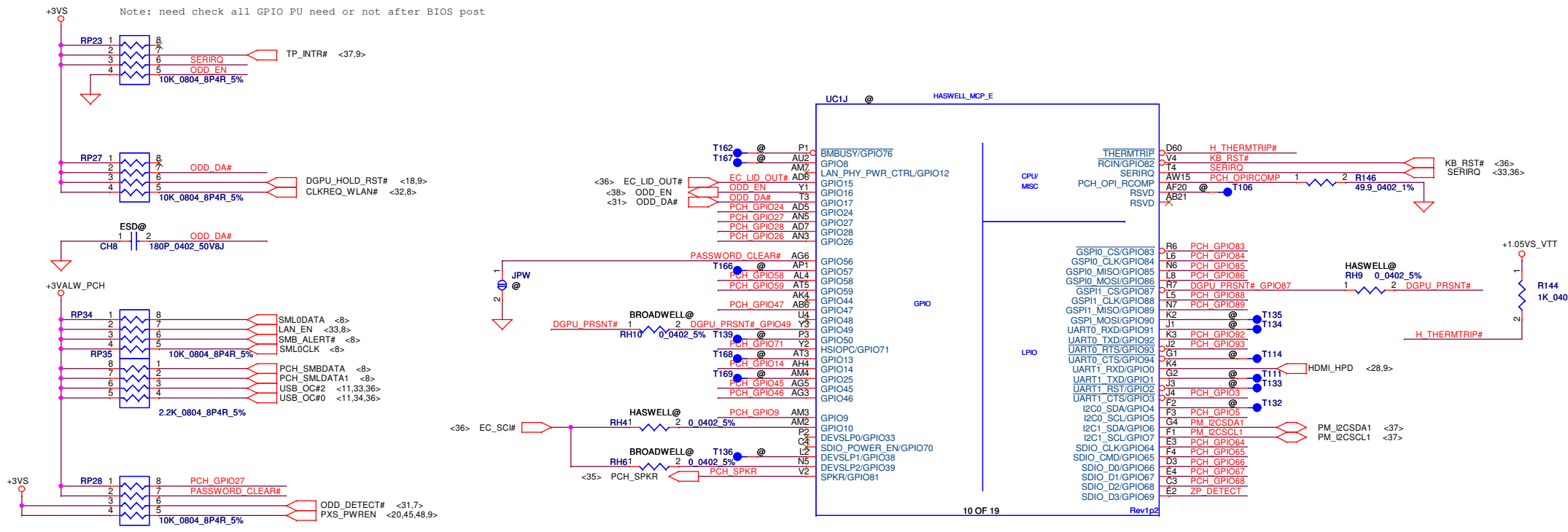
Change D21 P/N from SCS0340L010 to SCS00003500 for X code.

DDPB_CTRLCLK: Port B Detected
 DDPB_CTRLDATA: Port C Detected
 * 1: Port B or C is detected
 0: Port B or C is not detected
 (Have internal PD)

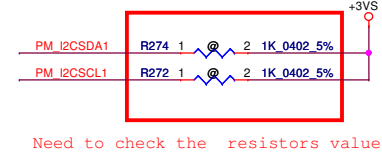
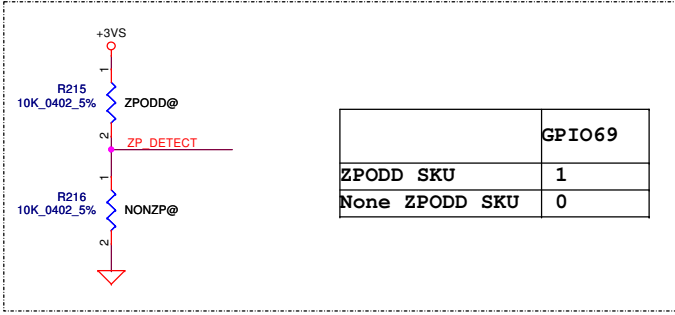


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Date				Sheet 9 of 52	

Note: need check all GPIO PU need or not after BIOS post

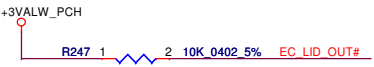


	GPIO88
TOUCH SKU	0
None TOUCH SKU	1



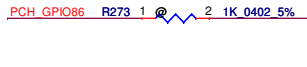
SPKR / GPIO81 : NO REBOOT

1: ENABLED
* 0: DISABLED (Have internal PD)



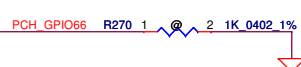
GPIO15 : TLS Confidentiality

1: Intel ME TLS with confidentiality
* 0: Intel ME TLS with no confidentiality (Have internal PD)



GSPI0_MOSI / GPIO86 : Boot BIOS Strap

1: ENABLED
* 0: SPI ROM (Have internal PD)

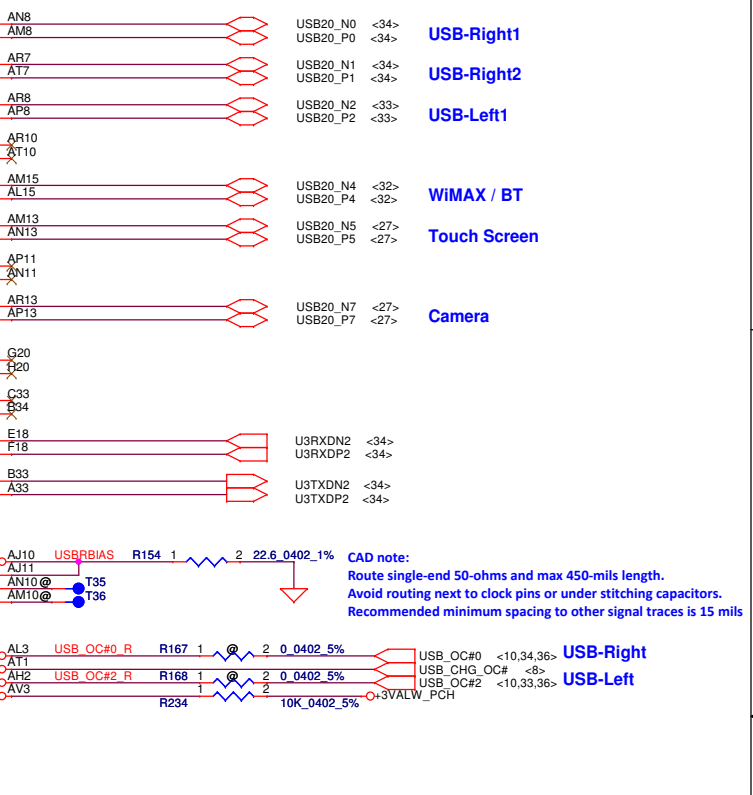
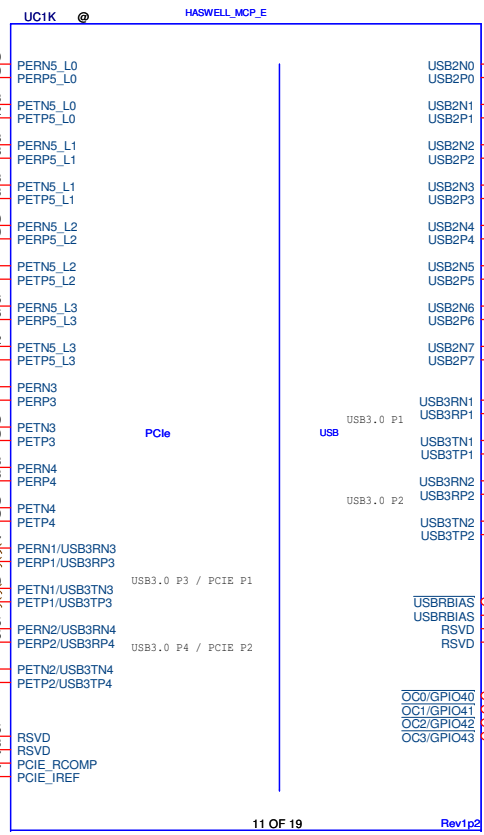
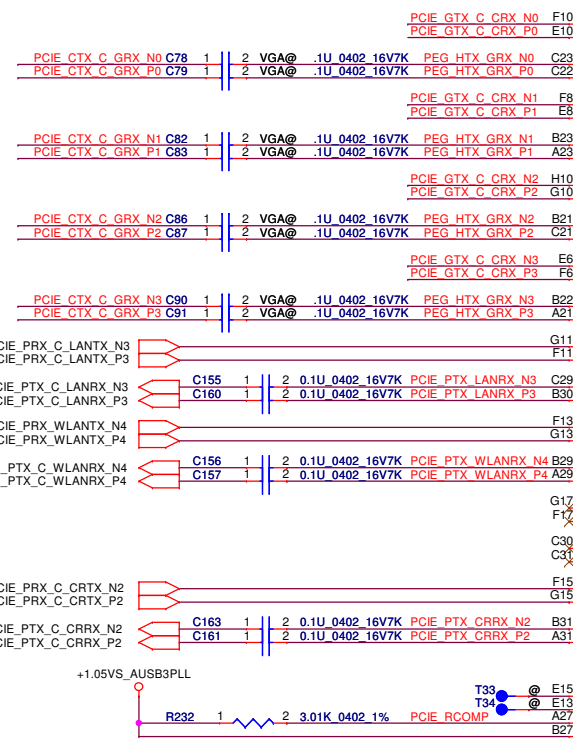
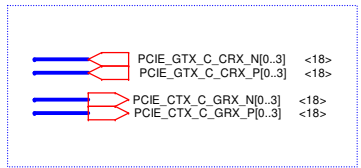


SDIO_D0 / GPIO66 : Top-Block Swap Override

* 1: ENABLED (Have internal PU)
0: DISABLED

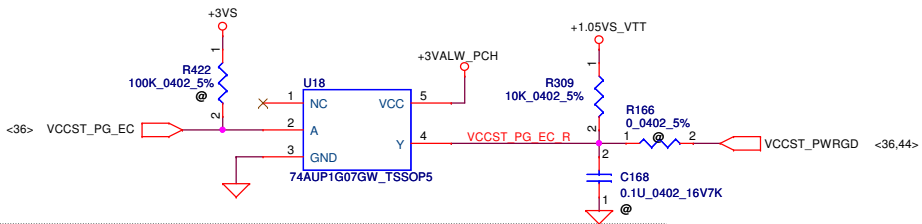
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Issued Date	2013/09/25	Deciphered Date
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Compal Electronics, Inc. HSW MCP(6/11) GPIO,LPIO		
Title	Document Number	Rev
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Date:	Monday, February 10, 2014	Sheet 10 of 52



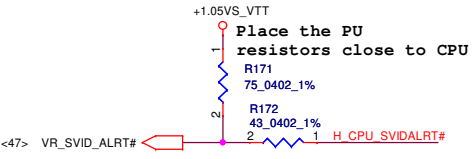
CAD note:
Route single-end 50-ohms and max 450-mils length.
Avoid routing next to clock pins or under stitching capacitors.
Recommended minimum spacing to other signal traces is 15 mils

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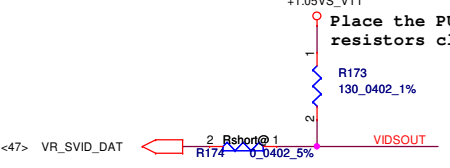
SVID ALERT

Place the PU resistors close to CPU

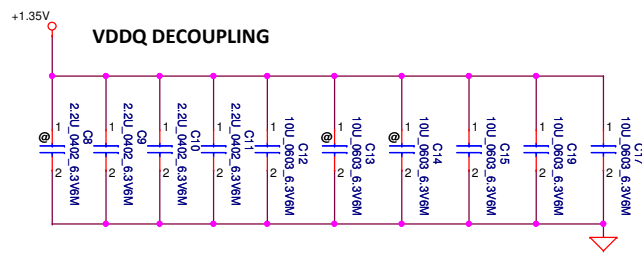
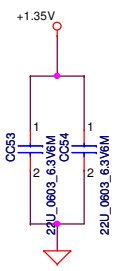
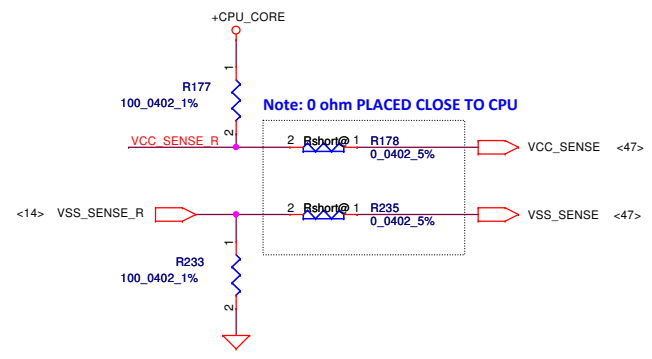


SVID DATA

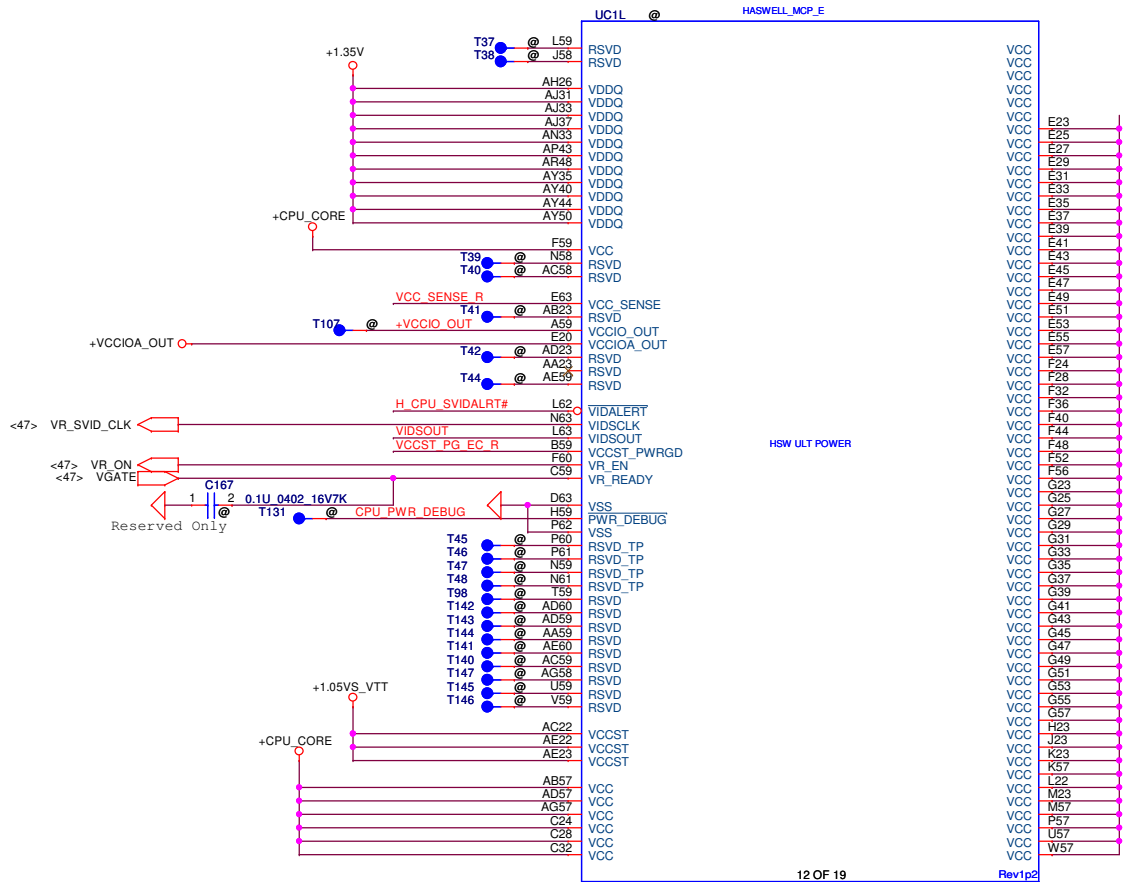
Place the PU resistors close to CPU



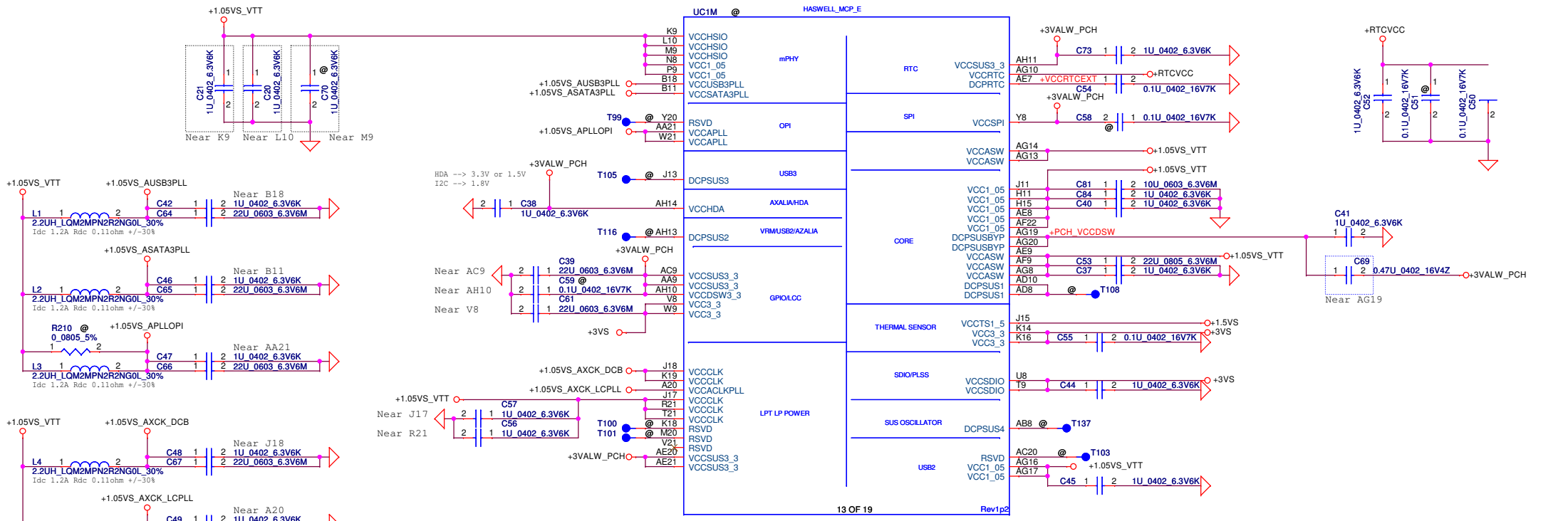
Note: 0 ohm PLACED CLOSE TO CPU



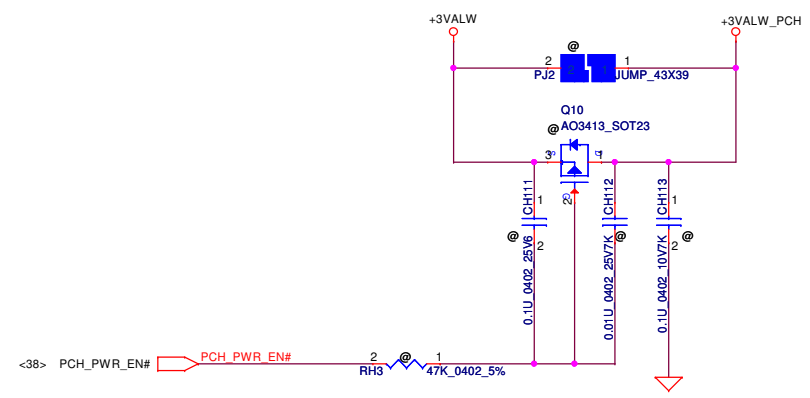
+1.35V : 470UF/2V/7343 *2
 10UF/6.3V/0603 * 6
 2.2UF/6.3V/0402 * 4



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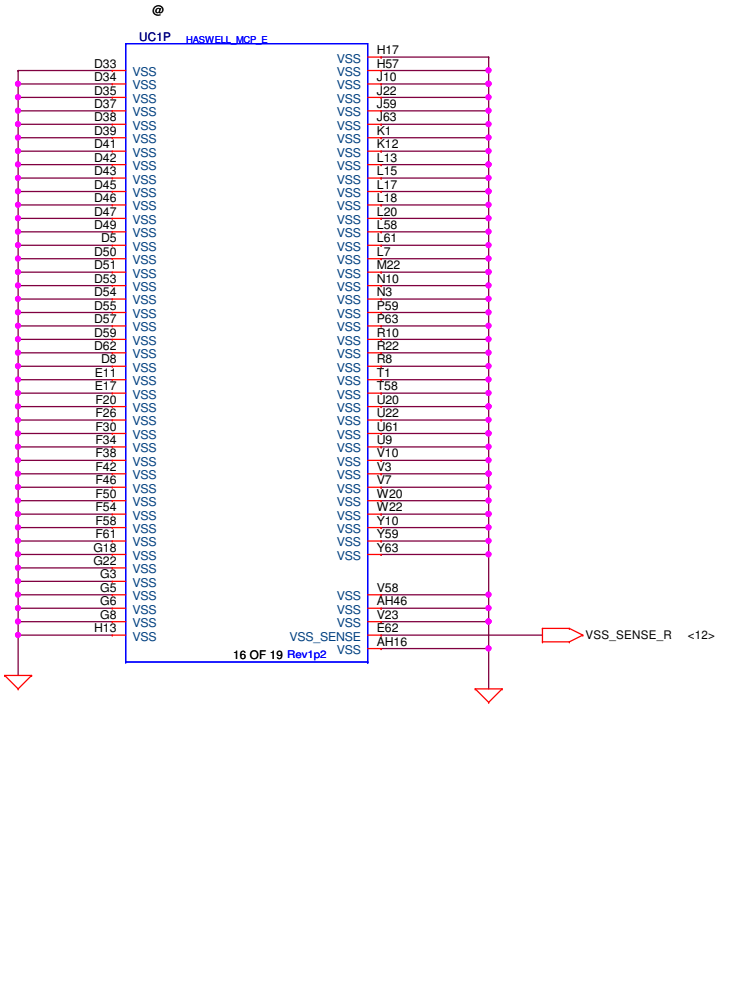
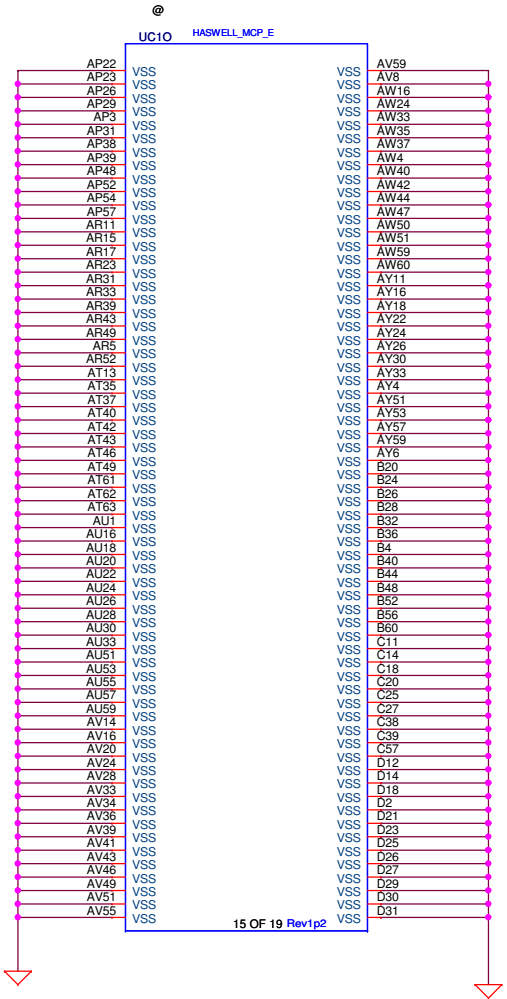
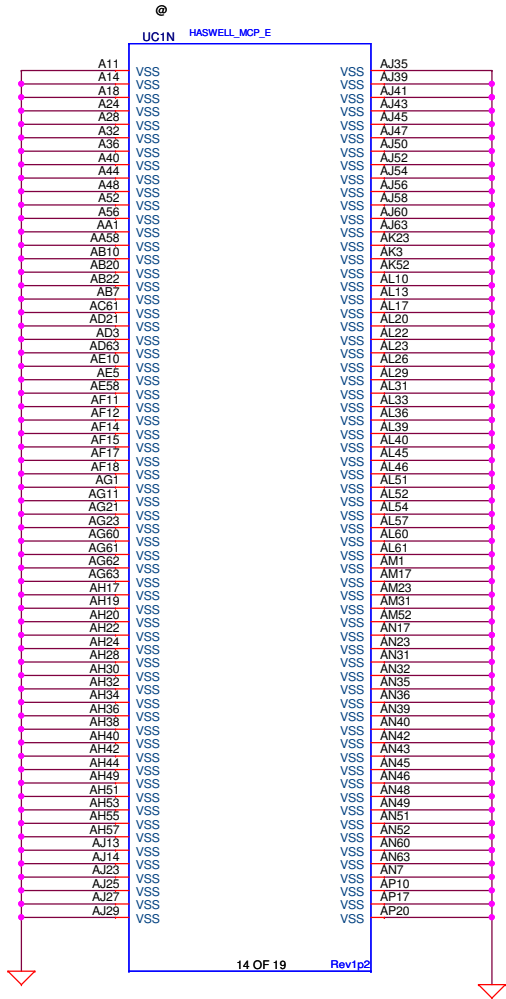
+3VALW to +3VALW_PCH



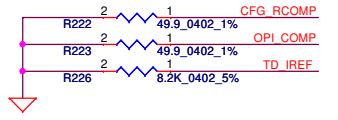
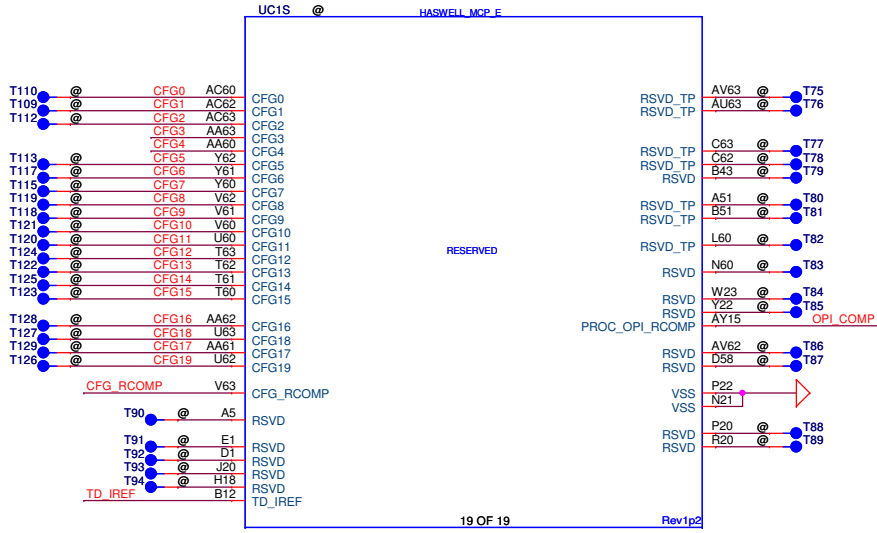
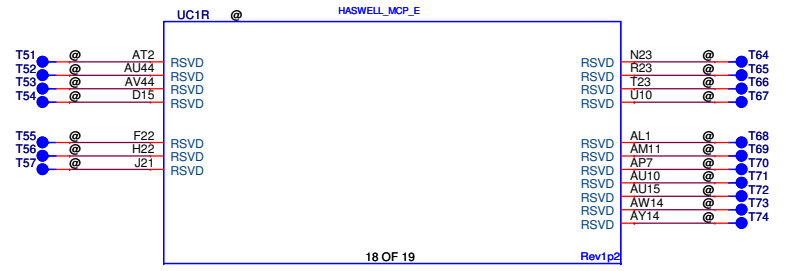
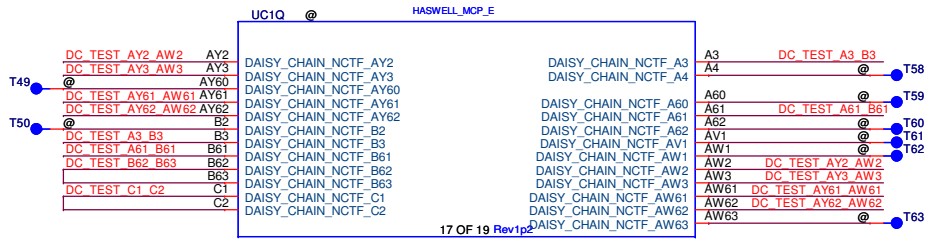
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Compal Electronics, Inc.
HSW MCP(9/11) Power

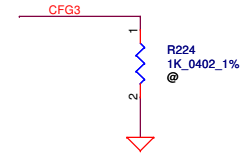
Rev 1.0



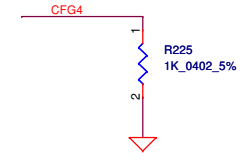
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					HSW MCP(10/11) GND
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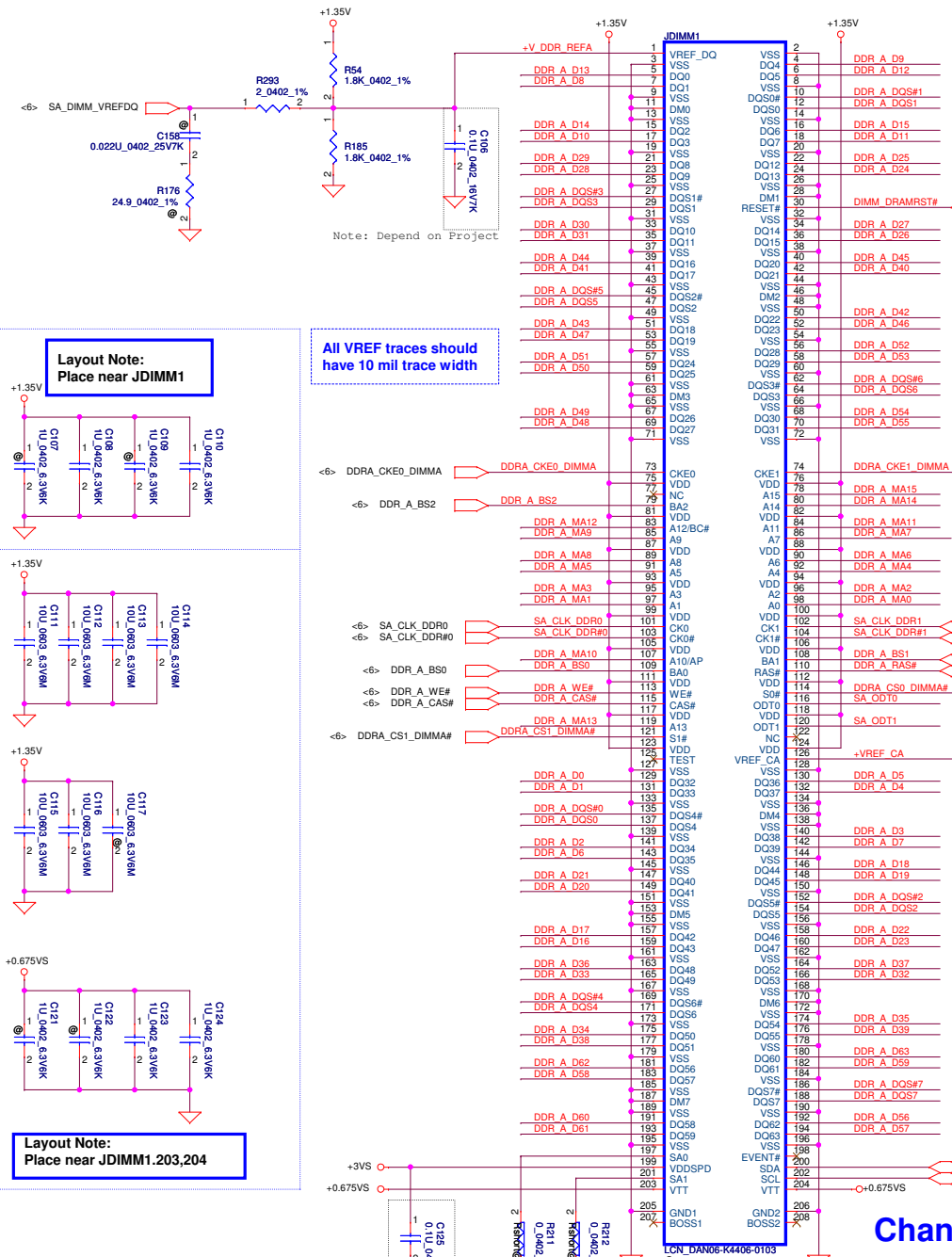
CFG Straps for Processor



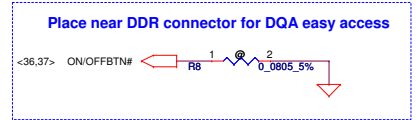
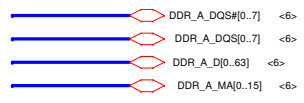
Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port



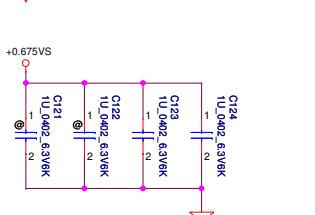
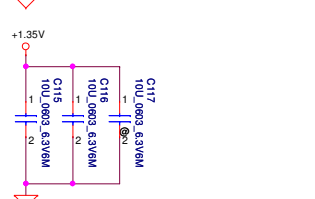
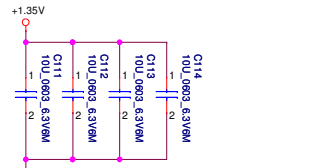
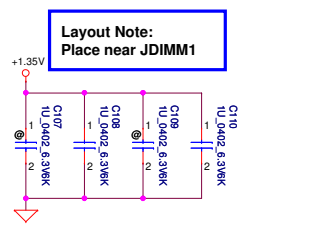
DDR3 SO-DIMM A Reverse Type H=4.0mm



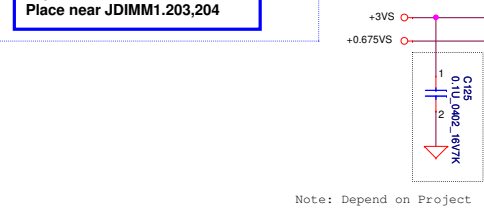
Layout Note:
Place near JDIMM1

All VREF traces should have 10 mil trace width

Place near DDR connector for DQA easy access



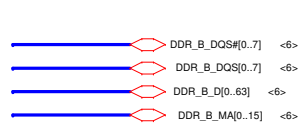
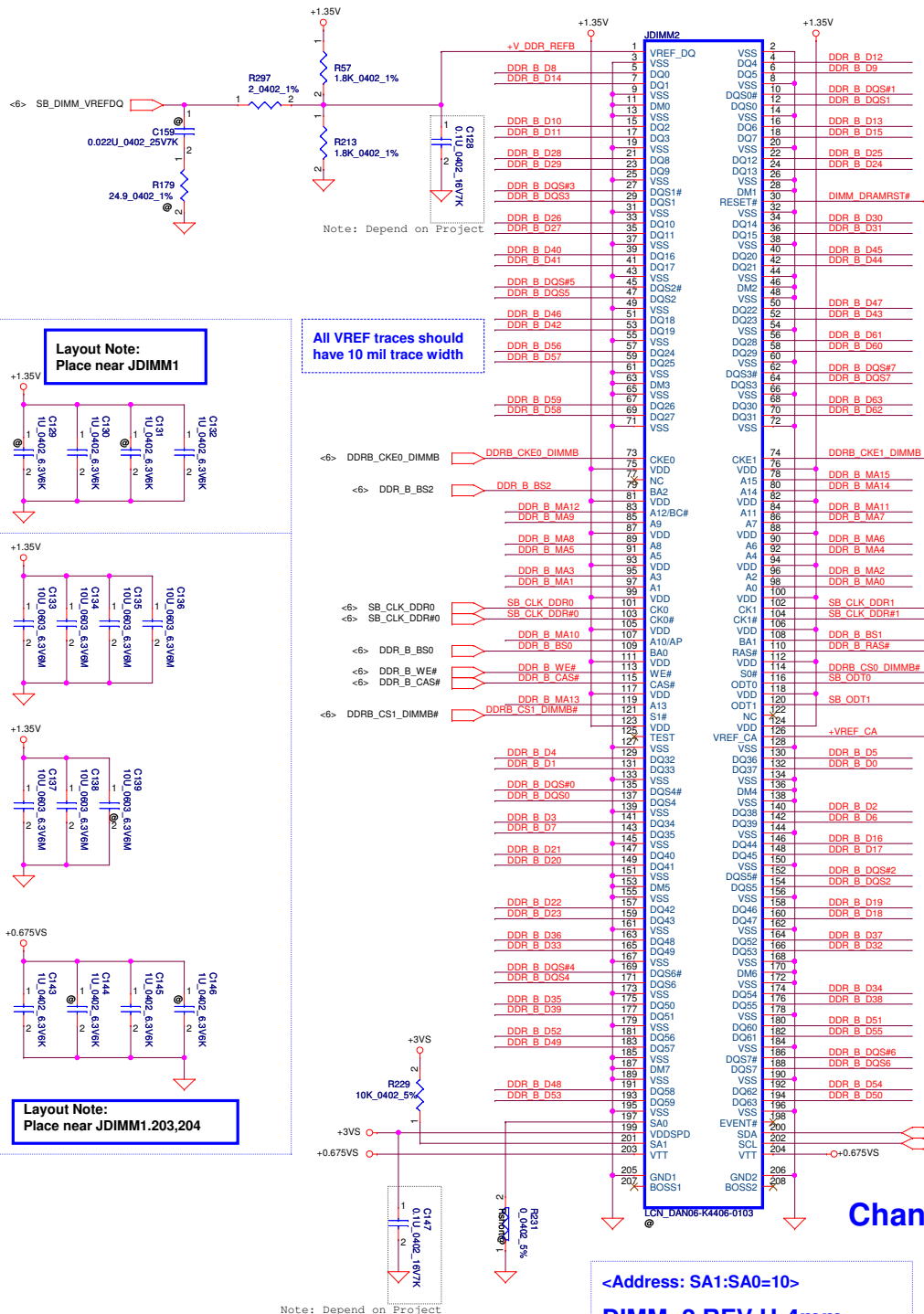
Layout Note:
Place near JDIMM1.203,204



Channel A

<Address: SA1:SA0=00>
DIMM_1 REV H:4mm

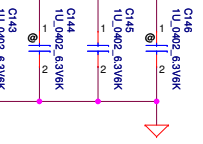
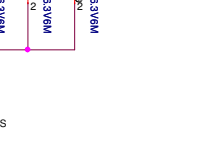
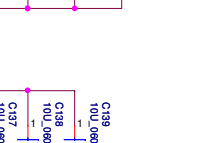
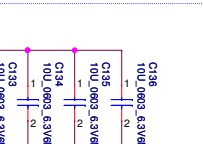
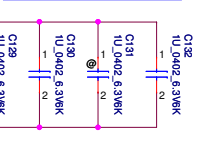
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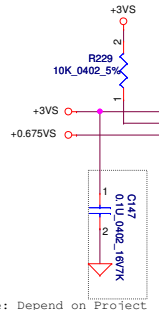
**DDR3 SO-DIMM B
Reverse Type
H=4.0mm**

**Layout Note:
Place near JDIMM1**

**All VREF traces should
have 10 mil trace width**



**Layout Note:
Place near JDIMM1.203,204**

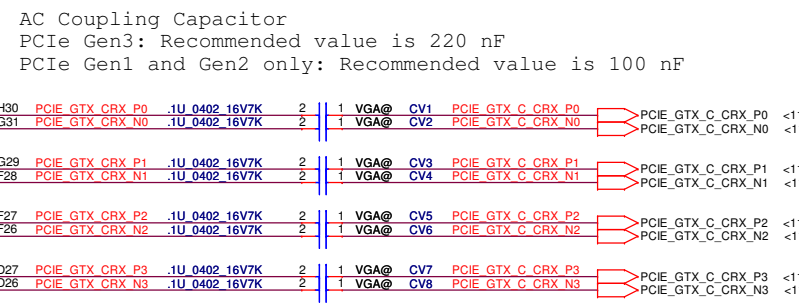
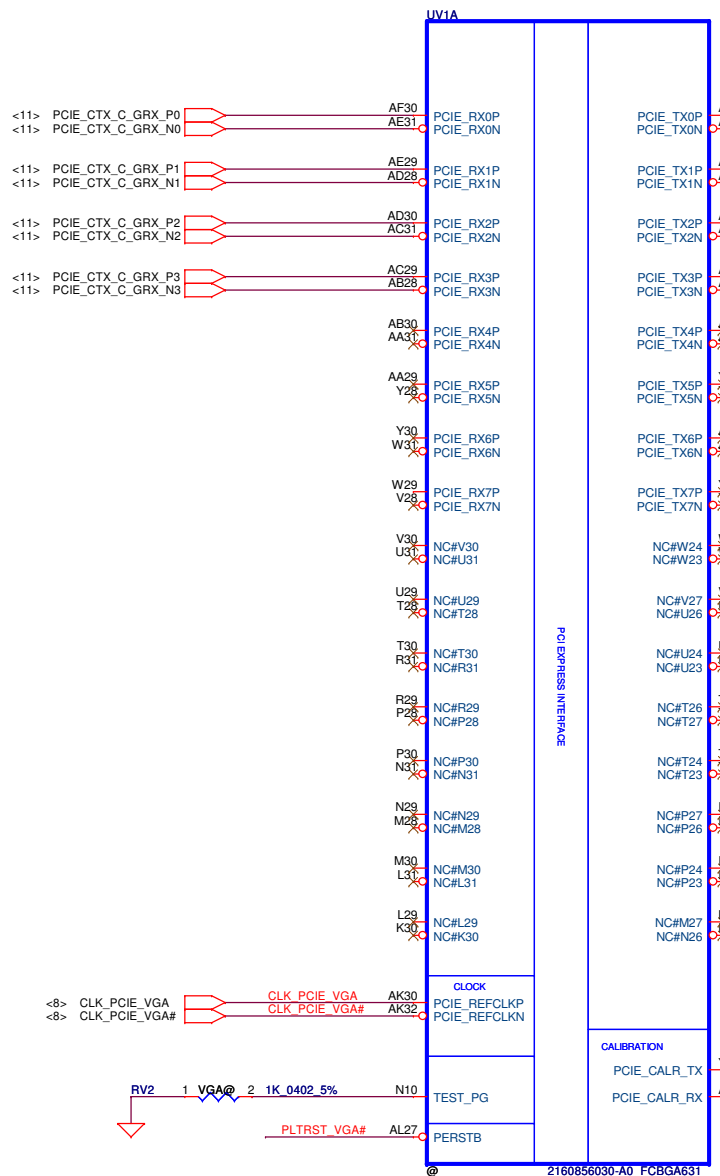


Note: Depend on Project

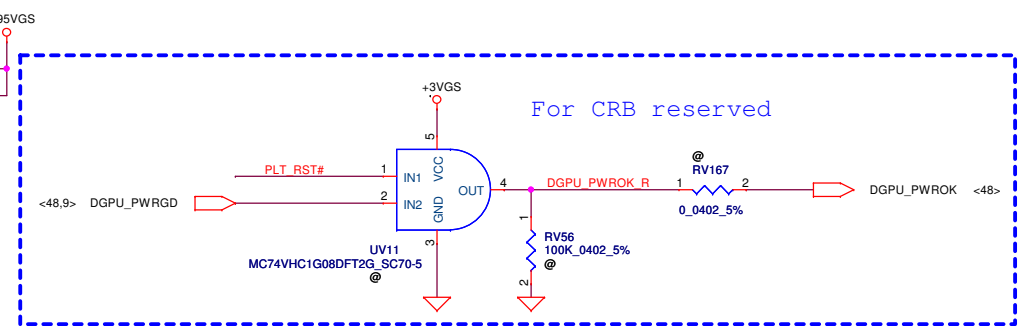
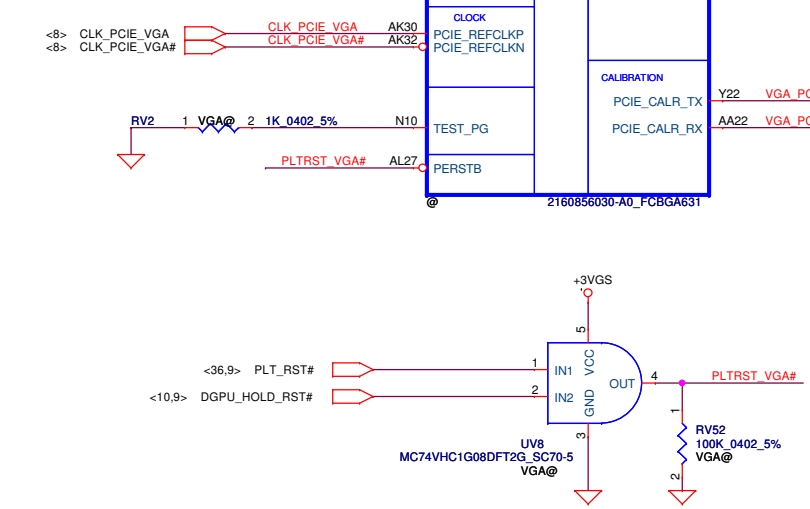
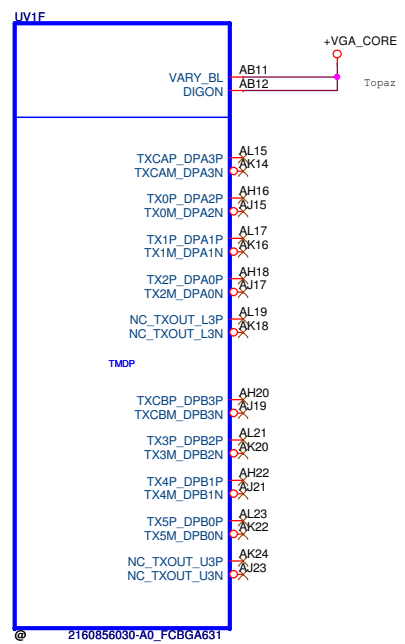
**<Address: SA1:SA0=10>
DIMM_2 REV H:4mm**

Channel B

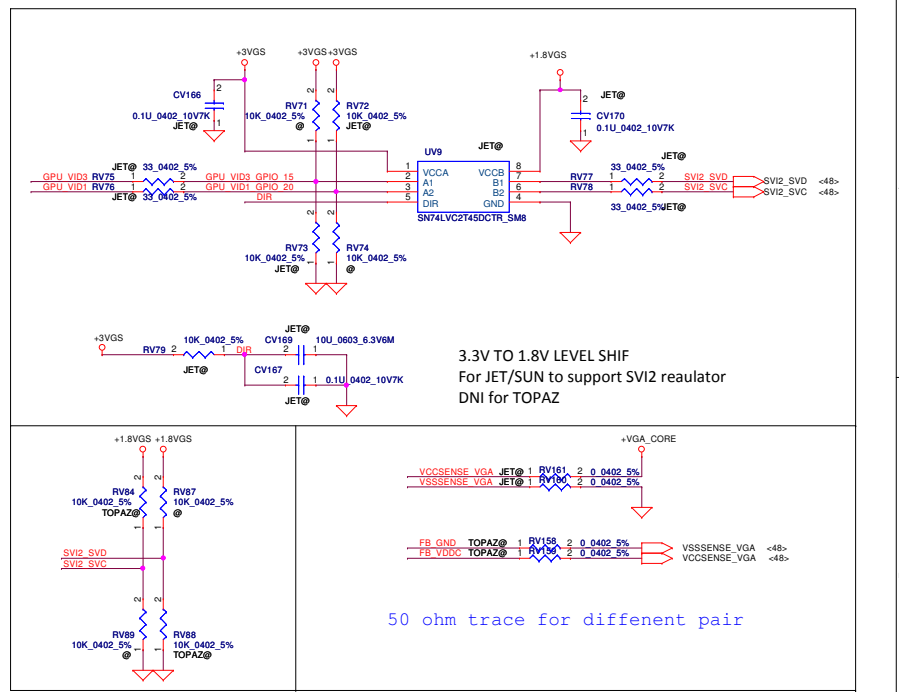
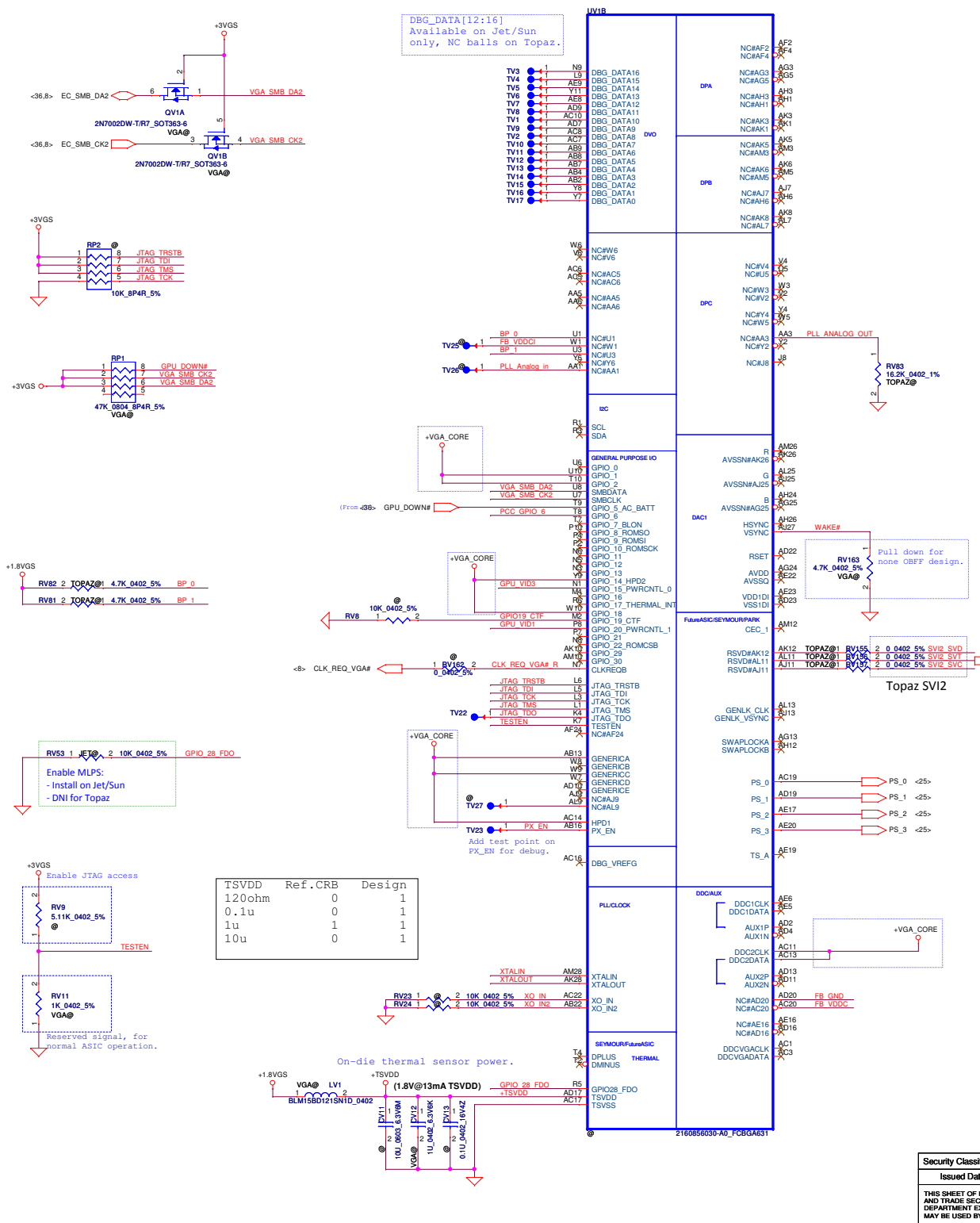
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LVDS Interface

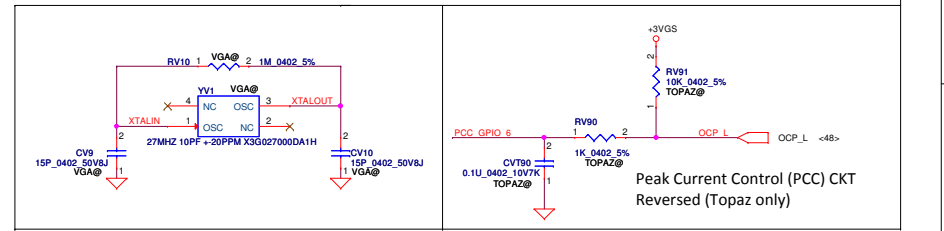


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Size Custom	Document Number	Date:		Rev	
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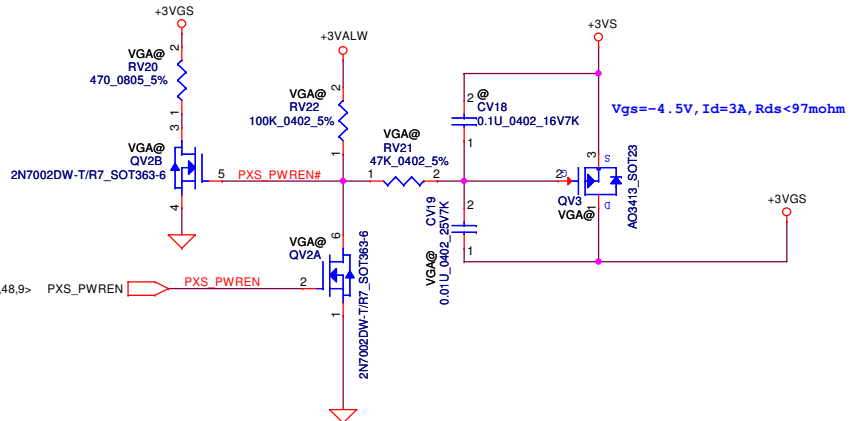


AMD SVI2 Master Interface

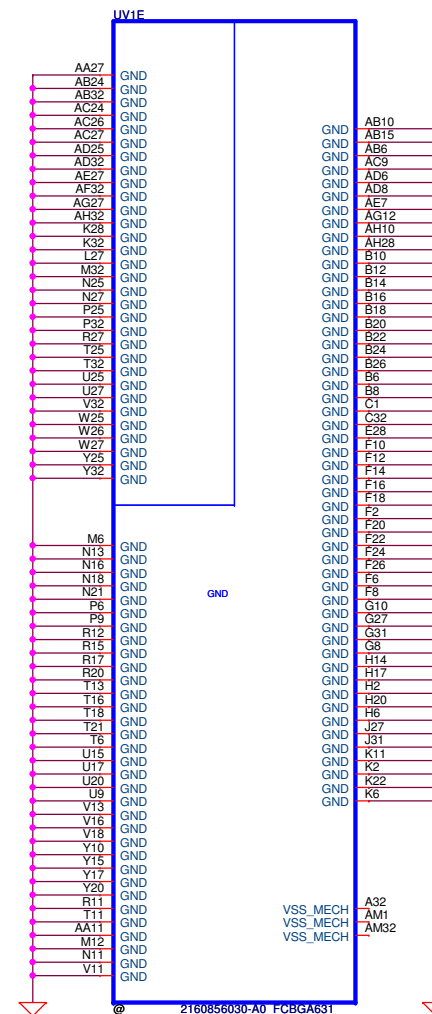
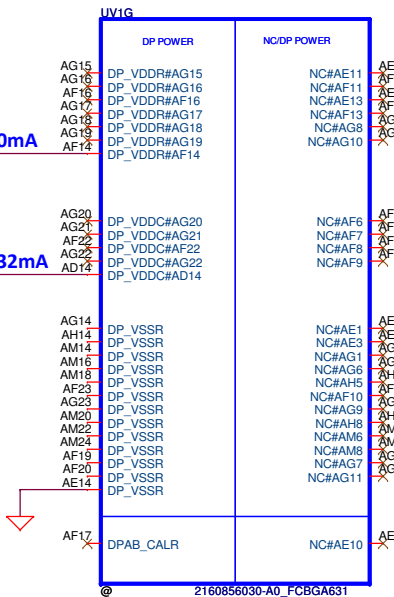
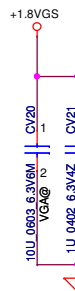
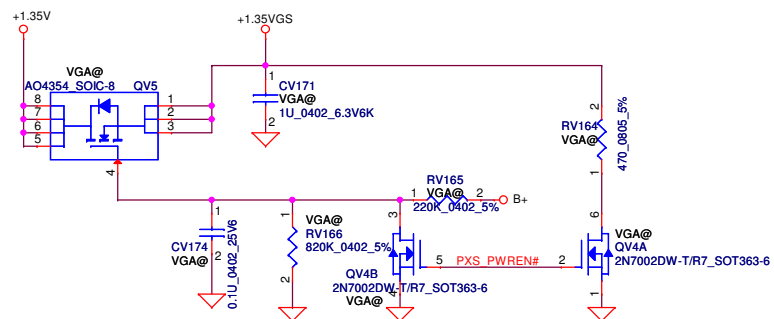
Pin Name	Type	PD/PU	Description
GPIO_SVC	I/O 1.8 V (VDD_GPI018)	PU	Serial VID clock. Push-pull clock output for the SVI2 data bus; driven by the GPU. Point-to-point connection to the SVI2 voltage regulator controller.
GPIO_SVD	I/O 1.8 V (VDD_GPI018)	PD	Serial VID data. Push-pull data output for the SVI2 data bus; driven by the GPU. Sets the voltage, power-state indicator, load-line slope, and voltage offsets for two voltage rails. Point-to-point connection to the SVI2 voltage regulator controller.
GPIO_SVT	I/O 1.8 V (VDD_GPI018)		Serial VID telemetry. Push-pull data input driven by the SVI2 voltage regulator controller. Continuously streams the voltage and current telemetry information to the GPU. Also provides and indication when positive voltage transitions are complete (VOTFC).



+3VS to +3VGS (25mA)



+1.35V to +1.35VGS (6.5A)



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PCIE_PVDD	Jet CRB	Design
1u	1	1
10u	1	1

PCIE_VDDC/BIF_VDDC	Jet CRB	Design
1u	6	6
10u	1	1

VDDR1	Jet CRB	Design
0.01u	1	1
0.1u	1	1
2.2u	5	5
10u	1	1

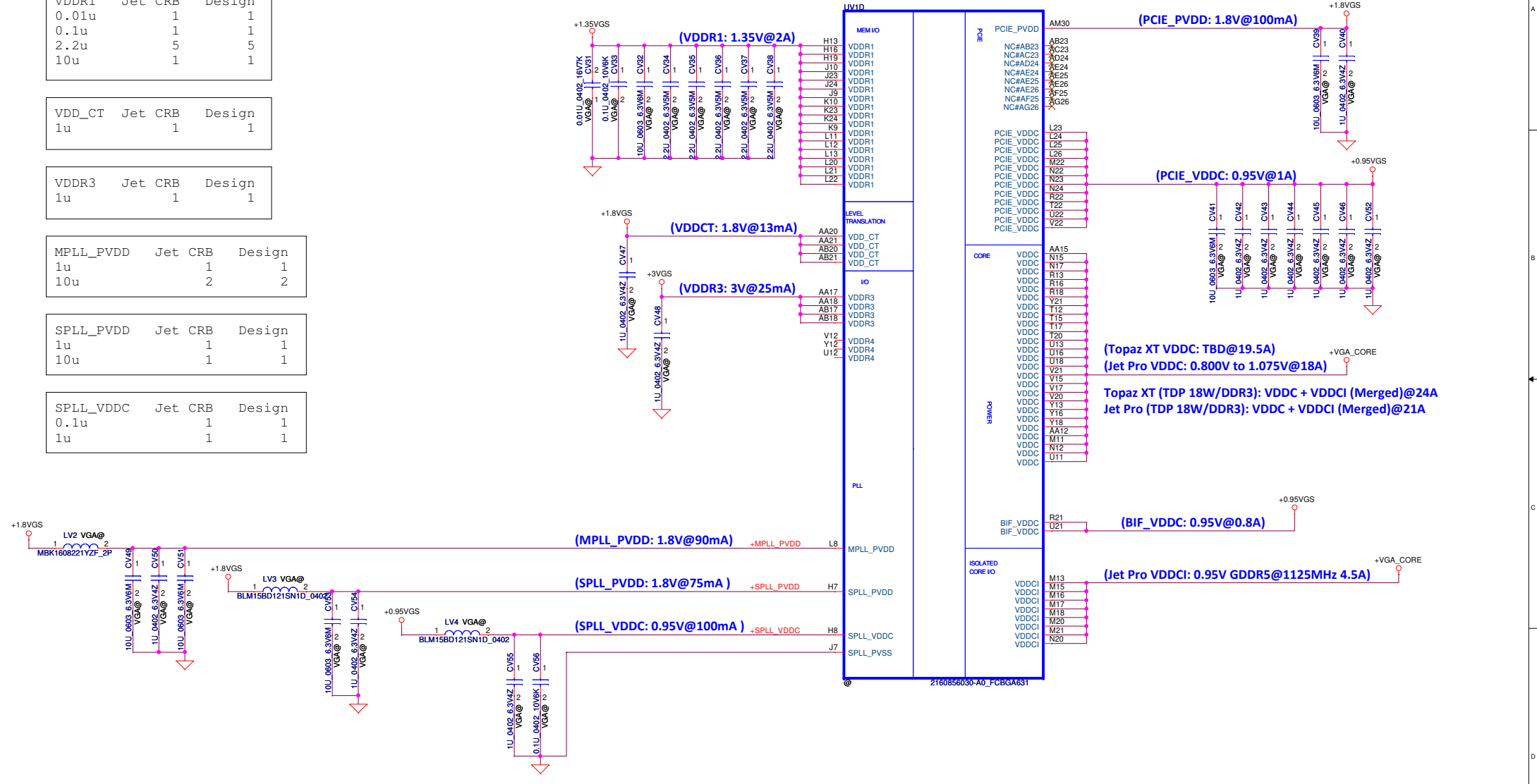
VDD_CT	Jet CRB	Design
1u	1	1

VDDR3	Jet CRB	Design
1u	1	1

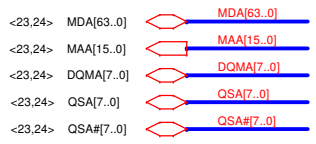
MPLL_PVDD	Jet CRB	Design
1u	1	1
10u	2	2

SPLL_PVDD	Jet CRB	Design
1u	1	1
10u	1	1

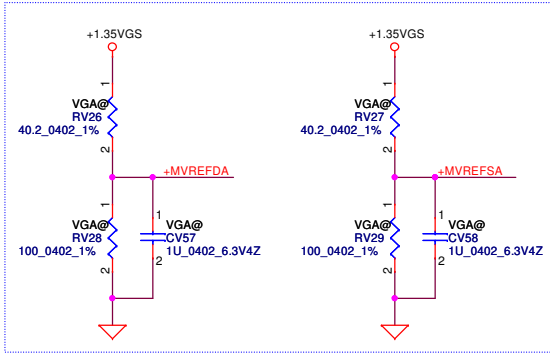
SPLL_VDDC	Jet CRB	Design
0.1u	1	1
1u	1	1



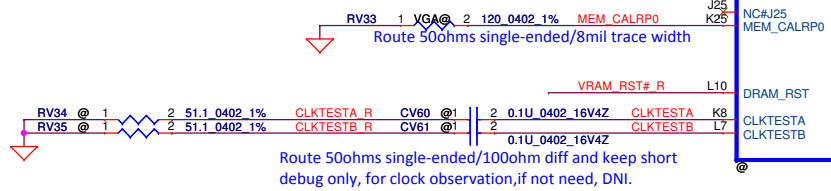
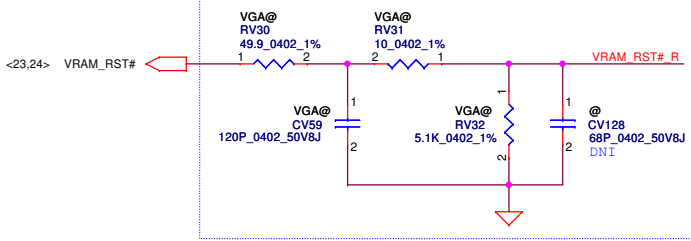
Security Classification	Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2013/09/25	Deciphered Date	2016/09/25	JET Power		Rev 1.0
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				Date:	Monday, February 10, 2014	Sheet 21 of 52



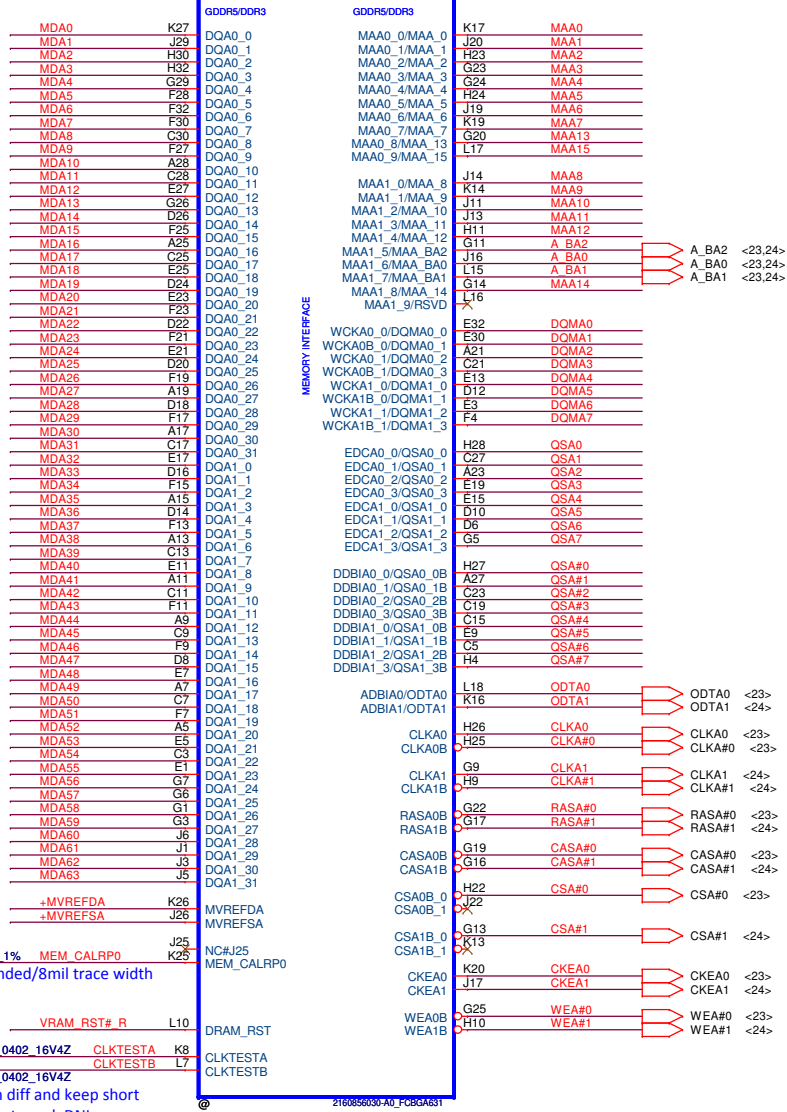
Place close to GPU (within 25mm)



Place all these components very close to GPU (within 25mm) and keep all components close to each other.



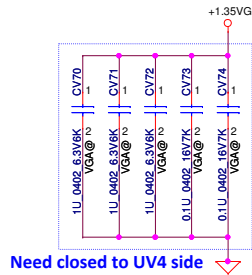
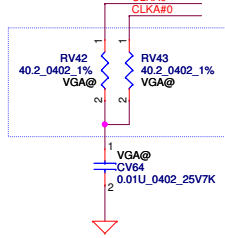
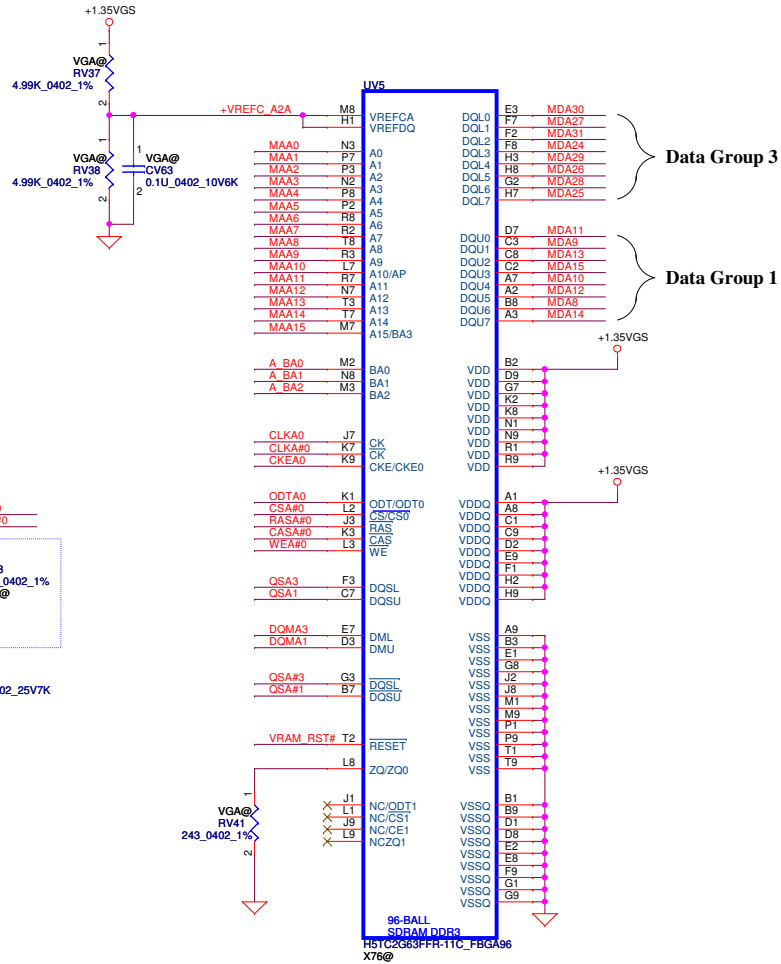
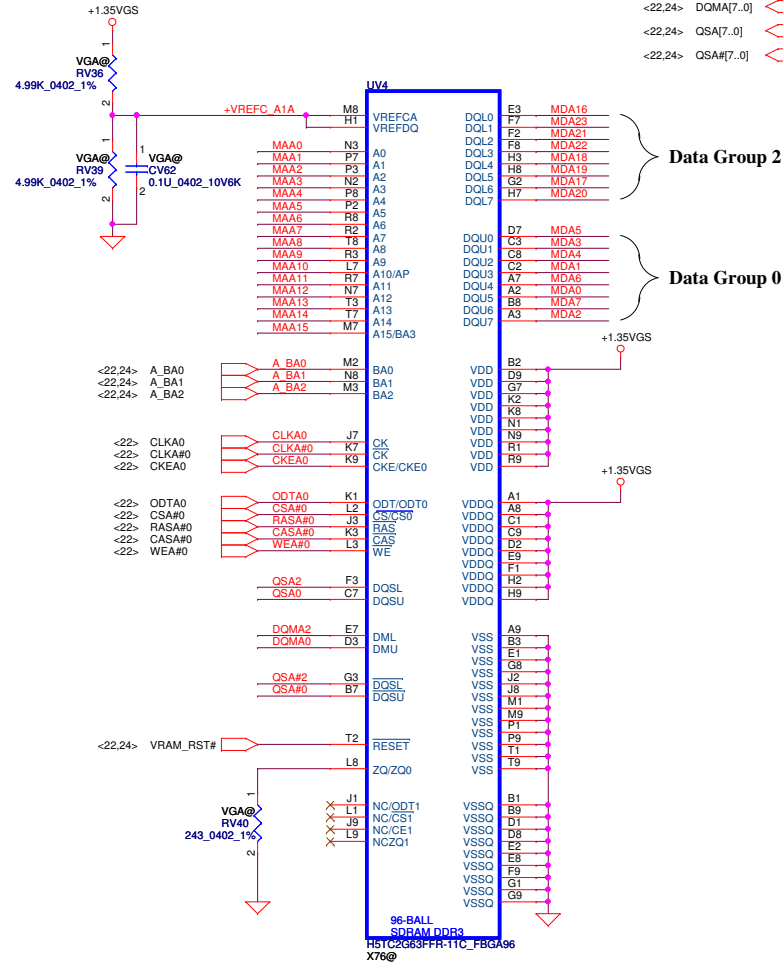
UV1C



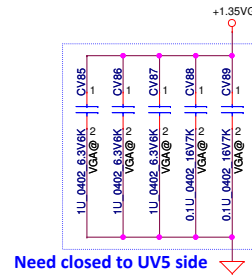
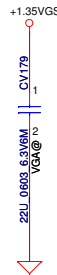
Memory Partition A - Lower 32 bits

<Channel A0>

- <22,24> MDA[63..0] MDA[63..0]
- <22,24> MAA[15..0] MAA[15..0]
- <22,24> DQMA[7..0] DQMA[7..0]
- <22,24> QSA[7..0] QSA[7..0]
- <22,24> QSA#[7..0] QSA#[7..0]



Need closed to UV4 side



Need closed to UV5 side

Channel A0, Data Group 0

- MDA0
- MDA1
- MDA2
- MDA3
- MDA4
- MDA5
- MDA6
- MDA7
- DQMA0
- QSA0
- QSA#0

Channel A0, Data Group 1

- MDA8
- MDA9
- MDA10
- MDA11
- MDA12
- MDA13
- MDA14
- DQMA1
- QSA1
- QSA#1

Channel A0, Data Group 2

- MDA16
- MDA17
- MDA18
- MDA19
- MDA20
- MDA21
- MDA22
- MDA23
- DQMA2
- QSA2
- QSA#2

Channel A0, Data Group 3

- MDA24
- MDA25
- MDA26
- MDA27
- MDA28
- MDA29
- MDA30
- MDA31
- DQMA3
- QSA3
- QSA#3

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Compal Electronics, Inc.

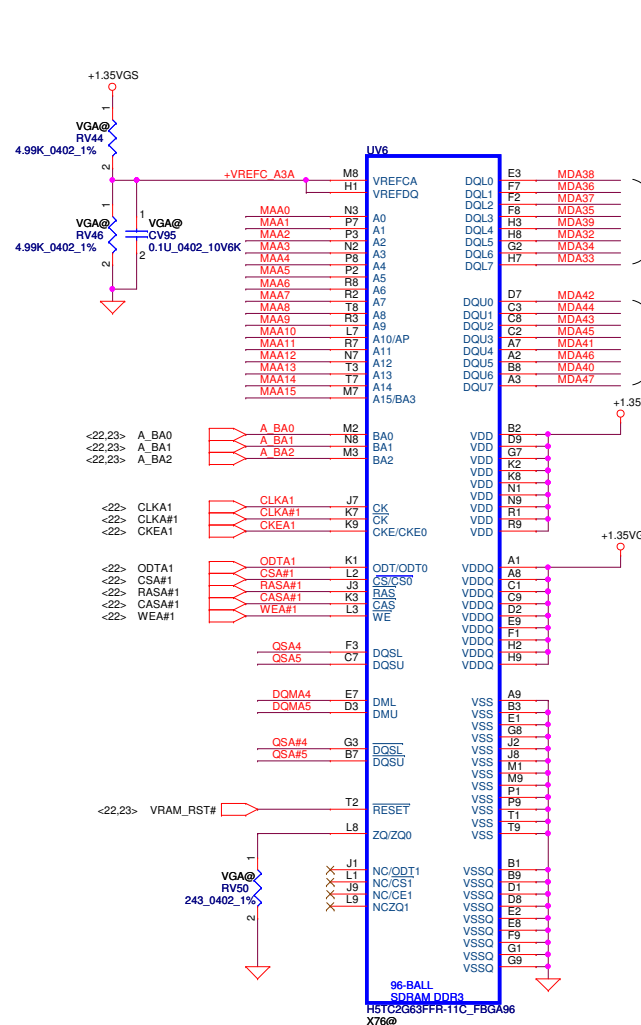
VRAM A Lower

ZSWAA/ZCWA LA-B301P

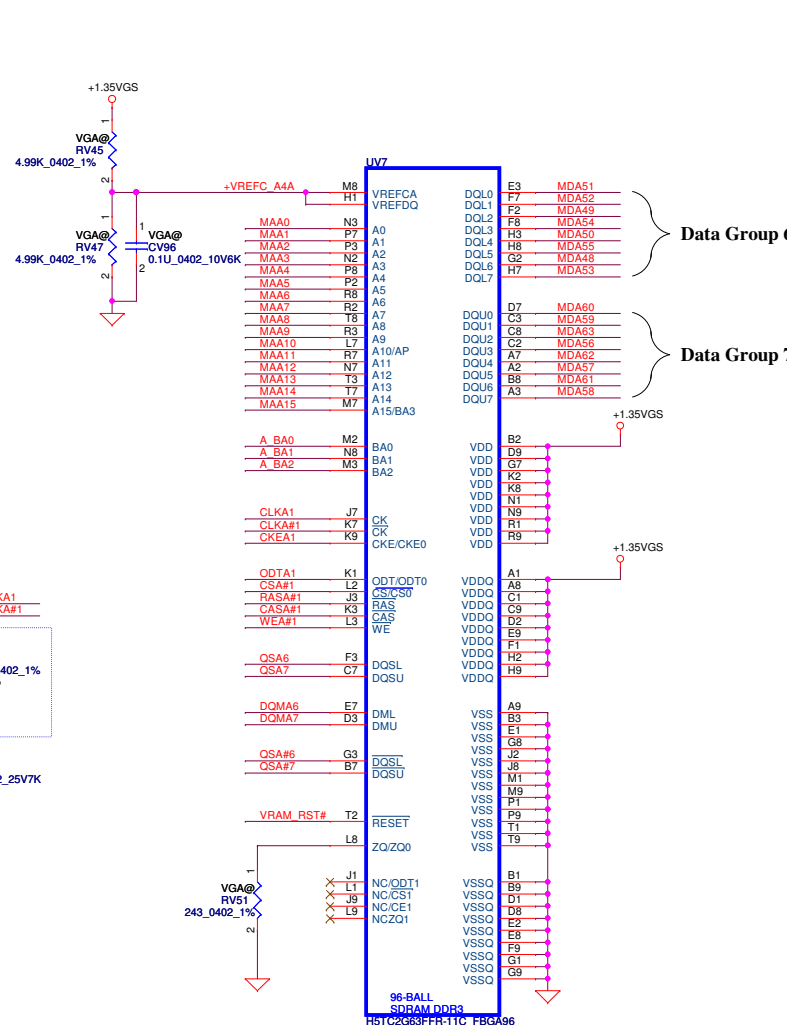
Rev 1.0

Memory Partition A - Upper 32 bits

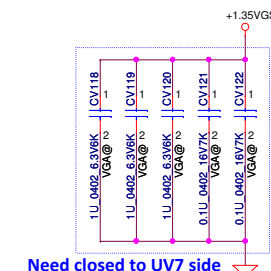
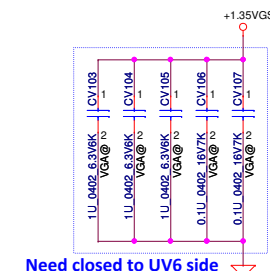
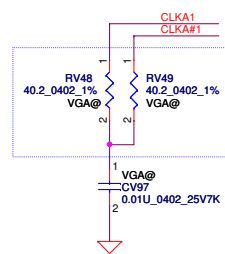
<Channel A1>



- <22,23> MDA[63..0] MDA[63..0]
- <22,23> MAA[15..0] MAA[15..0]
- <22,23> DQMA[7..0] DQMA[7..0]
- <22,23> QSA[7..0] QSA[7..0]
- <22,23> QSA[7..0] QSA[7..0]



- <22,23> A_BA0 A_BA0
- <22,23> A_BA1 A_BA1
- <22,23> A_BA2 A_BA2
- <22,23> CLKA1 CLKA1
- <22,23> CLKA#1 CLKA#1
- <22,23> CKEA1 CKEA1
- <22,23> ODTA1 ODTA1
- <22,23> CSA#1 CSA#1
- <22,23> RASA#1 RASA#1
- <22,23> CESA#1 CESA#1
- <22,23> WEA#1 WEA#1
- <22,23> QSA4 QSA4
- <22,23> QSA5 QSA5
- <22,23> DOMA4 DOMA4
- <22,23> DOMA5 DOMA5
- <22,23> QSA# QSA#
- <22,23> VRAM_RST# VRAM_RST#



Channel A1, Data Group 4	
MDA32	
MDA33	
MDA34	
MDA35	
MDA36	
MDA37	
MDA38	
MDA39	
DQMA4	
QSA4	
QSA#4	
Channel A1, Data Group 5	
MDA40	
MDA41	
MDA42	
MDA43	
MDA44	
MDA45	
MDA46	
MDA47	
DQMA5	
QSA5	
QSA#5	
Channel A1, Data Group 6	
MDA48	
MDA49	
MDA50	
MDA51	
MDA52	
MDA53	
MDA54	
MDA55	
DQMA6	
QSA6	
QSA#6	
Channel A1, Data Group 7	
MDA56	
MDA57	
MDA58	
MDA59	
MDA60	
MDA61	
MDA62	
MDA63	
DQMA7	
QSA7	
QSA#7	

Pin Name	Type	PD/PU	Description
GPIO_0	I/O 3.3 V (VDDR3)	PD-reset	Power-state indicator. Permits the voltage regulator to activate power-saving features. IF VR Support PSI# and DPRSLVPR PU 10K to +3VGS. PSI# :Low load current flag DPRSLVPR : Deeper sleep enable flag
GPIO_5_AC_BATT	I/O 3.3 V (VDDR3)	PD-reset	(Optional) An input which allows the system to request a fastpower reduction by setting GPIO_5_AC_BATT to low (0 V). The resulting state transition may disturb the display momentarily. Power reductions that are less time critical should use the standard software methods in order to prevent display disturbances.
GPIO_6 GPIO_15_PWRCNTL_0 GPIO_20_PWRCNTL_1 GPIO_29 GPIO_30	I/O 3.3 V (VDDR3)	PD-reset	Voltage control signals for the core (VDDC and VDDCI). At reset, these signals will be inputs with weak internal pulldown resistors. The VBIOS can define all voltage-control signals to be either 3.3-V or open-drain outputs (all signals must be the same type). The output states (high/low) of these pins are programmable for each AMD PowerPlay state when they are used as voltage control signals. Note: GPIO_29 and GPIO_30 are only available on 28-nm ASICs, and are NC on earlier generation ASICs.
GPIO_8_ROMSO	I 3.3 V (VDDR3)	PD-reset	Serial-ROM output from ROM. General purpose I/O or open-drain output. Design: No use external VGA ROM, so use the test point
GPIO_9_ROMSI	O 3.3 V (VDDR3)	PD-reset	Serial-ROM input to ROM. General purpose I/O or open-drain output.
GPIO_10_ROMSCK			Serial-ROM clock to ROM. General purpose I/O or open-drain output.
GPIO_22_ROMCSB			BIOS-ROM chip select. Used to enable the ROM for ROM read and program operations. Design: No use external VGA ROM, so use the test points.
GPIO_17_THERMAL_INT	I/O 3.3 V (VDDR3)	PD-reset	Thermal monitor interrupt. An input from an external temperature sensor (ALERTB).
GPIO_19_CTF	O 3.3 V (VDDR3)	PD-reset	Critical temperature fault (CTF) (active high) will output 3.3 V if the on-die temperature sensor exceeds a critical temperature so that the motherboard can protect the ASIC from damage by removing power. The CTF setpoint is 109°C by default, and is programmed during ASIC initialization. See the advisory for AMD PowerPlay states for more details.
GPIO_21	I/O 3.3 V (VDDR3)	PD-reset	(Optional) Voltage control signal for the memory-voltage regulator. Note: This signal must be low (0 V) at reset (failure to do so will prevent booting).
GPIO_28_FDO	I/O 3.3 V (VDDR3)	PD-reset	Disable MLPS: PU 10K ohm to 3.3V. (Do not install for Mars) Enable MLPS: PD 10K ohm to GND. (Install for Mars)
CLKREQB	O		Supports the CLKREQB feature for saving power to turn on/off the REFCLK clock on the ASIC.
PX_EN	O	PD	On/off regulator switch in AMD PowerXpress? (switchable graphics) BACO mode. High (3.3 V) switches the regulators off (enter BACO mode). Low (0 V) switches the regulators on. (Default) PX_EN is tri-state before internal TEST_PG is asserted and PERSTb is deasserted.

MLPS

MLPS Bit	Strap Name	Legacy	Description	Settings
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	GPIO[13:11]	If BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. Refer to current databooks for details.	001
PS_0[4]	N/A	GENLK_VSYNC	Reserved for internal use only. Must be 1 at reset.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	GPIO_2	Re-defined strap to indicate PCIe GEN3 capability. 1 = PCIe GEN3 supported. 0 = PCIe GEN3 not supported.	0
PS_1[2]	STRAP_BIF_CLK_PM_EN	GPIO_8	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	GENLK_CLK	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	TX_PWRS_ENB	GPIO_0	Transmitter (Tx) power savings enable. 0 = 50% Tx output swing. 1 = Full Tx output swing.	1
PS_1[5]	TX_DEEMPH_EN	GPIO_1	PCI EXPRESS transmitter, deemphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	1
PS_2[1]	N/A	N/A	Reserved.	0
PS_2[2]	N/A	N/A	Reserved.	0
PS_2[3]	BIOS_ROM_EN	GPIO_22	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	0
PS_2[4]	BIF_VGA_DIS	GPIO_9	VGA disable determines whether or not the card will be recognized as the system's VGA controller. 0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	0
PS_2[5]	N/A	N/A	Reserved.	0
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	N/A	Board configuration related strapping (such as memory ID).	Base on VRAM ID
PS_0[5] PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[0] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	N/A	Together with PS_0[5] form the three-bit strap option to indicate the number of audio-capable display outputs. In a given ASIC there are as many endpoints as there are digital display outputs, though not all outputs are audio capable. 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	111

MLPS Strap

	Bits[5:4]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	11	001	NC	8.45K	2K
PS_1[5:1]	11	000	NC	NC	4.75K
PS_2[5:1]	00	000	680 nF	NC	4.75K
PS_3[5:1]	11	XXX	NC	X	X

00 for JET
10 for Topaz

Mapping to VRAM type

Primary Memory Aperture Size Requested at PCI Configuration

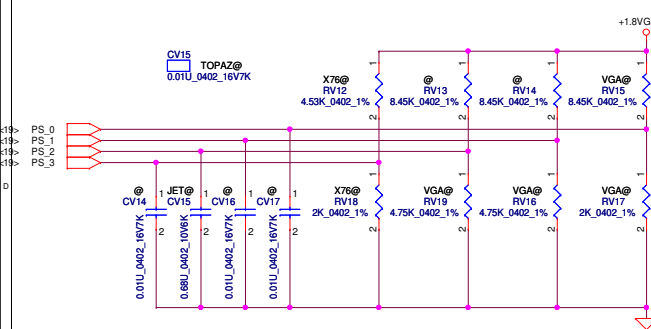
Size of the Primary Memory Apertures	ROM_CONFIG [2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not supported
1 GB	Not supported
2 GB	Not supported
4 GB	Not supported

MLPS configuration

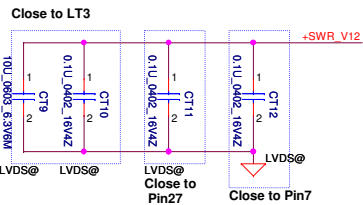
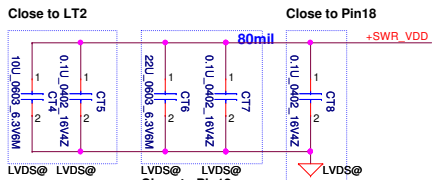
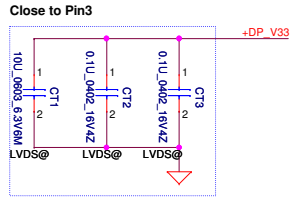
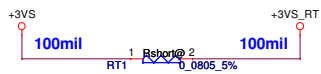
Bits[5:1]	PU(1%)	PD(1%)	Cap
xx000	NC	4.75k	
xx001	8.45k	2.00k	
xx010	4.53k	2.00k	
xx011	6.98k	4.99k	
xx100	4.53k	4.99k	
xx101	3.24k	5.62k	
xx110	3.40k	10.0k	
xx111	4.75k	NC	
00xxx			680nF
01xxx			82nF
10xxx			10nF
11xxx			NC

PS_3[3:1]

Memory ID	P/N	Vendor	Configuration	Size
000	SA000068U40	Samsung	K4W2G1646Q-BC1A	1G
001	SA00006H400	Hynix	H5TC2G63FFR-11C	1G
010	SA00005XB00	Micon	MT41K128M16JT-107G:K	1G
011	SA000076P00	Samsung	K4W4G1646D-BC1A	2G
100	SA00006E800	Hynix	H5TC4G63AFR-11C	2G
101	SA000065D00	Micon	MT41K256M16HA-107G:E	2G

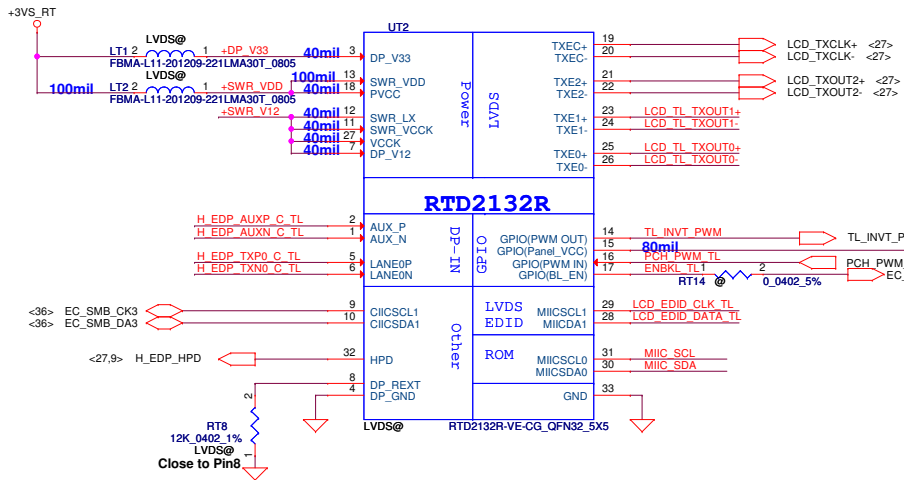


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Size	Document Number	Date	Sheet	of
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SWR / LDO Mode select

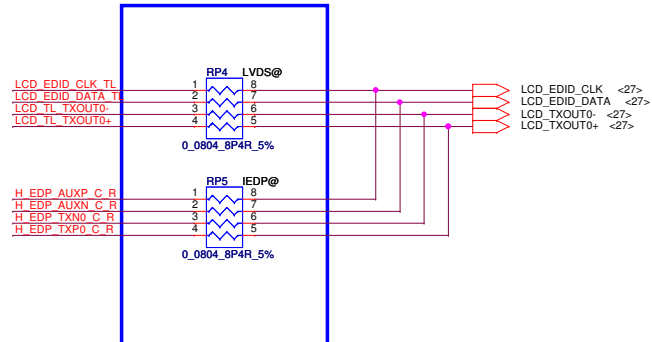
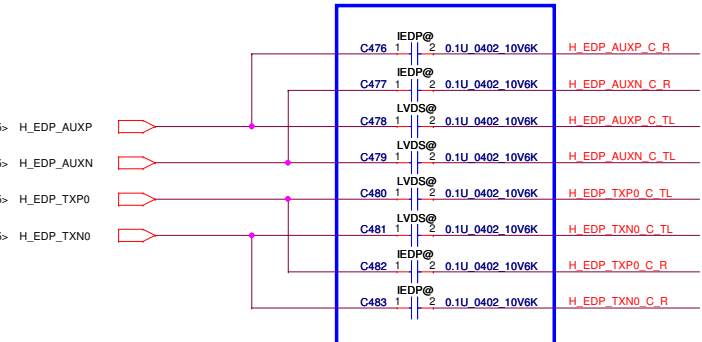
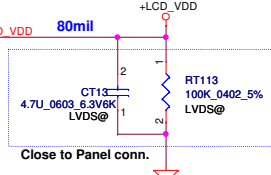
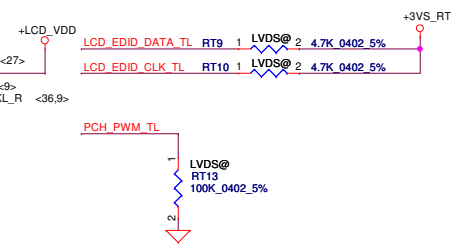
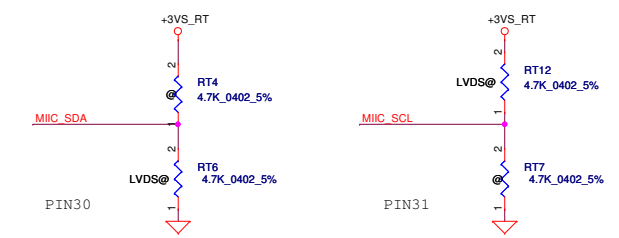
※LDO mode is adopted as default power regulator mode.
Also can implement SWR mode by add inductor.



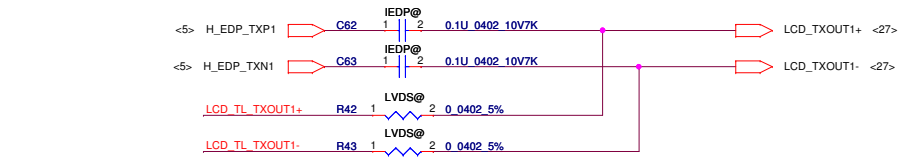
Mode Configure

※ROM only mode : PIN 30 4.7k pull low, Pin 31 4.7k pull high.
EP mode : PIN 30 4.7k pull high, Pin 31 4.7k pull low.
EEPROM : PIN 30 4.7k pull high, Pin 31 4.7k pull high.

< ※Default mode >



Place co-layer Resistor back to back on TOP and BOT



	PIN15
2132S	TL_ENVDD
2132R	+LCD_VDD *

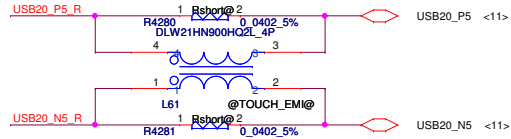
* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

PIN16	Accept voltage input (high level)
2132S	3.3V
2132R	1.5-3.3V

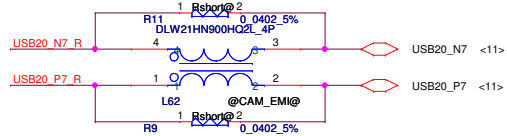
* Version R has internal level shifter, remove level shifter circuit on AMD platform

Different between 2132S and 2132R(N)	
2132S	2132R(N)
1. Support SWR mode	1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter

BTO : TOUCH_EMI@



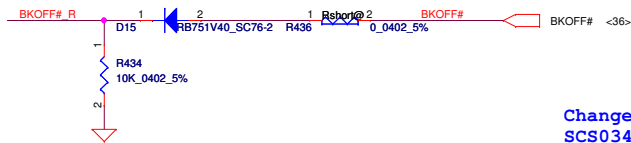
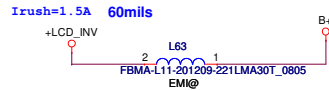
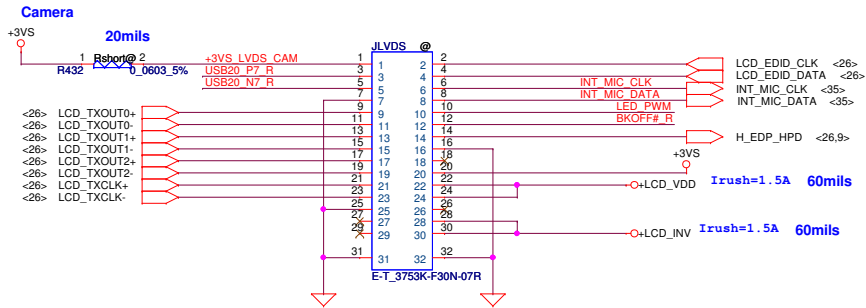
EMI request - Close to JLVDS connector



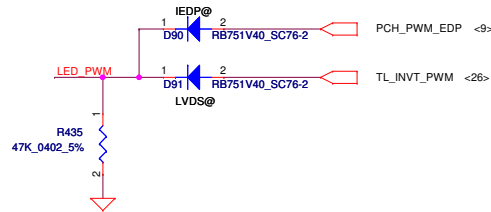
Change L62 P/N from SM070003Y00 to SM070003K00

LVDS colay eDP cable

Pin define will be change after ME ready

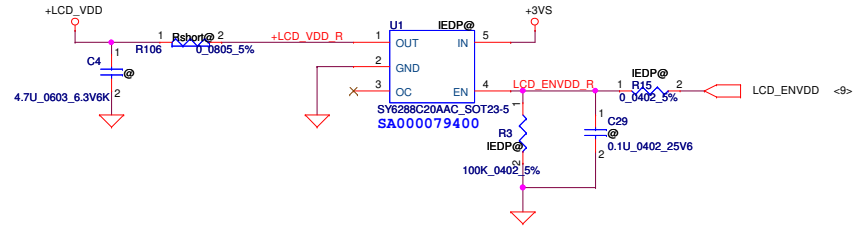


Change D15,D90,D91 P/N from SCS0340L010 to SCS00003500 for X code.

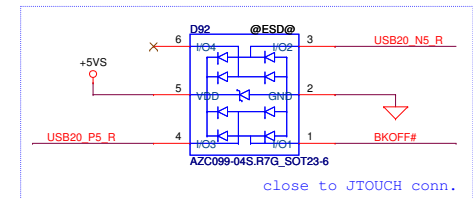
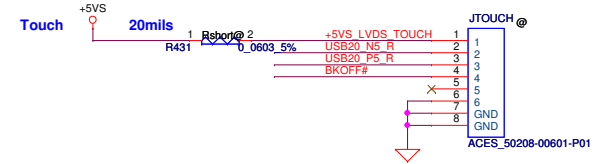
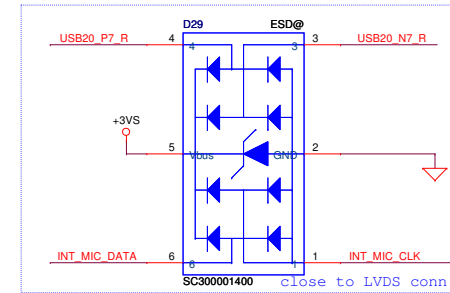


LCD POWER CIRCUIT (For EDP panel only)

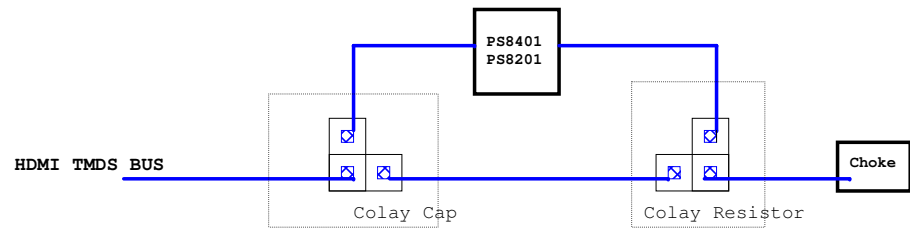
I rush=2A
W=80mils



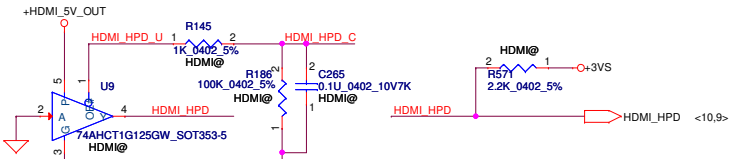
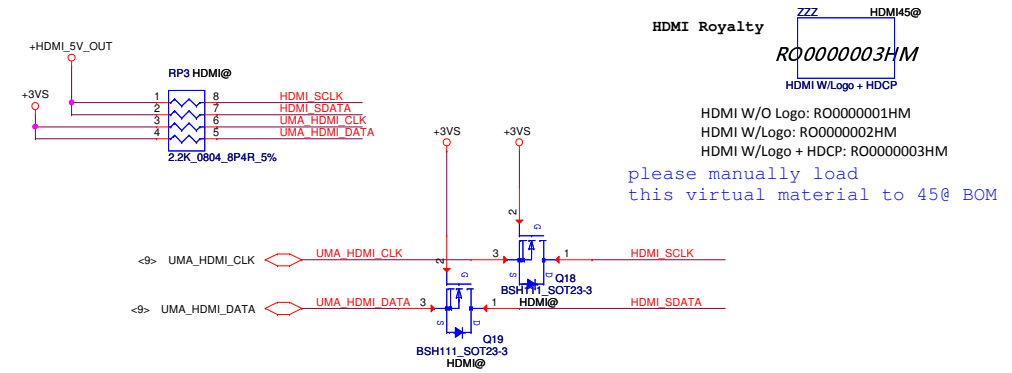
Camera & MIC



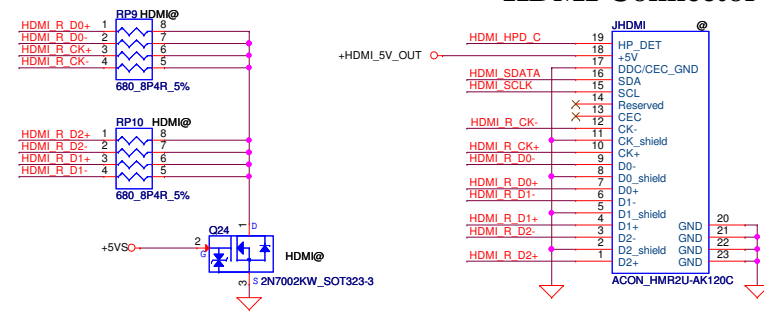
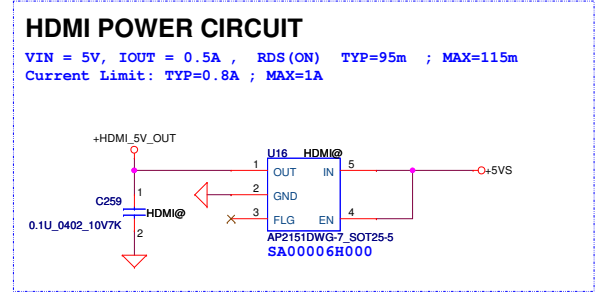
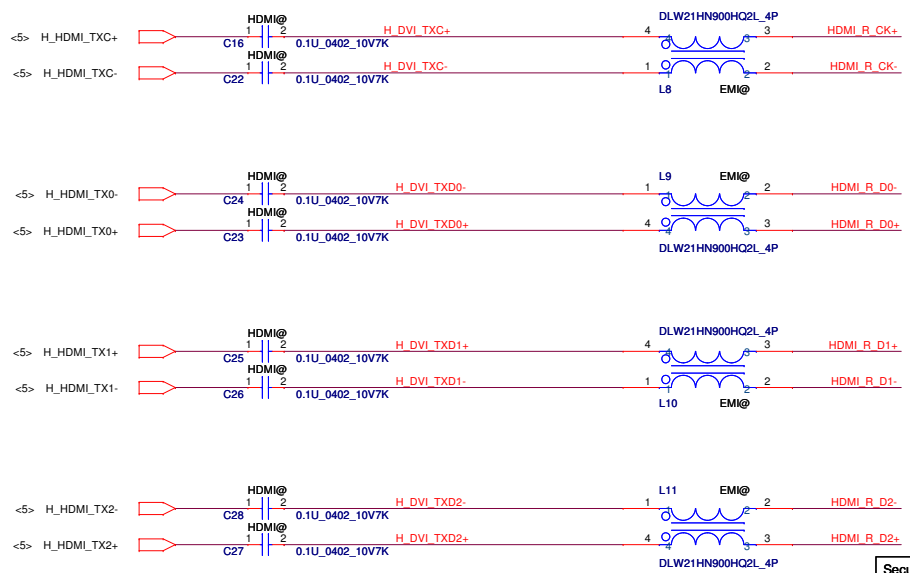
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Issued Date	2013/09/25	Deciphered Date	2016/09/25	LVDS
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Componet close to Conn.
Impedance depend on platform design guide

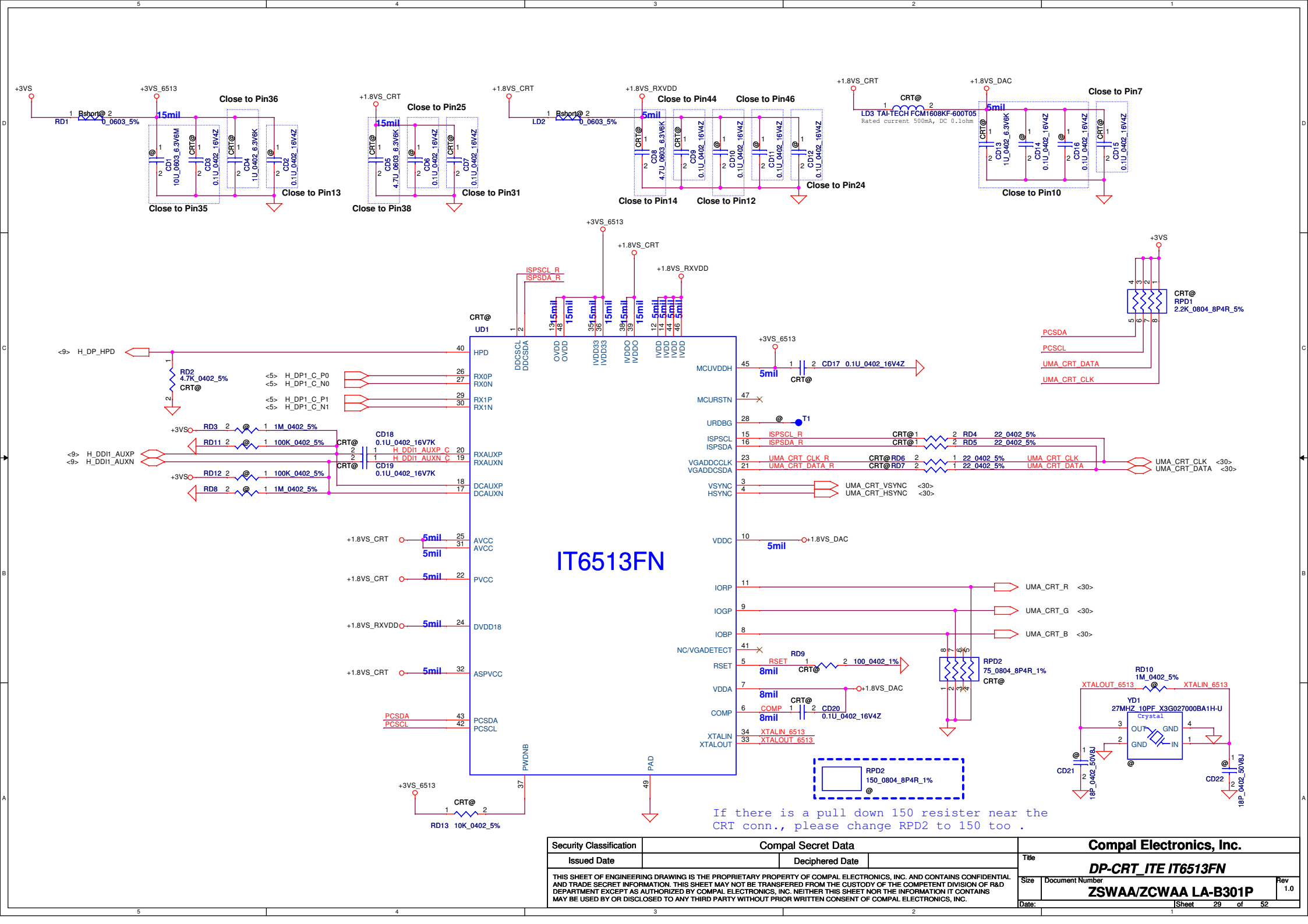


Change L8,L9,L10,L11 P/N from SM070003Y00 to SM070003K00



Common CHOKE use 90ohm

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				ZSWAA/ZCWAA LA-B301P	1.0
				Date: Monday, February 10, 2014	Sheet 28 of 52

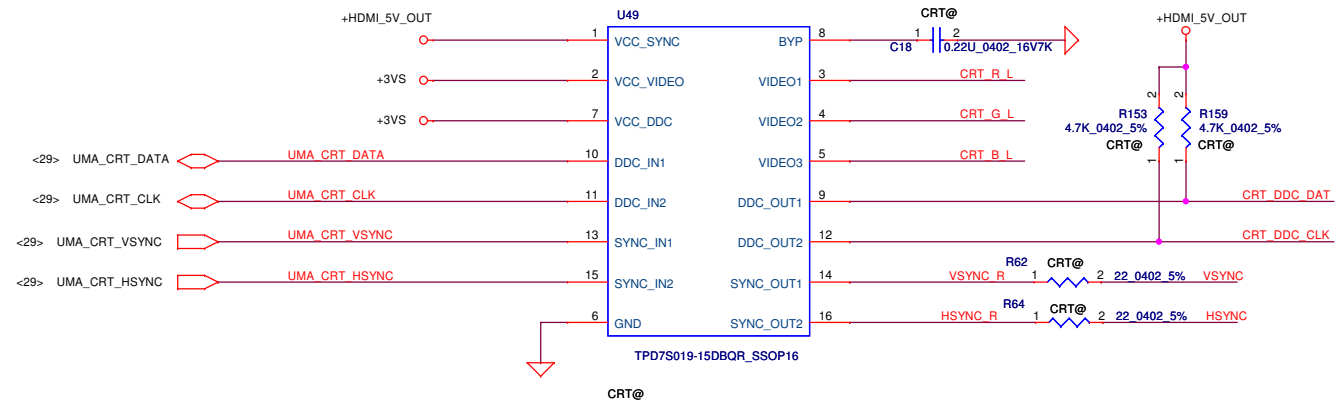
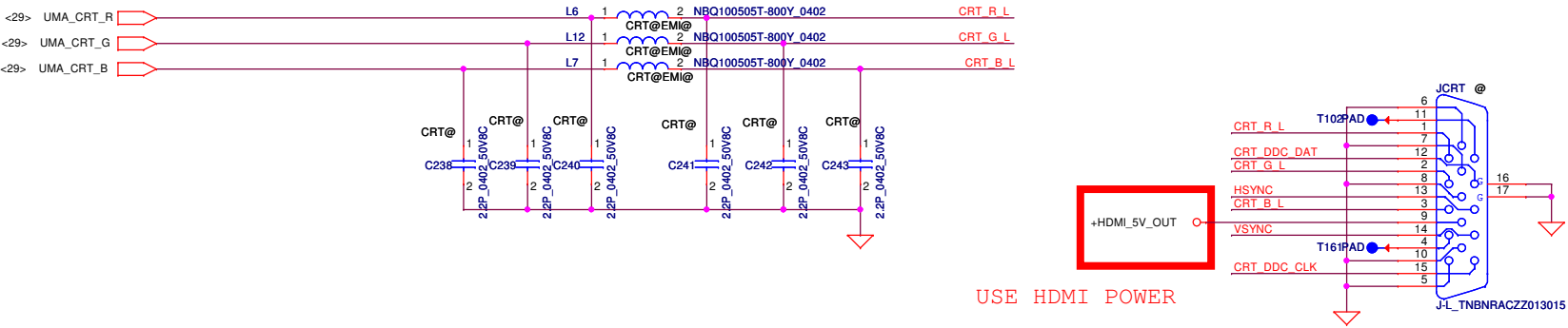


IT6513FN

If there is a pull down 150 resistor near the CRT conn., please change RPD2 to 150 too.

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		Date:		ZSWAA/ZCWA LA-B301P	
		Sheet		29 of 52	

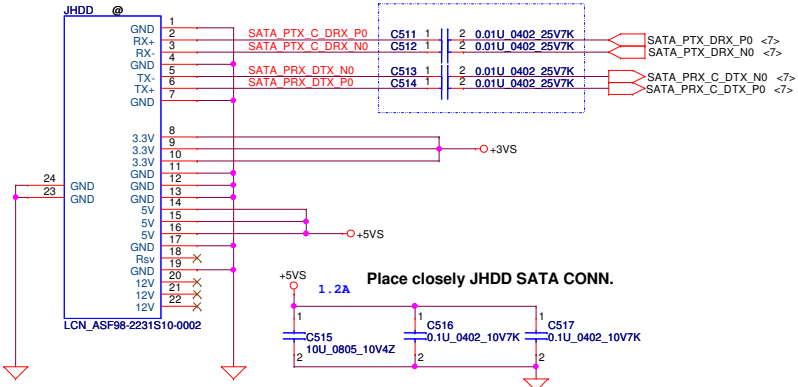
CRT CONNECTOR



Security Classification				Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2013/09/25		Deciphered Date		2016/09/25		Title					
								CRT					
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								ZSWAA/ZCWA LA-B301P		1.0			
Date:								Monday, February 10, 2014		Sheet 30 of 52			

SATA HDD/SSD Conn.

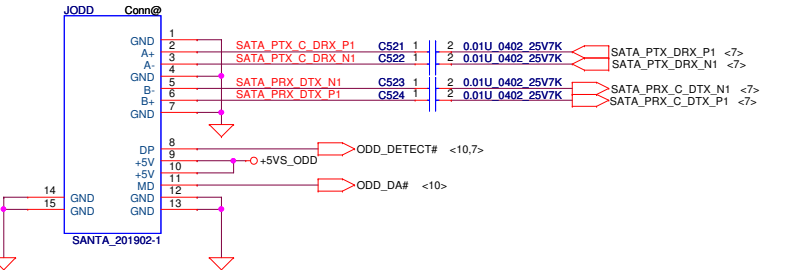
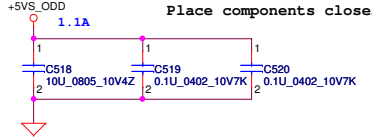
Close to JHDD



SATA ODD Conn

Place components closely ODD CONN.

Power Consumption	
Peak	1800 mA
Read (CD)	1100 mA
Read (DVD)	950 mA
Write	1300 mA
Standby	20mA



NGFF-Slot1-E-Key-WLAN

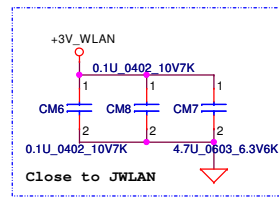
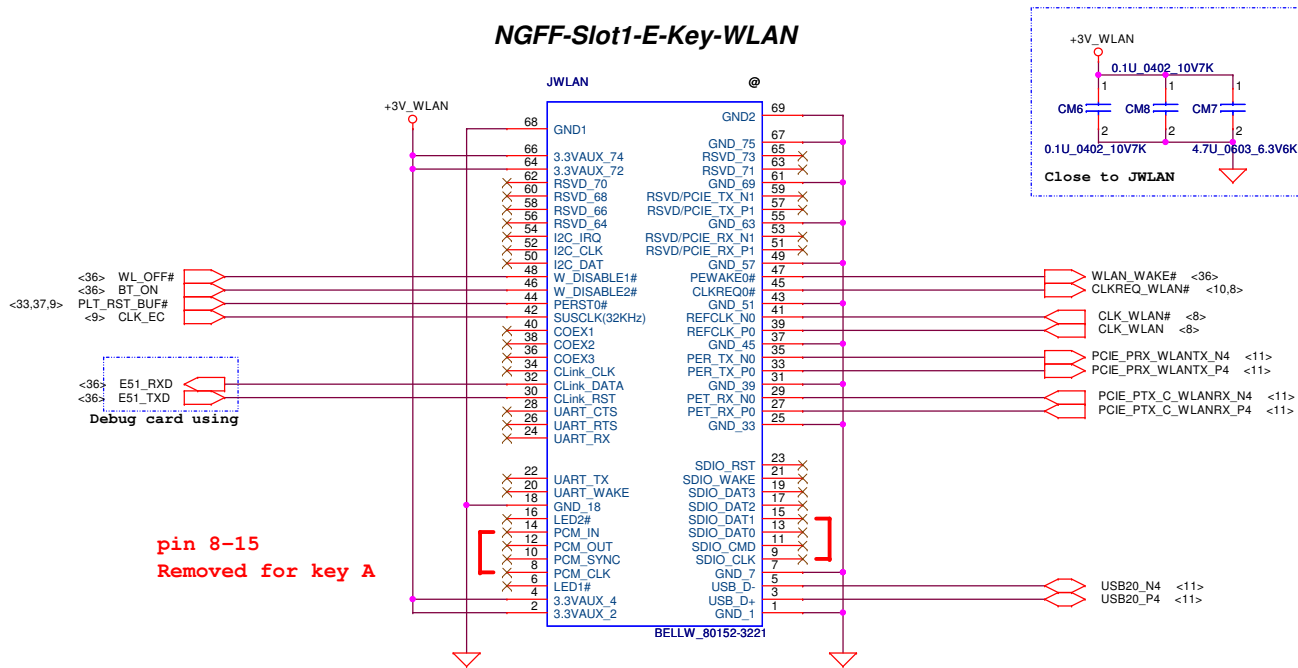


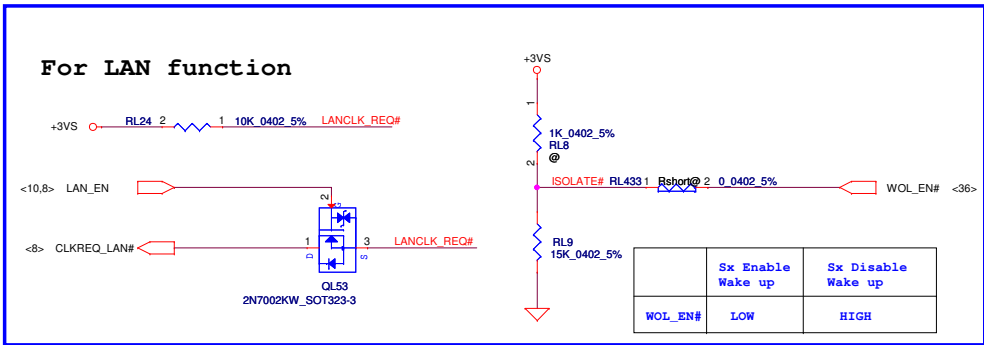
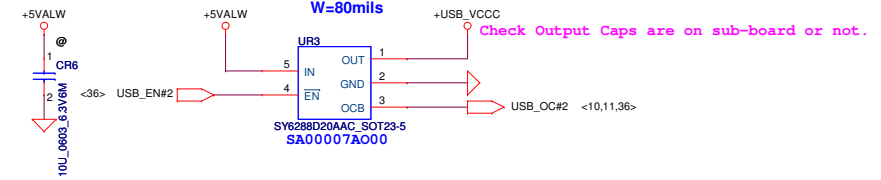
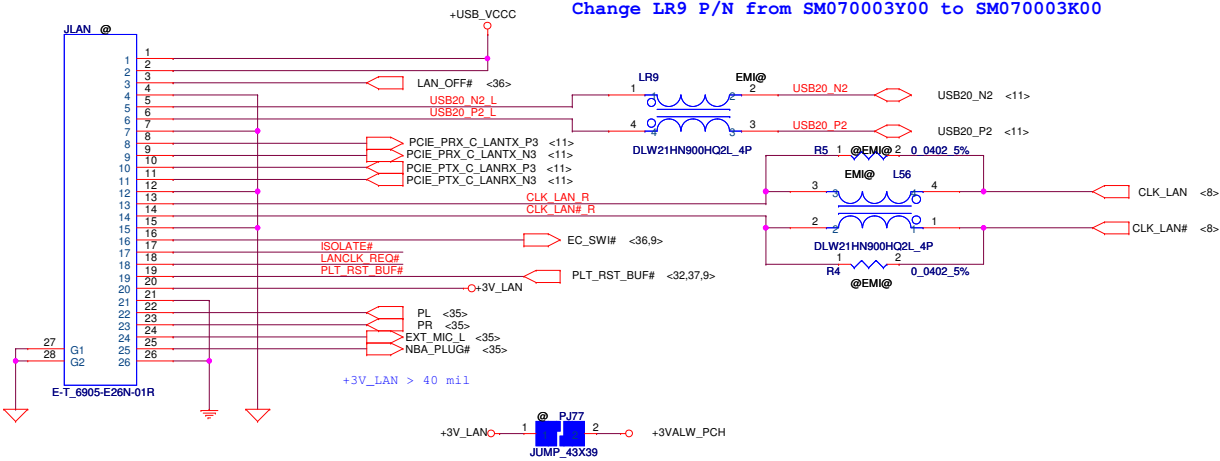
Table 23. SDIO Based Module Solution Pinout (Module Key E)

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKN1	73
70	UIM_Power_In/GPIO1/PEWake1#	RESERVED/REFCLKP1	71
68	UIM_Power_Out/CLKREQ1#	GND	69
66	UIM_SWP/PERST1#	Reserved/PETn1	67
64	RESERVED	Reserved/PETp1	65
62	ALERT#(O)(0/3.3)	GND	63
60	I2C_CLK (I)(0/3.3)	Reserved/PERn1	61
58	I2C_DATA (I)(0/3.3)	Reserved/PERp1	59
56	W_DISABLE#1 (I)(0/3.3V)	GND	57
54	Reserved/W_DISABLE#2 (I)(0/3.3V)	PEWake# (I)(0/3.3V)	55
52	PERST# (O)(0/3.3V)	CLKREQ# (I)(0/3.3V)	53
50	SUSCLK(32KHz) (I)(0/3.3V)	GND	51
48	COEX1 (I)(0/1.8V)	REFCLKN0	49
46	COEX2 (I)(0/1.8V)	REFCLKP0	47
44	COEX3 (I)(0/1.8V)	GND	45
42	VENDOR DEFINED	PET#0	43
40	VENDOR DEFINED	PET#0	41
38	VENDOR DEFINED	PER#0	39
36	UART_CTS (I)(0/1.8V)	PER#0	37
34	UART_RTS (O)(0/1.8V)	PER#0	35
32	UART_Rx (I)(0/1.8V)	GND	33
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
	Module Key	Module Key	
22	UART_Tx (O)(0/1.8V)	SDIO_Reset (I)(0/1.8V)	23
20	UART_Wake (O)(0/3.3V)	SDIO_Wake (O)(0/1.8V)	21
18	GND	SDIO_DAT3 (IO)(0/1.8V)	19
16	LED#2 (O)(OD)	SDIO_DAT2 (IO)(0/1.8V)	17
14	PCM_IN/IZS_SD_IN (I)(0/1.8V)	SDIO_DAT1 (IO)(0/1.8V)	15
12	PCM_OUT/IZS_SD_OUT (O)(0/1.8V)	SDIO_DAT0 (IO)(0/1.8V)	13
10	PCM_SYNC/IZS_WS (IO)(0/1.8V)	SDIO_CMD (IO)(0/1.8V)	11
8	PCM_CLK/IZS_SCK (IO)(0/1.8V)	SDIO_CLK (IO)(0/1.8V)	9
6	LED#1 (O)(OD)	GND	7
4	3.3V	USB_D-	5
2	3.3V	USB_D+	3
		GND	1

LAN/USB Small board Conn

Left USB 2.0 x 1

Current Limit 2A



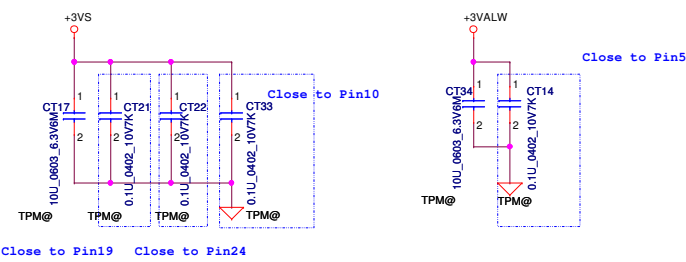
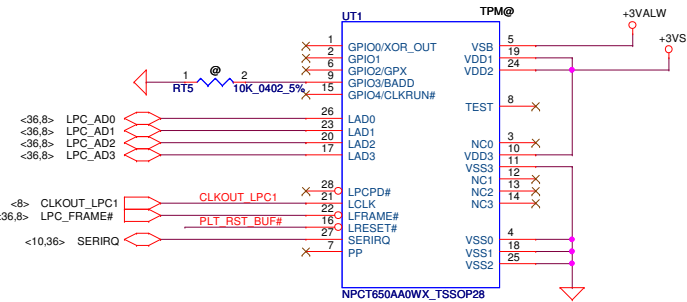
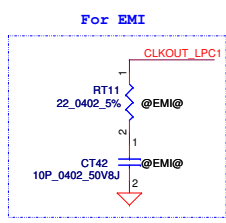
LAN	WOL	LAN_EN		ISOLATEB	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

* S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms

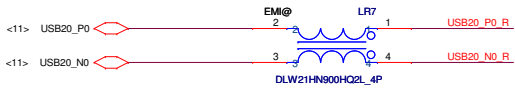
+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

TPM

BADD	ADDRESS
0	EEh - EFh
* Floating	7Eh - 7Fh

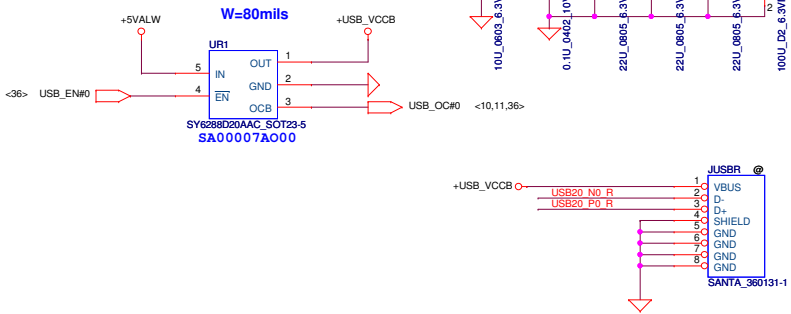


Right rear USB2.0 Conn.



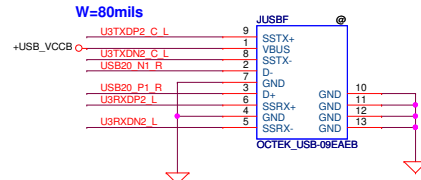
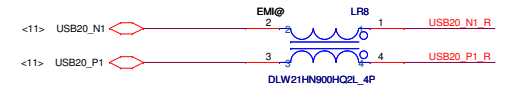
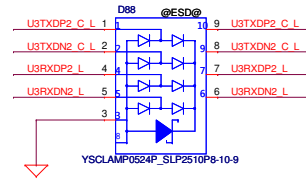
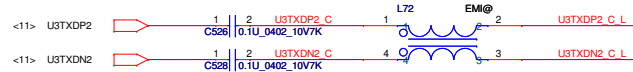
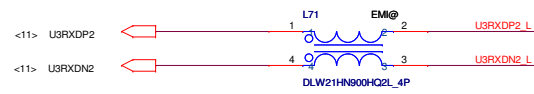
CLOSE UR1
W=80mils

Current Limit 2A

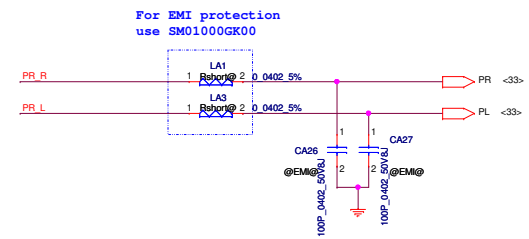
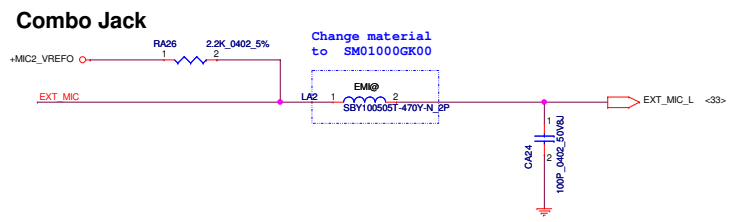
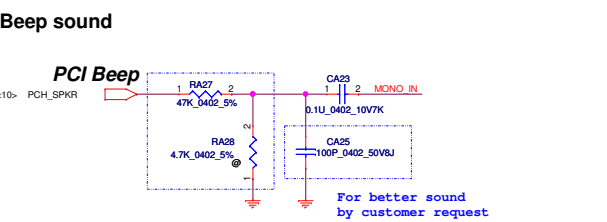
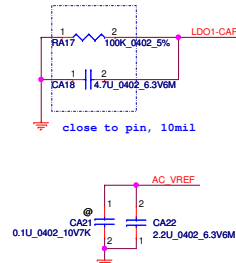
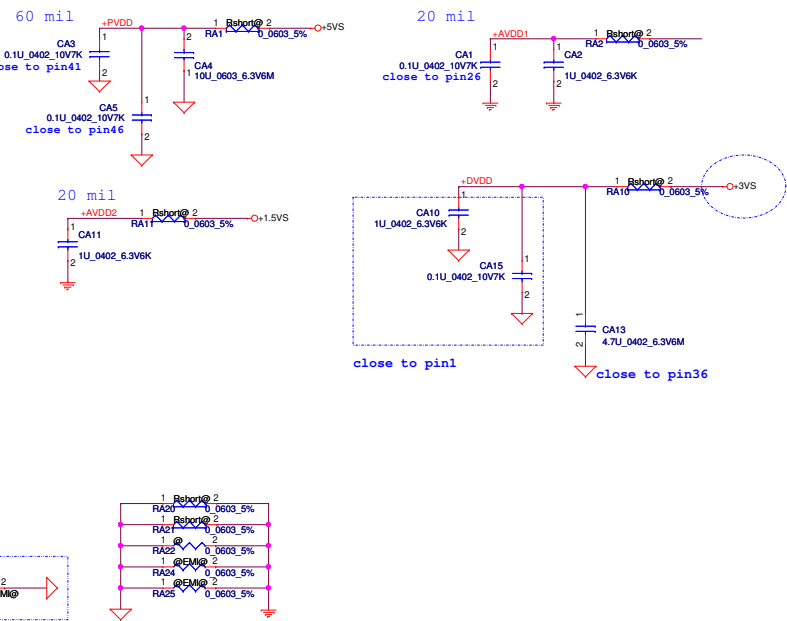
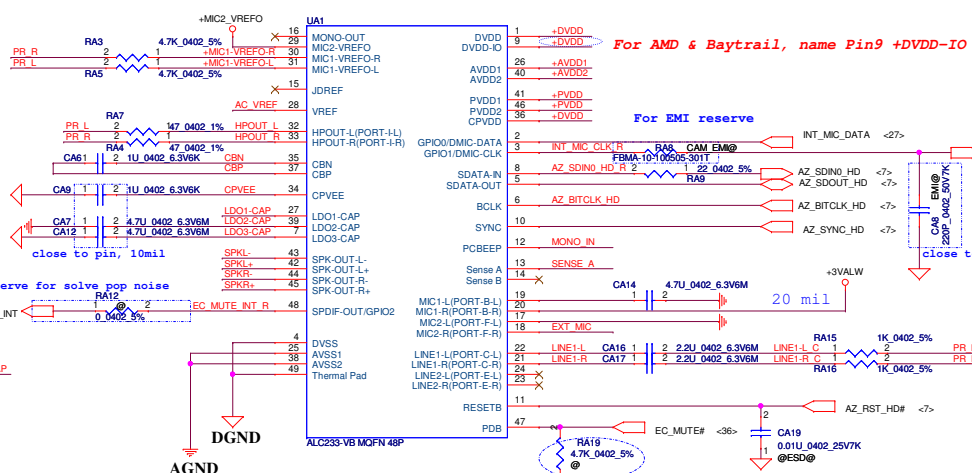


Right side USB 3.0 x 1 W/O Sleep&Charge

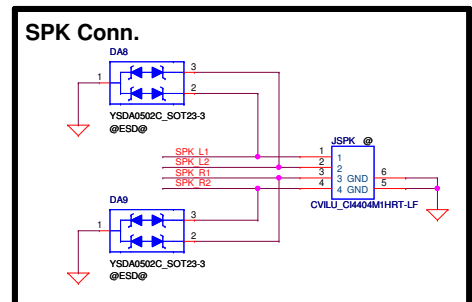
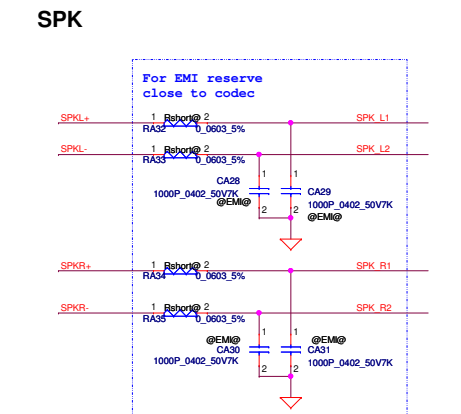
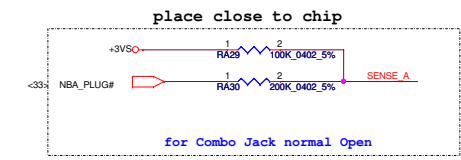
Change L71, L72, LR7, LR8 P/N
from SM070003Y00 to SM070003K00



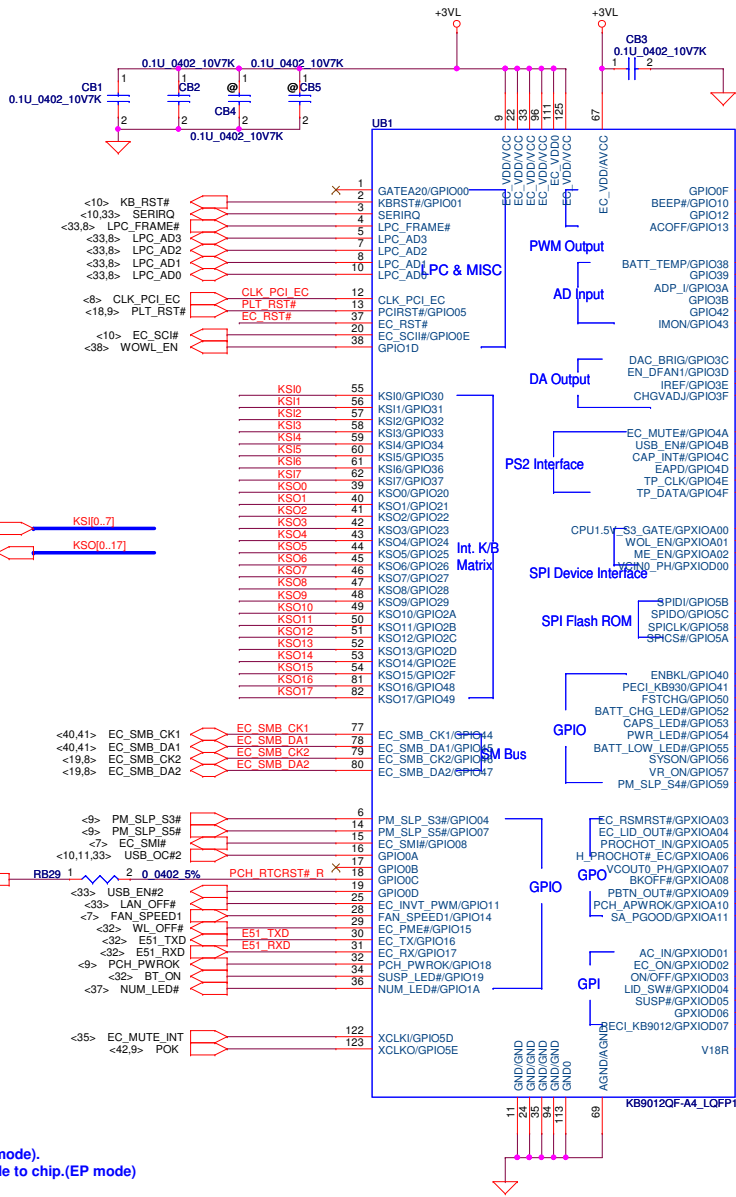
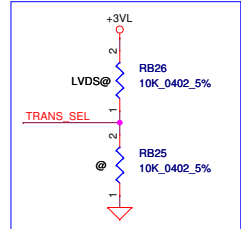
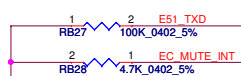
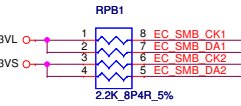
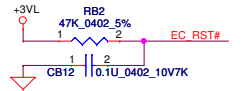
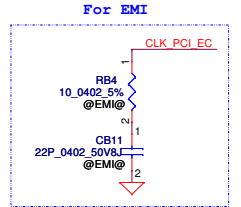
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(ALC233 supported iPhone headset/ Headphone/ MIC in)

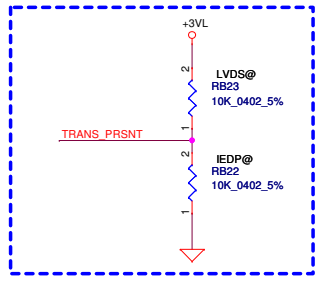


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Voltage Comparator Pins FOR 9012 A3

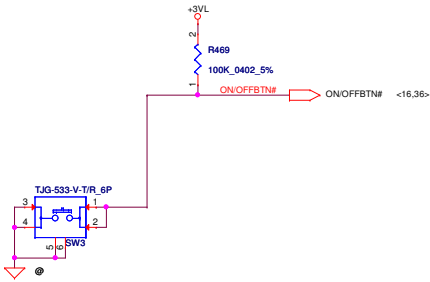
VCIN0 pin109	>1.2V	<1.2V
VCIN1 pin102		
VCOUT0 pin104	HIGH (default)	LOW
VCOUT1 pin103	HIGH	LOW (default)



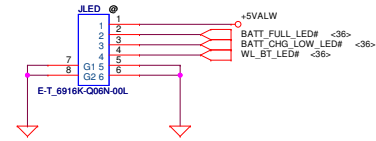
Signal pull high is default status (ROM only mode).
If signal pull low, EC will send translator code to chip.(EP mode)

Reserve TRANS_PRSENT for panel timing tuning.

Power Button

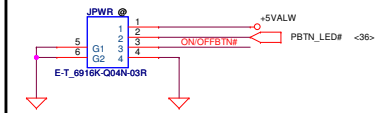


LED Small board to Conn

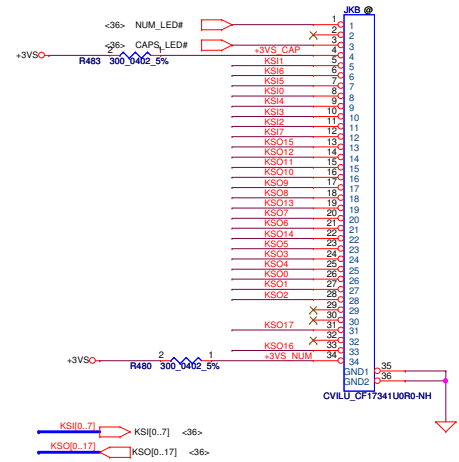


PBTN/B to M/B

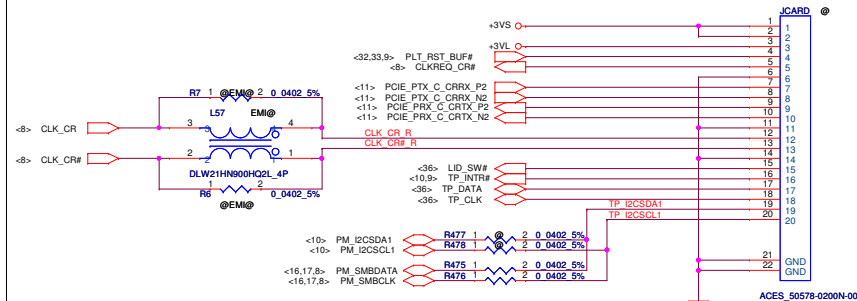
NOTICE: ON/OFFBTN# have pull-high resistance on motherboard



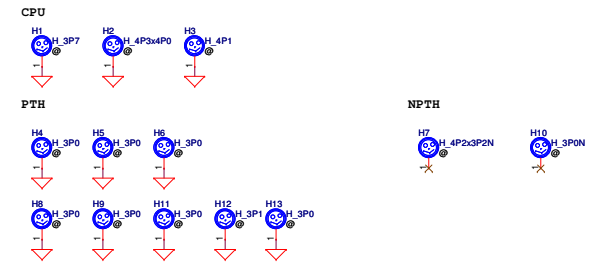
KEYBOARD CONN.



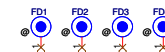
Card Reader + TP + Lid SW



Screw Hole



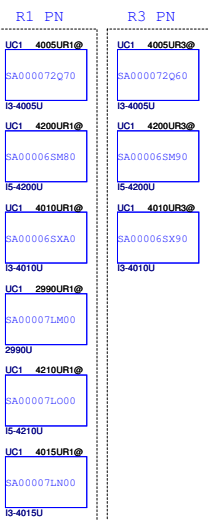
PCB Fedcal Mark PAD



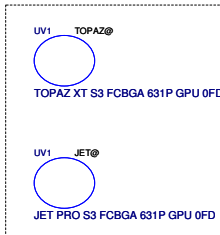
ISPD



CPU



GPU



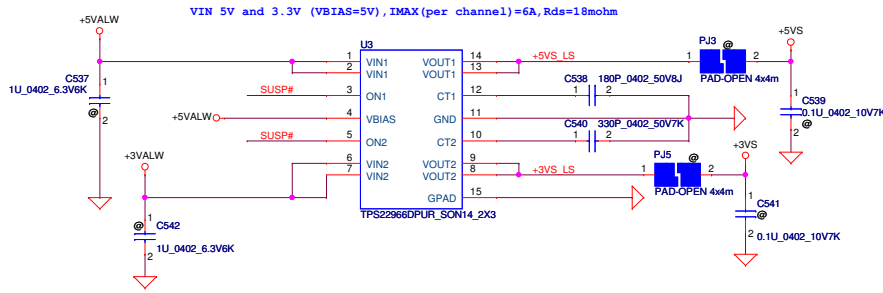
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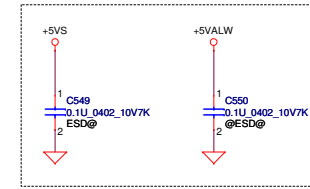
TP/ISPD/KB/Screw

ZSWAA/ZCWAA LA-B301P

+3VALW TO +3VS
+5VALW TO +5VS
Load Switch

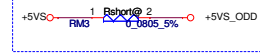


For ESD

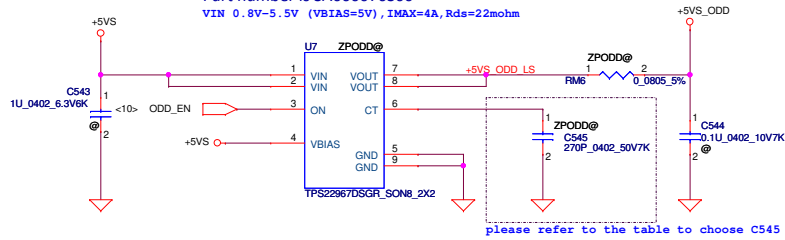


+5VS TO +5VS_ODD

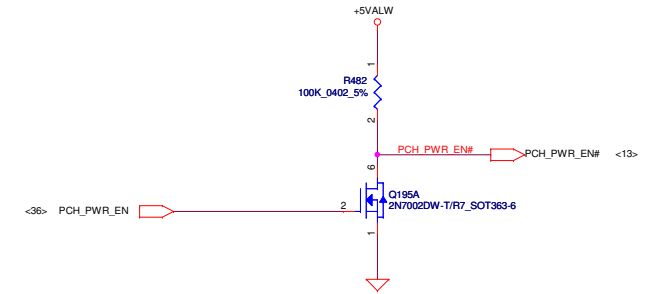
Need mount RM3 if system don't support ZPODD



Part number is SA000070S00
 VIN 0.8V-5.5V (VBIAS=5V), IMAX=4A, Rds=22mohm

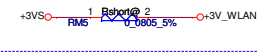


please refer to the table to choose C545

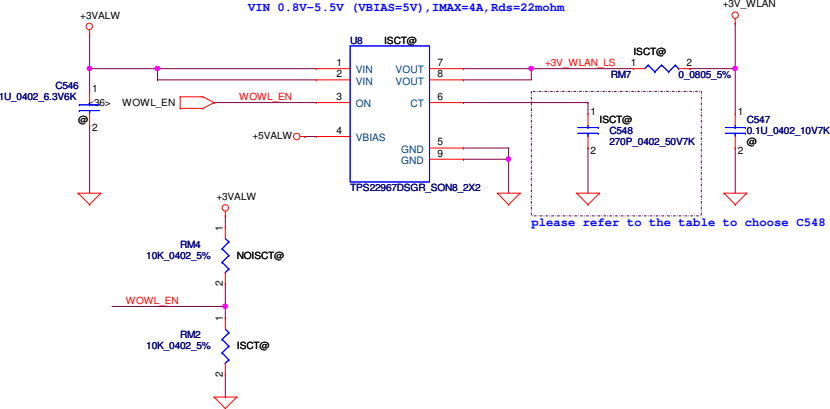


+3VALW TO +3V_WLAN
for WOWL

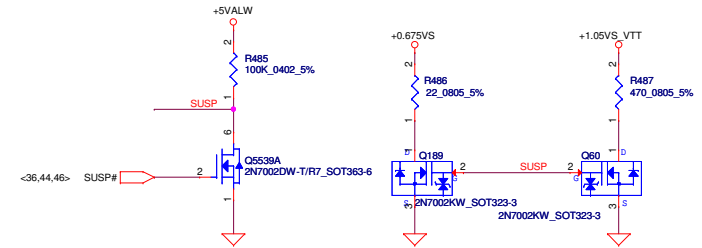
Need mount RM5 if system don't support ISCT



Part number is SA000070S00
 VIN 0.8V-5.5V (VBIAS=5V), IMAX=4A, Rds=22mohm



please refer to the table to choose C548

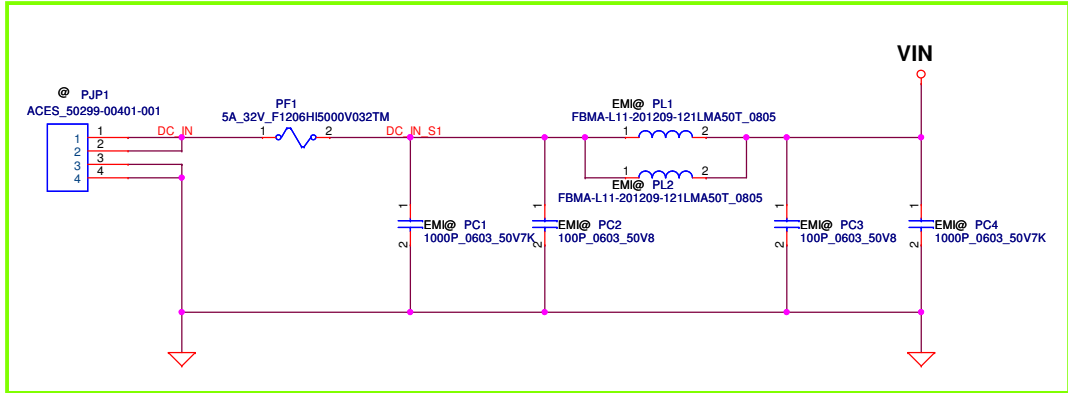


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Issued Date	2013/09/25	Deciphered Date	2016/09/25	Title
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				ZSWAA/ZCWAA LA-B301P
Date	Monday, February 10, 2014	Sheet	38	of 52

Mark Green frame that means this part is not belong to layout module part .

Function Field :

Support 37.1
 RTC 38.2
 EMI Part 47.1

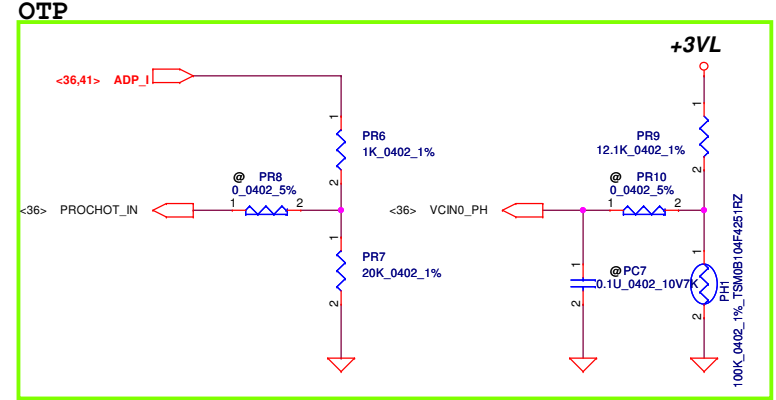
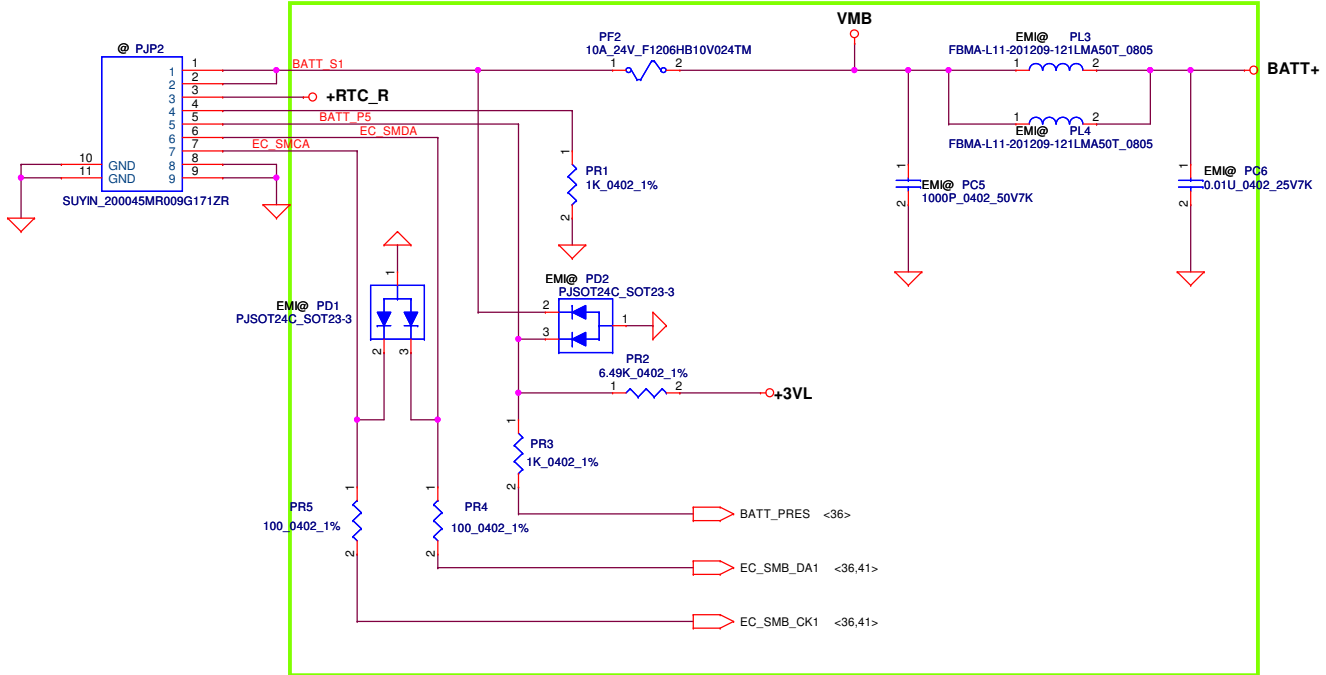


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title DCIN	
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Date: Monday, February 10, 2014				Sheet	Rev 1.0
				39	of 52

Mark Green frame that means this part is not belong to layout module part .

Function Field :

- Support 37.1
- OTP 39.7
- EMI Part 47.1
- ESD DIODE 47.2



	Initial	Recovery
45W UMA	0.55V	0.43V

	Initial	Recovery
CPU OTP	90 C	70 C

Module model information

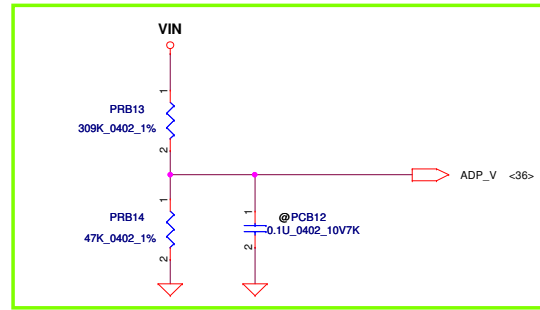
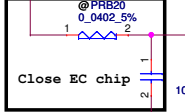
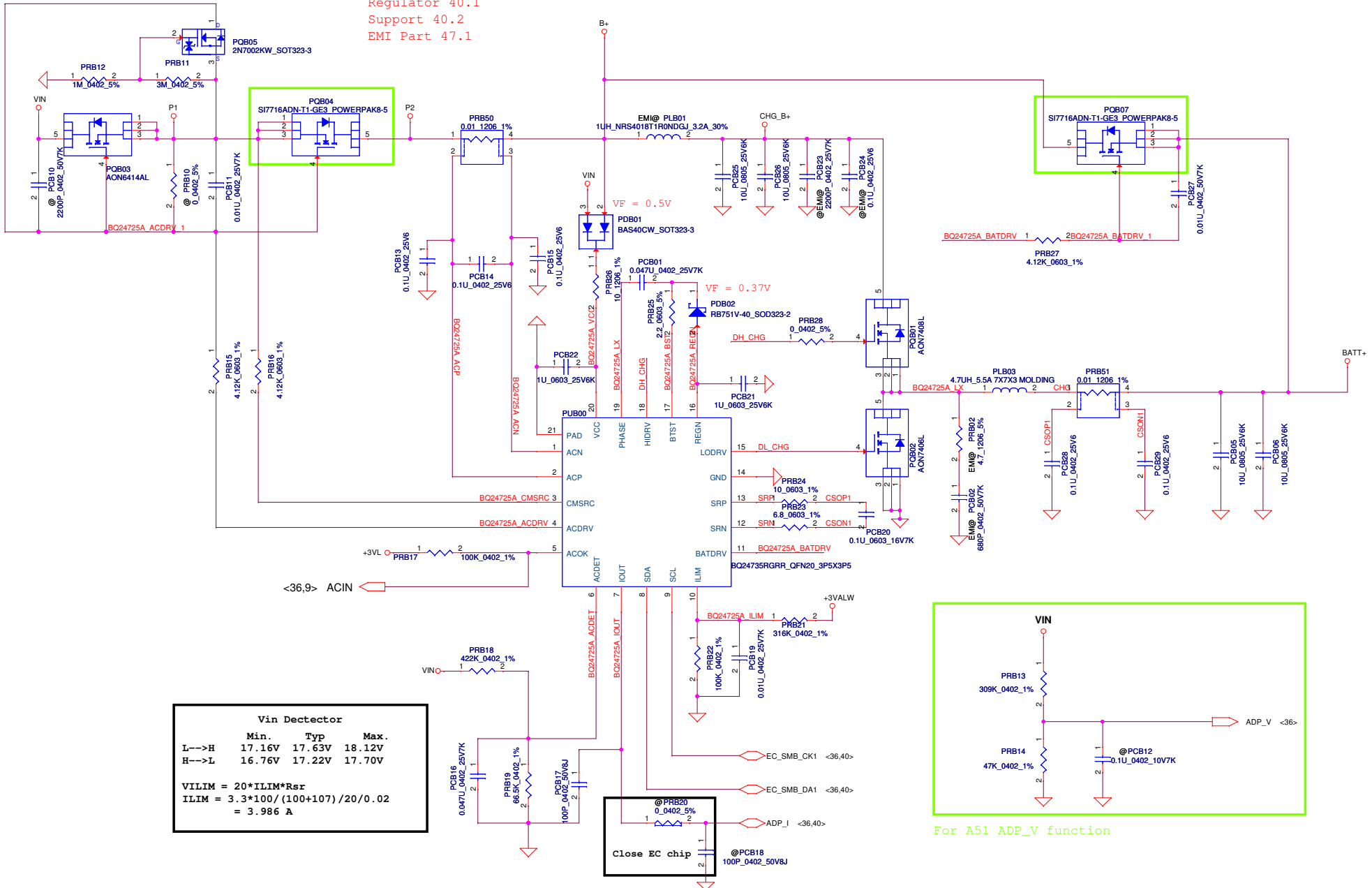
BQ24735A_V1.mdd

BQ24735A_V2.mdd

Mark Green frame that means this part is not belong to layout module part .

Function Field :

- Regulator 40.1
- Support 40.2
- EMI Part 47.1



For A51 ADP_V function

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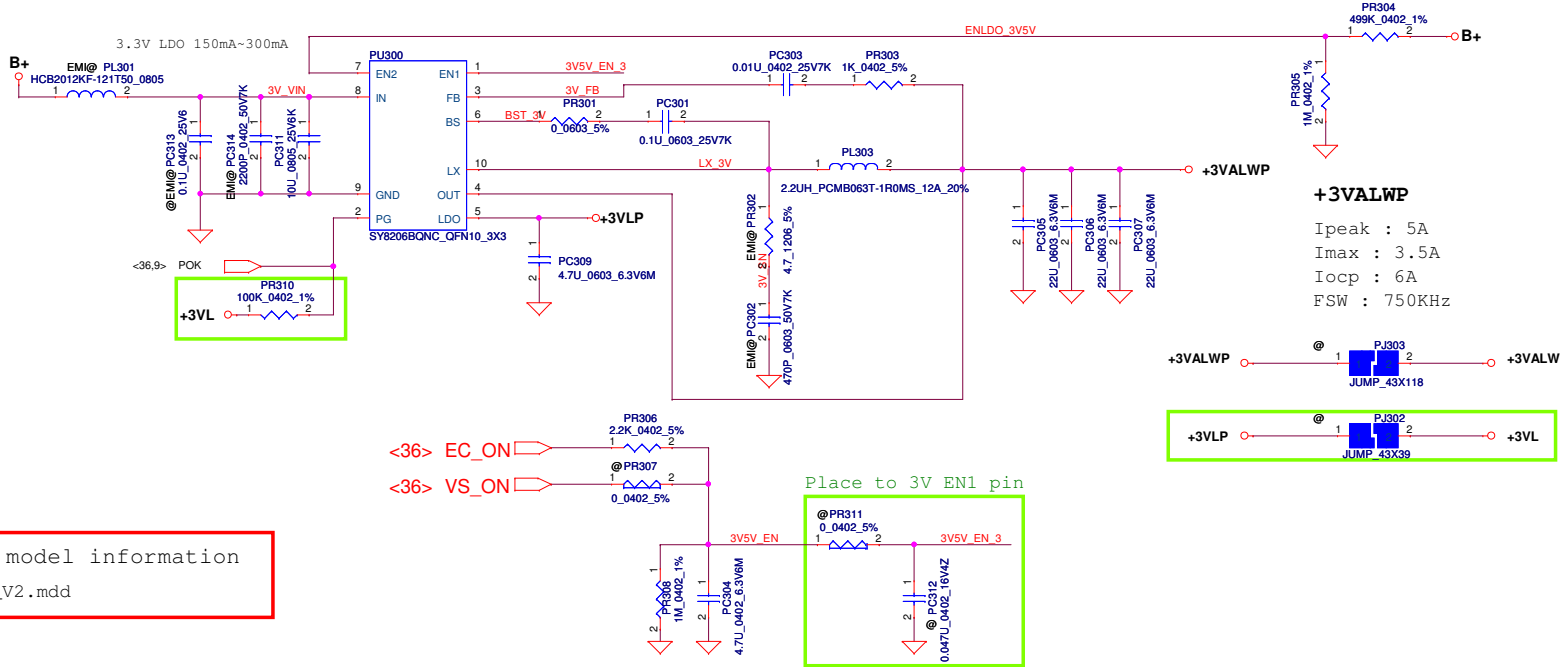
Module model information

SY8206B_V2.mdd

Mark Green frame that means this part is not belong to layout module part .

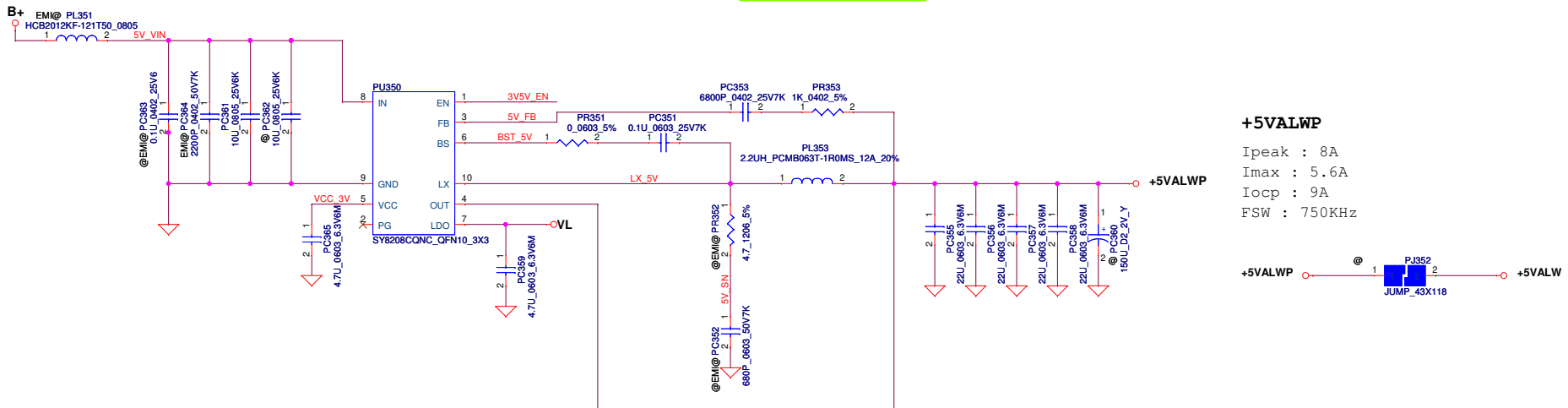
Function Field :

Regulator 35.1
Support 35.2
EMI Part 47.1



Module model information

SY8208C_V2.mdd



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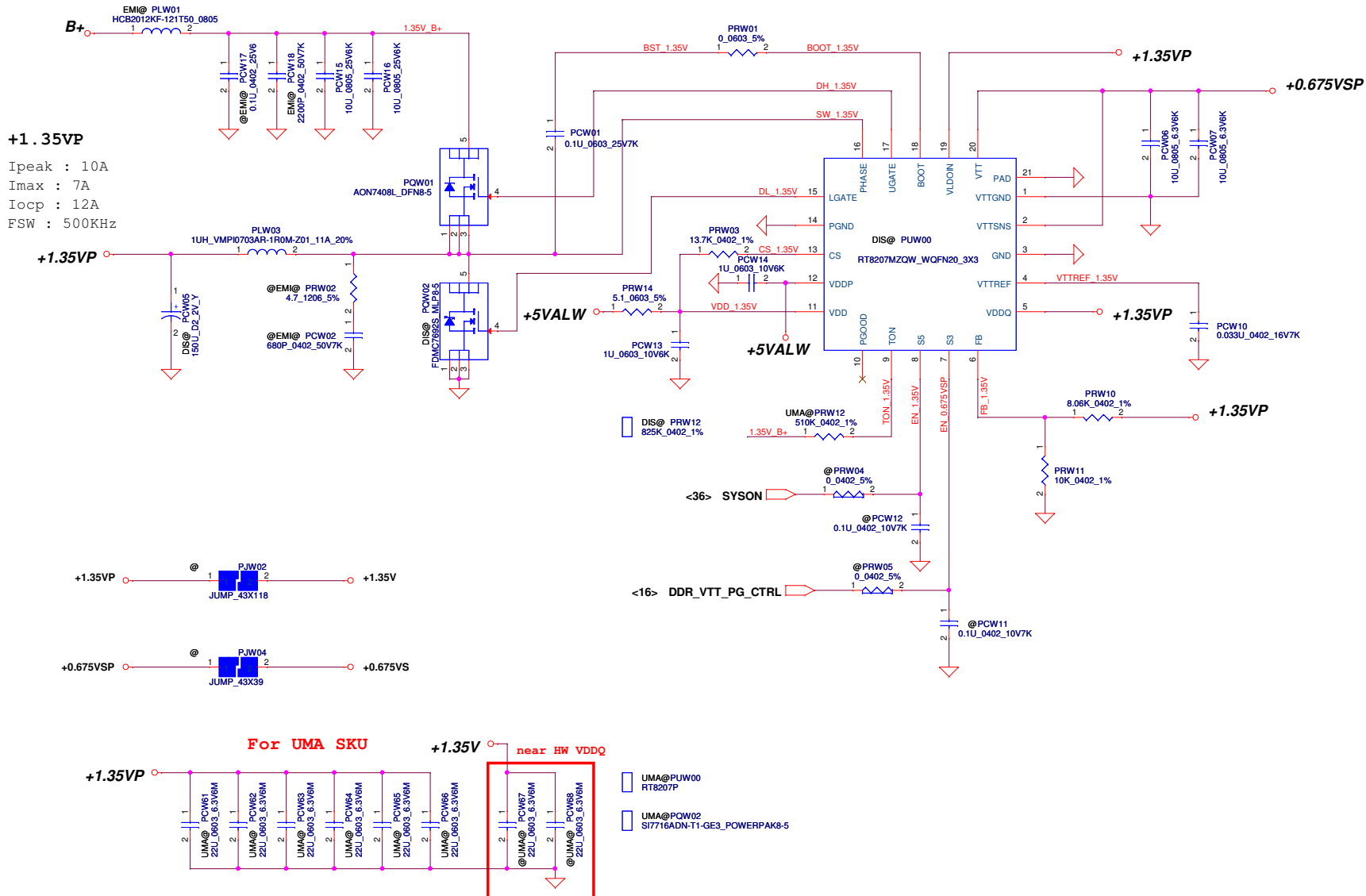
Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Mark Green frame that means this part is not belong to layout module part .

Function Field :

Regulator 35.3
Support 35.4
EMI Part 47.1



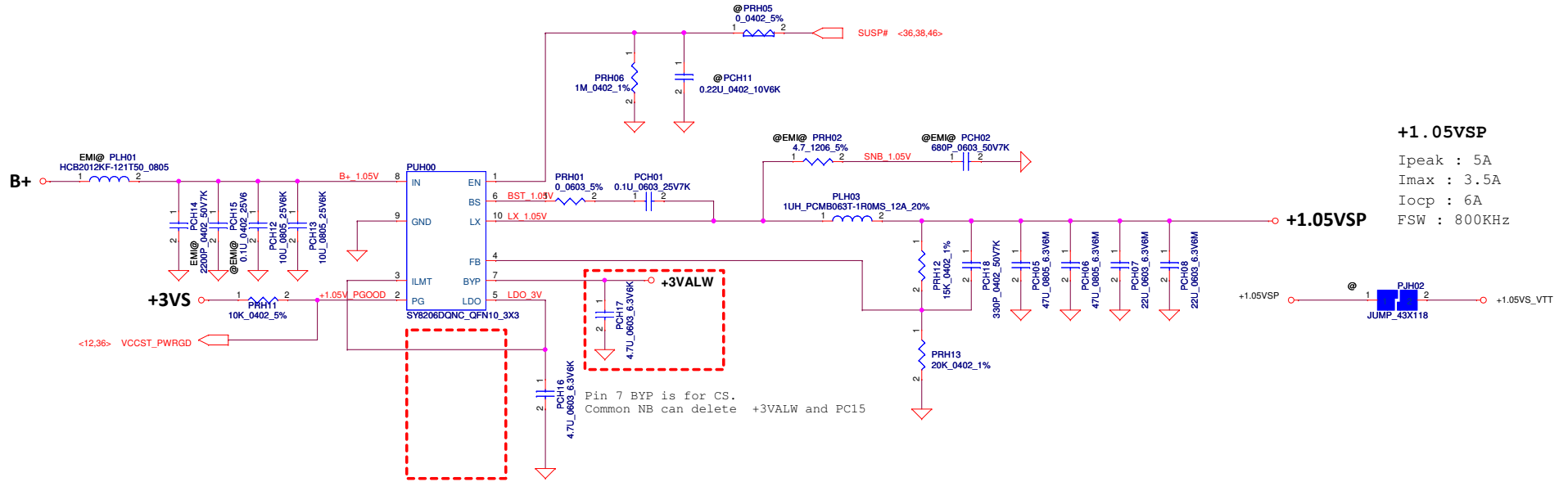
Security Classification	Compal Secret Data		Title	
Issued Date		Deciphered Date	Compal Electronics, Inc.	
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			Date: Monday, February 10, 2014	Sheet 43 of 52

Mark Green frame that means this part is not belong to layout module part .

Function Field :

Regulator 35.5
Support 35.6
EMI Part 47.1

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



+1.05VSP

Ipeak : 5A
Imax : 3.5A
Iocp : 6A
FSW : 800KHz

<12.36> VCCST_PWRGD

Pin 7 BYP is for CS.
Common NB can delete

+3VALW and PC15

The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

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Issued Date		Deciphered Date		+1.05VS	
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				ZSWAAZCWAAL A-B301P	1.0
Date: Monday, February 10, 2014				Sheet	44 of 52

Module model information
SY8033_V1.mdd

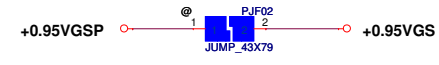
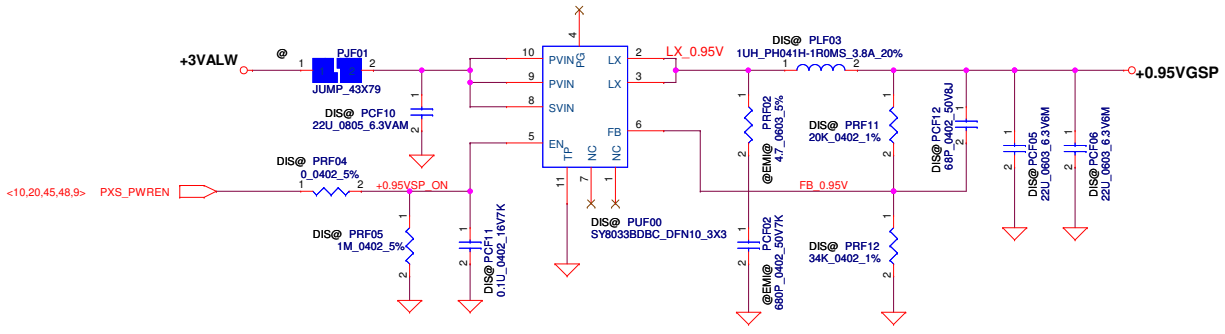
Mark Green frame that means this part is not belong to layout module part .

Function Field :

Regulator 35.15
Support 35.16
EMI Part 47.1

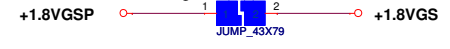
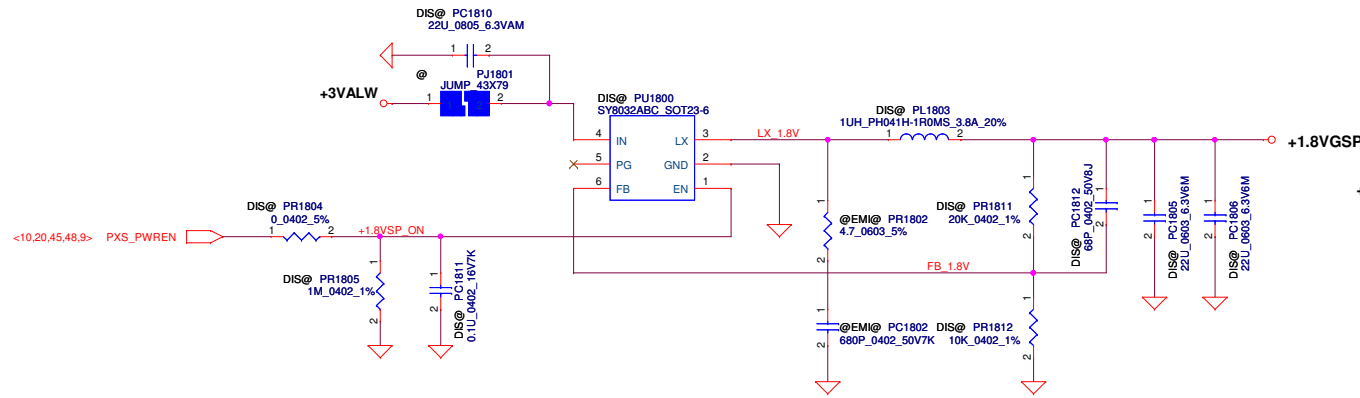
+0.95VGSP

Ipeak : 3A
Imax : 2.1A
Iocp : 4A
FSW : 1MHz



+1.8VGSP

Ipeak : 1A
Imax : 0.7A
Iocp : 2.5A
FSW : 1MHz



Note: Use VCCSA_SEL to switch High & Low Level for VID[1] (ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

Security Classification	Compal Secret Data			Compal Electronics, Inc. +0.95VGS / +1.8VS		
Issued Date		Deciphered Date				
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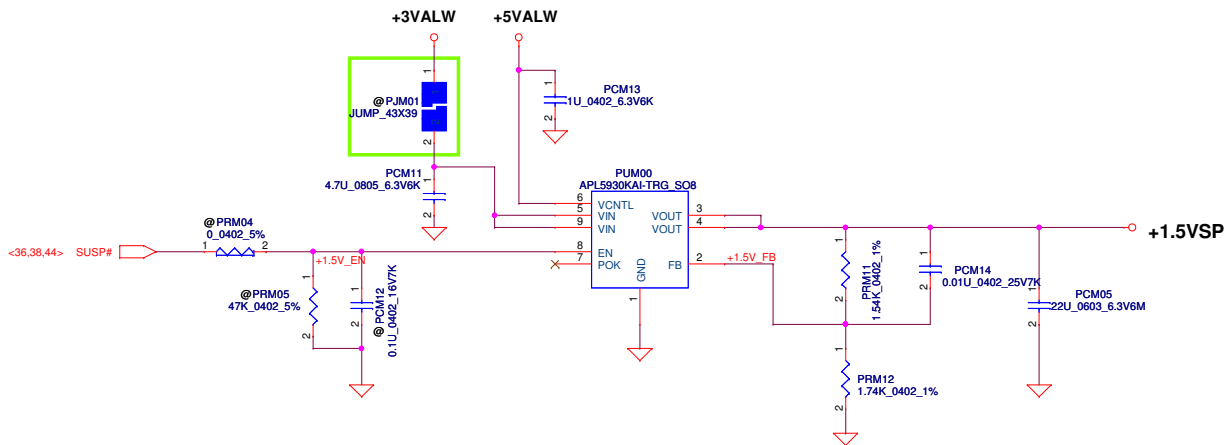
Module model information

APL5930_V1.mdd

Mark Green frame that means this part is not belong to layout module part .

Function Field :

Regulator 35.31
Support 35.32
EMI Part 47.1



+1.5VSP

I_{peak} : 0.5A
I_{max} : 0.35A
I_{ocp} : 4.2A



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Module model information

TPS51622_V2A.mdd for IC portion
 TPS51624_V2B.mdd for SW portion

Mark Green frame that means this part is not belong to layout module part .

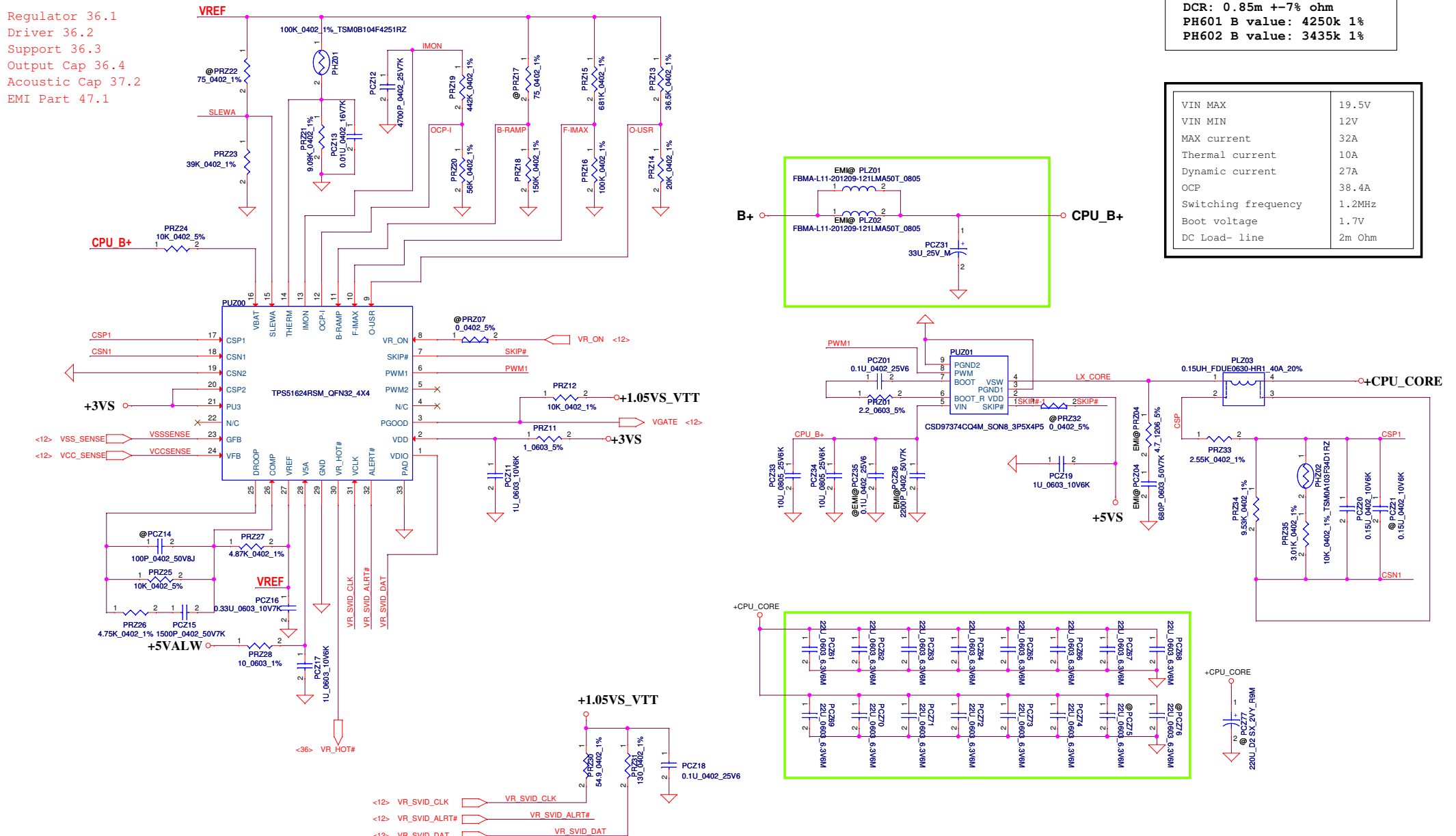
Function Field :

- Regulator 36.1
- Driver 36.2
- Support 36.3
- Output Cap 36.4
- Acoustic Cap 37.2
- EMI Part 47.1

VR_HOT#
 PR606 10K ohm for 100 degree
 PR606 8K ohm for 110 degree

CPU
 Frequency = 1MHz
 OCP Current 39 A
 DCR: 0.85m +-7% ohm
 PH601 B value: 4250k 1%
 PH602 B value: 3435k 1%

VIN MAX	19.5V
VIN MIN	12V
MAX current	32A
Thermal current	10A
Dynamic current	27A
OCP	38.4A
Switching frequency	1.2MHz
Boot voltage	1.7V
DC Load- line	2m Ohm

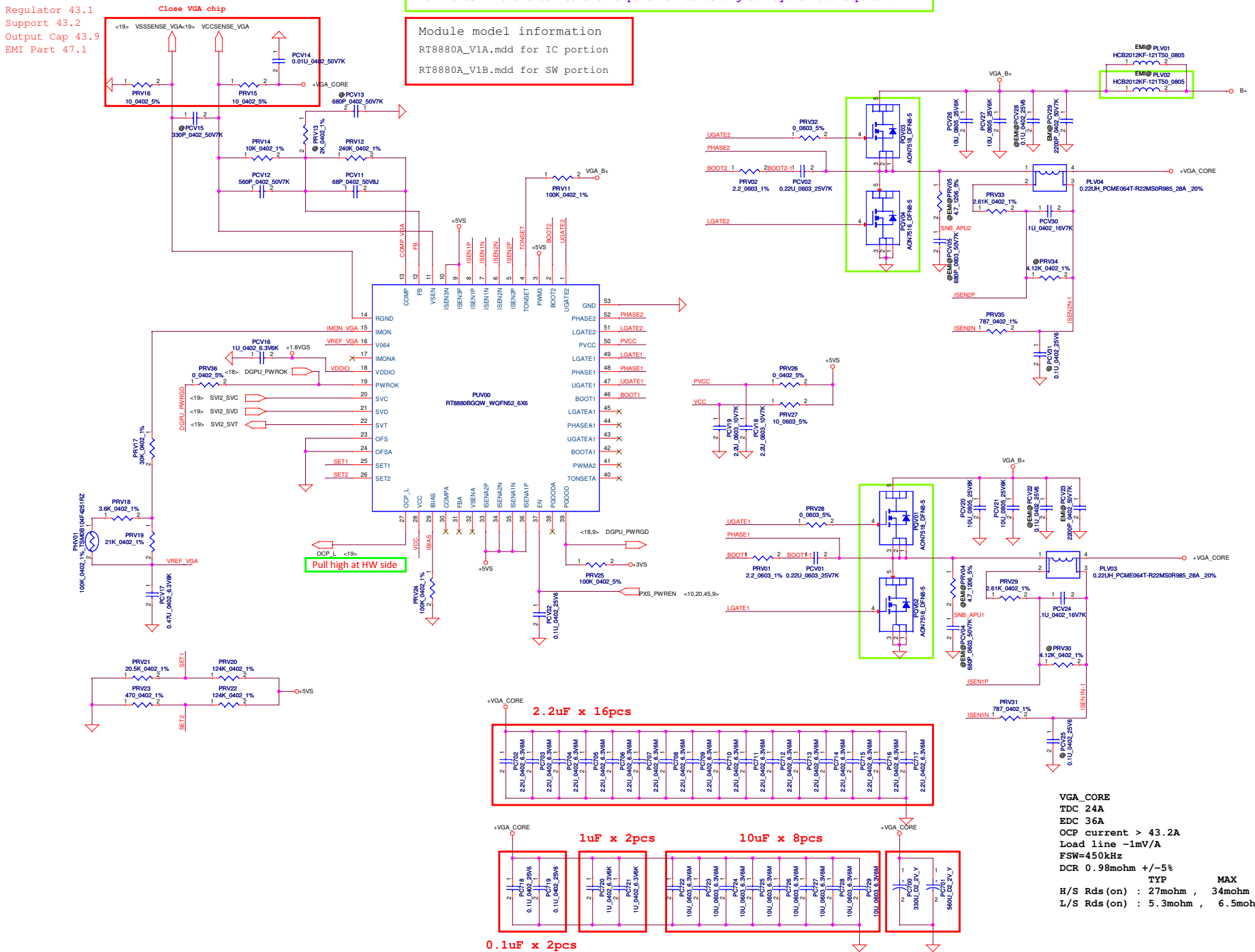


Function Field :

Regulator 43.1
 Output 43.2
 Output Cap 43.9
 EMI Part 47.1

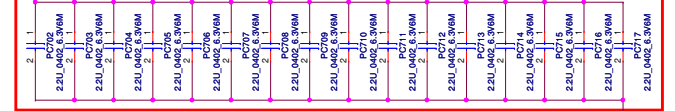
Mark Green frame that means this part is not belong to layout module part .

Module model information
 RT8880A_V1A.mdd for IC portion
 RT8880A_V1B.mdd for SW portion



Pull high at HW side

2.2uF x 16pcs



0.1uF x 2pcs

1uF x 2pcs

10uF x 8pcs



VGA_CORE
 TDC 24A
 EDC 36A
 OCP current > 43.2A
 Load line -1mV/A
 FSW=450kHz
 DCR 0.98mohm +/-5%
 TYP MAX
 H/S Rds (on) : 27mohm , 34mohm
 L/S Rds (on) : 5.3mohm , 6.5mohm

Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		VGA_CORE	
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PWR PIR (Product Improve Record)

ZSWAA LA-B301P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.2

PVT GERBER_OUT DATE: 2013/12/02

Item	Date	Page	Action	Component	Request
1)	11/21	48	Change	PRZ12 change to 10K and pull high +1.05VS_VTT	For design change
2)	11/21	48	Delete	PRZ29 removed	HW portion pull high
5)	11/25	41, 48	Change	PH1,PHZ01 part number change to SL200002H00	change for common PN
6)	11/25	48	Change	PHZ02 part number change to SL200002F00	change for common PN
7)	11/25	42	Change	change PQB03 to SB000000NW00 AON6414AL	change for allocation
8)	12/03	48	Change	PRZ27 change to 4.87K	change for compensation
9)	12/03	41	Change	PF2 change to 1206 footprint component SP040005P00	for ME limitation
10)	12/03	44	Change	change PQW02 to SB000000GW00 SI7716 at UMA SKU	change for allocation
11)	12/03	48	Change	PRZ19 change to 316K	for CPU core conversation fine tune
12)	12/03	48	Change	PRZ20 change to 56K	for CPU core conversation fine tune

REVISION CHANGE: 0.3

PV REGRESSION GERBER_OUT DATE: 2014/01/06

Item	Date	Page	Action	Component	Request
13)	01/03	40	Change	change DC in jack footprint	for customer request
14)	01/03	43	Add	Add PR312 0ohm 0402	for HW 5V drop fine tune
15)	01/08	43	Change	change PR312 to 15ohm	for HW 5V drop fine tune
16)	01/08	47	Change	change PRZ19 to 442kohm	for CPU core conversation fine tune
17)	01/15	41	Delete	PCB10 2200p	for B2B fine tune
18)	01/15	41	Change	PCB11 0.1u change to 0.01u	for B2B fine tune
19)	01/16	43	Add	PR302,PC302 mount and PC302 change to 470p	for EMI request
20)	01/16	42	change	PCB16 2200p change to 0.047u	for decoupling cap fine tune
21)	01/22	47	Add	PRZ04,PCZ04 mount	for EMI request
22)	01/22	41	Add	PRB02,PCB02 mount	for EMI request
23)	01/22	47	change	PCZ31 100u change to 33u	for sourcer request

REVISION CHANGE: 1.0

Pre-MP GERBER_OUT DATE: 2014/02/10

Item	Date	Page	Action	Component	Request
24)	02/07	42	Delete	remove PR312 15ohm	for HW request
25)	02/07	48	Change	change net name from VREF to VREF_VGA change net name from VREF to IMON_VGA change net name from VREF to COMP_VGA	resolve duplicate net name
26)	02/10	42, 44, 46	Change	change PR311,PRH05,PRM04 footprint to 0ohm shortpad	common design rule

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Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title	Power-PIR	
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HW PIR (Product Improve Record)

ZSWAA LA-B301P Schematic Change List

REVISION: 0.1

Gerber-out date: 2013/10/29

Item	Date	Page	Action	Component	Request
1)	10/15	37	Add	CB14 on SUSP#	For ESD request
2)	10/15	16, 17	Change	Swap DDR data of JDIMM1 & JDIMM2	For common module layout
3)	10/15	08	Add	RH91 on CLK_REQ_VGA#	For follow AMD GPU reference schematic
4)	10/15	34	Reserve	CR6 to +5VALW	For power switch common design
5)	10/15	35	Add	CR2, CR3, CR5 to +USB_VCCB	For power switch common design
6)	10/16	37	Add	RB11, RB12	For colay EC 9022
7)	10/16	37	Add	RB13, RB14	For colay Normal pad & Click pad
8)	10/17	38	Add	R8, R9	For colay Normal pad & Click pad
9)	10/17	27	Add	R15, C29 on LCD_ENVDD	For tune LCD_VDD sequence
10)	10/18	34	Swap	LR9	For smooth USB signal
11)	10/18	37	Change	DFAN1 to Pin 70	For EC request
12)	10/20	34	Remove	RT2, RT3	For no need
13)	10/22	39	Change	RM5, RM6, RM7 to 0_0805	For max current design
14)	10/22	10	Add	Test point on GPIO10	For SW debug
15)	10/22	07	Add	Test point on GPIO34	For SW debug
16)	10/23	16	Reserve	0_0805	For DQA's experiment
17)	10/23	05	Change	R23 to 121_0402_1%	For Intel check list
18)	10/23	38	Remove	SW2	For layout space concern
19)	10/23	30	Reserve	RD11, RD12	For Intel check list
20)	10/24	08	Change	Y2 to 4 pin	For common part
21)	10/24	10	Add	RH4, RH6, RH9, RH10	For SW request
22)	10/24	26	Change	RT1 from 0603 to 0805	For current concern
23)	10/24	09	Add	RH7, RH8	For SW request
24)	10/24	27	Change	JTOUCH from 4pin to 6pin	For module pin define
25)	10/27	20	Change	QV5 to AO4354	For sourcer request
26)	10/27	34	Change	UT1 P/N to SA00007IO00	For TPM2.0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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HW PIR (Product Improve Record)

ZSWAA LA-B301P Schematic Change List

REVISION: 0.2

Gerber-out date: 2013/12/2

Item	Date	Page	Action	Component	Request
01)	11/22	36	Delete	RA22	For audio codec
02)	11/22	36	Add	Add a reserve 0ohm resistor RA25	For EMI request
03)	11/22	27	Change	Change D15 P/N from SCS00002G00 to SCS00000Z00	For material shortage
04)	11/22	27, 29, 34, 35	Change	Change L10, L11, L62, L71, L72, L8, L9, LR7, LR8, LR9 P/N from SM070003Y00 to SM070003K00	For material shortage
05)	11/22	05	Change	Change R184 from SD013470080 to SD028470080	The same as CRB board
06)	11/26	26	Change	Change RT14 config. from @ to LVDS@	For BKOFF circuit
07)	11/26	09	Change	Change RH19 config. to IEDP@	For BKOFF circuit
08)	11/26	09	Connect	Connect EC_ENBKL_R_CPU to AND GATE U50.1	For BKOFF circuit
09)	11/26	27	Change	Change U50.1 from EC_ENBKL_R to EC_ENBKL_R_CPU	For BKOFF circuit
10)	11/26	27	Change	Change U50 and R433 config. from IEDP@ to always mount	For BKOFF circuit
11)	11/26	27	Change	Change D15 and R436 config. from LVDS@ to @	For BKOFF circuit
12)	11/26	36	Change	Change UB1.26 (EC GPIO12) from NC to TRANS_PRSNLT	For BKOFF circuit
13)	11/26	36	Add	Add a pull high 10Kohm (RB23) to +3VL and a pull down 10Kohm (RB22) to GND on TRANS_PRSNLT	For BKOFF circuit
14)	11/27	27	Change	Change D15 P/N from SCS00000Z00 to SCS0340L010	For BOM reduce
15)	11/27	29	Change	Change UD1.25, UD1.31, UD1.22, UD1.32 from +1.8VS_RXVCC to +1.8VS_CRT	For DP to CRT translator
16)	11/27	29	Change	UD1.45 pull high from +3VS to +3VS_6513	For DP to CRT translator
17)	11/27	29	Add	Add test point on UD1.37	For DP to CRT translator
18)	11/27	29	Add	Add RPD2 symbol for 150ohm	For DP to CRT translator
19)	11/27	33	Change	Change LAN/USB Small board Connector pin (JLAN.3 to JLAN.6) define	For LAN/USB Small board
20)	11/27	35	Change	Change UA1 all analog output net name to PR_L/PR_R	Unify net name
21)	11/27	35	Change	Change CA15 0.1u cap from 16V4Z to 10V7K	Don't need to use 16V4Z
22)	11/27	35	Change	Add net name Line1-L_C & Line1-L_R on UA1 pin 21.22	For trace length table
23)	11/27	35	Detete	Delete ALC233 co-lay component RA6, RA30, UA1	Change to ALC233VB Only
24)	11/27	35	Change	Swap RA21 & RA22 BOM structure	Balance caps alignment
25)	11/28	29	Change	Change test point T2 to a pull high 10Kohm (RD13) to +3VS_6513	For DP to CRT translator
26)	11/28	27	Add	Add a reserved ESD diode (D92) for JTOUCH	For ESD reueset
27)	11/28	07	Change	Change Dual ESD diode (D13) to two single diodes (D16, D17)	For RTC circuit
28)	11/28	07	Change	Change R437.1 connecting from +RTCBATT to +RTCVCC	For RTC circuit
29)	11/29	07	Change	Change R437 from 0ohm to 1kohm	For RTC circuit
30)	11/29	33, 37	Change	Change L56, L57 from SM070001U00 to SM070003K00	For EMI request
31)	11/29	33, 37	Change	Change L56, L57 from @EMI@ to EMI@	For EMI request
32)	11/29	33, 37	Change	Change R4, R5, R6, R7 from EMI@ to @EMI@	For EMI request
33)	11/29	34	Change	Change CR2, CR3, CR5 from 22U_0603 to 22U_0805	For droop issue
34)	11/29	35	Change	Change CA15 from SE076104K80 to SE102104K00	For BOM change
35)	11/29	07	Change	Change R277.2 net name from N113579902 to +RTCBATT_R	For RTC circuit
36)	12/01	33, 37	Change	Swap L56, L57 pin define	For layout request
37)	12/01	27	Add	Add R9, R11 on EMI camera choke	For EMI request
38)	12/01	27	Change	Change L62 from CAM_EMI@ to @CAM_EMI@	For EMI request

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Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title	
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HW PIR (Product Improve Record)

ZSWAA LA-B301P Schematic Change List

REVISION: 0.3

Gerber-out date: 2014/01/06

Item	Date	Page	Action	Component	Request
01)	12/12	09	Change	Change RH19 BOM structure from IEDP@ to always mount	For LVDS & eDP cost down plan
02)	12/12	26	Change	Change RT14 BOM structure from LVDS@ to @	For LVDS & eDP cost down plan
03)	12/12	27	Delete	Delete U50,R433	For LVDS & eDP cost down plan
04)	12/12	27	Change	Change D15,R436 BOM structure from @ to always mount	For LVDS & eDP cost down plan
05)	12/12	36	Change	Change RB22 BOM structure from @ to IEDP@	For LVDS & eDP cost down plan
06)	12/12	36	Change	Change RB23 BOM structure from @ to LVDS@	For LVDS & eDP cost down plan
07)	12/12	07	Change	Change R277,D17 BOM structure from always mount to @	For RTC circuit
08)	12/12	07	Change	Change R437 BOM structure from @ to always mount	For RTC circuit
09)	12/30	11	Add	Add two reserved resistors R167,R168	For no use USB over current
10)	12/30	11	Change	Change UC1.AL3 connect to USB_OC#0_R	For no use USB over current
11)	12/30	11	Change	Change UC1.AH2 connect to USB_OC#2_R	For no use USB over current
12)	01/03	34	Add	Add a reserved capacitor CR7 on +USB_VCCB	For USB
13)	01/03	13	Add	Add a jumper PJ2 between +3VALW to +3VALW_PCH	For +3VALW to +3VALW_PCH
14)	01/06	38	Add	Add C549 and C550	For ESD's request
15)	01/06	37	Change	Change JLED footprint from E-T_6916K-Q06N-00L_6P to ACES_51524-0060N-001_6P	For DFX's request
16)	01/06	37	Change	Change JPWR footprint from E-T_6916K-Q04N-03R_4P to ACES_50504-0040N-001_4P	For DFX's request
17)	01/06	35	Change	Change UA1 Compal PN from SA00007BF00 to SA00007BF10	For audio codec
18)	01/07	13	Change	Change CH111,CH112,CH113,Q10,RH3 BOM structure from always mount to @	For +3VALW to +3VALW_PCH
19)	01/14	27	Change	Change D29 BOM structure from @ESD@ to ESD@	For ESD's request

ZSWAA LA-B301P Schematic Change List

REVISION: 1.0

Gerber-out date: 2014/02/10

Item	Date	Page	Action	Component	Request
01)	01/21	07,09,27	Change	Change D90,D91,D15,D16,D21,D17 from SCS0340L010 to SCS00003500.	For X code
02)	01/21	31	Change	Change JHDD footprint from SANTA_191503-1_22P-T to LCN_ASF98-2231S10-0002_22P.	For DFX's request
03)	01/21	37	Change/Add	Change CPU R1 BOM config and add R3 BOM config	For CPU BOM config
04)	01/29	33,36	Add	Add a GPIO pin LAN_OFF# for UB1.25 and connected to JLAN.3	For Disable/Enable LAN chip
05)	01/29	36	Add	Add a GPIO pin PCH_RTCRST#_R for UB1.18 and connected to a 0ohm resistor (RB29) and connected to PCH_RTCRST#.	For RTC reset
06)	01/29	34	Add	Add a reserved capacitor 100uF (CR14) for +USB_VCCB.	For USB droop
07)	02/05	07,09,27,35	Change	Change 0ohm resistor (RH19,R436,R32,R431,R432,RA11,RA1,RA2,RA10,R106) footprint to 0ohm short pad.	For 0ohm short pad
08)	02/05	35	Delete/Change	Delete RA13,RA18 and change UA1.18 to EXT_MIC and UA1.20 to +3VALW	For audio codec
09)	02/05	37	Change	Change SW3 BOM config from mount to un-mount.	For Pre-MP phase
10)	02/06	26,27,29,35	Change	Change 0ohm resistor (RT1,RD1,LD2,RA20,RA21,R4280,R4281,R11,R9) footprint to 0ohm short pad, and BOM config to Rshort@.	For 0ohm short pad
11)	02/07	07,09,12,27,35,16,17,36	Change	Change 0ohm resistor (RH19,R65,R178,R235,R174,R211,R212,R231,R436,LA1,LA3,RB34,RB1,R32,R431,R432,RA32,RA33,RA34,RA35,RA11,RA1,RA2,RA10,R106) BOM config to Rshort@.	For 0ohm short pad
12)	02/07	34	Delete	Delete CR7.	For USB droop
13)	02/07	38	Change	Change 0ohm resistor (RM3,RM5) footprint to 0ohm short pad, and BOM config to Rshort@.	For 0ohm short pad
14)	02/10	37	Change	Change screw hole size for H1,H2,H3.	For ME's request

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