**Compal Confidential**

MODEL NAME : ZIVY1

PCB NO : LA-B131P

BOM P/N : SKU1_4519RY38L05 (I5-4200U 1.6GHZ - Hynix 2G)
SKU2_4519RY38L05 (I5-4200U 1.6GHZ - Micro 2G)
SKU3_4519RY38L08 (I7-4500U 1.8GHZ - Hynix 4G) FAI
SKU3_4519RY38L08 (I7-4510U 1.8GHZ - Hynix 4G) main SMT
SKU4_4519RY38L07 (I2-4200U 1.6GHZ - Micro 4G)
SKU5_4519RY38L05 (I5-4200U 1.6GHZ - Samsung 2G)
SKU6_4519RY38L07 (I5-4200U 1.6GHZ - Samsung 4G)

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## Lamborghini Y40 M/B Schematics Document

### Intel Haswell / Broadwell ULT Processor + AMD Venus XTX

2014-03-03

REV:1.0

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Title: *Cover Sheet*

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Date: Tuesday, March 04, 2014 | Sheet 1 of 52

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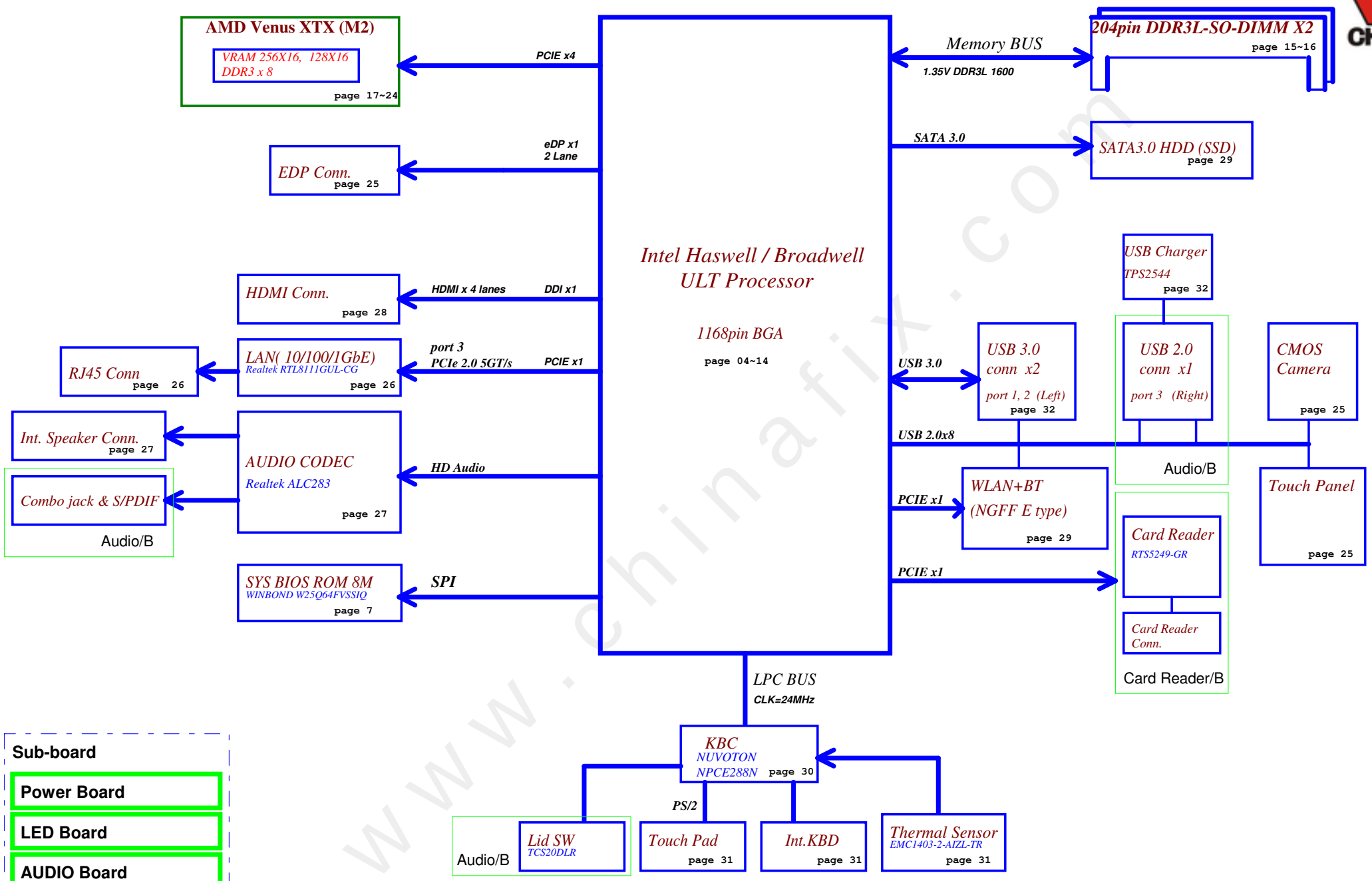


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Title: Block Diagram

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## Voltage Rails

| State \ power plane | B+ | +5VALW<br>+3VALW | +1.35V | +5VS<br>+3VS<br>+1.5VS<br>+1.05VS<br>+CPU_CORE<br>+0.675VS<br>+VGA_CORE<br>+MEM_GFX<br>+3VGA<br>+1.8VGA<br>+VGA_PCIE |
|---|---|---|---|---|
| S0 | O | O | O | O |
| S3 | O | O | O | X |
| S5 S4/AC | O | O | X | X |
| S5 S4/ Battery only | X | X | X | X |
| S5 S4/AC & Battery don't exist | X | X | X | X |

| STATE \ SIGNAL | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V | +VS | Clock |
|---|---|---|---|---|---|---|---|---|
| Full ON | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S1(Power On Suspend) | LOW | HIGH | HIGH | HIGH | ON | ON | ON | LOW |
| S3 (Suspend to RAM) | LOW | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | LOW | LOW | LOW | HIGH | ON | OFF | OFF | OFF |
| S5 (Soft OFF) | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF |

## BOM Structure Table

| BTO Item | BOM Structure |
|---|---|
| Unpop | @<br>@CONN@ / @DIS@<br>@EMI@ / @ESD@ |
| CPU OPTION | CPU1@ ~ CPU4@ |
| AMD Venus XTX | DIS@ |
| VRAM Option | V2G@ / V4G@<br>HYN2@ / HYN4@<br>SAM2@ / SAM4@<br>MIC2@ / MIC4@ |
| Platform | BDW@ / HSW@ |
| DS3 | DS3@ |
| NODS3 | NODS3@ |
| LAN RTL8111GUS | SWR@ / LDO@ |
| EMI PART | EMI@ |
| ESD PART | ESD@ |
| Crystal | NOGCLK@ |
| Green CLK | GCLK@ |
| SATA Repeater | TI@ / Parade@ |
| EC | 9022@ / 9012@ |
| Connector | CONN@ |

## PCB part

ZZZ @ DA8000ZQ010 PCB 14P LA-B131P REV1 M/B 4

ZZZ DAZ14P00100 PCB ZIVY1 LA-B131P LS-B131P/B132/B133 02

SVT

## CPU part (R1)

| | |
|---|---|
| HSW | U9 CPU3@ R3 I5-4200U 1.6G SA00006SMC0; U9 CPU1@ R1 I5-4210U 1.7GHZ SA00007LC10; U9 CPU2@ R3 I7-4500U 1.8G SA00006SLA0; U9 CPU4@ R1 I7-4510U 2GHZ SA00007M700 |
| BDW | |

SVT

## VRAM * 8 (R1)

ZZZ V2G@ H5TC2G63FFR-11C

**2G X7654038L01**

ZZZ V4G@ H5TC4G63AFR-11C

**4G X7654038L04**

U21 HYN2@ H5TC2G63FFR-11C; U16 HYN2@ H5TC2G63FFR-11C; U15 HYN2@ H5TC2G63FFR-11C; U20 HYN2@ H5TC2G63FFR-11C; RV6 HYN2@ 10K_0402_5%; RV8 HYN2@ 10K_0402_5%; U19 HYN2@ H5TC2G63FFR-11C; U17 HYN2@ H5TC2G63FFR-11C; U14 HYN2@ H5TC2G63FFR-11C; U18 HYN2@ H5TC2G63FFR-11C; RV10 HYN2@ 10K_0402_5%

SA00006H410

**Hynix_X7654038L01**

U14 HYN4@ H5TC4G63AFR-11C; U16 HYN4@ H5TC4G63AFR-11C; U18 HYN4@ H5TC4G63AFR-11C; U20 HYN4@ H5TC4G63AFR-11C; RV6 HYN4@ 10K_0402_5%; RV7 HYN4@ 10K_0402_5%; U15 HYN4@ H5TC4G63AFR-11C; U17 HYN4@ H5TC4G63AFR-11C; U19 HYN4@ H5TC4G63AFR-11C; U21 HYN4@ H5TC4G63AFR-11C; RV9 HYN4@ 10K_0402_5%

SA00006E830

**Hynix_X7654038L04**

U21 MIC2@ MT41J128M16JT-093G:K; U18 MIC2@ MT41J128M16JT-093G:K; U14 MIC2@ MT41J128M16JT-093G:K; U19 MIC2@ MT41J128M16JT-093G:K; RV6 MIC2@ 10K_0402_5%; RV8 MIC2@ 10K_0402_5%; U20 MIC2@ MT41J128M16JT-093G:K; U16 MIC2@ MT41J128M16JT-093G:K; U15 MIC2@ MT41J128M16JT-093G:K; U17 MIC2@ MT41J128M16JT-093G:K; RV9 MIC2@ 10K_0402_5%

SA000067510

**Micron_X7654038L02**

U20 MIC4@ MT41J256M16HA-093G; U14 MIC4@ MT41J256M16HA-093G; U17 MIC4@ MT41J256M16HA-093G; U18 MIC4@ MT41J256M16HA-093G; RV5 MIC4@ 10K_0402_5%; RV8 MIC4@ 10K_0402_5%; U21 MIC4@ MT41J256M16HA-093G; U15 MIC4@ MT41J256M16HA-093G; U16 MIC4@ MT41J256M16HA-093G; U19 MIC4@ MT41J256M16HA-093G; RV10 MIC4@ 10K_0402_5%

SA000077K10

**Micron_X7654038L05**

U15 SAM2@ K4W2G1646Q-BC1A; U21 SAM2@ K4W2G1646Q-BC1A; U17 SAM2@ K4W2G1646Q-BC1A; U14 SAM2@ K4W2G1646Q-BC1A; RV6 SAM2@ 10K_0402_5%; RV7 SAM2@ 10K_0402_5%; U20 SAM2@ K4W2G1646Q-BC1A; U19 SAM2@ K4W2G1646Q-BC1A; U16 SAM2@ K4W2G1646Q-BC1A; U18 SAM2@ K4W2G1646Q-BC1A; RV10 SAM2@ 10K_0402_5%

SA000068U50

**Samsung_X7654038L03**

U21 SAM4@ K4W4G1646D-BC1A; U14 SAM4@ K4W4G1646D-BC1A; U16 SAM4@ K4W4G1646D-BC1A; U19 SAM4@ K4W4G1646D-BC1A; RV5 SAM4@ 10K_0402_5%; RV8 SAM4@ 10K_0402_5%; U20 SAM4@ K4W4G1646D-BC1A; U17 SAM4@ K4W4G1646D-BC1A; U15 SAM4@ K4W4G1646D-BC1A; U18 SAM4@ K4W4G1646D-BC1A; RV9 SAM4@ 10K_0402_5%

SA000076P10

**Samsung_X7654038L06**

## EC SM Bus1 address

| Device | Address |
|---|---|
| Smart Battery | 0001 0010 |

## EC SM Bus2 address

| Device | Address |
|---|---|
| Thermal Sensor | 1001 101xb |

## PCH SM Bus address

| Device | Address | |
|---|---|---|
| DDR_JDIMM1 | 1010 000x | A0h |
| DDR_JDIMM2 | 1010 010x | A4h |
| TP module | | |

### SMBUS Control Table

| | SOURCE | BATT | VGA | SODIMM | EC-KB9022 | TP | Smart Charge | Thermal Sensor |
|---|---|---|---|---|---|---|---|---|
| SMB_EC_CK1<br>SMB_EC_DA1 | EC | V | X | X | X | X | V | X |
| SMBCLK<br>SMBDATA | PCH | X | X | V | X | V | X | X |
| SML0CLK<br>SML0DATA | PCH | X | X | X | X | X | X | X |
| SML1CLK<br>SML1DATA | PCH | X | V | X | V | X | X | V |

### USB2.0

| Port | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| | Left USB3.0 | Left USB3.0 | Right USB2.0 | | Touch Panel | Camera | BT (NGFF) | |

### Flexible I/O Capable Ports

| HSIO Port | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| USB 3.0 | 1<br>USB3.0_1 | 2<br>USB3.0_2 | | | | | | | | | | | | |
| PCIe | | | 1 | 2<br>CardReader | 3<br>LAN | 4<br>WLAN | 5-L0<br>GPU_Venus | 5-L1<br>GPU_Venus | 5-L2<br>GPU_Venus | 5-L3<br>GPU_Venus | 6-L0 | 6-L1 | 6-L2 | 6-L3 |
| SATA | | | | | | | | | | | 3 | 2 | 1 | 0<br>HDD(SSD) |

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| Issued Date | 2014/03/03 | Deciphered Date 2015/03/03 | Title: Notes List |

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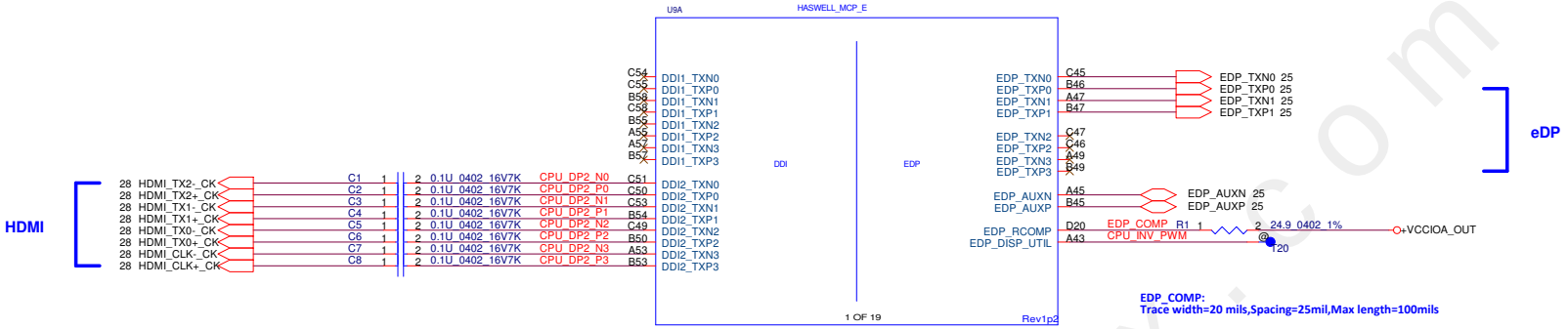
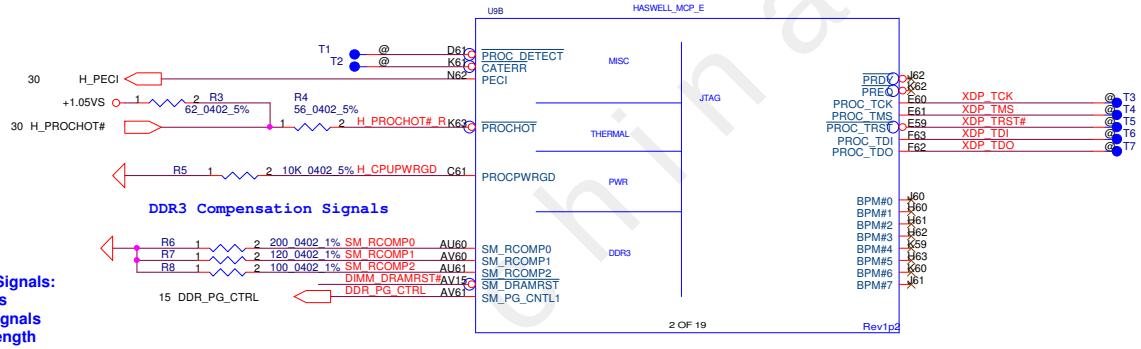
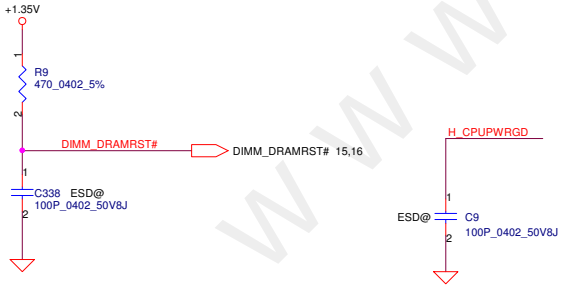



**EDP_COMP:**
**Trace width=20 mils,Spacing=25mil,Max length=100mils**




**DDR3 Compensation Signals**

**DDR3 Compensation Signals:**
**20mils to comp signals**
**25mils to non-comp signals**
**500mil for Max trace length**

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Title: *BDW ULT(1/11) DDI,MSIC,XDP*

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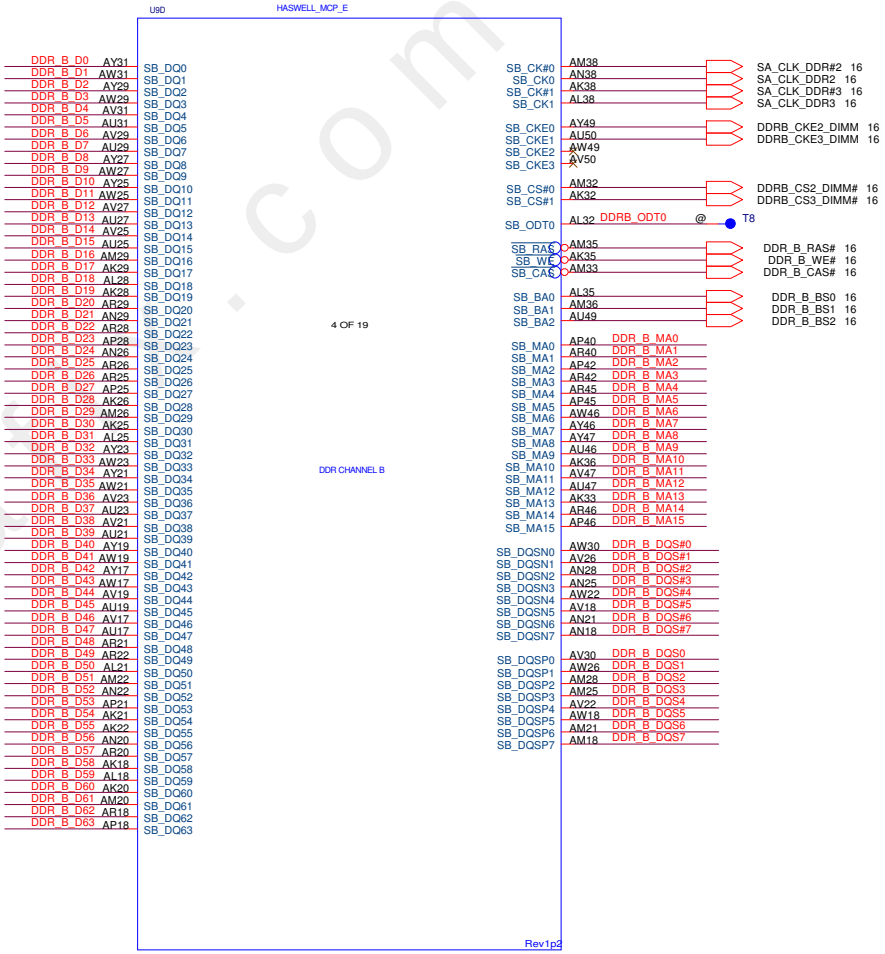


15 DDR_A_D[0..63]
15 DDR_A_MA[0..15]
15 DDR_A_DQS#[0..7]
15 DDR_A_DQS[0..7]

16 DDR_B_D[0..63]
16 DDR_B_MA[0..15]
16 DDR_B_DQS#[0..7]
16 DDR_B_DQS[0..7]

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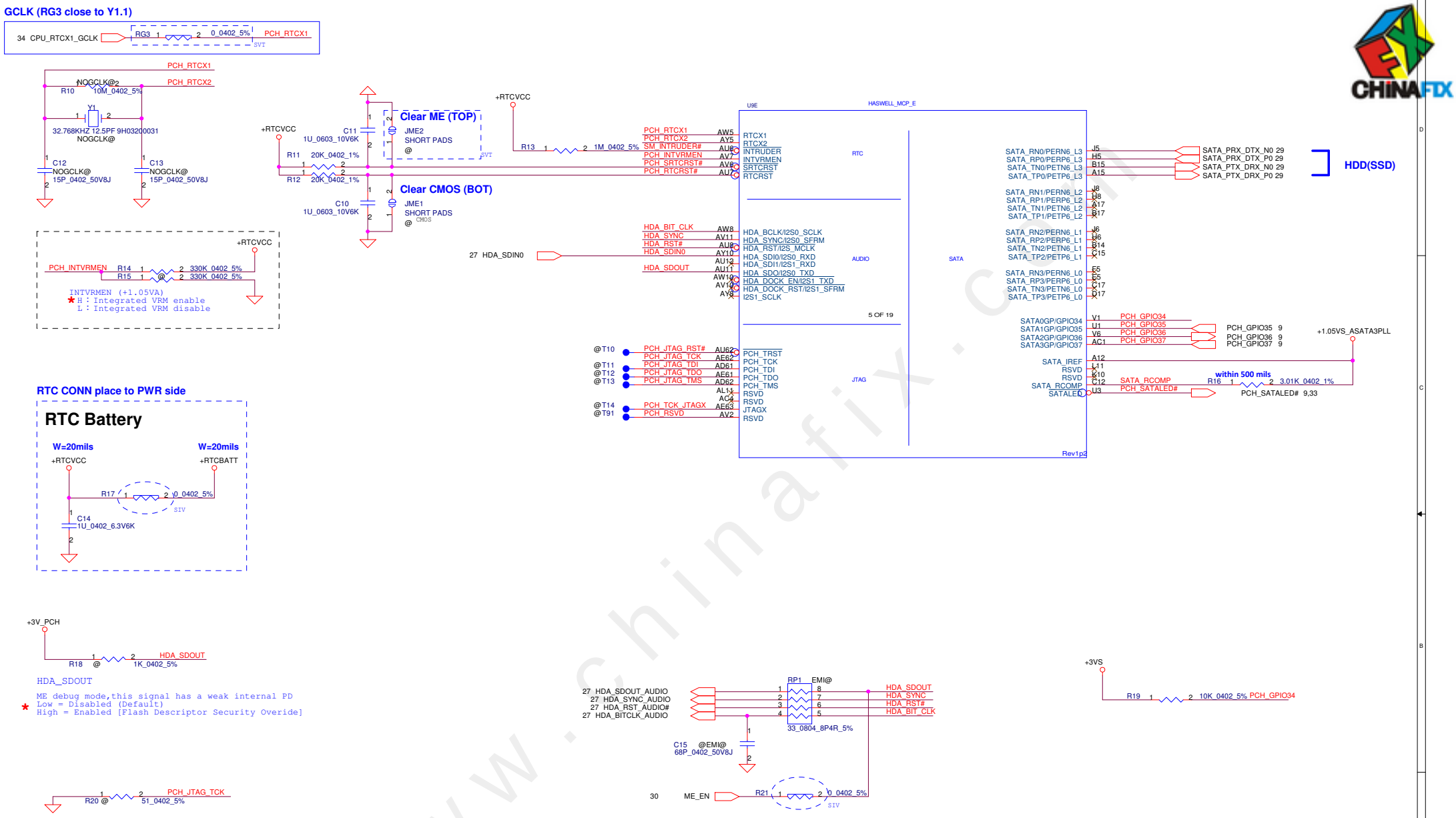


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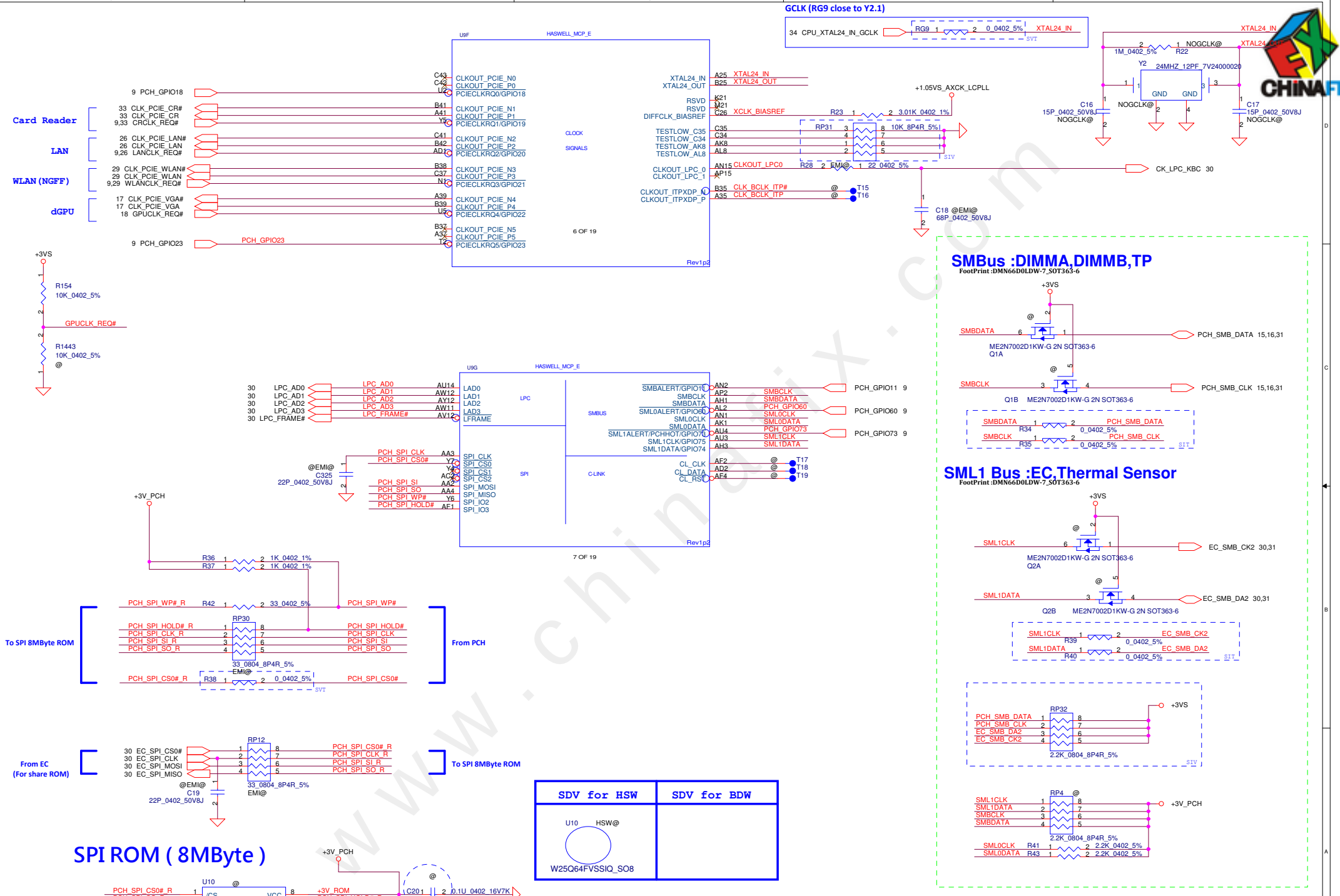


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Compal Electronics, Inc.

Title: BDW ULT(4/11)CLK,SPI,SMBUS

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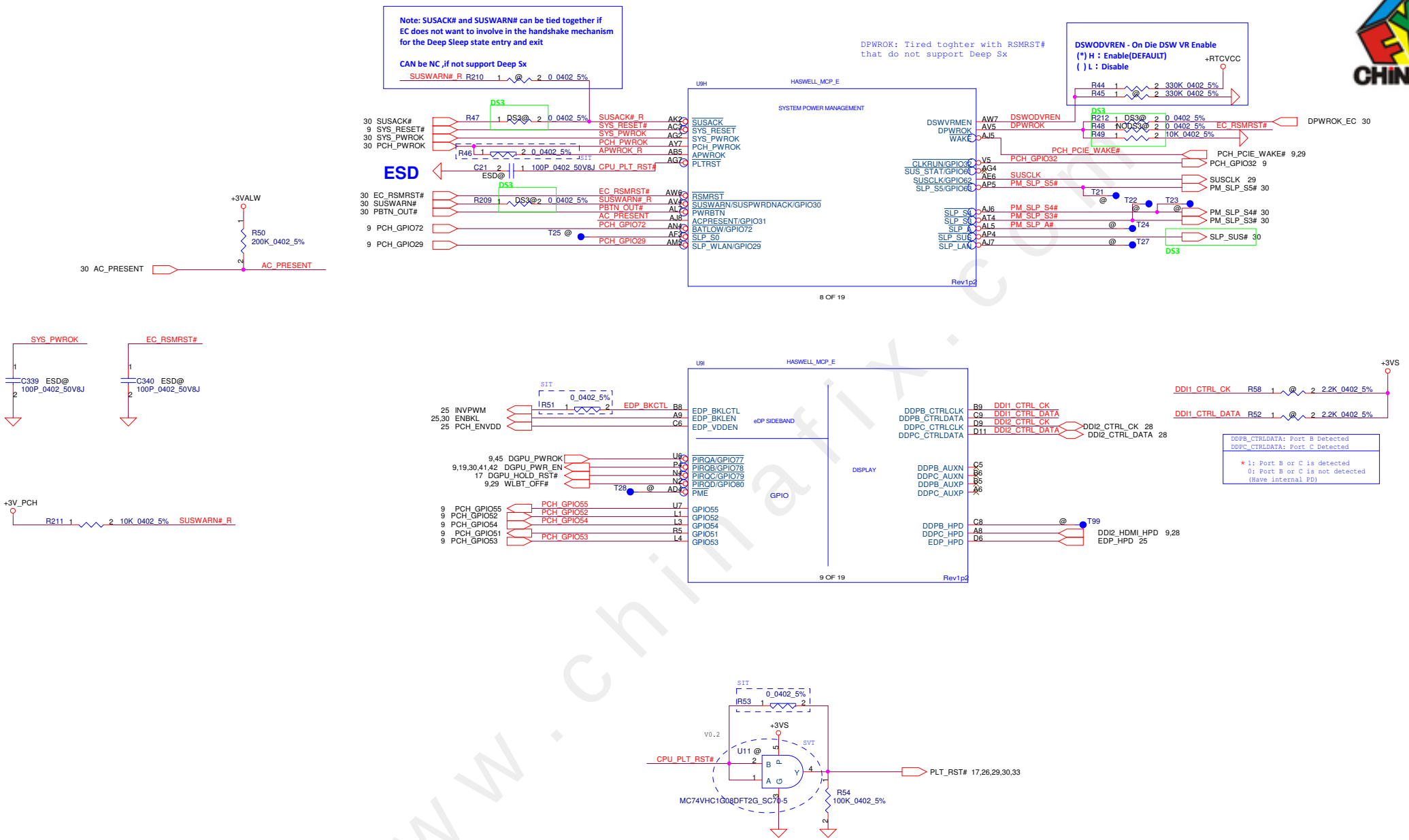


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Title: **BDW ULT(5/11) PM,GPIO,DDI**

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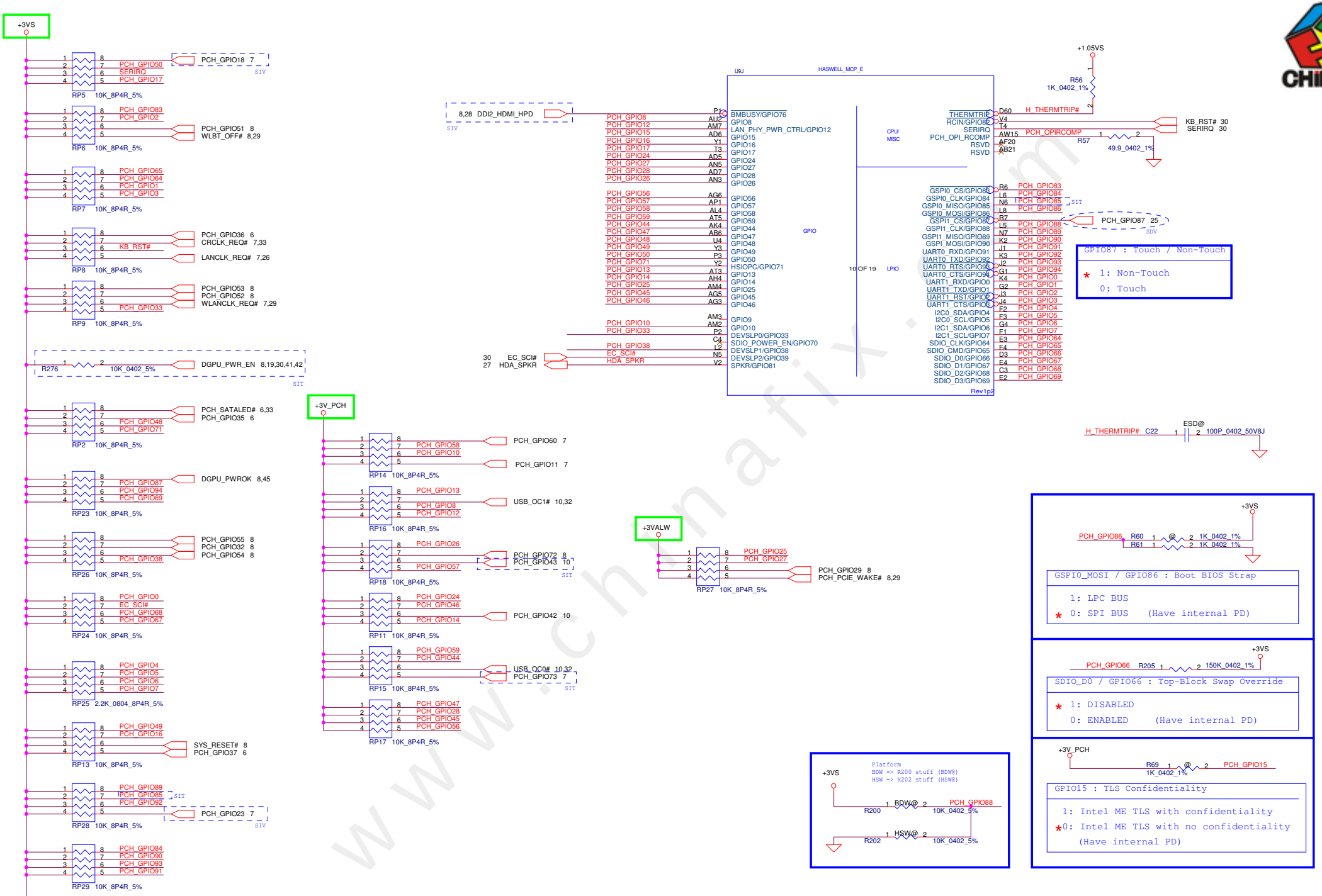


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Title: **BDW ULT(6/11) GPIO,LPIO**

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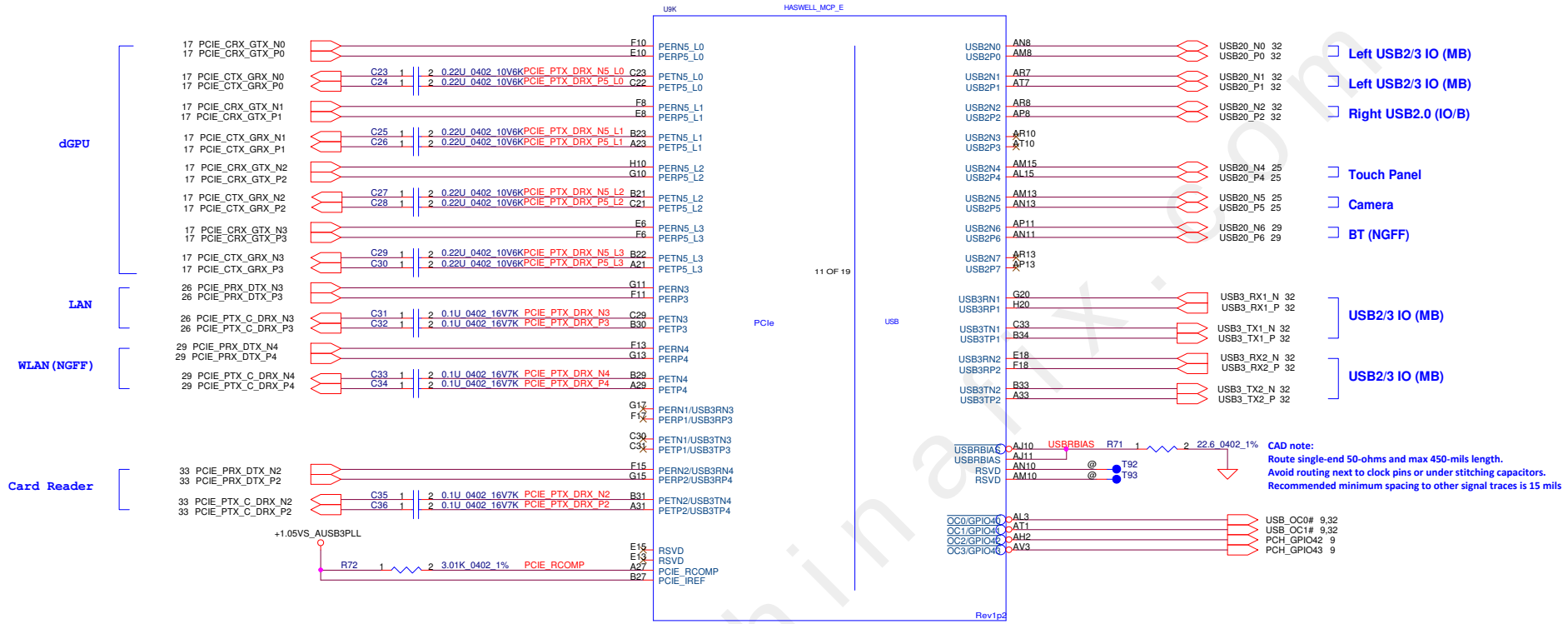


## USB2.0

| Port | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| | Left USB3.0 | Left USB3.0 | Right USB2.0 | | Touch Panel | Camera | BT (NGFF) | |

## Flexible I/O Capable Ports

| HSIO Port | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| USB 3.0 | 1<br>USB3.0_1 | 2<br>USB3.0_2 | | | | | | | | | | | | |
| PCIe | | | 1 | 2<br>CardReader | 3<br>LAN | 4<br>WLAN | 5-L0<br>GPU_Venus | 5-L1<br>GPU_Venus | 5-L2<br>GPU_Venus | 5-L3<br>GPU_Venus | 6-L0 | 6-L1 | 6-L2 | 6-L3 |
| SATA | | | | | | | | | | | 3 | 2 | 1 | 0<br>HDD(SSD) |

| | | | |
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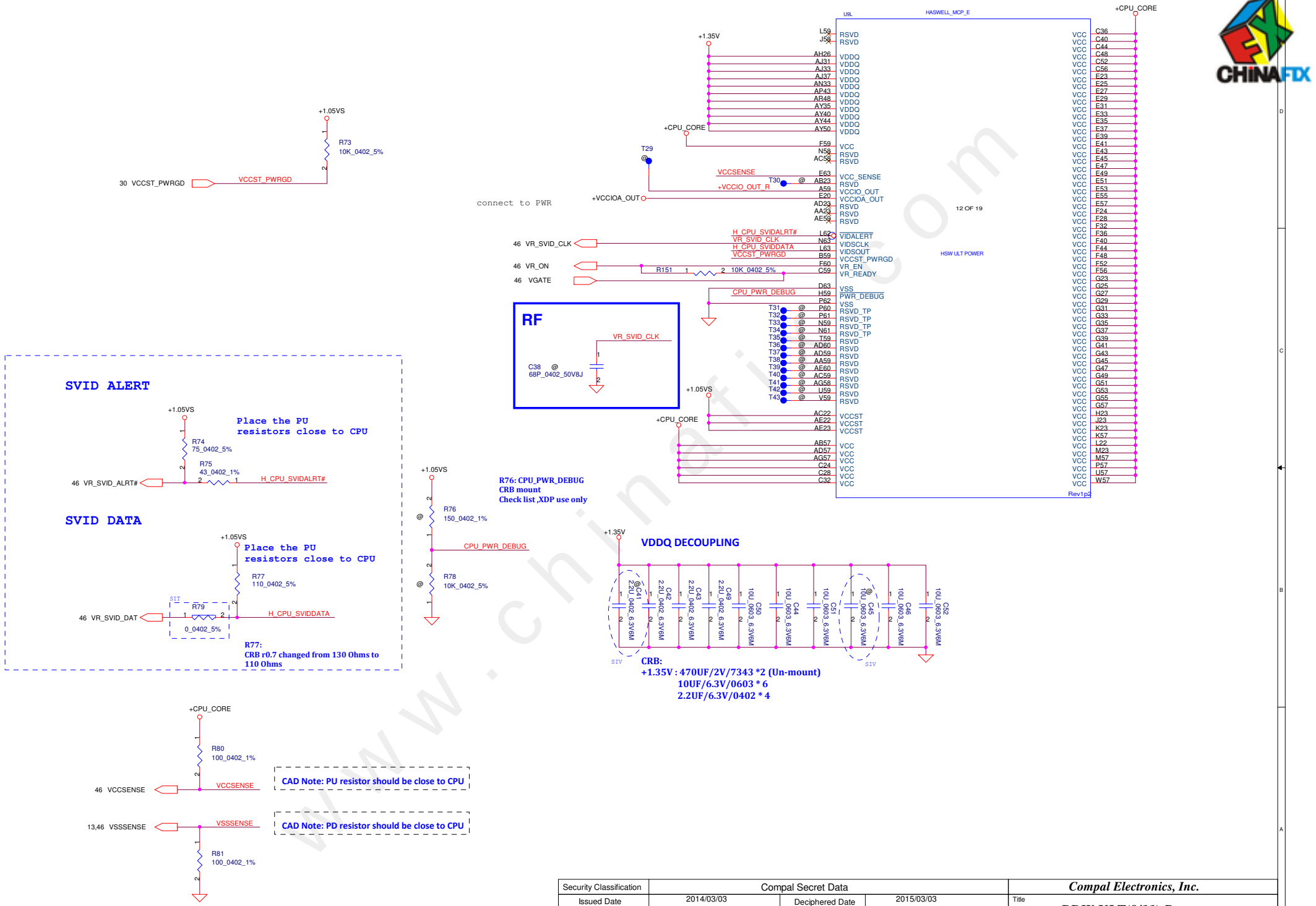


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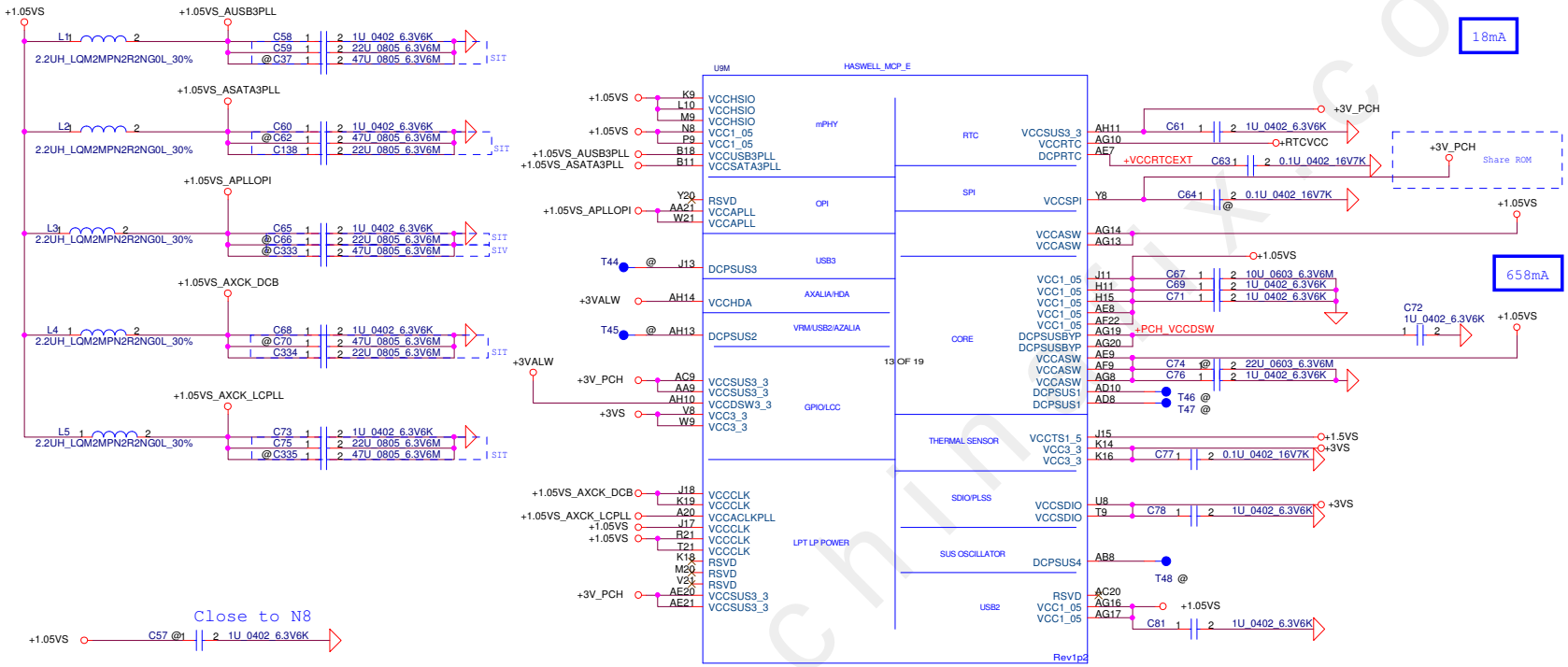
Check Power Source




Close to N8

+1.05VS — C57 @1 — 1U_0402_6.3V6K

Close to K9,M9

+1.05VS — C80, C82 — 1U_0402_6.3V6K

Close to AC9/AA9/AE20/AE21

+3V_PCH — C84 — 22U_0603_6.3V6M

Close to V8

+3VS — C85 — 22U_0603_6.3V6M

Close to J17

+1.05VS — C86 — 1U_0402_6.3V6K

Close to R21

+1.05VS — C87 — 1U_0402_6.3V6K

Close to AH14

+3VALW — C88 — 1U_0402_6.3V6K

V1.0

+3V_PCH — C83 — 0.47U_0402_16V4Z — +PCH_VCCDSW

| | | | |
|---|---|---|---|
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| Issued Date | 2014/03/03 | Deciphered Date 2015/03/03 | Title: BDW ULT(9/11) Power |
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| | | | Date: Tuesday, March 04, 2014; Sheet 12 of 52 |

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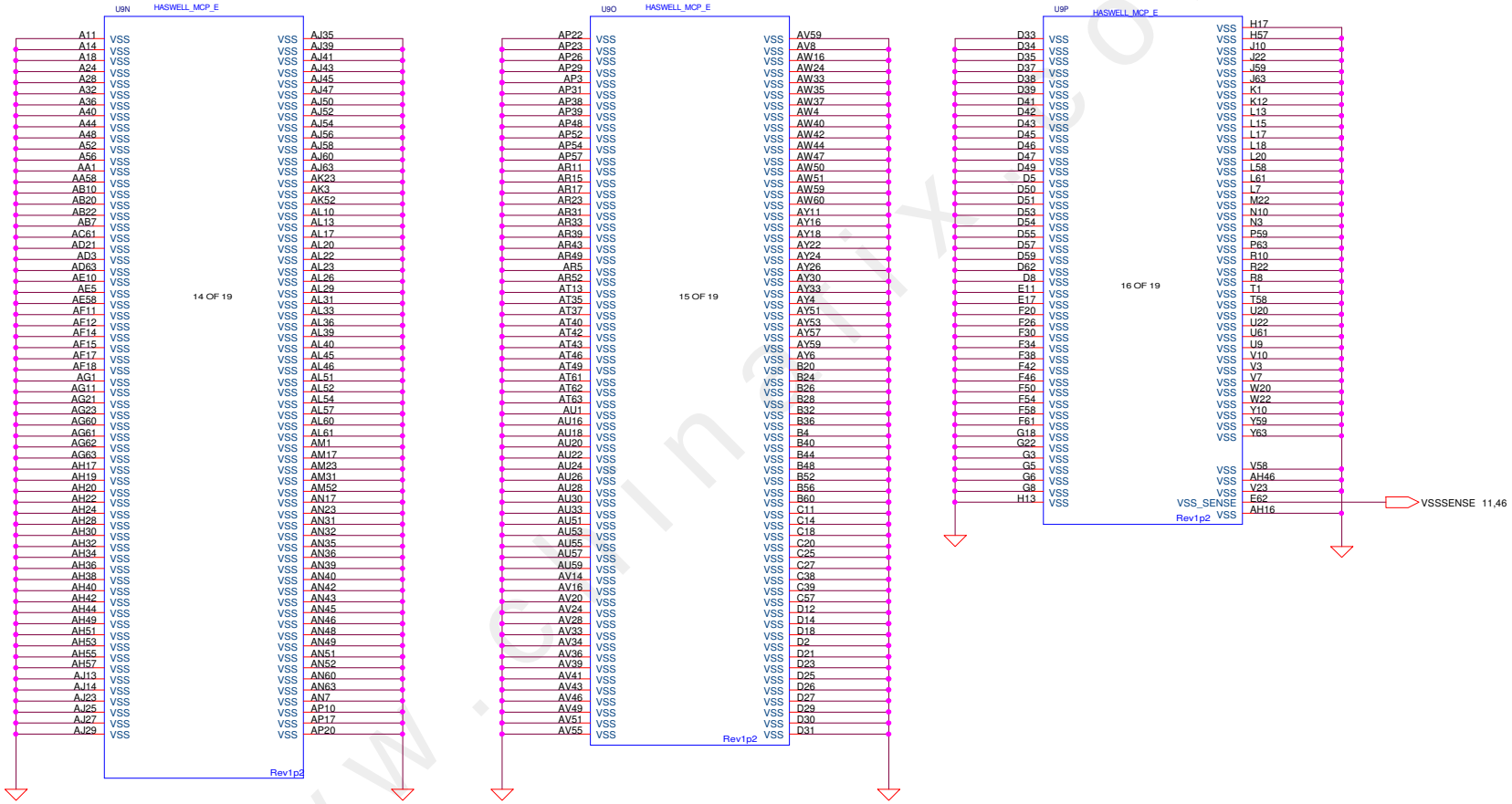


| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2014/03/03 | Deciphered Date 2015/03/03 | Title BDW ULT(10/11) GND |
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| | | | Date: Tuesday, March 04, 2014 / Sheet 13 of 52 |

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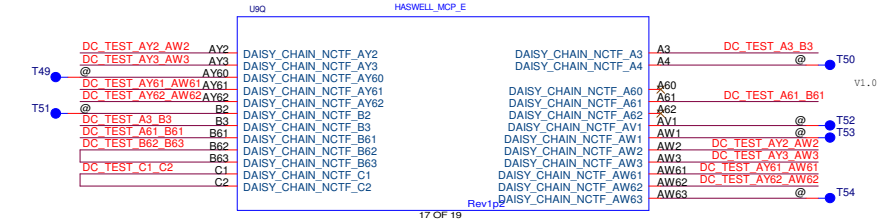
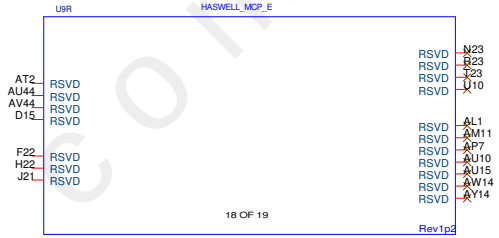
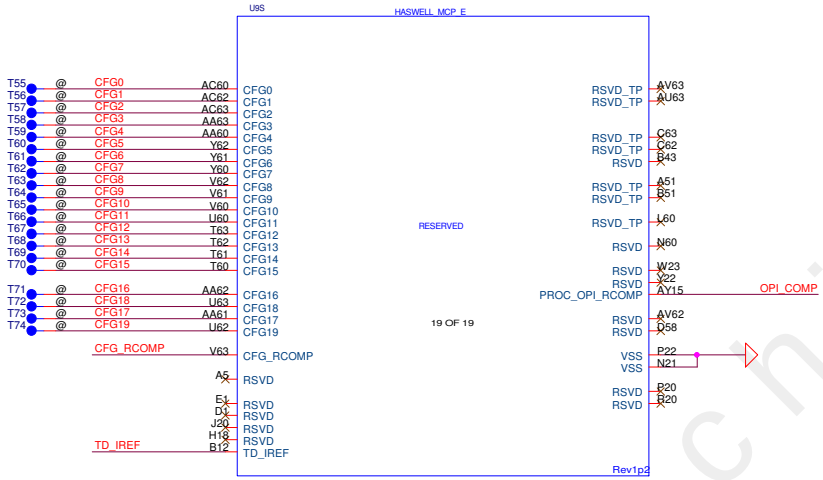
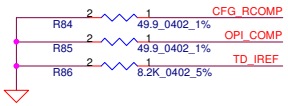
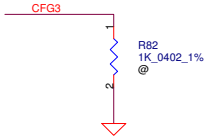


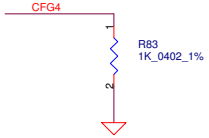




## CFG Straps for Processor




| Physical Debug Enable (DFX Privacy) | |
|---|---|
| CFG3 | 1: DISABLED<br>0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR |




| Display Port Presence Strap | |
|---|---|
| CFG4 | 1 : Disabled; No Physical Display Port attached to Embedded Display Port<br>0 : Enabled; An external Display Port device is connected to the Embedded Display Port |

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|---|---|---|
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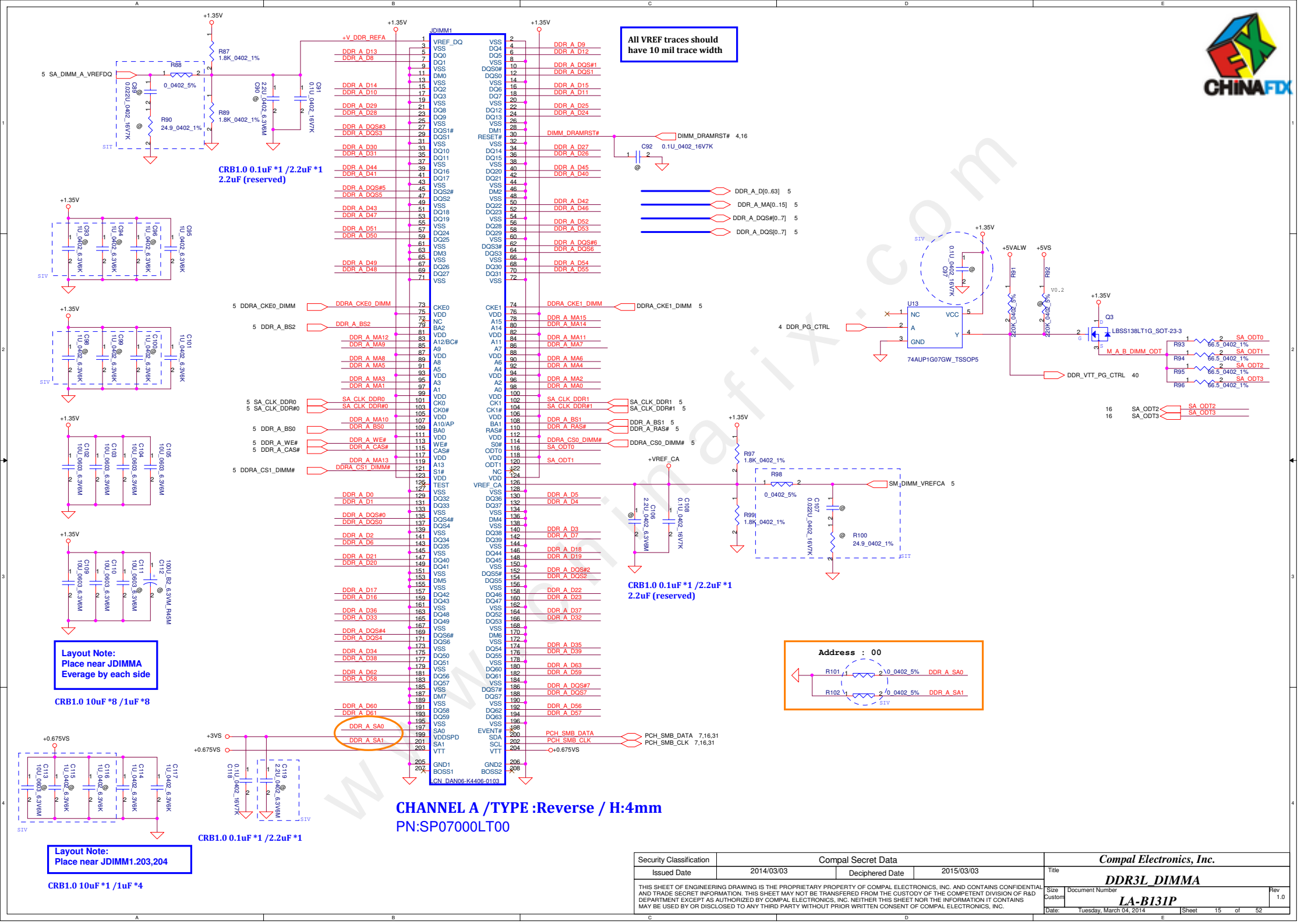


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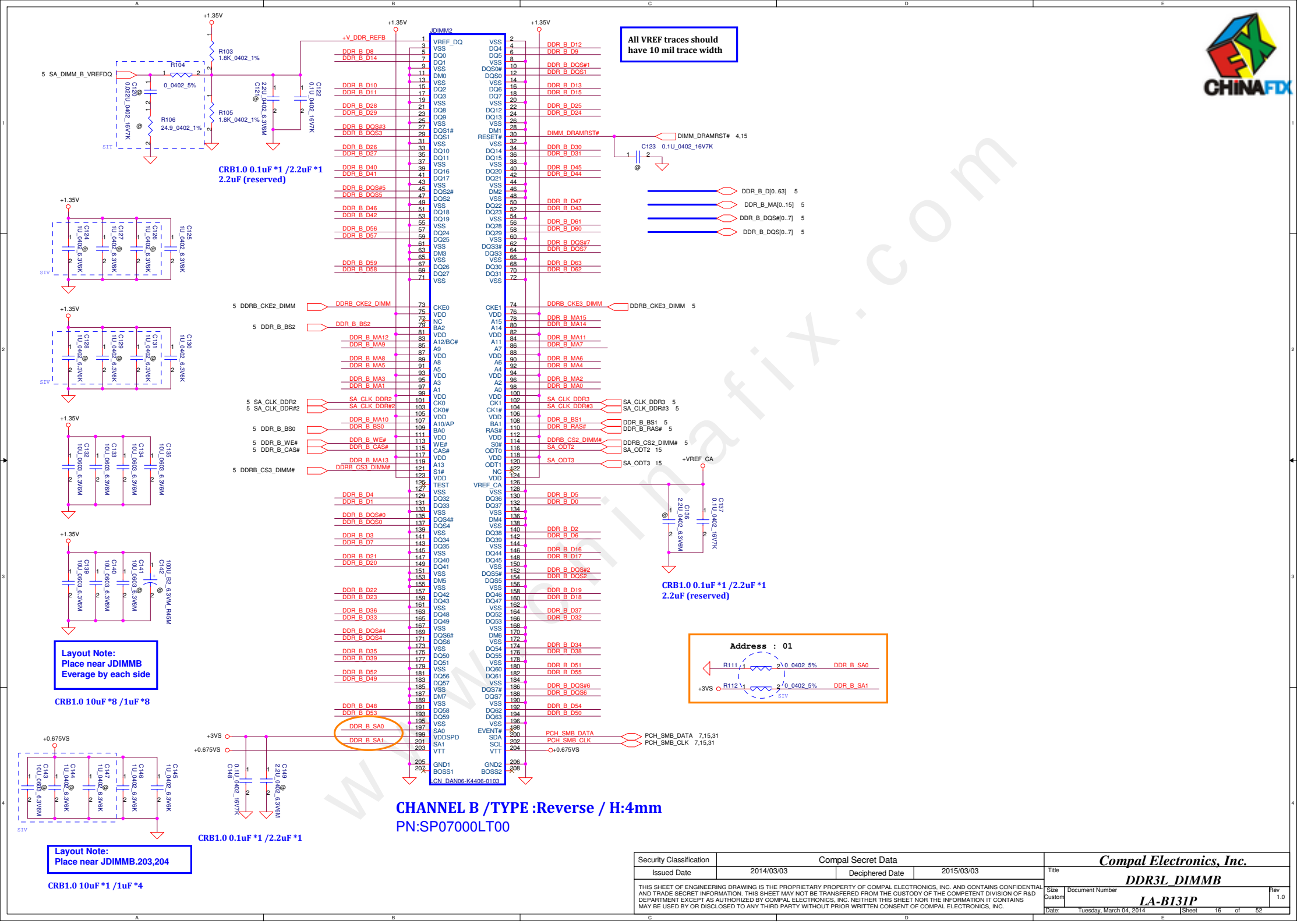
Compal Electronics, Inc.

Title: DDR3L_DIMMA

Size: Custom | Document Number: LA-B131P | Rev: 1.0

Date: Tuesday, March 04, 2014 | Sheet 15 of 52

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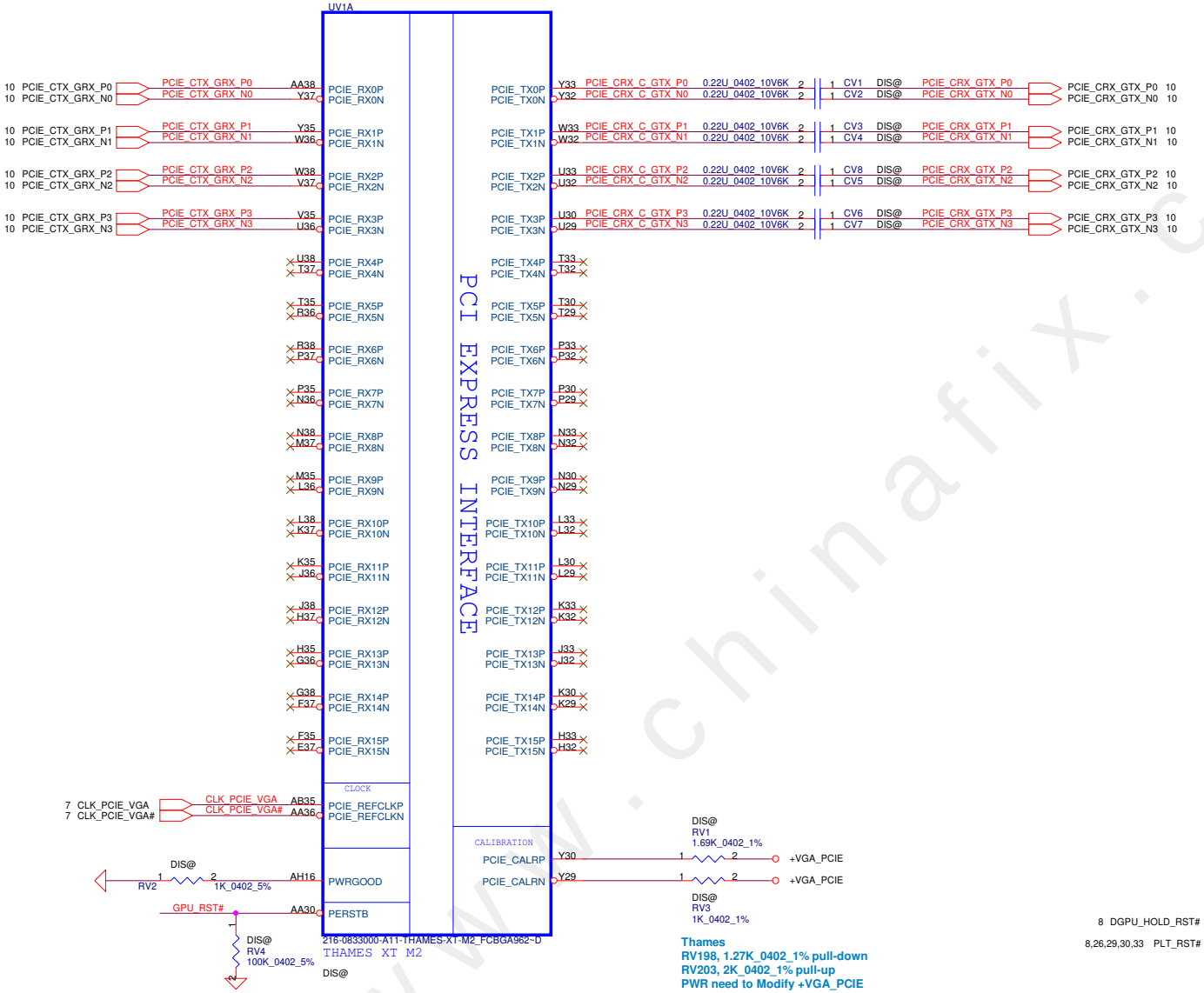
Compal Electronics, Inc.

Title: DDR3L_DIMMB

Size: Custom | Document Number: LA-B131P | Rev: 1.0

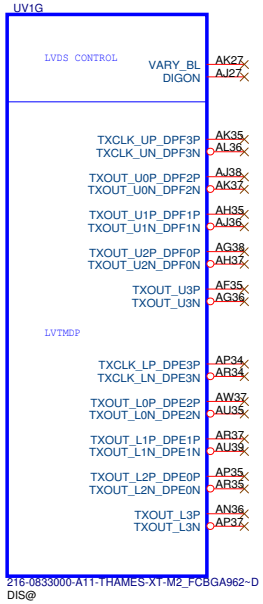
Date: Tuesday, March 04, 2014 | Sheet 16 of 52

# GFX PCIE LANE REVERSAL

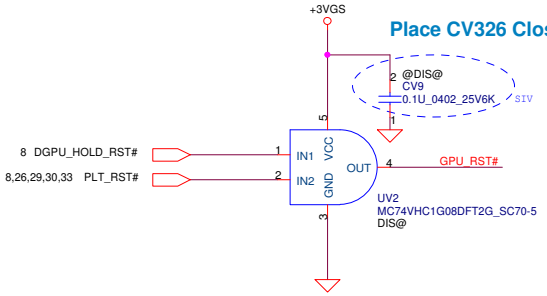



**Thames**
**RV198, 1.27K_0402_1% pull-down**
**RV203, 2K_0402_1% pull-up**
**PWR need to Modify +VGA_PCIE**

## LVDS Interface




**Place CV326 Close to UV13**

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**Compal Electronics, Inc.**

Title: **Venus XTX(1/8) PCIE/PWRseq**

Size: Custom | Document Number: **LA-B131P** | Rev: 1.0

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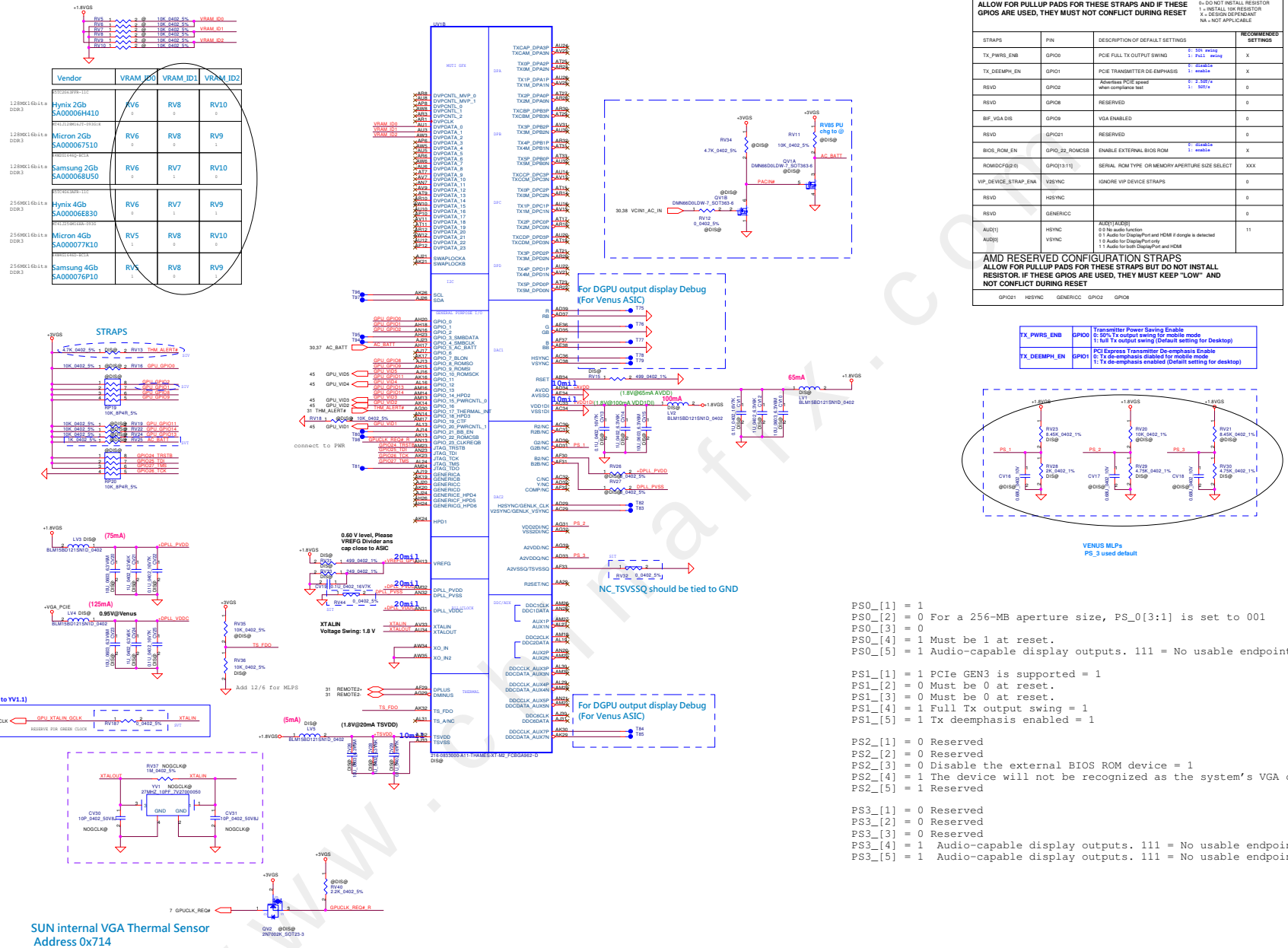


## CONFIGURATION STRAPS

**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET**

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

| STRAPS | PIN | DESCRIPTION OF DEFAULT SETTINGS | RECOMMENDED SETTINGS |
|---|---|---|---|
| TX_PWRS_ENB | GPIO0 | PCIE FULL TX OUTPUT SWING 0: 50% swing 1: Full swing | X |
| TX_DEEMPH_EN | GPIO1 | PCIE TRANSMITTER DE-EMPHASIS 0: disable 1: enable | X |
| RSVD | GPIO2 | Advertises PCIE speed when compliance test 0: 2.5GT/s 1: 5GT/s | 0 |
| RSVD | GPIO8 | RESERVED | 0 |
| BIF_VGA DIS | GPIO9 | VGA ENABLED | 0 |
| RSVD | GPIO21 | RESERVED | 0 |
| BIOS_ROM_EN | GPIO_22_ROMCSB | ENABLE EXTERNAL BIOS ROM 0: disable 1: enable | X |
| ROMIDCFG[2:0] | GPIO[13:11] | SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT | XXX |
| VIP_DEVICE_STRAP_ENA | V2SYNC | IGNORE VIP DEVICE STRAPS | 0 |
| RSVD | H2SYNC | | 0 |
| RSVD | GENERICC | | 0 |
| AUD[1] AUD[0] | HSYNC VSYNC | AUD[1:]AUD[0]: 0 0 No audio function; 0 1 Audio for DisplayPort and HDMI if dongle is detected; 1 0 Audio for DisplayPort only; 1 1 Audio for both DisplayPort and HDMI | 11 |

## AMD RESERVED CONFIGURATION STRAPS

**ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET**

GPIO21 H2SYNC GENERICC GPIO2 GPIO8

| | | |
|---|---|---|
| TX_PWRS_ENB | GPIO0 | Transmitter Power Saving Enable<br>0: 50% Tx output swing for mobile mode<br>1: full Tx output swing (Default setting for Desktop) |
| TX_DEEMPH_EN | GPIO1 | PCI Express Transmitter De-emphasis Enable<br>0: Tx de-emphasis diabled for mobile mode<br>1: Tx de-emphasis enabled (Defailt setting for desktop) |

PS0_[1] = 1
PS0_[2] = 0 For a 256-MB aperture size, PS_0[3:1] is set to 001
PS0_[3] = 0
PS0_[4] = 1 Must be 1 at reset.
PS0_[5] = 1 Audio-capable display outputs. 111 = No usable endpoints.

PS1_[1] = 1 PCIe GEN3 is supported = 1
PS1_[2] = 0 Must be 0 at reset.
PS1_[3] = 0 Must be 0 at reset.
PS1_[4] = 1 Full Tx output swing = 1
PS1_[5] = 1 Tx deemphasis enabled = 1

PS2_[1] = 0 Reserved
PS2_[2] = 0 Reserved
PS2_[3] = 0 Disable the external BIOS ROM device = 1
PS2_[4] = 1 The device will not be recognized as the system's VGA controller = 1
PS2_[5] = 1 Reserved

PS3_[1] = 0 Reserved
PS3_[2] = 0 Reserved
PS3_[3] = 0 Reserved
PS3_[4] = 1 Audio-capable display outputs. 111 = No usable endpoints.
PS3_[5] = 1 Audio-capable display outputs. 111 = No usable endpoints.

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Title: *Compal Electronics, Inc.*
*Venus XTX(2/8) Main Gen*

Size: D | Document Number: *LA-B131P* | Rev: 1.0

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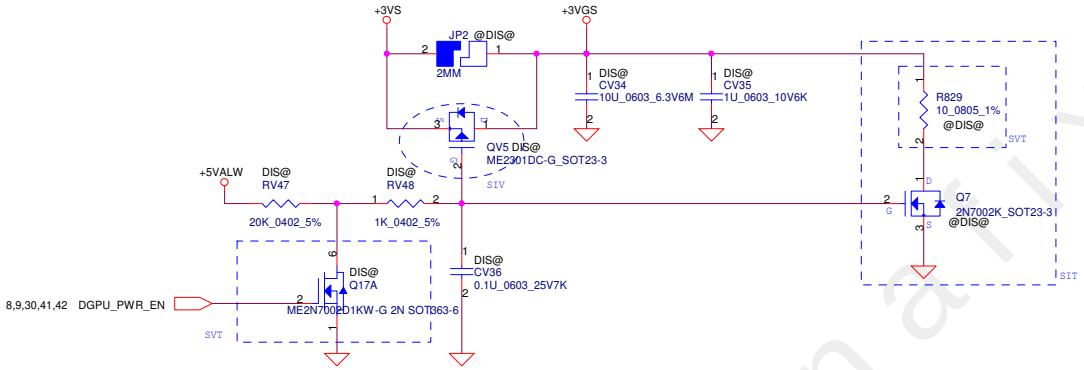
PX_MODE=1 for Normal Operation
PX_MODE=0 for BACO mode to shut down power rails expcept VDDR3,PCIE_VDDC and 1.8V rail

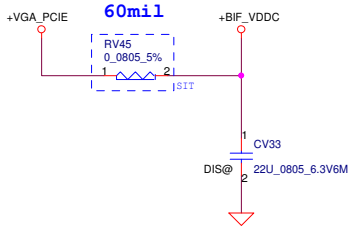
**Note:**

PX4.0 +VGA_CORE,VDDCI,+1.5VGS ON
PX4.0 +3VGS, +1.0VGS,+1.8VGS OFF
PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF

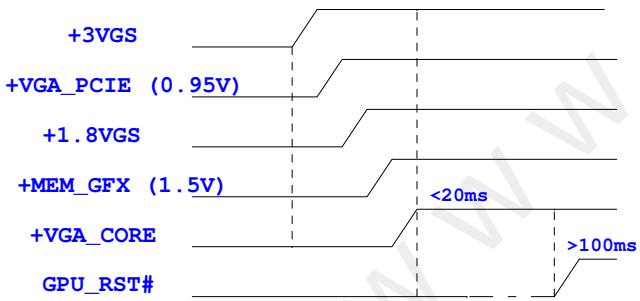
# Switch circuits in BACO desingns for Thames/Seymour only 55mA@1.0V, in BACO mode

## +3VS TO +3VGS

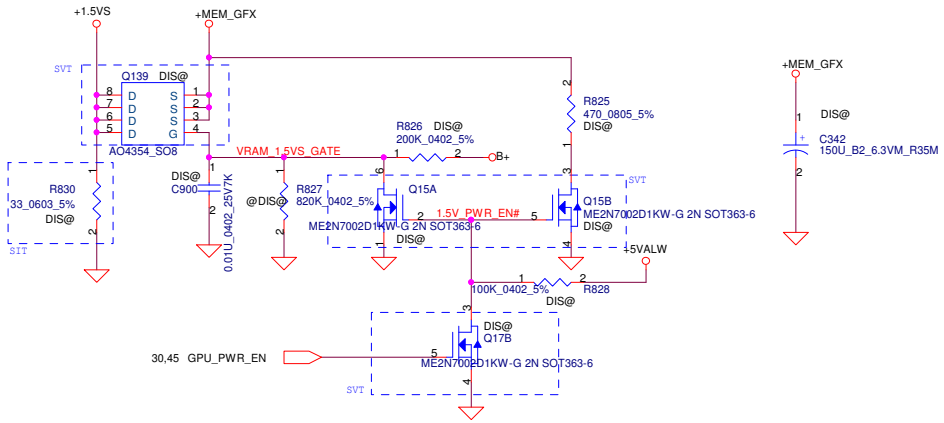



## Power seguence of Venus XTX




## +1.5VS to +MEM_GFX

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Compal Electronics, Inc.

Title: Venus XTX(3/8) DC/DC POWER

Size: Custom | Document Number: LA-B131P | Rev: 1.0

Date: Tuesday, March 04, 2014 | Sheet 19 of 52

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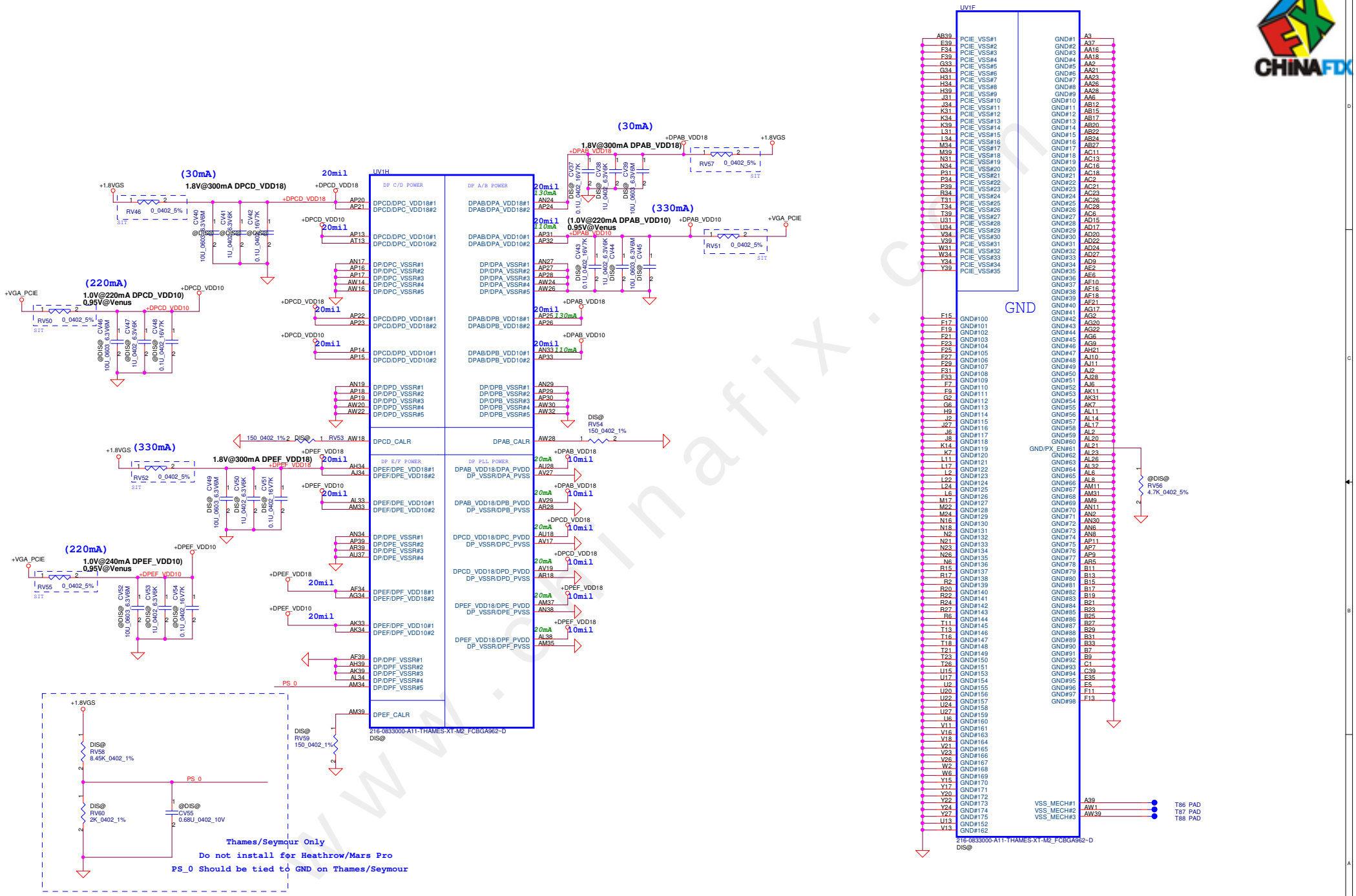


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Compal Electronics, Inc.

Title: Venus XTX(4/8)DPX Power/GND

Size: Custom | Document Number: LA-B131P | Rev: 1.0

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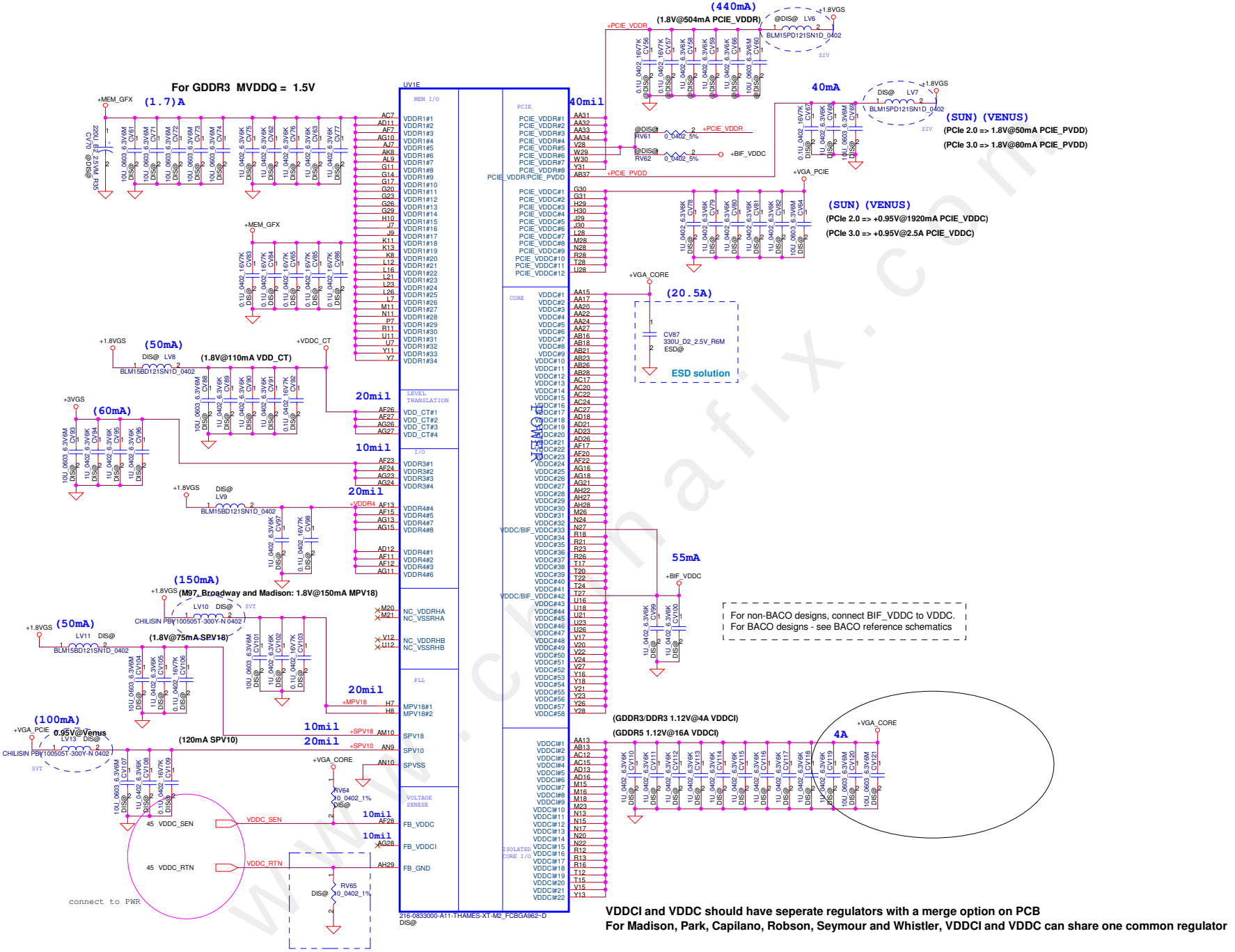


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Compal Electronics, Inc.

Title: Venus XTX(5/8) Power

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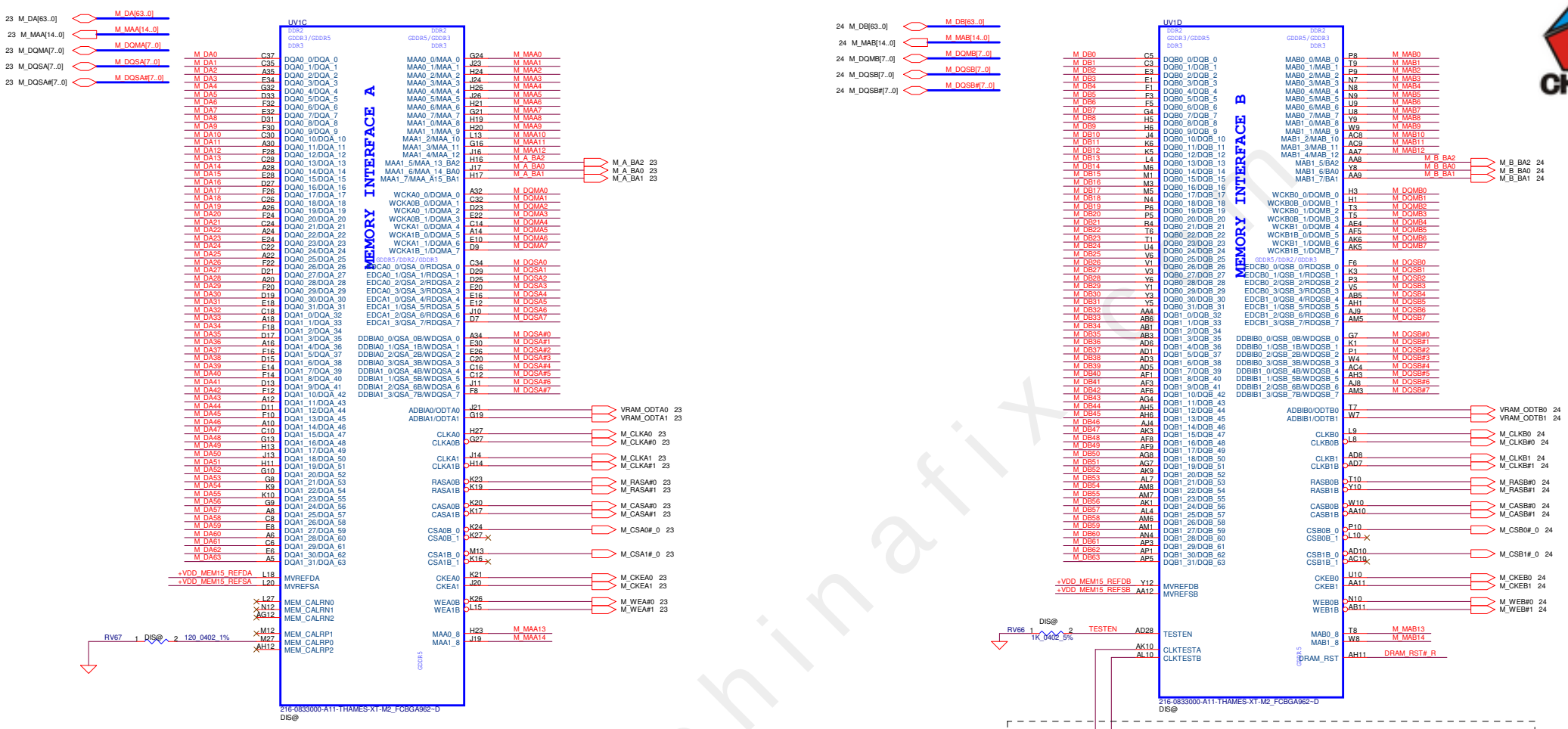
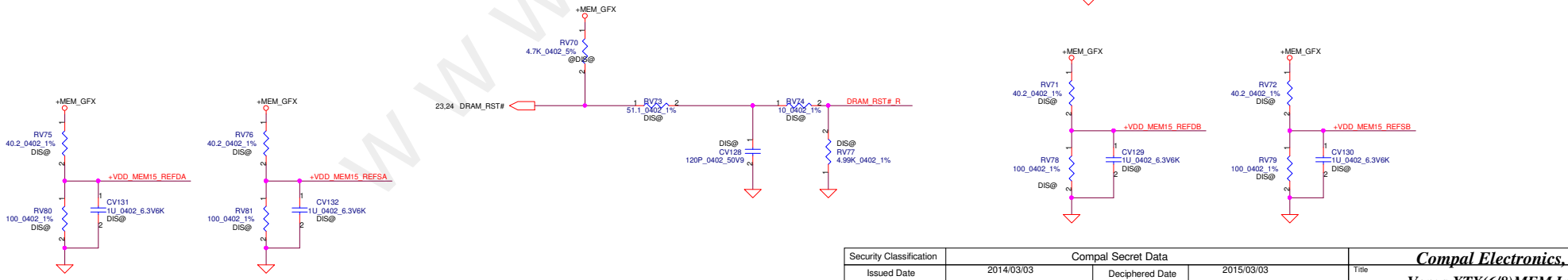



This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

route 50ohms single-ended/100ohms diff
and keep short
Debug only, for clock observation, if not needed, DNI
5mil 5mil

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Compal Electronics, Inc.

Title: Venus XTX(6/8)MEM Interface

Size: Custom | Document Number: LA-B131P | Rev: 1.0

Date: Tuesday, March 04, 2014 | Sheet 22 of 52

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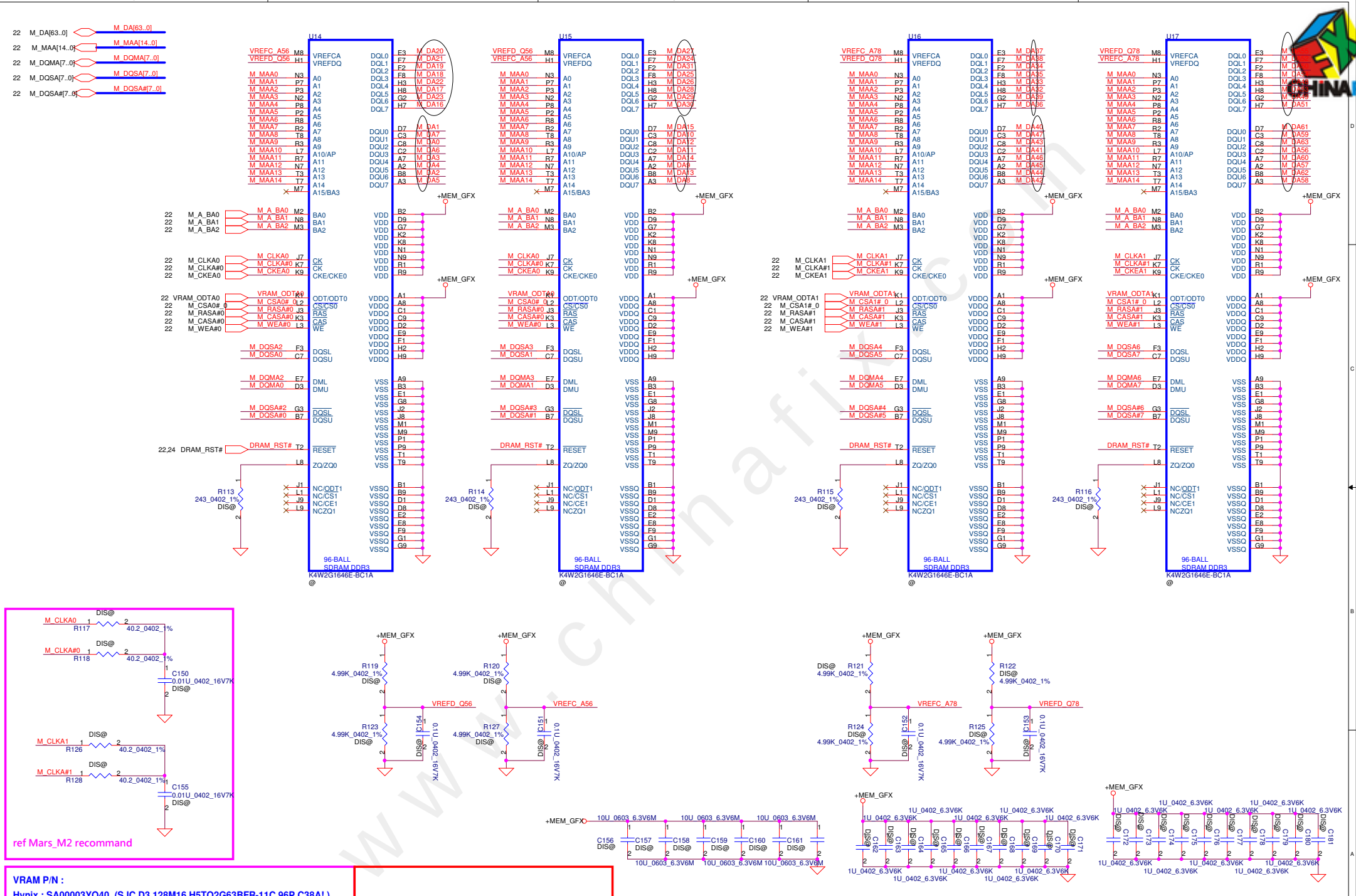


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**Compal Electronics, Inc.**

Title: **Venus XTX(7/8) DDR3 VRAM_A**

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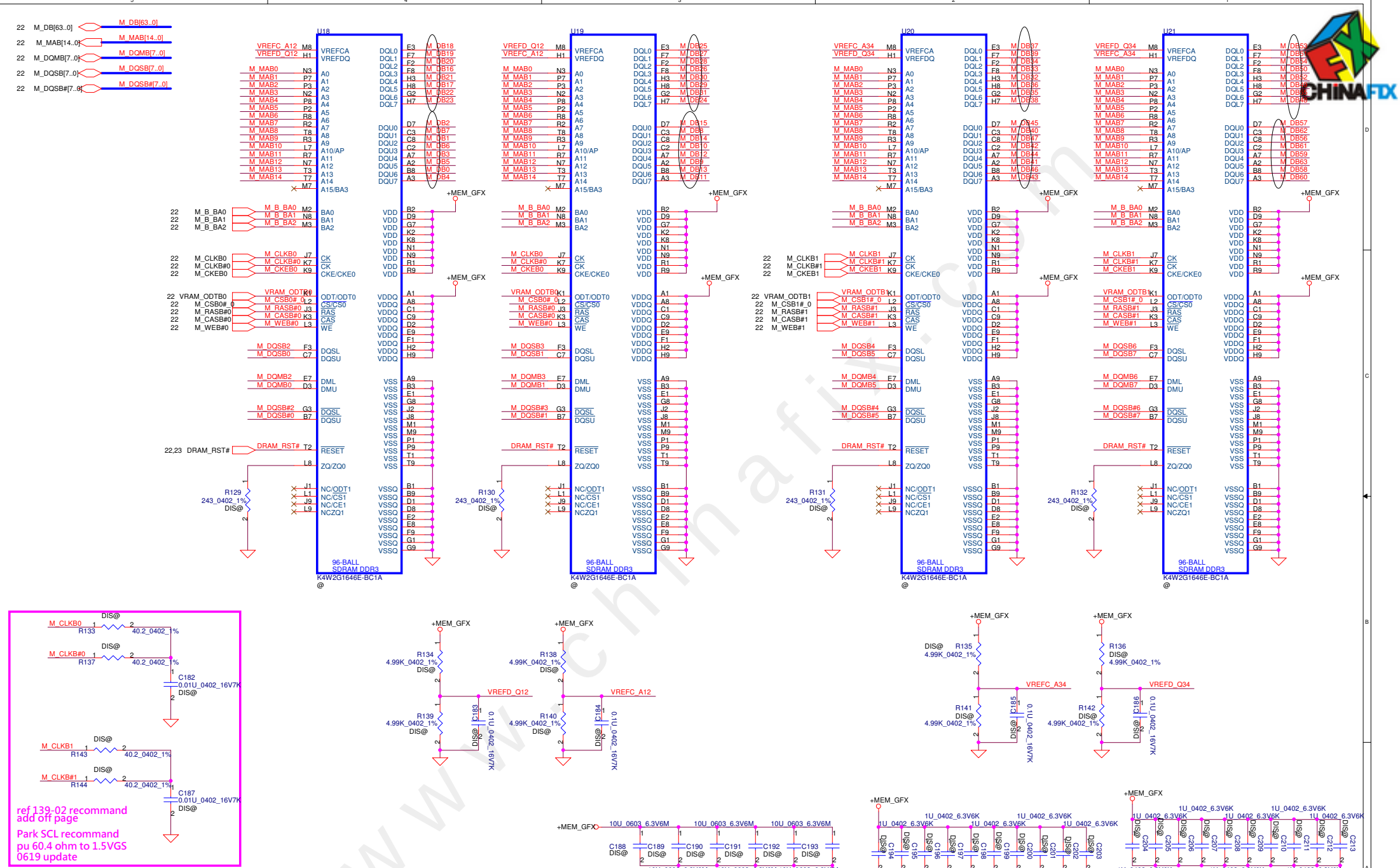


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| Issued Date | 2014/03/03 | Deciphered Date | 2015/03/03 |

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**Compal Electronics, Inc.**

Title: **Venus XTX(8/8) DDR3 VRAM_B**

Size: Custom | Document Number: **LA-B131P** | Rev: 1.0

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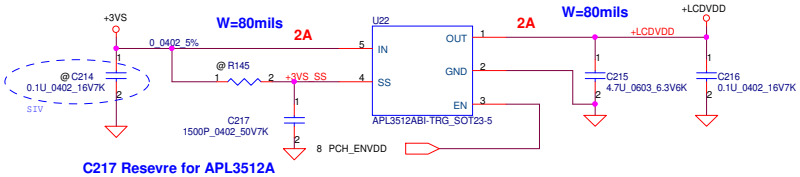
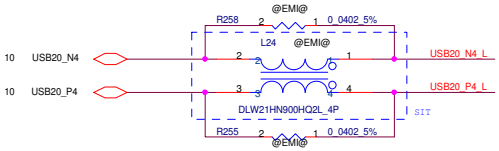
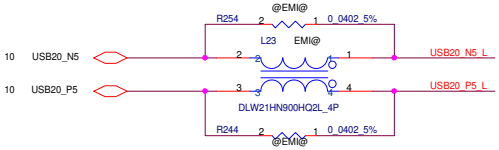
# LCD POWER CIRCUIT

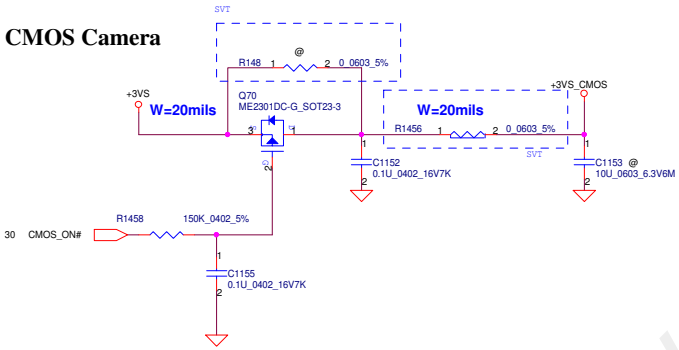


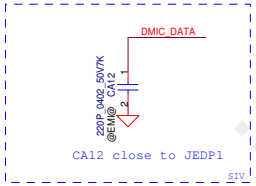

**C217 Resevre for APL3512A**
**R145 Resevre for G5243AT11U**

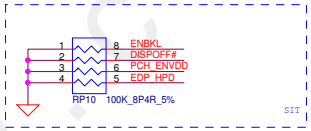


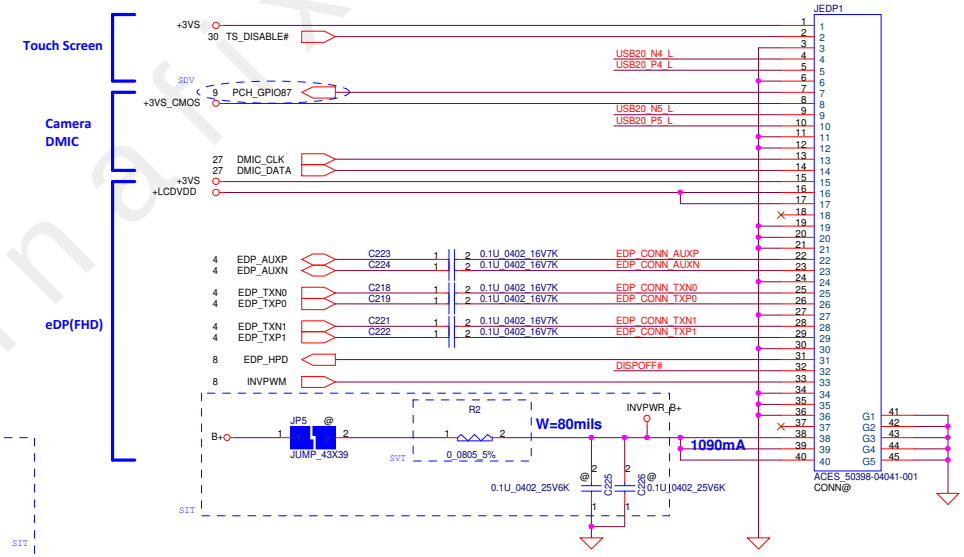

## CMOS Camera

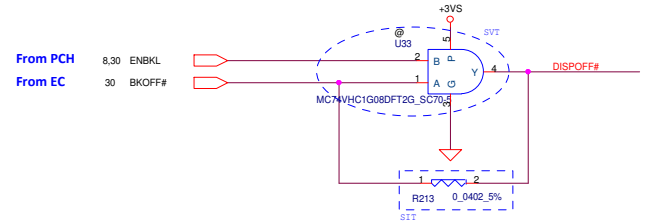


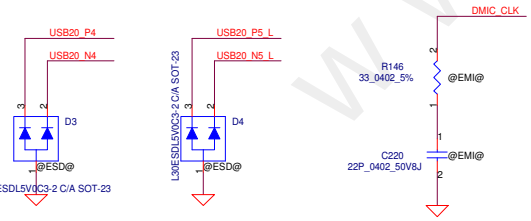




## eDP(FHD) + TOUCH + Camera

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**Compal Electronics, Inc.**

Title: **eDP LCD / Camera / Touch**

Size: Custom | Document Number: **LA-B131P** | Rev: 1.0

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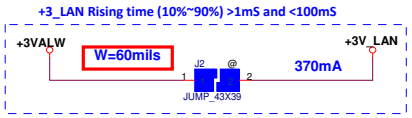
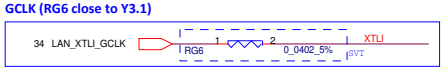
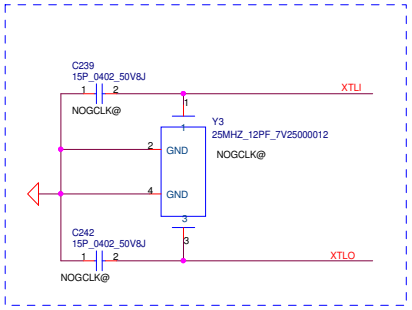
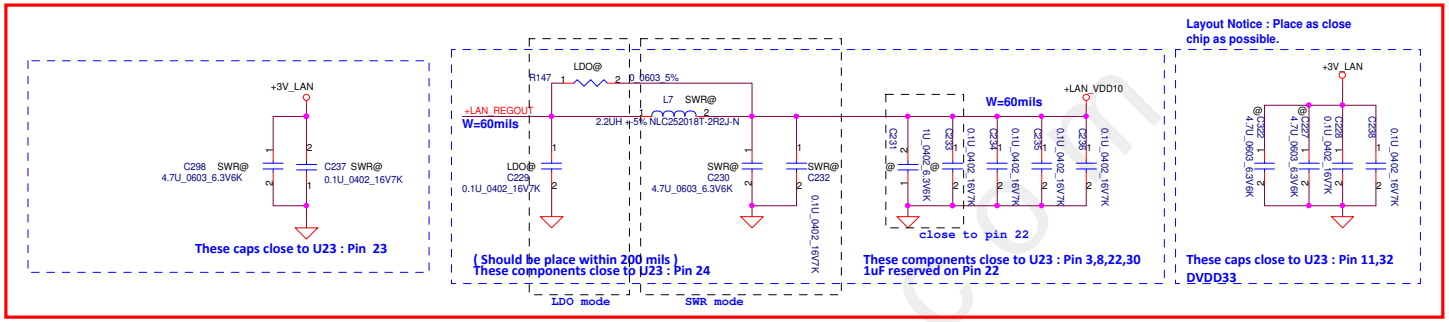
| RTL8111GS | L7 | C230 C232 | C298 C237 | R147 | C229 |
|---|---|---|---|---|---|
| SWR mode | O | O | O | X | X |

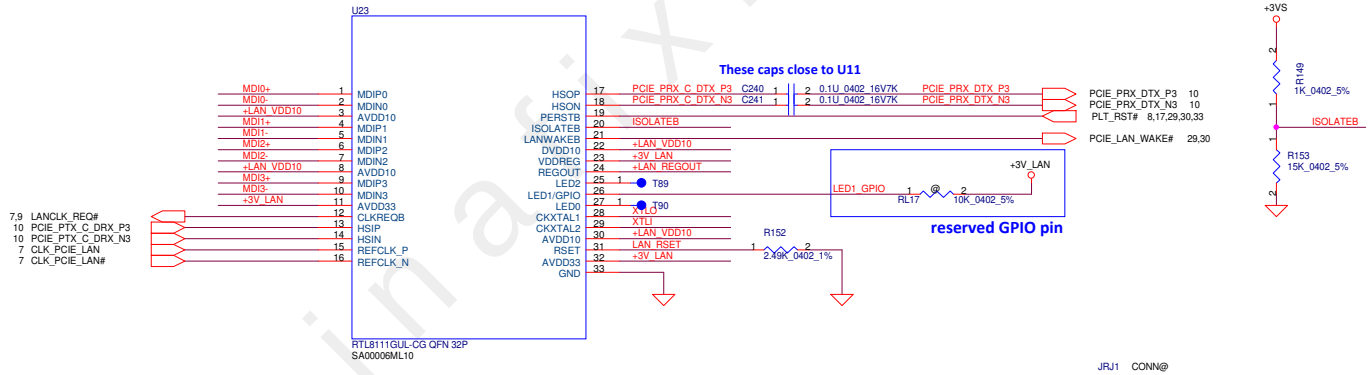
| RTL8111G | L7 | C230 C232 | C298 C237 | R147 | C229 |
|---|---|---|---|---|---|
| LDO mode | X | X | X | O | O |

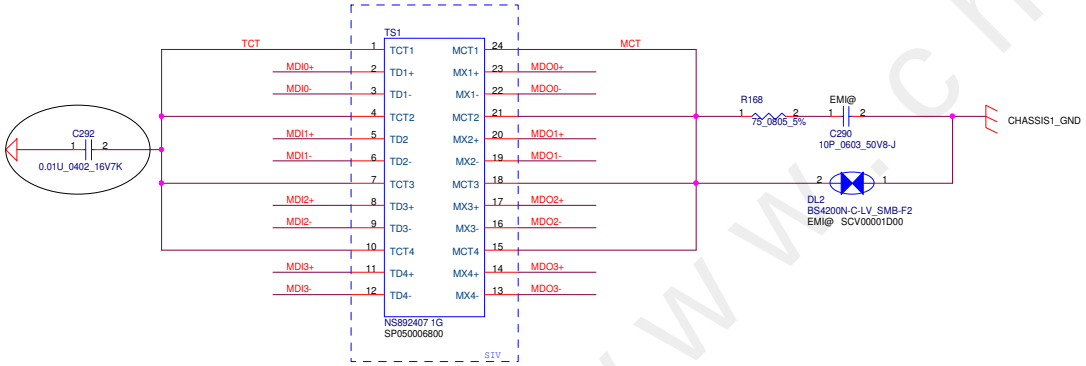


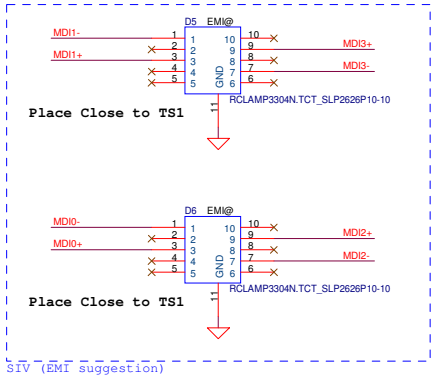



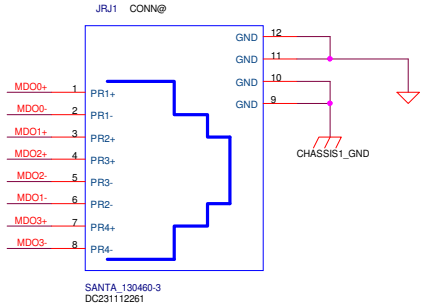

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Compal Electronics, Inc.

Title: LAN_RTL8111G-CG

Size: Custom | Document Number: LA-B131P | Rev: 1.0

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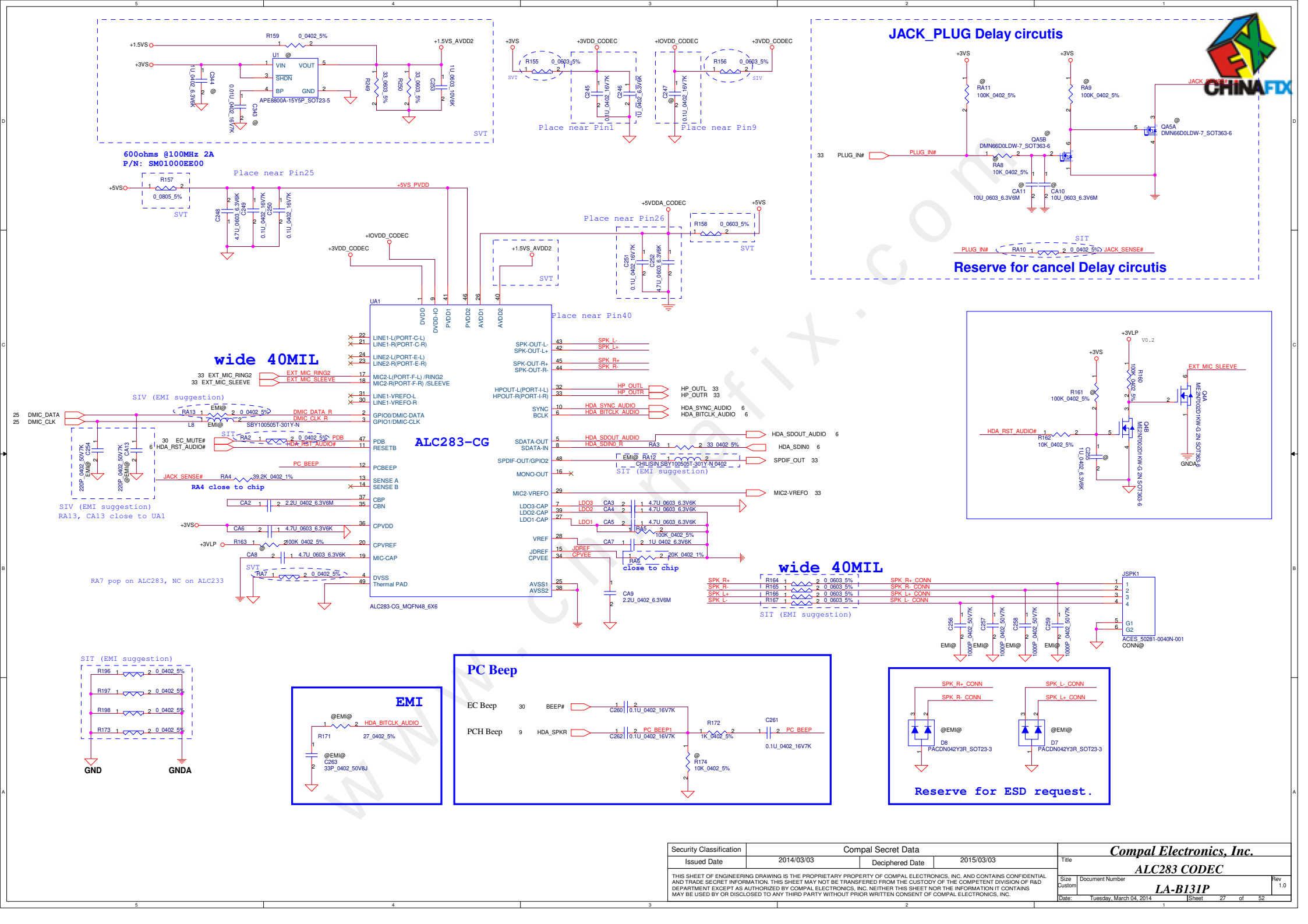


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|---|---|---|---|
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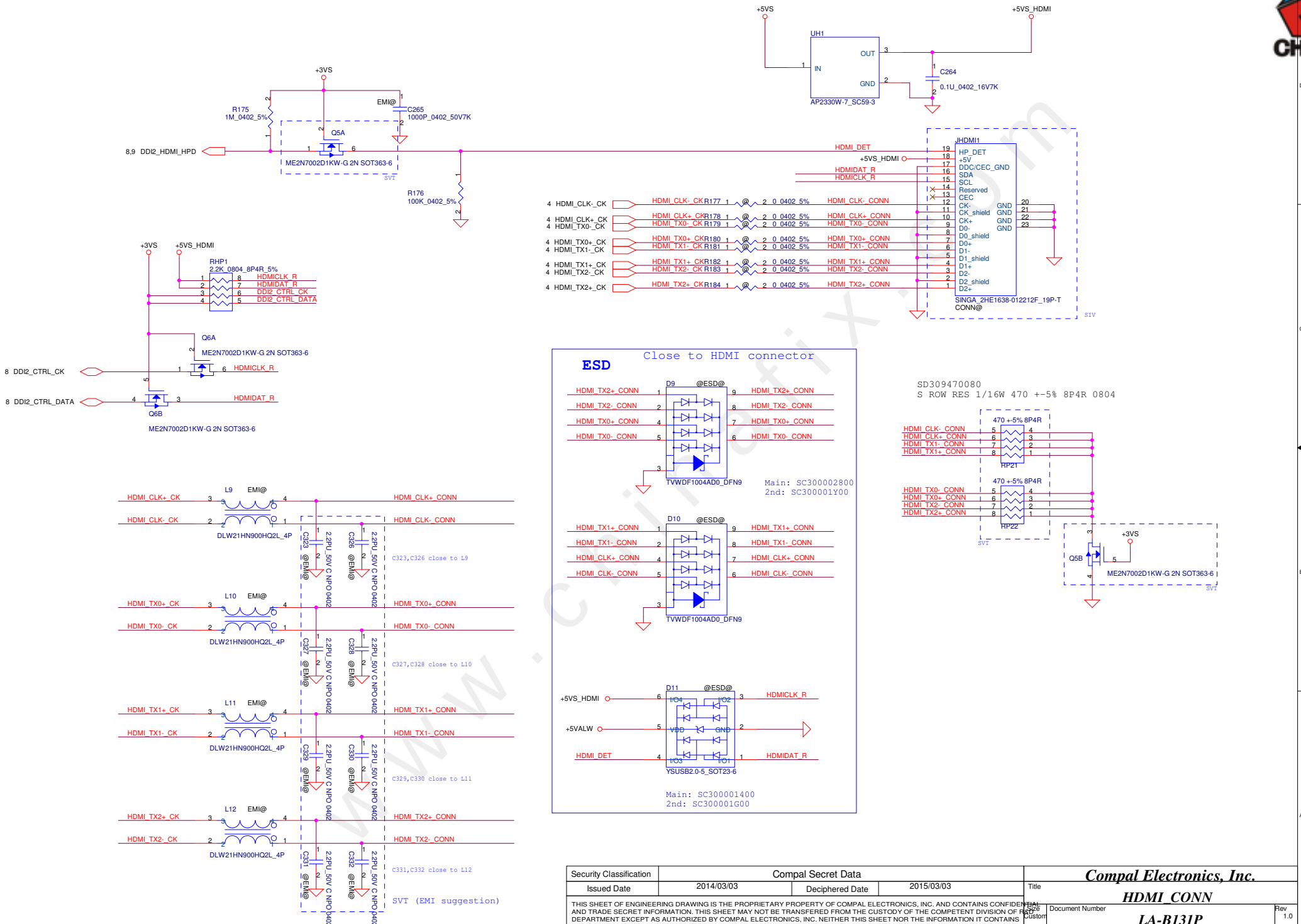
Compal Electronics, Inc.

Title: ALC283 CODEC

Size: Custom | Document Number: LA-B131P | Rev: 1.0

Date: Tuesday, March 04, 2014 | Sheet 27 of 52

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| Issued Date | 2014/03/03 | Deciphered Date | 2015/03/03 |

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**Compal Electronics, Inc.**

Title: **HDMI_CONN**

Size: Custom | Document Number: **LA-B131P** | Rev: 1.0

Date: Tuesday, March 04, 2014 | Sheet 28 of 52

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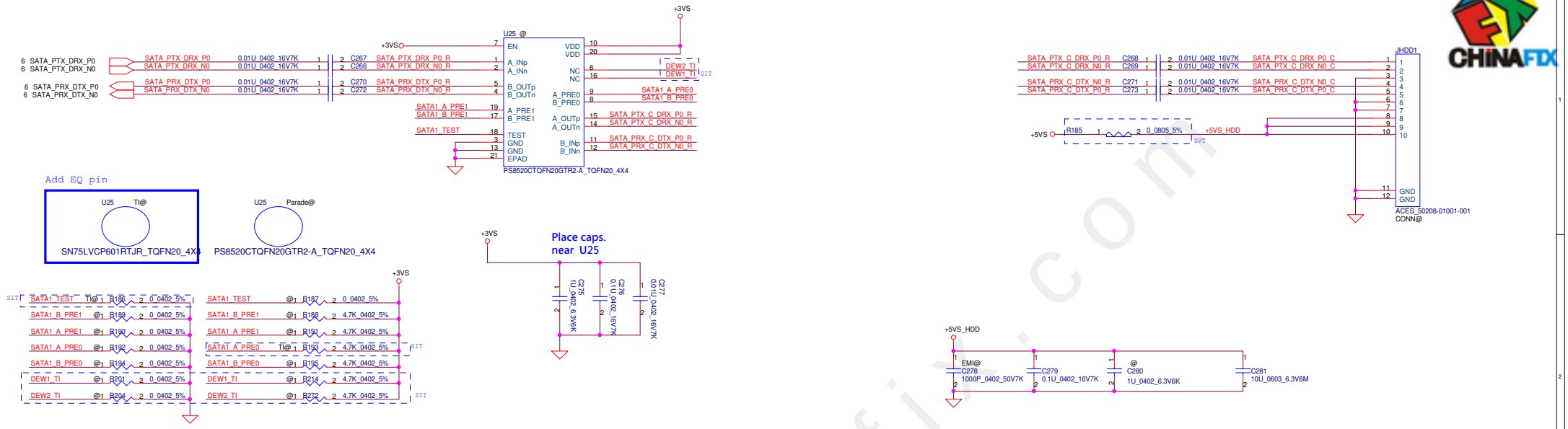
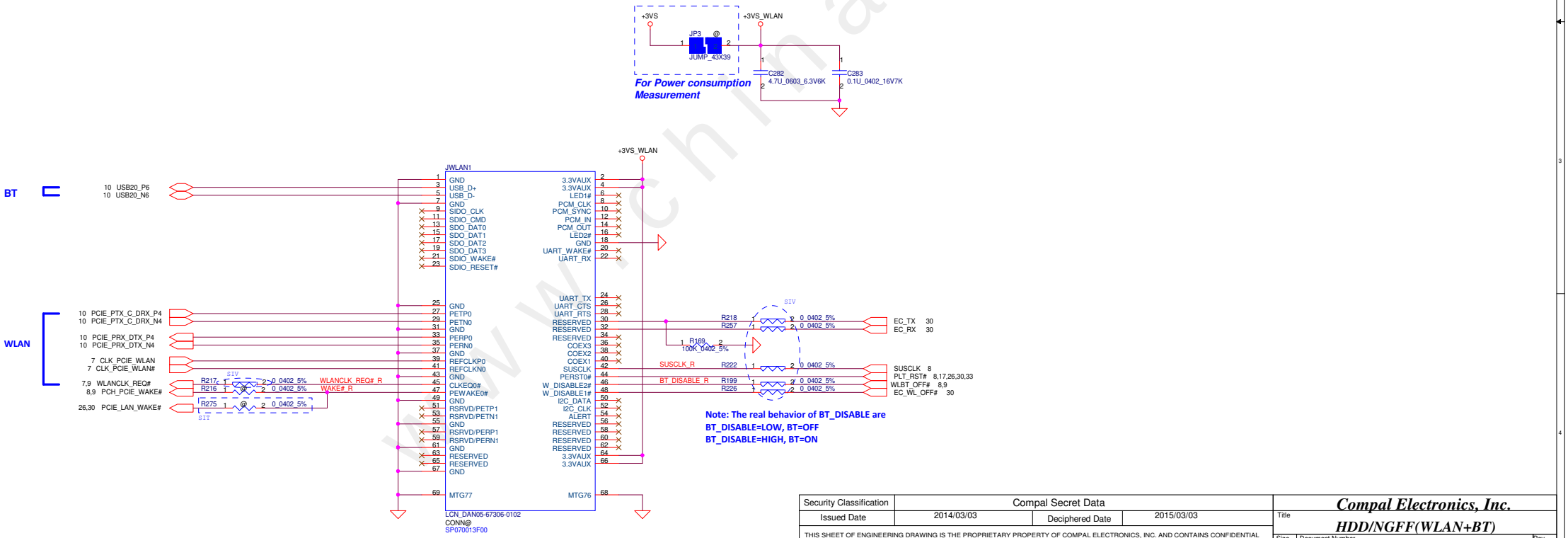
# SATA HDD (SSD) CONN.




# NGFF for WLAN+BT

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Compal Electronics, Inc.

Title: HDD/NGFF(WLAN+BT)

Size: Custom | Document Number: LA-B131P | Rev: 1.0

Date: Tuesday, March 04, 2014 | Sheet 29 of 52

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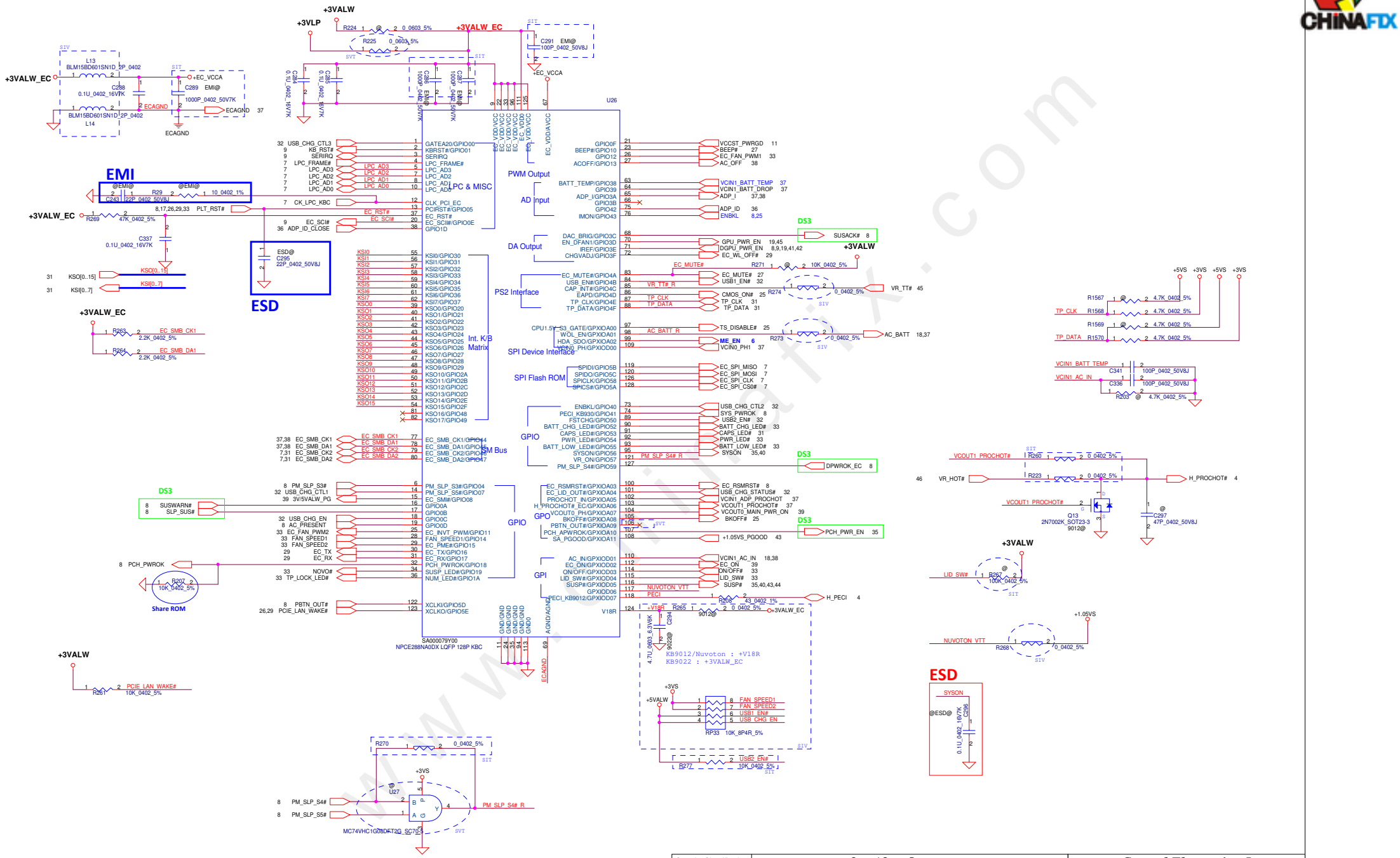


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|---|---|---|---|
| Issued Date | 2014/03/03 | Deciphered Date | 2015/03/03 |

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**Compal Electronics, Inc.**

Title: **BIOS & EC I/O Port**

Size: C | Document Number: **LA-B131P** | Rev: 1.0

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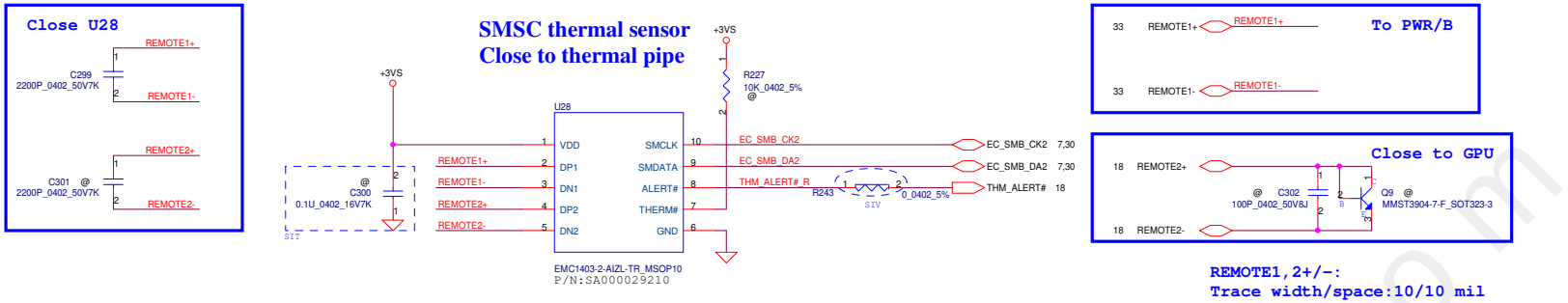
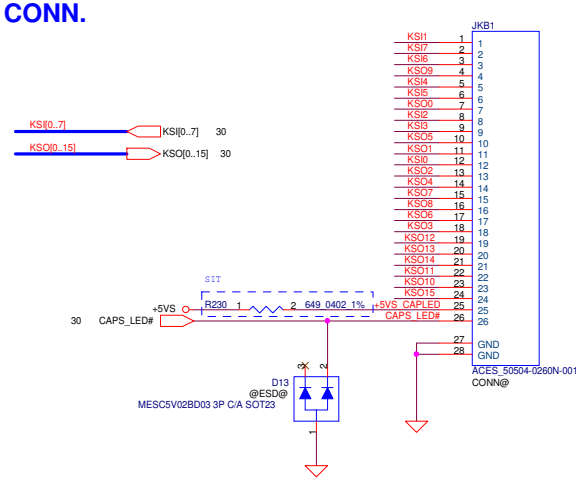
# Thermal Sensor




Address 1001_101xb F75303M P/N:SA000046C00

# KB CONN.

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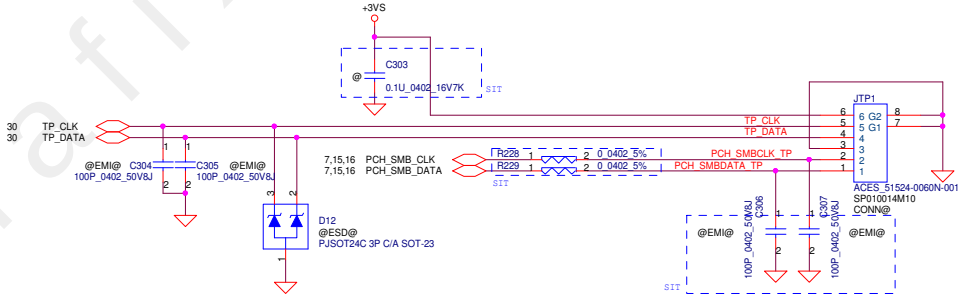


# Screw

**CPU**

H7 HOLEA — H_3P7
H12 HOLEA — H_3P7
H14 HOLEA — H_3P7

**GPU**

H9 HOLEA — H_3P7
H10 HOLEA — H_3P7
H11 HOLEA — H_3P7

FD1 FD2 FD3 FD4

**LAN**

H2 HOLEA — CHASSIS1_GND, H_3P3
H3 HOLEA — H_3P3
H5 HOLEA — H_1P5N
H8 HOLEA — H_1P5N

**Zero point**

H4 HOLEA — H_3P1N

**Board side**

H13 HOLEA — H_2P5
H15 HOLEA — H_2P5
H20 HOLEA — H_2P5
H19 HOLEA — H_4P1X3P1N
H16 HOLEA — H_2P5
H18 HOLEA — H_3P0
H6 HOLEA — H_2P5

**NGFF**

H17 HOLEA — H_3P3

**Fan**

H21 HOLEA — H_1P3X1P8N

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Compal Electronics, Inc.

Title: KB/TP/Thermal Sensor

Size: Custom | Document Number: LA-B131P | Rev: 1.0

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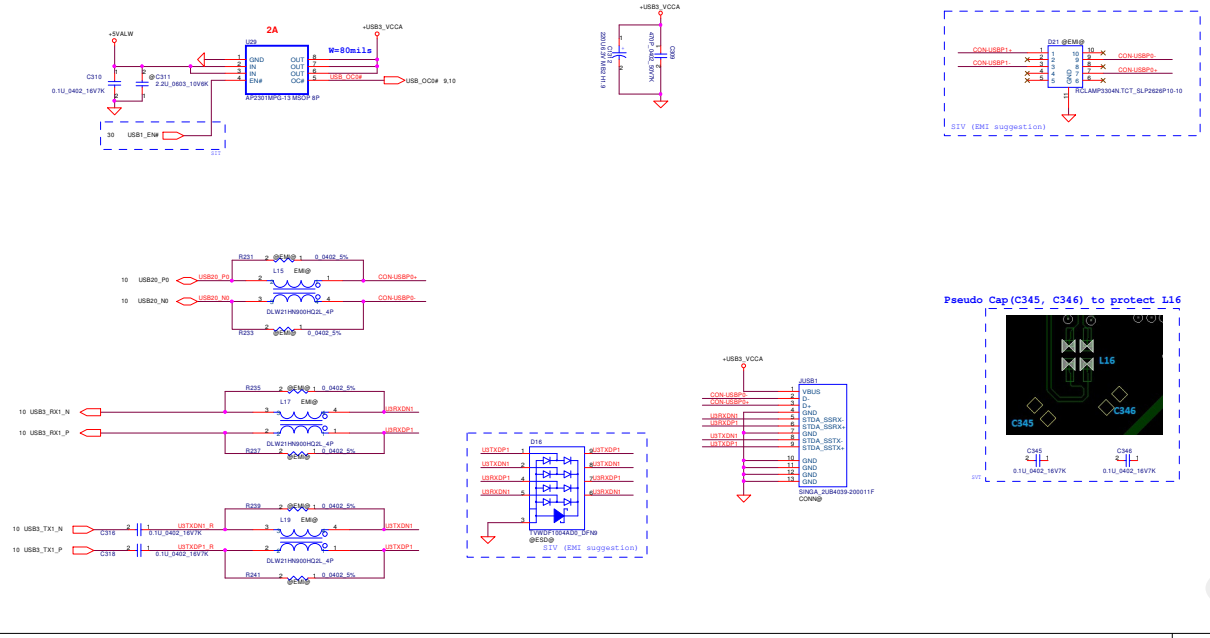
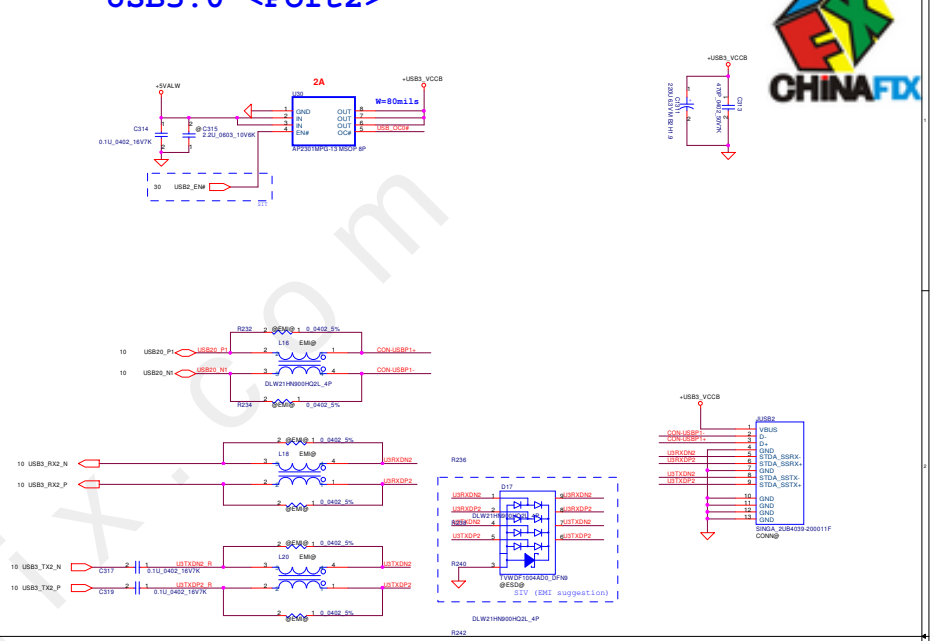
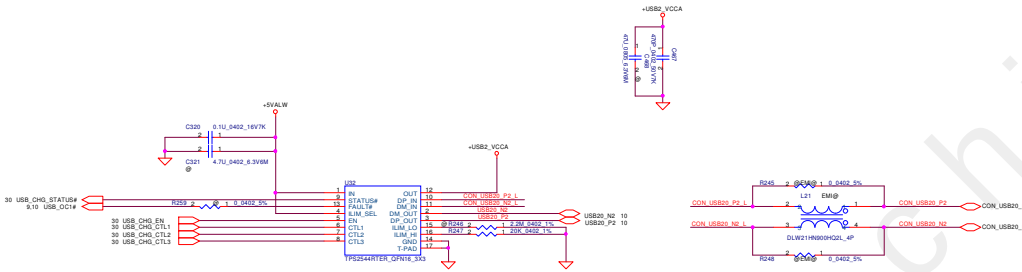
# USB3.0 <Port1>




# USB3.0 <Port2>




# USB2.0 + Charger

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Title: Compal Electronics, Inc.
USB2.0/3.0

Size: D | Document Number: LA-B131P | Rev: 1.0

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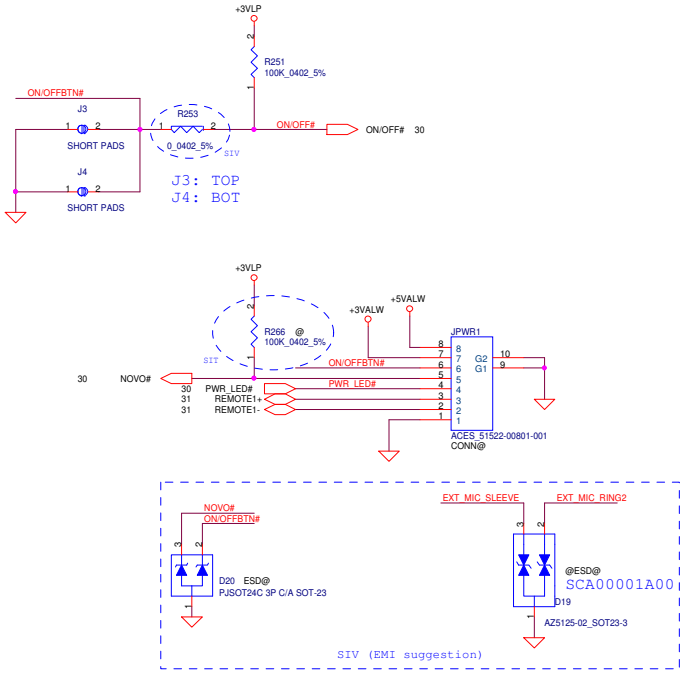
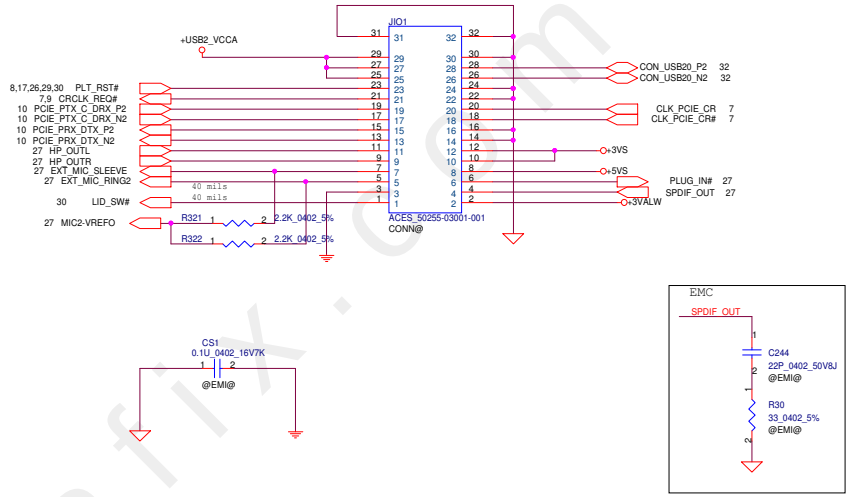
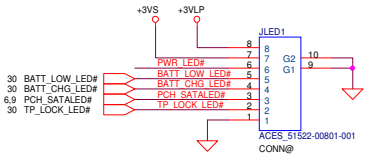
## Power Board CONN.



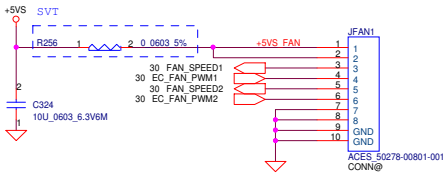

## I/O Board CONN.

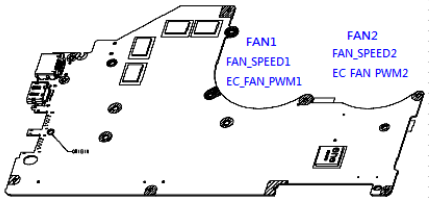



## LED Board CONN.




## FAN1 Conn




| FAN1 | FAN2 |
|---|---|
| FAN_SPEED1<br>EC_FAN_PWM1 | FAN_SPEED2<br>EC_FAN_PWM2 |

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2014/03/03 | Deciphered Date | 2015/03/03 |

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| | | |
|---|---|---|
| Title | Compal Electronics, Inc.<br>FAN/PWR/LED/IO Board | |
| Size C | Document Number<br>LA-B131P | Rev 1.0 |
| Date: Tuesday, March 04, 2014 | Sheet 33 of 52 | |

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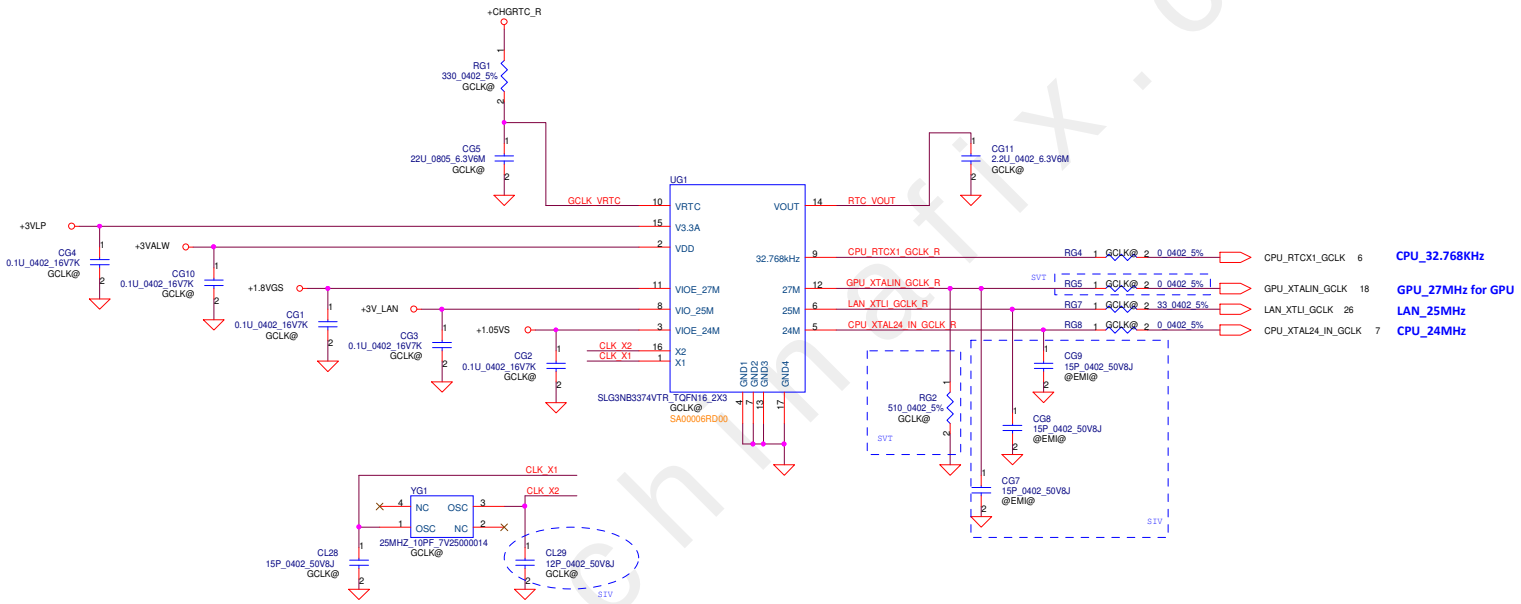


| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2014/03/03 | Deciphered Date | 2015/03/03 |

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**Compal Electronics, Inc.**

Title: **GCLK**

Size | Document Number: **LA-B131P** | Rev: 1.0

Date: Tuesday, March 04, 2014 | Sheet 34 of 52

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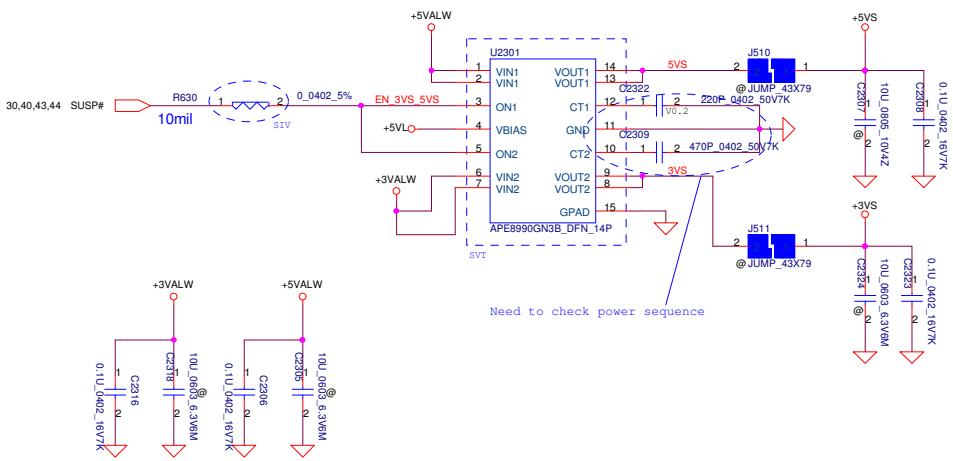
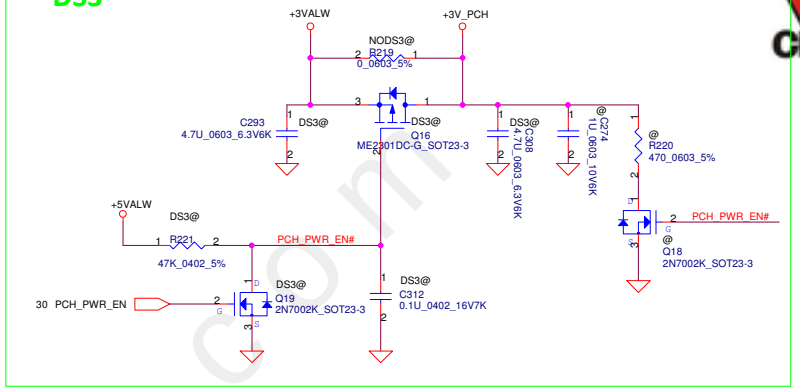
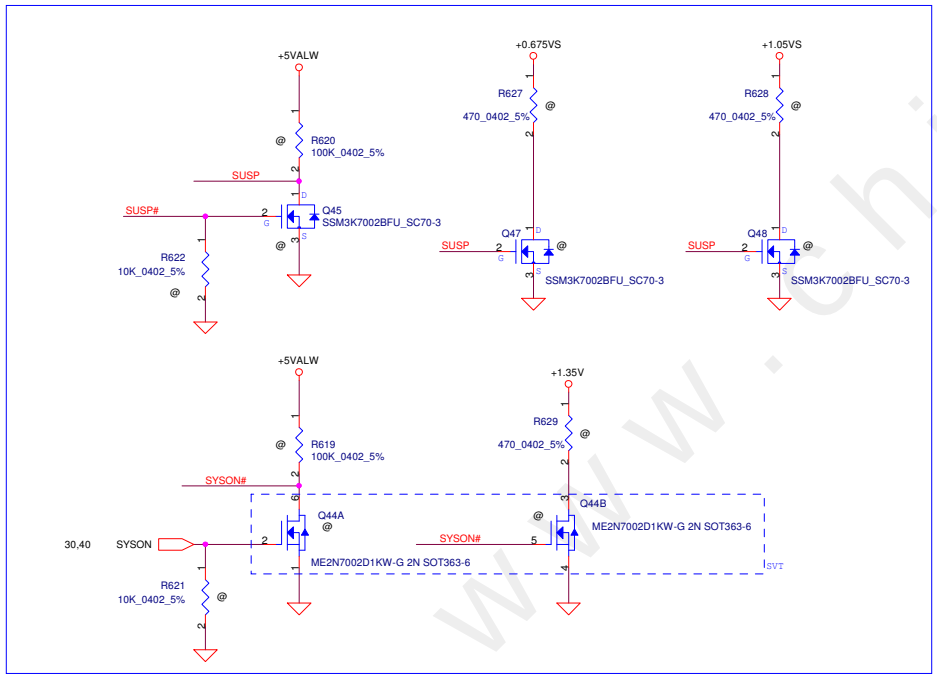
## +5VALW TO +5VS
## +3VALW TO +3VS




## DS3

## +3VALW to +3V_PCH

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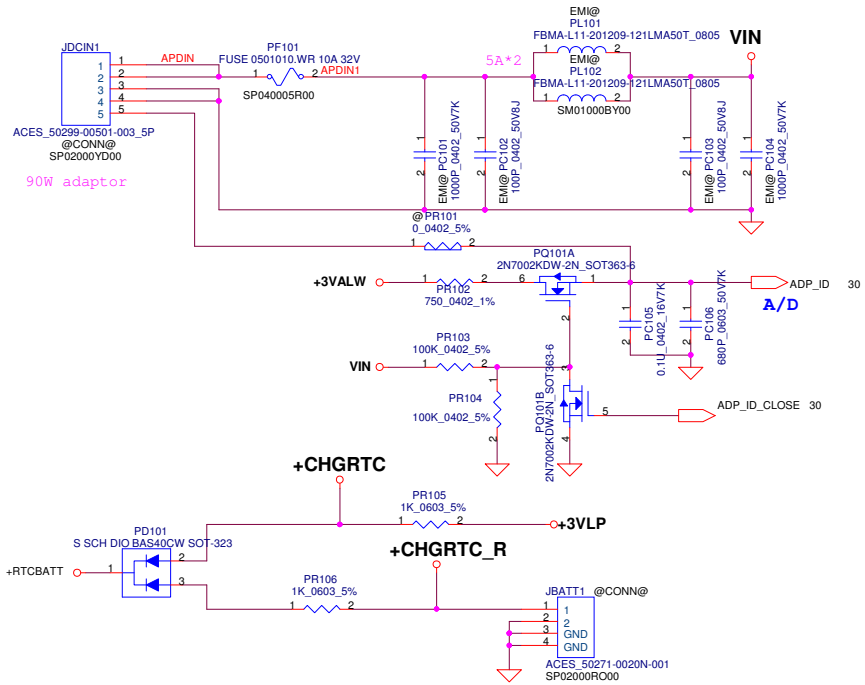
**Compal Electronics, Inc.**

Title: DC/DC Interface

Size: Custom | Document Number: LA-B131P | Rev: 1.0

Date: Tuesday, March 04, 2014 | Sheet 35 of 52




**RTC Battery** GC02001DR00
BATT CR2032 3V 210MAH MB 5 W/C
30MM

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| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2014/03/03 | Deciphered Date | 2015/03/03 |

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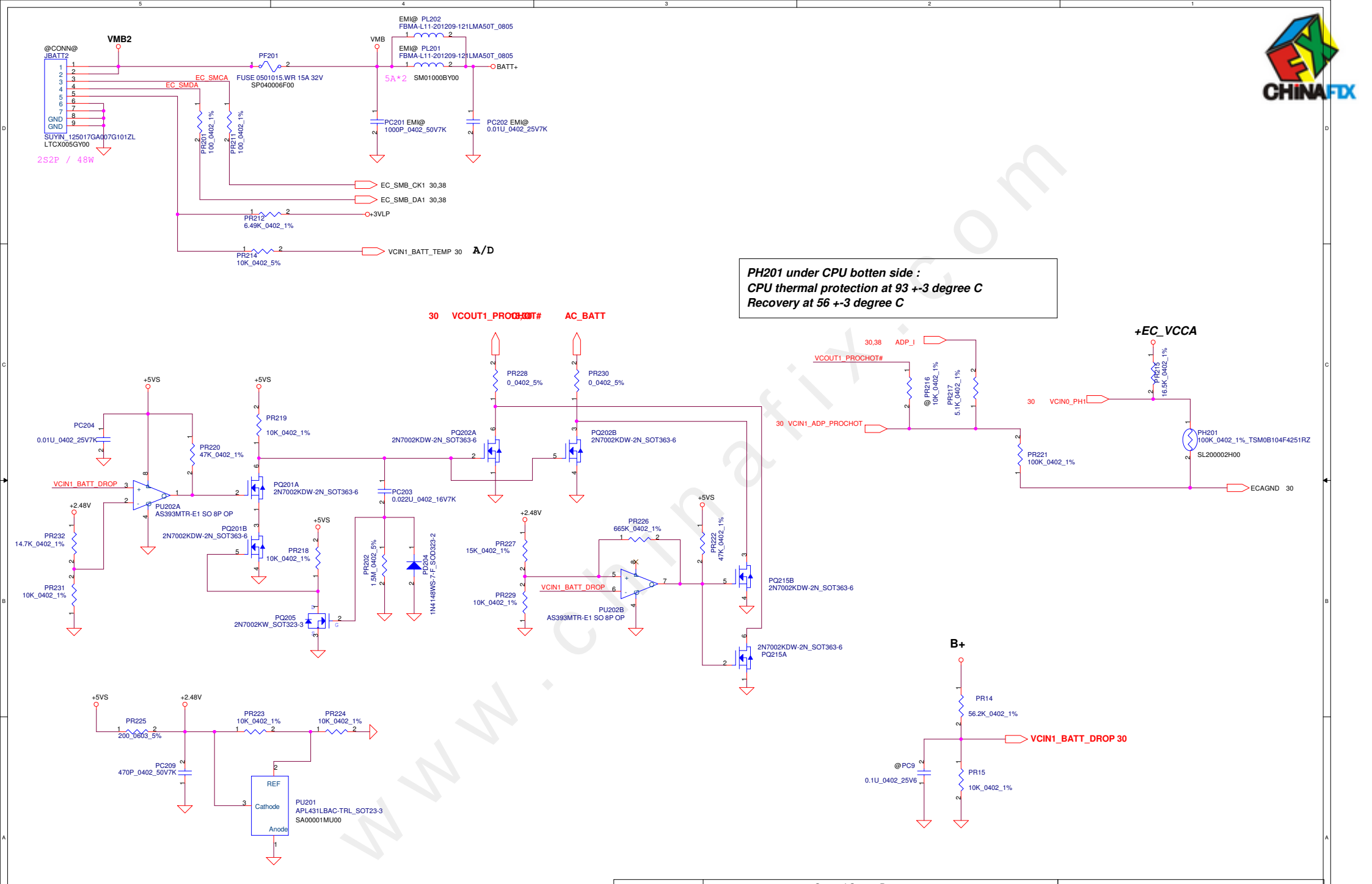
*Compal Electronics, Inc.*

Title: **PWR DCIN / RTC Battery**

Size: Custom | Document Number: **BE_BDW** | Rev: 1.0

Date: Tuesday, March 04, 2014 | Sheet 36 of 52

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Title: *Compal Electronics, Inc.*
**PWR-BATTERY CONN/OTP**

Size: Custom | Document Number: **BE_BDW** | Rev: 1.0

Date: Tuesday, March 04, 2014 | Sheet 37 of 52

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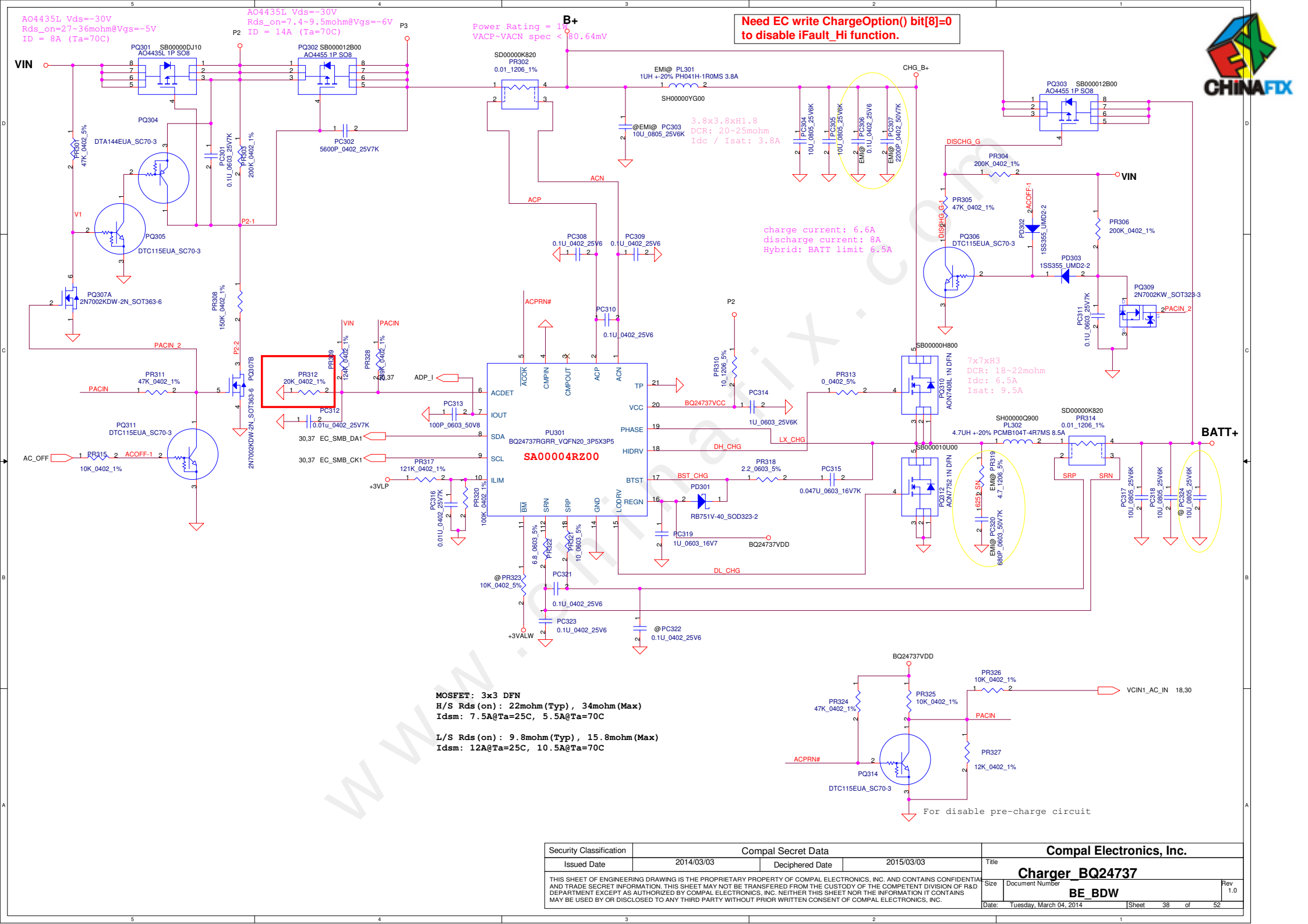


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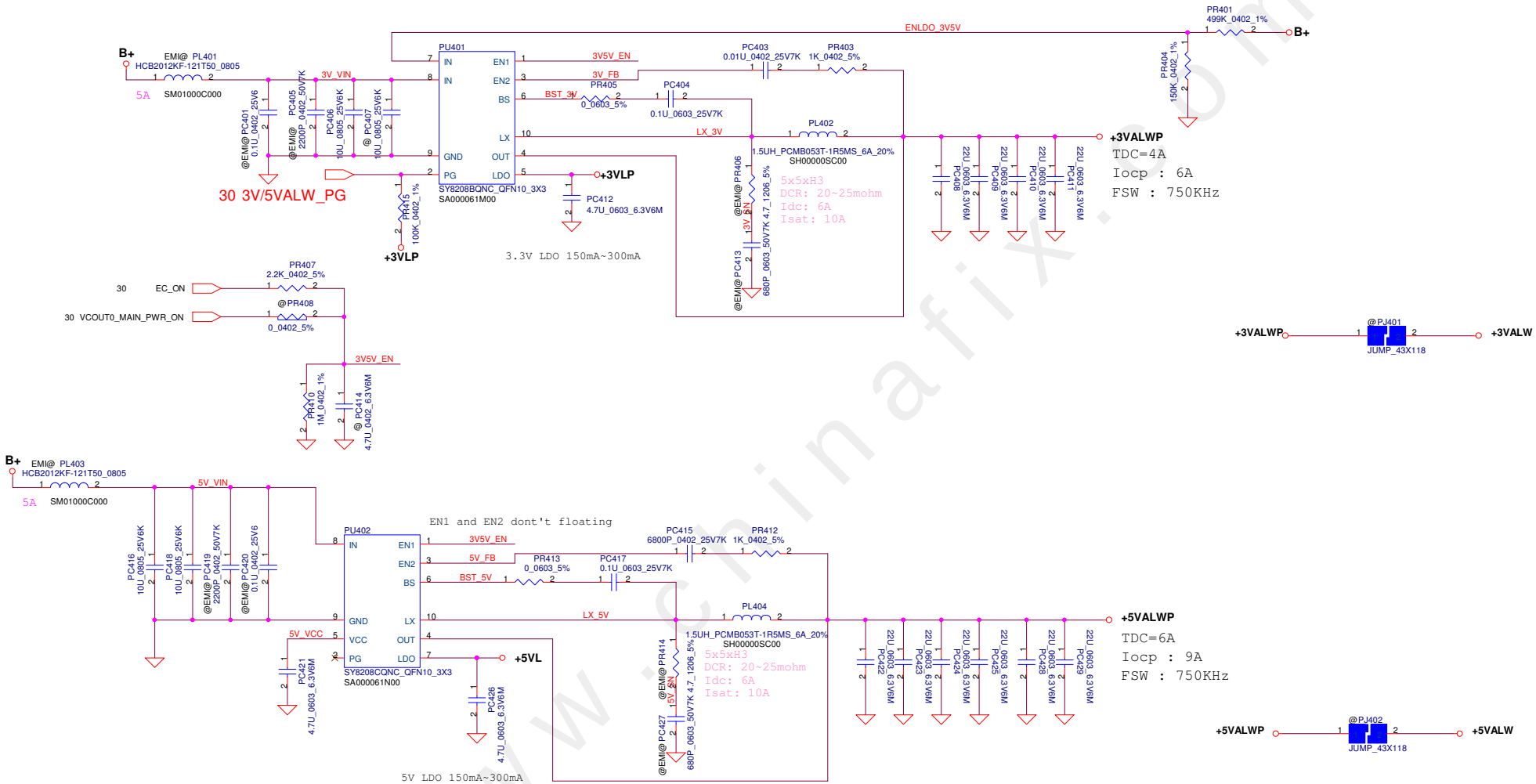


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| Issued Date | 2014/03/03 | Deciphered Date | 2015/03/03 |

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**Compal Electronics, Inc.**

Title: **+3VALW/+5VALW**

Size: Custom | Document Number: **BE_BDW** | Rev: 1.0

Date: Tuesday, March 04, 2014 | Sheet 39 of 52

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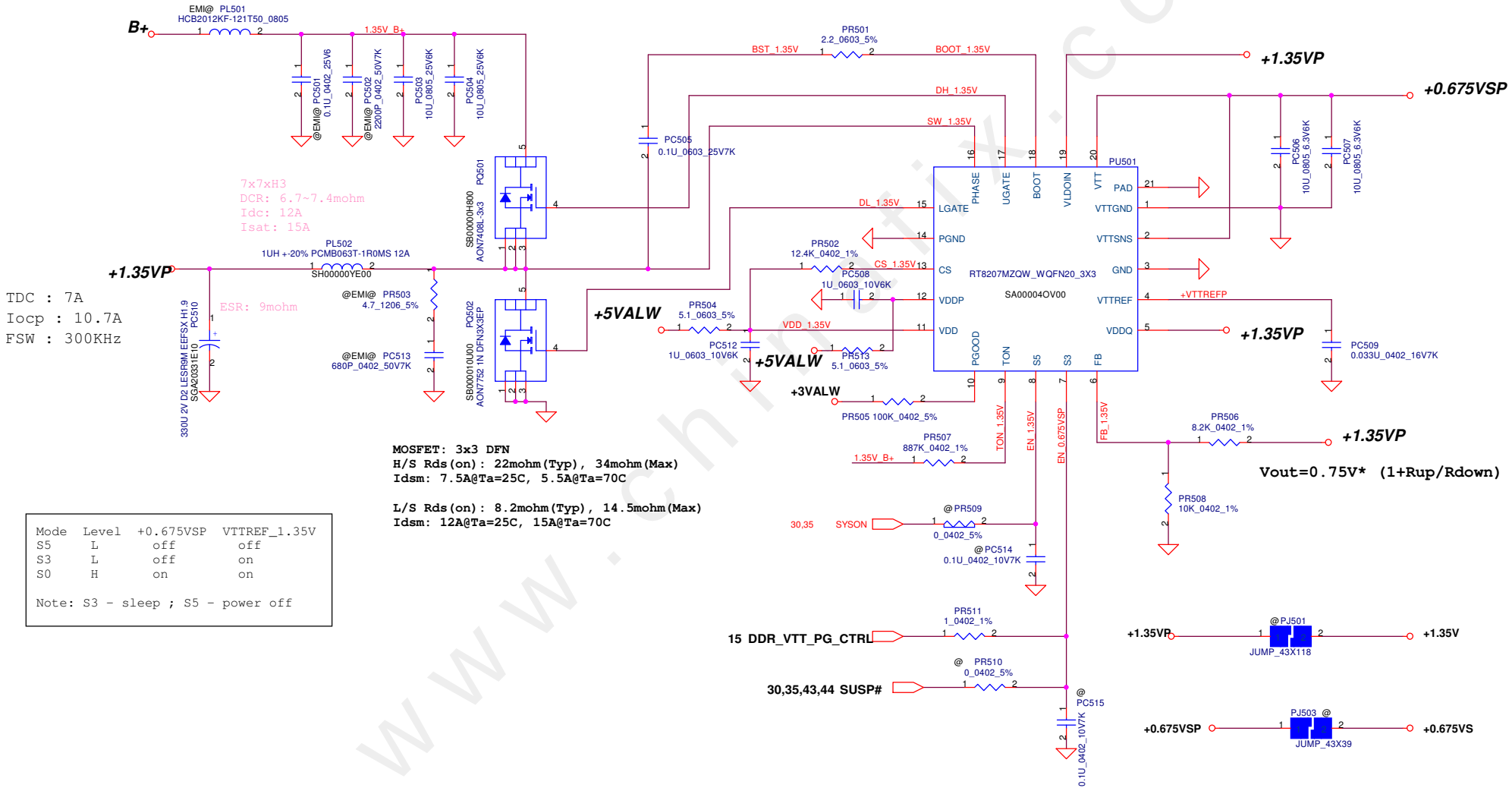


| Mode | Level | +0.675VSP | VTTREF_1.35V |
|---|---|---|---|
| S5 | L | off | off |
| S3 | L | off | on |
| S0 | H | on | on |

Note: S3 - sleep ; S5 - power off

| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2014/03/03 | Deciphered Date | 2015/03/03 |

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Compal Electronics, Inc.

Title: RT8207M

Size: Custom | Document Number: BE_BDW | Rev: 1.0

Date: Tuesday, March 04, 2014 | Sheet 40 of 52

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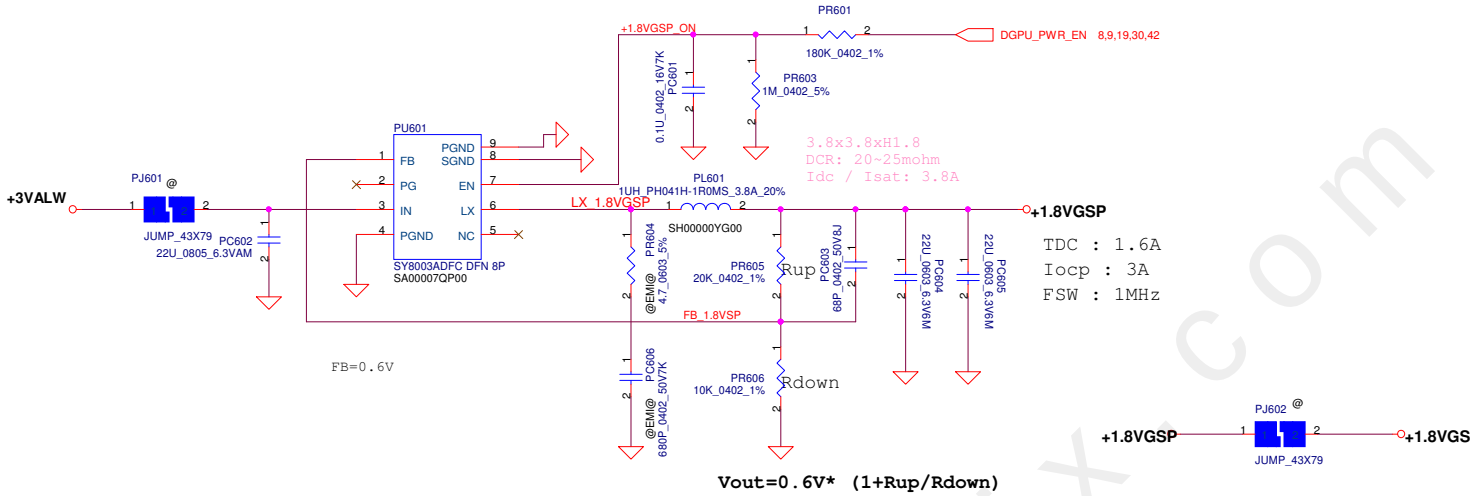


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| Issued Date | 2014/03/03 | Deciphered Date | 2015/03/03 | Title: +1.8VGS |
| | | | | Size: Custom; Document Number: BE_BDW; Rev: 1.0 |
| | | | | Date: Tuesday, March 04, 2014; Sheet 41 of 52 |

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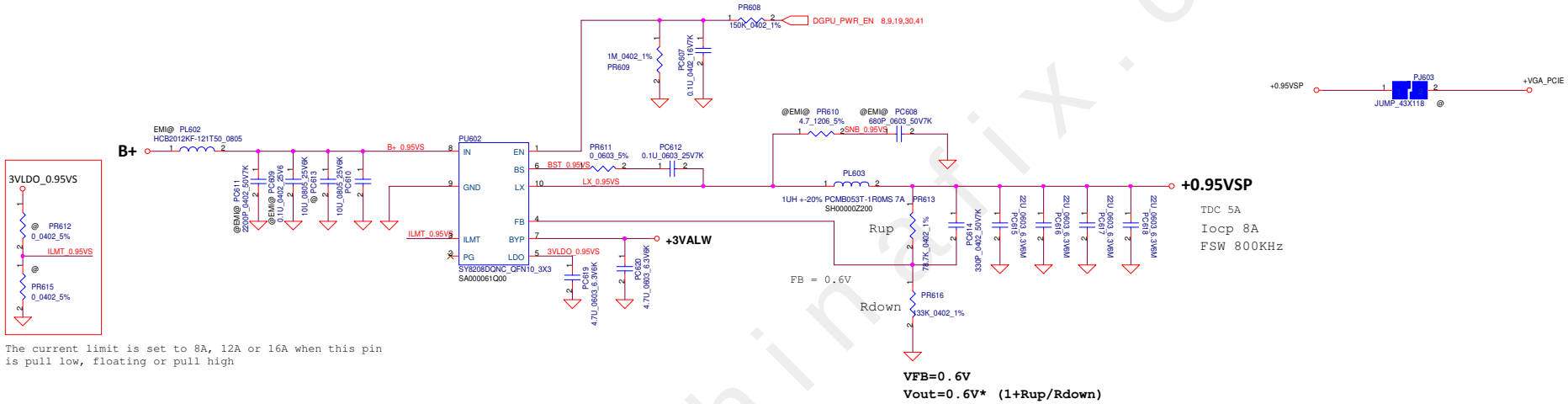


The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. |
|---|---|---|---|---|
| Issued Date | 2014/03/03 | Deciphered Date | 2015/03/03 | Title: 0.95VS |
| | | | | Size: C; Document Number: BE_BDW; Rev: 1.0 |
| | | | | Date: Tuesday, March 04, 2014; Sheet 42 of 52 |

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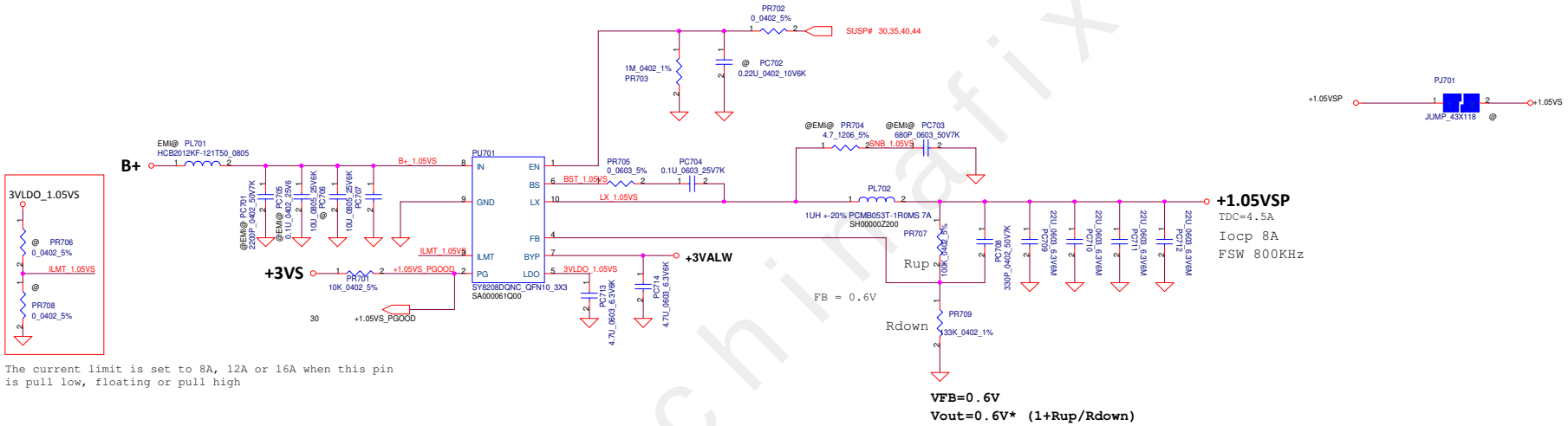


The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

**VFB=0.6V**
**Vout=0.6V* (1+Rup/Rdown)**

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2014/03/03 | Deciphered Date | 2015/03/03 |

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*Compal Electronics, Inc.*

Title: **+1.05VS**

Size: C | Document Number: **BE_BDW** | Rev: 1.0

Date: Tuesday, March 04, 2014 | Sheet 43 of 52

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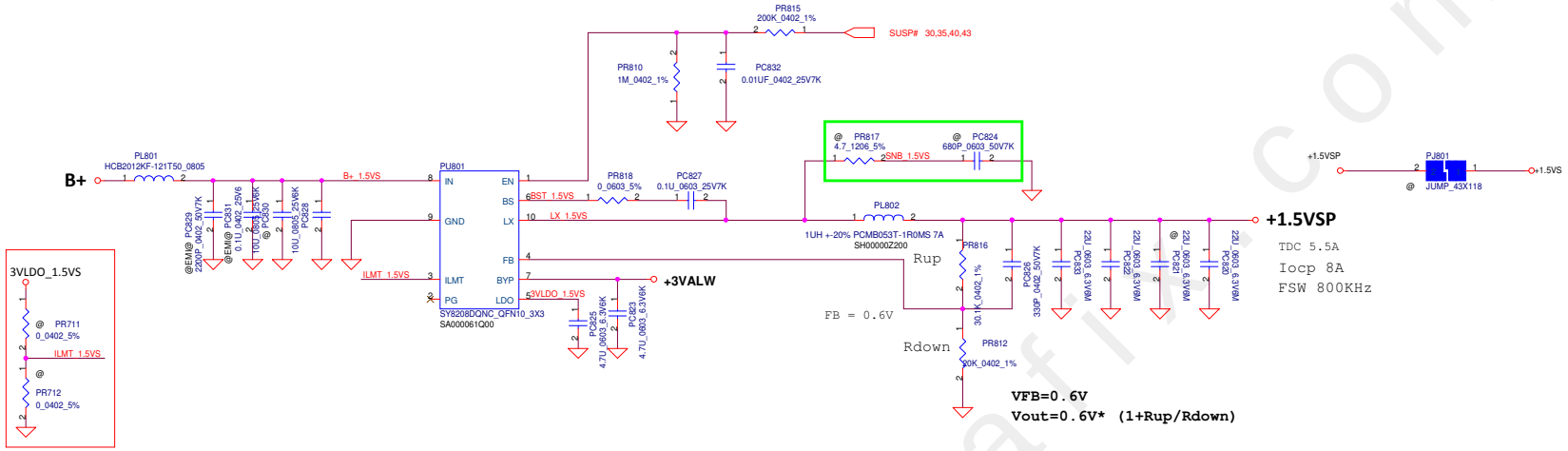


The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

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|---|---|---|---|
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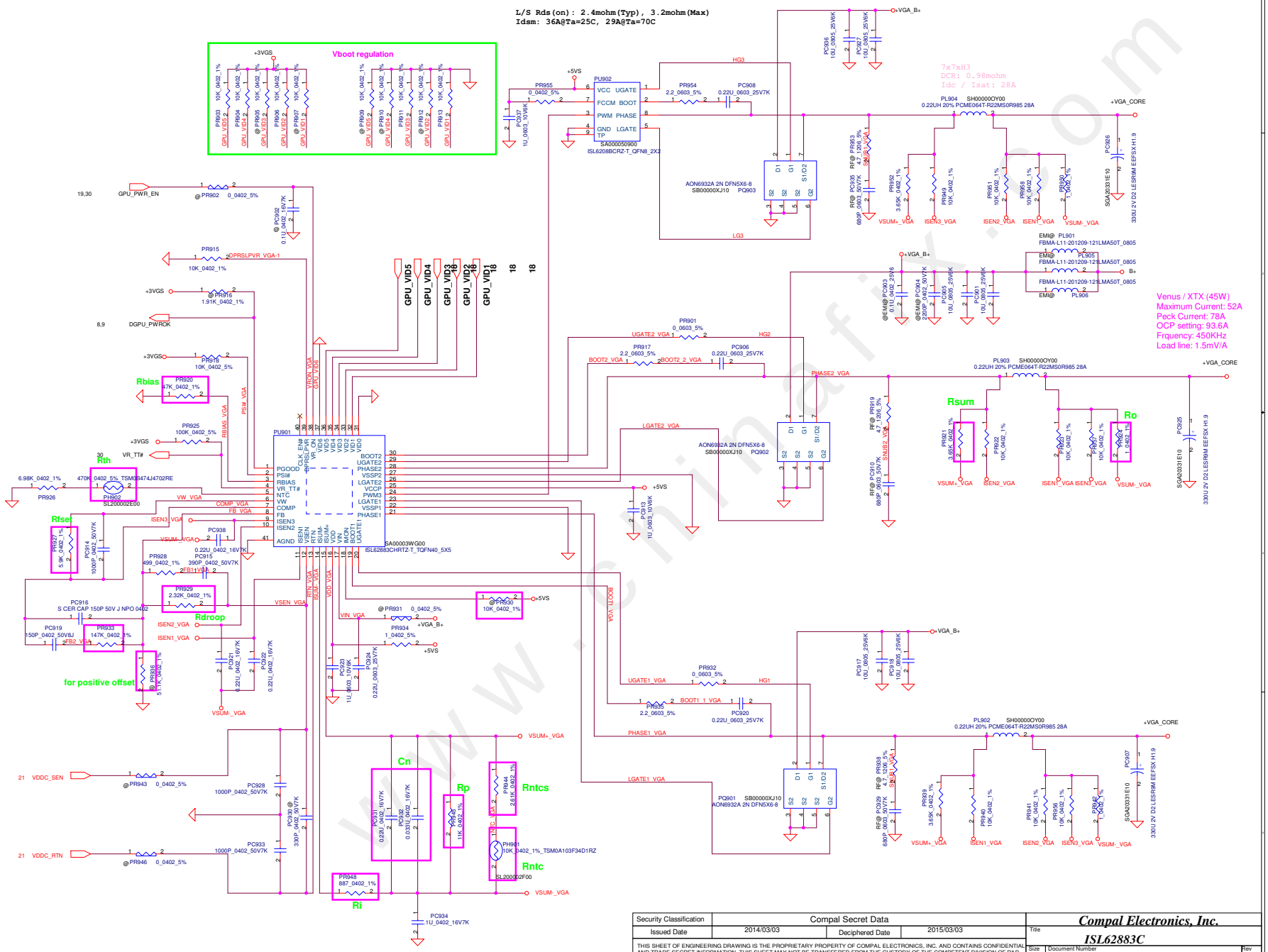
**Compal Electronics, Inc.**

Title: **+1.5VSP**

Size: C | Document Number: **LA-A321PR01** | Rev: 1.0

Date: Tuesday, March 04, 2014 | Sheet 44 of 52




| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2014/03/03 | Deciphered Date | 2015/03/03 |

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Compal Electronics, Inc.

Title: ISL62883C

Size | Document Number | Rev 1.0

Date: Tuesday, March 04, 2014 | Sheet 45 of 52

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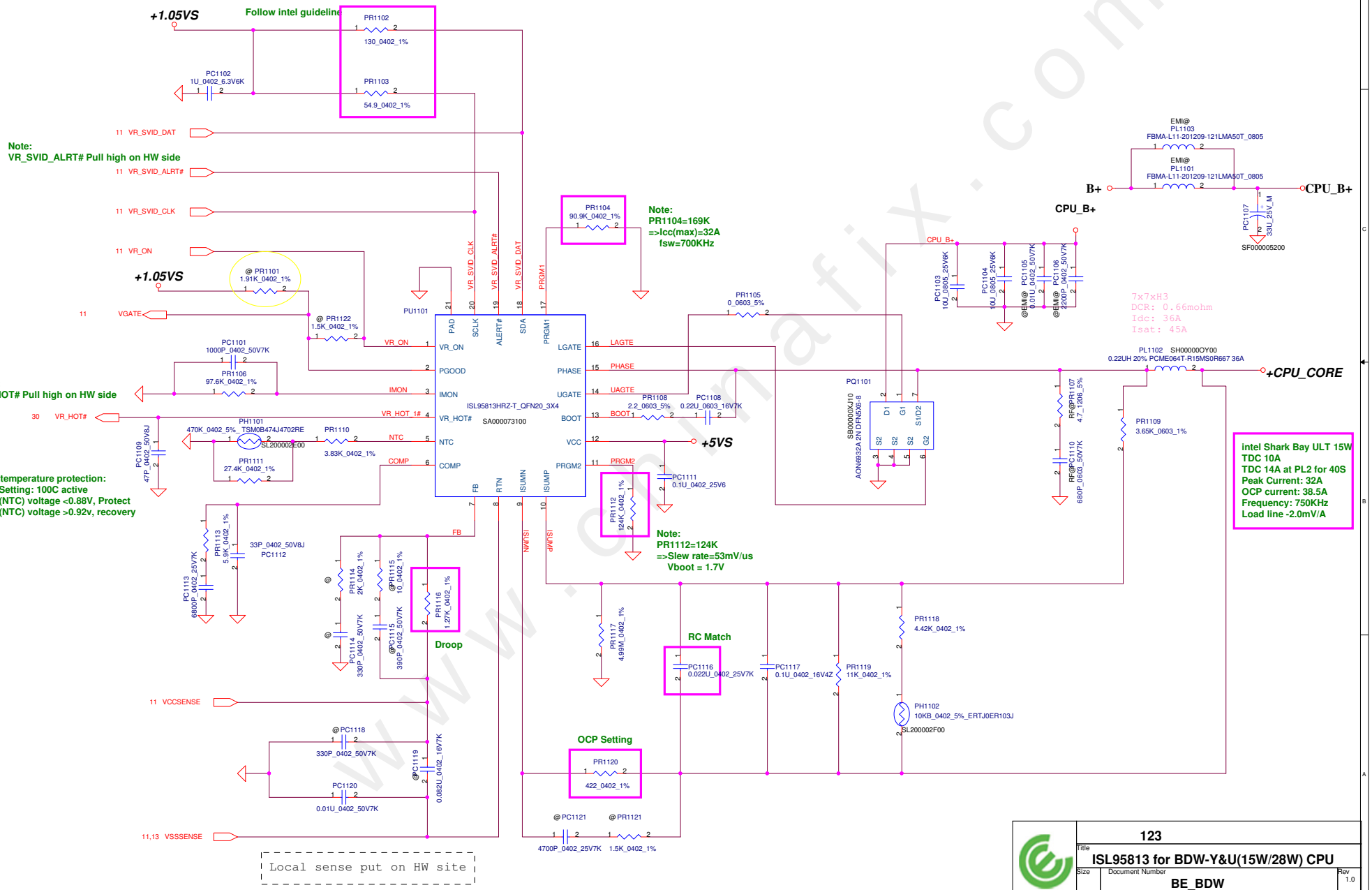


| | |
|---|---|
| Title | ISL95813 for BDW-Y&U(15W/28W) CPU |
| Size | |
| Document Number | BE_BDW |
| Rev | 1.0 |
| Date: | Tuesday, March 04, 2014 |
| Sheet | 46 of 52 |

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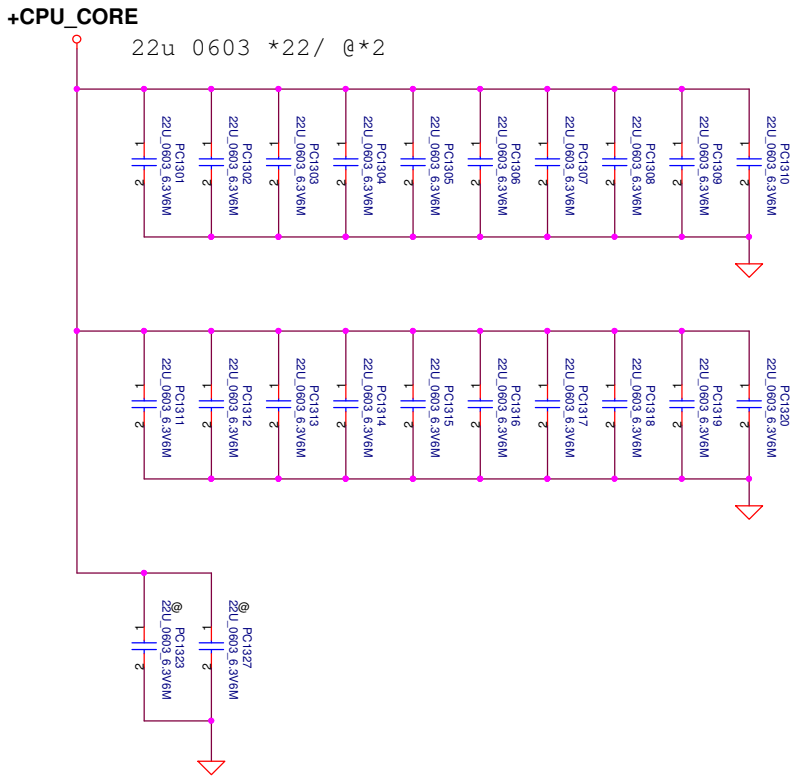


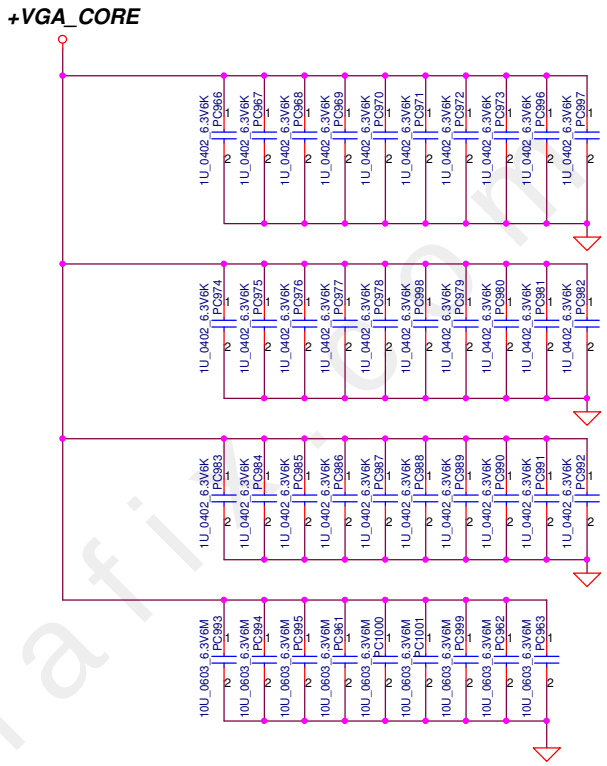


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| Issued Date | 2014/03/03 | Deciphered Date | 2015/03/03 |

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**Compal Electronics, Inc.**

Title: **PWR-PROCESSOR DECOUPLING**

Size: Custom | Document Number: **BE_BDW** | Rev: 1.0

Date: Tuesday, March 04, 2014 | Sheet 47 of 52

# Version change list (P.I.R. List)



| Item | Reason for change | PG# | Modify List | Date | Phase |
|---|---|---|---|---|---|
| 1 | link with HW side | 45 | change net name +3VS_VGA or +3VGS | 11/15 | SIV |
| 2 | modify VCORE setting | 46 | 1. Change the PR1120 from 280 Ohm to 287 Ohm.<br>2. Change the PR1117 from @ to 4.99MOhm.<br>3. Change the PR1118 from 2.61kOhm to 4.42kOhm.<br>4. Change the PC1101 from @ to 1000pF.<br>5. Change the PR1106 from @ to 97.5kOhm.<br>6. Change the PR1114 from 2kOhm to @.<br>7. Change the PC1114 from 330pF to @. | 11/15 | SIV |
| 3 | for RF request | 45 | PR953, PC935, PR919, PC910, PR938, PC929 change to mount | 11/19 | SIV |
| 4 | for RF request | 46 | PR1107, PC1110 change to mount | 11/19 | SIV |
| 5 | SIV MEMO | 46 | PR1101 change to NA | 12/24 | SIT |
| 6 | Valure modify | 45 | PC916 change to 150p | 12/24 | SIT |
| 7 | AC detect valure setting | 38 | PR309 is changed from 392K_0402_1% to 124K_0402_1% (SD034124380)<br>PR312 is changed from 59K_0402_1% to 20K_0402_1% (SD034200280)<br>Add a resistor 249K_0402_1% (SD034249380) between pin 6 of PU301 and PACIN.<br>PC312 is changed from 2200pF_0402_25V_X7R to 0.01uF_0402_25V_X7R (SE075103K80) | 12/24 | SIT |
| 8 | for EMI request | 38 | Add 2caps to GND, Add 1 SNUB<br>(PC320=0603 680pF, PR319=1206 4.7ohm, PC306=0.1uF, PC307=2200pF) | 12/24 | SIT |
| 9 | battery can't be remove | 37 | del PC206, PD201, PC205, PR307, PQ306, PQ313 | 12/24 | SIT |
| 10 | modify VCORE setting | 46 | Change PR1120 to 422ohm.<br>Change PR1104 to 90.9Kohm. | 02/20 | SVT |
| 11 | modify VCORE setting | 47 | Add PC1320 22uF. | 02/20 | SVT |

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# Version change list (P.I.R. List)



| Item | Reason for change | PG# | Modify List | Date | Phase |
|---|---|---|---|---|---|
| 1 | HW design | 09 | Change U9J.P1 from PCH_GPIO76 to DDI2_HDMI_HPD | 10/02 | SIV |
| 2 | EMI recommend | 26 | Change D5, D6 from SC300001G00 to SC300001J00<br>Change D5, D6 from @EMI@ to EMI@ | 10/29 | SIV |
| 3 | EMI recommend | 27 | Change RA12 from SD028000080 to SM01000DF00<br>Change C254 from SE071220J80 to SE074221K80<br>Change C254 from @EMI@ to EMI@ | 10/29 | SIV |
| 4 | EMI recommend | 32 | Change D21 from SC300001G00 to SC300001J00 | 10/29 | SIV |
| 5 | HW design | 07 | Change C20 to @<br>Remove R201 | 11/06 | SIV |
| 6 | HW design | 11 | Change C41, C45 to @ | 11/06 | SIV |
| 7 | HW design | 15 | Change C97,C119,C113,C115,C116 to @<br>Change C93,C94,C96,C98,C99,C100 to @ | 11/06 | SIV |
| 8 | HW design | 16 | Change C124,C126,C127,C128,C129,C131 to @<br>Change C149,C143,C144,C147 to @ | 11/06 | SIV |
| 9 | HW design | 17 | Change CV9 to @DIS@ | 11/06 | SIV |
| 10 | HW design | 25 | Change C214 to @<br>Remove R722,R721 | 11/06 | SIV |
| 11 | Vendor recommend | 34 | Change CL29 form 15p to 12p | 11/06 | SIV |
| 12 | HW design | 06 | Change R17,R21 to short pad | 11/07 | SIV |
| 13 | HW design | 07 | Change R24,R25,R26,R27 to RP31<br>Change R31,R33,R32,R55 to RP32 | 11/07 | SIV |
| 14 | HW design | 15 | Change R101,R102 to short pad | 11/07 | SIV |
| 15 | HW design | 16 | Change R111,R112 to short pad | 11/07 | SIV |
| 16 | HW design | 18 | Remove RV17<br>Move GPU_GPIO1 to RP19.7 | 11/07 | SIV |
| 17 | HW design | 25 | Add PCH_GPIO87 to JEDP1.7 | 11/07 | SIV |
| 18 | HW design | 27 | Change R156 to short pad | 11/07 | SIV |
| 19 | EMI recommend | 27 | Add RA13 for EMI@<br>Add CA12 for @EMI@ | 11/07 | SIV |
| 20 | HW design | 29 | Change R217,R218,R257,R222,R199,R226 to short pad | 11/07 | SIV |
| 21 | HW design | 30 | Change R273,R274,R268 to short pad<br>Remove R266,R276,R214,R272<br>Move USB_CHG_EN#, USB_EN#, FAN_SPEED2, FAN_SPEED1 to RP33 | 11/07 | SIV |
| 22 | HW design | 31 | Change R243 to short pad | 11/07 | SIV |
| 23 | HW design | 33 | Change R253 to short pad | 11/07 | SIV |
| 24 | HW design | 35 | Change R630 to short pad | 11/07 | SIV |
| 25 | EMI recommend | 28 | Add C323,C326,C327,C328,C329,C330,C331,C332 for @EMI@ | 11/07 | SIV |
| 26 | HW design | 32 | Add R249,R250 | 11/10 | SIV |

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| Item | Reason for change | PG# | Modify List | Date | Phase |
|---|---|---|---|---|---|
| 27 | HW design | 09 | Change PCH_GPIO85 to PCH_USB_EN# | 11/10 | SIV |
| 28 | HW design | 18 | Add RV13 for THM_ALERT# | 11/10 | SIV |
| 29 | ME recommend | 28 | Change JHDMI1 footprint to SINGA_2HE1638-012212F_19P-T | 11/10 | SIV |
| 30 | HW design | 12 | Change C59,C62,C66,C70,C75 from SE000000000 to SE00000PL00<br>Add C37,C138,C333@,C334,C335 SE00000PL00 | 11/10 | SIV |
| 31 | HW design | 07 | RP31.1 & RP31.3 swap RP31.2 & RP31.4 swap => modify RP31 symbol<br>RP32.1 & RP32.2 swap RP32.3 & RP32.4 swap | 11/10 | SIV |
| 32 | EMI recommend | 27 | Add CA13 close to UA1 | 11/11 | SIV |
| 33 | HW design | 30<br>32 | Change USB_CHG_EN# to USB_CHG_EN | 11/11 | SIV |
| 34 | HW design | 09 | Remove DGPU_PWR_EN, DGPU_HOLD_RST#<br>Change PCH_GPIO18 from RP10.5 to RP5.8<br>Change PCH_GPIO23 from RP10.6 to RP28.5<br>Remove RP10 | 11/12 | SIV |
| 35 | HW design | 25 | Remove JP5 | 11/15 | SIV |
| 36 | Busyer suggestion | 19 | Change QV5 from SB000007H10 to SB00000QP00 | 11/15 | SIV |
| 37 | Busyer suggestion | 21 | Change LV6, LV7 from SM01000BZ00 to SM01000FF00 | 11/15 | SIV |
| 38 | Busyer suggestion | 30 | Change L13,L14 from SM010016810 to SM01000LP00 | 11/15 | SIV |
| 39 | HW design | 32 | swap D21 (Pin1=>Pin9, Pin3=>Pin1, Pin7=>Pin3, Pin9=>Pin7) | 11/18 | SIV |
| 40 | EMI recommend | 26 | Change TS1 from SP050006F00 to SP050006800 | 11/20 | SIV |
| 41 | EMI recommend | 25 | Change CA12 from 2.2u to 220P | 12/02 | SIV |
| 42 | EMI recommend | 27 | Change RA3 from 45.1 to 10.6<br>Change CA13 from 2.2u to 220P | 12/02 | SIV |
| 43 | EMI recommend | 28 | Change C323,C326,C327,C328,C329,C330,C331,C332 from 0.1u to 2.2P | 12/02 | SIV |
| 44 | EMI recommend | 32 | Change D16, D17 from ESD@ to @ESD@ | 12/02 | SIV |
| 45 | EMI recommend | 33 | Change D19 from ESD@ to @ESD@<br>Change D20 from @ESD@ to ESD@ | 12/02 | SIV |

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# Version change list (P.I.R. List)



| Item | Reason for change | PG# | Modify List | Date | Phase |
|---|---|---|---|---|---|
| 1 | HW design | 33 | Add R266(@) 100K pull-high to +3VLP for NOVO# | 12/05 | SIT |
| 2 | HW design | 29 | Add NET: DEW1_TI / DEW2_TI | 12/09 | SIT |
| 3 | HW design | 09 | Add R276 10K pull-high to +3VS for DGPU_PWR_EN | 12/19 | SIT |
| 4 | Vendor recommend | 29 | Change R186, R193 from @ to TI@ | 12/20 | SIT |
| 5 | HW design | 25 | Change +12VS_Panel to B+<br>Add JP5<br>Delete R215, R504, R148 for RP10<br>Add RP10<br>Change R213 to short pad | 12/20 | SIT |
| 6 | HW design | 30 | Change R267 to @<br>Change net name from USB_EN# to USB1_EN#<br>Add USB2_EN# to U26.89<br>Add R277 (10K) pull-high +5VALW<br>Change R270 to short pad | 12/20 | SIT |
| 7 | HW design | 32 | Change net name from USB_EN# to USB1_EN# by U29.4<br>Change net name from USB_EN# to USB2_EN# by U30.4<br>Delete R249, R250 | 12/20 | SIT |
| 8 | HW design | 09 | Change PCH_USB_EN# to PCH_GPIO85<br>Delete R252,R262 | 12/20 | SIT |
| 9 | HW design | 08 | Delete R206 for RP10<br>Change R46,R51,R53 to short pad | 12/20 | SIT |
| 10 | HW design | 07 | Change R34, R35, R39, R40 to short pad | 12/20 | SIT |
| 37 | HW design | 11 | Change R79 to short pad | 12/20 | SIT |
| 38 | HW design | 15 | Change R88, R98 to short pad | 12/20 | SIT |
| 39 | HW design | 16 | Change R104 to short pad | 12/20 | SIT |
| 40 | HW design | 18 | Change RV44,RV32 to short pad | 12/20 | SIT |
| 41 | HW design | 19 | Change RV45 to short pad | 12/20 | SIT |
| 42 | HW design | 20 | Change RV46, RV50, RV52, RV55, RV57, RV51 to short pad | 12/20 | SIT |
| 43 | HW design | 28 | Delete Q5, Q7<br>Add Q5A, Q5B | 12/20 | SIT |
| 44 | EMI recommend | 32 | Change C306, C307 from 0.1u to100P | 12/20 | SIT |
| 45 | HW design | 33 | Change R230 from 300 ohm to 649 ohm | 12/23 | SIT |
| 46 | Busyer suggestion | 21 | (X1 code) Change LV10, LV13 from SM01000BL00 to SM01000GG00 | 12/23 | SIT |
| 47 | Busyer suggestion | 08 | (X1 code) Change U11 from SA00006QR00 to SA741080400 | 12/23 | SIT |
| 48 | Busyer suggestion | 25 | (X1 code) Change U33 from SA00006QR00 to SA741080400 | 12/23 | SIT |
| 49 | Busyer suggestion | 30 | (X1 code) Change U27 from SA00006QR00 to SA741080400 | 12/24 | SIT |
| 50 | EMI recommend | 27 | Change RA12 from 120 ohm(SM01000DF00) to 300 ohm (SM01000I000) | 12/24 | SIT |
| 51 | HW design | 27 | Change RA2, RA10 to short pad | 12/24 | SIT |
| 52 | EMI recommend | 30 | Change C286, C287, C289, C291 from @ to EMI@ | 12/24 | SIT |
| 53 | HW design | 30 | Change R260, R223 to short pad | 12/24 | SIT |
| 54 | HW design | 31 | Change R228, R229 to short pad | 12/24 | SIT |
| 55 | HW design | 19 | Change R260, R223 to short pad | 12/25 | SIT |
| 56 | HW design | 25 | Change L24 from EMI@ to @EMI@ | 12/25 | SIT |

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# Version change list (P.I.R. List)



| Item | Reason for change | PG# | Modify List | Date | Phase |
|---|---|---|---|---|---|
| 57 | HW design | 29 | Change R275 to @ | 12/27 | SIT |
| 58 | HW design | 28 | Change C323, C326, C327, C328, C329, C330, C331, C332 from @EMI@ to EMI@ | 12/27 | SIT |
| 59 | HW design | 31 | Change R230 from 649 ohm 5% to 649 ohm 1%. | 12/31 | SIT |
| 60 | Vendor recommend | 21 | Change LV10, LV13 from SM01000GG00 to SM01000I300. | 01/03 | SIT |
| 61 | HW design | 12 | Change C59, C138, C66, C334, C75 from 47uF to 22uF | 01/07 | SIT |
| 62 | HW design | 15 | Change C89, R90, C107, R100 to @ | 01/07 | SIT |
| 63 | HW design | 16 | Change C120, R106 to @ | 01/07 | SIT |
| 64<br>65<br>66 | HW design | 25 | Change R1456 to short pad<br>Change C225, C226 to @<br>Change L6 from SM010014520 to SD002000080 (0 ohm) and change location to R2 | 01/07 | SIT |
| 67 | HW design | 31 | Change C300, C303 to @ | 01/07 | SIT |
| 68 | HW design | 33 | Change R256 to short pad | 01/07 | SIT |
| 69 | HW design | 12 | Change C37, C62, C70, C335 to @ | 01/03 | SIT |
| 1 | HW design | 25 | Change location L6 to R2 | 01/12 | SVT |
| 2 | HW design | 19 | Change location C989 to R830 | 01/12 | SVT |
| 3 | EMI recommend | 28 | Change C327, C328, C329, C330, C331, C332, C323, C326 from EMI@ to @EMI@ | 01/14 | SVT |
| 4 | HW design | 27 | Add U1(LDO), C344, C343 | 01/20 | SVT |
| 5 | DFx recommend | 32 | Add C345, C346 | 01/22 | SVT |
| 6 | Busyer suggestion | 21 | Change LV10, LV13 from SM01000I300 to SM01000F100 | 01/22 | SVT |
| 7 | HW design | 27 | Add R249, R250<br>Change C253 from 1uF_0402 tp 1uF_0603 | 01/22 | SVT |
| 8 | HW design | 06 | Change RG3 to short pad | 01/22 | SVT |
| 9 | HW design | 07 | Change RG9, R38 to short pad | 01/22 | SVT |
| 10 | HW design | 25 | Change R2 to short pad | 01/22 | SVT |
| 11 | HW design | 18 | Change RV187 to short pad | 01/22 | SVT |
| 12 | HW design | 29 | Change R185 to short pad | 01/22 | SVT |
| 13 | HW design | 27 | Change R155, R157, R158 to short pad | 01/22 | SVT |
| 14 | HW design | 26 | Change RG6 to short pad | 01/22 | SVT |
| 15 | HW design | 30 | Change R225 to short pad | 01/22 | SVT |
| 16 | HW design | 18 | Change RV25 from 100K to 1K | 02/10 | SVT |
| 17 | HW design | 28 | Change RP21, PR22 from 680 ohm to 470 ohm | 02/12 | SVT |
| 18 | HW design | 25 | Add R148 | 02/19 | SVT |
| 19 | HW design | 30 | Delete net: BATT_LEN# | 02/20 | SVT |
| 20 | HW design | 19 | Change R829 from 470 ohm to 10 ohm | 02/21 | SVT |
| 21 | HW design | 18 | Change RV187 from short pad to 0 ohm | 02/21 | SVT |
| 22 | EMI recommend | 27 | Change R164, R165, R166, R167 from 0 ohm to short pad<br>Change R196, R197, R198, R173 from 0 ohm to short pad | 02/21 | SVT |
| 23 | Busyer suggestion | 19 | Change Q139 from SB000003W00 to SB00000ZN00 | 02/21 | SVT |
| 24 | Vendor recommend | 34 | Add RG2<br>Change RG5 from 10 ohm to 0 ohm | 02/24 | SVT |
| 25 | DFx recommend | 32 | Change C346@ to C346 | 02/26 | SVT |

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