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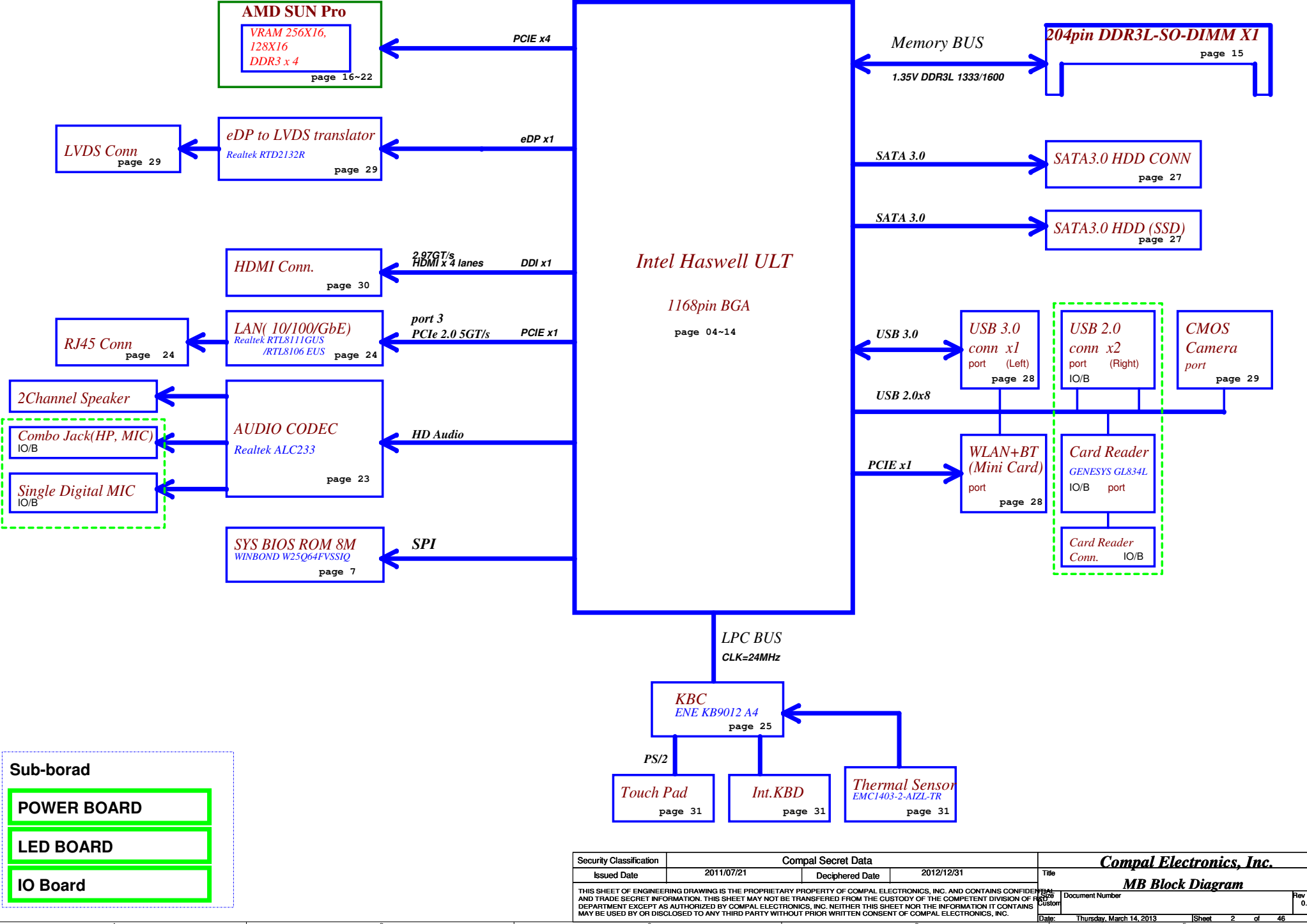
Model Name : ZIUS6/S7
File Name : LA-A321PR01
BOM P/N:4319OP38L5x -- ZIUS7
4319OP38L0x -- ZIUS6

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ZIUS6/S7 M/B Schematics Document
Intel SharyBay ULT Processor + AMD SUN Pro

2013-03-14
REV: 0.2

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Cover Page	
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Voltage Rails

power plane State	B+	+5VALW +3VALW	+1.35V	+5VS +3VS +1.5VS +1.05VS_VTT +CPU_CORE +0.675VS +VGA_CORE (PX) +0.95VS_VGA (PX) +3.3VS_VGA (PX) +1.8VS_VGA (PX) +1.5VS_VGA (PX)
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S0#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	0.2
3	0.1
4	
5	
6	
7	

BOM Structure Table

BTO Item	BOM Structure
Connector	ME@
45 LEVEL	45@
Unpop	@
CPU OPTION	CPU1@
INTEL UMA	UMA@
AMD SUN Pro	PX@
VRAM Option	S1G@ M1G@ H1G@ S2G@ M2G@
LAN RTL8111GUS	8111@ SWR@
LAN RTL8106EUS	8106@ SWR@
USB3.0	USB3@
EMI PART	EMI@
ESD PART	ESD@

EC SM Bus1 address

Device	Address
Smart Battery Charger	

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2-AIZL-TR Panel - eDP to LVDS translator SharkBay ULT AMD SUN Pro	1001_101xb

CPU SM Bus address

Device	Address
DDR DIMM0 WALN Touch Pad	0XA0

CPU SML0 Bus address

Device	Address
--------	---------

USB 2.0 Port Table

USB 2.0 Port	3 External USB Port
0	USB 2.0 Port (I/O Board)
1	USB 3.0/2.0 Port (MB)
2	USB 2.0 Port (I/O Board)
3	Card Reader
4	Touch Screen (reserve)
5	Camera
6	Mini Card (WLAN/BT)
7	

USB 3.0 Port Table

Port	
1	
2	USB 3.0 Port (MB)
3	
4	

PCIe Port Table

Port	Lane	
1		
2		LAN
3		WLAN
4		
5	0	
	1	
	2	GPU
	3	
6	0	
	1	
	2	
	3	

SATA Port Table

Port	
3	
2	
1	mSATA SSD
0	HDD

SMBUS Control Table

	HOST	VGA	BATT	KB9012	SODIMM	WLAN	PANEL sensor ADM1032	Thermal sensor EMC1403	VGA sensor ADM1032	CPU Sensor	Touch Pad	Security ROM	NFC
EC_SMB_CK1 EC_SMB_DA1	KB9012 +3VLP	X	+3VLP	X	X	X	X	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB9012 +3VS	+3VS	X	X	X	X	+3VS	+3VS	+3VS	+3VALW	X	X	X
SMBCLK SMBDATA	CPU +3VALW	X	X	X	+3VS	+3VS	X	X	X	X	+3VS	+3VS	+3VS
SMLCLK SML0DATA	CPU +3VALW	X	X	X	X	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	KB9012 +3VS	X	X	+3VS	X	X	X	X	X	+3VALW	X	X	X

CPU part

U1 CPU1@	U1 CPU2@	U1 CPU3@	U1 CPU4@	U1 CPU5@
I5-3317U 1.7G SA00006FY20	I3-4010U 1.7G SA00006SX20	I3-4100U 1.8G SA00006SU20	I5-4250U 1.3G SA00006NM40	I5-4200U 1.6G SA00006SM20
U1 CPU6@	U1 CPU7@			
I7-4550U 1.5G SA00006SJ30	I7-4500U 1.8G SA00006SL20			

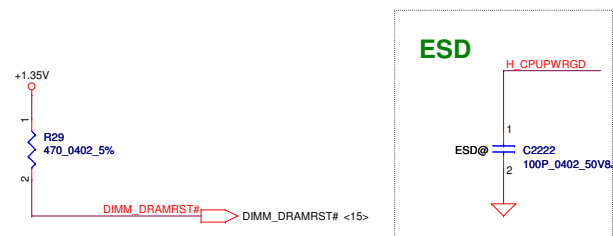
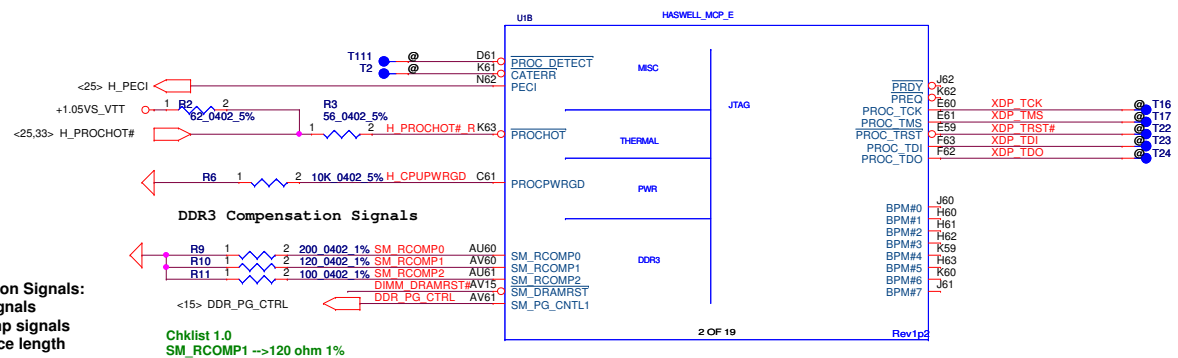
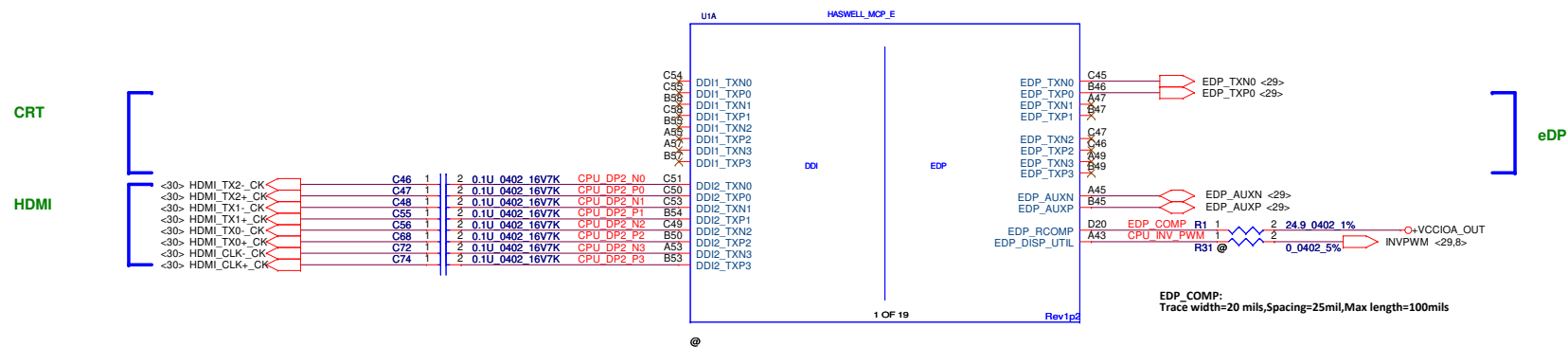
PCB part

ZZZ5
PCB OR LA-A321P REV0 M/B DA600104000

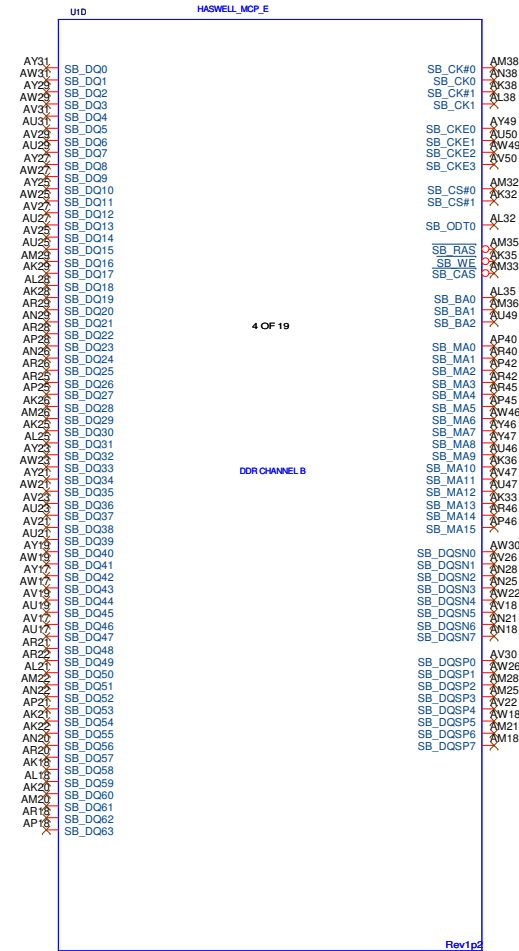
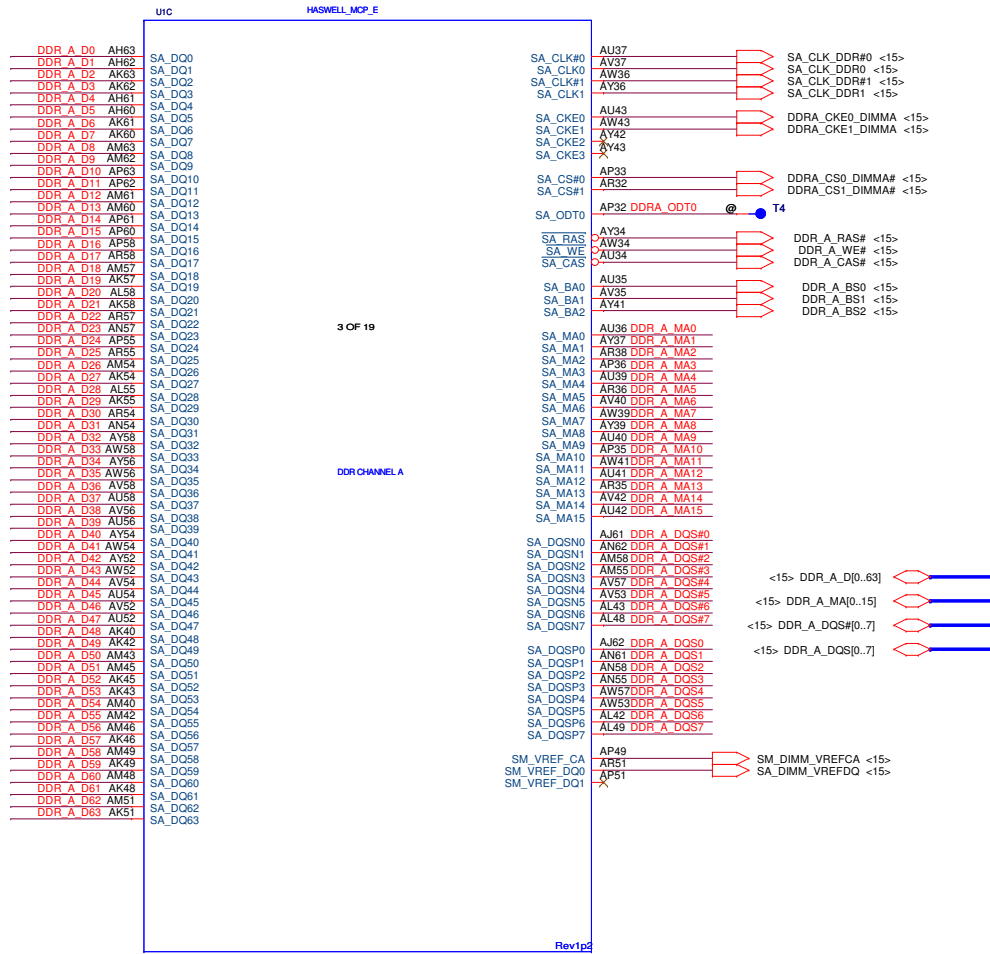
VRAM

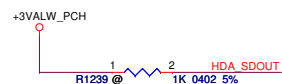
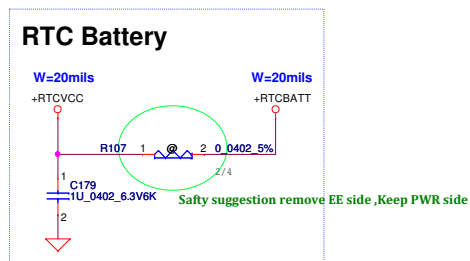
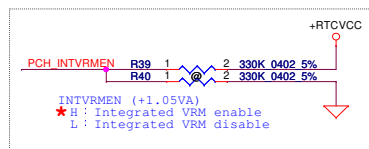
ZZZ3	ZZZ7	ZZZ6	ZZZA	ZZZ8
Samsung S2G@ X7641338L34 K4W401646B-HC11	MICRON M2G@ X7641338L35 MT41K256M168A-1070:E	Samsung S1G@ X7641338L31 K4W201646B-BC1A	MICRON M1G@ X7641338L32 MT41K256M168A-1070:E	Hynix H1G@ X7641338L33 K4W201646B-BC1A

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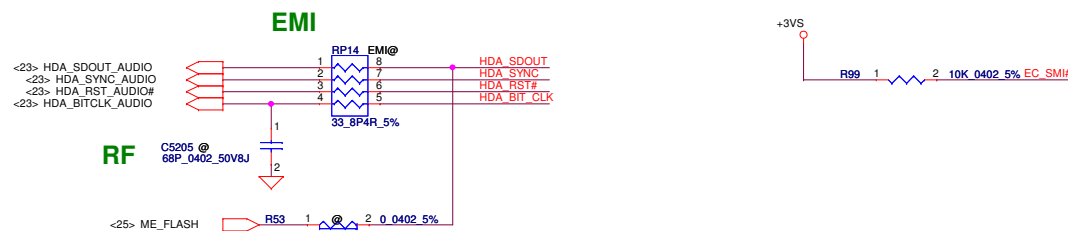
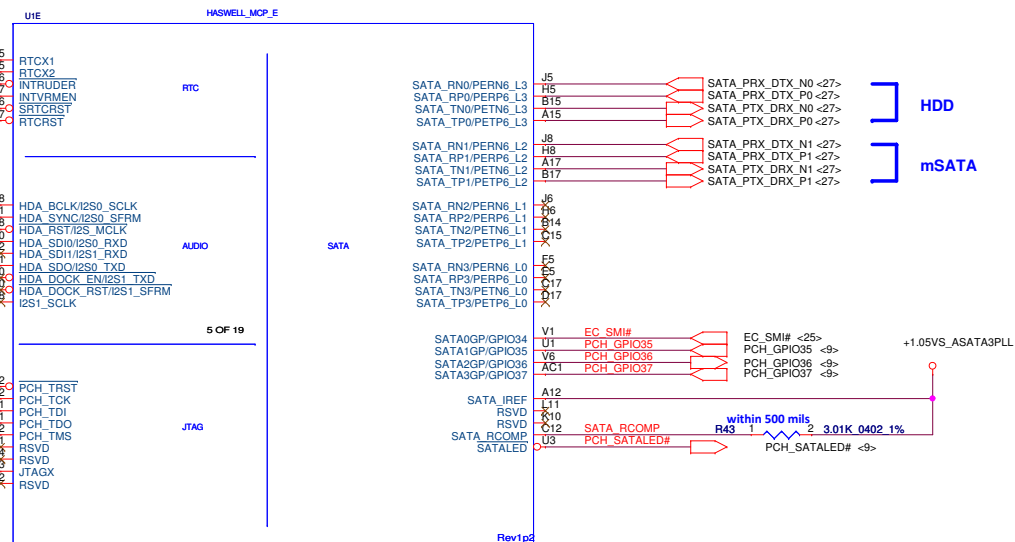
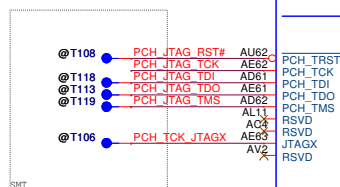
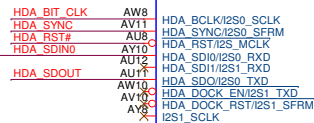
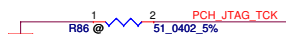


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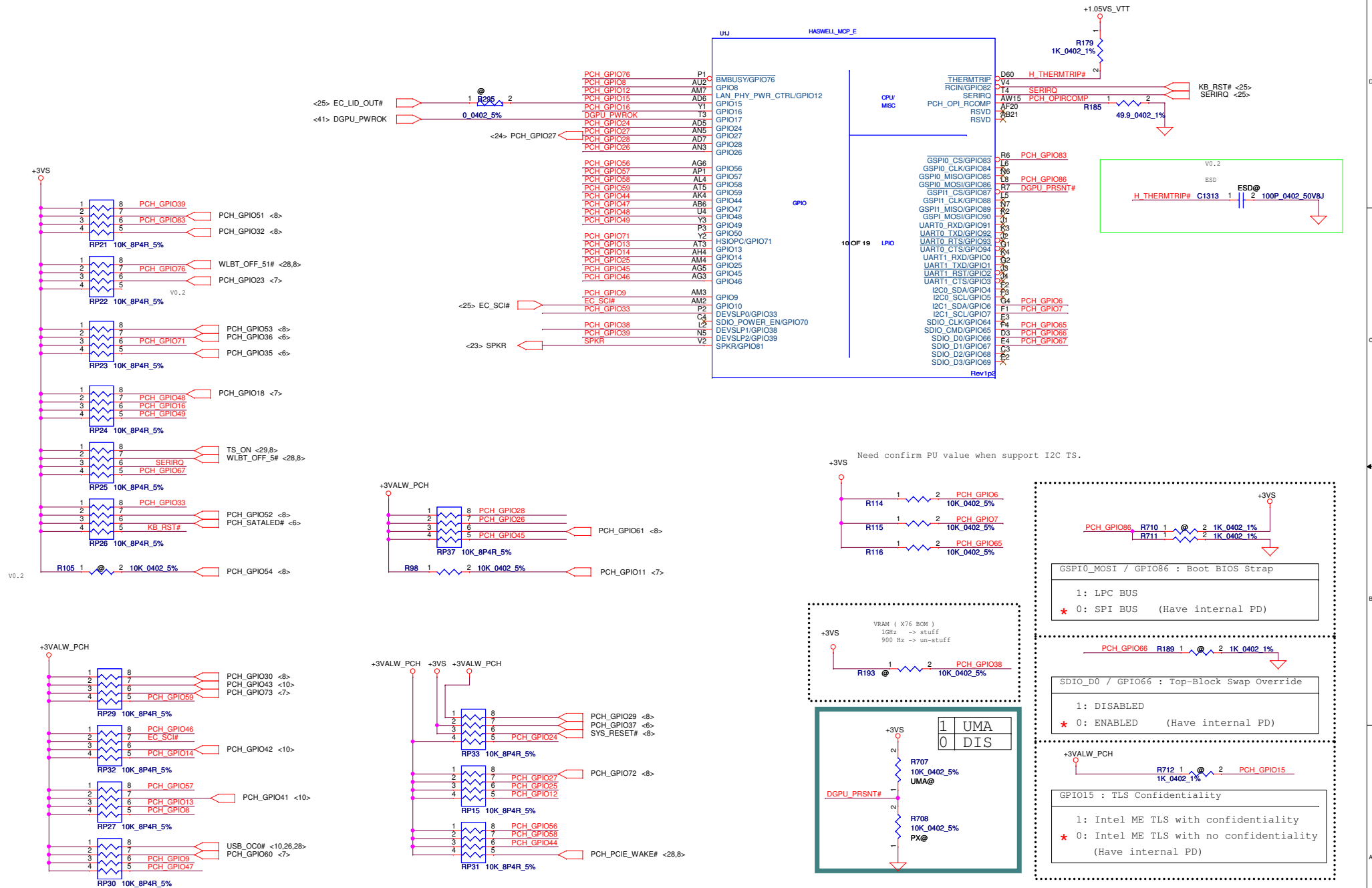


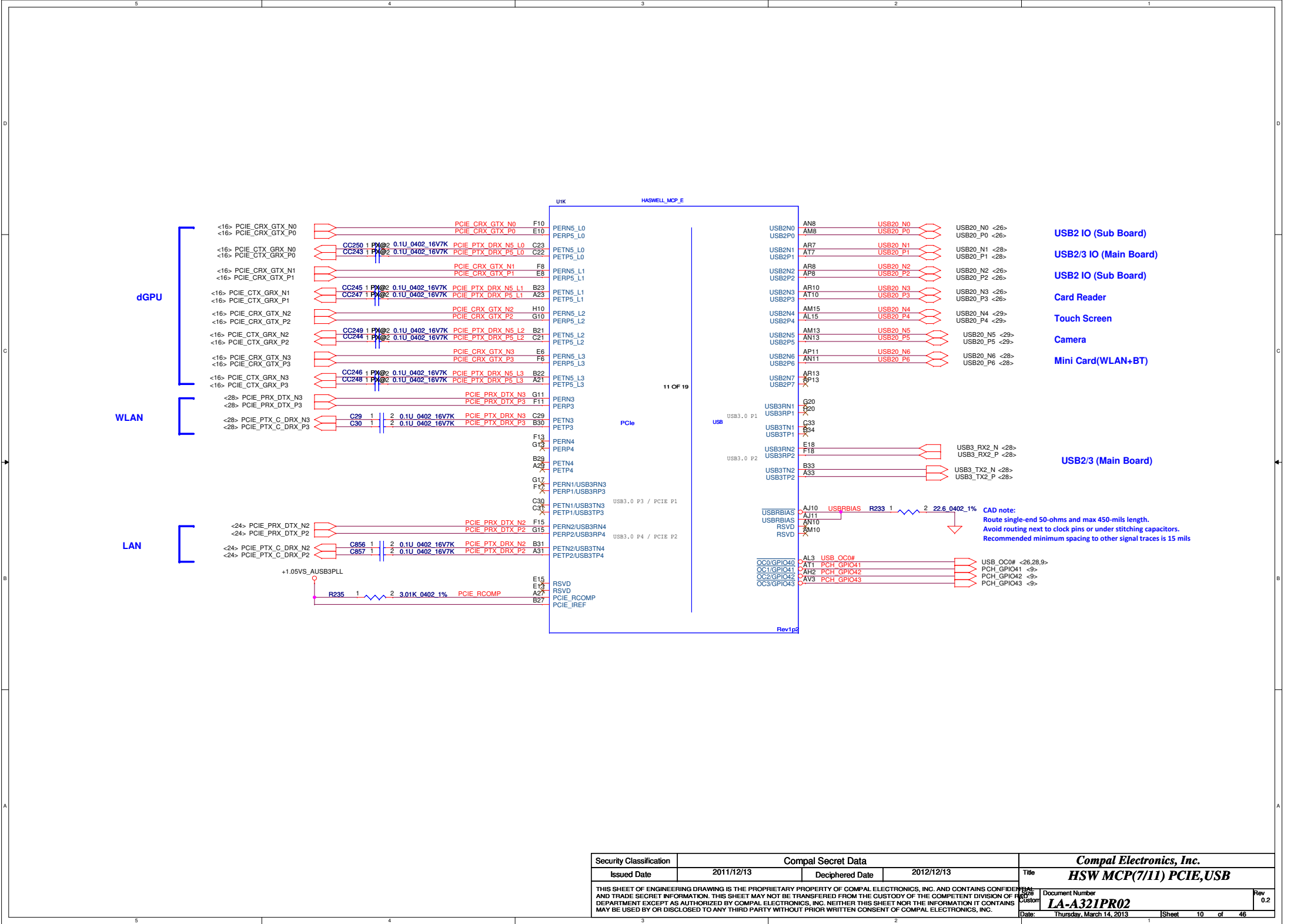
```
HDA_SDOUT
ME debug mode, this signal has a weak internal PD
* Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Override]
```

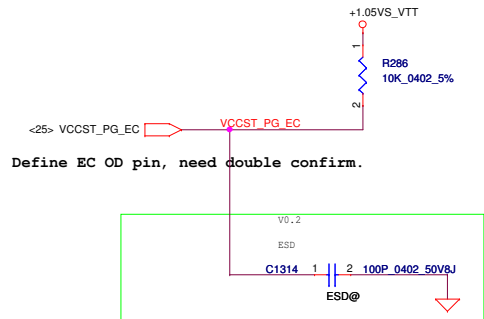


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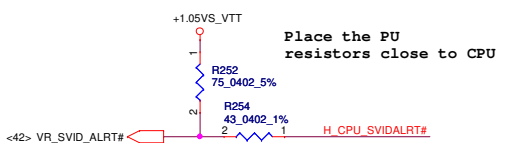
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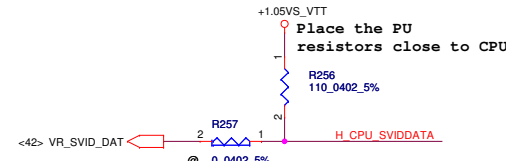




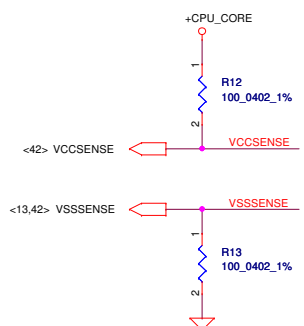
SVID ALERT



SVID DATA

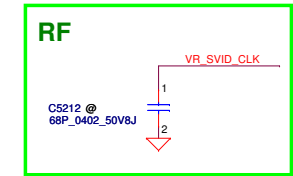


R256:
CRB r0.7 changed from 130 Ohms to 110 Ohms

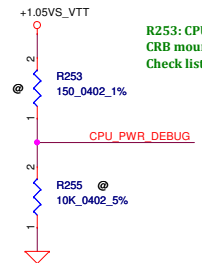


CAD Note: PU resistor should be close to CPU

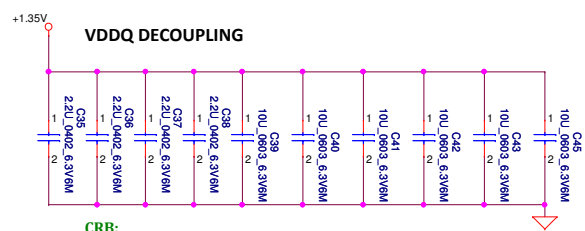
CAD Note: PD resistor should be close to CPU



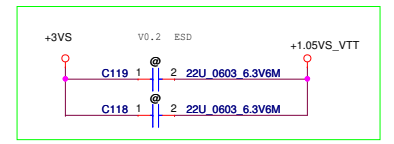
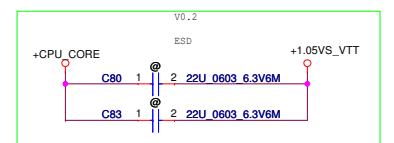
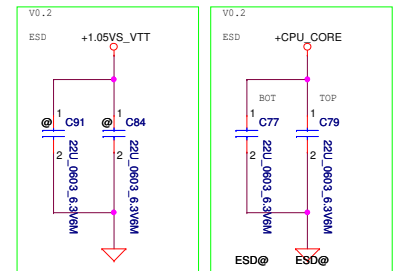
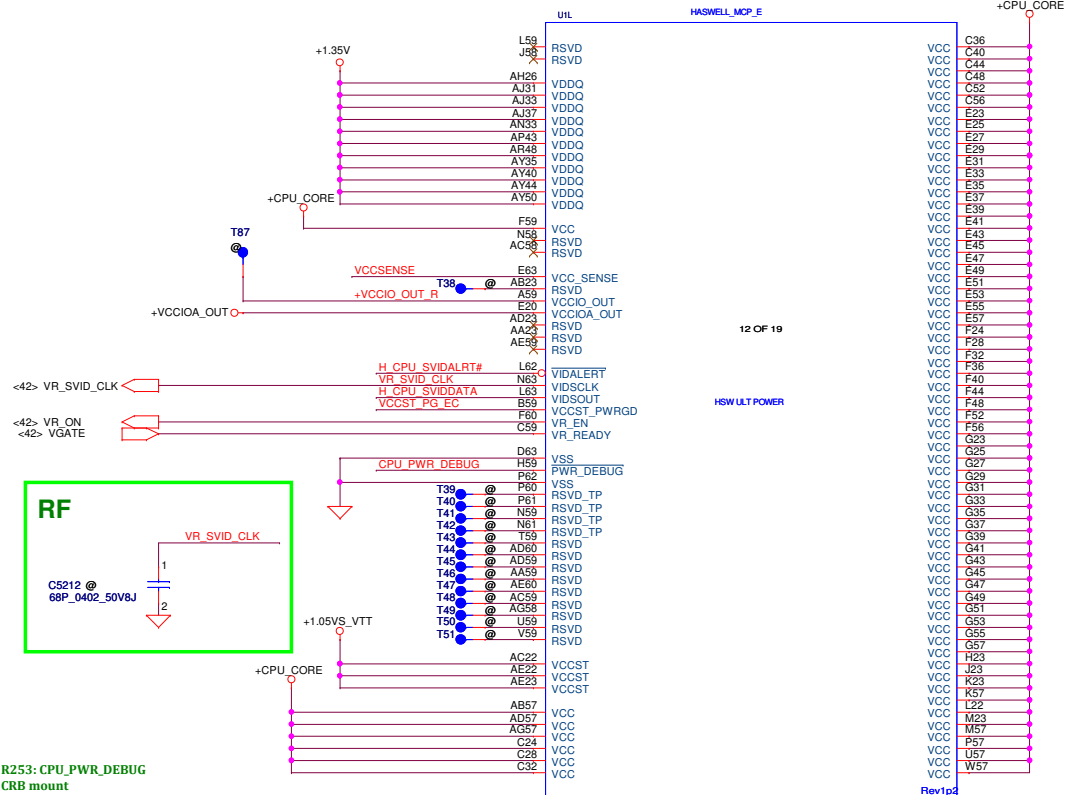
R253: CPU_PWR_DEBUG
CRB mount
Check list_XDP use only



VDDQ DECOUPLING

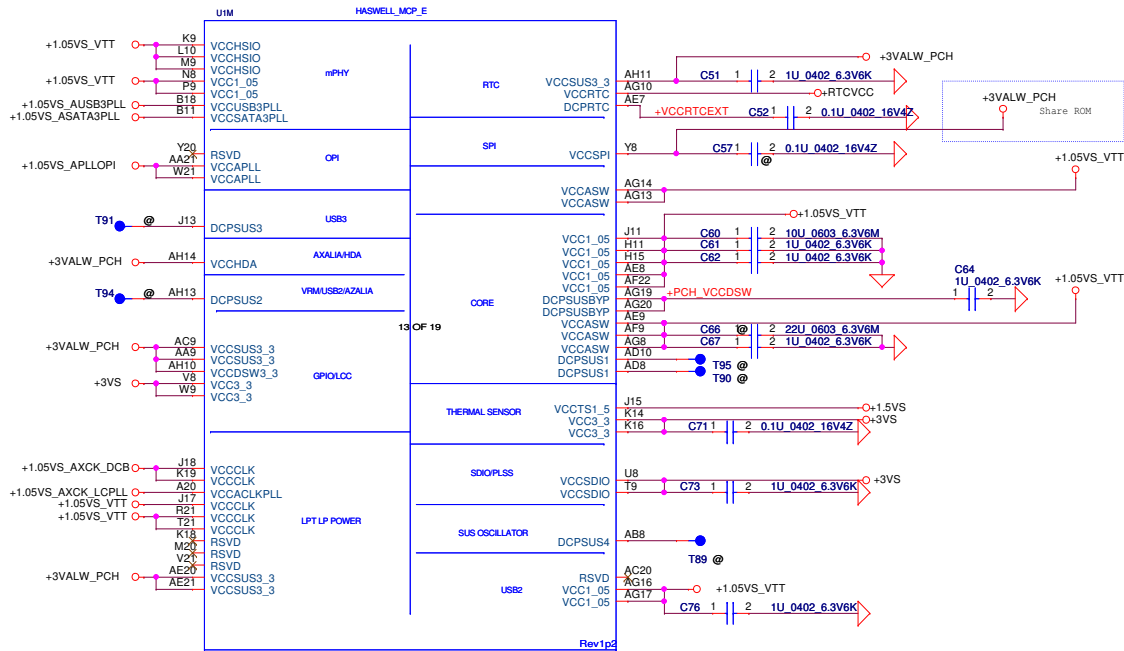
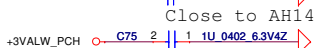
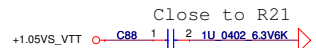
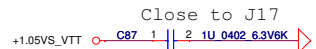
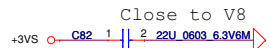
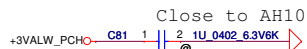
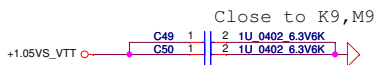
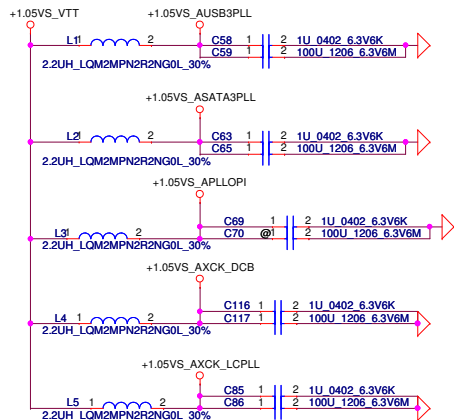


CRB:
+1.35V : 470UF/2V/7343 *2 (Un-mount)
10UF/6.3V/0603 *6
2.2UF/6.3V/0402 *4



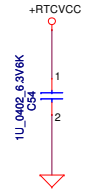
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Check Power Source Close to N8
+1.05VS_VTT C53 @ 2 1U 0402 6.3V6K

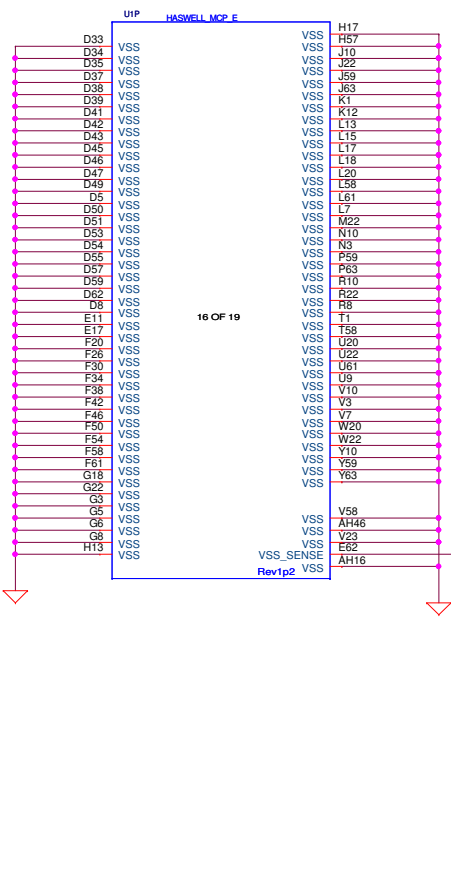
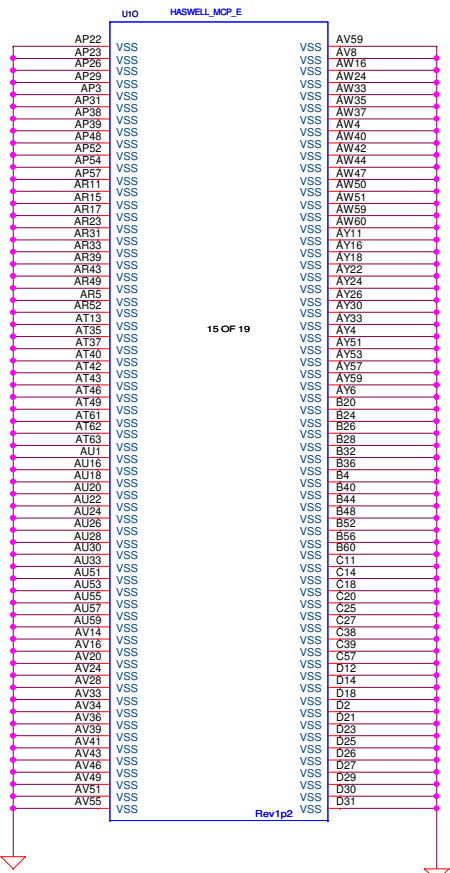
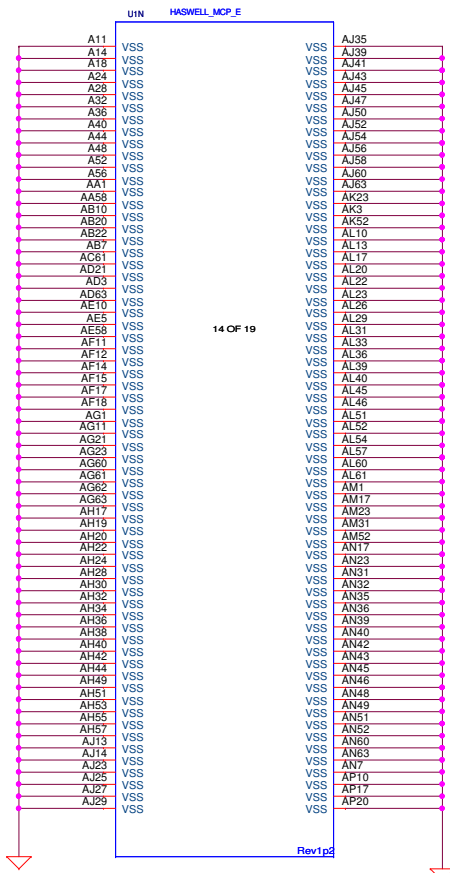


18mA

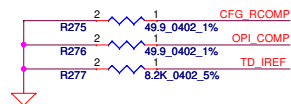
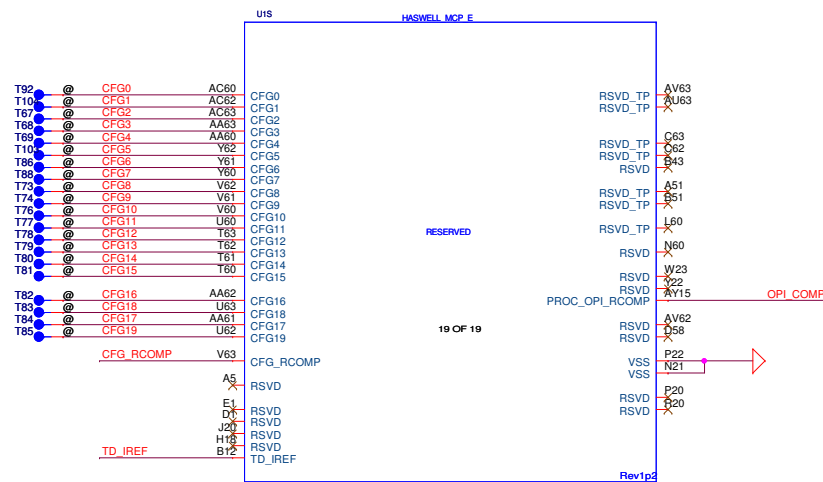
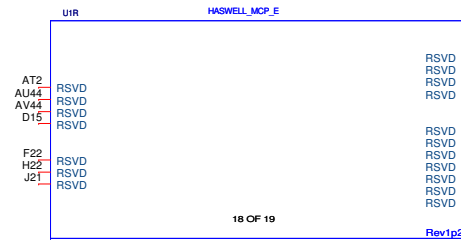
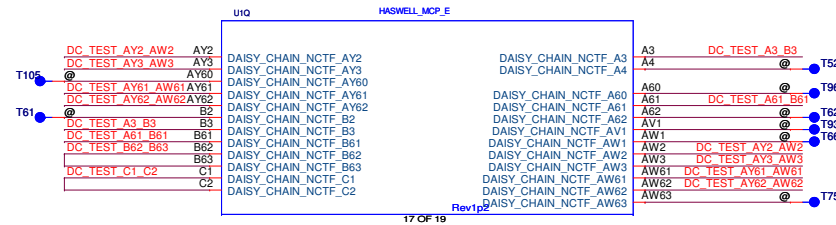
658mA



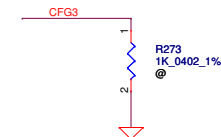
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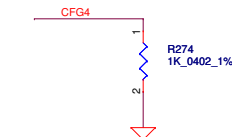
VSSSENSE <11,42>



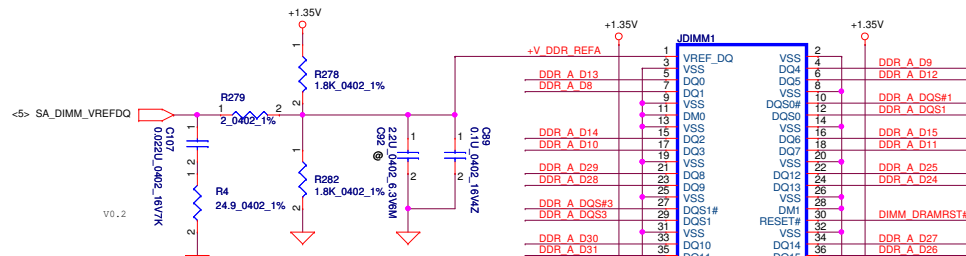
CFG Straps for Processor



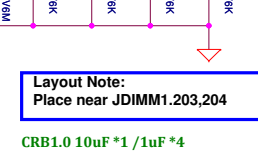
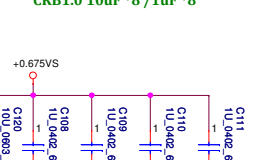
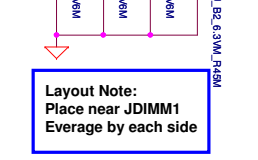
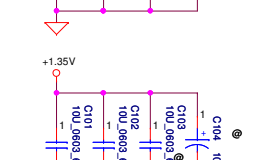
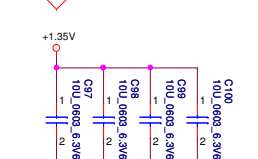
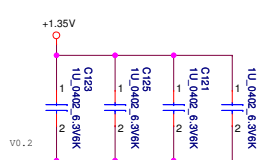
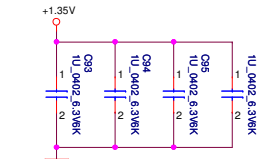
Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



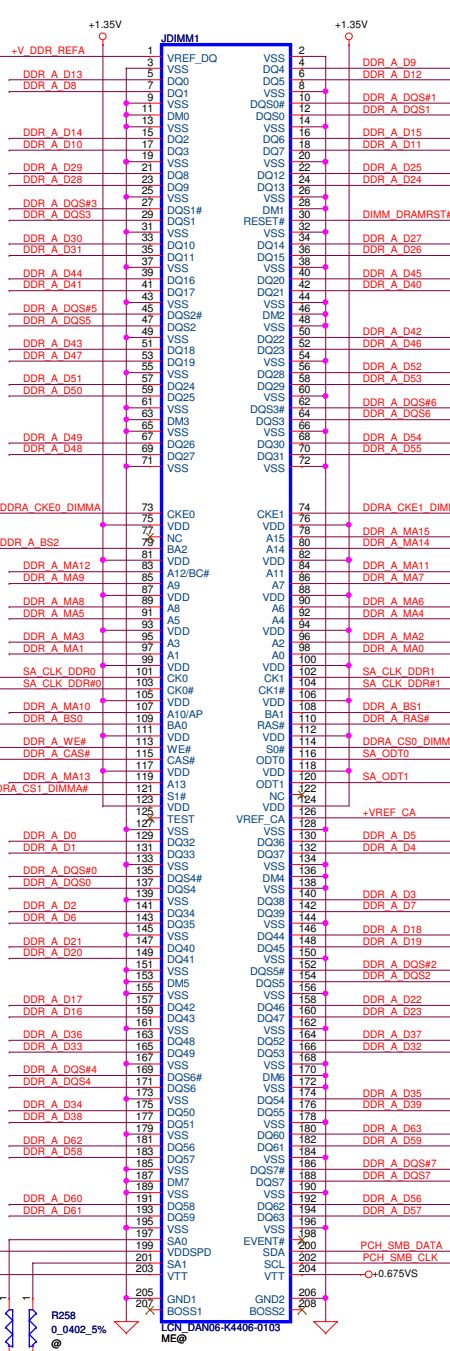
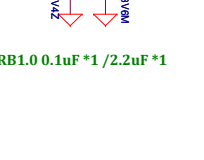
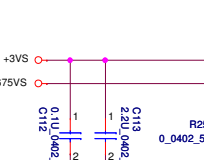
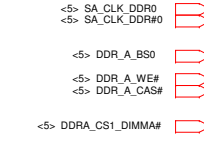
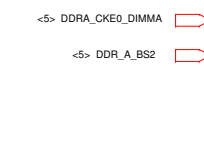
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



Follow PDG1.0

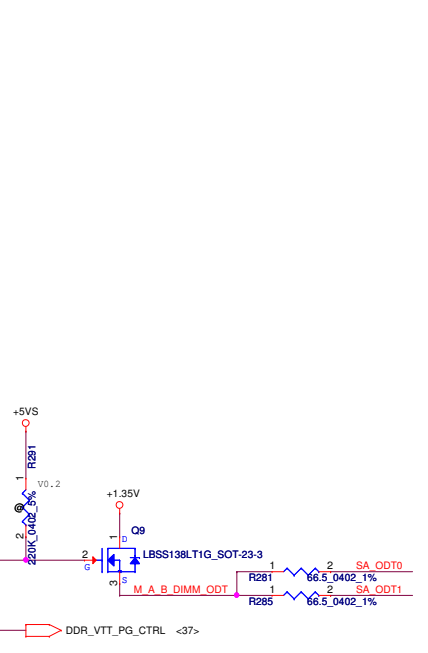
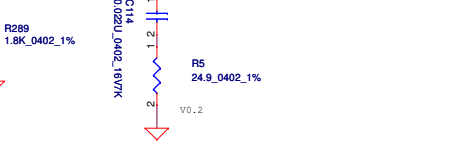
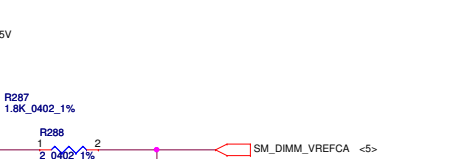
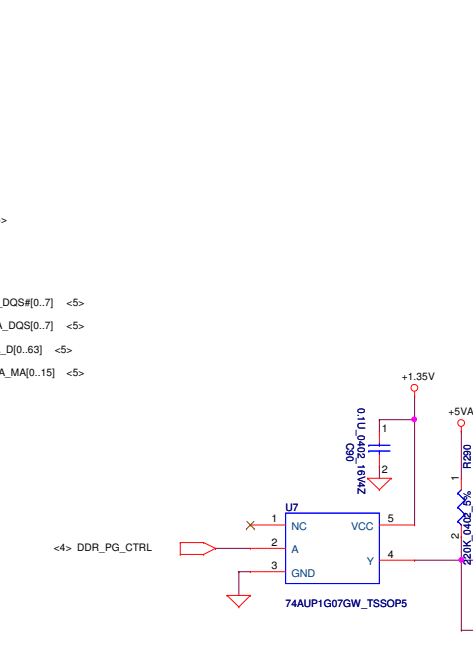
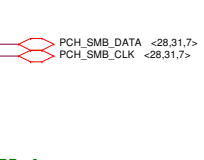


CRB1.0 0.1uF *1 / 2.2uF *1
2.2uF (reserved)



All VREF traces should have 10 mil trace width

CRB1.0 0.1uF *1 / 2.2uF *1
2.2uF (reserved)



CHANNEL A /TYPE :Reverse / H:4mm

CHA SPD ADDRESS IS 0x40

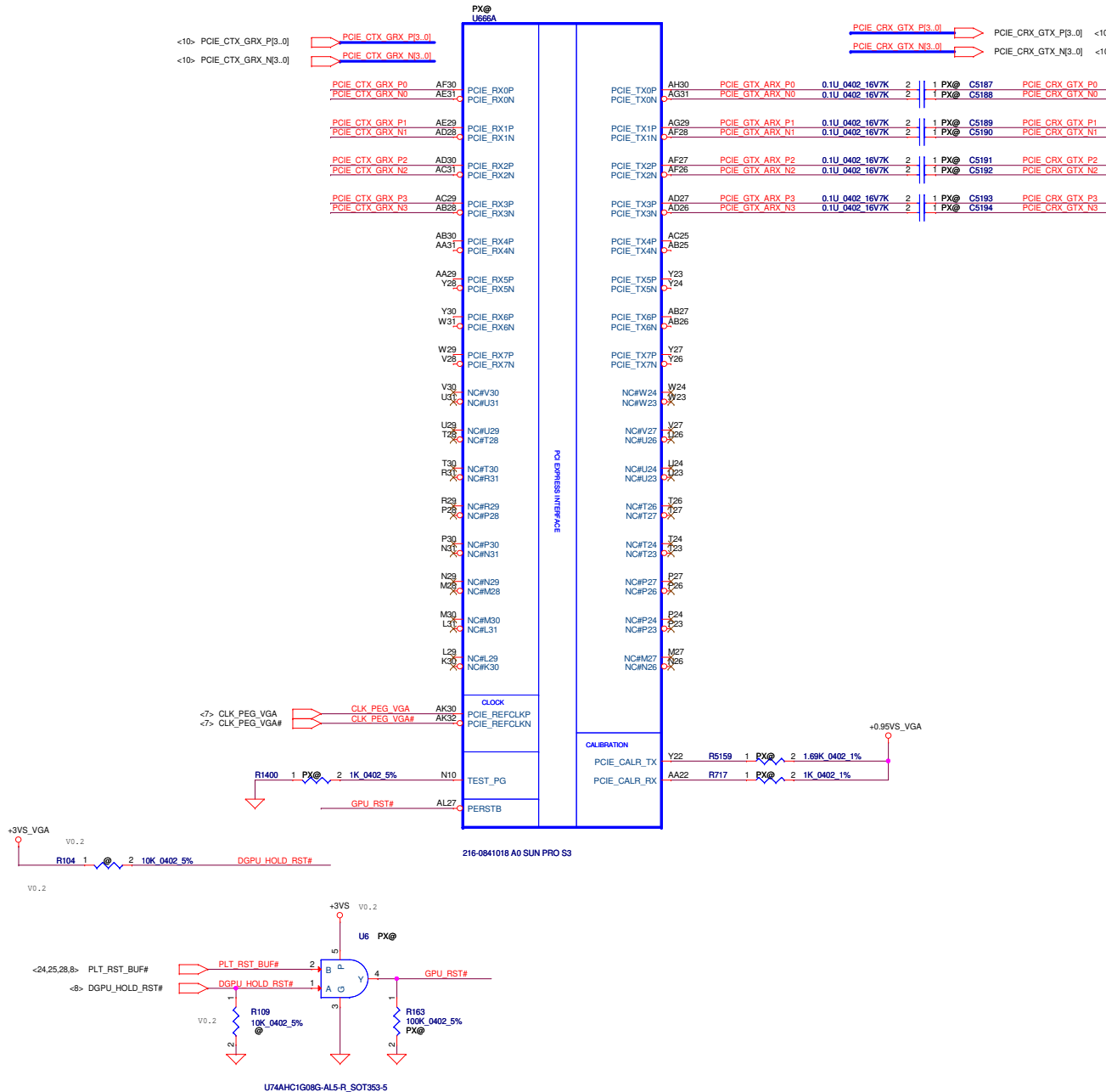
CHA TS ADDRESS IS 0x30

PN:SP07000LT00

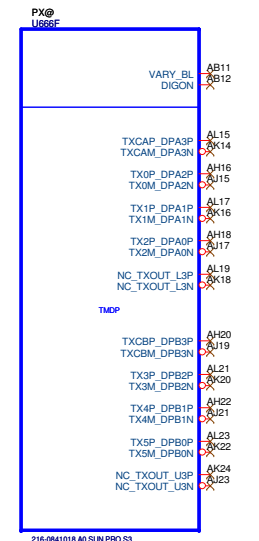
Layout Note:
Place near J1MM1.203,204

CRB1.0 10uF *1 / 1uF *4

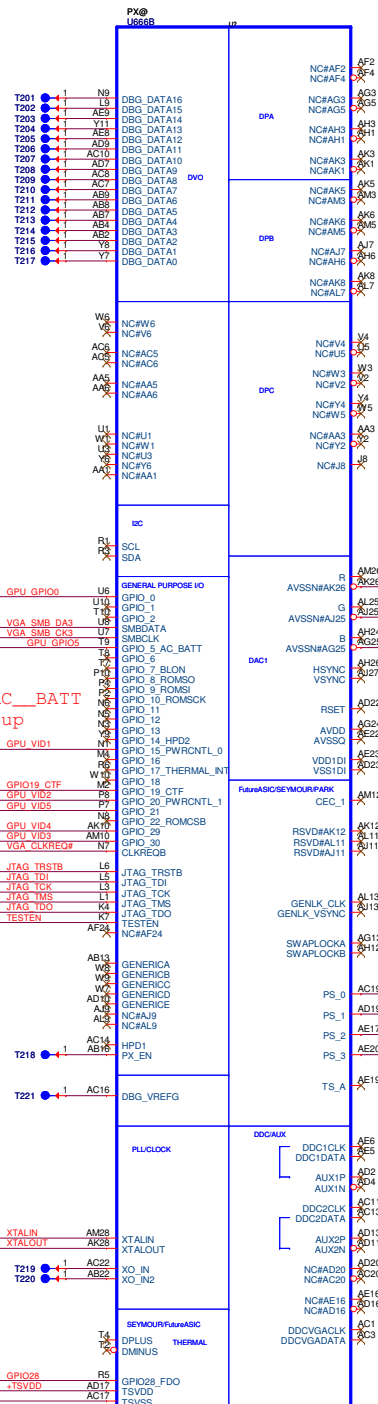
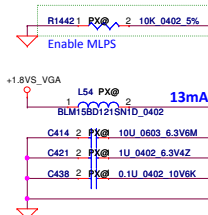
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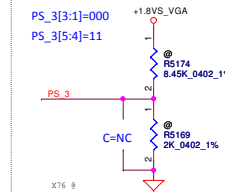
No Use GPU Display Port output



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				SUN_PCIE/DP	
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				Date: Thursday, March 14, 2013	Sheet 16 of 46



Capacitor Divider Lookup Table	
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

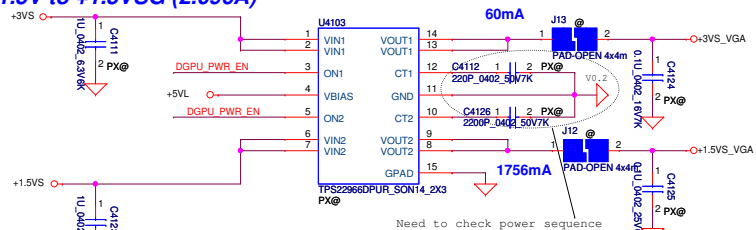


Strap Name :

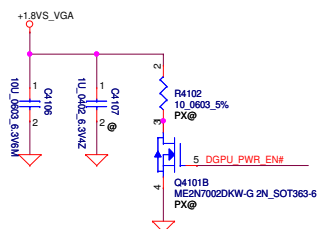
- PS_3[1] BOARD_CONFIG[0] (Memory ID)
- PS_3[2] BOARD_CONFIG[1] (Memory ID)
- PS_3[3] BOARD_CONFIG[2] (Memory ID)
- PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
- PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

Memory ID	Memory Type	Configuration	Size
000	SA000068U00	Samsung K4W2G1646E-BC1A	1GB
001	SA000067500	Micron MT41J128M16JT-093G:K	1GB
010	SA00006H400	Hynix H5TC2G63FFR-11C	1GB
011	SA000068R10	Samsung K4W4G1646B-HC11	2GB
100	SA000065D20	Micron MT41K256M16HA-107G:E	2GB

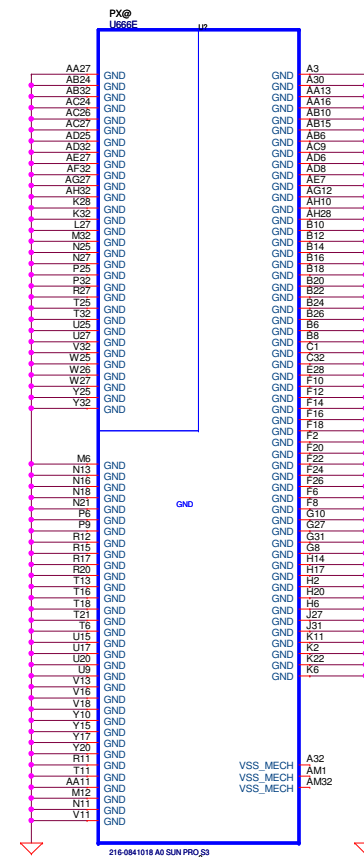
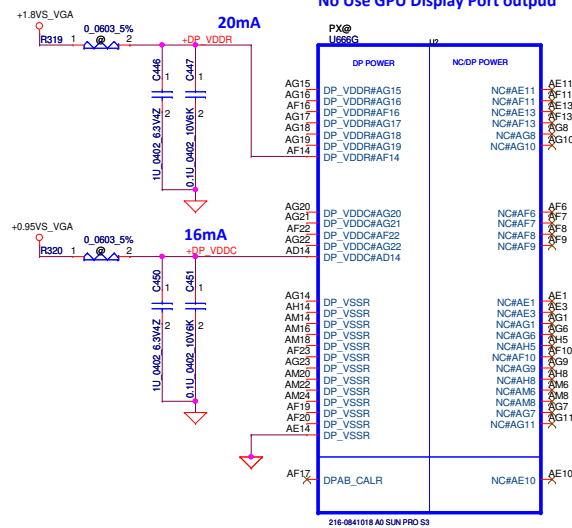
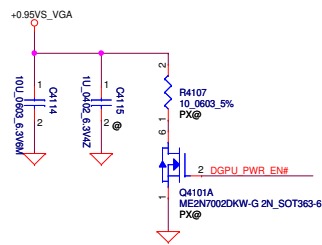
+3VS to +3VSG (60mA)
+1.5V to +1.5VSG (2.096A)



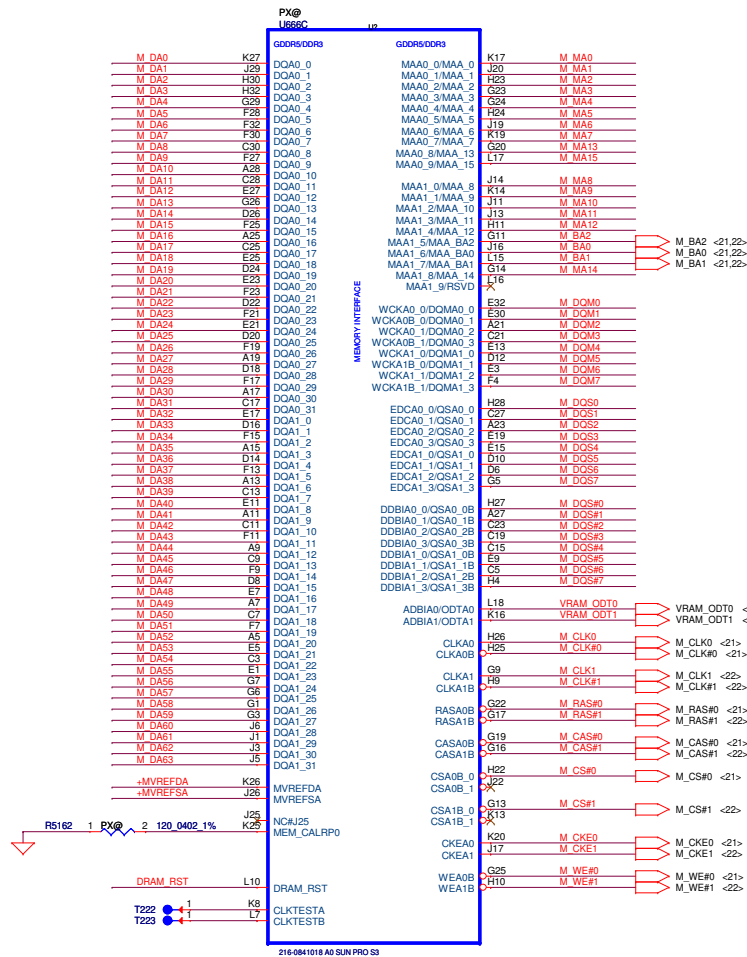
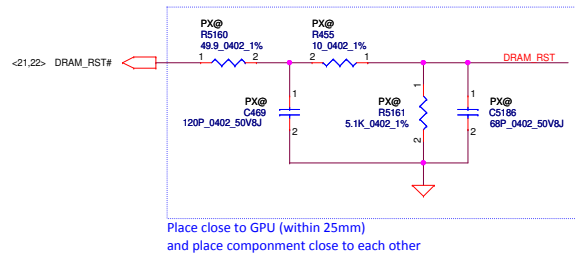
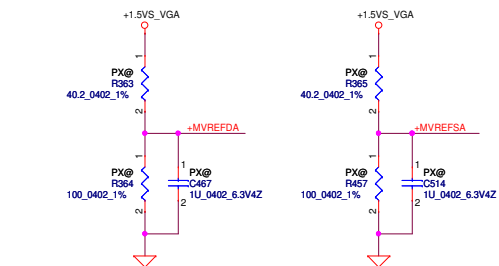
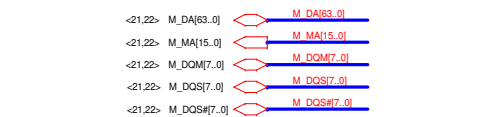
+1.8VALW to +1.8VSG (818mA)



+0.95VALW to +0.95VSG (4.016A)

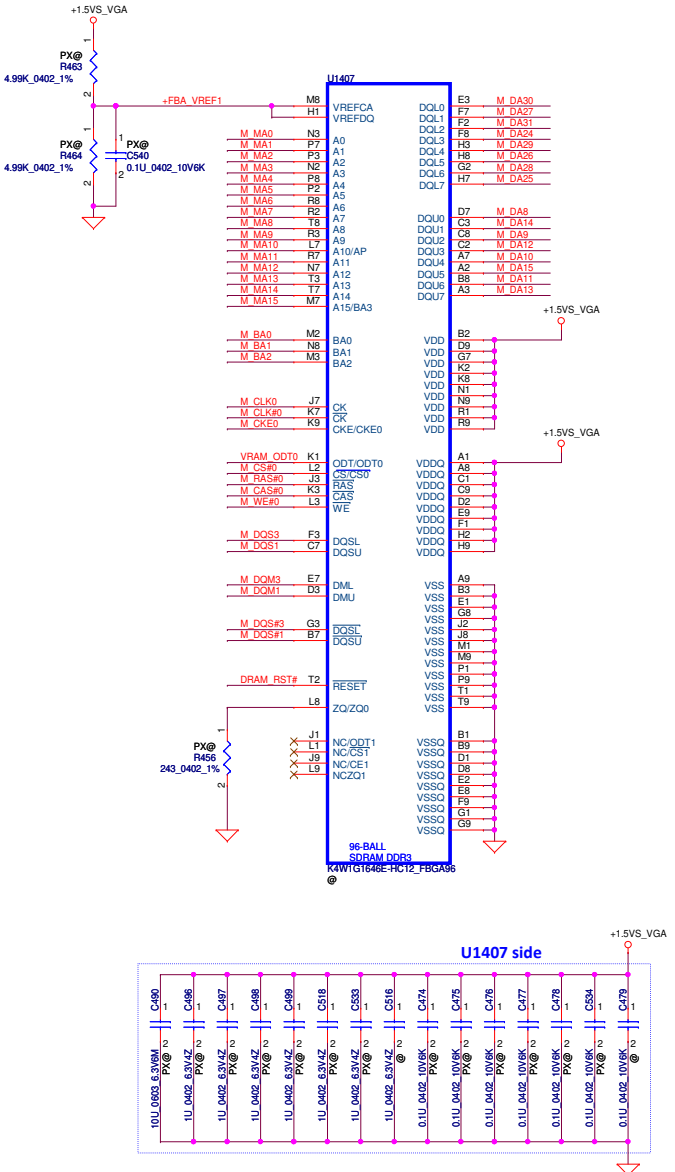
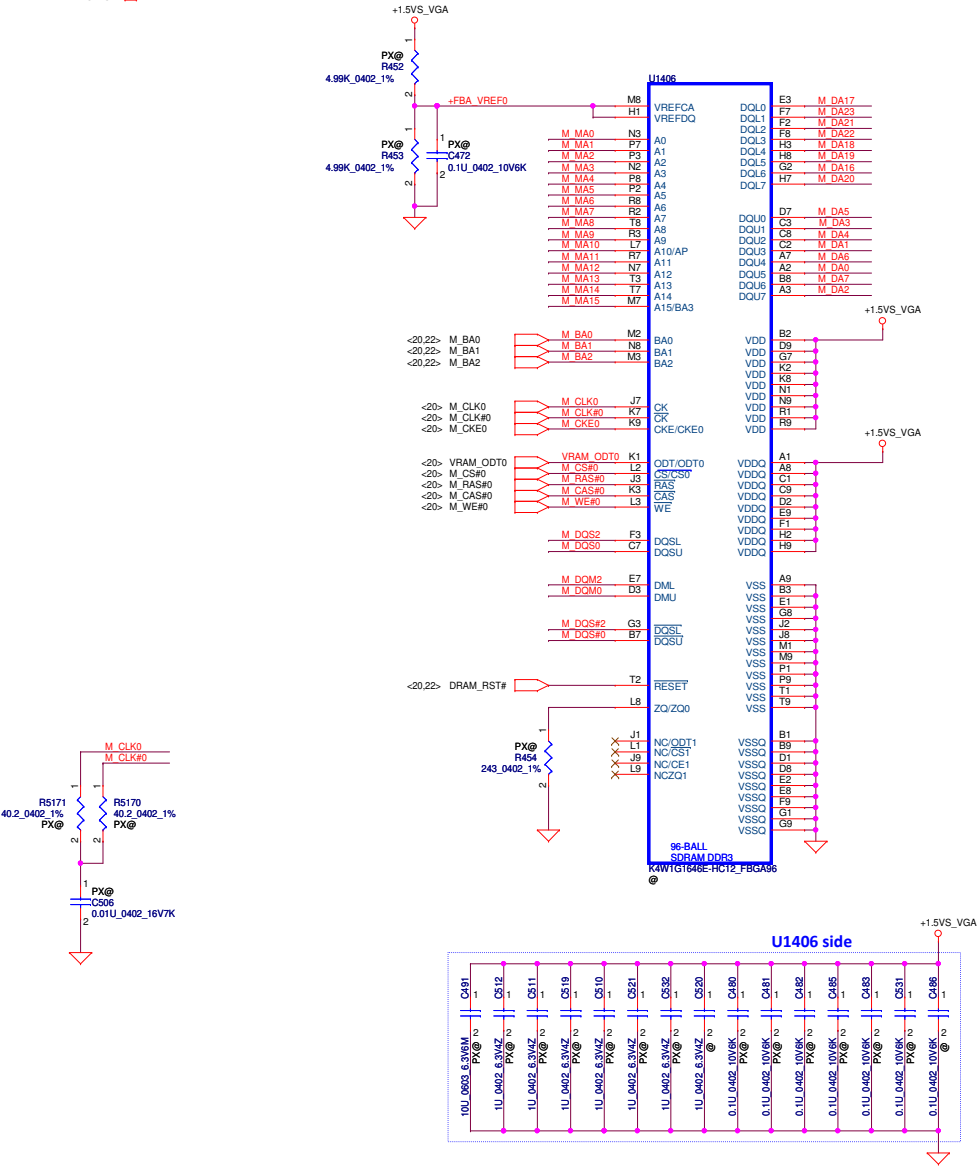


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				Size Custom		Document Number		Rev
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				LA-A321P02				

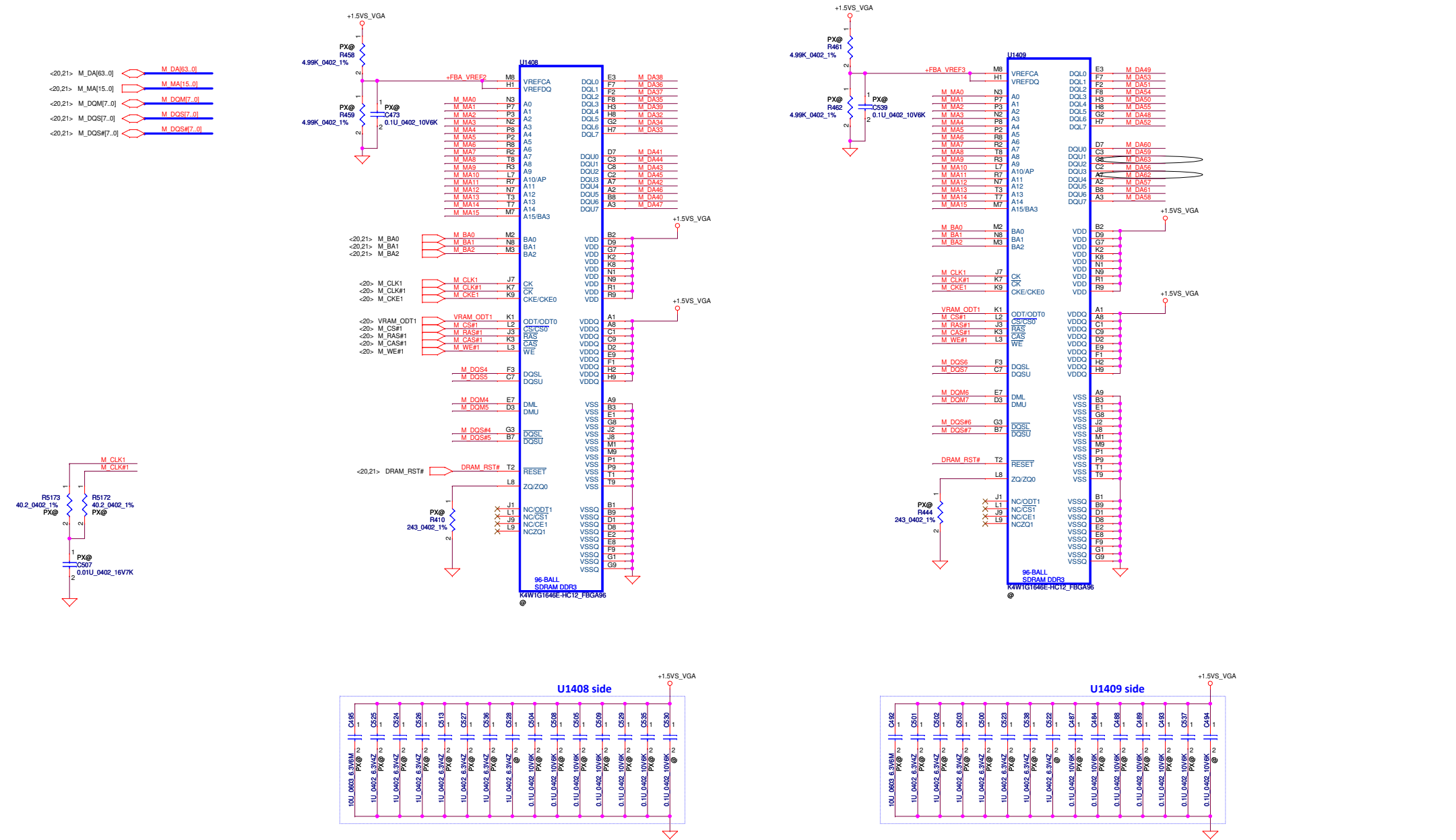


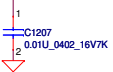
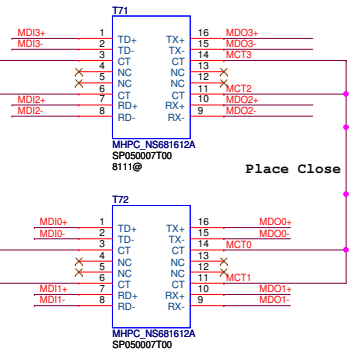
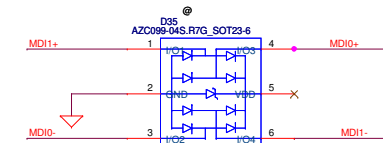
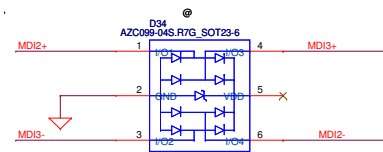
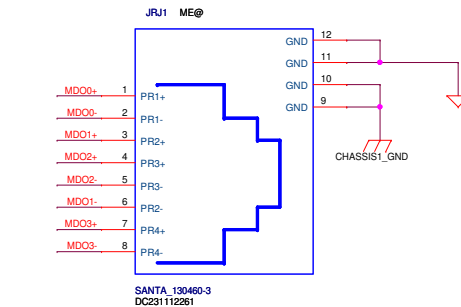
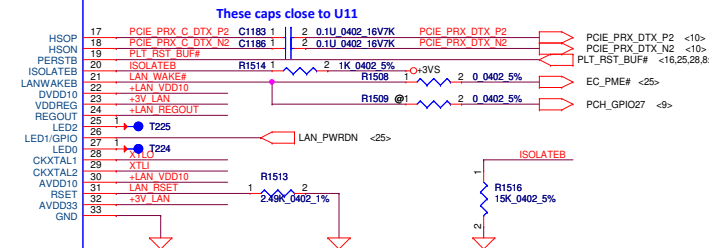
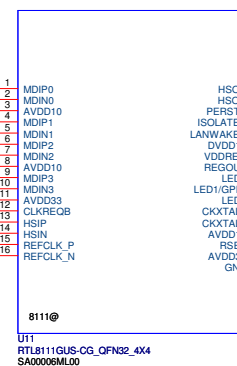
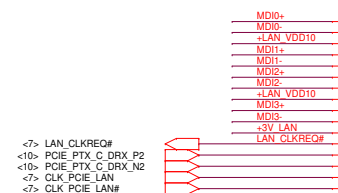
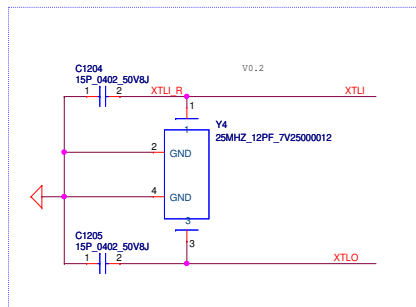
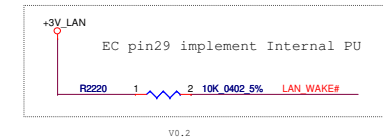
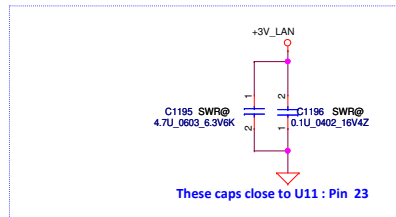
Memory Partition A - Lower 32 bits

- <20,22> M_DA[63..0] M_DA[63..0]
- <20,22> M_MA[15..0] M_MA[15..0]
- <20,22> M_DQM[7..0] M_DQM[7..0]
- <20,22> M_DQS[7..0] M_DQS[7..0]
- <20,22> M_DQS# [7..0] M_DQS# [7..0]



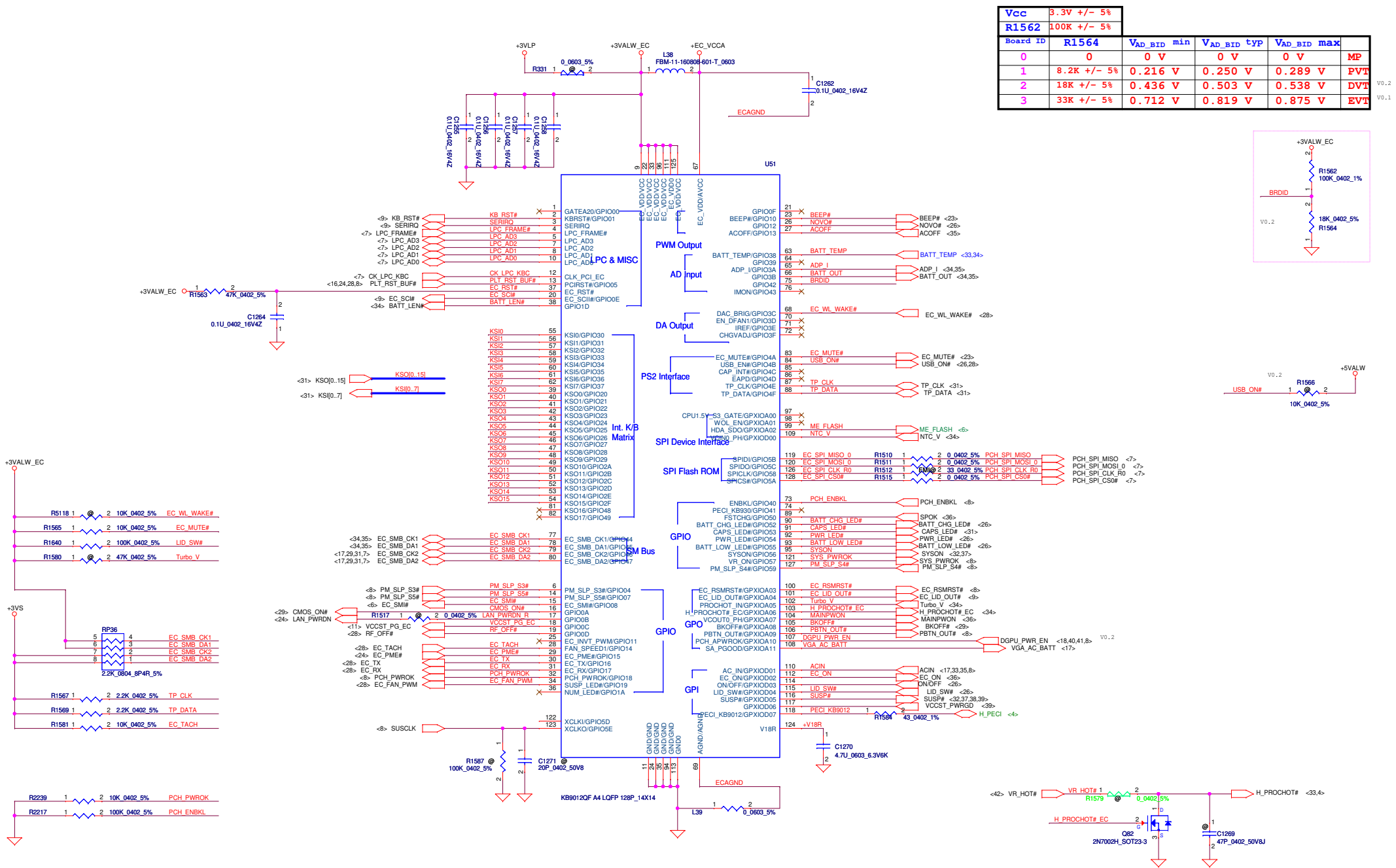
Memory Partition A - Upper 32 bits



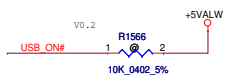
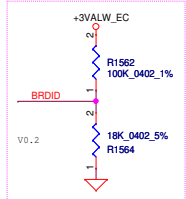


D34/D35
1'S PN:SC300001G00
2'S PN:SC300002E00

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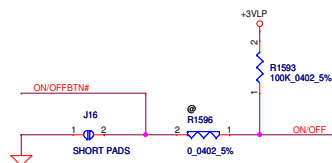


Vcc	3.3V +/- 5%				
R1562	100K +/- 5%				
Board ID	R1564	VAD_BID min	VAD_BID typ	VAD_BID max	
0	0	0 V	0 V	0 V	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	EVT



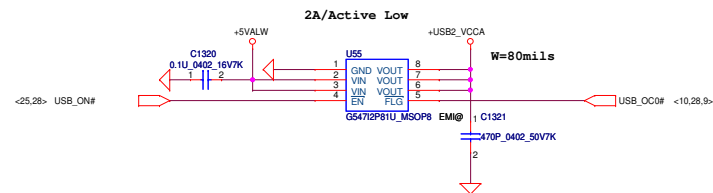
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Connector: 0.3A / pin



ACES_51524-0080N-001
SP0110A900

Pin 1 connection diagram for the LED1 module. The diagram shows a 6-pin header with pins 1 through 6. Pin 6 is connected to +5VALW. Pin 5 is connected to PWR_LED#. Pin 4 is connected to BATT_LOW_LED#. Pin 3 is connected to BATT_CHG_LED#. Pin 2 is connected to BATT_LOW_LED#. Pin 1 is connected to BATT_CHG_LED#. The diagram also shows a 5V pin connected to pin 1 and a GND pin connected to pin 2. The module is labeled JLED1 ME@ and has a part number ACES_51524-0060N-001 SP010014M10.

[illegible]

IO Board

USB2_VCCA +3VS

0.1uF 0402 10VWK C1306

0.1uF 0402 10VWK C1307

W=40mils

W=80mils

JCR1 ME#

USB20 P0_R

USB20 N0_R

USB20 P2_R

USB20 N2_R

USB20 P3_R

USB20 N3_R

DMIC_CLK

DMIC_DATA

PLUG_IN#

HP_OUTL

HP_OUTR

EXT_MIC_SLEEVE

EXT_MIC_RING2

MIC2_VREFO

R1584 1 2 2.2K 0402 5%

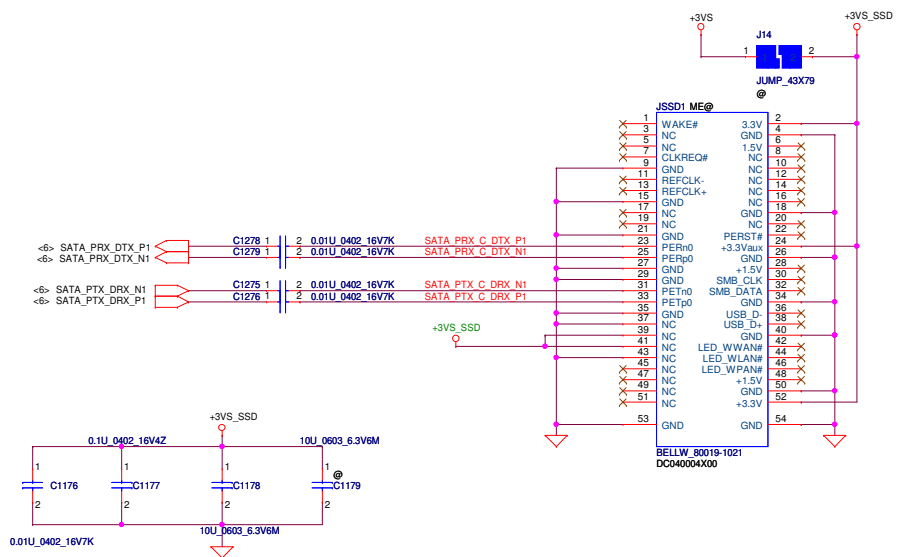
R1595 1 2 2.2K 0402 5%

ACES_88514-02401-07

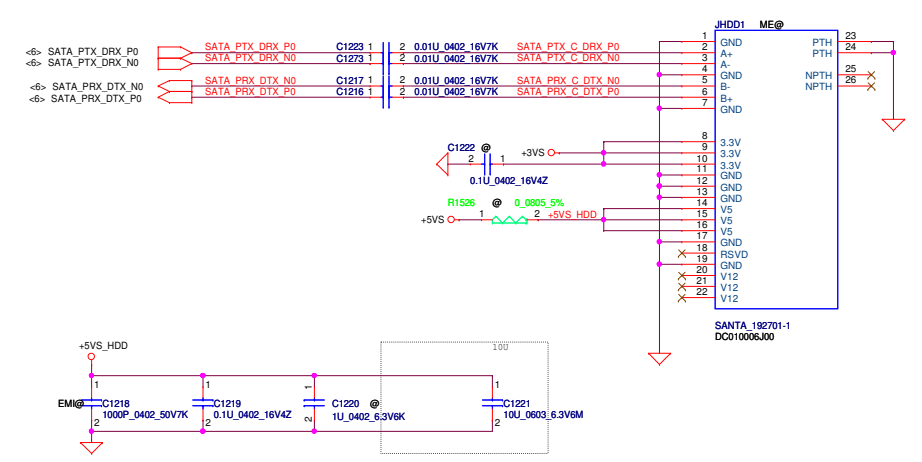
SP010015W00

Security Classification		Compal Secret Data		Compal Electronics, Inc. ROM/KBD/PWR/CR/LED/TP Conn.	
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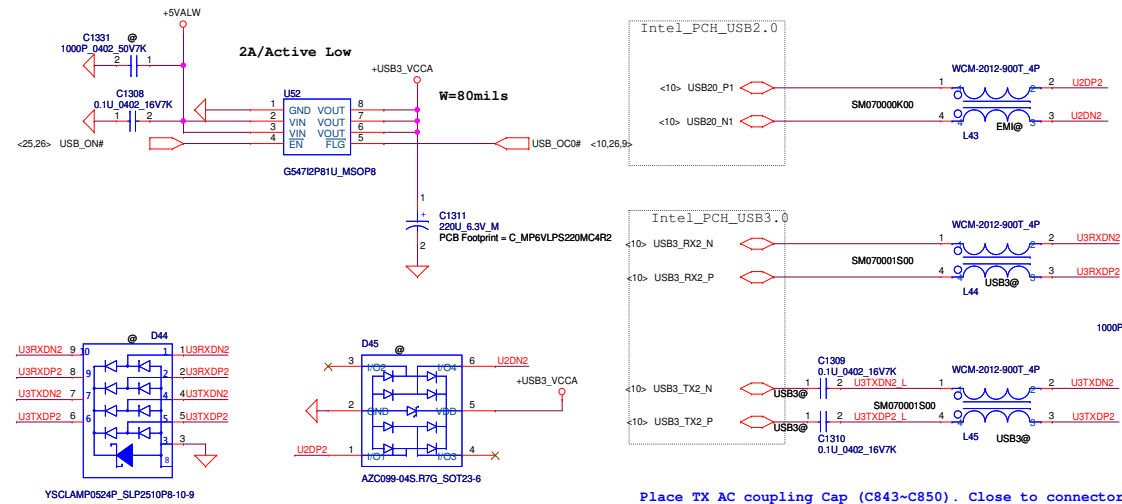
mSATA CONN.



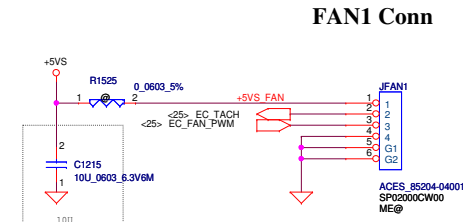
SATA HDD CONN.



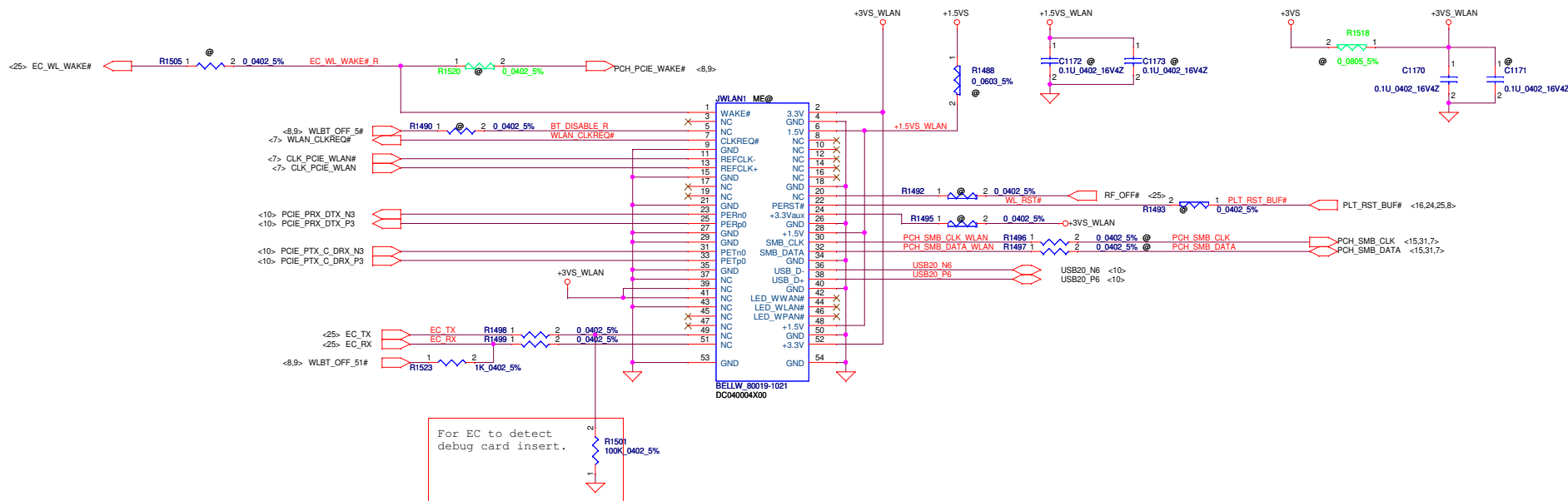
USB 3.0 Charger & Conn.



FAN CONN.



Mini-Express Card for WLAN(Half)



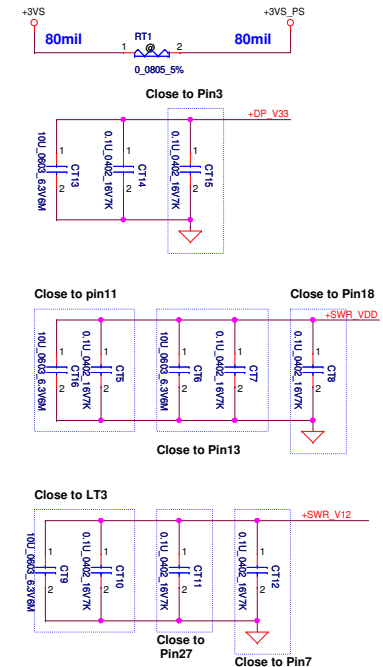
Note: The real behavior of BT_DISABLE are
BT_DISABLE=LOW, BT=OFF
BT_DISABLE=HIGH, BT=ON

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Issued Date	2011/07/21	Deciphered Date	2012/12/31	Mini-Card	
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The schematic diagram illustrates the RTD2132S board layout, showing various components and their connections. Key elements include:

- Power Section:** Features a 3V5 PS input connected to a network of capacitors (40mil, 60mil, 20mil, 60mil) and resistors (4.7uH, 1.1A_20%) to regulate SWR_VDD, SWR_VDD, SWR_LX, and SWR_VCCX. It also shows connections for TXEC+, TXEC-, TXE2+, TXE2-, TXE1+, TXE1-, TXE0+, and TXE0-.
- I2C Section:** Shows the I2C address 0xA8 connected to the EDP_AUXP and EDP_AUXN pins. It includes a 1k resistor (R1560) and a 12k resistor (RT8) connected to the EDP_HPD pin.
- Other Section:** Details the connection of the RTD2132S chip to the LVDS, EDID, and ROM sections. It shows connections for the LVDS_ACLK, LVDS_A2, LVDS_A2#, LVDS_A1, LVDS_A1#, LVDS_A0, and LVDS_A0# pins. It also shows connections for the EDID_CLK, EDID_DATA, MIIC_SCL, and MIIC_SDA pins.
- Component Values:** Various component values are specified, including 40mil, 60mil, 20mil, 60mil, 4.7uH, 1.1A_20%, 1k, 12k, 100k, and 12K_0402_1%.

MIIC_SDA MIIC_SCL	0	1
0	X	EC CODE
1	Internal ROM	EEPROM



The schematic shows the internal components of the APL3512ABITRG_SOT23-5 IC. The input voltage is +3VS, which is connected to VIN (pin 5) through a 60mils trace. VIN is also connected to SS (pin 4). A 1500P_0402_50V7K capacitor (C614) is connected between SS and ground. The output VOUT (pin 1) is connected to LCDVDD_CONN, which is also connected to +LCDVDD_CONN. The GND pin (pin 2) is connected to ground. The EN pin (pin 3) is connected to ground. The APL3512 EN signal is connected to the EN pin through a 4.7nF_0803_6.3V6K capacitor (C613). The TL_ENVDD signal is connected to the APL3512 EN signal through a 0.0402_5% resistor (R1471). The PCH_ENVDD signal is connected to the APL3512 EN signal through a 0.0402_5% resistor (R1470). The R399 resistor (100K_0402_5%) is connected between the APL3512 EN signal and ground.

Q70 CMOS@
PMV65XP_SOT23-3-D

3V3V_CMOS

100

0.0603 5% (20 MIL) R1456

CMOS@

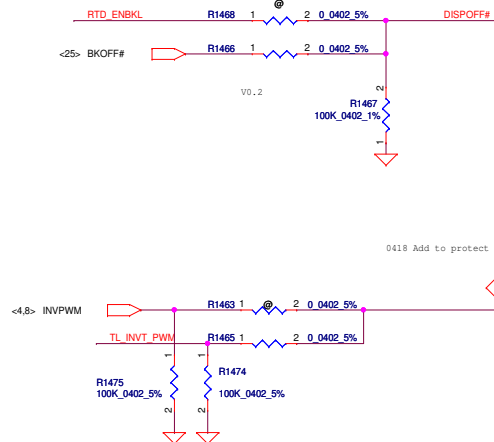
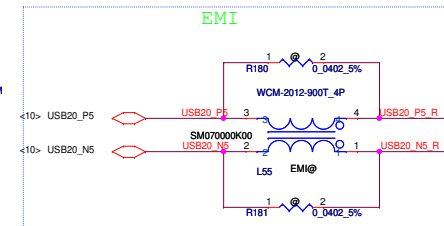
C1152 0.1U_0402_16V4Z

R1456 CMOS@ 150K_0402_5%

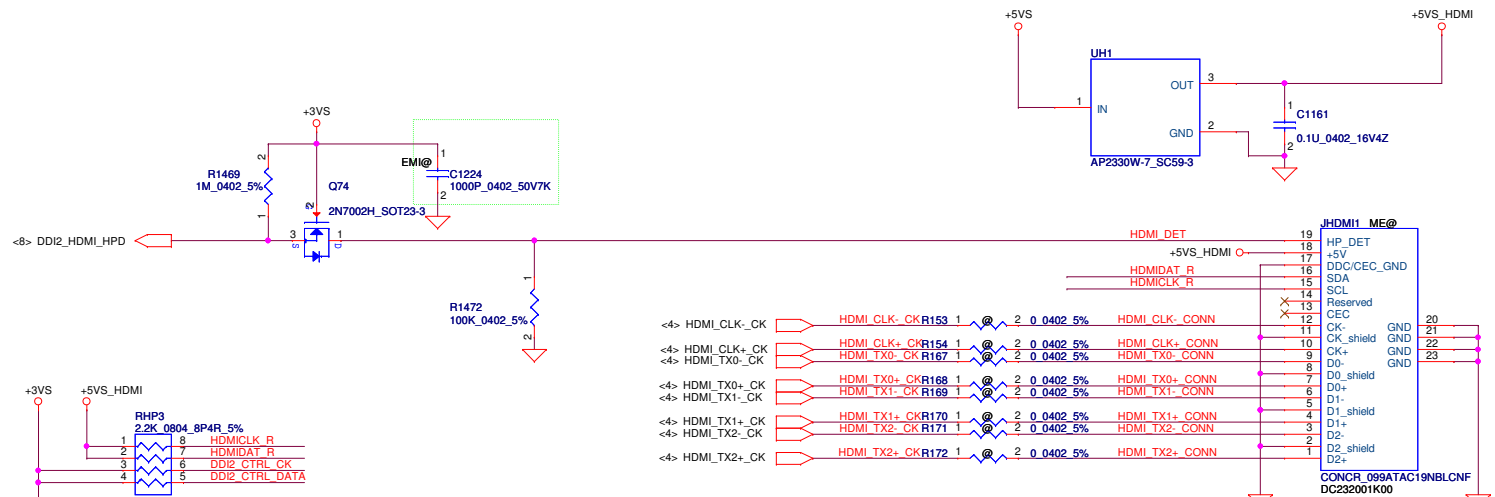
C1155 CMOS@ 0.1U_0402_16V4Z

C1153 10U_0603_6.3V6M

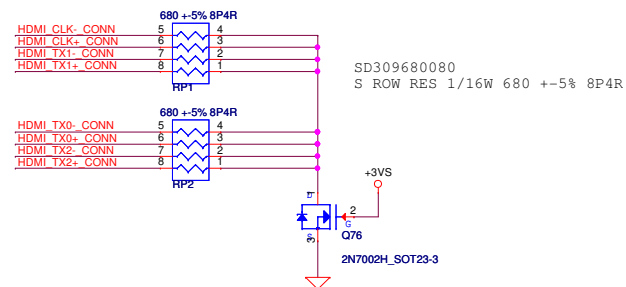
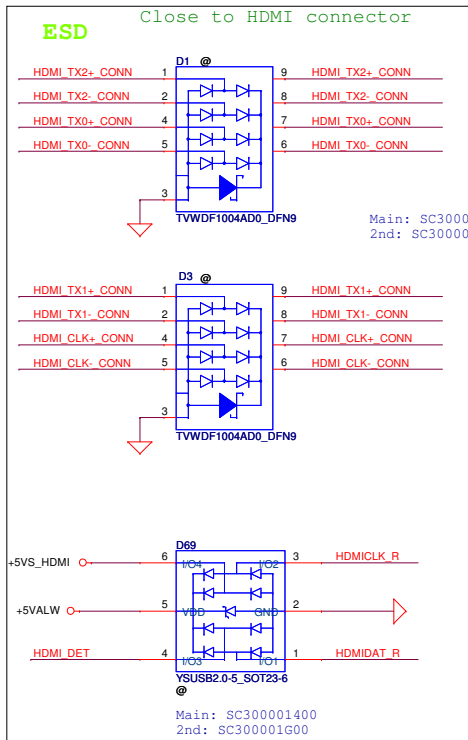
R296 for CMOS shake issue reserve

[illegible]

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				Custom Document Number LA-A321PR02	0.2
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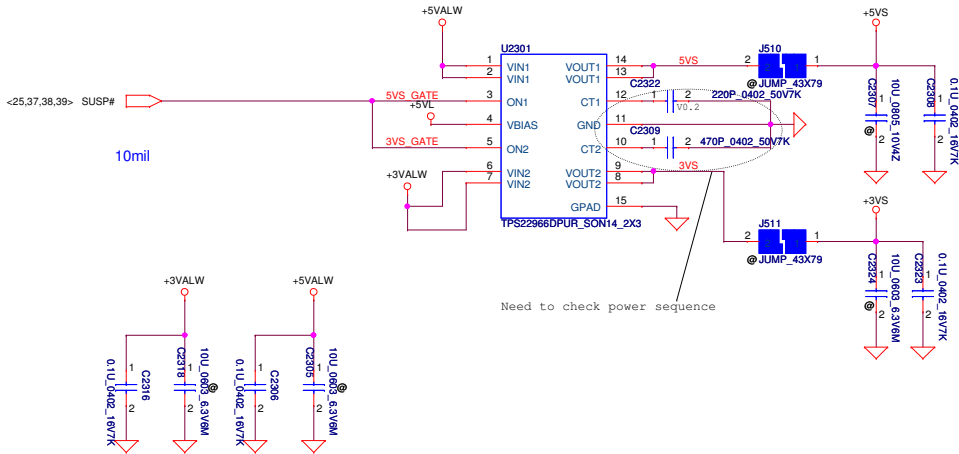


Change Symbol to main source 02/24

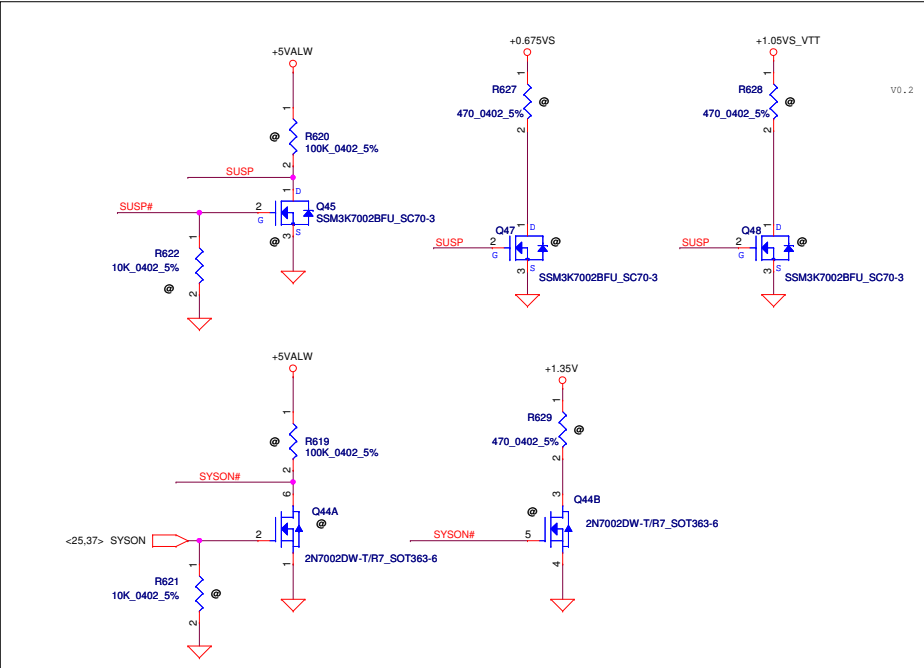
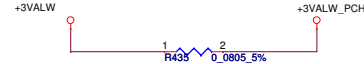


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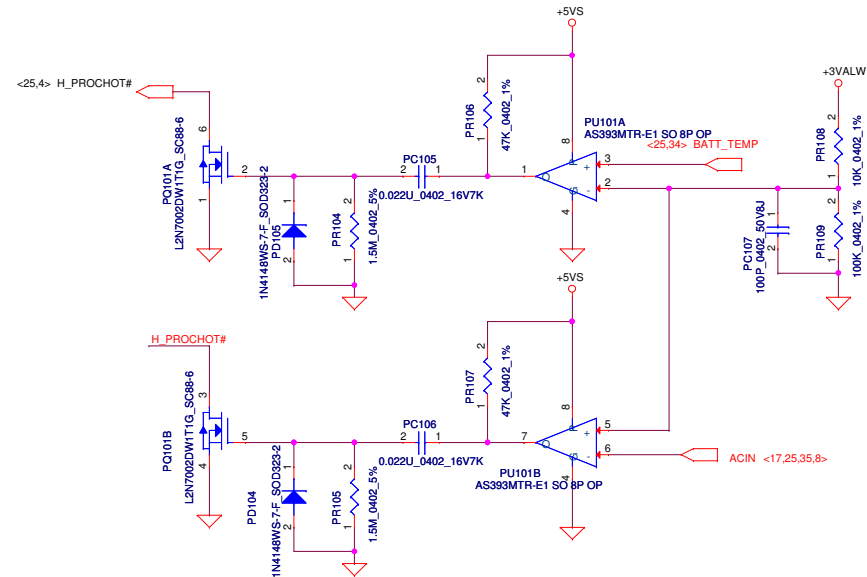
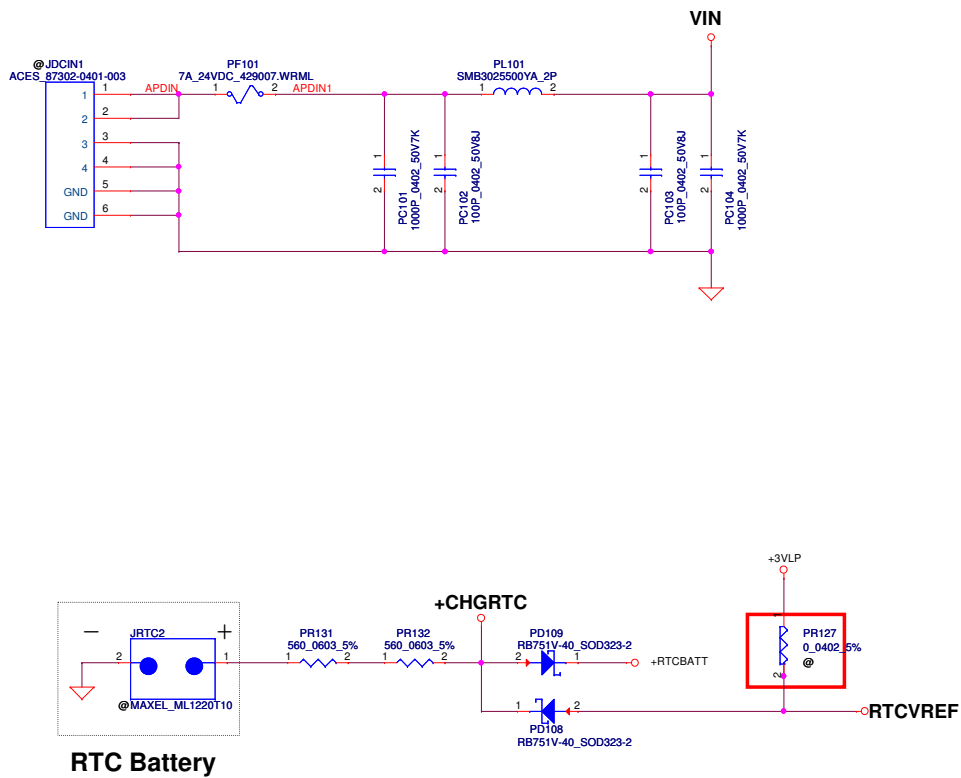
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+3VALW TO +3VS



+3VALW TO +3VALW(PCH AUX Power)
+5VALW TO +5VALW(PCH AUX Power)

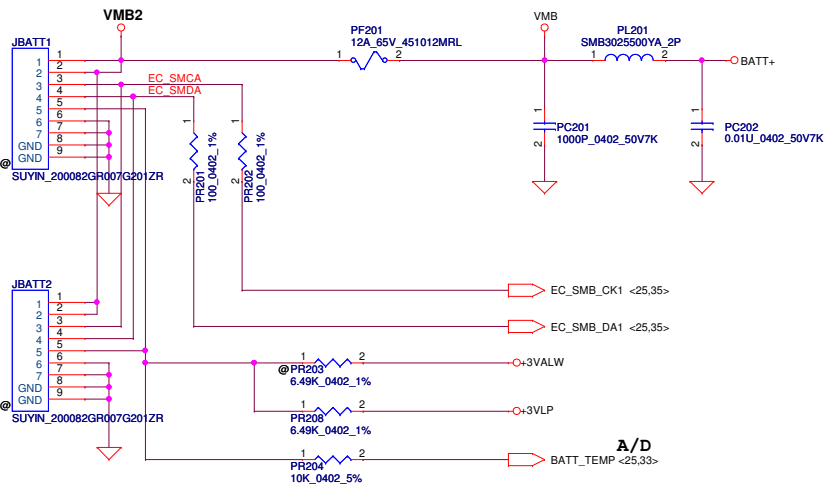


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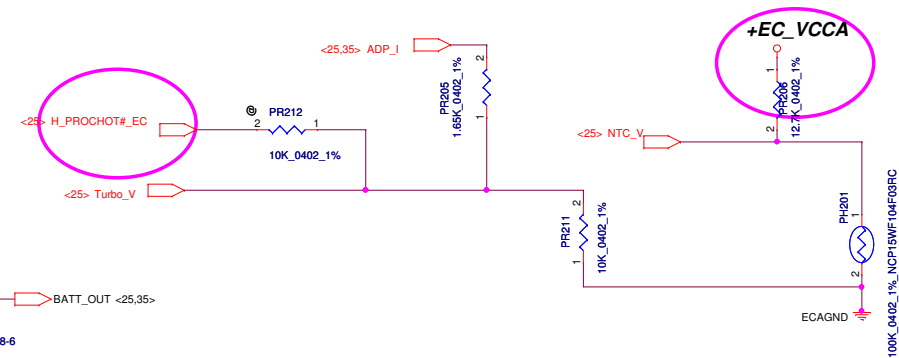
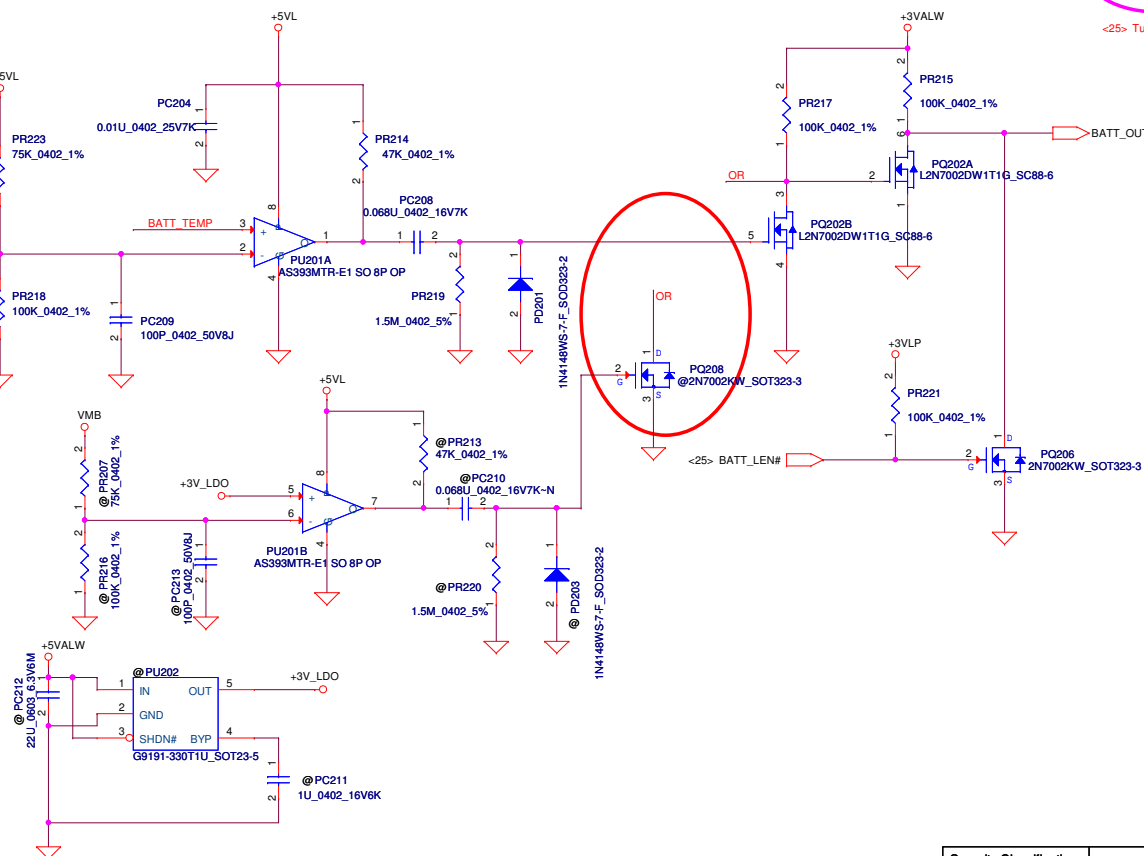
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Issued Date	2010/01/25	Deciphered Date	2012/07/11	Title	PWR DCIN
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JBATT1 Just for 13.3"
JBATT2 Just for 14"

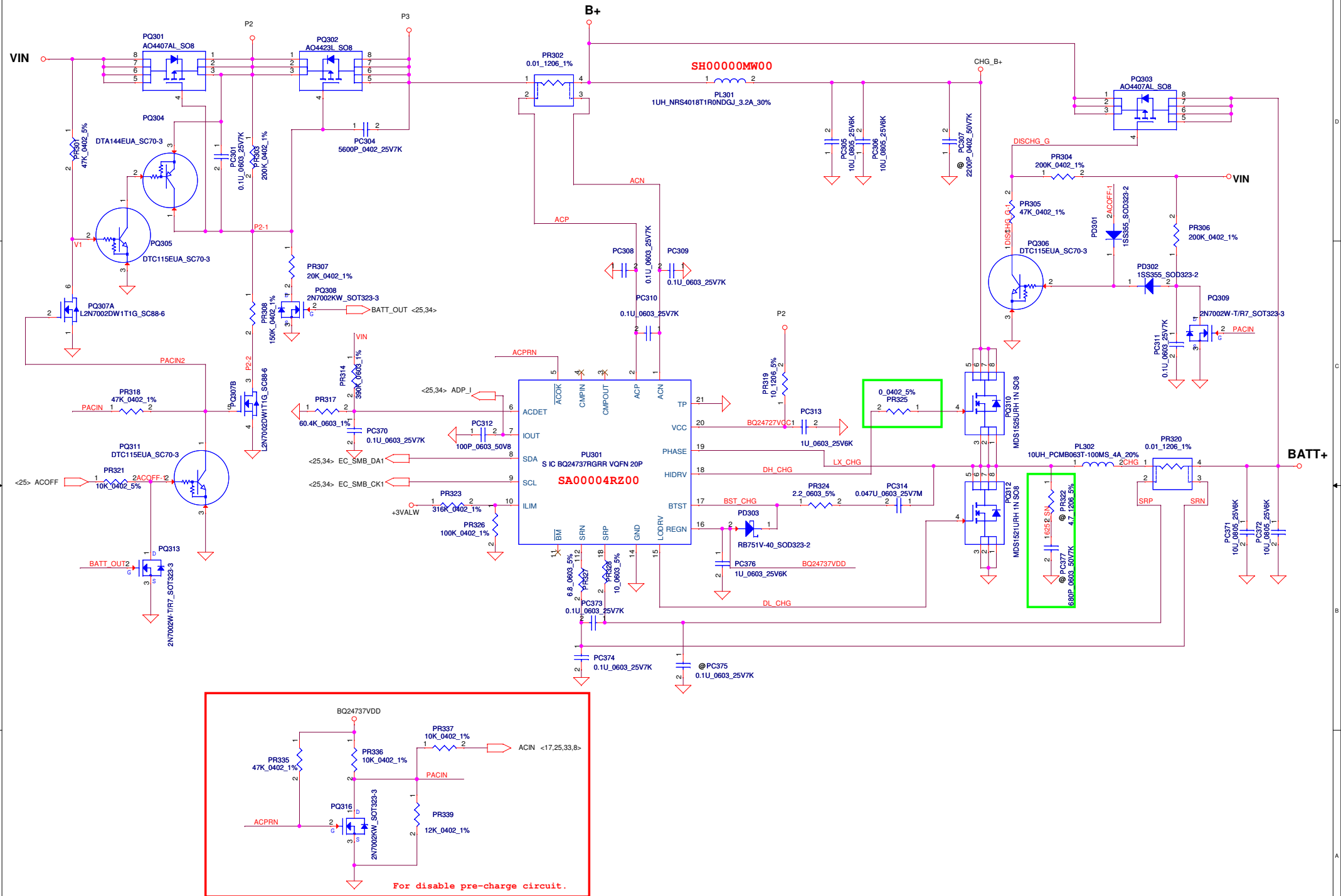


PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

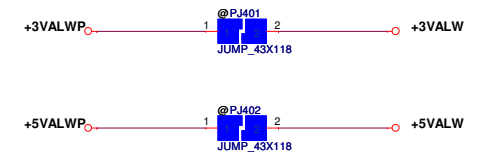
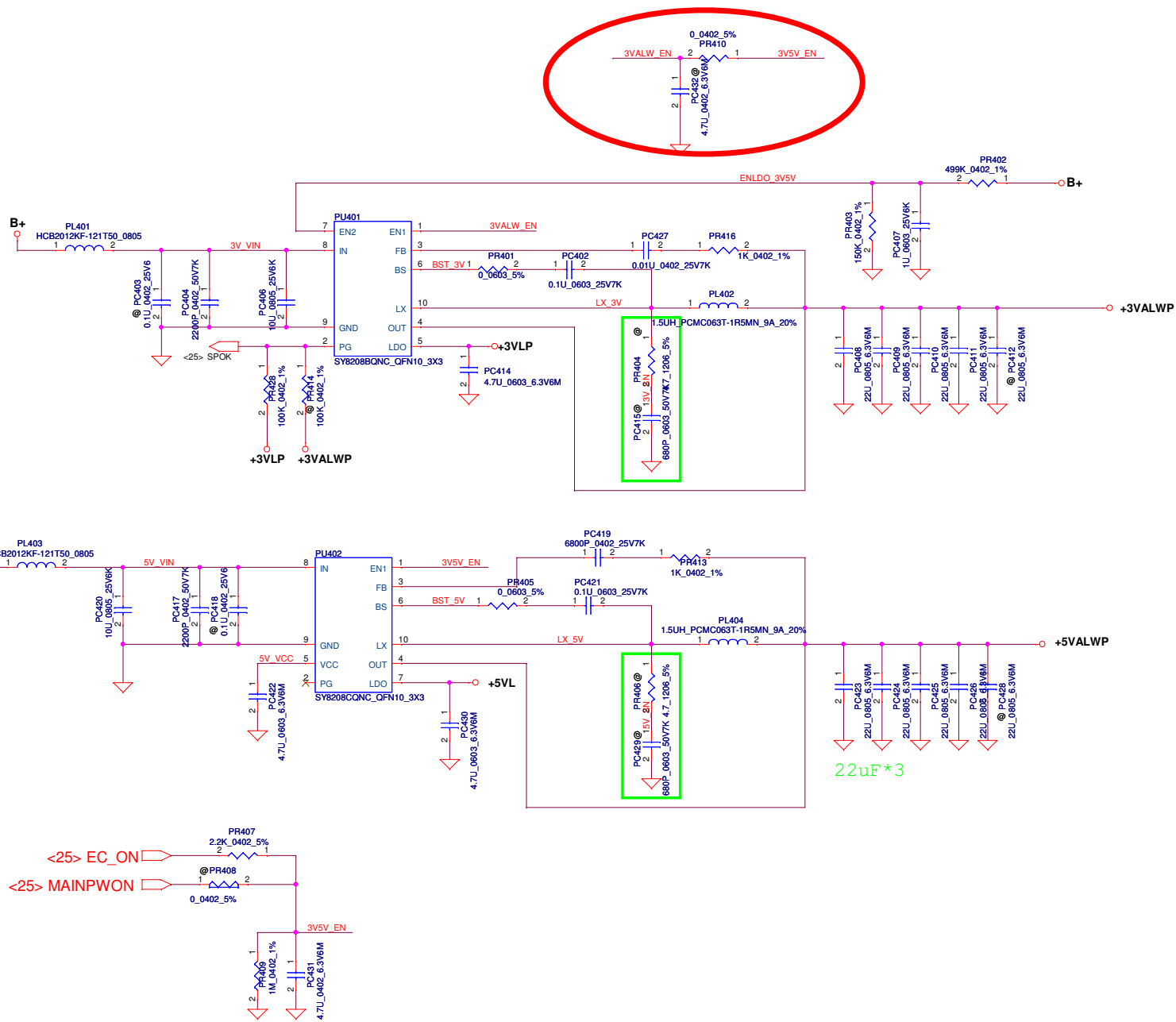
65W(UMA) : PR205=1.65K(SD034165180)



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Issued Date	2010/01/25	Deciphered Date	2012/07/11	Document Number	PWR-BATTERY CONN/OTP	
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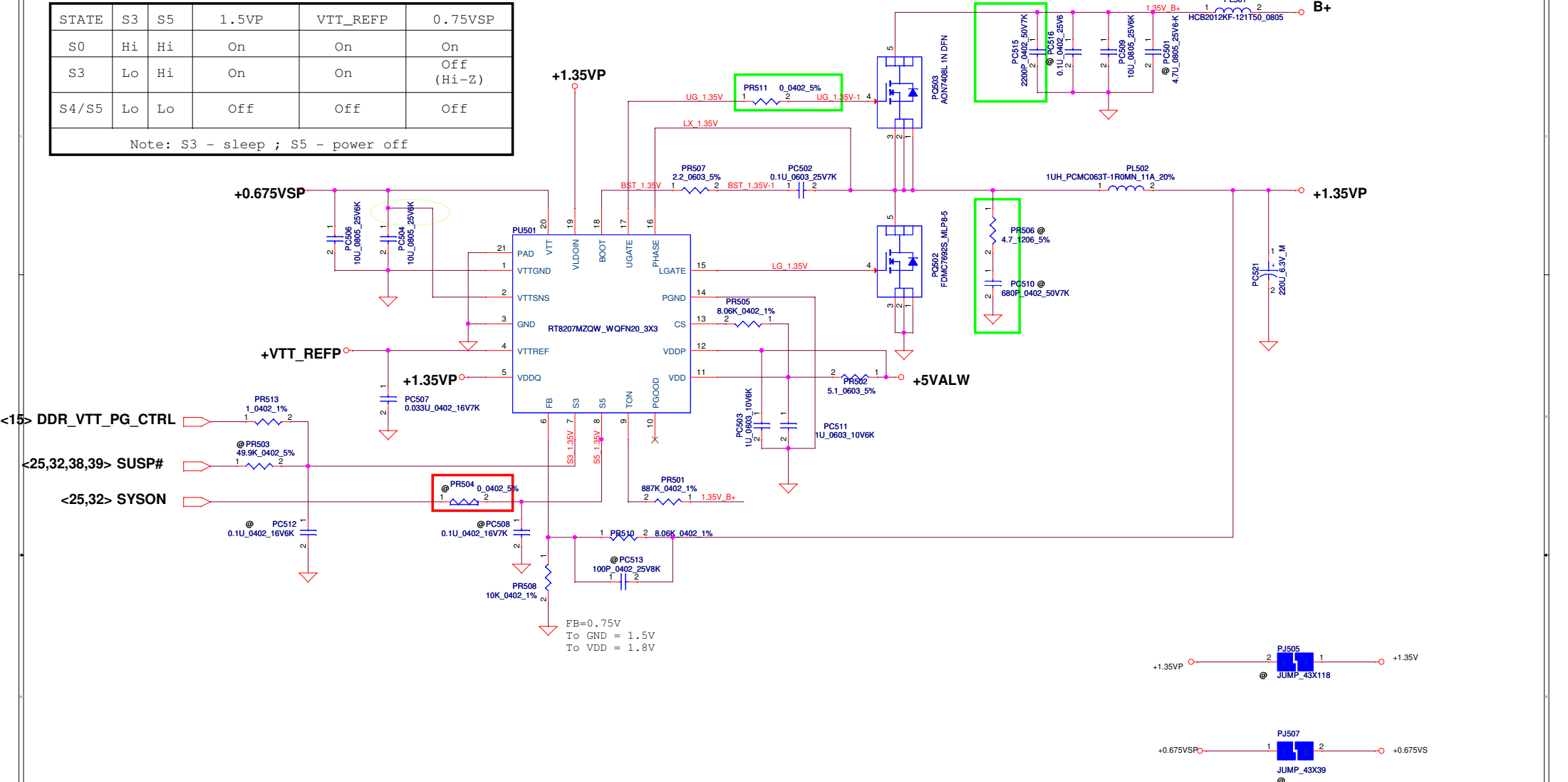


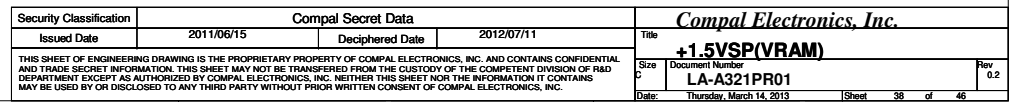
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/01/13	Deciphered Date	2012/07/11	Title	CHARGER
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				Date:	Thursday, March 14, 2013	Sheet	36 of 46

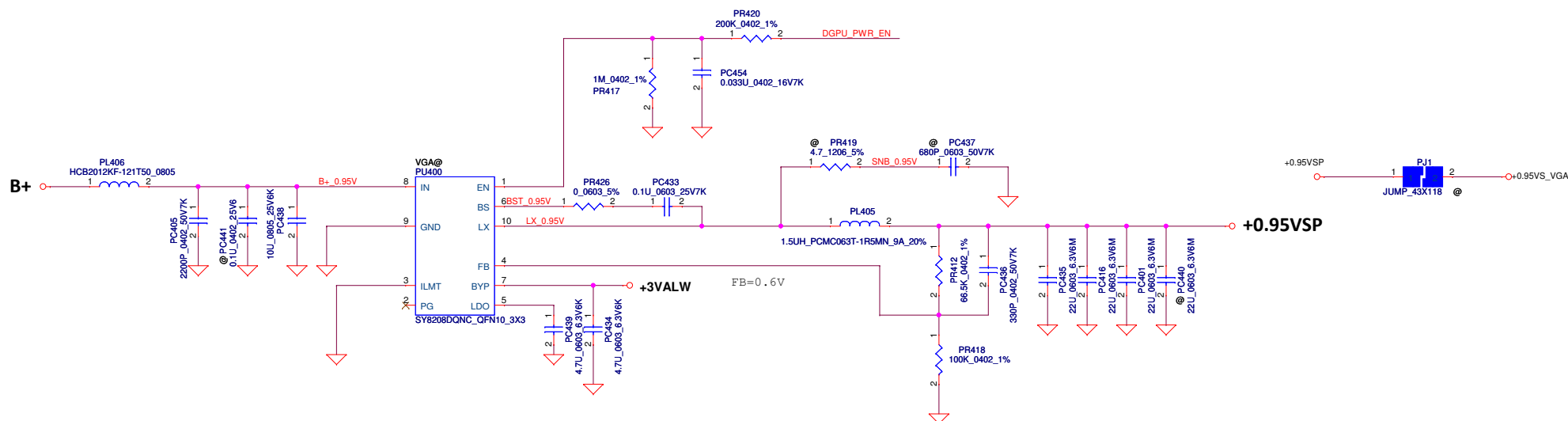
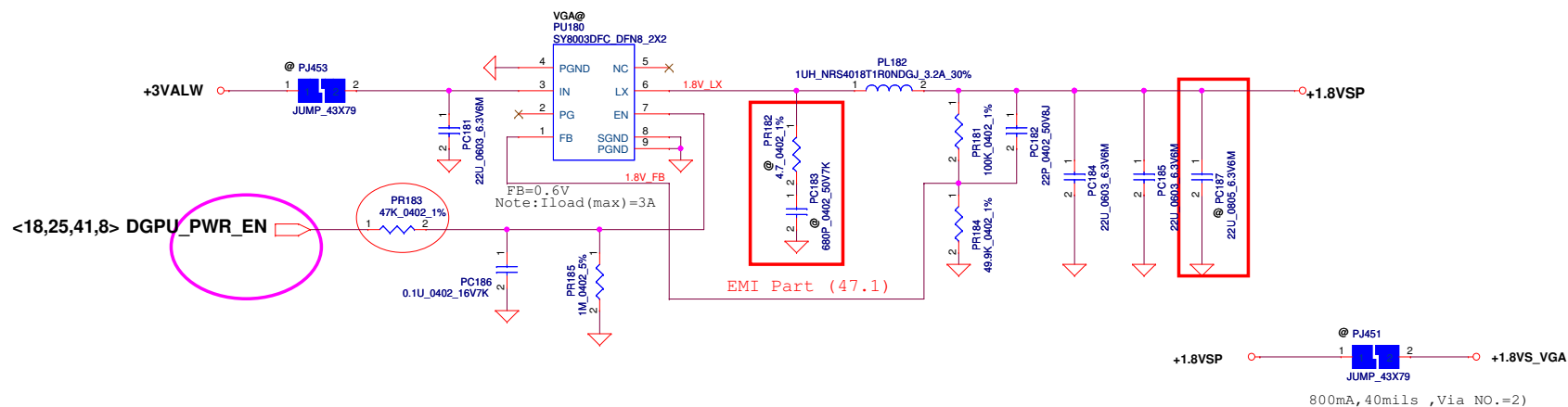
STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					



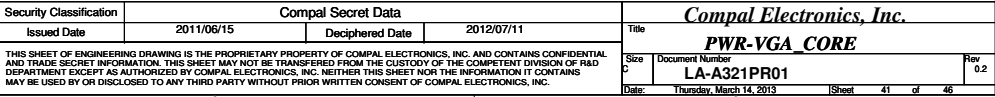


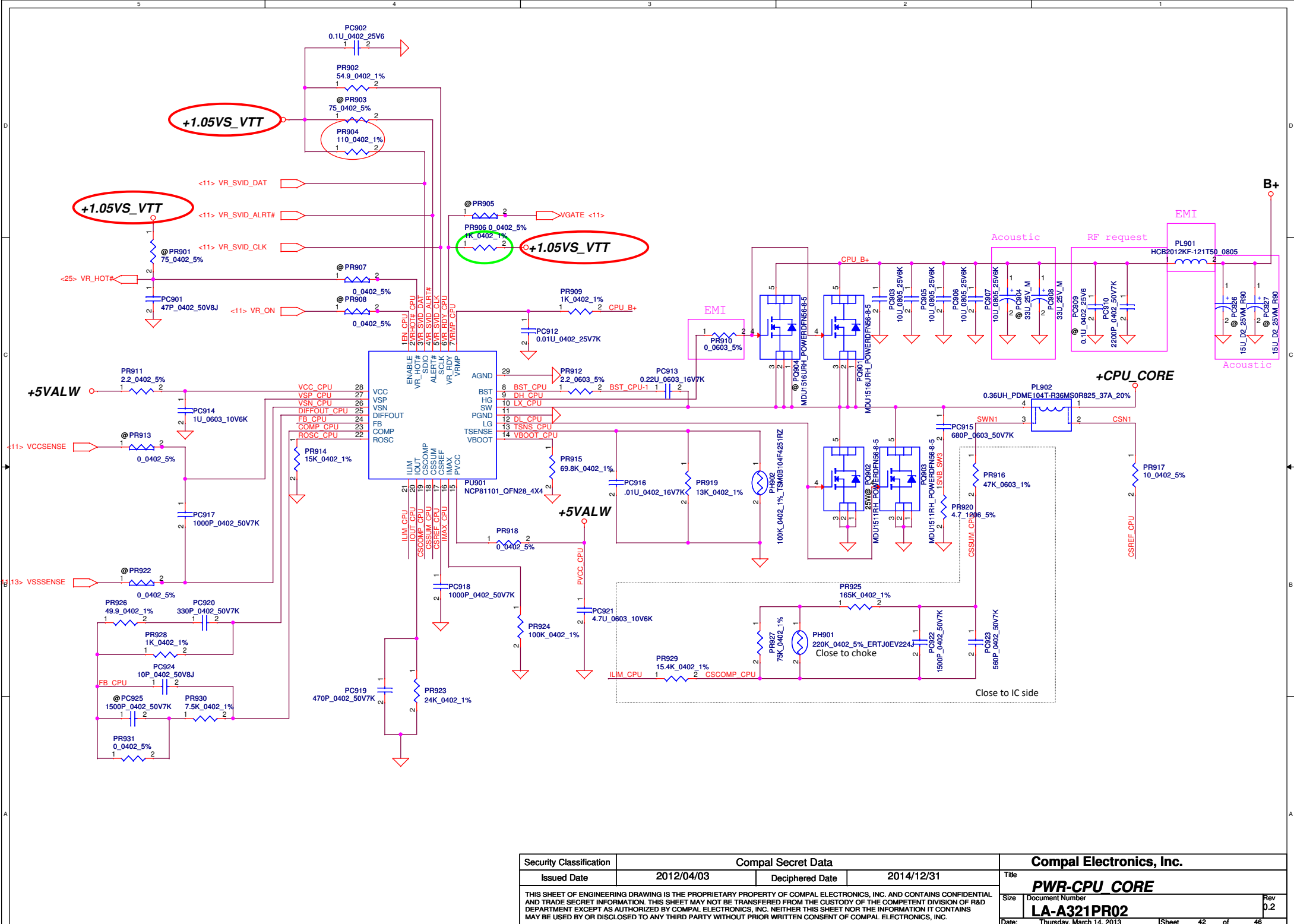
EMI

1.8V controller (35.15), Support component (35.16)



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+CPU_CORE

30 X 22u/0805

RF request

Reserve

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Version change list (P.I.R. List)

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for PWR

Item	Modify List	PG#	Reason for change	Date	Phase
1	For HW sequence	44	ADD PR821 100K ohm pull high +VS_VGA	3/11	SDV
2	For HW sequence	37	Remove PC512 0.1U_0402	3/11	SDV
3	For HW sequence	39	Change PC443 to 0.1U_0402	3/11	SDV
4	For HW sequence	40	Change PC186 to 0.1uf	2/7	SDV
5	For HW sequence	40	Change PC454 to 0.033uf	2/7	SDV
6	For HW sequence	40	Change PR183 to 47K ohm	2/7	SDV
7					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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				Size Custom	
Document Number				Rev	
C38-AMD KABINI Schematic				0.2	
Date: Thursday, March 14, 2013				Sheet 44 of 46	

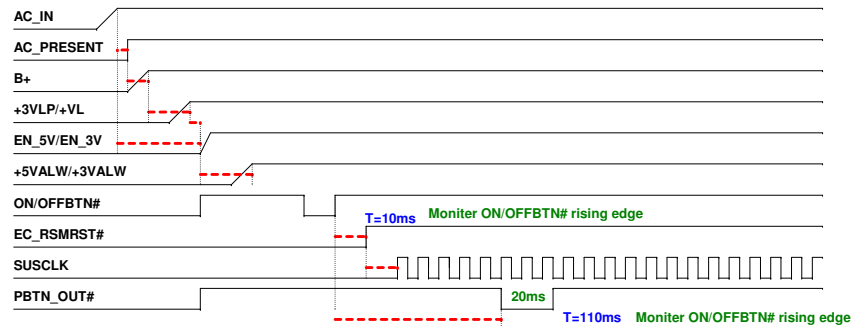
Version change list (P.I.R. List)

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for HW

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	PIR (EE)
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[AC Mode]



[DC Mode]

