

MODEL NAME : VBW01
PROJECT CODE : ANRVBW0100
PCB NO : DA8000WL000 LA-9982P M/B
DA40001FO00 LS-9101P POWER BUTTON/B
DA40001FP00 LS-9102P USB/B
DA40001FQ00 LS-9103P TP BUTTON/B

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Schematic Document

Intel Shark Bay ULT
OAK Mainstream2
UMA/DIS AMD Venus Pro

2013-05-29

Rev: 3.0

X76@ : 76 level
46@ : 46 level
@ : Nopop component
CONN@ : Connector component
XDP@ : XDP function
UMA@ : Only for UMA
DIS@ : Only for Discrete
VENUS@ : VENUS Pro,VENUS XT
VENUSXT@ : VENUS XT
VENUSPRO@ : VENUS Pro
@VENUS@ : VENUS nopop component
EMI@ : EMI parts
@EMI@ : Reserve EMI parts
ESD@ : ESD parts
RF@ : RF parts

BOM config

UMA : UMA@,EMI@,ESD@,RF@

DIS VENUS : VENUS@,VENUSPRO@,DIS@,EMI@,ESD@,RF

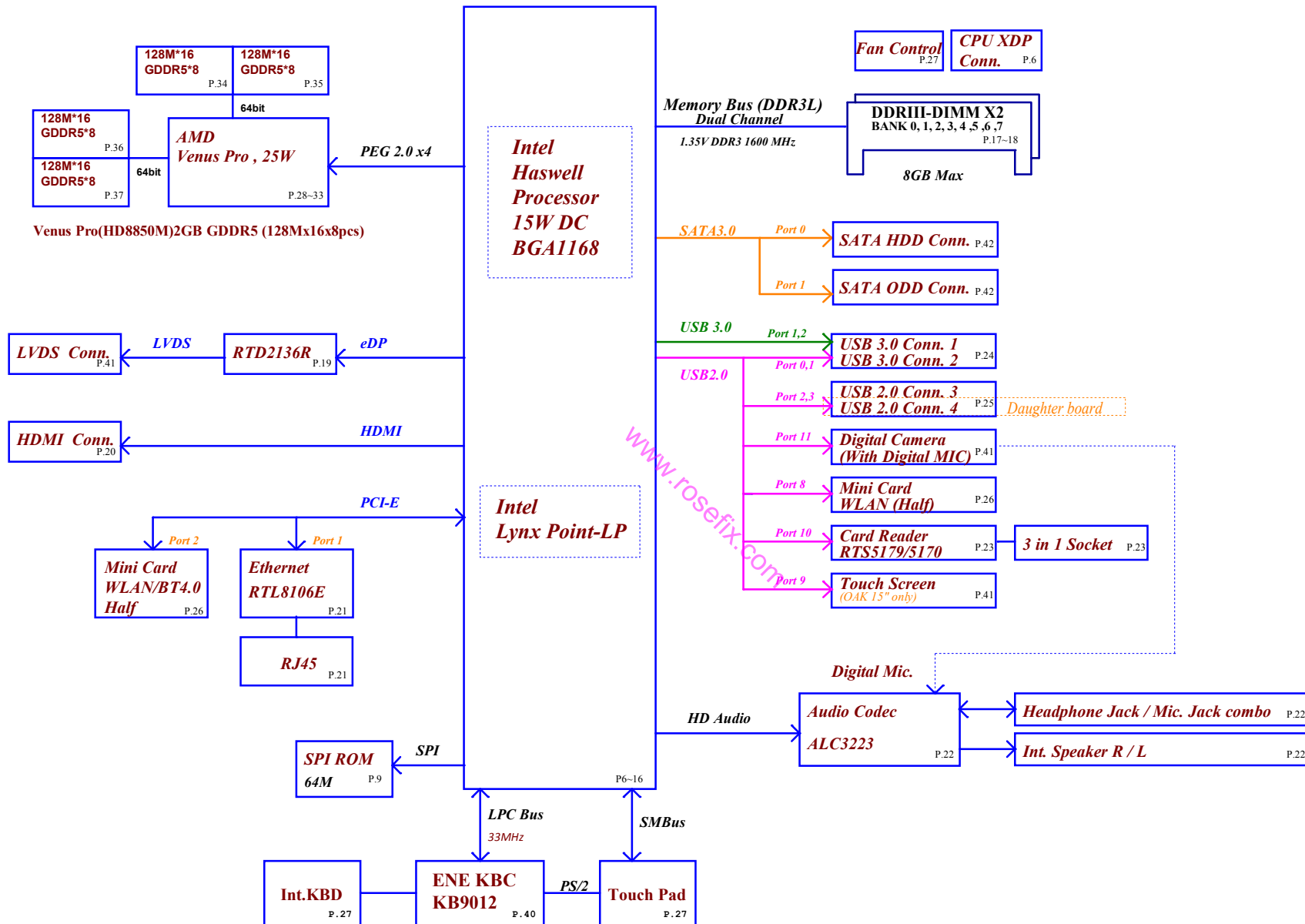
ZZZ R1@



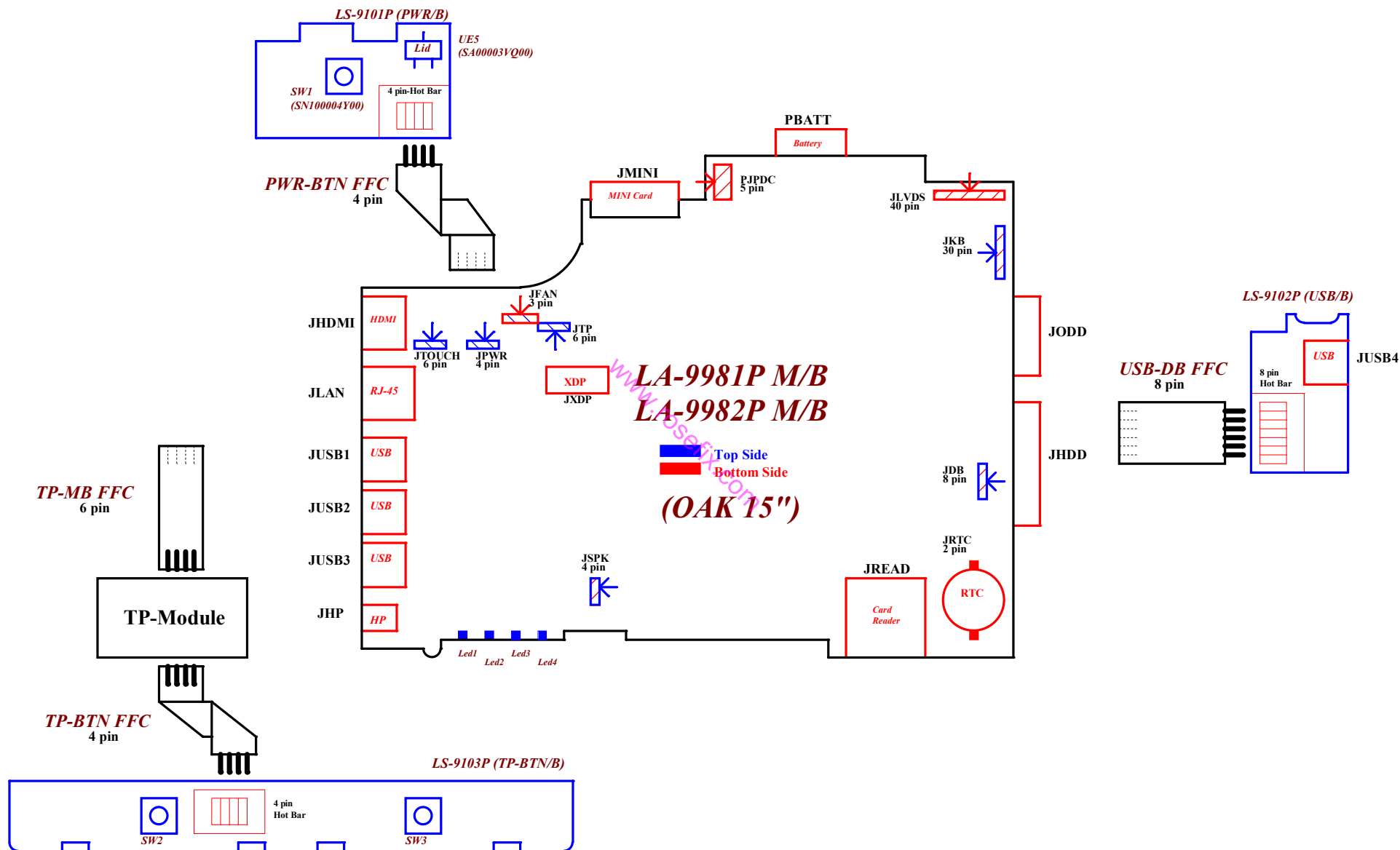
PCB VBW01 LA9982P/LS9101P/LS9102P/LS9103P
DA20ZG00120

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Issue Date	2013/05/29	Deciphered Date	2014/06/01	Title	Cover Page
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				Custom	LA-9982P
				Date	Wednesday, May 29, 2013
				Sheet	1 of 57
				Rev	3.0



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Project Code : VAW00 / VAW01
File Name : LA-9981P / LA-9982P



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				Date	Wednesday, May 29, 2013
				Sheet	3 of 57
				Rev	3.0

Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	V _{AD_BID min}	V _{AD_BID typ}	V _{AD_BID max}	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.677V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

SMBUS Control Table

	SOURCE	BATT	Charger	RTD2136S	VGA	DDR3L	XDP	WLAN mini card	Touch pad
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V						
EC_SMB_CK2 EC_SMB_DA2	KB9012			V	V				
SMBCLK SMBDATA	ULT					V	V	V	V
SML0CLK SML0DATA	ULT								
SML1CLK SML1DATA	ULT								

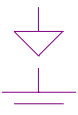
www.rosefix.com

Link

Board ID TABLE

ID	PCB Revision	UMA	Sun XT	VenusPro	VenusXT
0	SSI&A02				
1		SSI&A02			
2				SSI&A02	
3					SSI&A02
4	PT				
5		PT			
6			PT		
7				PT	PT
8	ST				
9		ST			
10				ST	
11					ST
12	XB				
13		XB			
14				XB	
15					XB
16	A01				
17		A01			
18				A01	
19					A01

Symbol Note :



: means Digital Ground

: means Analog Ground

CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU
CLKOUT_PCIE5	

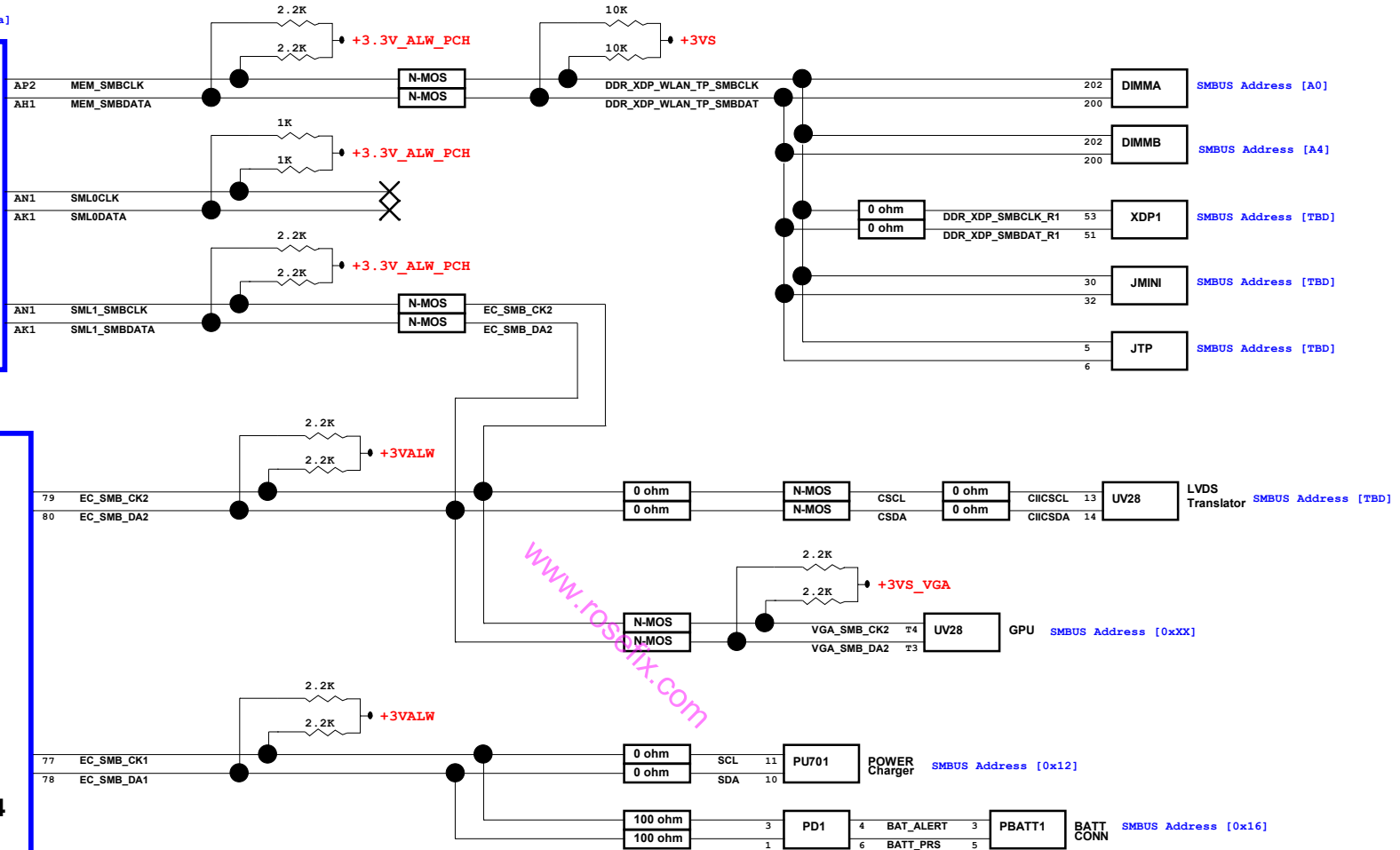
USB3.0	
Port1	USB connector 2
Port2	USB connector 1
Port3	
Port4	
USB2.0	
Port0	USB connector 2
Port1	USB connector 1
Port2	USB connector 3
Port3	USB connector 4 (DB)
Port4	MINI Card (WLAN)
Port5	Touch Screen Panel
Port6	Card Reader
Port7	Camera
PCI EXPRESS	
Lane 1	
Lane 2	
Lane 3	10/100 LAN
Lane 4	MINI Card (WLAN)
Lane 5	PEG (N14P)
Lane 6	PEG (N14P)
SATA	
SATA0	HDD
SATA1	ODD
SATA2	
SATA3	

ULT

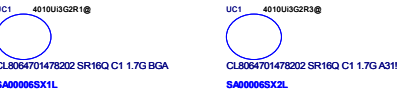
SMBUS Address [0x9a]

MCH
Shark bay

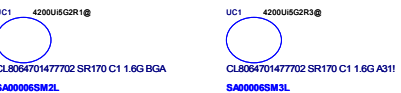
KBC
KB9012A4



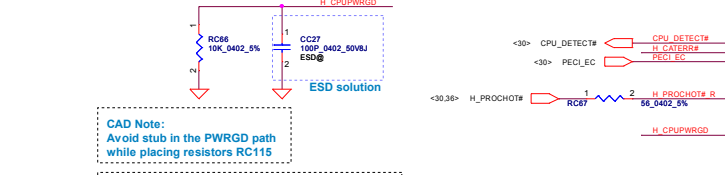
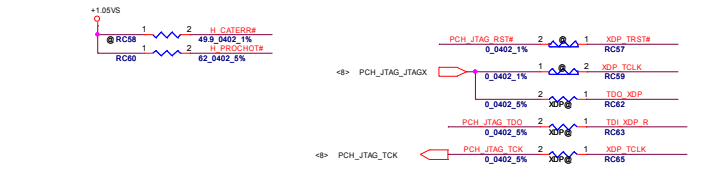
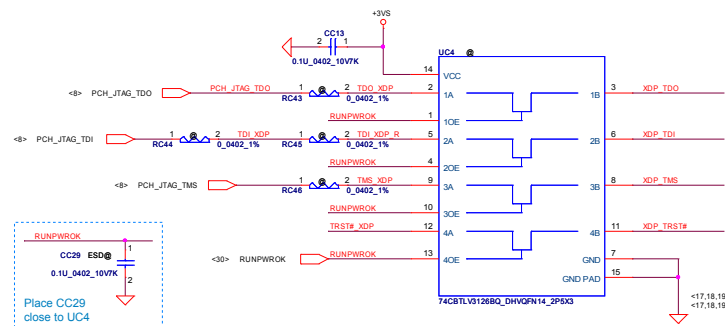
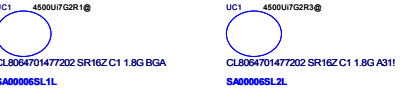
i3-4010U-15W-GT2-MP



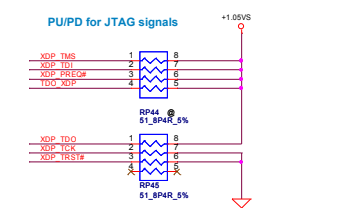
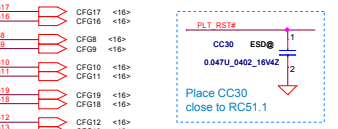
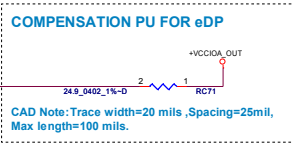
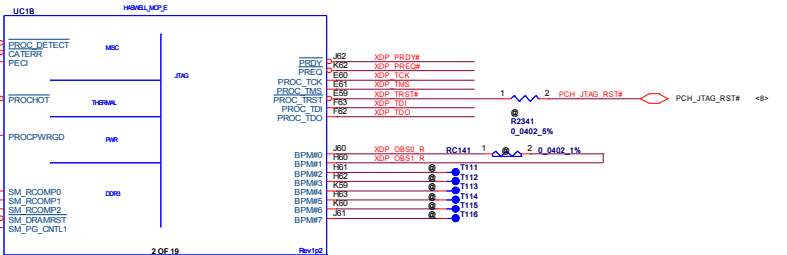
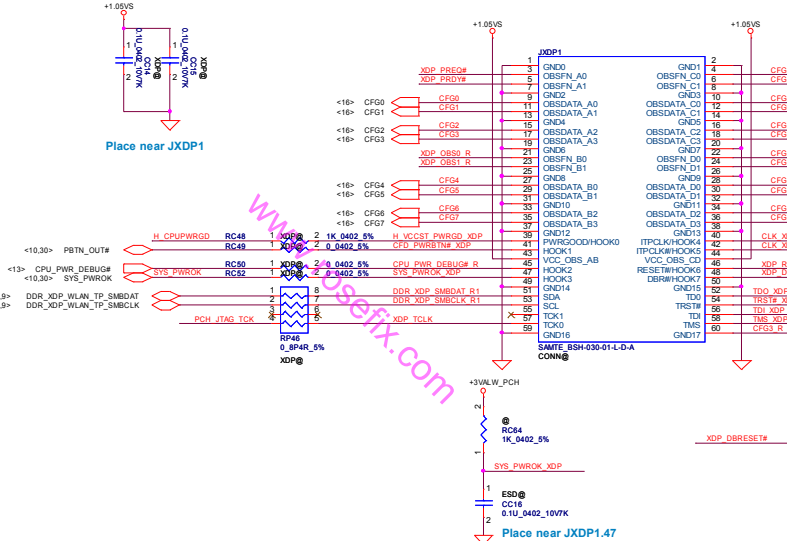
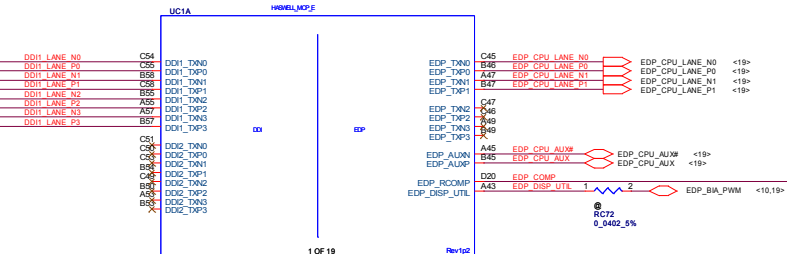
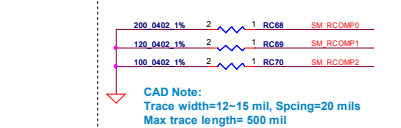
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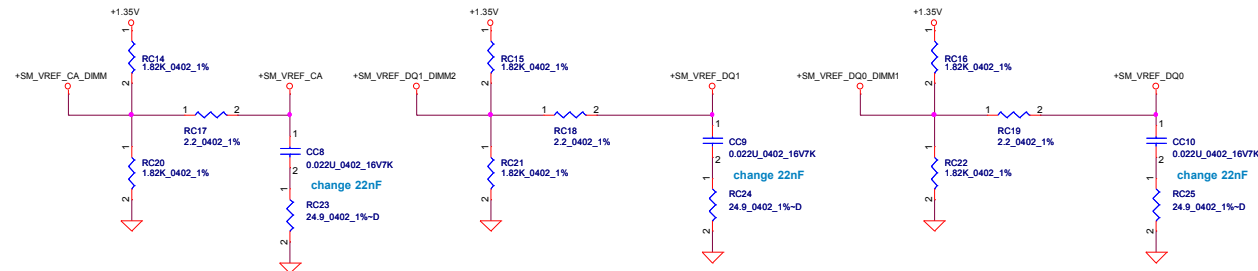
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DDR3 COMPENSATION SIGNALS

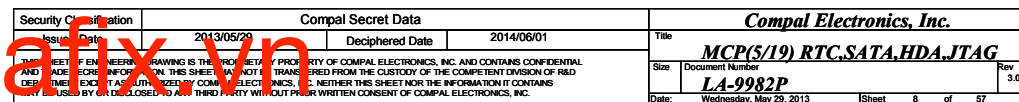


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Issued Date	2013/05/29	Deciphered Date	2014/06/01	Title	MCP(1,2/19) eDP.XDP.MISC
Rev	3.0	Rev	3.0	Site	Document Number: LA-9982P
				Date	Wednesday, May 28, 2013
				Sheet	6 of 67

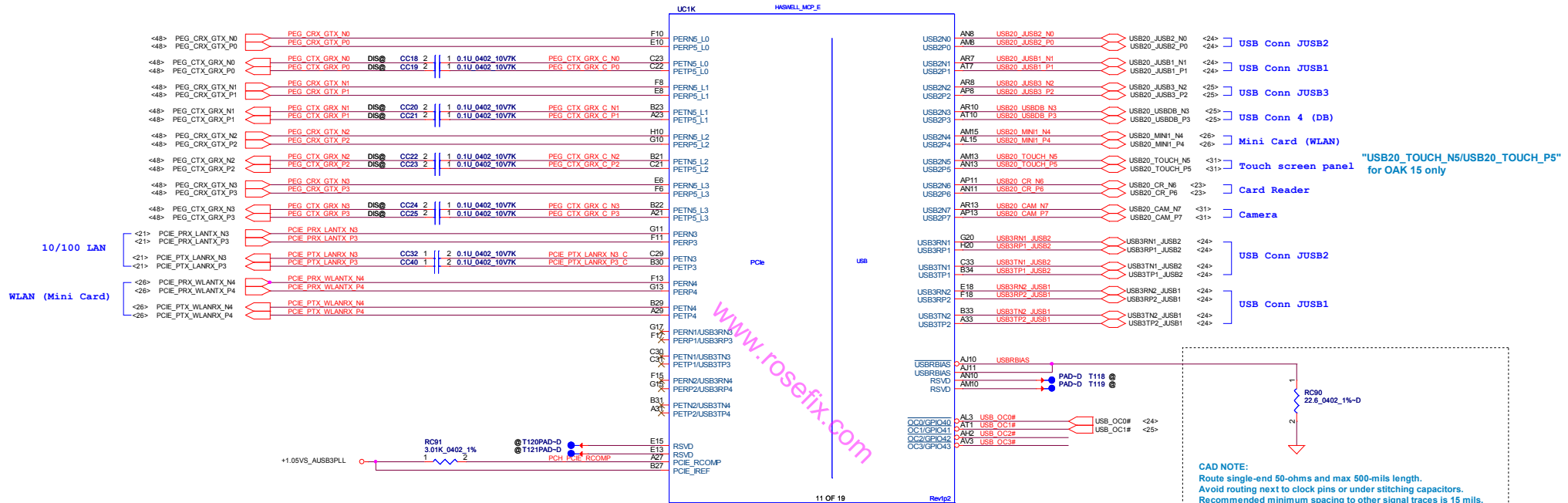


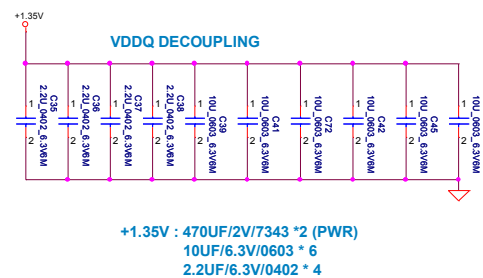
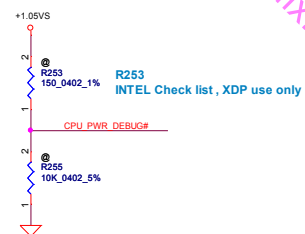
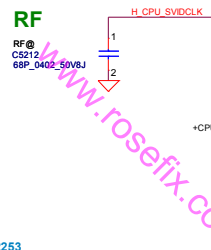
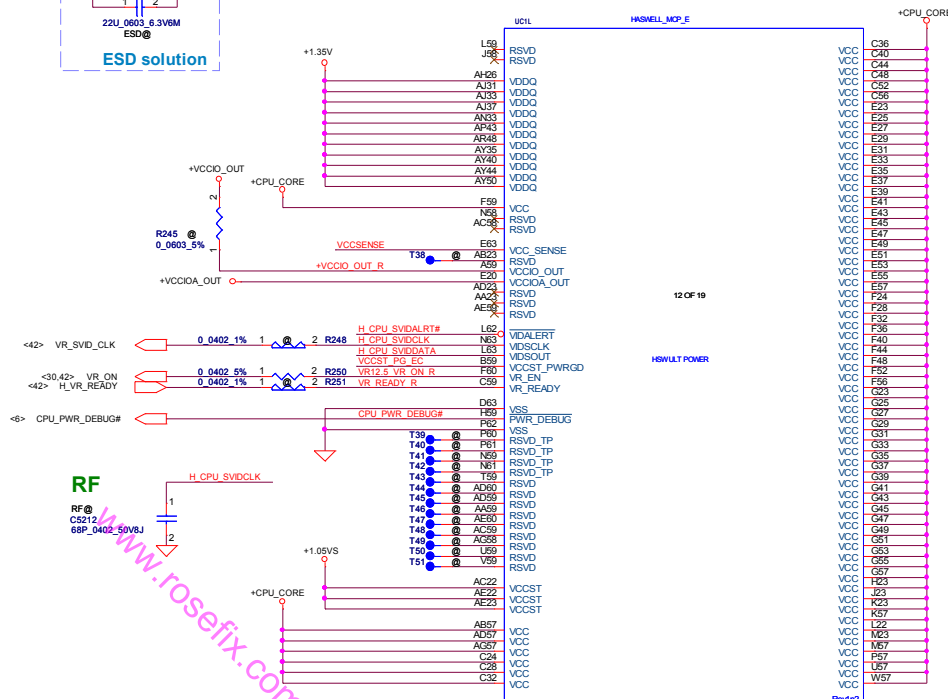
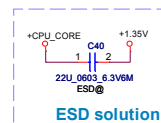
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				Date:	Wednesday, May 28, 2013
				Sheet	7 of 57
				Rev	3.0

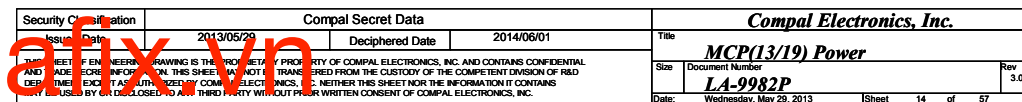
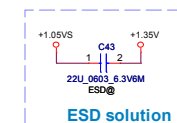


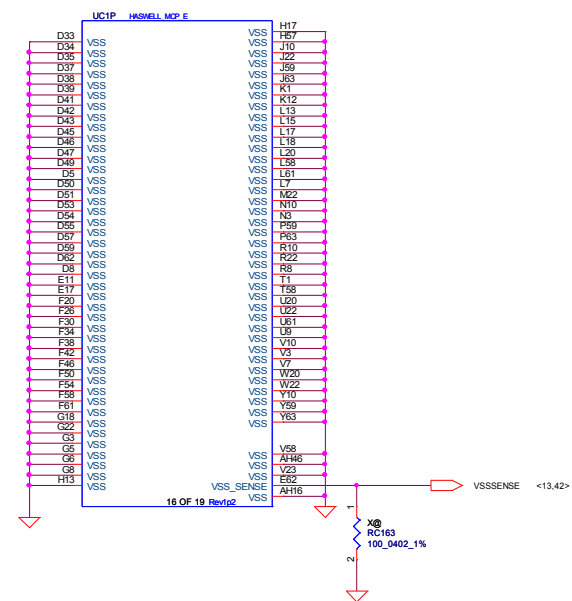
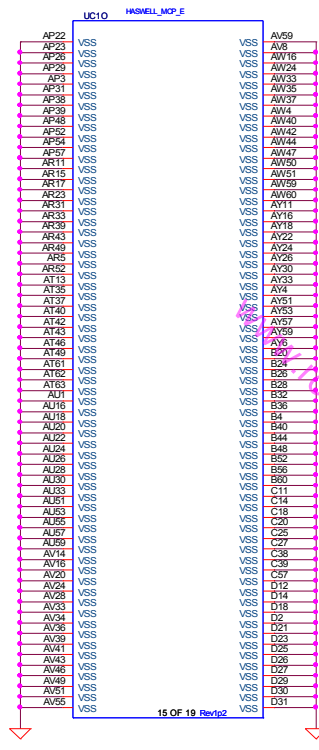
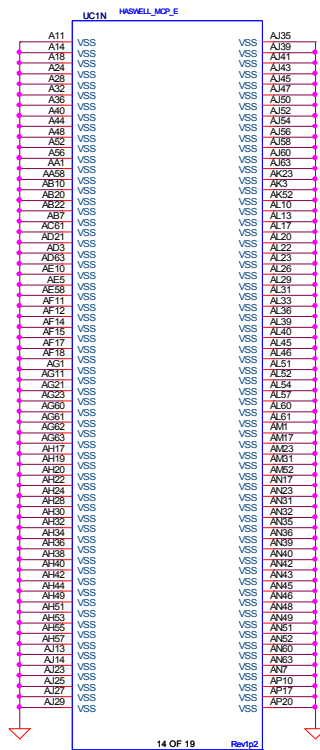






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				Size	Document Number	Rev
				LA-9982P		3.0
Date	Wednesday, May 29, 2013	Sheet	13	of	57	

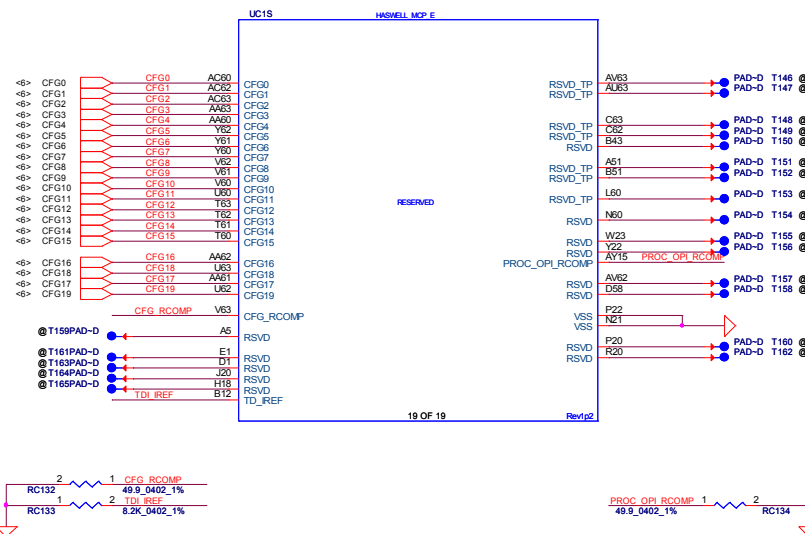
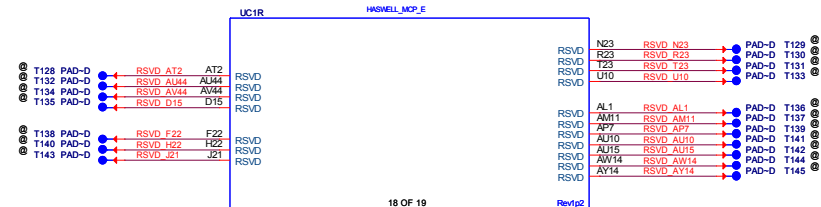
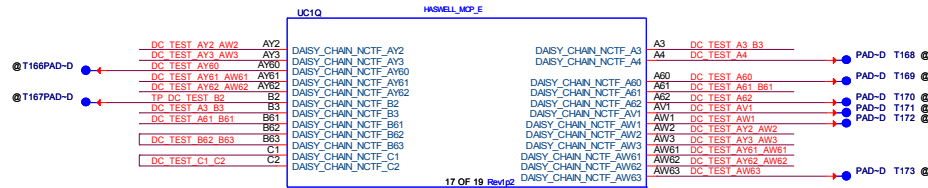




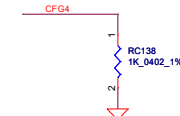
CAD Note: RC163 SHOULD BE PLACED CLOSE TO CPU

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					LA-9982P
				Date	Wednesday, May 29, 2013
				Sheet	15 of 57
				Rev	3.0



CFG STRAPS for CPU



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

H=4mm

2-3A to 1 DIMMs/channel

Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

<7> DDR_A_DQS[0..7]
<7> DDR_A_DQ[0..63]
<7> DDR_A_DQS[0..7]
<7> DDR_A_MA[0..15]

All VREF traces should have 10 mil trace width

Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

<18> DDR3_DRAMRST# <6> DDR3_DRAMRST#_CPU

DDR3L SODIMM ODT GENERATION

Place CC31 between QD2 and R2349

Layout Note:
Place near JDIMM1.203,204

<6> DDR_PG_CTRL

<18,19,26,27,6,9>
<18,19,26,27,6,9>

ESD solution

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Issued On		Deciphered Date		DDR3L DIMMA	
2013/05/29		2014/06/01		Document Number	
LA-9982P		Rev		3.0	
Date		Wednesday, May 29, 2013		Sheet	
17		of		57	

H=4mm
2-3A to 1 DIMMs/channel

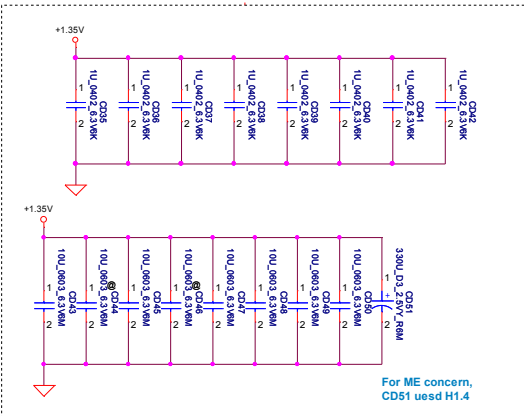
Populate RD4, De-Populate RD8 for Intel DDR3
VREFDQ multiple methods M1
Populate RD8, De-Populate RD4 for Intel DDR3
VREFDQ multiple methods M3

<7> DDR_B_DQS#0[0..7]
<7> DDR_B_DQ[0..63]
<7> DDR_B_DQS#0[0..7]
<7> DDR_B_MA[0..15]

All VREF traces should
have 10 mil trace width

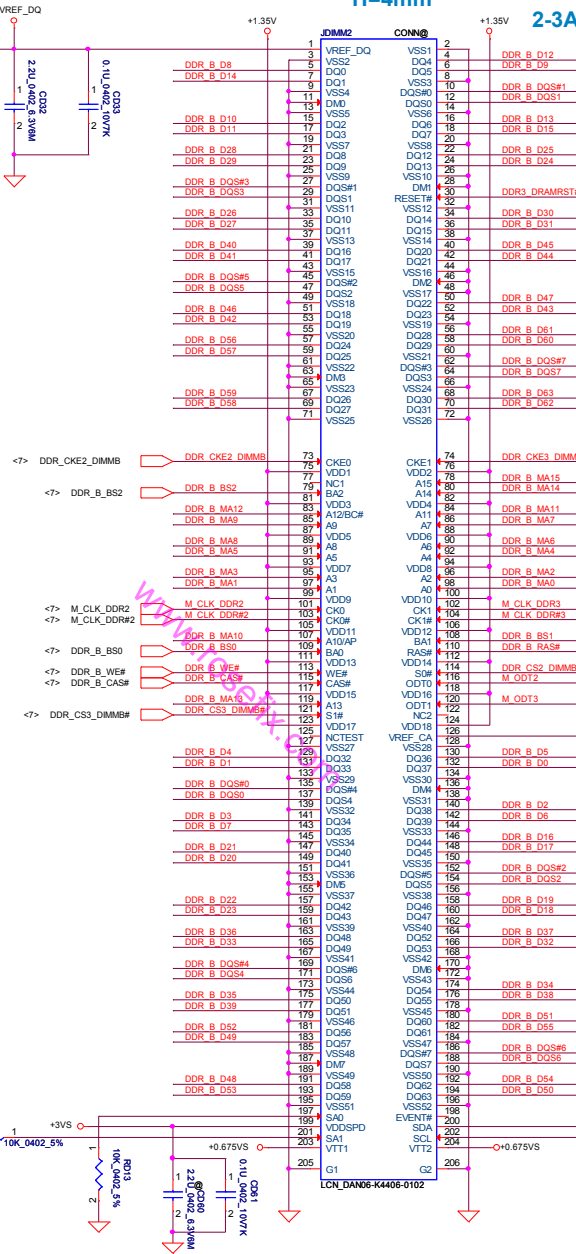
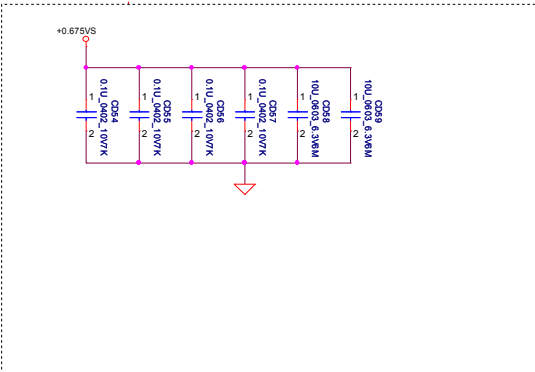
Layout Note:
Place near JDIMM2

Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

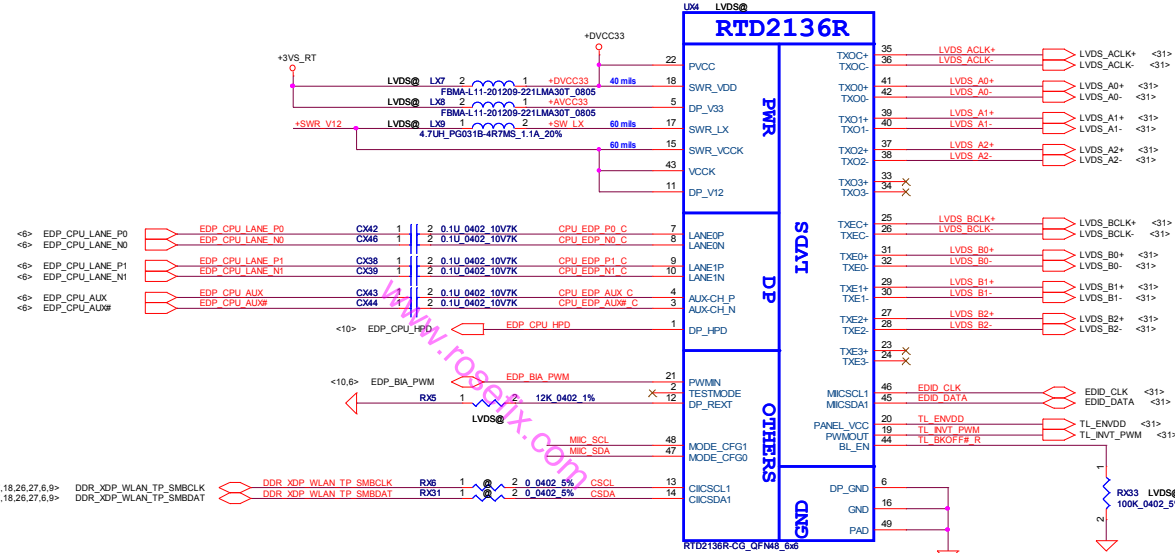
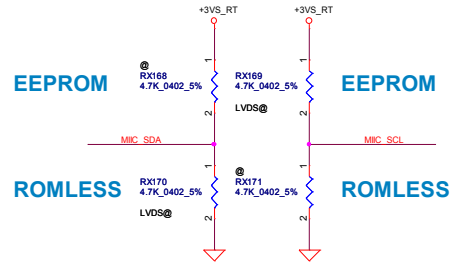
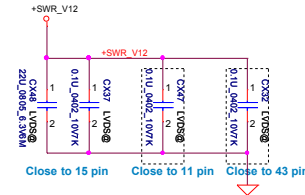
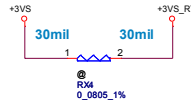
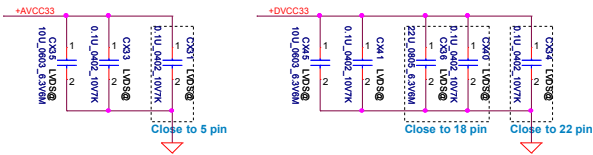


For ME concern,
CDS1 used H1.4

Layout Note:
Place near JDIMM2.203,204

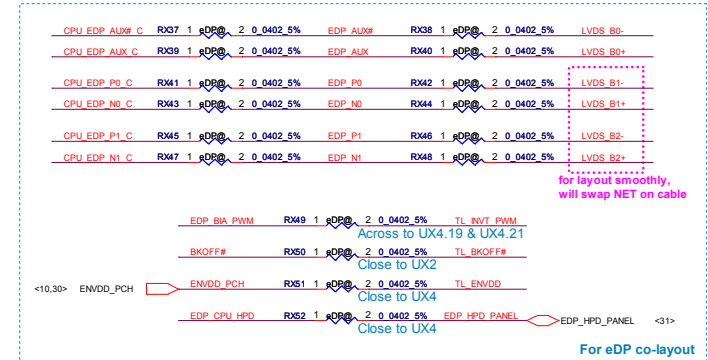
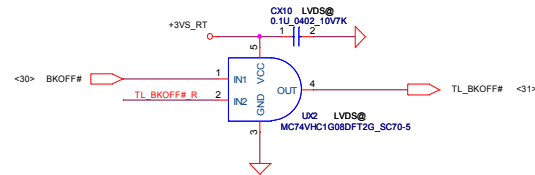


CAD NOTE
PLACE THE CAP NEAR TO
DIMM RESET PIN



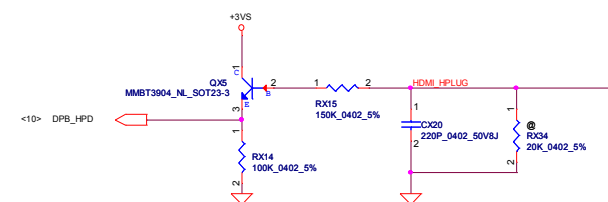
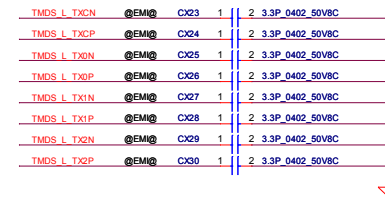
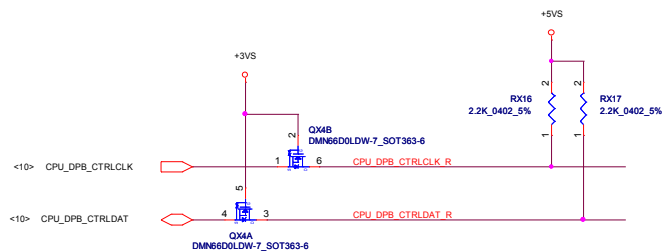
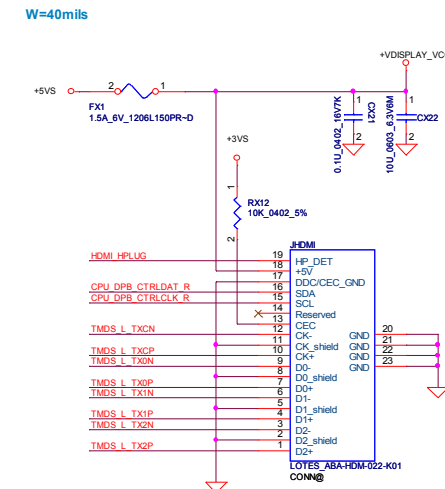
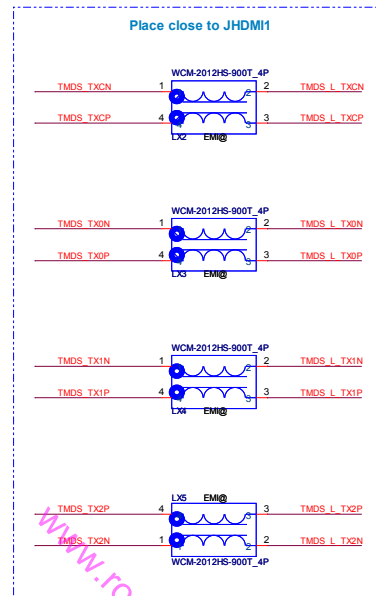
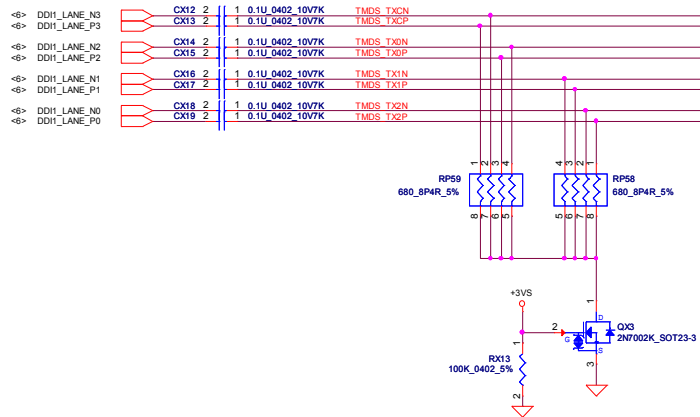
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RTD2136R : SA000067100

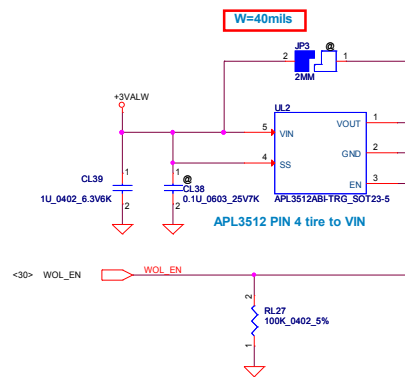
Vendor advise reserve it



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Security Classification		Compal Secret Data		Title	
Issued Date	2013/05/29	Deciphered Date	2014/06/01	eDP to LVDS converter	
Document Number	LA-9982P	Rev	3.0	Date: Wednesday, May 29, 2013	
Sheet		19		of 57	

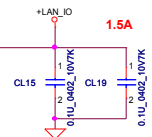




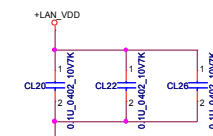
SS table

Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

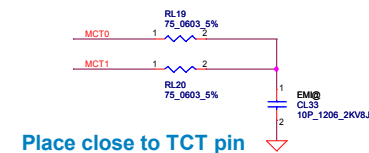
W=40mils +LAN_IO rising time : >1ms and <100ms



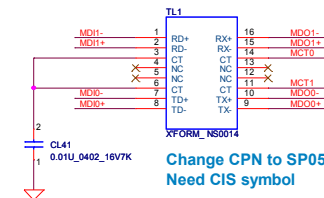
These caps close to Pin 23,32
For 8106E pop the capacitor close pin 23,32



These caps close to Pin 8,30
For 8106E pop capacitor close to pin 8,30

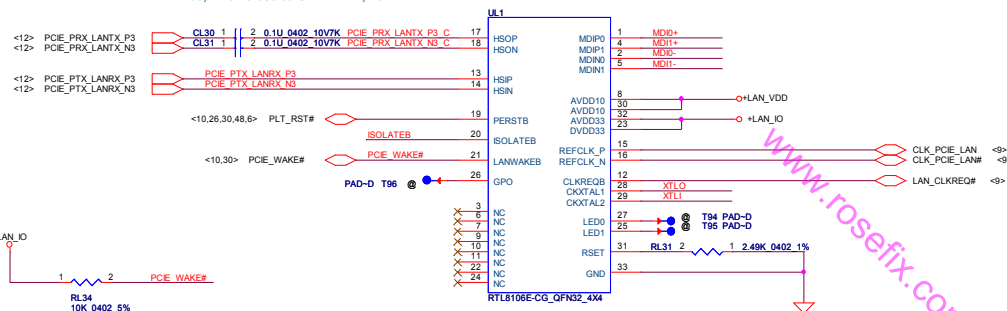


Place close to TCT pin

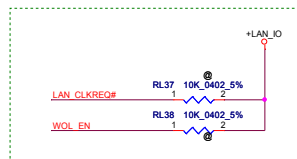
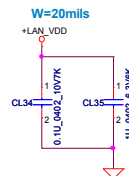
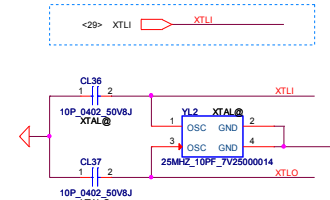


Change CPN to SP050007J00 only
Need CIS symbol

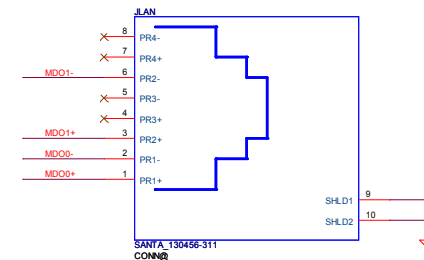
CL30, CL31 close to UL1 Pin 17, 18



For GCLK



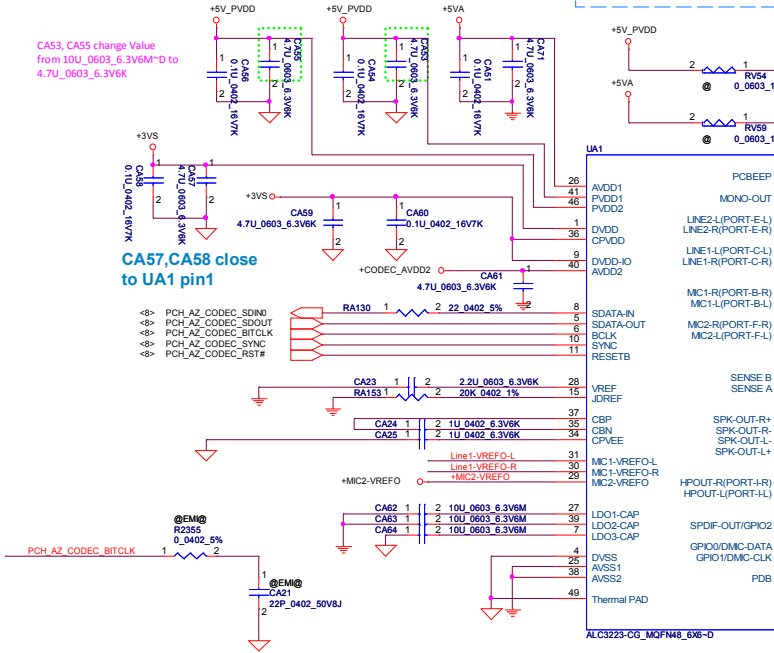
Reserve 10K pull LAN_IO



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Issued Date	2013/05/29	Deciphered Date	2014/06/01	LAN RTL8106E
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Date:	Wednesday, May 29, 2013	Sheet	21	of 57

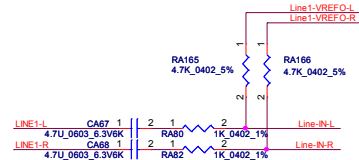
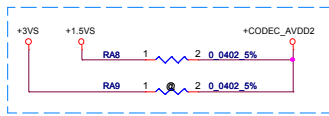
CA71, CA51 place close to Pin 26

CA53, CA55 change Value from 10U_0603_6.3V6M to 4.7U_0603_6.3V6K

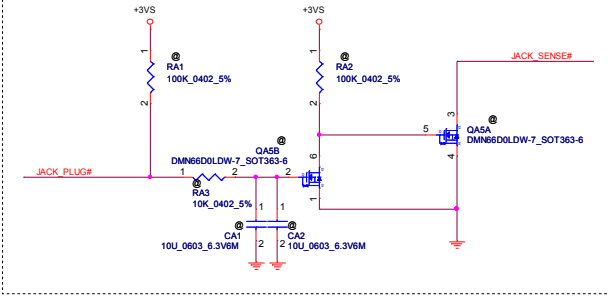


CA57, CA58 close to UA1 pin1

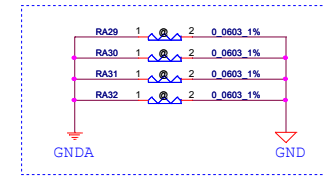
Reserve for HDA issue



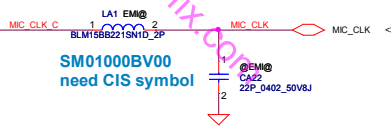
JACK_PLUG Delay circuitis



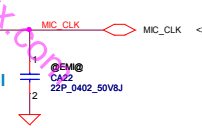
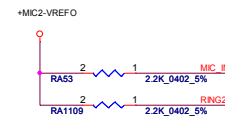
Reserve for cancel Delay circuitis



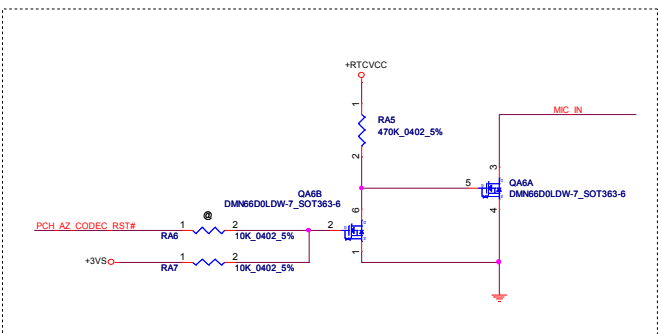
Place on the moat between GND & GNDA.



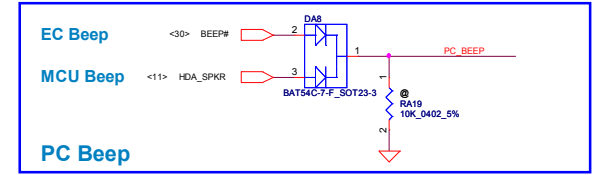
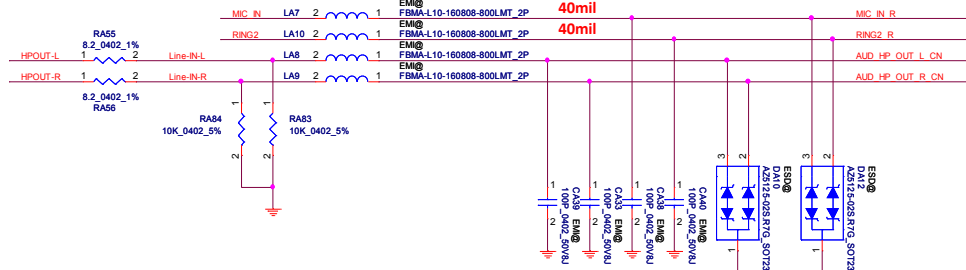
RA51, RA33 place close to UA1



RA51, RA33 place close to UA1

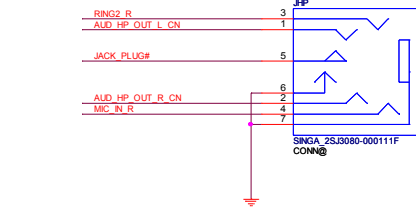
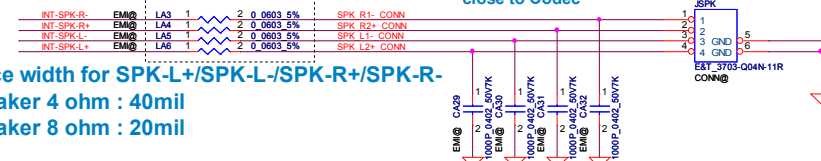


iPhone and Nokia type Combo Jack



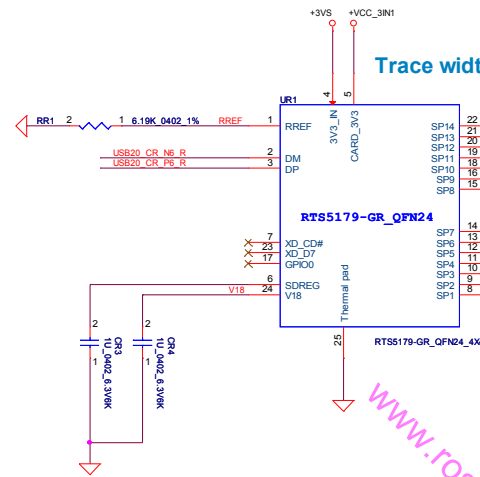
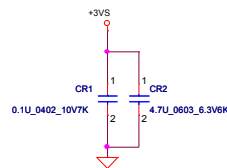
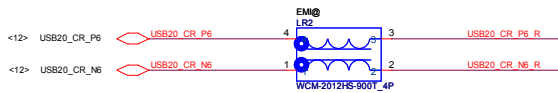
Close to UA1 Pin11,13,14,16

Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R- Speaker 4 ohm : 40mil Speaker 8 ohm : 20mil

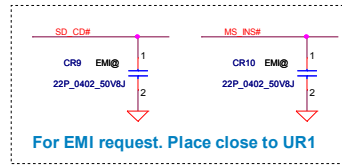


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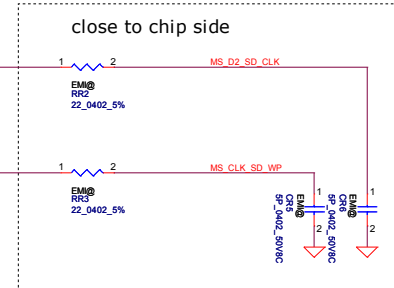
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Issue Date		Deciphered Date		2014/06/01	
2013/05/29		2014/06/01		Compal Electronics, Inc.	
2013/05/29		2014/06/01		Audio Codec ALC3223	
2013/05/29		2014/06/01		Size	
2013/05/29		2014/06/01		Document Number	
2013/05/29		2014/06/01		LA-9982P	
2013/05/29		2014/06/01		Date	
2013/05/29		2014/06/01		Wednesday, May 29, 2013	
2013/05/29		2014/06/01		Sheet	
2013/05/29		2014/06/01		22 of 57	
2013/05/29		2014/06/01		Rev	
2013/05/29		2014/06/01		3.0	



Trace width:40mil



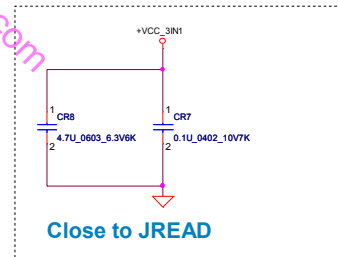
For EMI request. Place close to UR1



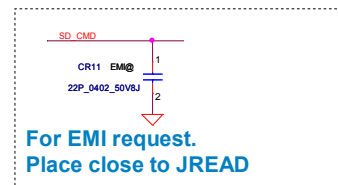
close to chip side

拉MS_D2_SD_CLK到Conn pin 13 SD_CLK
再打Via拉到pin 10 MS_D2

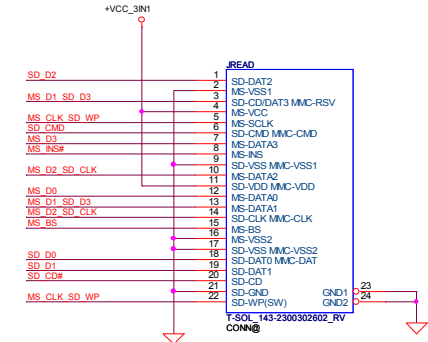
拉MS_CLK_SD_WP到Conn pin 5 MS_CLK
再打Via拉到pin 20 SD_W



Close to JREAD

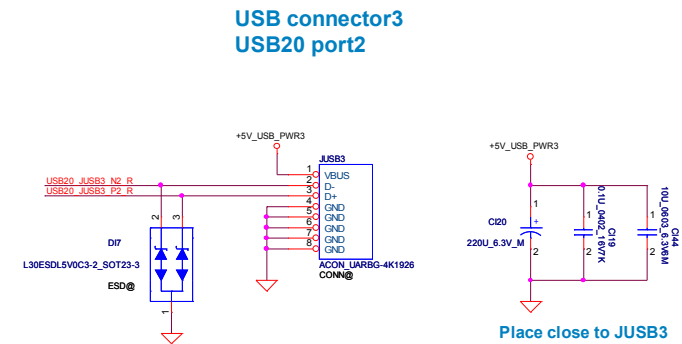


For EMI request.
Place close to JREAD



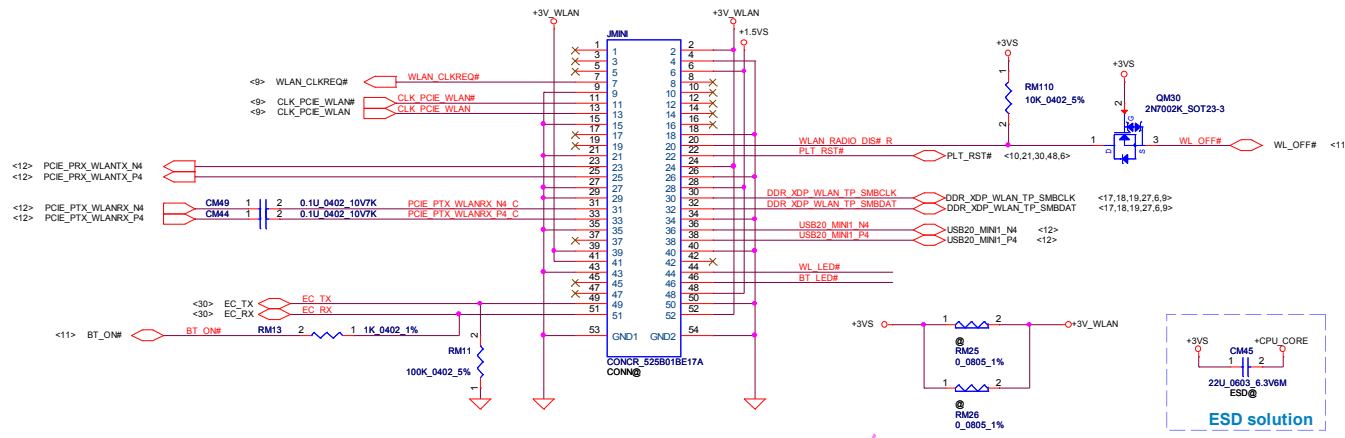
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Issue Date	2013/05/29	Deciphered Date	2014/06/01	Title	Card Reader RTS5179
Issue By	2013/05/29	Deciphered By	2014/06/01	Size	Document Number
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Date: Wednesday, May 29, 2013				Sheet	23 of 57

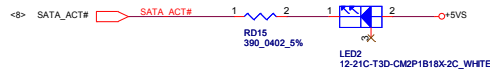


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				Size	Document Number	Rev
				LA-9982P		
Date:				Wednesday, May 29, 2013	Sheet	25 of 57

Mini WLAN/WIMAX H=6.7



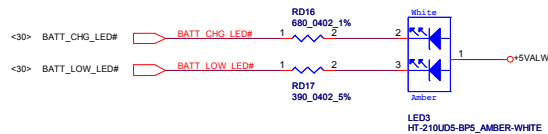
HDD LED



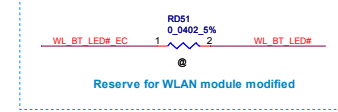
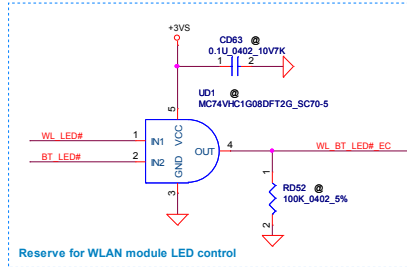
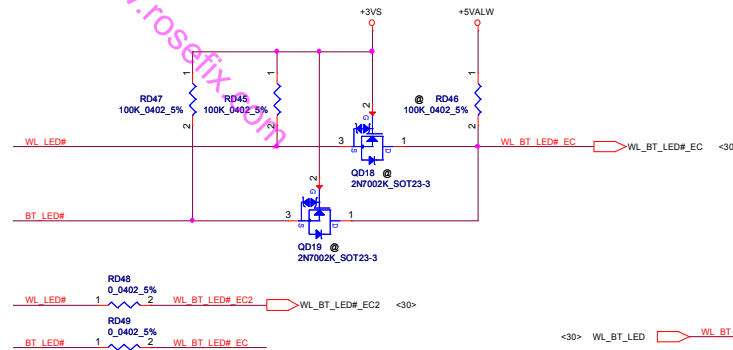
Power LED



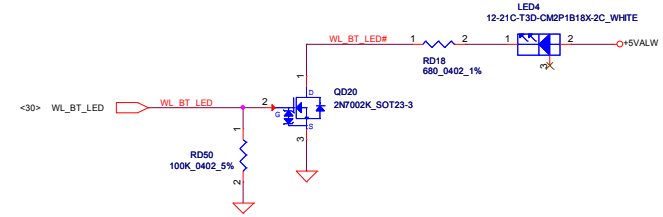
Battery LED



10mils, All pins

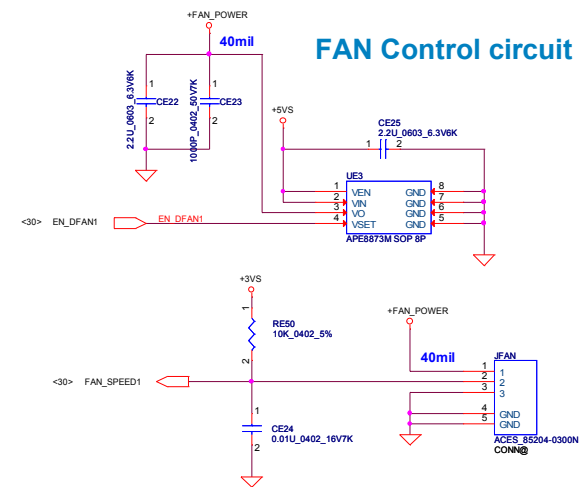
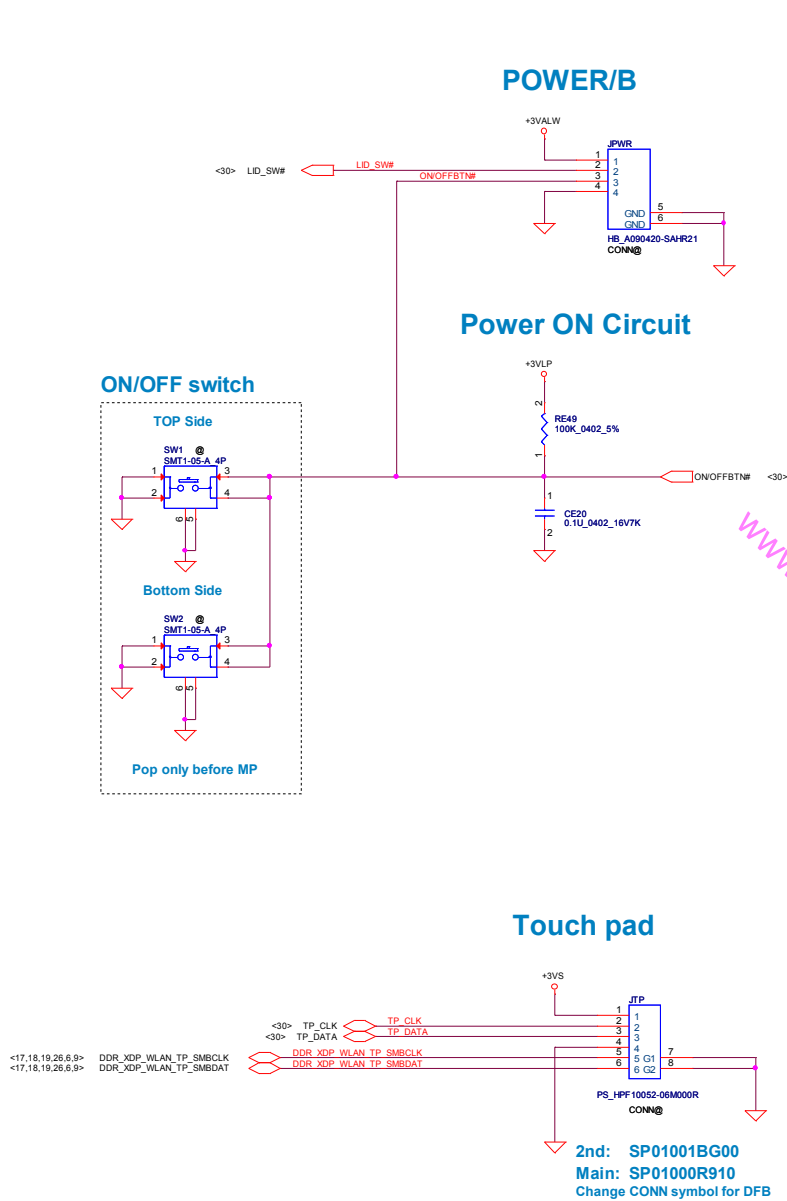


Wireless LED



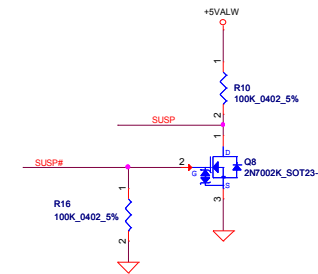
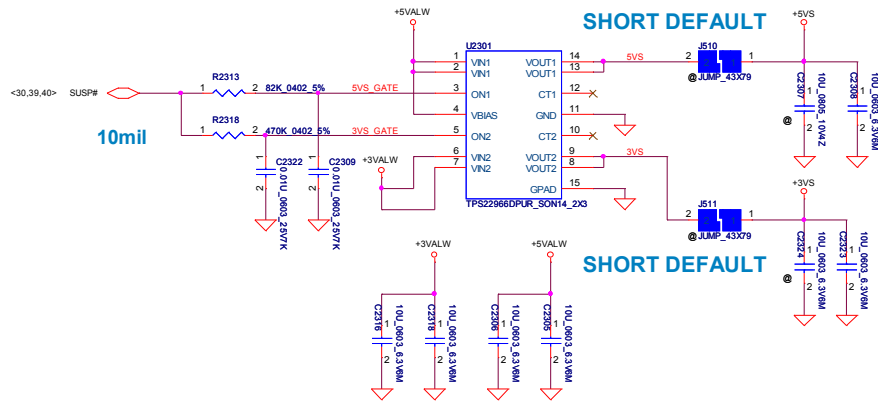
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				Date	Wednesday, May 29, 2013
				Sheet	26 of 57
				Rev	3.0

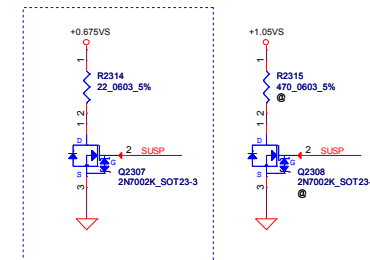
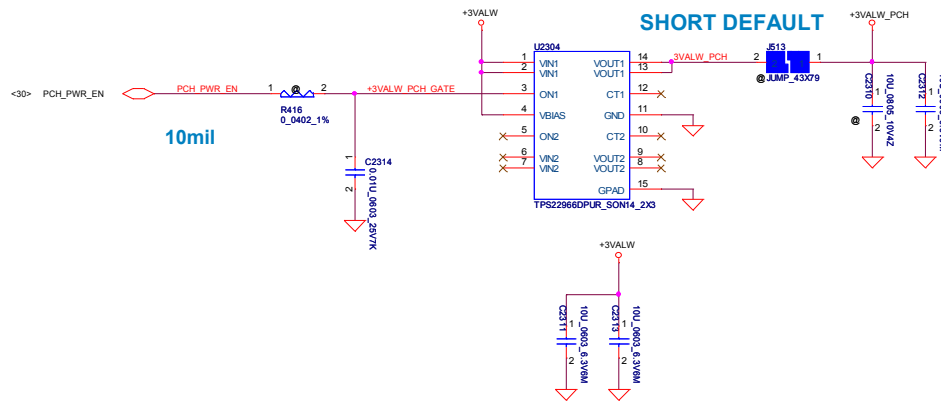


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				Date	Wednesday, May 29, 2013
				Sheet	27 of 57
				Rev	3.0

+5VS and +3VS switch



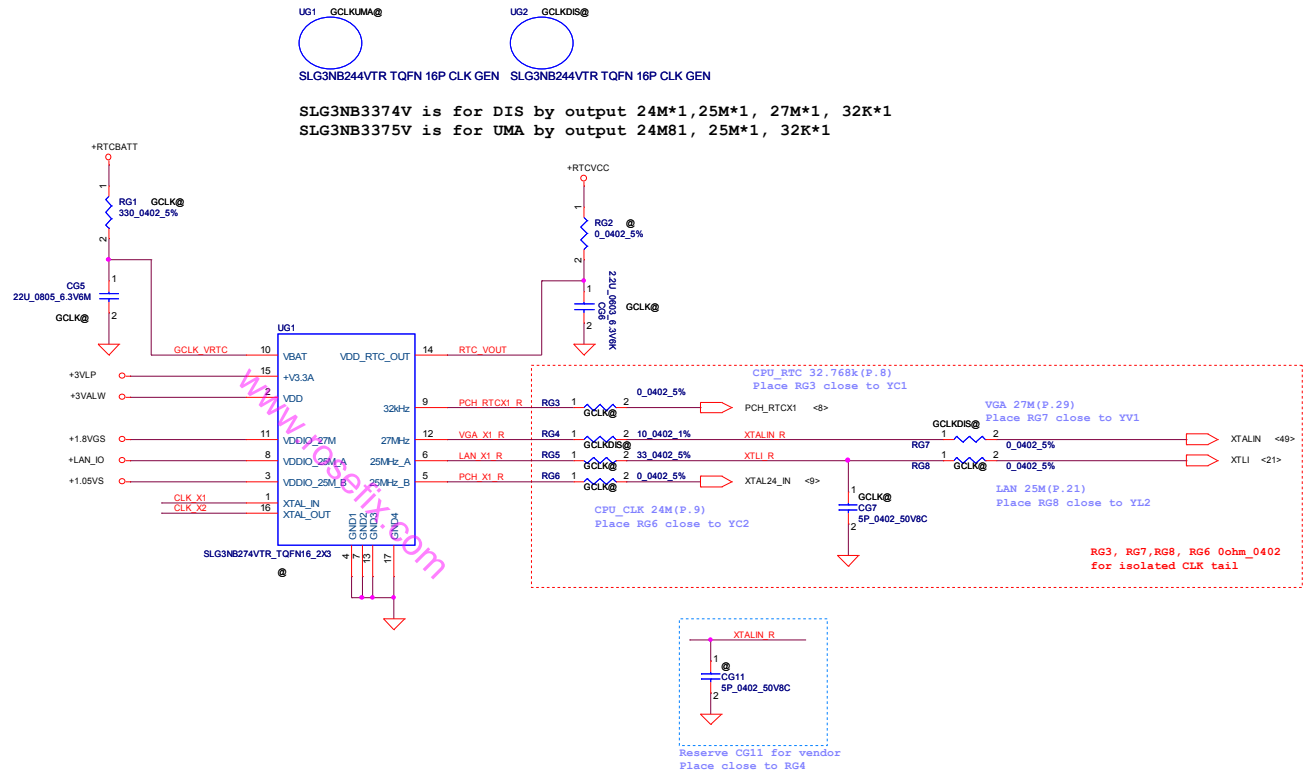
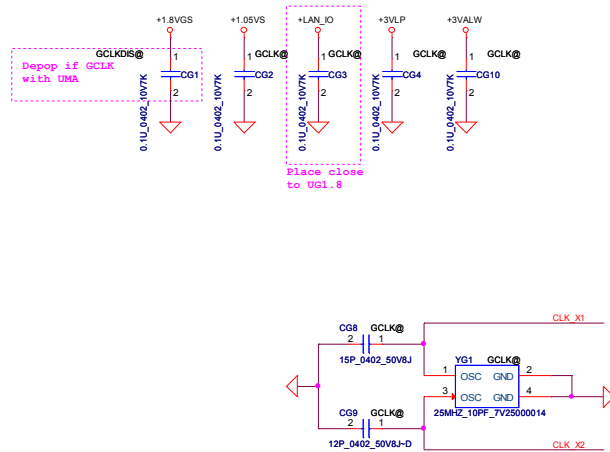
+3VALW_PCH switch

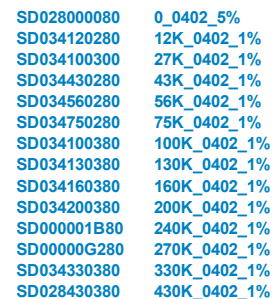


For Intel S3 Power Reduction

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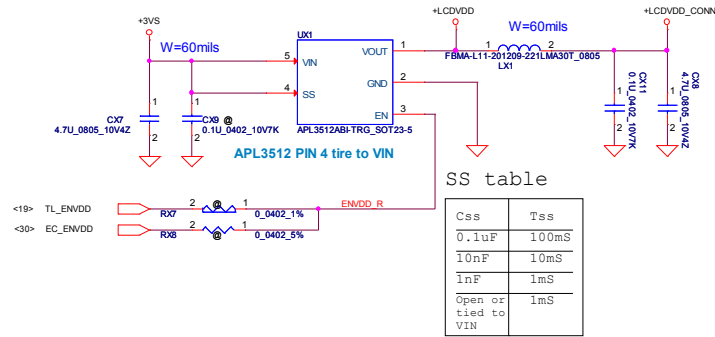
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Issue Date	2013/05/29	Deciphered Date	2014/06/01	Title	DC/DC Interface
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					LA-9982P
				Date	Wednesday, May 29, 2013
				Sheet	28 of 57
				Rev	3.0



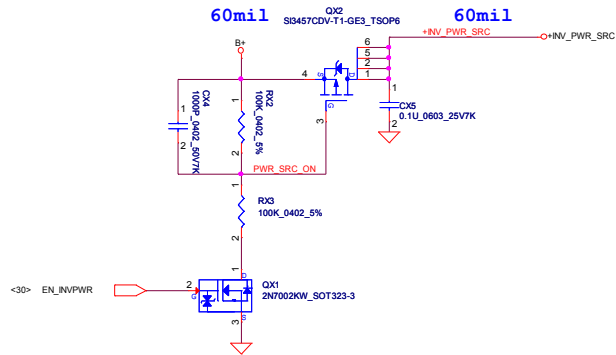


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				LA-9982P	Rev 3.0
Date	Wednesday, May 29, 2013	Sheet	30	of	57

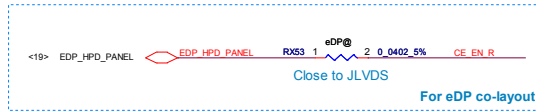
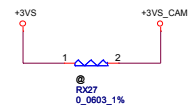
LCD PWR CTRL



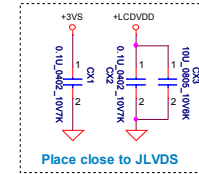
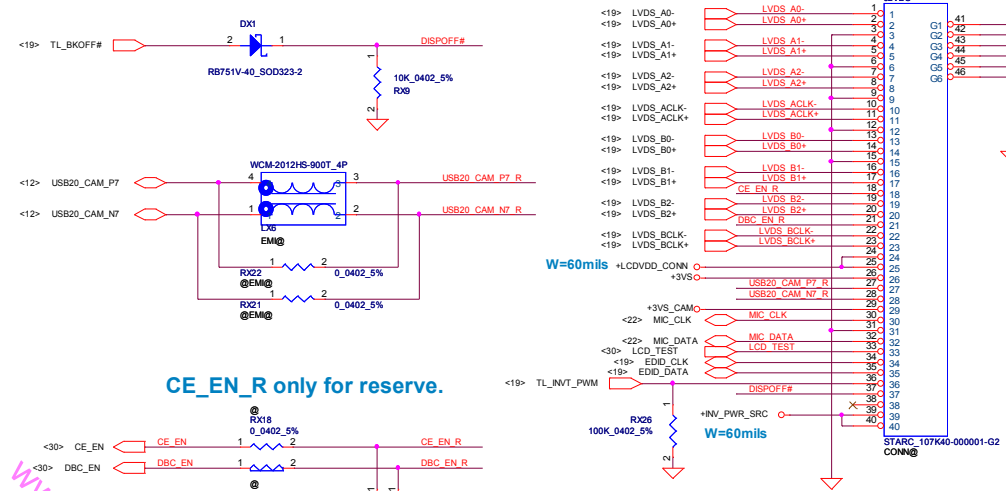
LCD backlight PWR CTRL



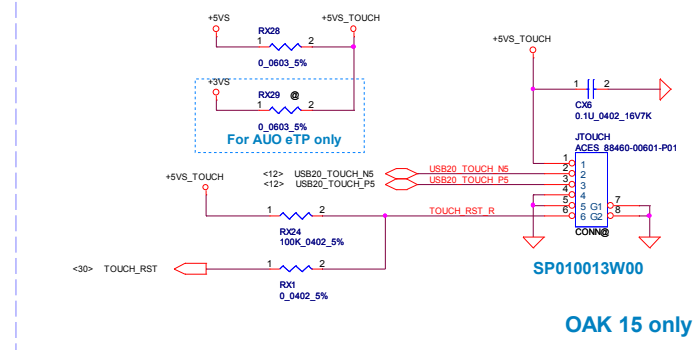
Webcam PWR CTRL



LVDS Connector

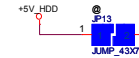


* Touch Screen Panel

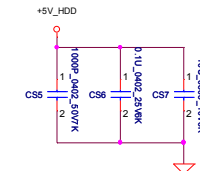
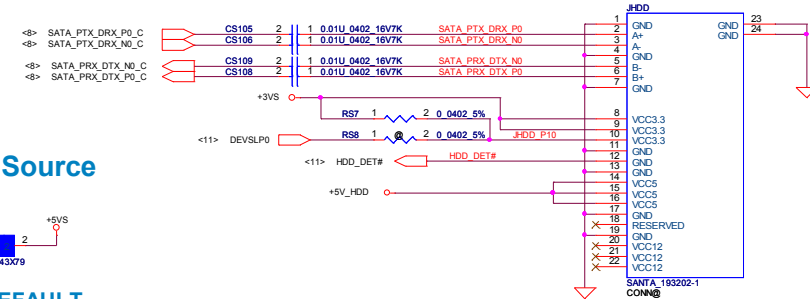


SATA HDD Connector

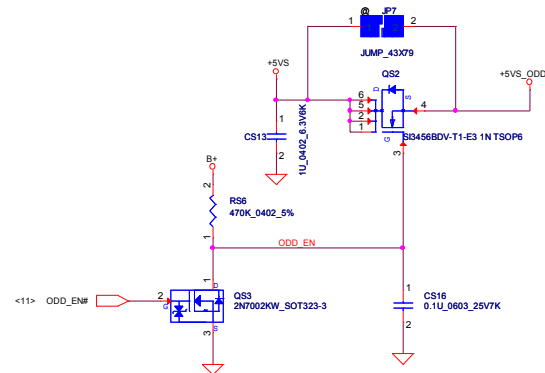
+5V_HDD Source



SHORT DEFAULT

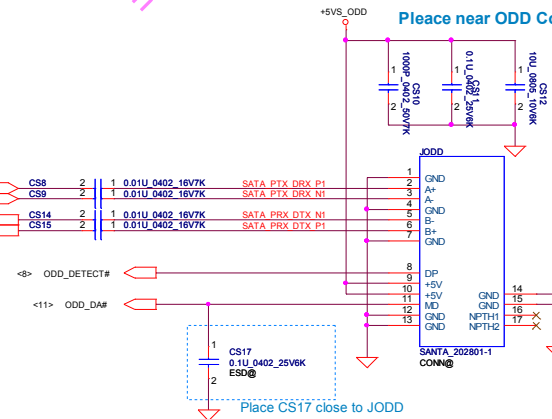


ODD Power Control

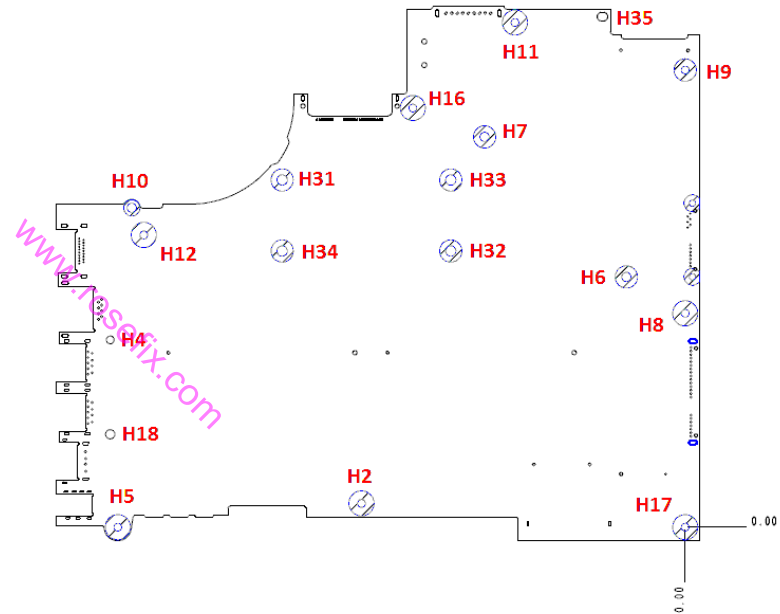
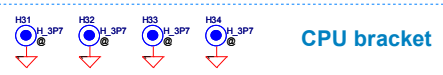
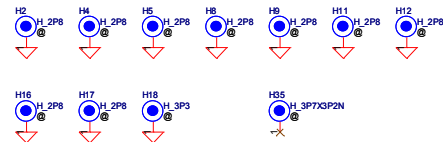


SATA ODD Connector

Place near ODD Connector



Screw Hole



Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	Card Reader	2012/04/27	HW	The Card reader USB signal is incorrect.	SWAP UR1 USB signal P/N	0.2
2							
3							
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www.rosefix.com

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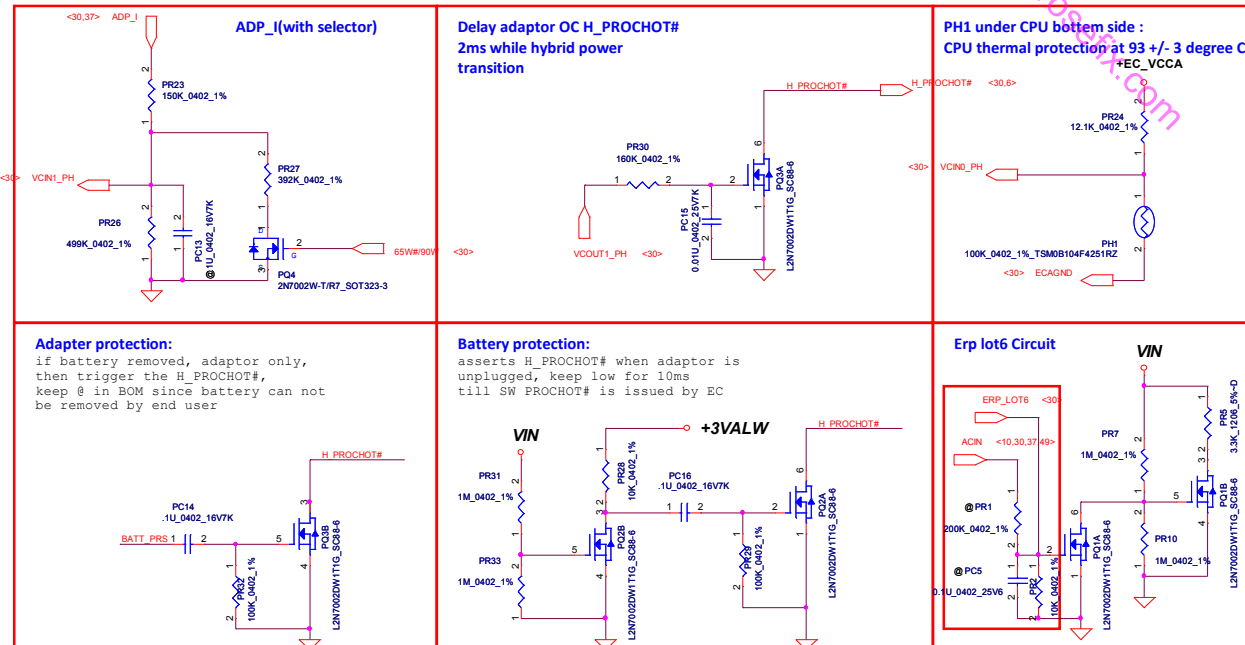
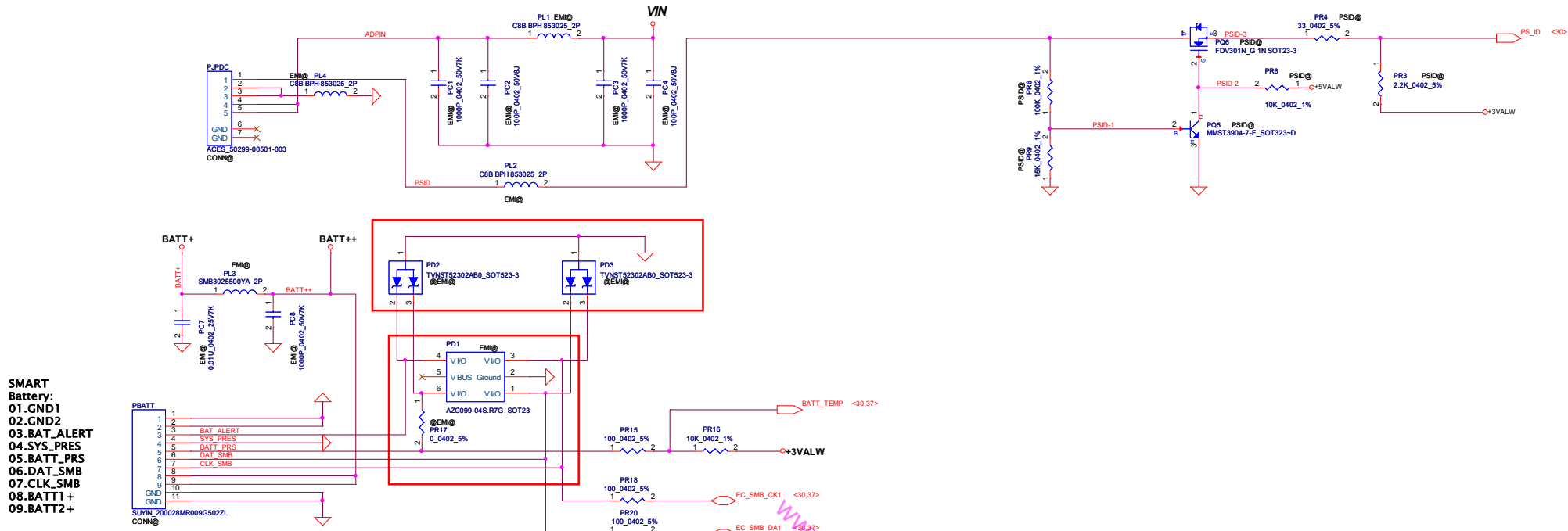
Security Classification		Compal Secret Data		Title	
Issue Date	2013/05/29	Deciphered Date	2014/06/01	HW-PIR Page.1	
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				LA-9982P	Rev 3.0
				Date: Wednesday, May 29, 2013	Sheet 34 of 57

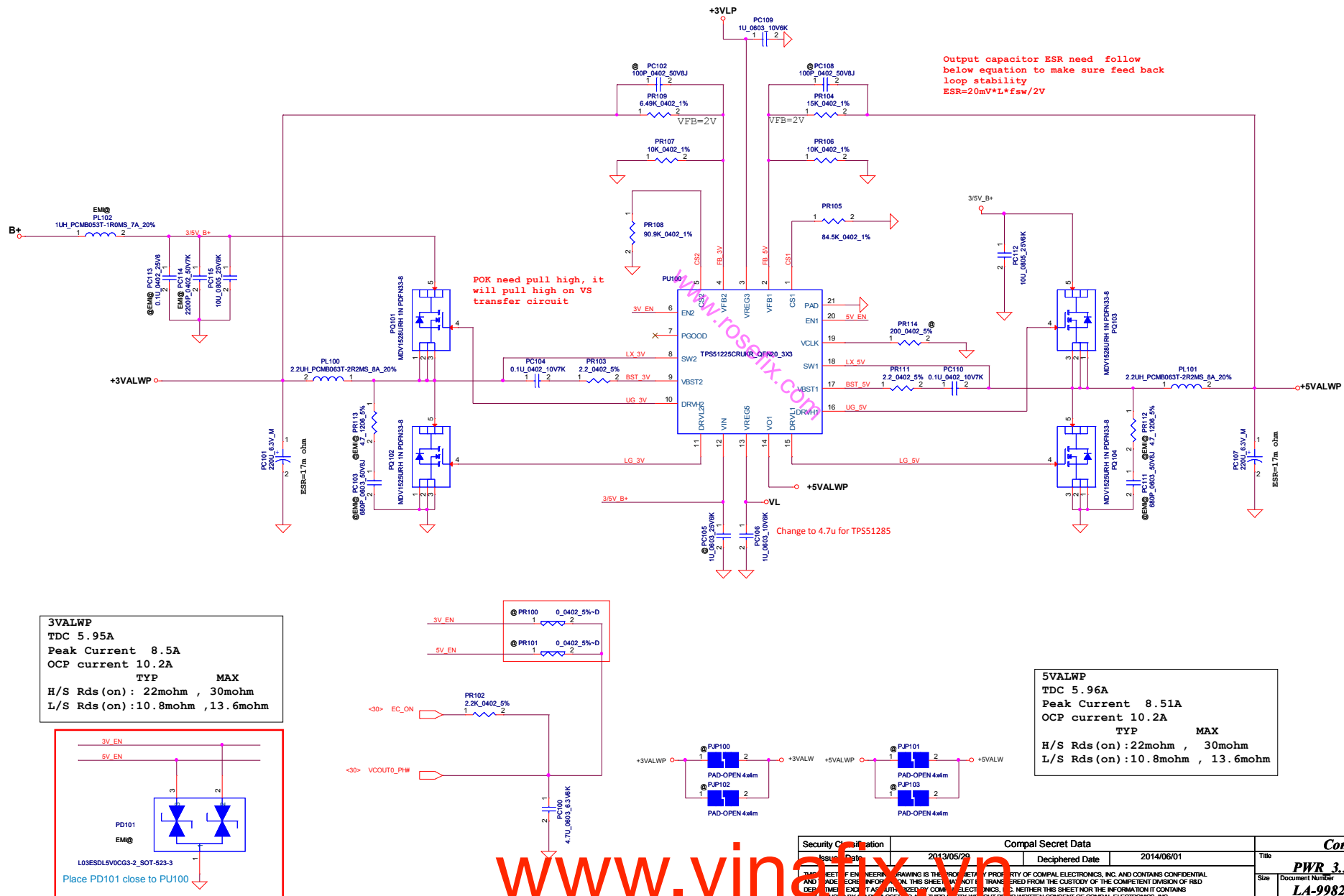
Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
40							
41							
42							
43							
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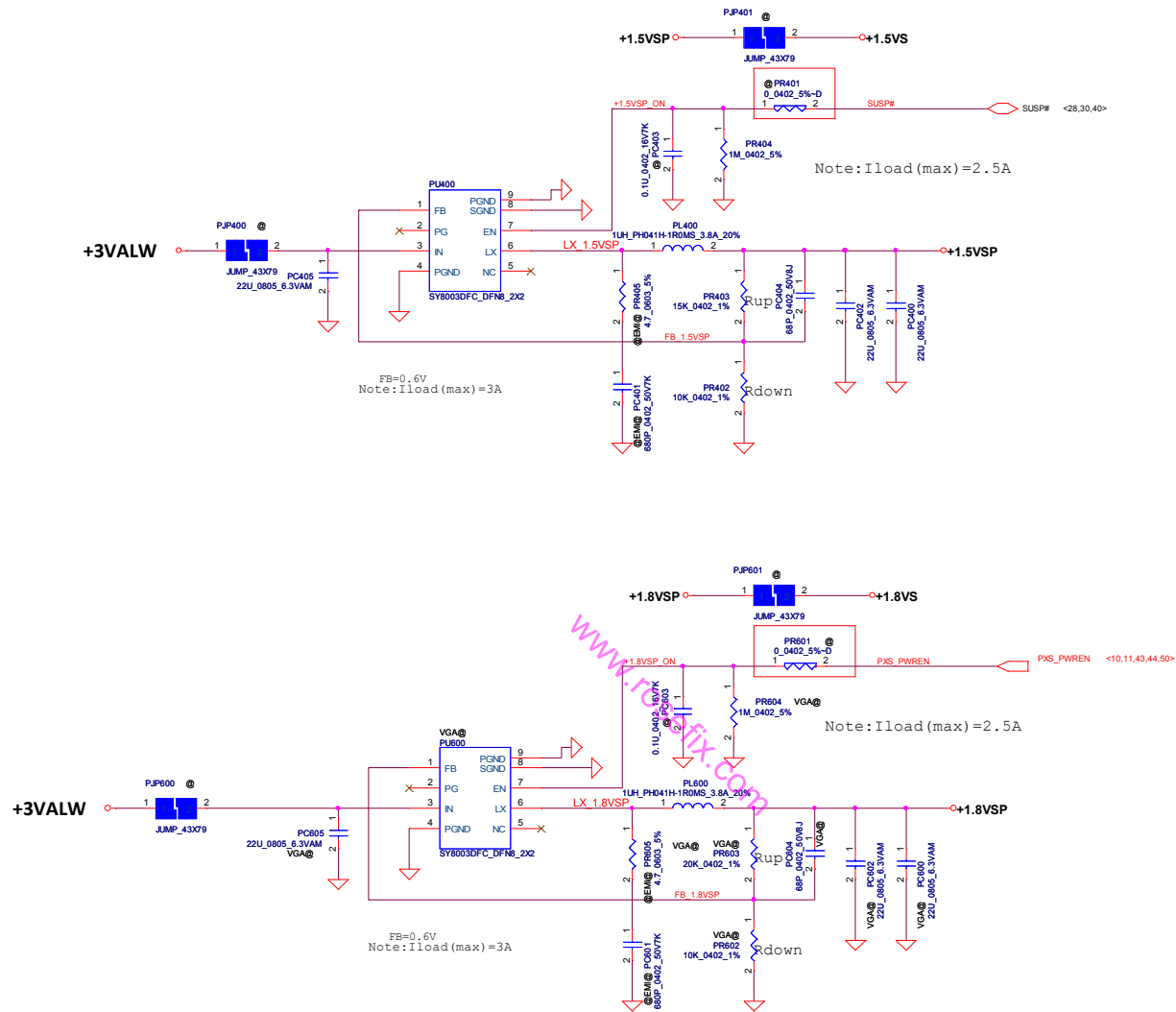
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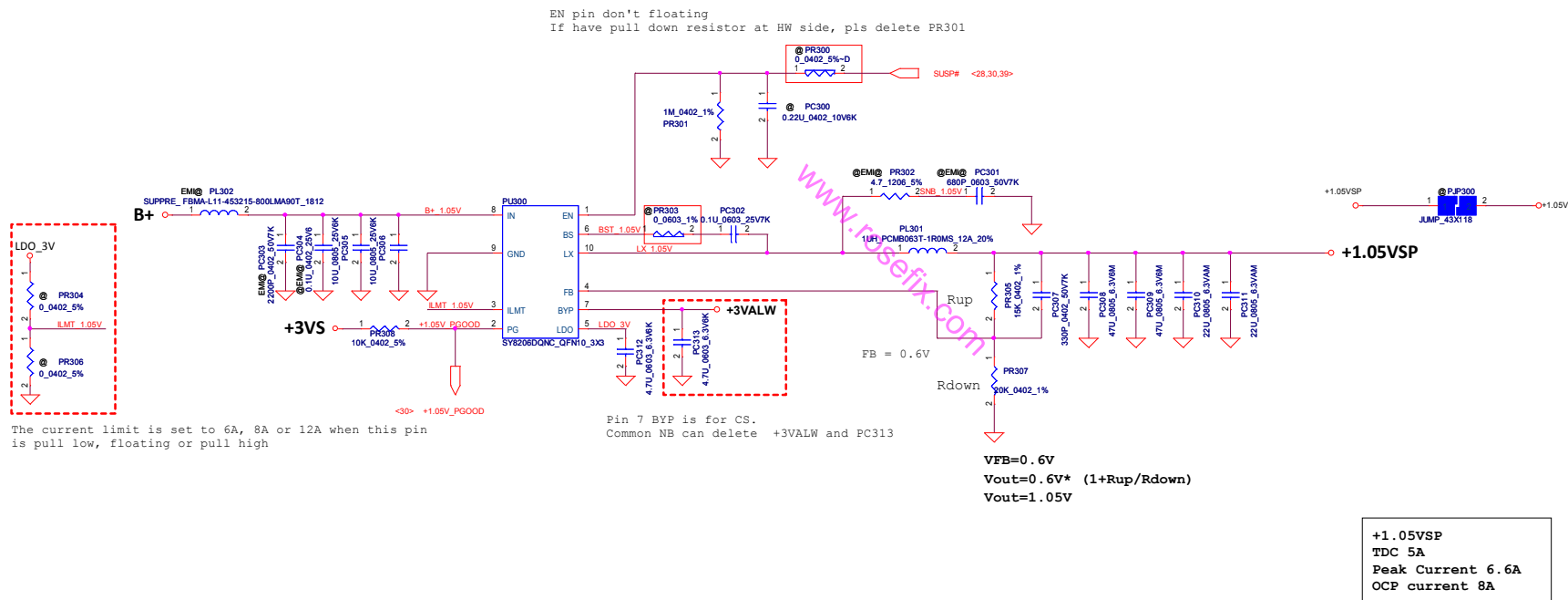
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Issue Date		Deciphered Date		Date	
2013/05/29		2014/06/01		Wednesday, May 29, 2013	
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Document Number				3.0	
LA-9982P				Sheet 35 of 57	

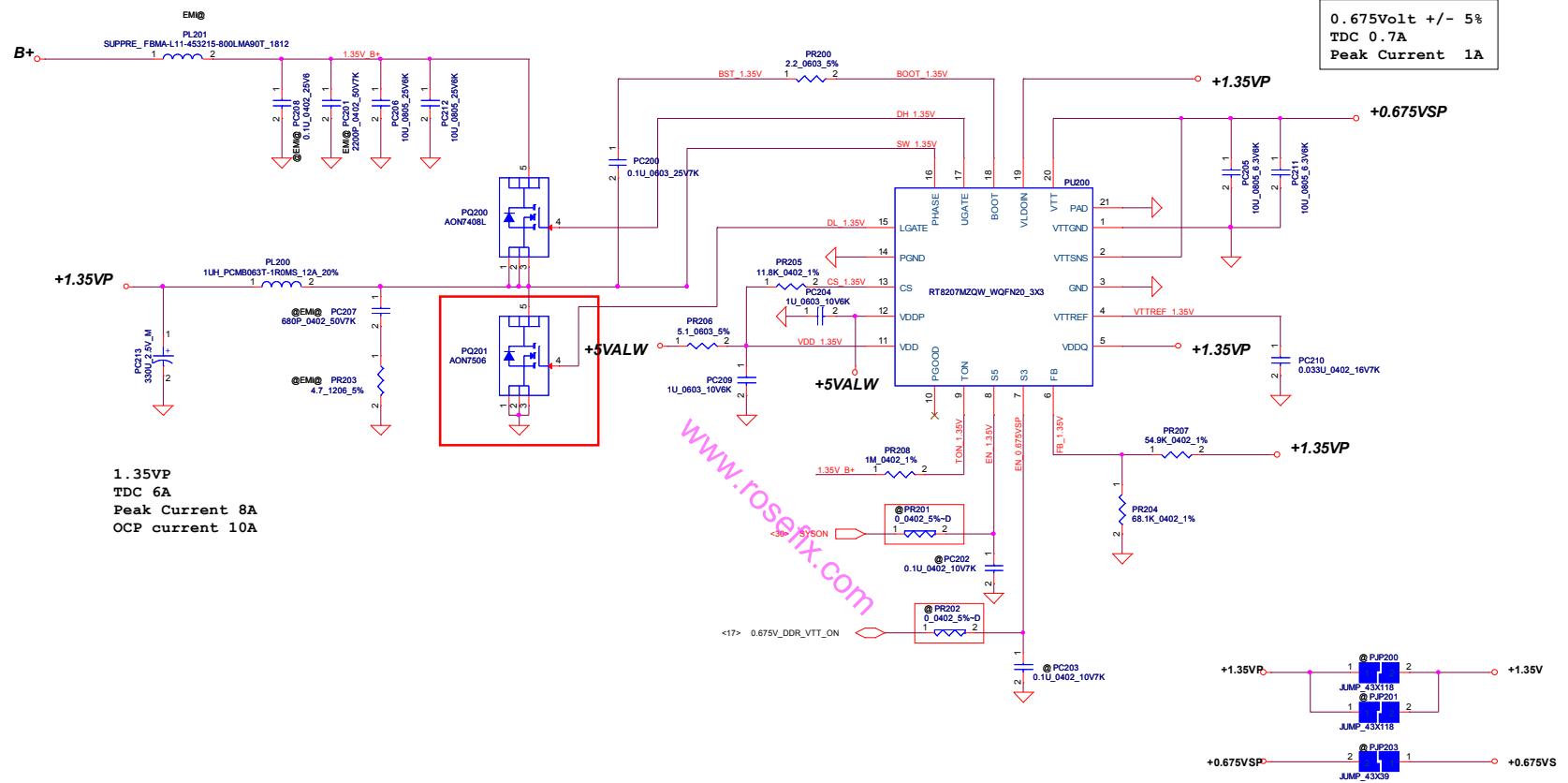




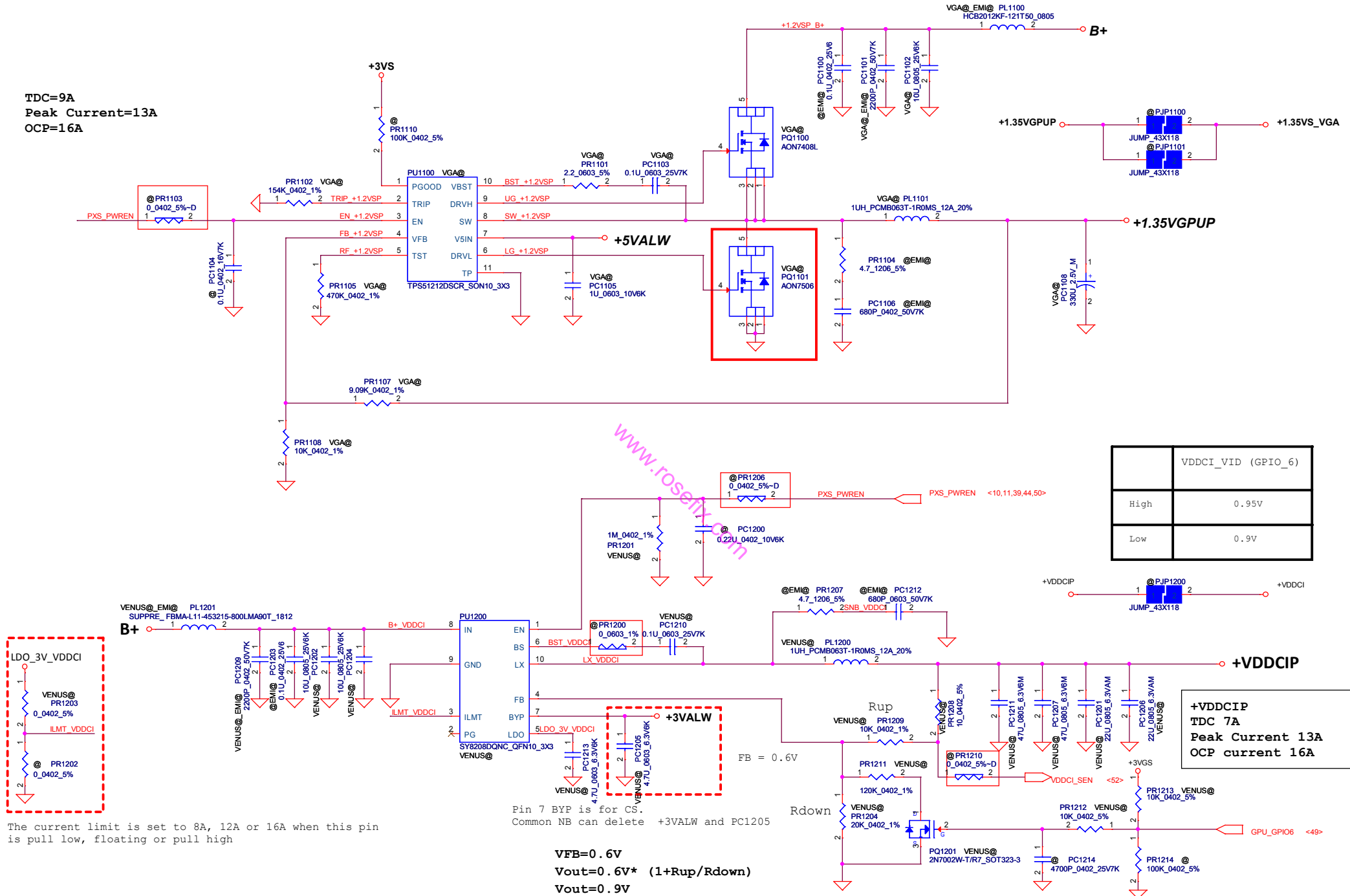
Security Classification		Compal Secret Data		Title	
Issue Date	2013/05/29	Deciphered Date	2014/06/01	Document Number	PWR_3.3VALWP/SVALWP
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Date: Wednesday, May 29, 2013				Sheet	38 of 57



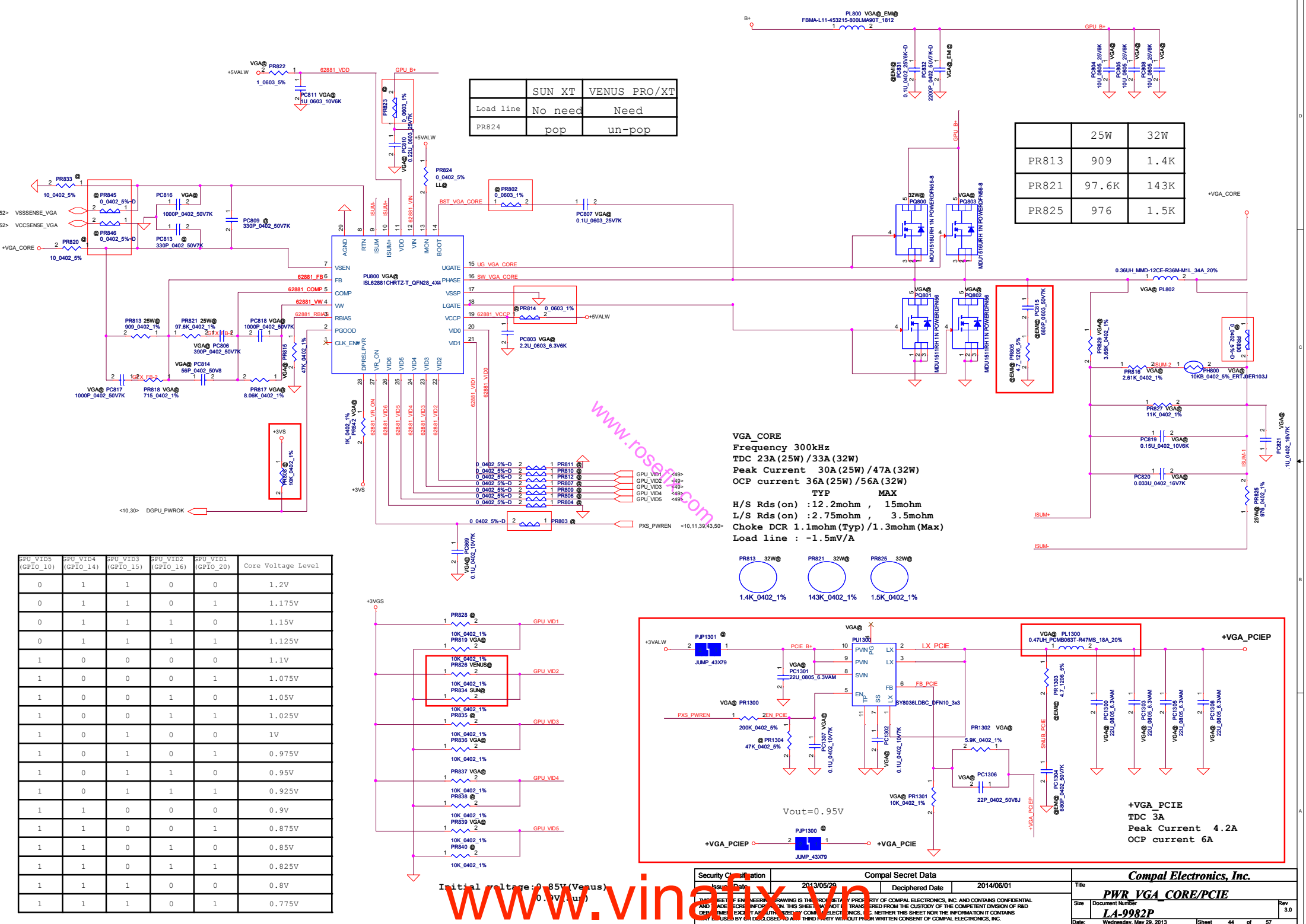




TDC=9A
Peak Current=13A
OCP=16A



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Issued Date	2013/05/29	Deciphered Date	2014/06/01	Title	PWR +1.35VGPU/VDDCIP
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					LA-9982P
				Date	Wednesday, May 29, 2013
				Sheet	43 of 57
				Rev	3.0



	SUN XT	VENUS PRO/XT
Load line	No need	Need
PR824	pop	un-pop

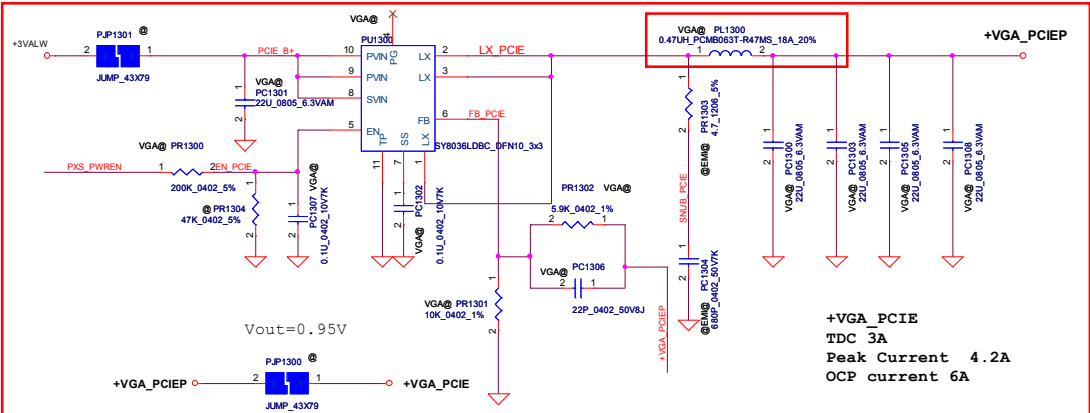
	25W	32W
PR813	909	1.4K
PR821	97.6K	143K
PR825	976	1.5K

VGA_CORE
Frequency 300kHz
TDC 23A (25W) / 33A (32W)
Peak Current 30A (25W) / 47A (32W)
OCP current 36A (25W) / 56A (32W)
TYP MAX
H/S Rds(on) : 12.2mohm , 15mohm
L/S Rds(on) : 2.75mohm , 3.5mohm
Choke DCR 1.1mohm (Typ) / 1.3mohm (Max)
Load line : -1.5mV/A

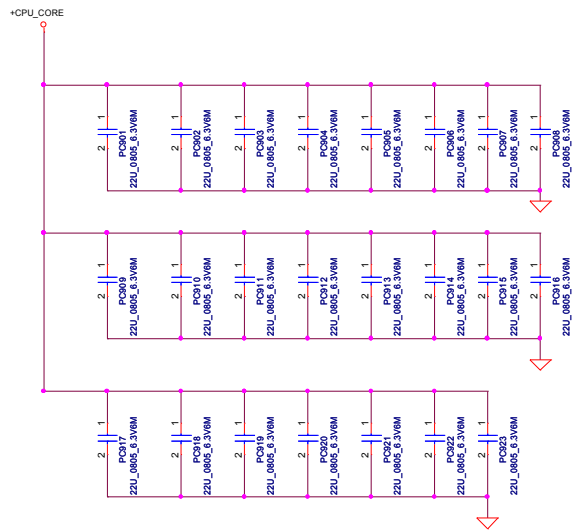


SPU_VID5 (GPIO_10)	SPU_VID4 (GPIO_14)	SPU_VID3 (GPIO_15)	SPU_VID2 (GPIO_16)	SPU_VID1 (GPIO_20)	Core Voltage Level
0	1	1	0	0	1.2V
0	1	1	0	1	1.175V
0	1	1	1	0	1.15V
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V
1	1	1	1	1	0.775V

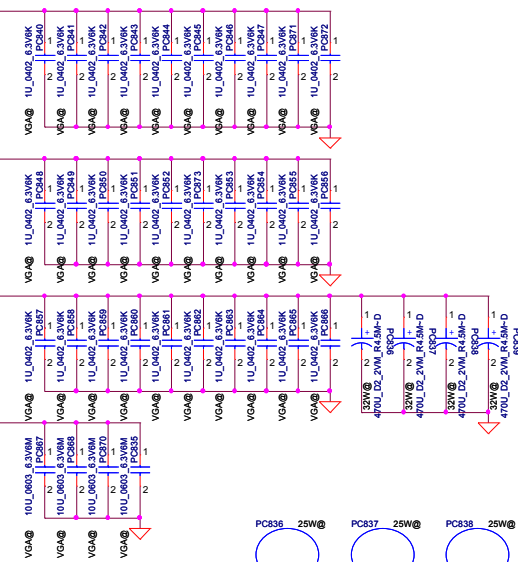
Initial voltage: 0.85V (Venus)
0.7V (Sun)



+VGA_PCIE
TDC 3A
Peak Current 4.2A
OCP current 6A



+VGA_CORE

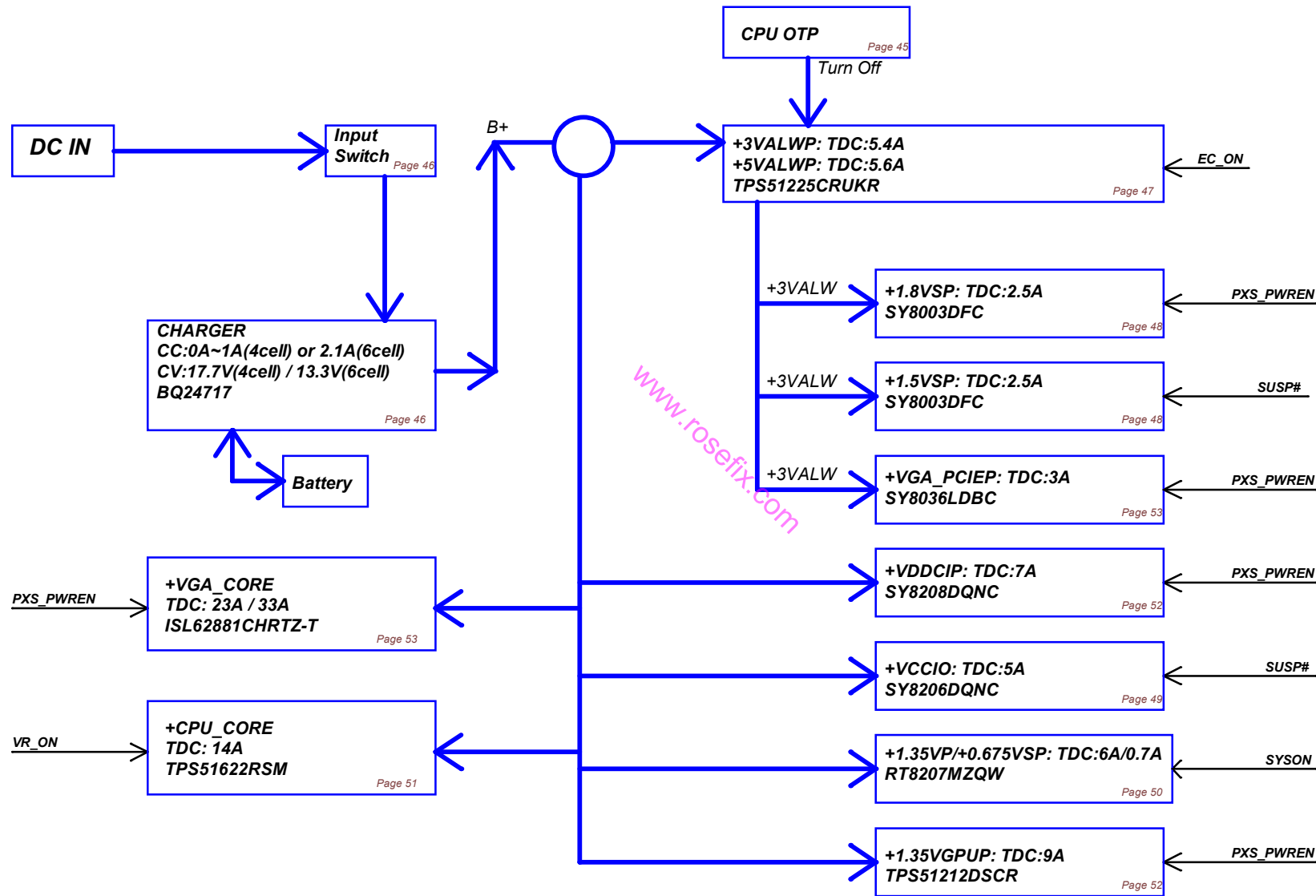


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Issue Date	2013/05/29	Deciphered Date	2014/06/01	PWR PROCESSOR DECOUPLING	
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					LA-9982P
				Date	Wednesday, May 29, 2013
				Sheet	45 of 57
				Rev	3.0

Power block



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Issue Date	2013/05/29	Deciphered Date	2014/06/01	Title	PWR POWER BLOCK DIAGRAM
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				Date	Wednesday, May 29, 2013
				Sheet	46 of 57
				Rev	3.0

Version Change List (P. I. R. List)

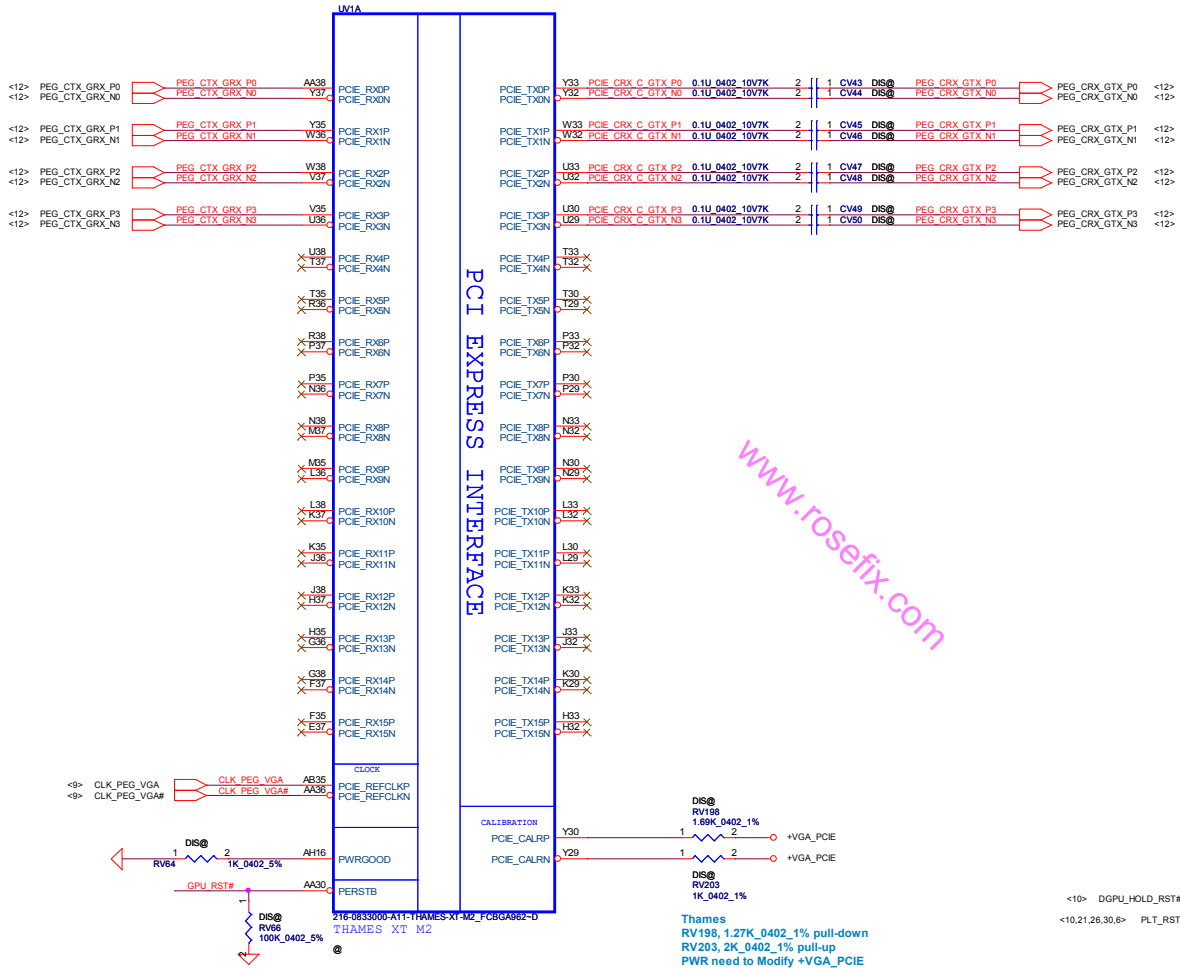
Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	CHARGER	13/01/30	Morris	adjust design parameter from vendor recommend	delete PD702 change PC712 to unpop change PQ704 to unpop change PC707 from 0.1uF 0402 to 1uF_0603 change PC720 from 0.1uF to 100pF change PC711 from 1000pF to 0.01uF change PQ705 from SB00000SD00 to SB00000WY00	0.3
2	42	VCORE	13/01/30	Morris	adjust design parameter from vendor recommend	change PC509 from 0.1uF to 1000pF change PR529 from 3.83K to 5.76K change PR504 from 523K to 499K	0.3
3	36	DCIN/BATT CONN/OTP	13/01/30	Morris	change from ESD request	change PD1 from SC300002E00 to SC300001G00	0.3
4	38	3.3VALWP/SVALWP	13/02/01	Morris	add ESD diode from ESD request	add PD101 (SCA00002A00)	0.3
5	42	VCORE	13/02/21	Morris	adjust design parameter from fine tune result	change PR501 from 422K to 523K change PR503 from 56K to 75K	0.3
6	44	VGA_CORE/PCIE	13/02/21	Morris	unpop from EE request	unpop PR808	0.3
7	44	VGA_CORE/PCIE	13/03/05	Morris	adjust output voltage from vender request	unpop PR826 and pop PR834 (only for Sun XT)	0.4
8	37 38 39 40 41 42	CHARGER 3.3VALWP/SVALWP 1.5VSP/1.8VSP +VCCIO +1.35VP/0.675VSP VCORE	13/03/28	Morris	verify function ok, so delete 0 ohm to short	unpop PR100, PR101, PR201, PR202, PR300, PR303, PR401, PR522, PR535, PR704, PR708, PR710, PR714, PR715, PR717	1.0
9	36	DCIN/BATT CONN/OTP	13/04/09	Morris	design change for solve issue	unpop PR1 and PC5	2.0
10	41 43	+1.35VP/0.675VSP +1.35VGPU/VDDCI	13/04/09	Morris	part shortage issue	change PQ201 and PQ1101 from SB00000T600 to SB000010A00	2.0
11	39 43 44	1.5VSP/1.8VSP +1.35VGPU/VDDCI VGA_CORE/PCIE	13/04/09	Morris	verify function ok, so delete 0 ohm to short	unpop PR601, PR802, PR803, PR814, PR823, PR830, PR845, PR846, PR1103, PR1200, PR1206, PR1210	2.0
12	43	+1.35VGPU/VDDCI	13/04/09	Morris	unpop VDDCI parts from vendor recommend and EEverify ok only for Sun XT	unpop PL1200, PL1201, PU1200, PQ1201, PR1201, PR1203, PR1204, PR1208, PR1209, PR1211, PR1212, PR1213, PC1201, PC1202, PC1204, PC1205, PC1206, PC1207, PC1209, PC1210, PC1211, PC1213 (only for Sun XT)	2.0
13	44	VGA_CORE/PCIE	13/04/12	Morris	part shortage issue	change PL1300 from SH00000GQ00 to SH00000PK00	2.0
14	36	DCIN/BATT CONN/OTP	13/04/12	Morris	customer request	add PR2 10kohm	2.0
15	42	VCORE	13/04/15	Morris	EMI request	pop PC522 and add PC523 0.1uF	2.0
16	36	DCIN/BATT CONN/OTP	13/05/22	Morris	reserve parts from ESD request	reserve PD2, PD3, PR17 and unpop PR17	3.0

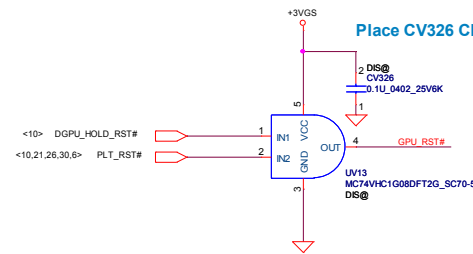
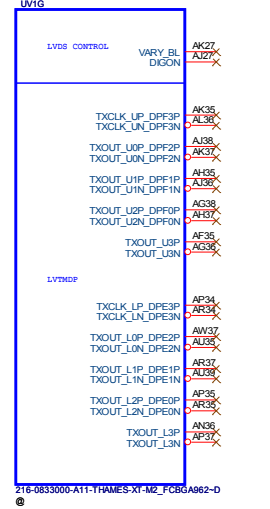
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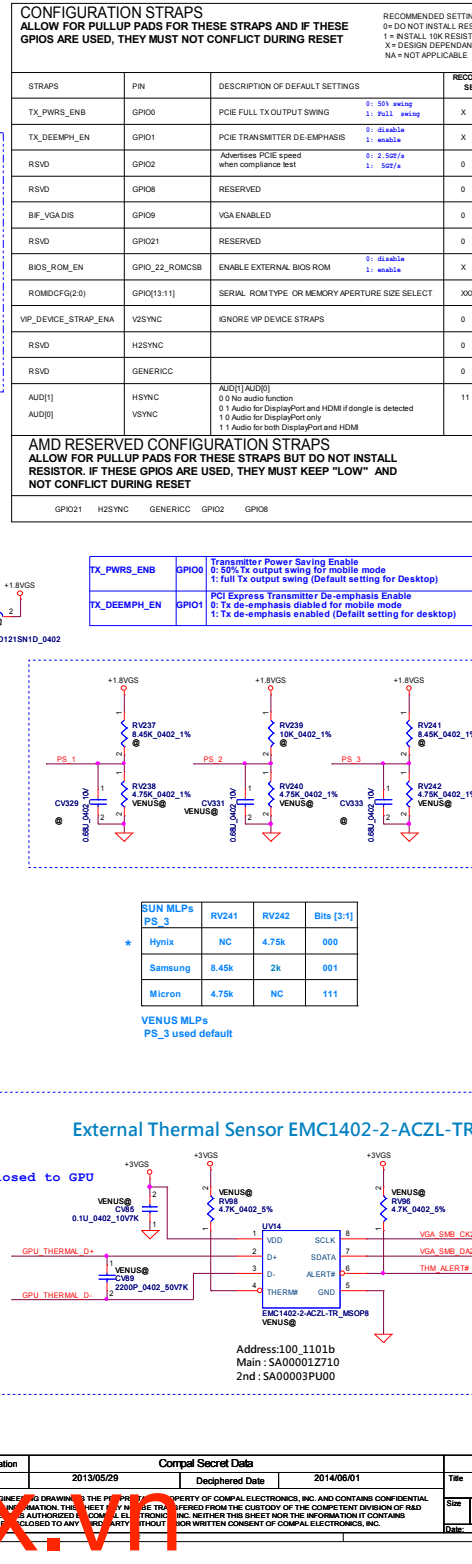
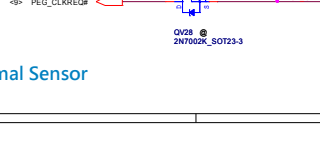
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Date: Wednesday, May 29, 2013				3.0
Sheet 47 of 57				

GFX PCIE LANE REVERSAL



LVDS Interface

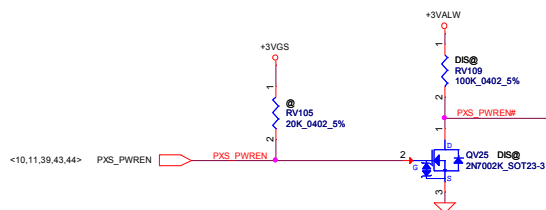


[illegible]

PX_MODE=1 for Normal Operation
 PX_MODE=0 for BACO mode to shut down power rails except VDDR3, PCIE_VDDC and 1.8V rail

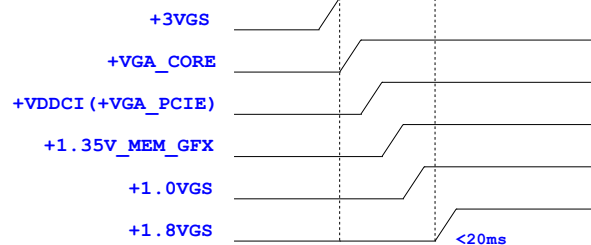
Note:

PX4.0 +VGA_CORE, VDDCI, +1.5VGS ON
 PX4.0 +3VGS, +1.0VGS, +1.8VGS OFF
 PX5.0 +3VGS, +VGA_CORE, VDDCI, +1.5VGV, +1.0VGS, +1.8VGS OFF

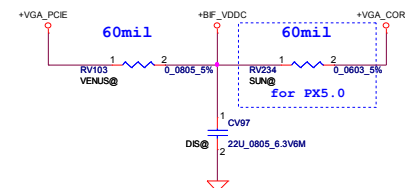


for PX4.0 and PX5.0

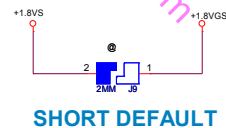
Power sequence of Sun XT, Venus Pro, Venus XT



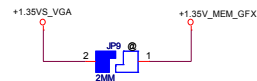
Switch circuits in BACO desings for Thames/Seymour only
 55mA@1.0V, in BACO mode



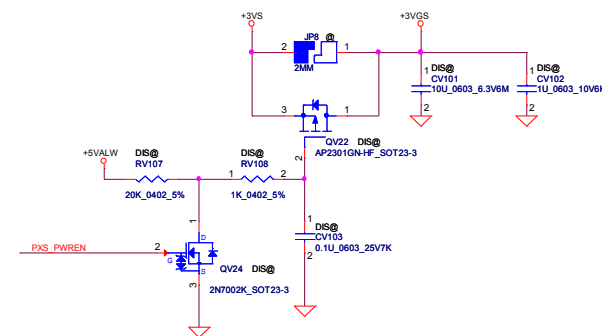
+1.8VS TO +1.8VGS

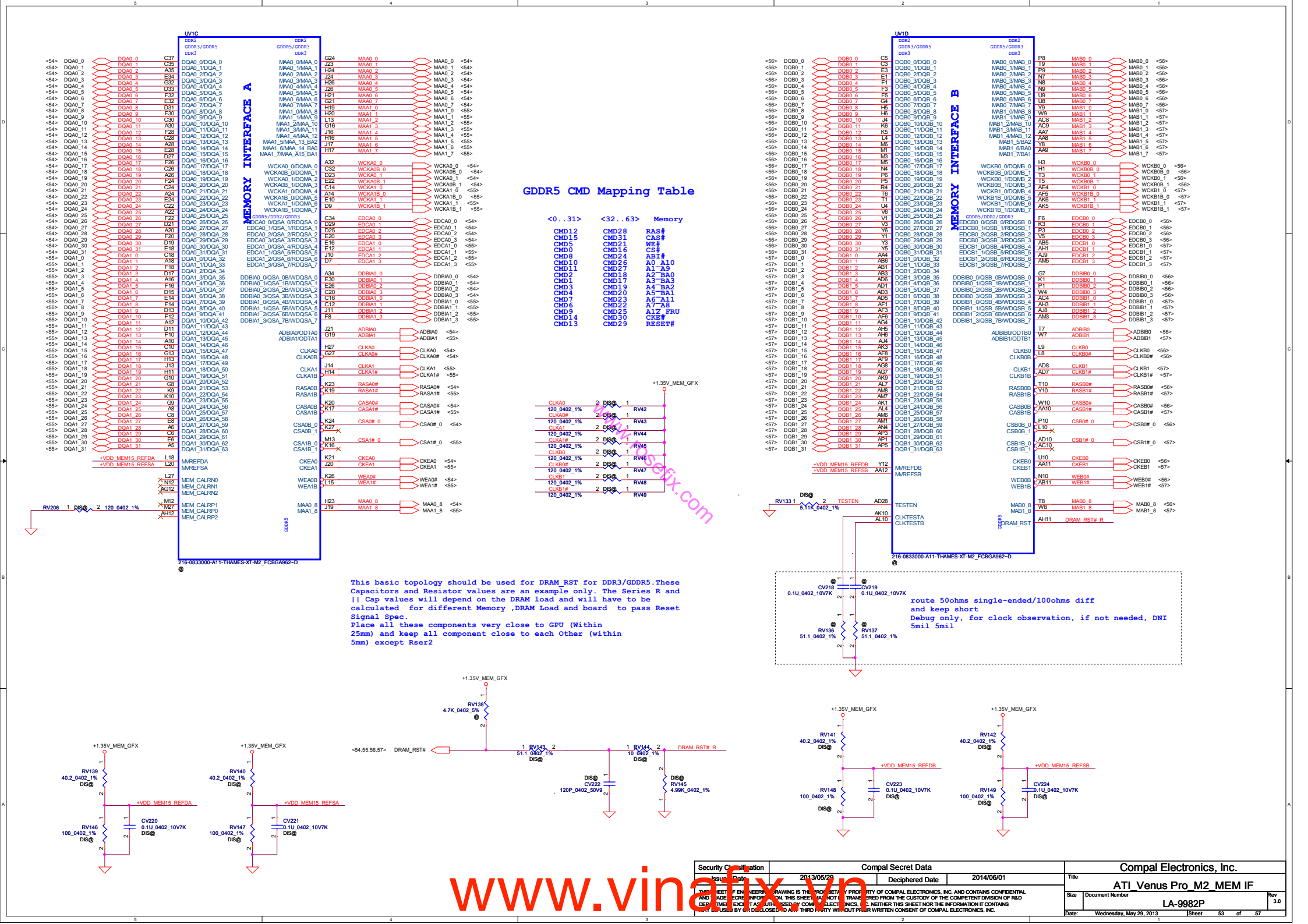


+1.35VS_VGA TO +1.35V_MEM_GFX

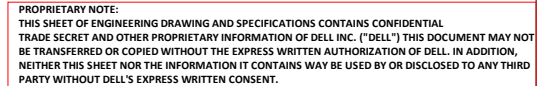


+3VS TO +3VGS





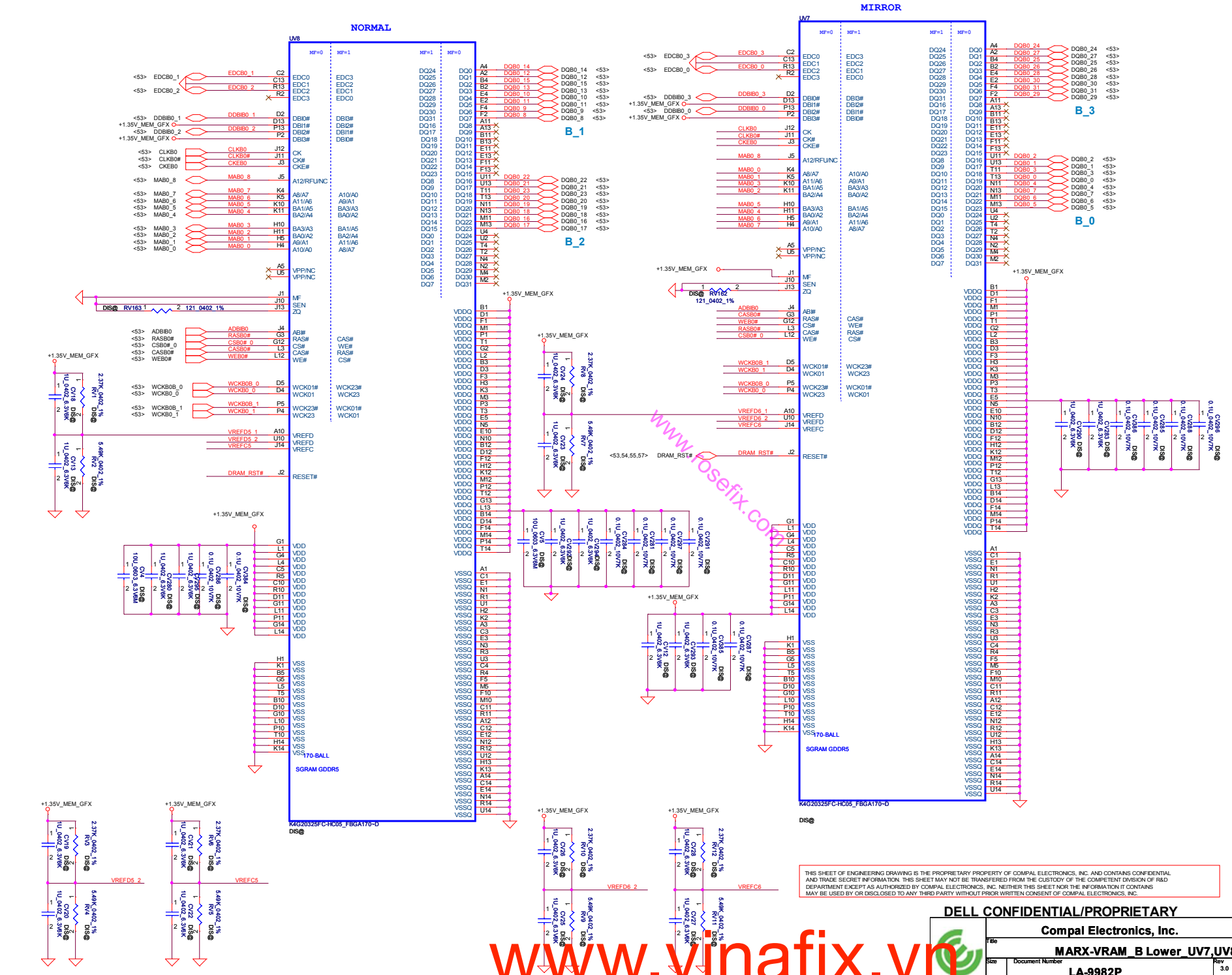
64X32 GDDR5



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Title				Rev
VRAM A Lower UV4,UV5				3
Size	Document Number			
	LA-9982P			
Date:	Wednesday, May 29, 2013	Sheet	54	of 57

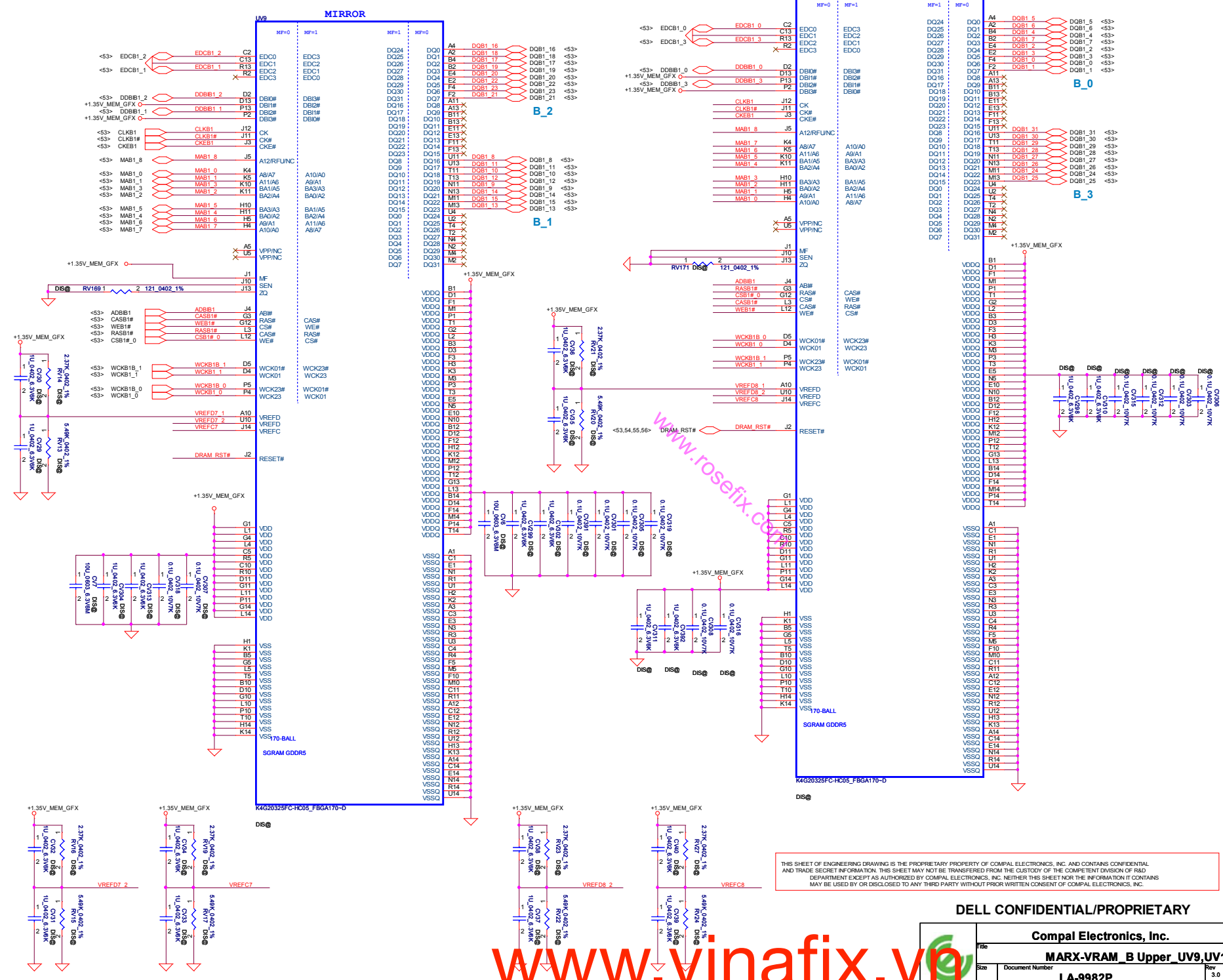
Memory Partition B - Lower 16 bits



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File	MARX-VRAM B Lower UV7,UV8
Size	Document Number
LA-9982P	
Date	Wednesday, May 29, 2013
Sheet	56 of 57

Memory Partition B - Upper 16 bits



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File	MARX-VRAM_B Upper_UV9,UV10
Size	Document Number
LA-9982P	
Date	Wednesday, May 29, 2013
Sheet	57 of 57
Rev	3.0

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