

VDKTE

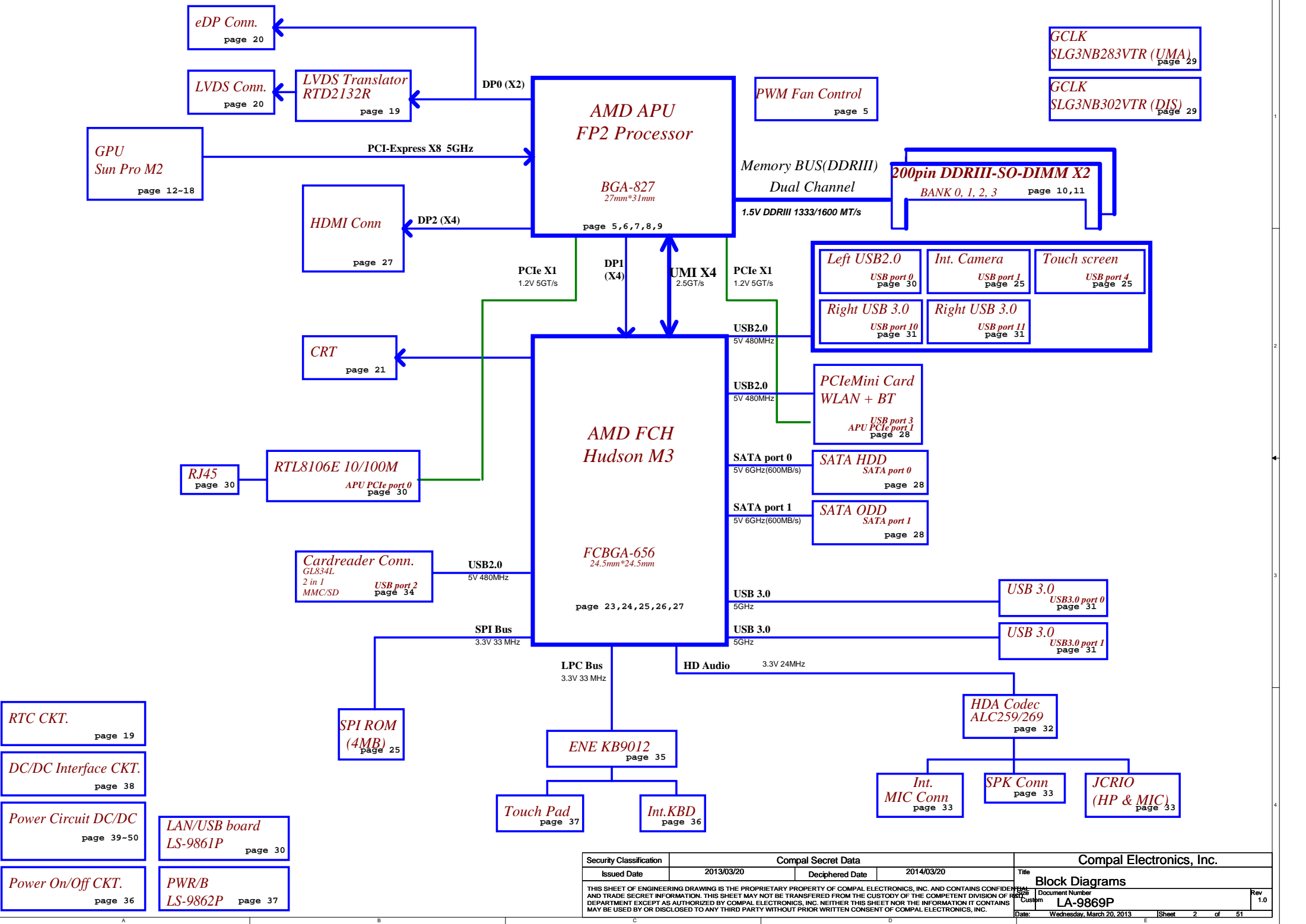
Rosetta 10ADT/10ADTG

LA-9869P REV 1.0 Schematic

AMD APU RICHLAND FP2 / FCH BOLTON-M3

2013-03-20 Rev 1.0

| | | | | | | |
|--|--------------------|-----------------|------------|----------------------------|---------------------------|---------------|
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| | | | | Custom | LA-9869P | 1.0 |
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Cardreader Conn. GL834L
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RTC CKT.
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DC/DC Interface CKT.
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Power Circuit DC/DC
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Power On/Off CKT.
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LAN/USB board LS-9861P
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PWR/B LS-9862P
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LVDS Translator RTD2132R
page 19

DP0 (X2)

DP2 (X4)

DP1 (X4)

PCIe X1 1.2V 5GT/s

PCIe X1 1.2V 5GT/s

UMI X4 2.5GT/s

PCIe X1 1.2V 5GT/s

USB2.0 5V 480MHz

USB2.0 5V 480MHz

SATA port 0 5V 6GHz(600MB/s)

SATA port 1 5V 6GHz(600MB/s)

USB2.0 5V 480MHz

USB2.0 5V 480MHz

SPI Bus 3.3V 33 MHz

LPC Bus 3.3V 33 MHz

HD Audio 3.3V 24MHz

SPI ROM (4MB)
page 25

ENE KB9012
page 35

Touch Pad
page 37

Int. KBD
page 36

AMD APU FP2 Processor
BGA-827
27mm*31mm
page 5,6,7,8,9

AMD FCH Hudson M3
FCBGA-656
24.5mm*24.5mm
page 23,24,25,26,27

PWM Fan Control
page 5

Memory BUS(DDRIII) Dual Channel
1.5V DDRIII 1333/1600 MT/s

200pin DDRIII-SO-DIMM X2
BANK 0, 1, 2, 3
page 10,11

Left USB2.0
USB port 0
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Int. Camera
USB port 1
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Touch screen
USB port 4
page 25

Right USB 3.0
USB port 10
page 31

Right USB 3.0
USB port 11
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PCIeMini Card WLAN + BT
USB port 3
APU PCIe port 1
page 28

SATA HDD
SATA port 0
page 28

SATA ODD
SATA port 1
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USB 3.0
5GHz
USB3.0 port 0
page 31

USB 3.0
5GHz
USB3.0 port 1
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HDA Codec ALC259/269
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Int. MIC Conn
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SPK Conn
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JCRIO (HP & MIC)
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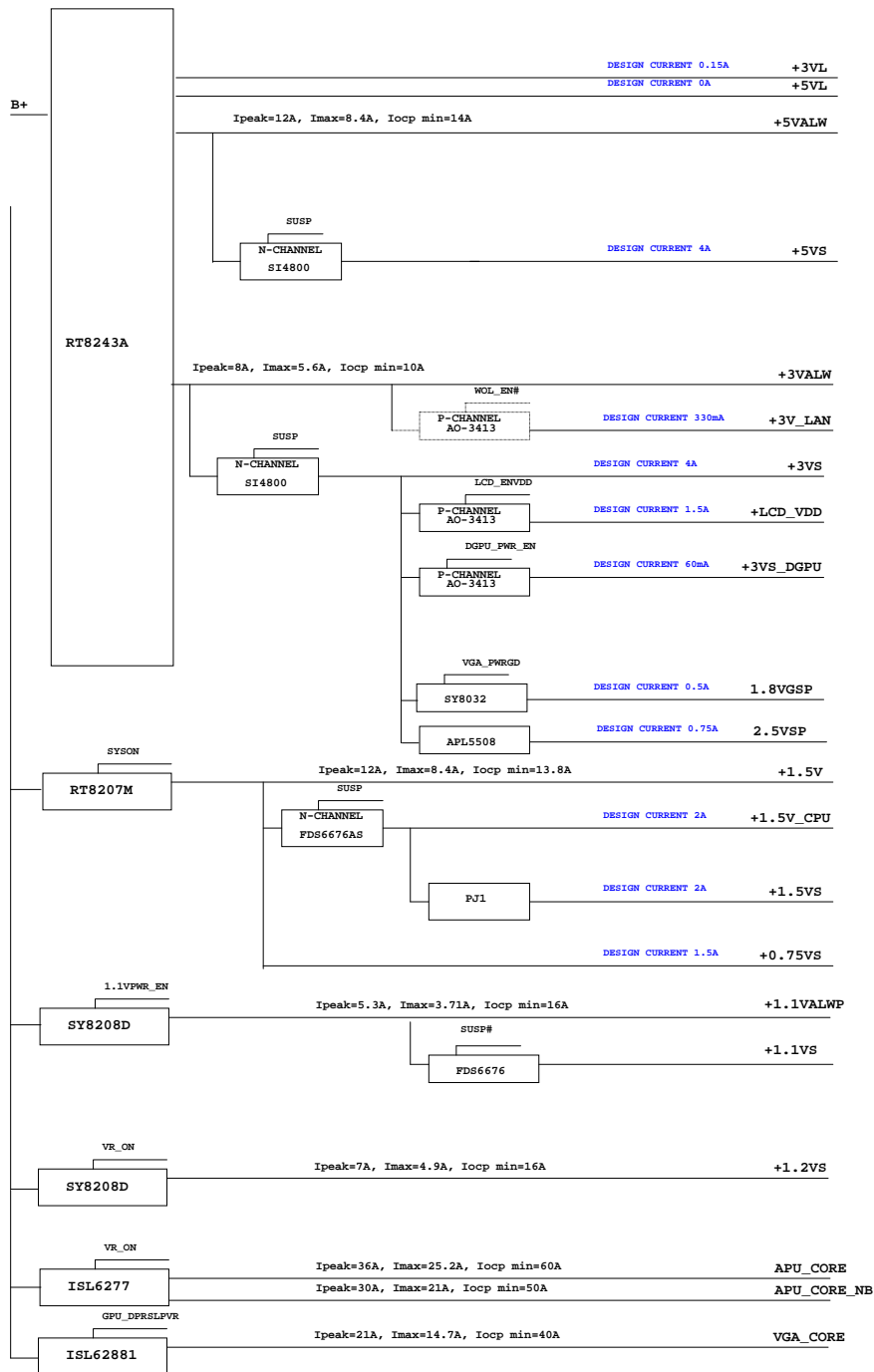
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Block Diagrams

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Voltage Rails

(O MEANS ON X MEANS OFF)

| power plane / State | +RTCVCC | B+ | VL +3VL | +5VALW +3VALW | +1.5V | +5VS +3VS +2.5VS +1.5VS +1.2VS +1.1VS +0.75VS +APU_CORE +APU_CORE_NB +1.1VALW |
|--------------------------------|---------|----|---------|---------------|-------|---|
| S0 | O | O | O | O | O | O |
| S1 | O | O | O | O | O | O |
| S3 | O | O | O | O | O | X |
| S5 S4/AC | O | O | O | O | X | X |
| S5 S4/ Battery only | O | O | O | X | X | X |
| S5 S4/AC & Battery don't exist | O | X | X | X | X | X |

BTO Option Table

| Function | APU | | FCH | | GPU | |
|-------------|--------|----|-----------|----------|-----|----|
| description | Bolton | | | | | |
| explain | R1 | R3 | R1 | R3 | R1 | R3 |
| BTO | | | BOLTONR1@ | HUDM3R3@ | | |

| Function | 3D sensor | KB LED | Clock | | UMA/DIS | |
|-------------|-----------|--------|-------------|----------------|---------|------|
| description | | K | | | 1G | U |
| explain | G-sensor | KB LED | Green Clock | No Green Clock | DIS | UMA |
| BTO | GSENSOR@ | KBL@ | GCLK@ | NOGCLK@ | VGA@ | UMA@ |

| Function | Panel | | | |
|-------------|-------|-------|--|--|
| description | S | D | | |
| explain | LVDS | eDP | | |
| BTO | LVDS@ | IEDP@ | | |

FCH SM Bus Address (SCL0/SDA0)

| Power | Device | HEX | Address |
|-------|---------------|------|-------------|
| +3VS | DDR SO-DIMM 0 | A0 H | 1010 000X b |
| +3VS | DDR SO-DIMM 1 | A2 H | 1010 001X b |
| +3VS | WLAN | | |

EC SM Bus1 Address

| Power | Device | HEX | Address |
|-------|---------------|------|-------------|
| +3VL | Smart Battery | 16 H | 0001 0110 b |
| +3VL | Charger | 12 H | 0001 0010 b |

EC SM Bus2 Address

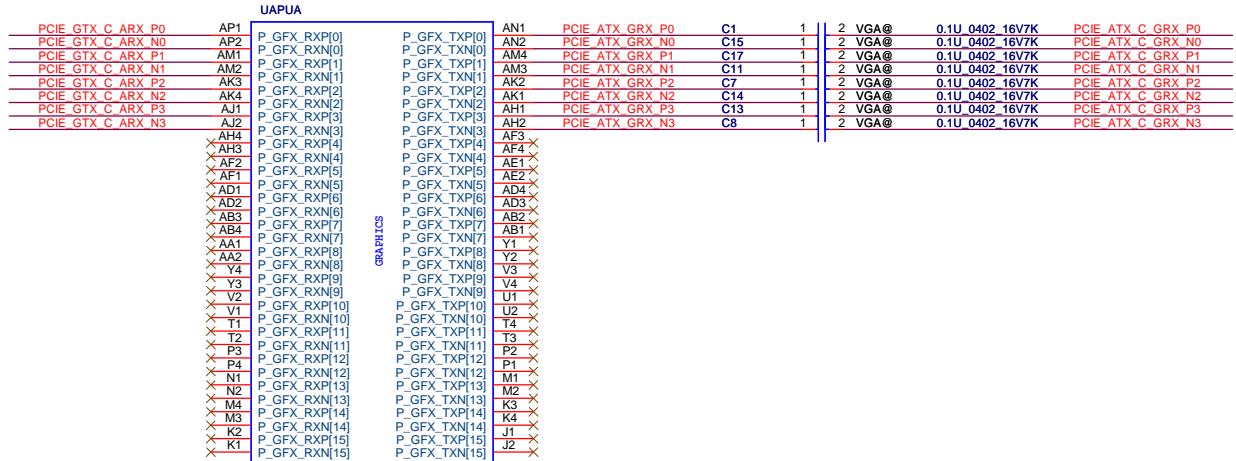
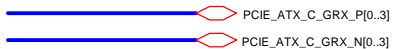
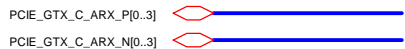
| Power | Device | HEX | Address |
|-------|-------------|------|-------------|
| +3VL | SB-TSI | 98 H | 1001 1001 b |
| +3VS | G-Sensor | 40 H | 0100 0000 b |
| +3VS | VGA Thermal | 82H | 1000 0010 b |

EC SM Bus3 Address

| Power | Device | HEX | Address |
|-------|-----------------|------|-------------|
| +3VS | LVDS Translator | 94 H | 1001 0100 b |

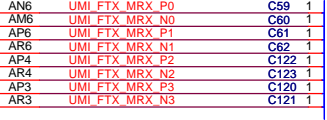
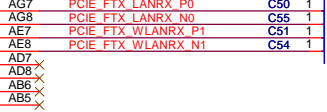
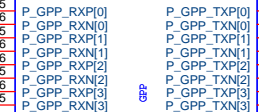
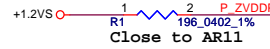
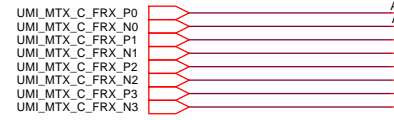
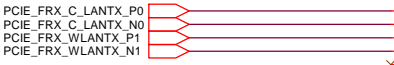
| STATE \ SIGNAL | SLP_S3# | SLP_S5# |
|-----------------------|---------|---------|
| Full ON | HIGH | HIGH |
| S1 (Power On Suspend) | HIGH | HIGH |
| S3 (Suspend to RAM) | LOW | HIGH |
| S4 (Suspend to Disk) | LOW | HIGH |
| S5 (Soft OFF) | LOW | LOW |
| G3 | LOW | LOW |

| | | | | | | |
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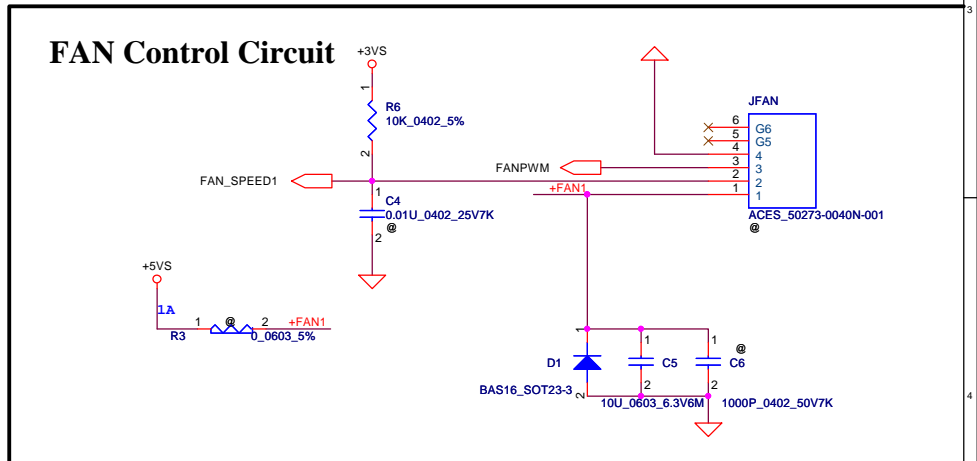
LAN
WLAN

LAN
WLAN

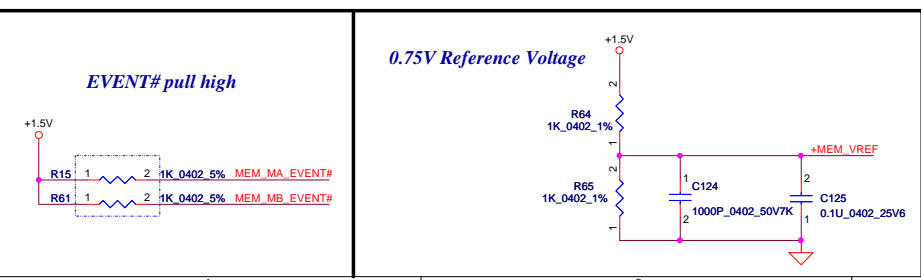
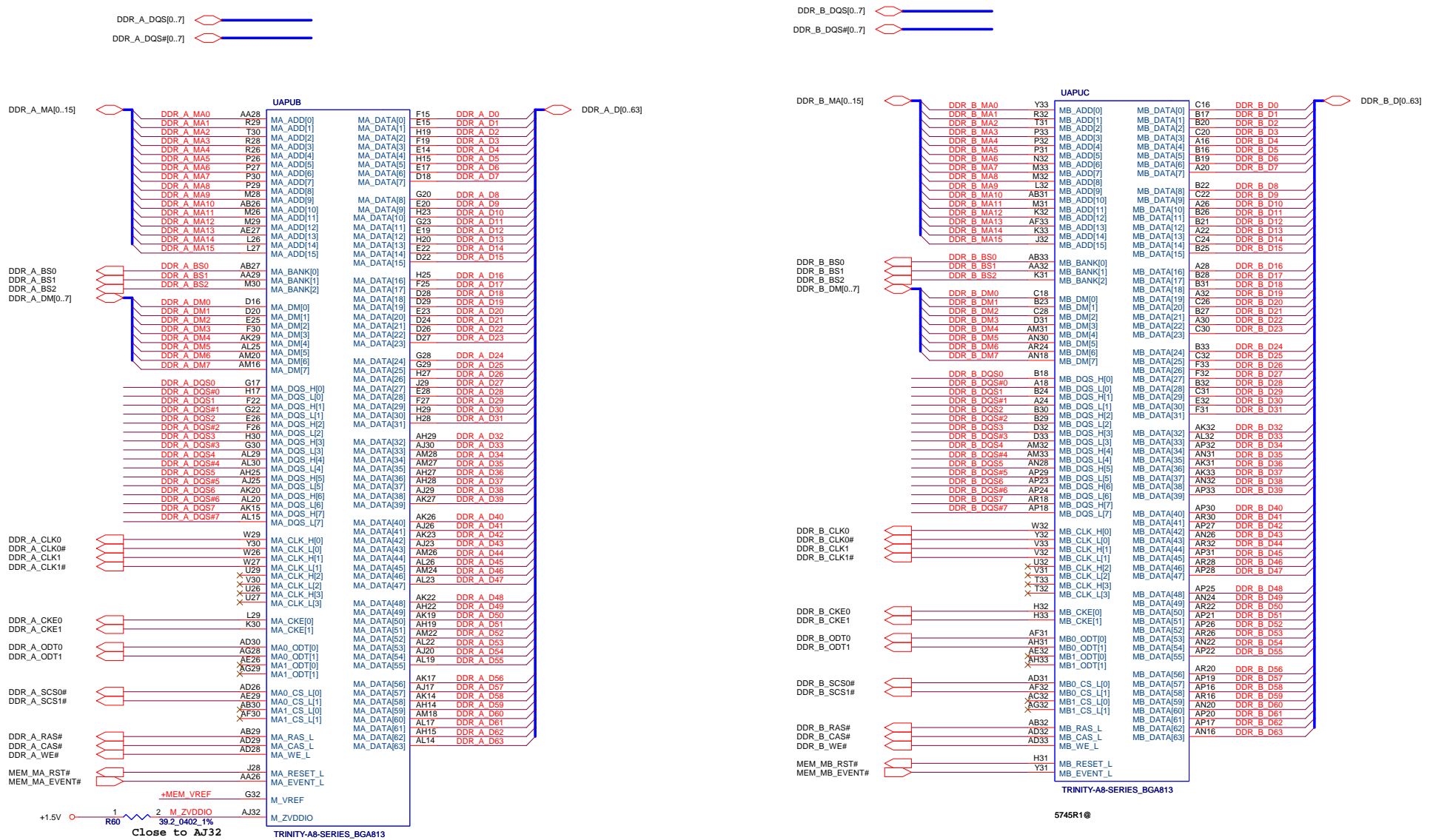


TRINITY-A8-SERIES_BGA813
5745R1@

Close to AP11

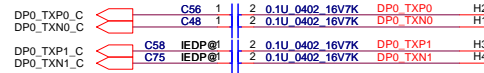


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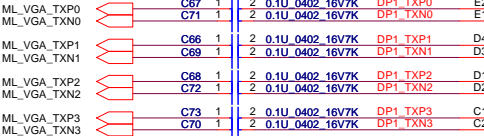


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LVDS/eDP



CRT (To FCH)

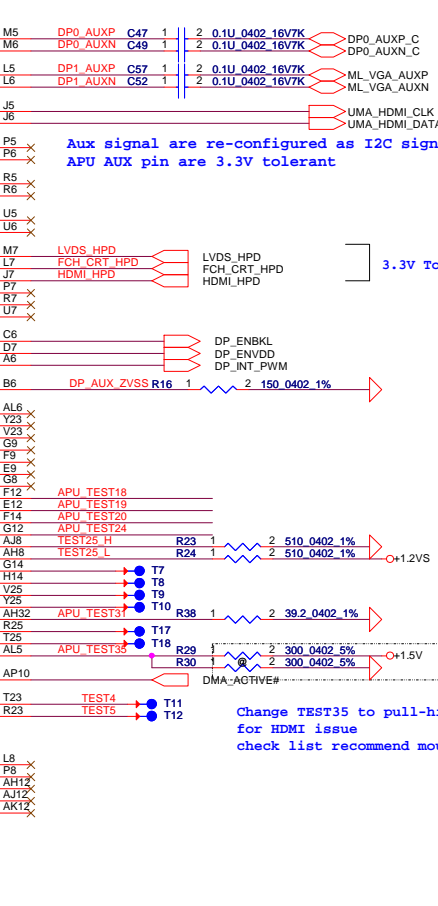
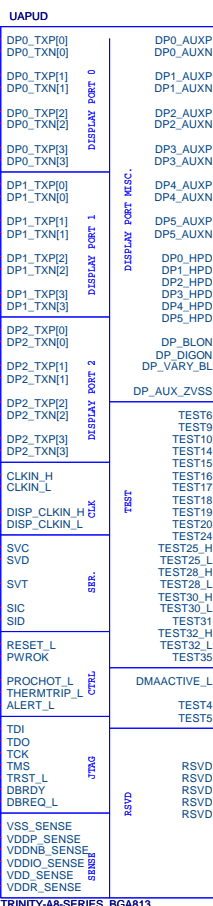
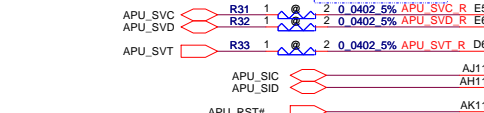
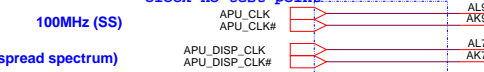


HDMI



100MHz (SS)

100MHz (Non-spread spectrum)



LVDS

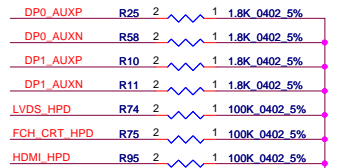
CRT (To FCH)

HDMI

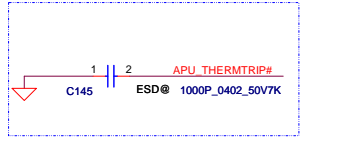
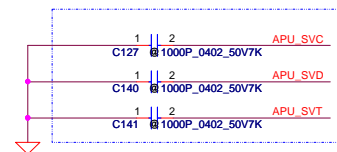
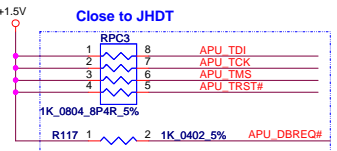
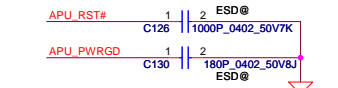
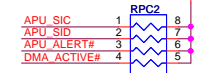
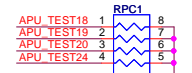
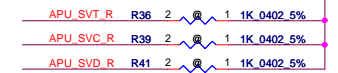
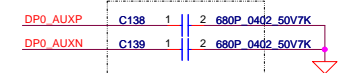
Aux signal are re-configured as I2C signals for DDC
APU AUX pin are 3.3V tolerant

3.3V Tolerance

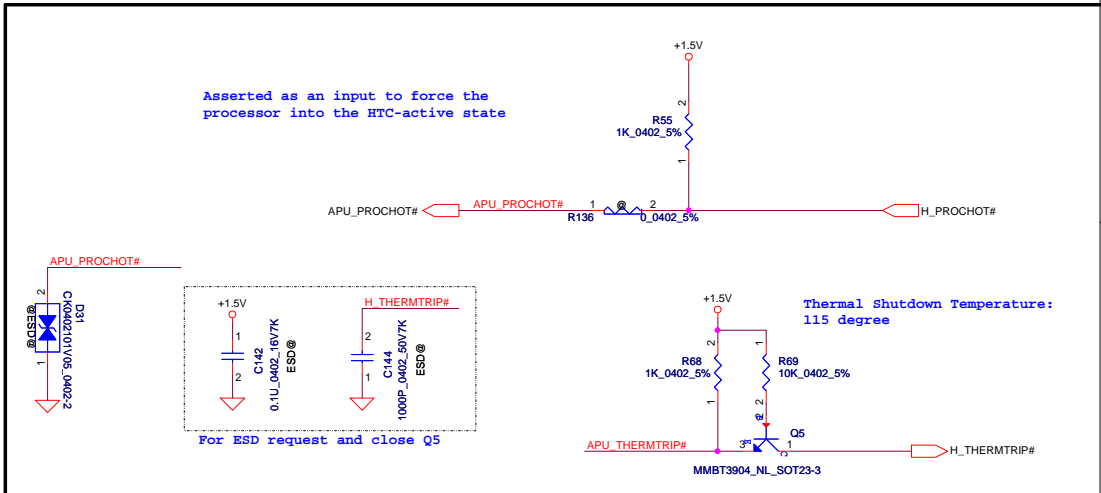
Change TEST35 to pull-high for HDMI issue
check list recommend mount R29 and R30 @



For 2132R



For ESD request and close APU

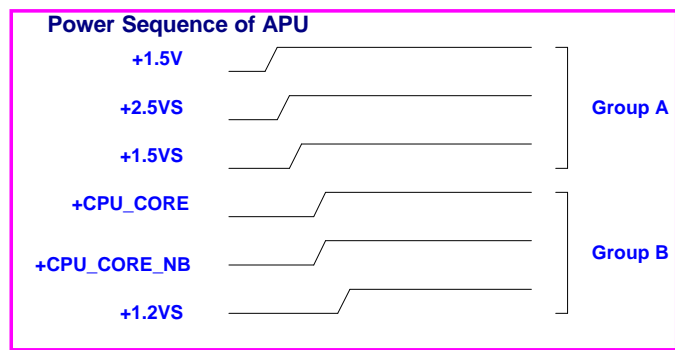
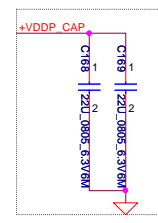
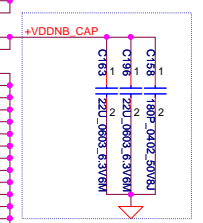
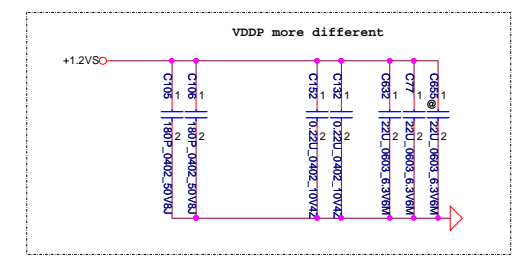
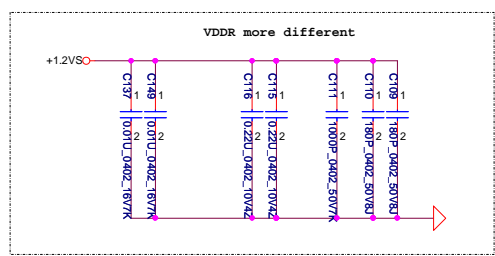
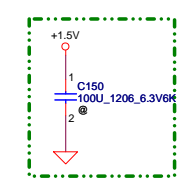
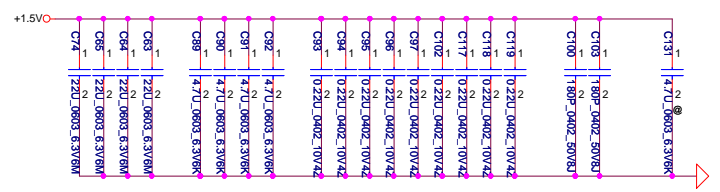
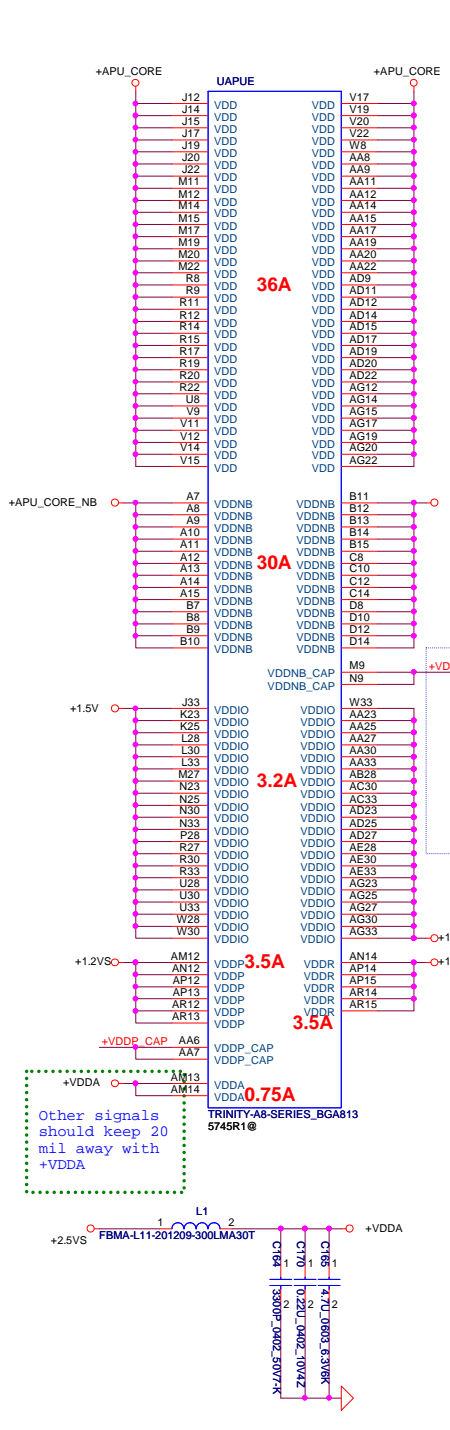


Asserted as an input to force the processor into the HTC-active state

Thermal Shutdown Temperature: 115 degree

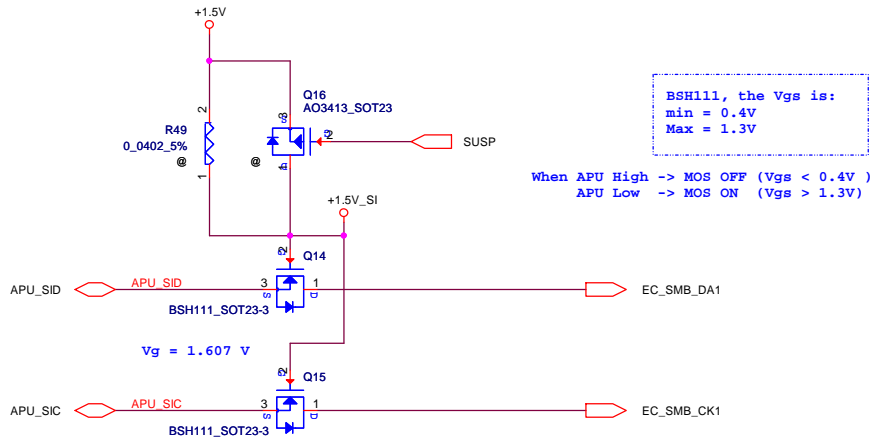
For ESD request and close Q5

| | | | | |
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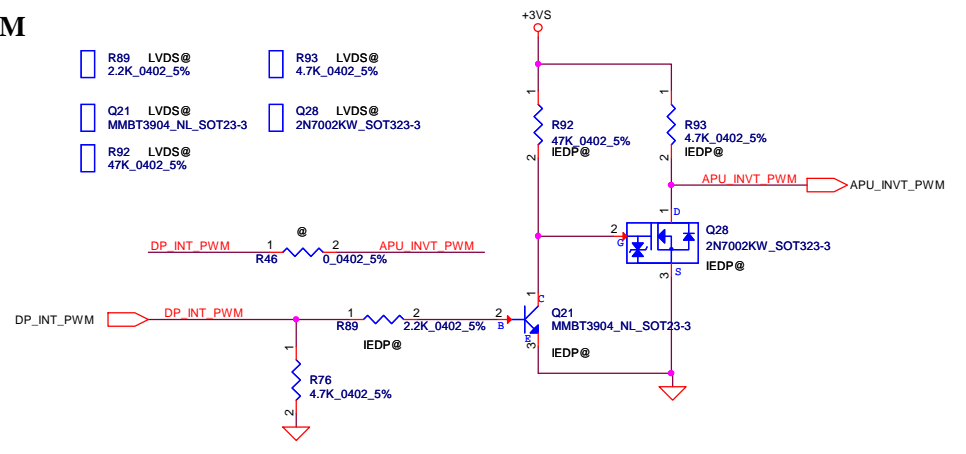


| UAPUF | | |
|-------|-----|------|
| A17 | VSS | Y11 |
| A19 | VSS | Y12 |
| A21 | VSS | Y14 |
| A23 | VSS | Y15 |
| A25 | VSS | Y17 |
| A27 | VSS | Y19 |
| A29 | VSS | Y20 |
| A31 | VSS | Y22 |
| B1 | VSS | AA4 |
| C3 | VSS | AA5 |
| C4 | VSS | AA6 |
| C33 | VSS | AA8 |
| D5 | VSS | AC1 |
| D9 | VSS | AC2 |
| D11 | VSS | AC4 |
| D14 | VSS | AC5 |
| D15 | VSS | AC11 |
| D17 | VSS | AC12 |
| D19 | VSS | AC14 |
| D21 | VSS | AC15 |
| D23 | VSS | AC17 |
| D25 | VSS | AC19 |
| D30 | VSS | AC20 |
| E4 | VSS | AC22 |
| E27 | VSS | AC23 |
| E29 | VSS | AC25 |
| E30 | VSS | AE4 |
| E31 | VSS | AE9 |
| F5 | VSS | AF11 |
| F6 | VSS | AF12 |
| F7 | VSS | AF14 |
| F8 | VSS | AF15 |
| F17 | VSS | AF17 |
| F20 | VSS | AF19 |
| F23 | VSS | AF20 |
| F28 | VSS | AF22 |
| F29 | VSS | AF23 |
| G1 | VSS | AF25 |
| G2 | VSS | AG1 |
| G4 | VSS | AG2 |
| G8 | VSS | AG3 |
| G19 | VSS | AG9 |
| G25 | VSS | AG11 |
| G26 | VSS | AG26 |
| G27 | VSS | AH7 |
| G33 | VSS | AH17 |
| H8 | VSS | AH20 |
| H9 | VSS | AH23 |
| H2 | VSS | AH26 |
| H26 | VSS | AH30 |
| J4 | VSS | AJ4 |
| J8 | VSS | AJ5 |
| J9 | VSS | AJ6 |
| J11 | VSS | AJ7 |
| J23 | VSS | AJ9 |
| J25 | VSS | AJ14 |
| J26 | VSS | AJ15 |
| J27 | VSS | AJ19 |
| J30 | VSS | AJ22 |
| K9 | VSS | AJ27 |
| K11 | VSS | AJ28 |
| K14 | VSS | AJ33 |
| K15 | VSS | AK8 |
| K17 | VSS | AK25 |
| K19 | VSS | AK28 |
| K20 | VSS | AK30 |
| K22 | VSS | AL1 |
| L1 | VSS | AL2 |
| L2 | VSS | AL4 |
| L4 | VSS | AL8 |
| M8 | VSS | AL11 |
| M23 | VSS | AL27 |
| M25 | VSS | AL28 |
| M4 | VSS | AL33 |
| N11 | VSS | AM5 |
| N12 | VSS | AM7 |
| N14 | VSS | AM9 |
| N15 | VSS | AM11 |
| N17 | VSS | AM15 |
| N19 | VSS | AM17 |
| N20 | VSS | AM19 |
| N22 | VSS | AM21 |
| R1 | VSS | AM23 |
| R2 | VSS | AM25 |
| R4 | VSS | AM29 |
| T9 | VSS | AM30 |
| T11 | VSS | AN3 |
| T12 | VSS | AN4 |
| T14 | VSS | AN33 |
| T15 | VSS | AP5 |
| T17 | VSS | AP9 |
| T19 | VSS | AR2 |
| T20 | VSS | AR5 |
| T22 | VSS | AR9 |
| U4 | VSS | AR17 |
| W1 | VSS | AR19 |
| W2 | VSS | AR21 |
| W4 | VSS | AR23 |
| W5 | VSS | AR25 |
| W6 | VSS | AR27 |
| W7 | VSS | AR29 |
| Y9 | VSS | AR31 |

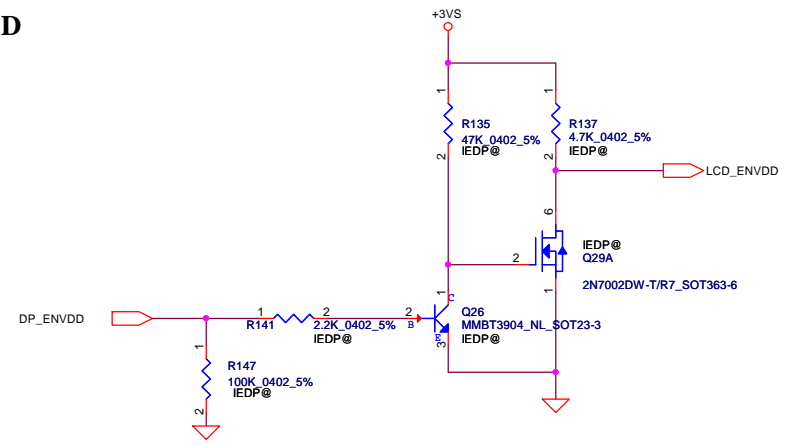
SB-TSI



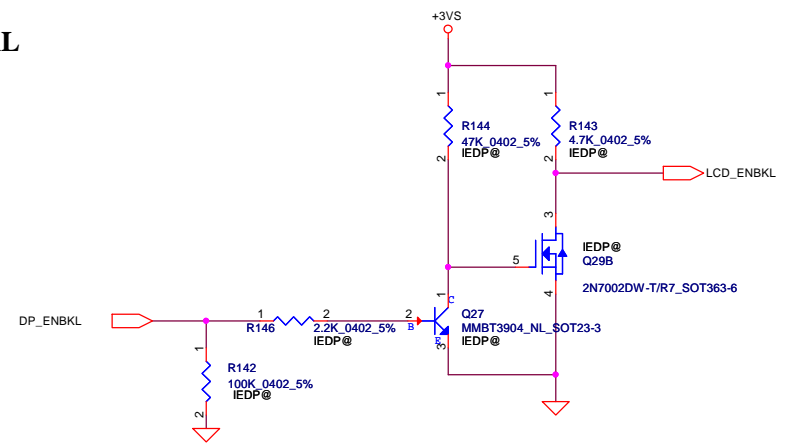
Panel PWM



eDP Panel ENVDD

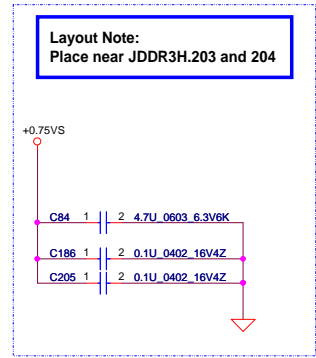
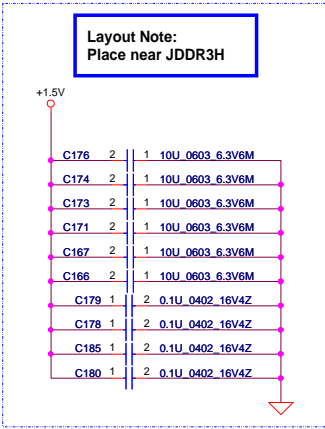
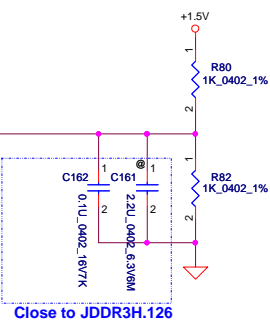
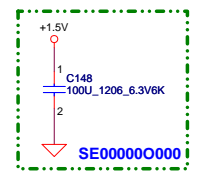
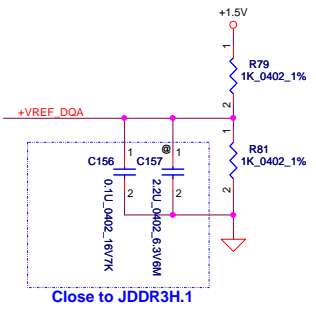
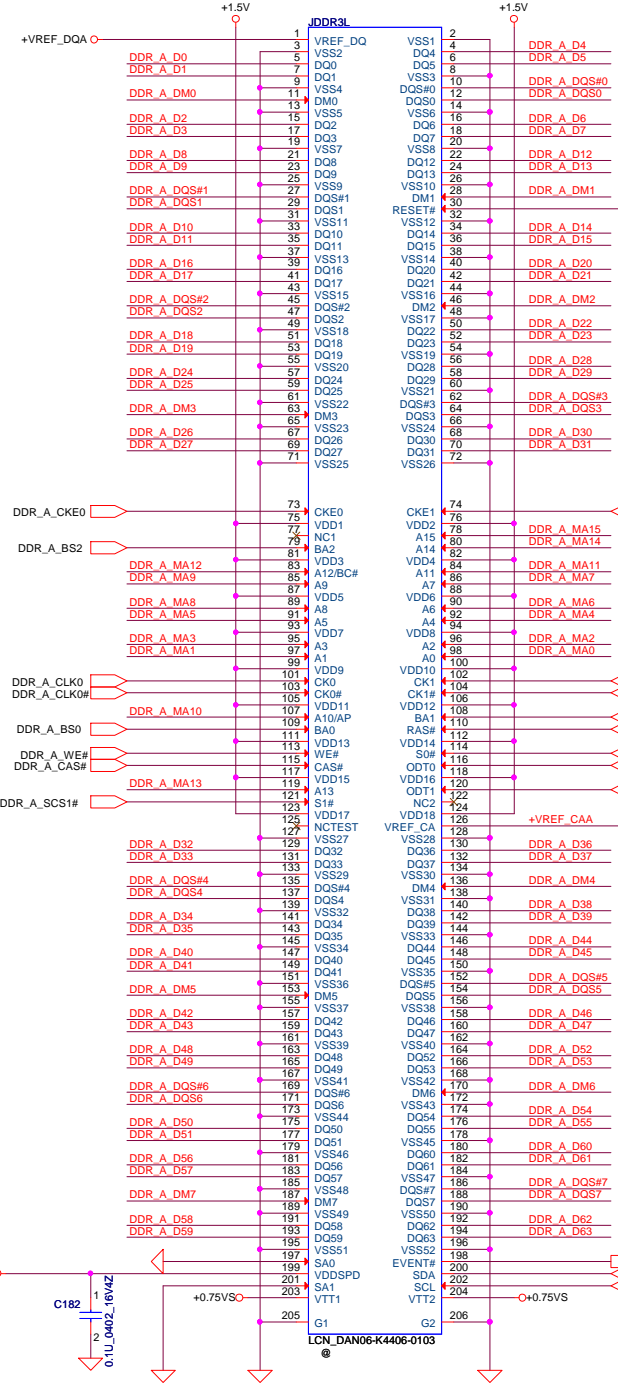


eDP Panel ENBKL



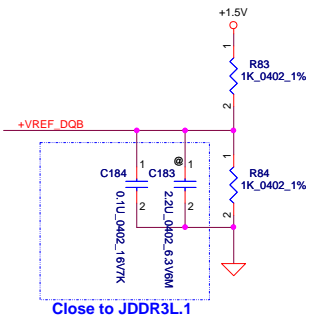
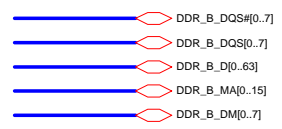
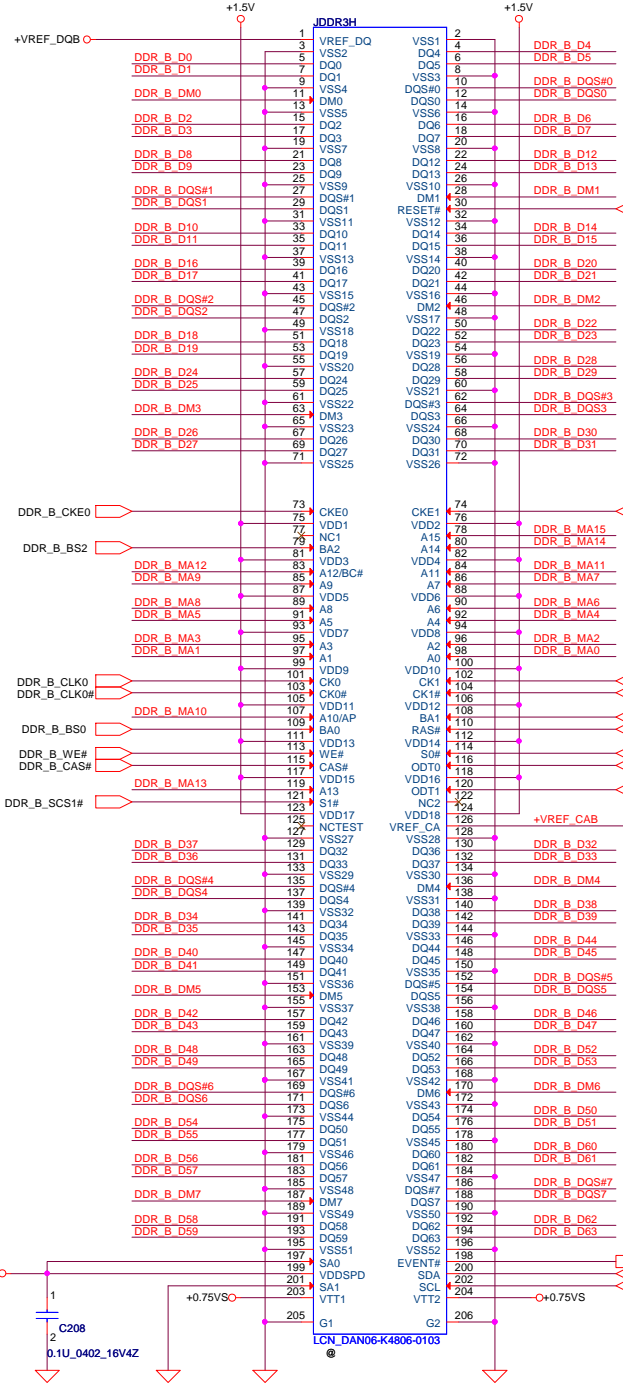
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|---|---------------------------|--------------------|------------|--------------------------------------|-----|
| Security Classification | | Compal Secret Data | | Title | |
| Issued Date | 2013/03/20 | Deciphered Date | 2014/03/20 | AMD Trinity FP2 Singal Level Shifter | |
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| Size | Custom | Document Number | LA-9869P | Rev | 1.0 |
| Date: | Wednesday, March 20, 2013 | Sheet | 9 | of | 51 |

DDR3 SO-DIMM A Reverse Type

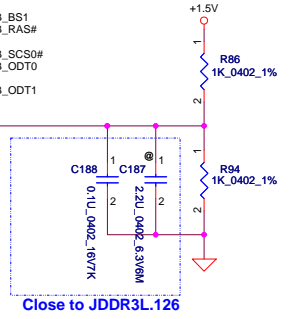


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| Security Classification | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2013/03/20 | Deciphered Date | 2014/03/20 | Title |
| | | | | DDRIII-SODIMMO |
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| | | | | Rev 1.0 |
| | | | | Sheet 10 of 51 |

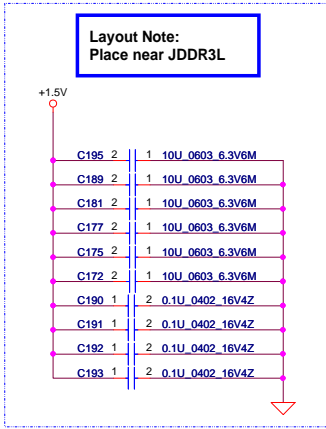
DDR3 SO-DIMM B Reverse Type



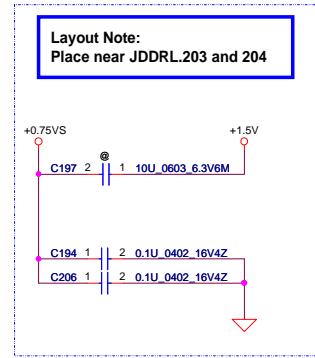
Close to JDDR3L.1



Close to JDDR3L.126



Layout Note:
Place near JDDR3L



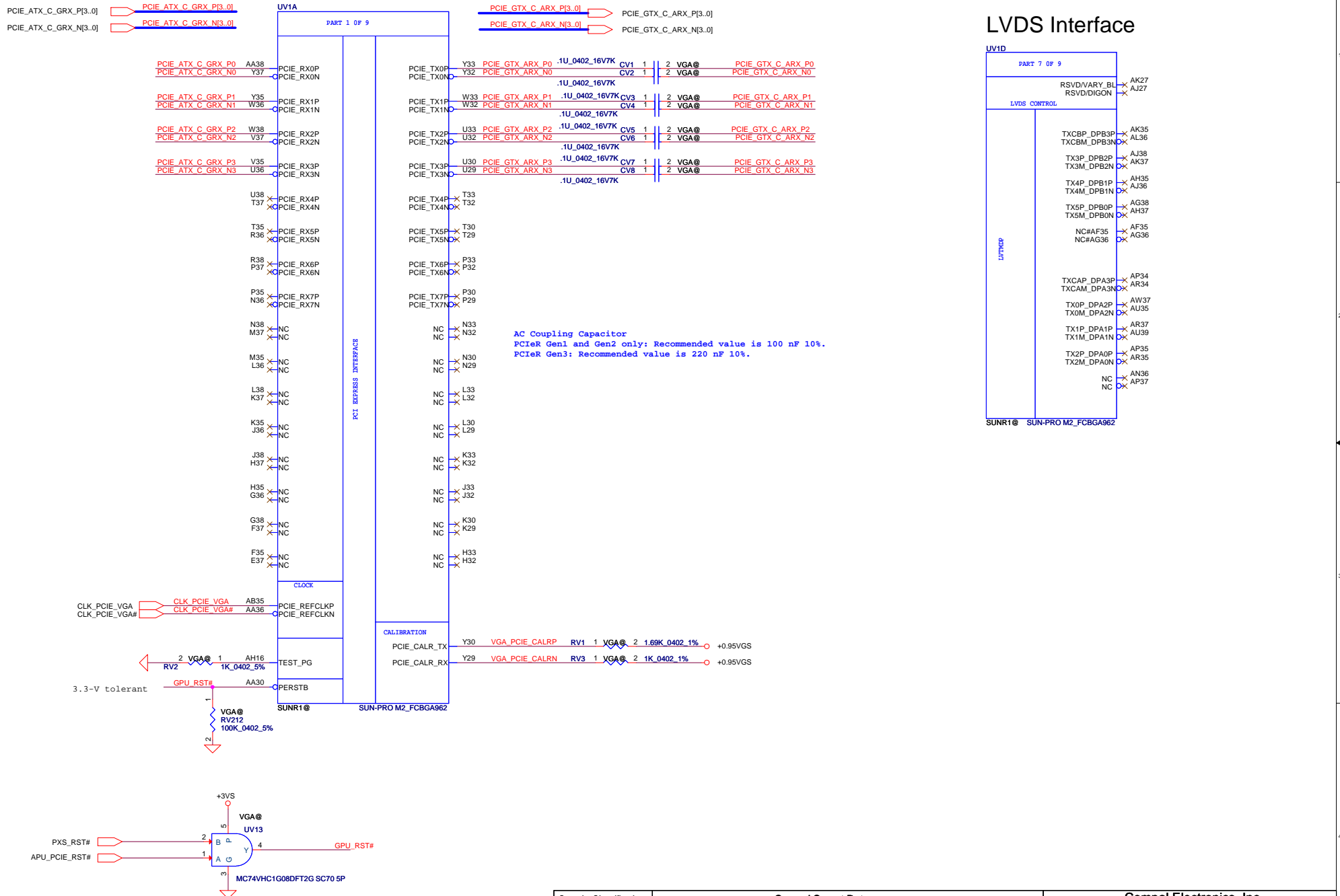
Layout Note:
Place near JDDR.L203 and 204

| | | | | | |
|---|--------------------|-----------------|------------|---------------------------------|----------------|
| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | |
| Issued Date | 2013/03/20 | Deciphered Date | 2014/03/20 | Title | |
| | | | | DDRIII-SODIMM1 | |
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| | | | | LA-9869P | 1.0 |
| | | | | Date: Wednesday, March 20, 2013 | Sheet 11 of 51 |

PCIE_ATX_C_GRX_P[3..0] PCIE_ATX_C_GRX_P[3..0]
 PCIE_ATX_C_GRX_N[3..0] PCIE_ATX_C_GRX_N[3..0]

PCIE GTX_C_ARX_P[3..0] PCIE_GTX_C_ARX_P[3..0]
 PCIE GTX_C_ARX_N[3..0] PCIE_GTX_C_ARX_N[3..0]

LVDS Interface

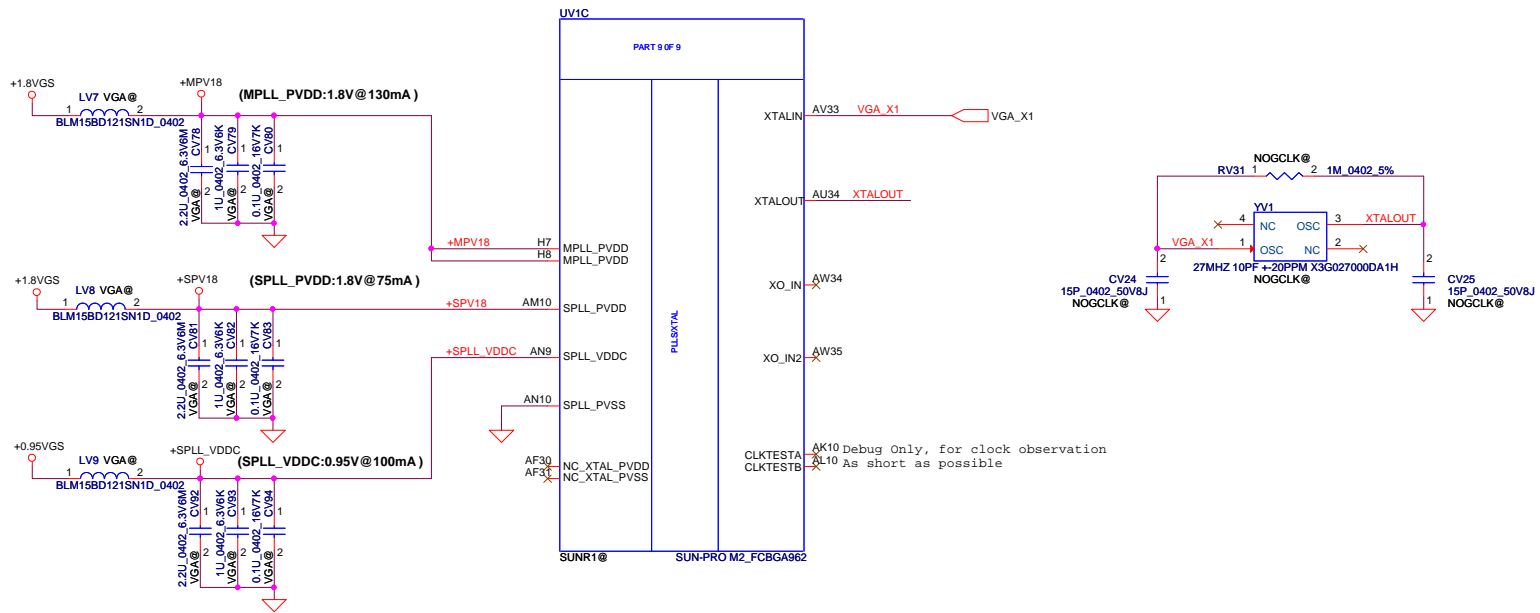


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|---|------------|-----------------|------------|--------------------|---------------------------|--------------------------|----|-------|
| Issued Date | 2013/03/20 | Deciphered Date | 2014/03/20 | Title | | | | |
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| | | | | Custom | LA-9869P | 1.0 | | |
| | | | | Date: | Wednesday, March 20, 2013 | Sheet | 12 | of 51 |

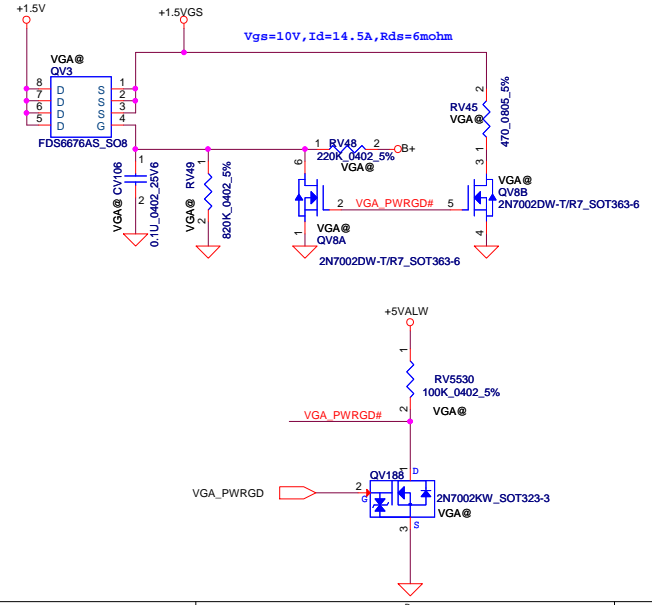
| MPLL_PVDD | MarsCRB | Design |
|-----------|---------|--------|
| 220ohm | 1 | 1 |
| 0.1u | 1 | 1 |
| 1u | 1 | 1 |
| 2.2u | 1 | 1 |

| SPLL_PVDD | MarsCRB | Design |
|-----------|---------|--------|
| 120ohm | 1 | 1 |
| 0.1u | 1 | 1 |
| 1u | 1 | 1 |
| 2.2u | 1 | 1 |

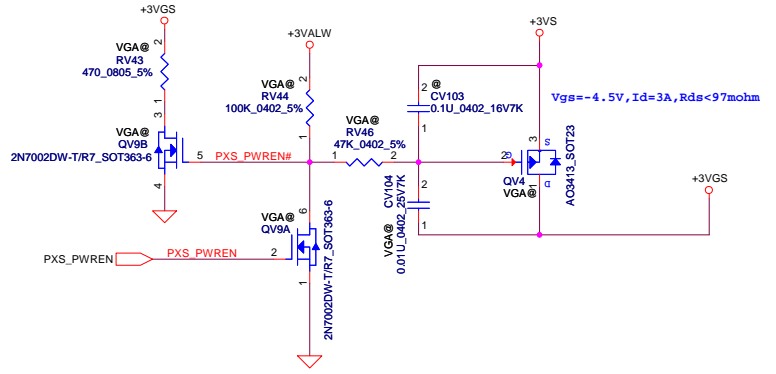
| SPLL_VDDC | MarsCRB | Design |
|-----------|---------|--------|
| 120ohm | 1 | 1 |
| 0.1u | 1 | 1 |
| 1u | 1 | 1 |
| 2.2u | 1 | 1 |



+1.5V to +1.5VGS



+3VS to +3VGS



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| | | | | Rev 1.0 |
| | | | | Sheet 14 of 51 |

| VDDR1 | MarsCRB | Design |
|-------|---------|--------|
| 0.01u | 5 | 0 |
| 0.1u | 5 | 0 |
| 2.2u | 5 | 5 |
| 10u | 3 | 3 |

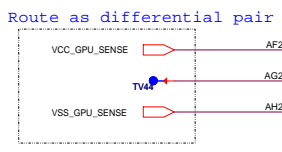
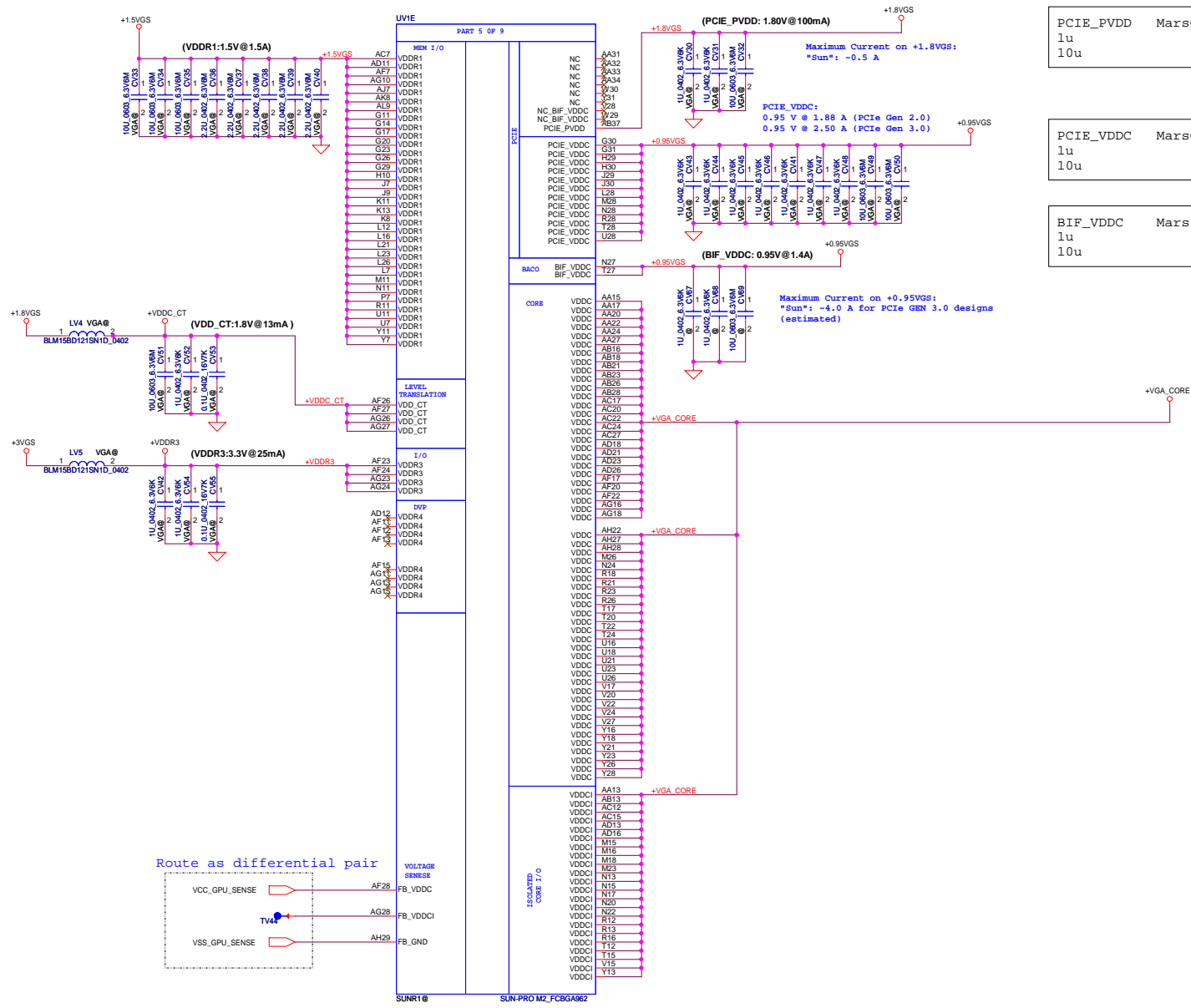
| VDD_CT | MarsCRB | Design |
|--------|---------|--------|
| 120ohm | 1 | 1 |
| 0.1u | 1 | 1 |
| 1u | 1 | 1 |
| 10u | 1 | 1 |

| VDDR3 | Mars | check list | Design |
|--------|------|------------|--------|
| 120ohm | 1 | 1 | 1 |
| 1u | 3 | 2 | 2 |
| 10u | 1 | 0 | 0 |
| 0.1u | 0 | 1 | 1 |

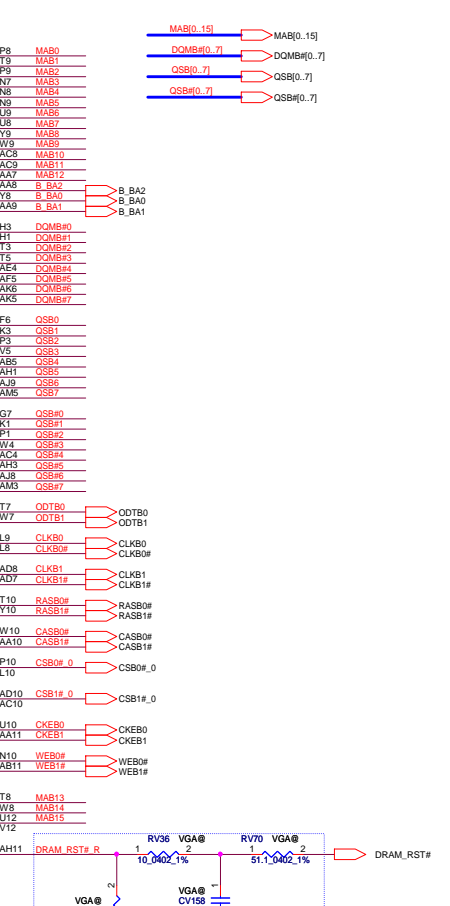
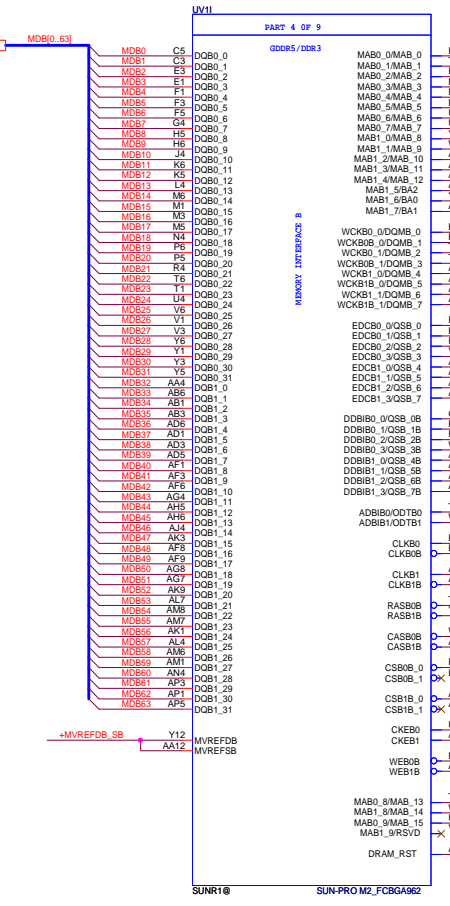
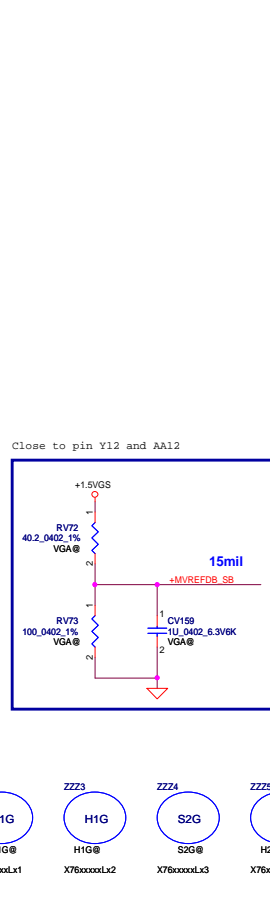
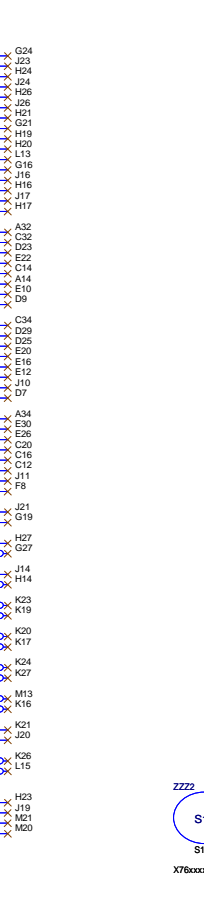
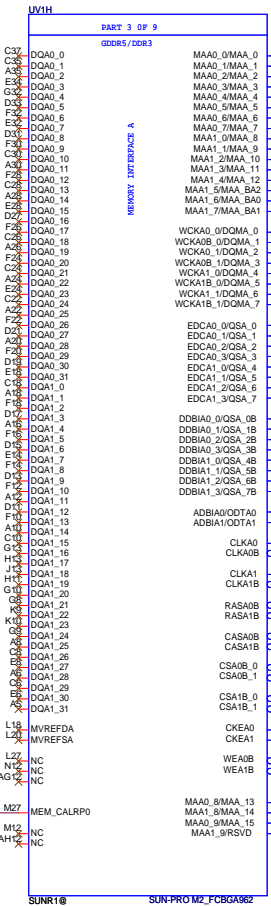
| PCIE_PVDD | MarsCRB | Design |
|-----------|---------|--------|
| 1u | 2 | 2 |
| 10u | 1 | 1 |

| PCIE_VDDC | MarsCRB | Design |
|-----------|---------|--------|
| 1u | 7 | 7 |
| 10u | 2 | 2 |

| BIF_VDDC | Mars | check list | Design |
|----------|------|------------|--------|
| 1u | 1 | 1 | 1 |
| 10u | 1 | 1 | 1 |



Need check all power current and decoupling capacitors after got SUN databook and reference schematic.

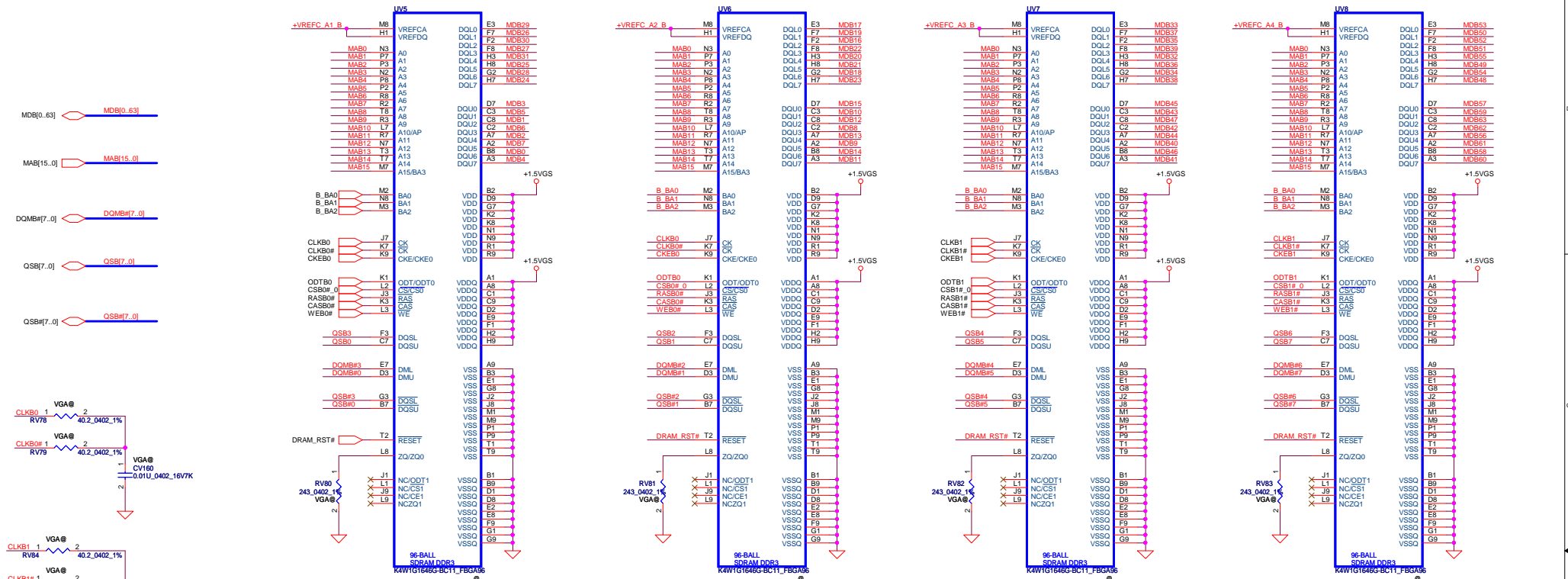


R_{pu} & R_{pd} resistor:
0402 1% resistors are required.

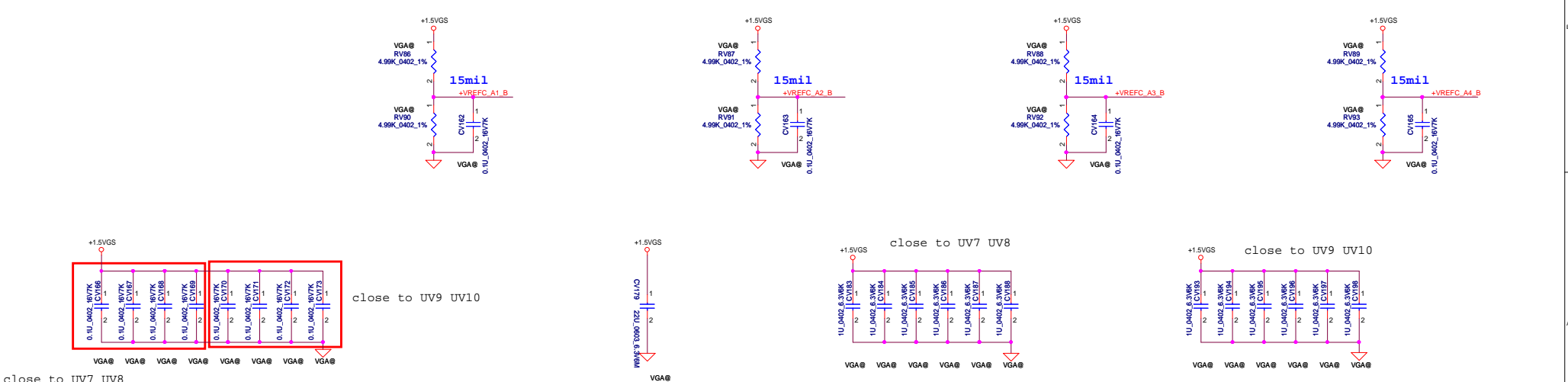
Place all these components close to GPU (Within 25mm) and keep all component close to each other

| GPU Type | Memory Bus Width | VRAM Vendor | Compal P/N | Manufacturer P/N | X76 P/N | Size per part | Configuration | Total Memory Size/Qty | PS_3[3] | PS_3[2] | PS_3[1] | R _{pu} | R _{pd} |
|------------|------------------|-------------|-------------|----------------------|-------------|---------------|---------------|-----------------------|---------|---------|---------|-----------------|-----------------|
| SUN PRO-M2 | 64bit | Hynix | SA00003YOG0 | H5TQ2G63DFR-11C | X7648051L01 | 2Gbit | 128M*16 | 1GB/4pcs | 0 | 0 | 0 | RV20 NC | RV27 4.75K |
| SUN PRO-M2 | 64bit | Hynix | SA000065320 | H5TQ2G63DFR-N0C | X7648051L02 | 2Gbit | 128M*16 | 1GB/4pcs | 0 | 1 | 0 | RV20 4.53K | RV27 2K |
| SUN PRO-M2 | 64bit | Micron | SA00005XB10 | MT41K128M16JT-107G.K | X7648051L03 | 2Gbit | 128M*16 | 1GB/4pcs | 0 | 0 | 1 | RV20 8.45K | RV27 2K |
| SUN PRO-M2 | 64bit | Samsung | SA00005SH40 | K4W2G1646E-BC11 | X7648051L04 | 2Gbit | 128M*16 | 1GB/4pcs | 1 | 1 | 1 | RV20 4.75K | RV27 NC |
| SUN PRO-M2 | 64bit | Samsung | SA000068U20 | K4W2G1646E-BC1A | X7648051L05 | 2Gbit | 128M*16 | 1GB/4pcs | 1 | 1 | 0 | RV20 3.4K | RV27 10K |

CHANNEL B: 512MB/1024MB DDR3

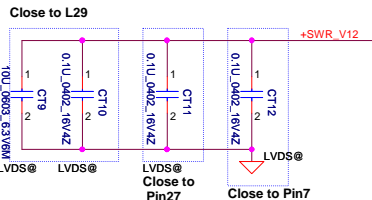
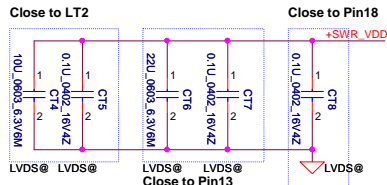
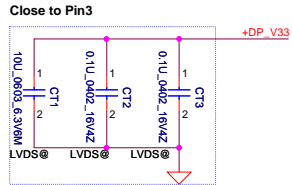
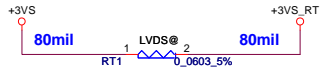


Supported Memory Configurations: Up to 4 Gbit/part for DDR3.

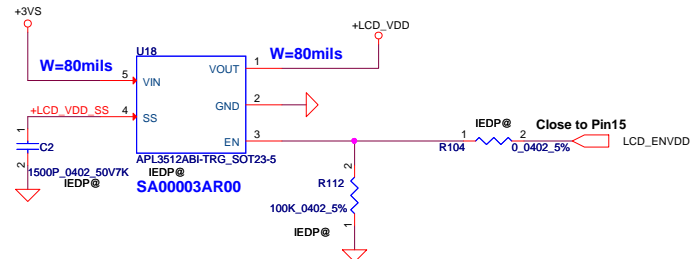


| | | | | |
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| Issued Date | 2013/03/20 | Deciphered Date | 2014/03/20 | VRAM Channel B |
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| Size | Document Number | Date | | Rev |
| C | LA-9869P | Wednesday, March 20, 2013 | | 1.0 |
| | | ISheet | | of 51 |

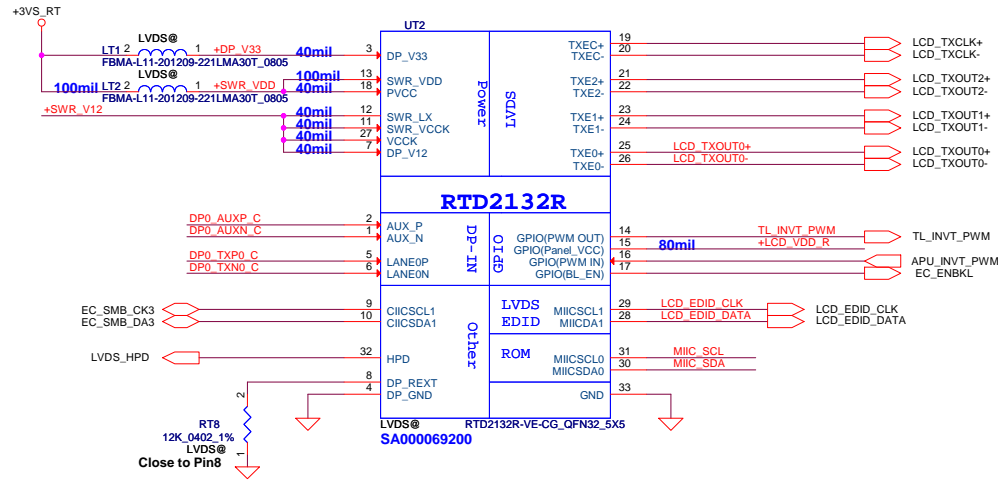
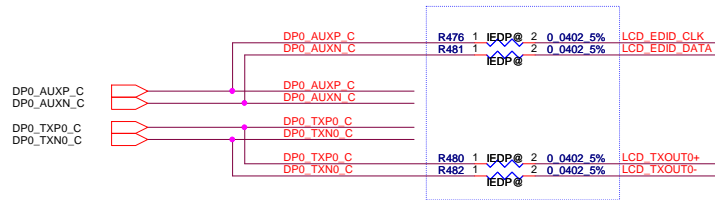
| SWR / LDO Mode select | | |
|--|------|-----|
| | LDO | SWR |
| 2132R | RT24 | |
| ※ If use 2132R, please select LDO mode as default. | | |



LCD POWER CIRCUIT (For eDP panel only)



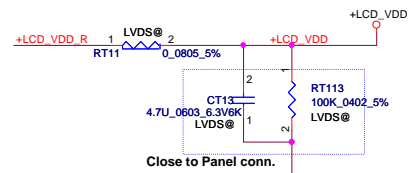
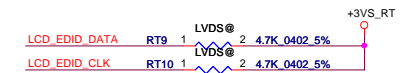
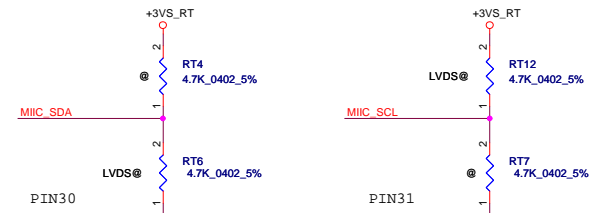
R476/481/480/482 need to place under UT2
In order to reduce sub-trace



Mode Configure

ROM only mode : PIN 30 4.7k pull low, Pin 31 4.7k pull high.
 ※EP mode : PIN 30 4.7k pull high, Pin 31 4.7k pull low.
 EEPROM : PIN 30 4.7k pull high, Pin 31 4.7k pull high.

< ※Default mode >



| | PIN15 |
|-------|-----------|
| 2132S | TL_ENVDD |
| 2132R | +LCD_VDD* |

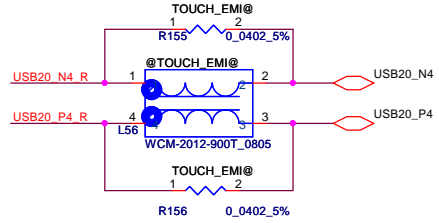
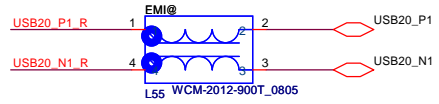
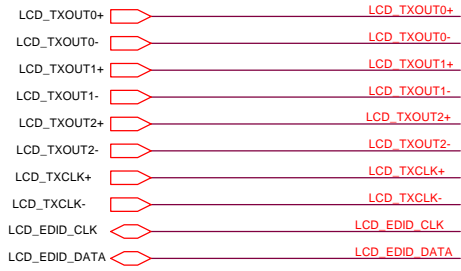
* Version R internal Power Switch, can output 1A, Rds(on)=0.2 ohm

| PIN16 | Accept voltage input (high level) |
|-------|-----------------------------------|
| 2132S | 3.3V |
| 2132R | 1.5~3.3V |

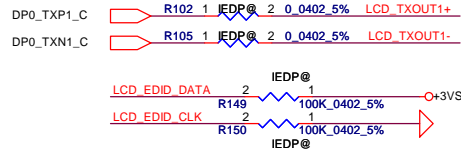
* Version R has internal level shifter, remove level shifter circuit on AMD platform

| Different between 2132S and 2132R | |
|-----------------------------------|---|
| 2132S | 2132R |
| 1. Support SWR mode | 1. Support LDO mode and SWR mode 2. Internal ROM 3. Support LCD_VDD(internal Power switch) 4. Integrates Level shifter |

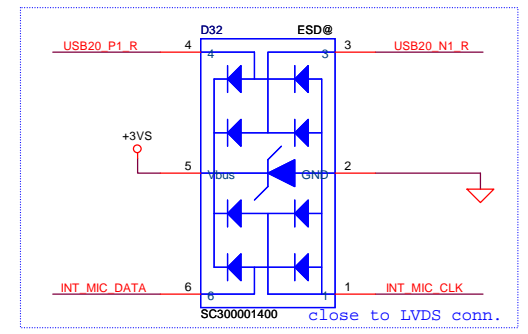
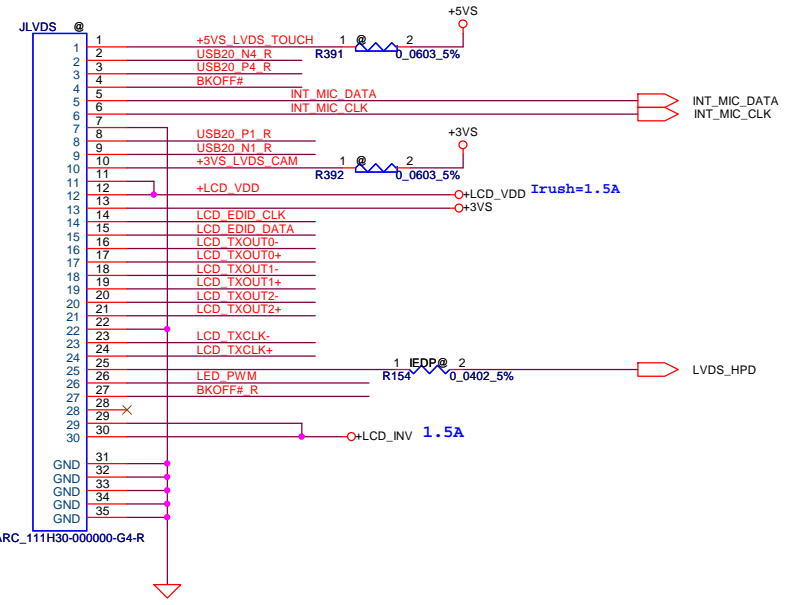
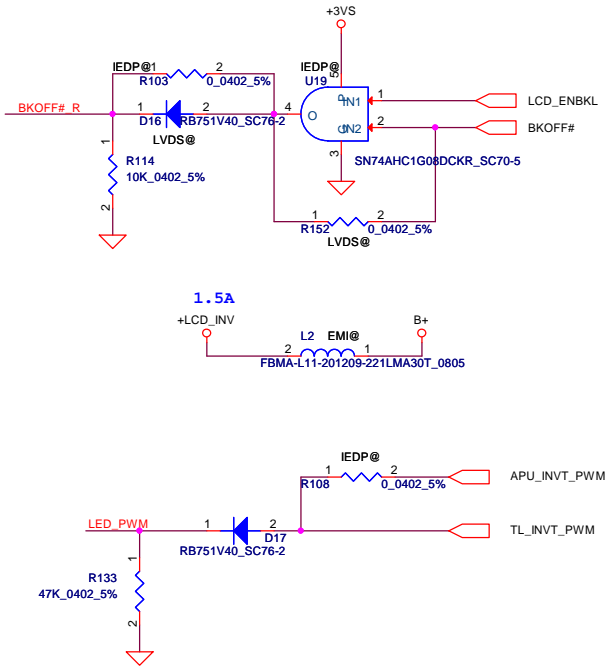
For LVDS 1ch Panel



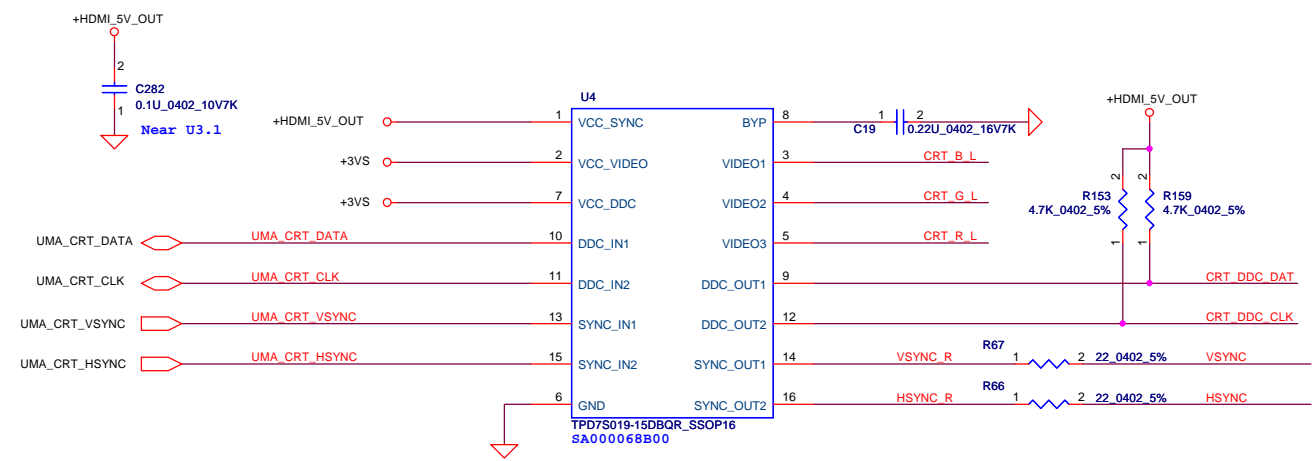
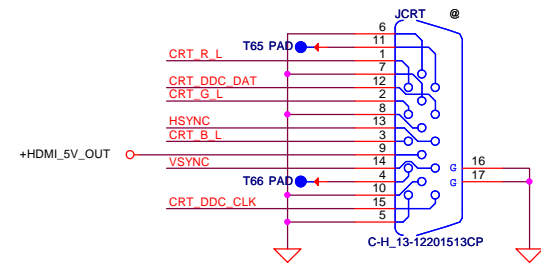
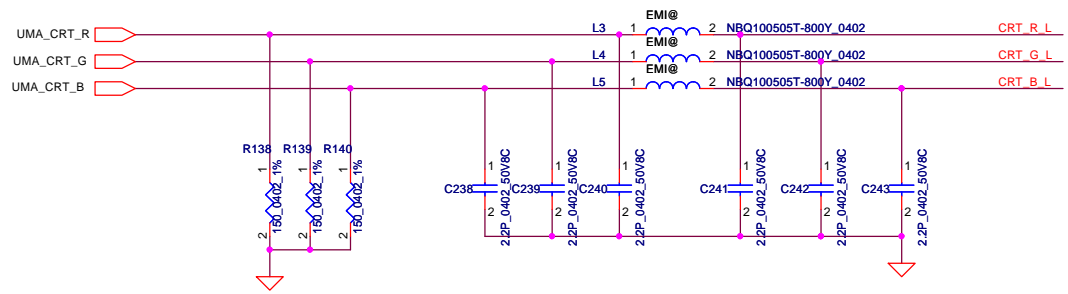
For eDP Panel



Reserve for eDP panel potience issue



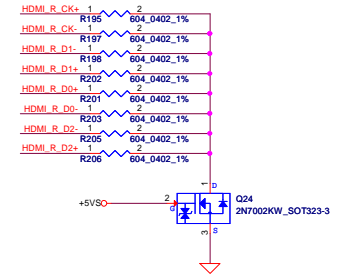
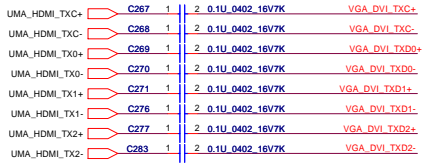
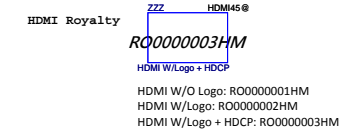
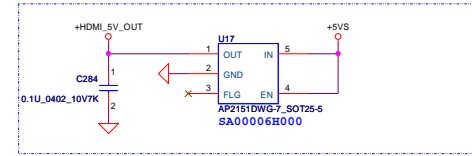
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| Issued Date | 2013/03/20 | Deciphered Date | 2014/03/20 | Title | |
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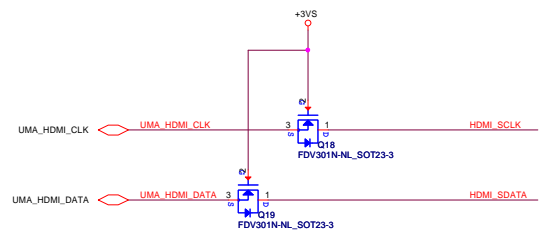
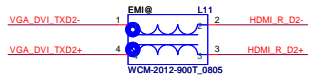
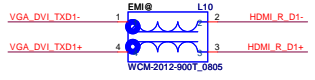
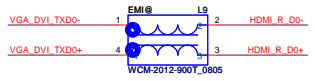
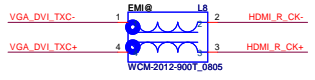
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| Issued Date | 2013/03/20 | Deciphered Date | 2014/03/20 | Title CRT | |
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| | | | | Date | Wednesday, March 20, 2013 |
| | | | | Sheet | 21 of 51 |
| | | | | Rev | 1.0 |

HDMI POWER CIRCUIT

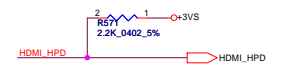
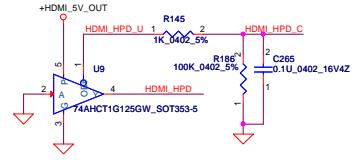
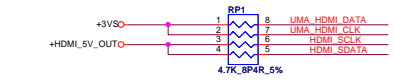
VIN = 5V, IOUT = 0.5A, RDS(ON) TYP=95m ; MAX=115m
 Current Limit: TYP=0.8A ; MAX=1A



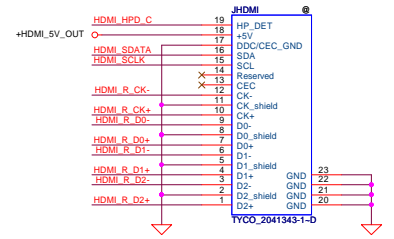
Change R184 and R185 from 2K to 4.7K for HDMI detect issue on Comal



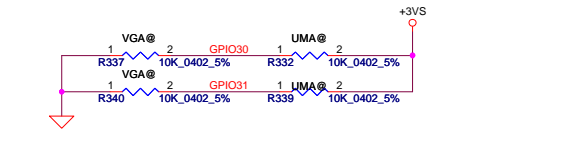
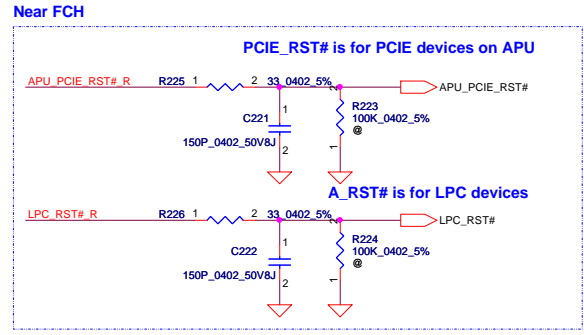
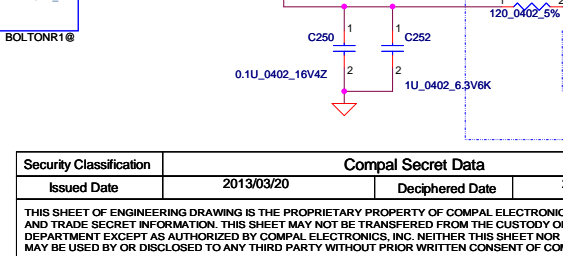
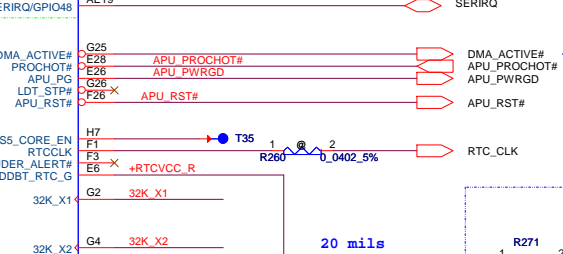
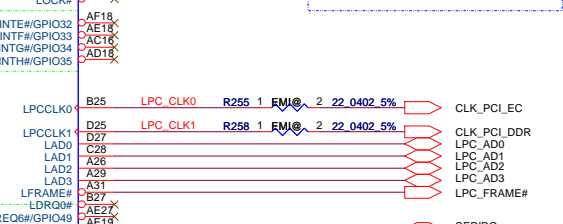
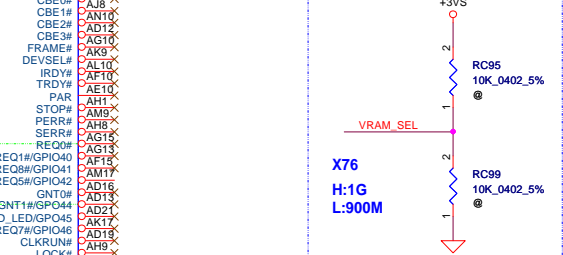
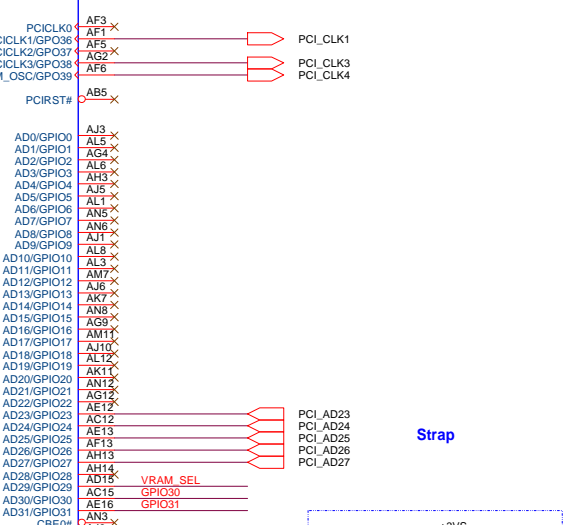
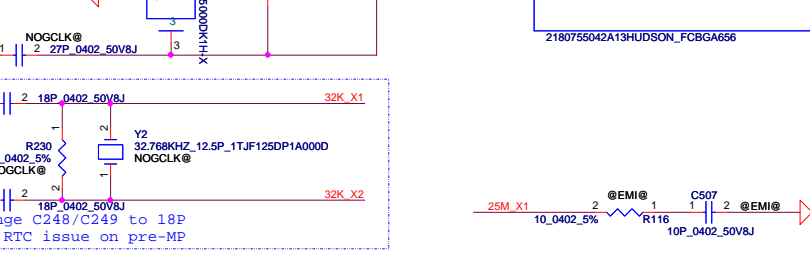
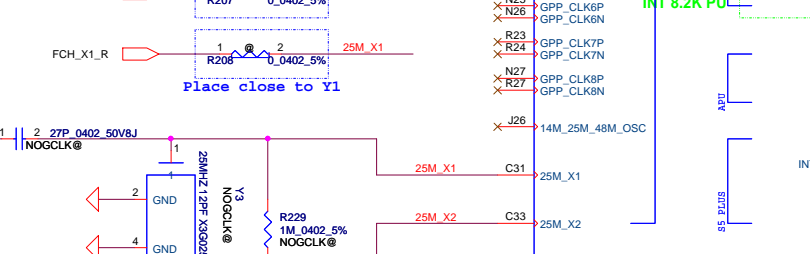
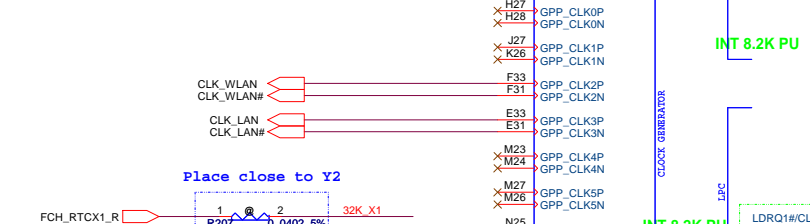
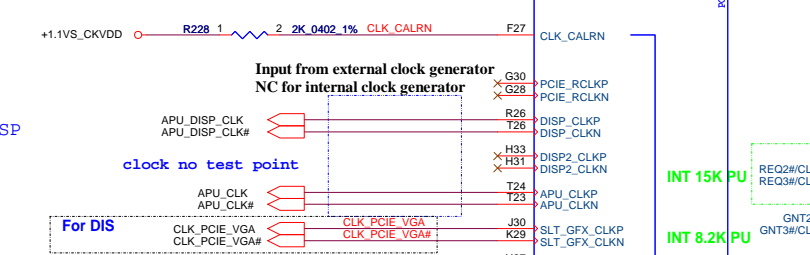
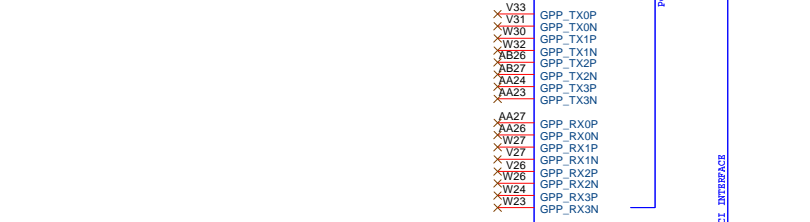
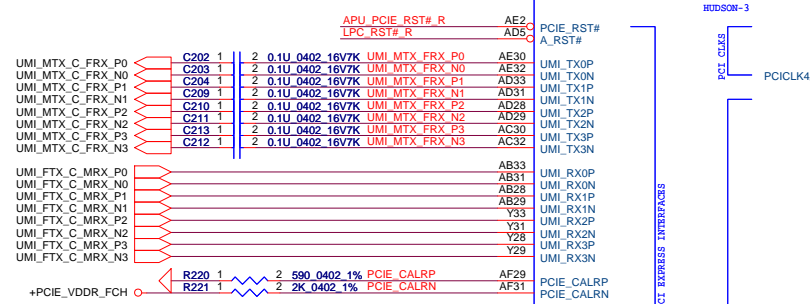
Q18/Q19 Change to FDV301 due to BSH111 EOL



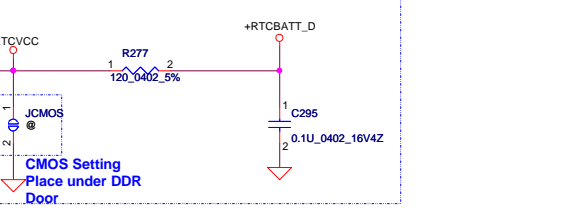
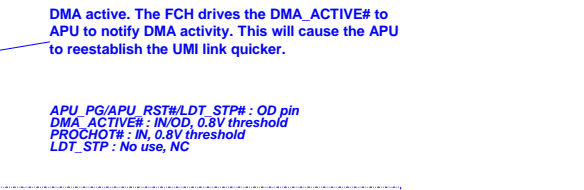
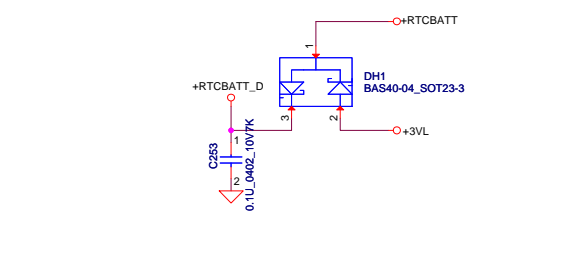
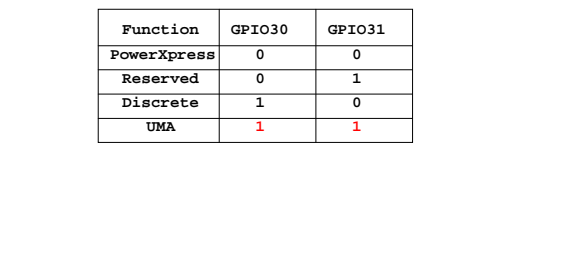
HDMI Connector

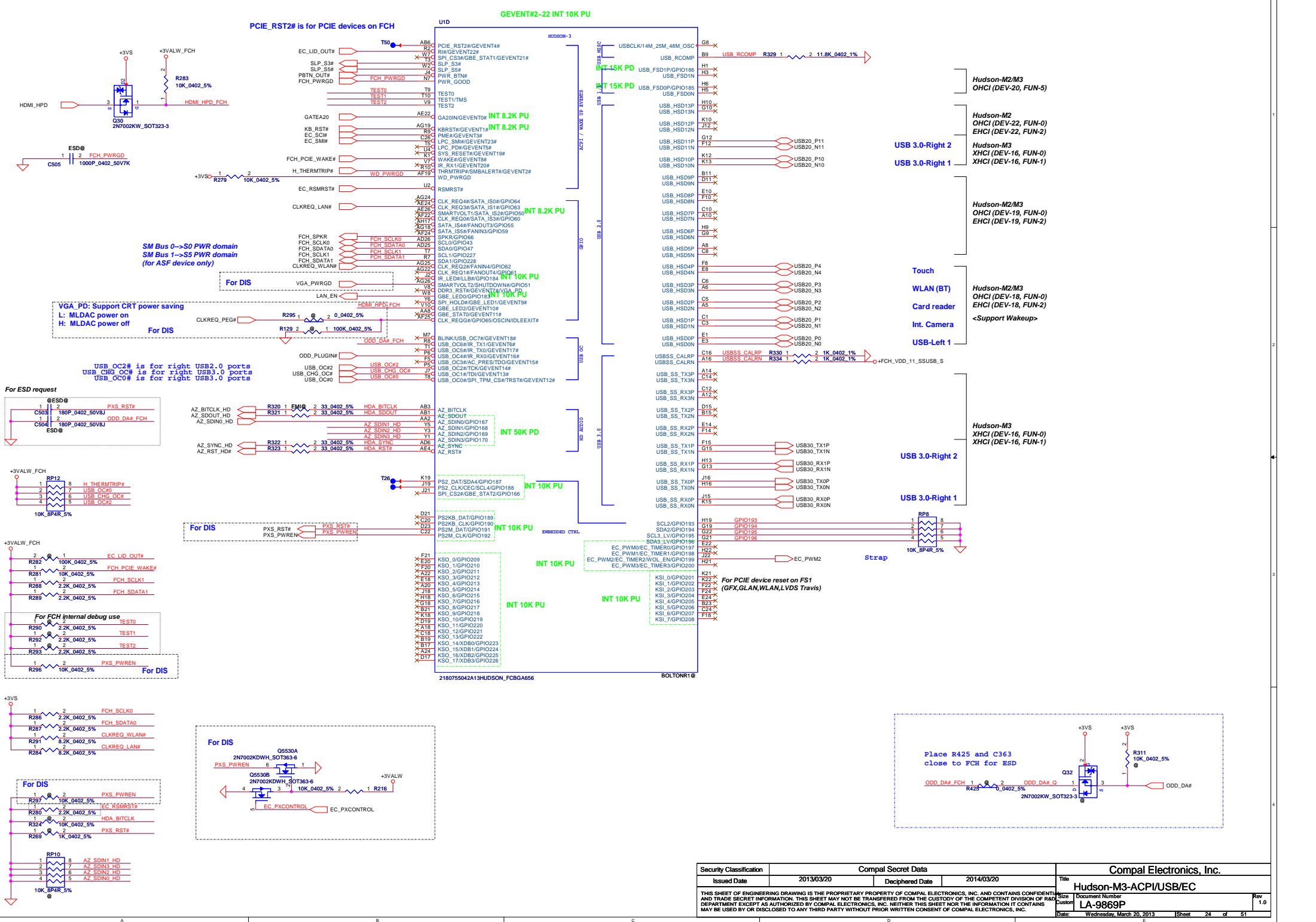


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| Size | Document Number | Rev | Date: Wednesday, March 20, 2013 Sheet 22 of 51 | | |
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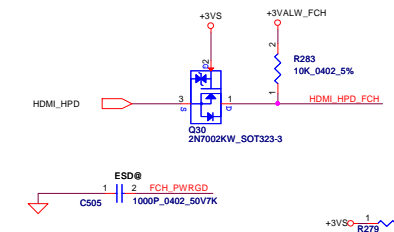
| Function | GPIO30 | GPIO31 |
|-------------|--------|--------|
| PowerXpress | 0 | 0 |
| Reserved | 0 | 1 |
| Discrete | 1 | 0 |
| UMA | 1 | 1 |





PCIE_RST2# is for PCIE devices on FCH

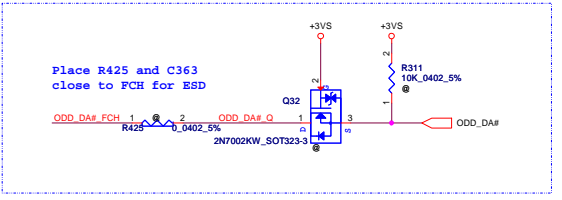
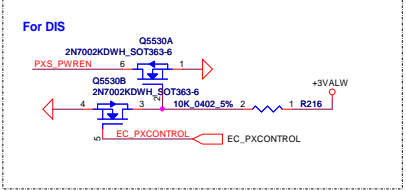
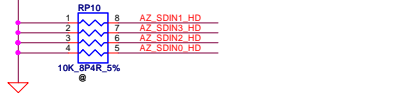
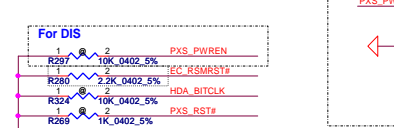
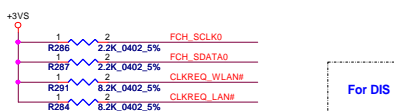
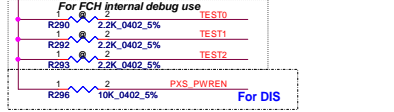
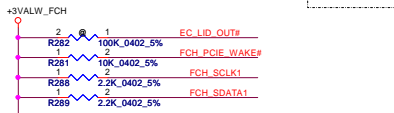
GEVENT#2-22 INT 10K PU



SM Bus 0 -> S0 PWR domain
SM Bus 1 -> S5 PWR domain
(for ASF device only)

VGA_PD: Support CRT power saving
L: MLDAC power on
H: MLDAC power off

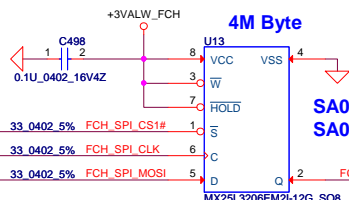
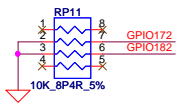
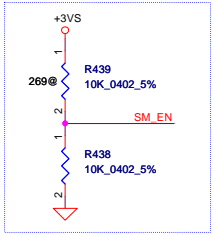
USB_OC2# is for right USB2.0 ports
USB_OC4# is for right USB3.0 ports
USB_OC0# is for right USB3.0 ports



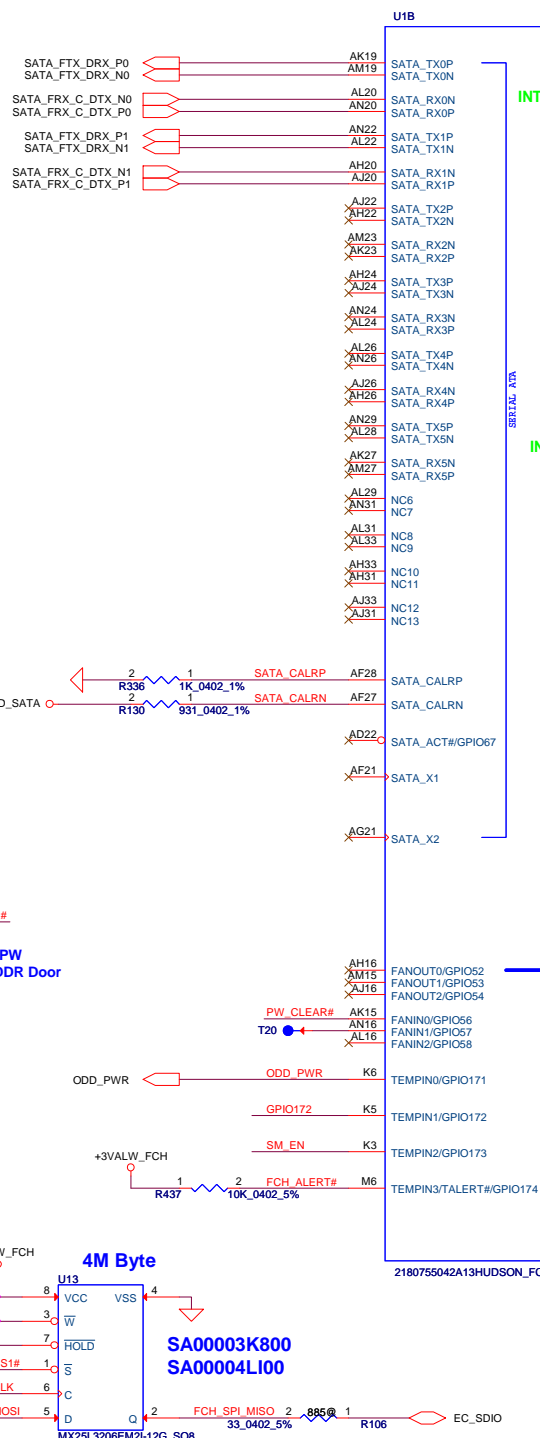
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|---|---------------------------|-----------------|------------|--------------------------|-----------------------|
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| Issued Date | 2013/03/20 | Deciphered Date | 2014/03/20 | Document Number | Hudson-M3-ACPI/USB/EC |
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HDD
ODD

| SM_EN | BIOS SETUP | SPK TYPE |
|-------|------------|---------------|
| 1 | S&M OPTION | HARMAN KARDON |
| 0 | NO | NO HARMAN |



Socket PN: SP07000F500/SP07000H900



INT 8.2K PU

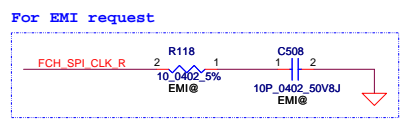
INT 10K PU

| Security Classification | Compal Secret Data | |
|-------------------------|--------------------|-----------------|
| Issued Date | 2013/03/20 | Deciphered Date |
| | | 2014/03/20 |

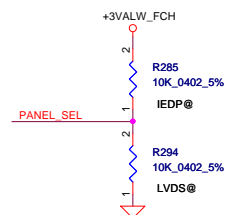
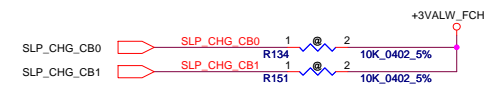
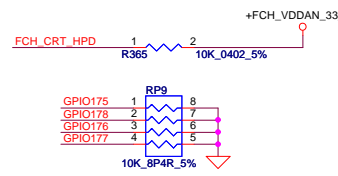
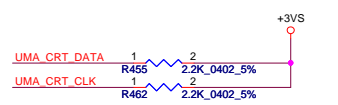
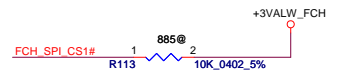
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HDMI_EN# (Internal 8.2K PU)

| HDMI_EN# | H | L |
|----------|--------------|----------|
| SKU | Non-HDMI SKU | HDMI SKU |



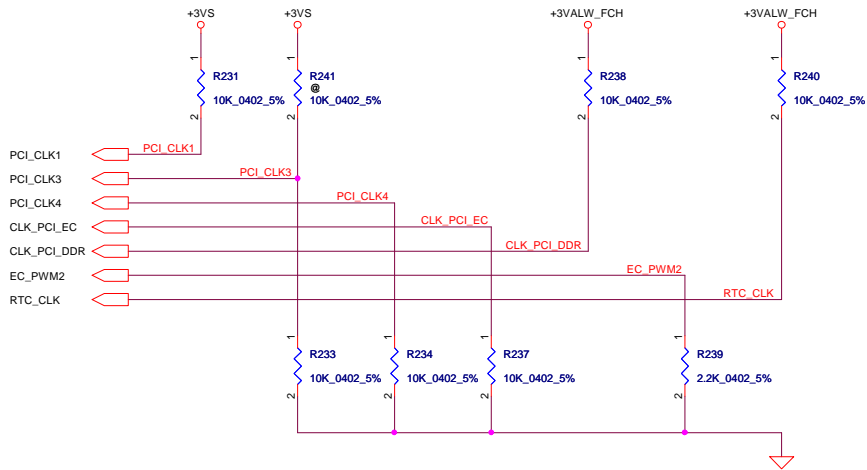
If an SPI ROM is shared between FCH and the Embedded Controller, a 10-k pull-up resistor to +3.3V_S5 is installed



| Compal Electronics, Inc. | |
|--------------------------|---------------------------|
| Hudson-M3-SATA/GBE/HWM | |
| Title | LA-9869P |
| Docment Number | LA-9869P |
| Date | Wednesday, March 20, 2013 |
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STRAP PINS

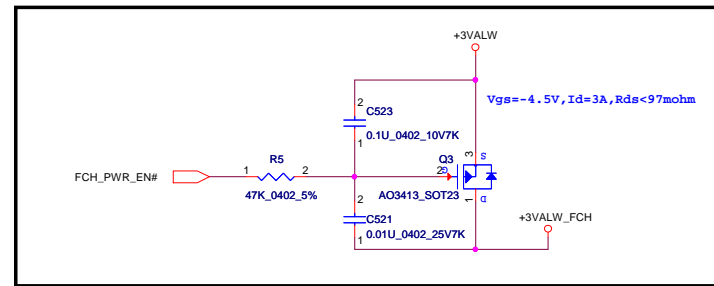
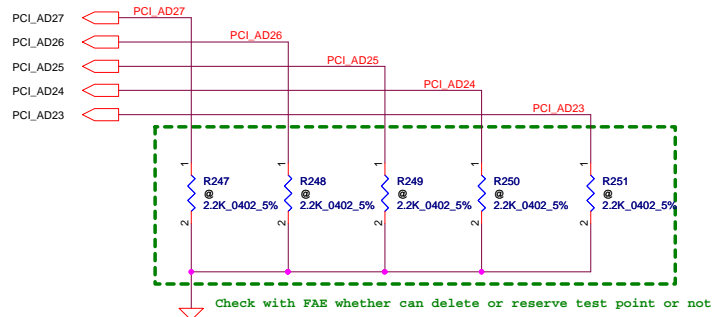
| | PCI_CLK1 | PCI_CLK3 | PCI_CLK4 | LPC_CLK0 | LPC_CLK1 | EC_PWM2 | RTC_CLK |
|------------------|-----------------------------------|---------------------------------------|-------------------------------------|-------------------------------|----------------|--|---|
| PULL HIGH | ALLOW PCIE GEN2 <i>DEFAULT</i> | ENABLE DEBUG STRAP | NON_FUSION CLOCK MODE | EC ENABLED | CLKGEN ENABLED | LPC ROM (INTERNAL 10K PULL-UP) <i>DEFAULT</i> | S5 PLUS MODE DISABLED <i>DEFAULT</i> |
| PULL LOW | FORCE PCIE GEN1 | DISABLE DEBUG STRAP <i>DEFAULT</i> | FUSION CLOCK MODE <i>DEFAULT</i> | EC DISABLED <i>DEFAULT</i> | CLKGEN DISABLE | SPI ROM <i>DEFAULT</i> | S5 PLUS MODE ENABLED |



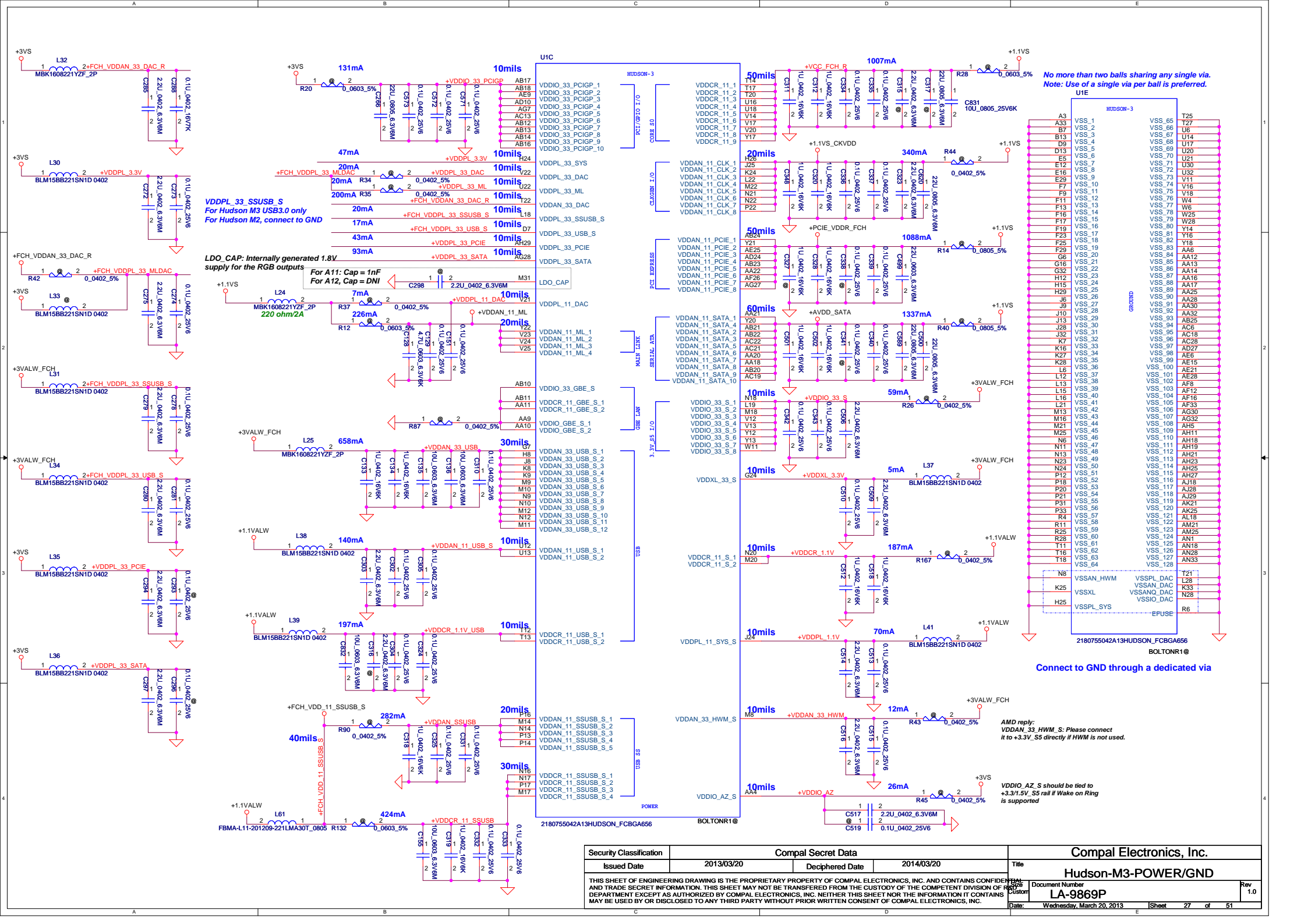
DEBUG STRAPS

FCH HAS 15K INTERNAL PU-UP FOR PCI_AD[27:23]

| | PCI_AD27 | PCI_AD26 | PCI_AD25 | PCI_AD24 | PCI_AD23 |
|------------------|-------------------------------|---------------------------------------|------------------------------|---|--|
| PULL HIGH | USE PCI PLL <i>DEFAULT</i> | DISABLE ILA AUTORUN <i>DEFAULT</i> | USE FC PLL <i>DEFAULT</i> | USE DEFAULT PCIE STRAPS <i>DEFAULT</i> | DISABLE PCI MEM BOOT <i>DEFAULT</i> |
| PULL LOW | BYPASS PCI PLL | ENABLE ILA AUTORUN | BYPASS FC PLL | USE EEPROM PCIE STRAPS | ENABLE PCI MEM BOOT |

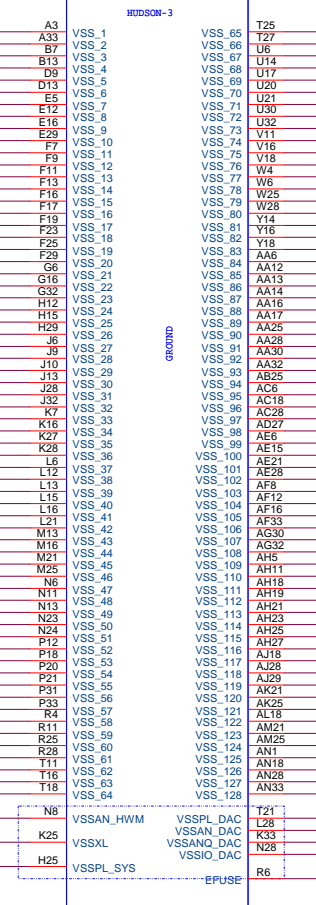


| | | | | | |
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| Date | | | | Document Number | Rev |
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No more than two balls sharing a single via.
 Note: Use of a single via per ball is preferred.

U1E



2180755042A13HUDSON_FCBA656

BOLTONR1@

Connect to GND through a dedicated via

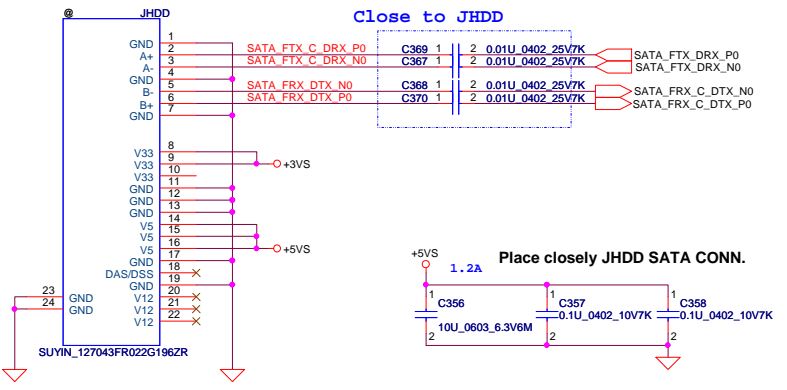
AMD reply:
 VDDAN_33_HWM_S: Please connect it to +3.3V_S5 directly if HWM is not used.

VDDIO_AZ_S should be tied to +3.3V_S5. S5 rail if Wake on Ring is supported

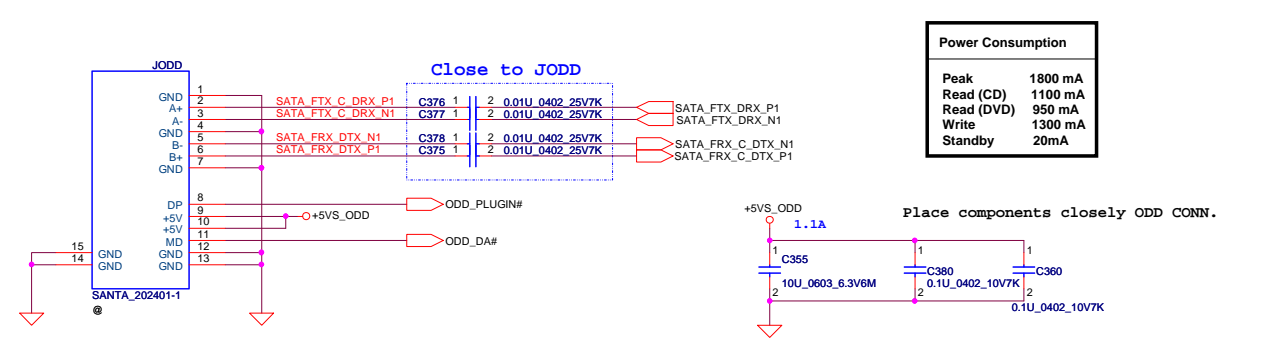
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| Security Classification | Compal Secret Data | |
| Issued Date | 2013/03/20 | Deciphered Date |
| | | 2014/03/20 |
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| Compal Electronics, Inc. | |
| Hudson-M3-POWER/GND | |
| Document Number | LA-9869P |
| Date: | Wednesday, March 20, 2013 |
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SATA HDD Conn.

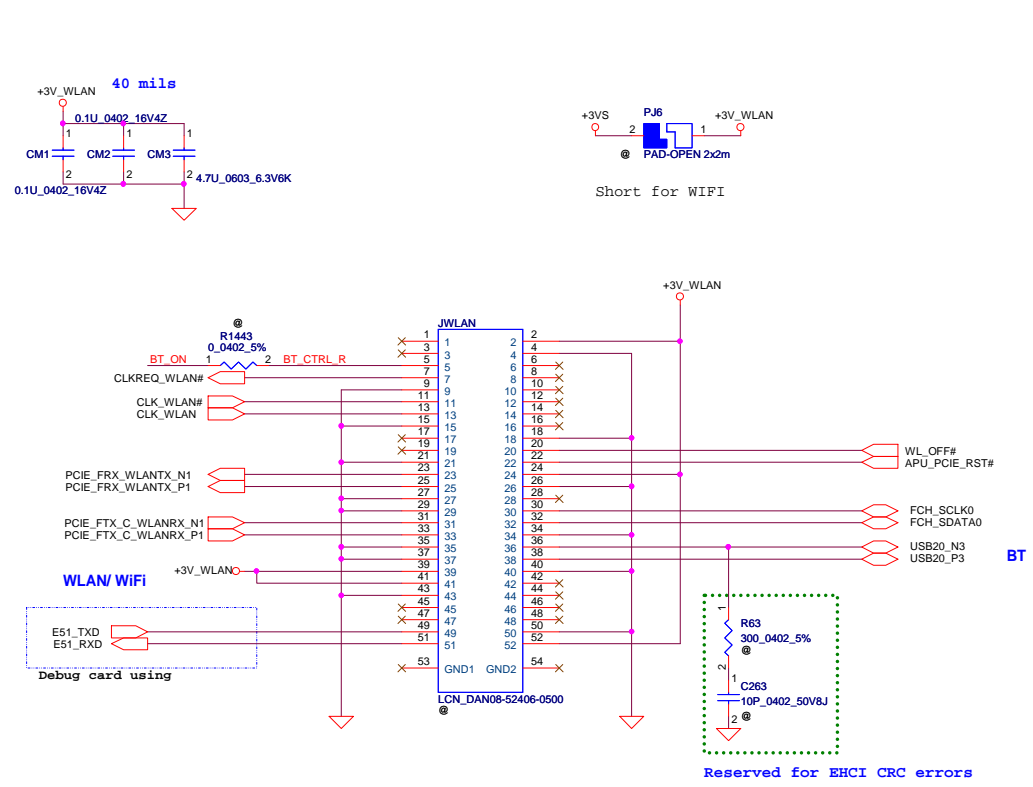


SATA ODD Conn



| Power Consumption | |
|-------------------|---------|
| Peak | 1800 mA |
| Read (CD) | 1100 mA |
| Read (DVD) | 950 mA |
| Write | 1300 mA |
| Standby | 20mA |

Slot 1 Half PCIe Mini Card-WLAN



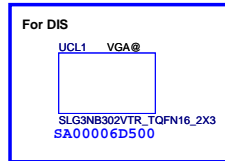
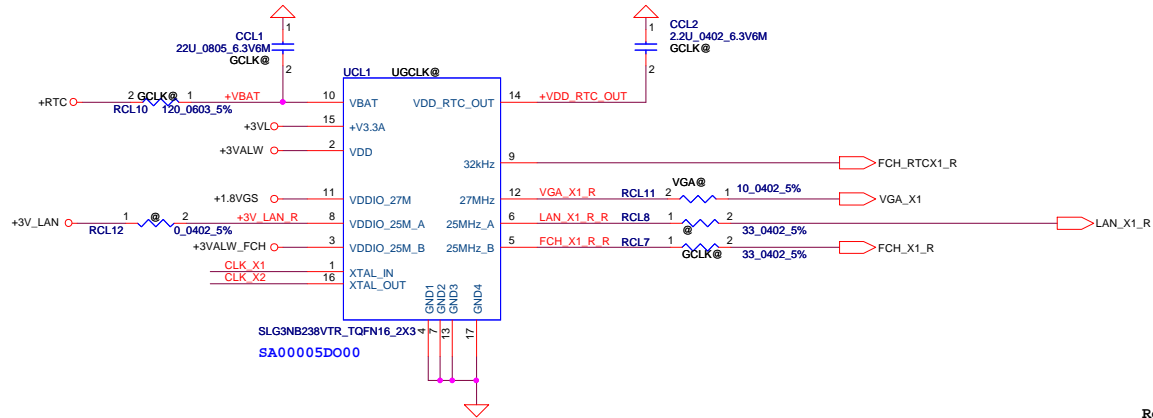
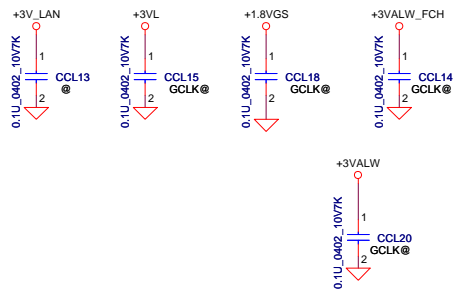
WLAN&BT Combo module circuits

| | BT on module Enable | BT on module Disable |
|-------|---------------------|----------------------|
| BT_ON | H | L |

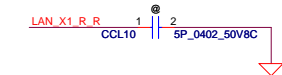
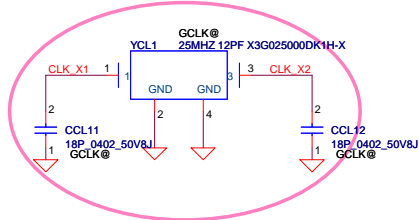
BT_ON \Rightarrow BT_ON 1 R327 2 E51_RXD 1K_0402_5%

For isolate BT_CTRL and Compal Debug Card.

Green Clock Generator



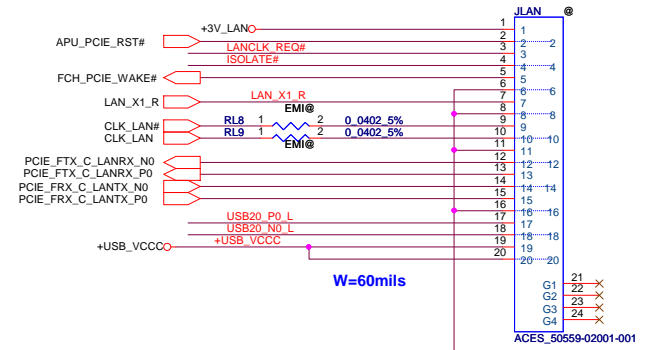
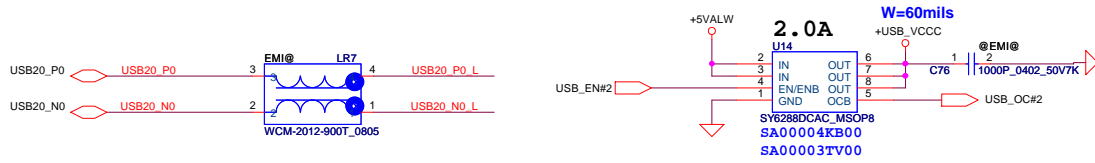
change part number to
SJ10000EF00



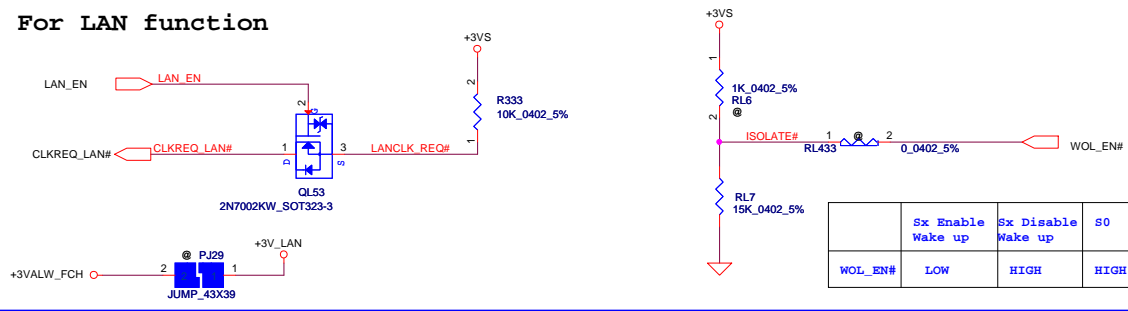
Reserved for Swing Level adjustment
(Close GCLK side)

| | | | | | |
|---|---------------------------|-----------------|------------|-----------------------|-----|
| Security Classification | Compal Secret Data | | Title | PCIe-WLAN/GCLK | |
| Issued Date | 2013/03/20 | Deciphered Date | 2014/03/20 | Document Number | Rev |
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| Date: | Wednesday, March 20, 2013 | Sheet | 29 | of | 51 |

Left USB 2.0 x 1



For LAN function



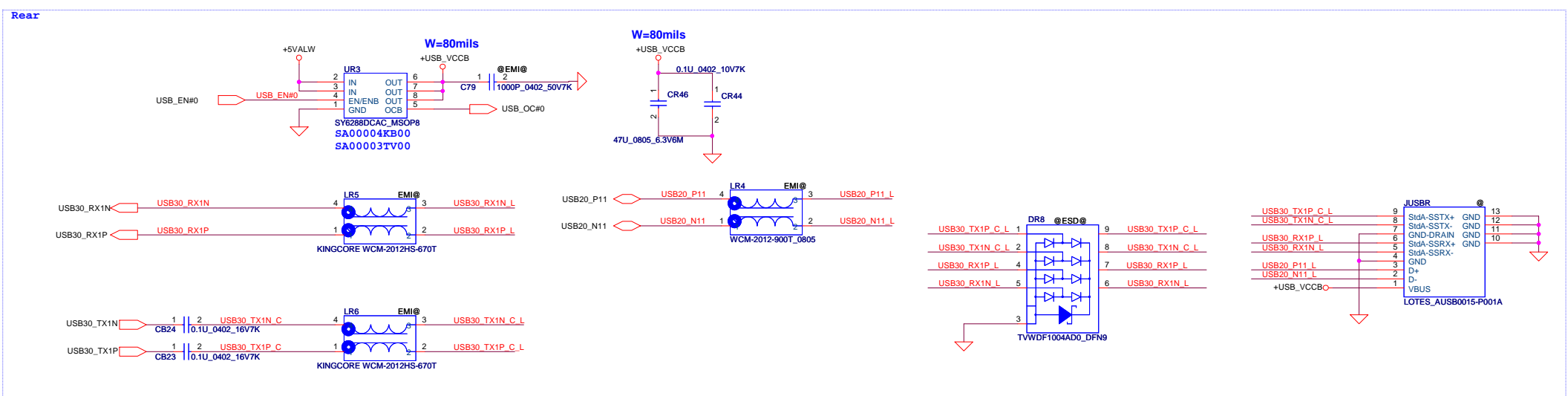
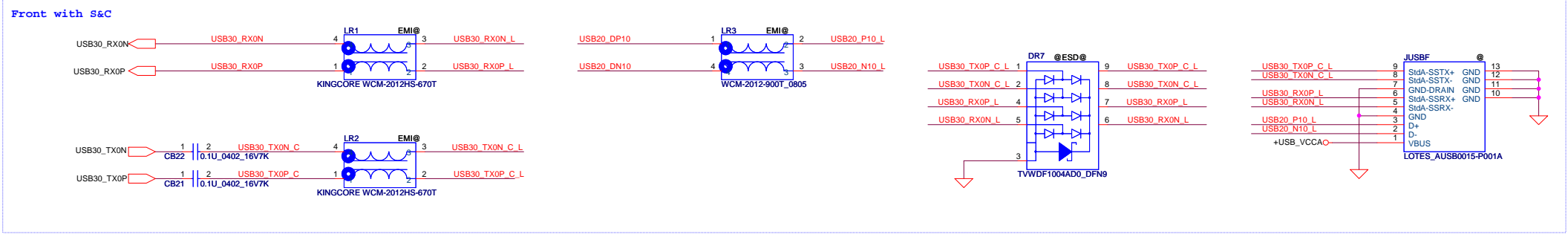
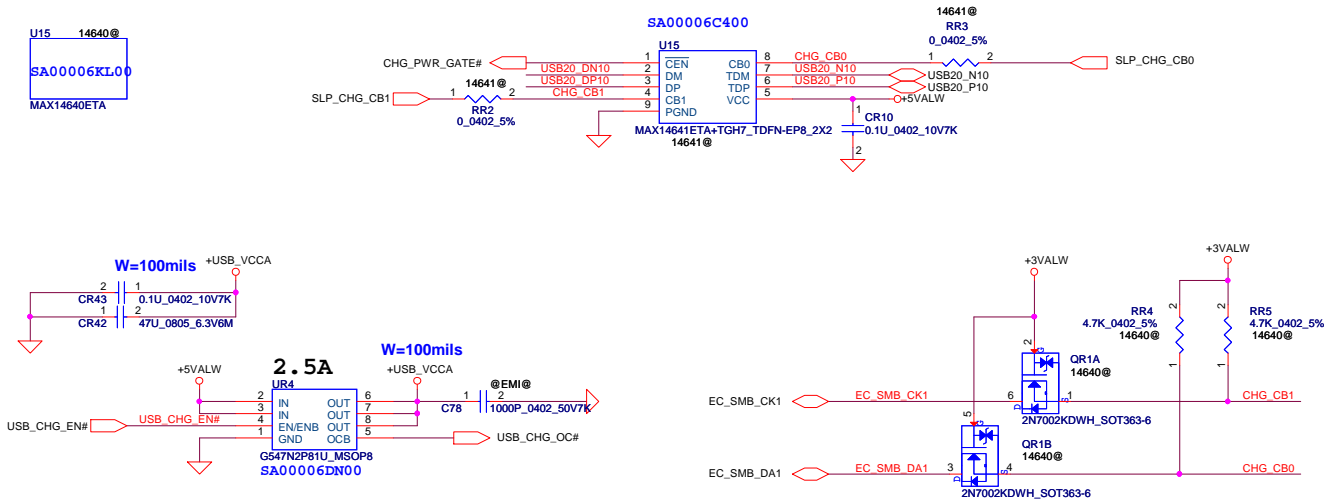
+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

| LAN | WOL | LAN_EN | | ISOLATEB | |
|-----|-----|--------|----|----------|----|
| | | S0 | Sx | S0 | Sx |
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0* |

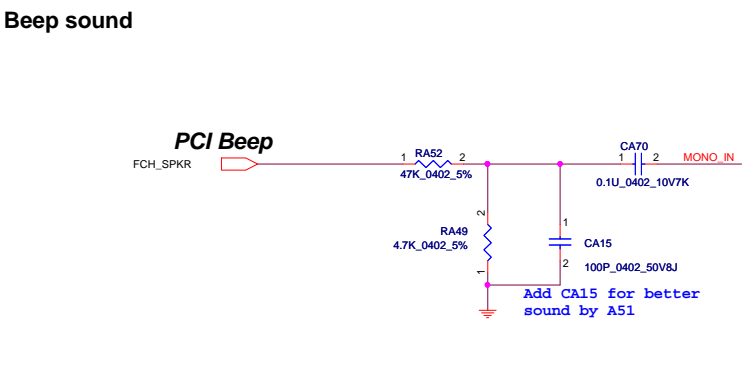
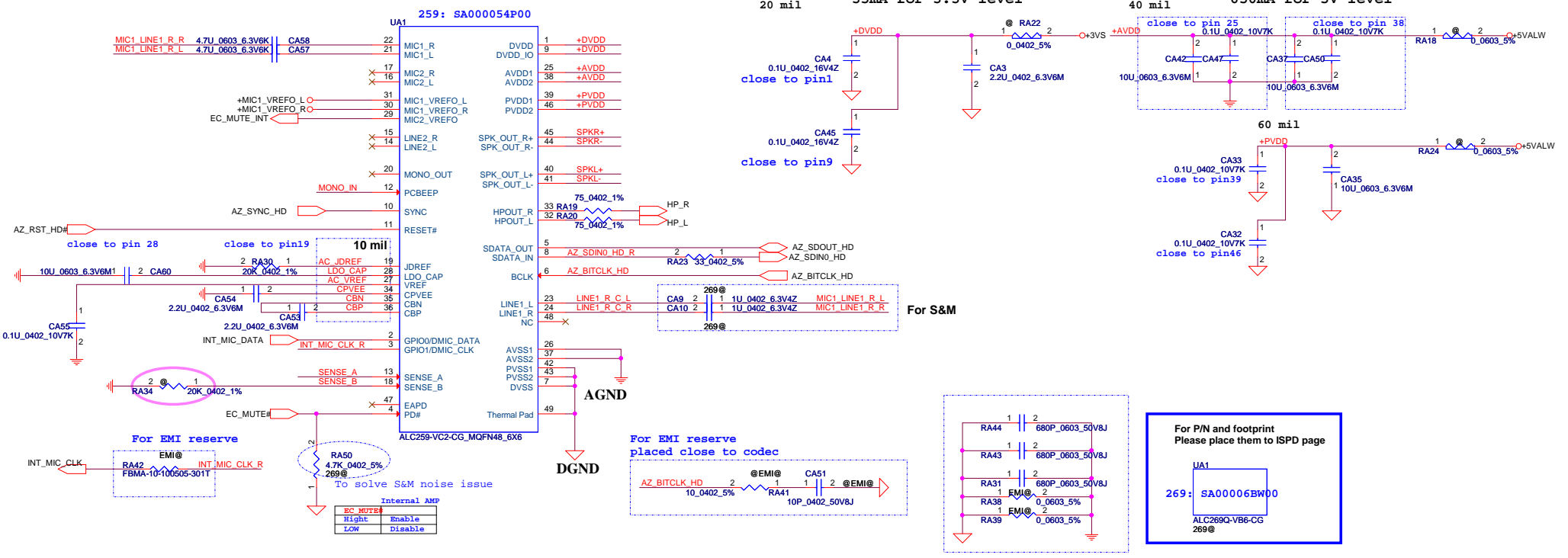
*
S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms

USB Sleep & Charge

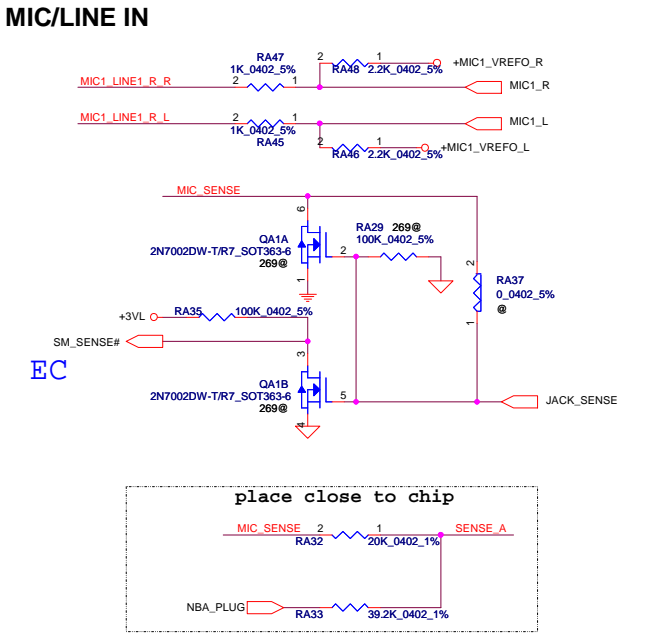
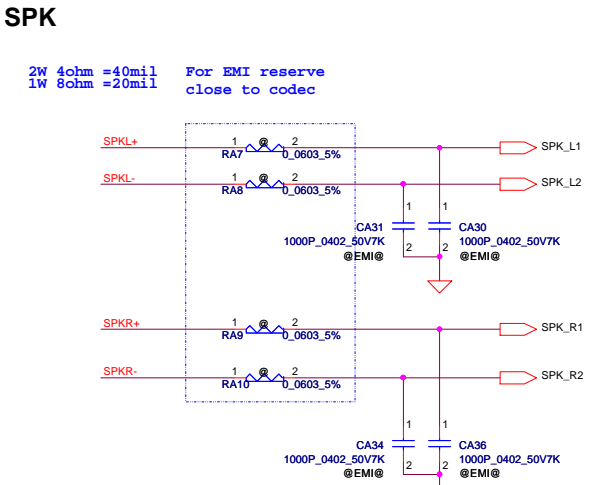
| State table for MAX14641 | | | |
|--------------------------|-----|------|---|
| CB0 | CB1 | Mode | STATUS |
| 0 | 0 | AM2 | 2A auto-detection charger mode for Apple device. Resistor dividers are connected to DP/DM. Including DCP |
| 0 | 1 | AP1 | Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM. |
| 1 | 0 | PM | USB pass-through mode. DP/DM are connected to TDP/TDM |
| 1 | 1 | CM | USB pass-through mode with CDP emulation. Auto connects DP/DM to TDP/TDM depending on CDP detection status. |



| | | | | | |
|---|--------------------|-----------------|------------|---------------------------------|----------------|
| Security Classification | Compal Secret Data | | | Title | |
| Issued Date | 2013/03/20 | Deciphered Date | 2014/03/20 | USB3.0 | |
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| | | | | LA-9869P | 1.0 |
| | | | | Date: Wednesday, March 20, 2013 | Sheet 31 of 51 |



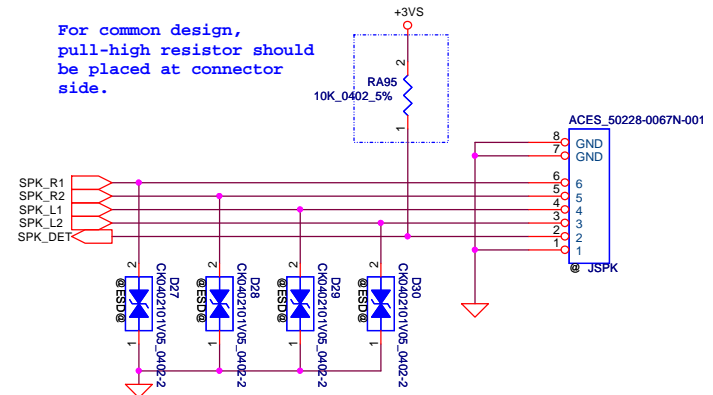
| Sense Pin | Impedance | Codec Signals | Function |
|-----------|-----------|---------------------|---------------|
| SENSE A | 39.2K | PORT-I (PIN 32, 33) | Headphone out |
| | 20K | PORT-B (PIN 21, 22) | Ext. MIC |
| | 10K | PORT-C (PIN 23, 24) | |
| SENSE B | 5.1K | (PIN 48) | |
| | 39.2K | PORT-E (PIN 14, 15) | |
| | 20K | PORT-F (PIN 16, 17) | |
| | 10K | PORT-H (PIN 20) | |



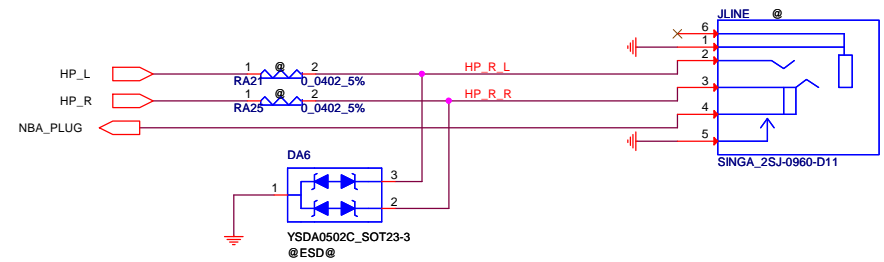
SPK CONN.

| | | |
|----------|----------------------|-----------|
| | Non-Harman detection | |
| SPK_DET0 | 0 | ONKYO |
| | 1 | Non-Brand |

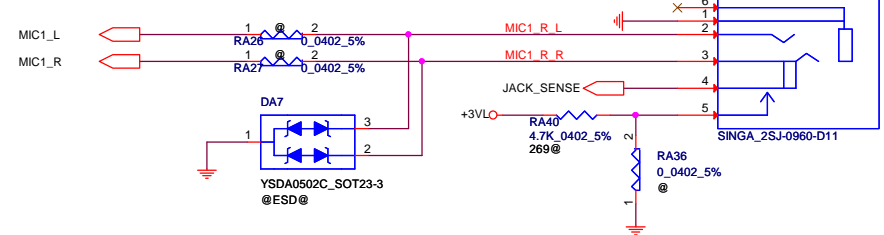
Please check SPK_DET pull high 10K to +3VS



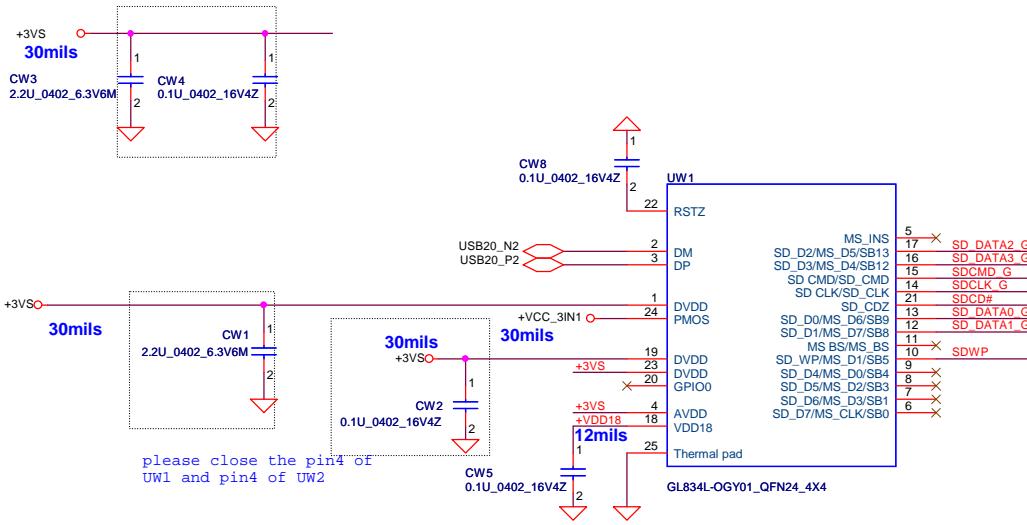
HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK



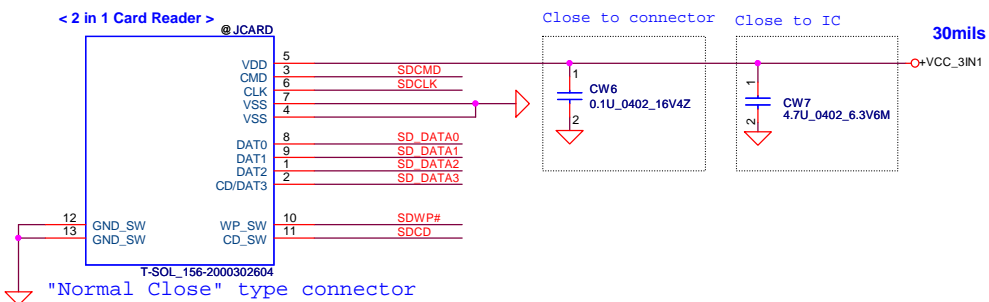
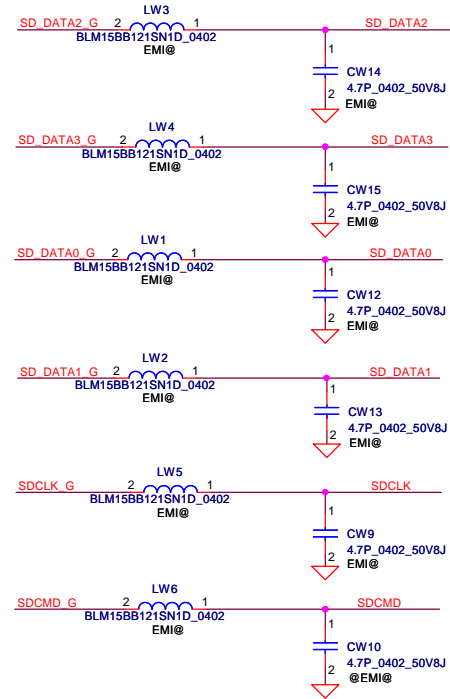
| | | | | |
|---|---------------------------|-----------------|------------|--------------------------|
| Security Classification | Compal Secret Data | | Title | |
| Issued Date | 2013/03/20 | Deciphered Date | 2014/03/20 | Compal Electronics, Inc. |
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| | | | | Size |
| | | | LA-9869P | 1.0 |
| Date: | Wednesday, March 20, 2013 | Sheet | 33 | of 51 |



please close the pin4 of UW1 and pin4 of UW2

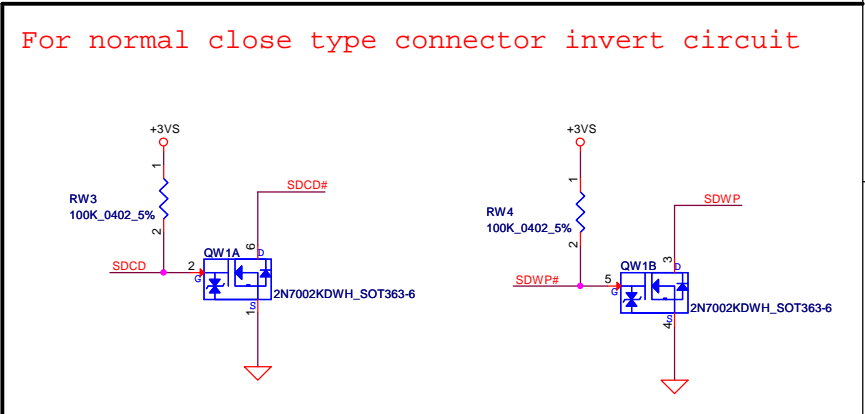
| | | |
|--------|-------------------|---------------|
| | NC (default) | 10K pull down |
| GPIIO0 | Power saving mode | Normal mode |

De-coupling and Bulk capacitor should place near to Cardreader chip and Combo Socket



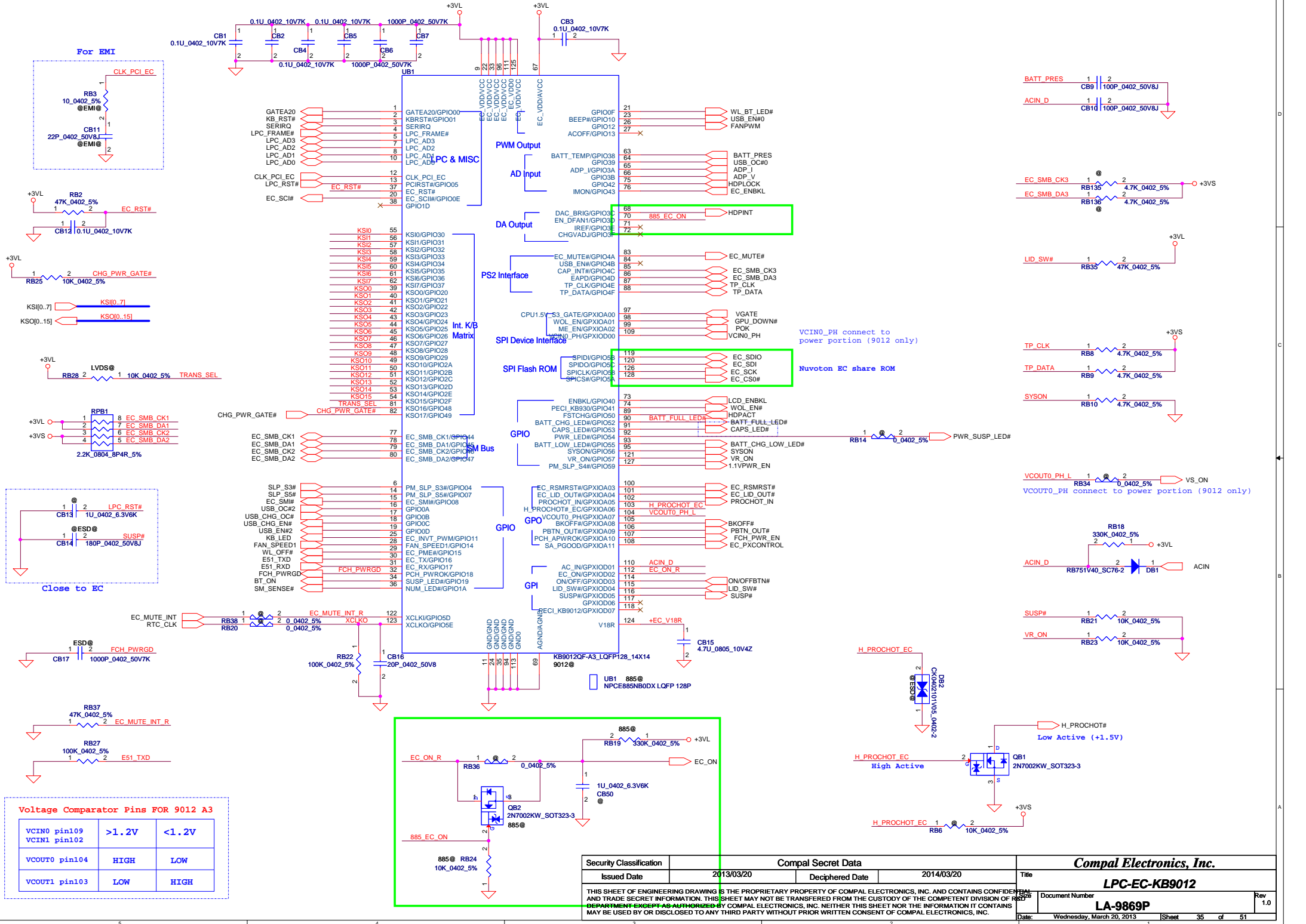
"Normal Close" type connector

| | CD_SW | WP_SW | |
|------------------|-------|-----------------|----------------|
| Card Uninsertion | Close | Protect disable | Protect Enable |
| | | Close | Close |
| Card Insertion | Open | Open | Close |



For normal close type connector invert circuit

| | | | | | |
|---|------------|--------------------|------------|-------------------------------|-----------------|
| Security Classification | | Compal Secret Data | | Title | |
| Issued Date | 2013/03/20 | Deciphered Date | 2014/03/20 | USB-CardReader GL834L/RTS5170 | |
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| | | | | LA-9869P | Rev 1.0 |
| Date: Wednesday, March 20, 2013 | | | | Sheet | 34 of 51 |



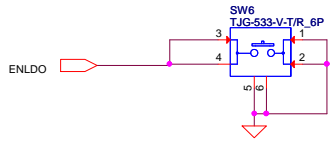
Voltage Comparator Pins FOR 9012 A3

| VCIN0 pin109 | >1.2V | <1.2V |
|---------------|-------|-------|
| VCOUT0 pin104 | HIGH | LOW |
| VCOUT1 pin103 | LOW | HIGH |

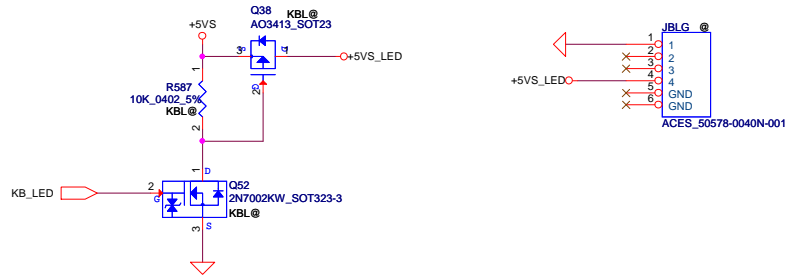
| Security Classification | | Compal Secret Data | |
|--|------------|--------------------|------------|
| Issued Date | 2013/03/20 | Deciphered Date | 2014/03/20 |
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| Compal Electronics, Inc. | | | |
|--------------------------|---------------------------|-------|----------|
| LPC-EC-KB9012 | | | |
| Document Number | LA-9869P | | Rev |
| Date: | Wednesday, March 20, 2013 | Sheet | 35 of 51 |

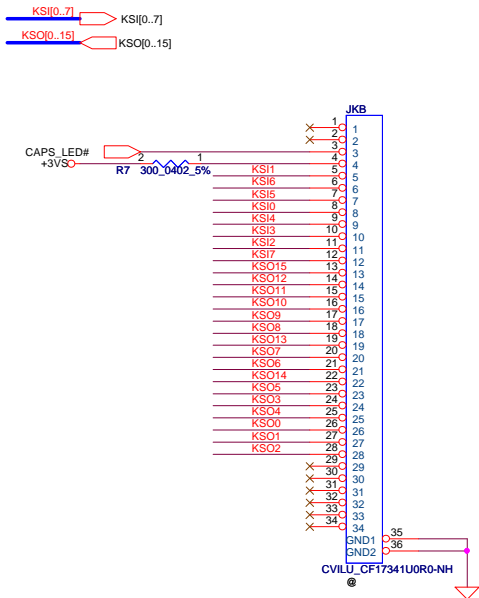
Battery Reset



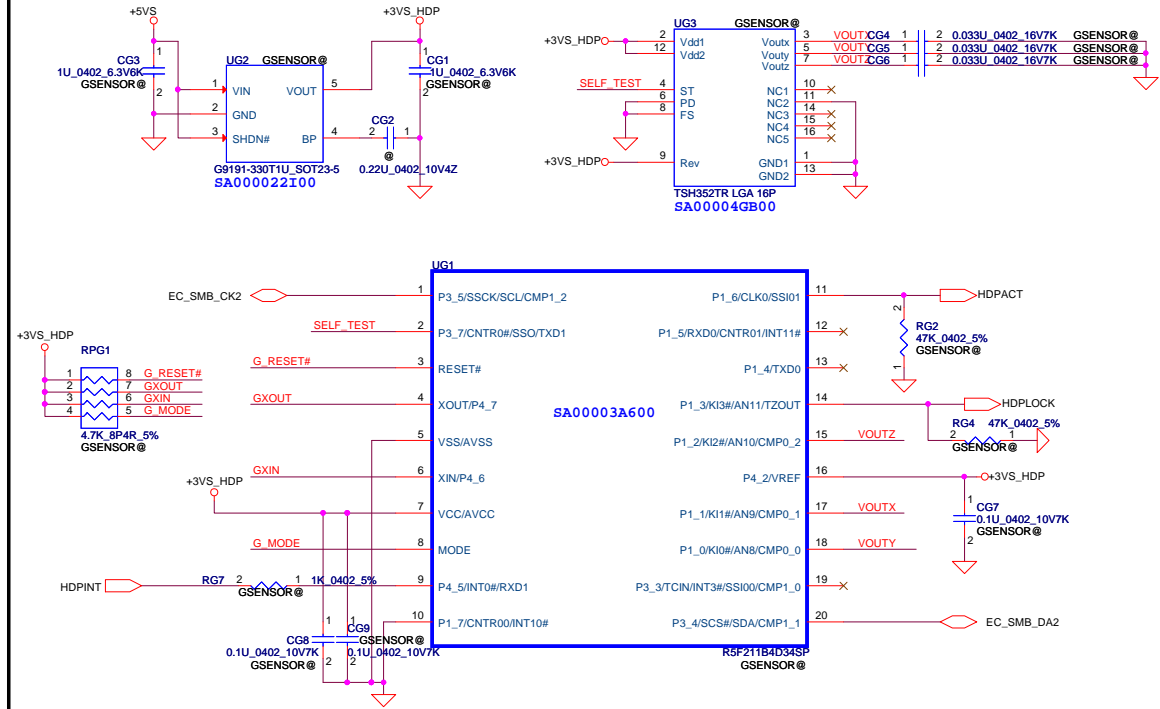
Keyboard LED



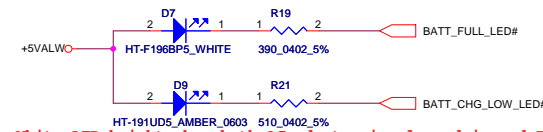
NEW KEYBOARD CONN.



G-SENSOR

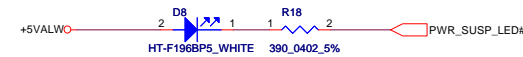


LED BATT CHARGE(Blink) /FULL LED



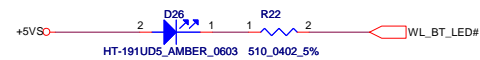
White LED bright when both AC-adaptor is plugged in and Battery is full charged
 Amber LED bright while charging battery from AC-adaptor.
 Amber LED blink during Critical Low Battery

POWER LED(Blink)

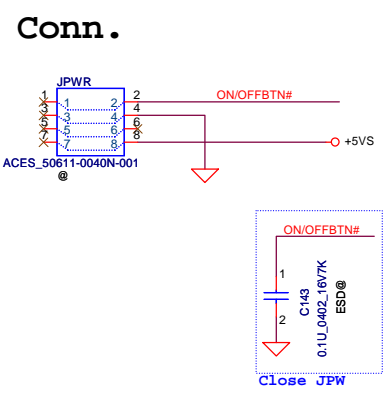
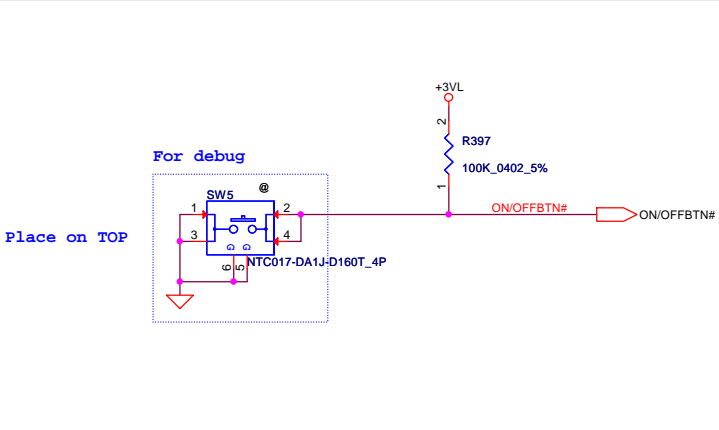


White LED bright when system is power on.
 White LED blink when system is sleep mode.

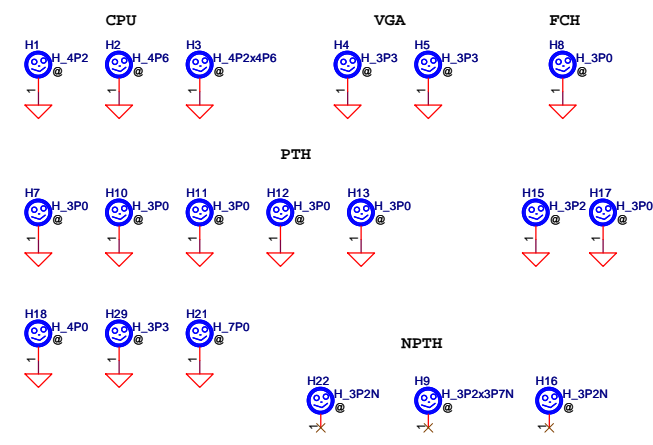
WLAN LED



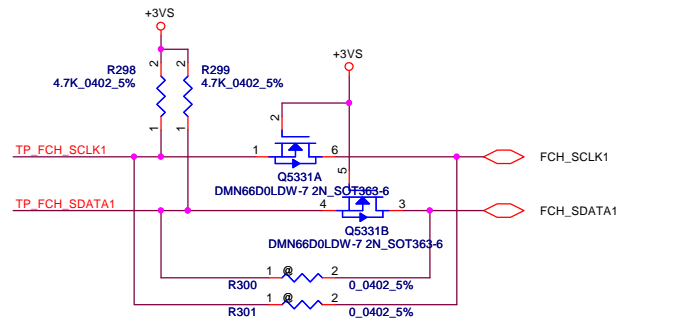
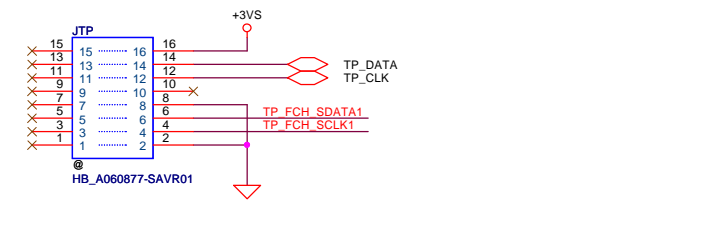
| | | | | |
|---|--------------------|-----------------|--------------------------|--|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2013/03/20 | Deciphered Date | 2014/03/20 | Title |
| | | | | Debug/KB |
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| | | | | Rev 1.0 |
| | | | | Date: Wednesday, March 20, 2013 Sheet 36 of 51 |



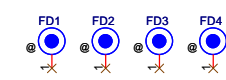
Screw Hole



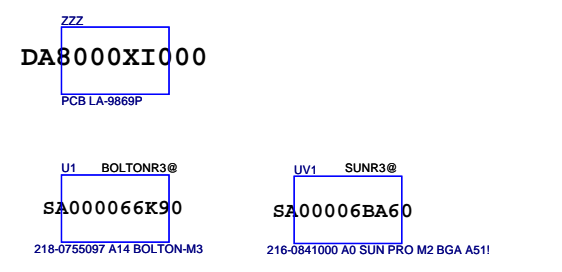
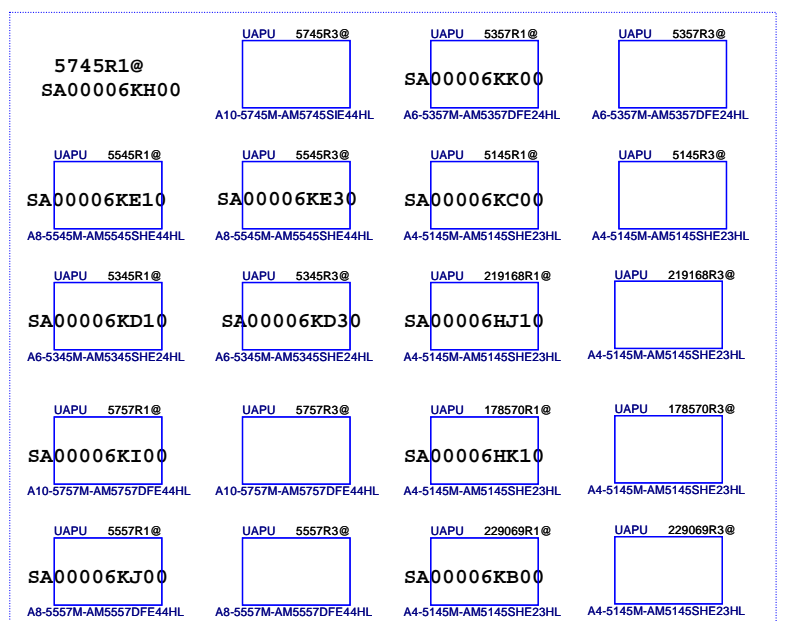
Touchpad Connector



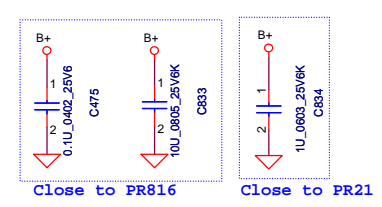
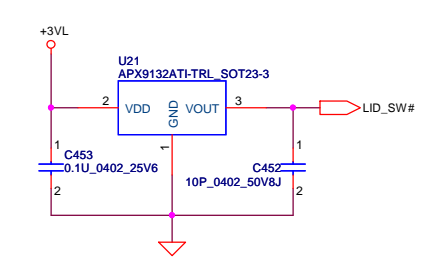
PCB Fedical Mark PAD



ISPD

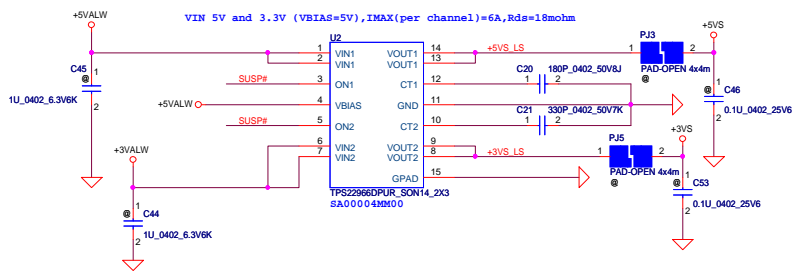


Lid SW

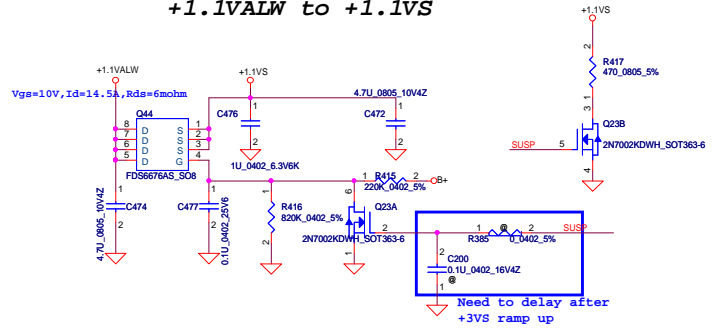


| | | | | | |
|---|---------------------------|--------------------|------------|------------------|-----------------|
| Security Classification | | Compal Secret Data | | Title | |
| Issued Date | 2013/03/20 | Deciphered Date | 2014/03/20 | TP/HDD LED/Screw | |
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| | | | | LA-9869P | |
| Date: | Wednesday, March 20, 2013 | Sheet | 37 | of | 51 |

+5VALW TO +5VS
+3VALW TO +3VS
Load switch

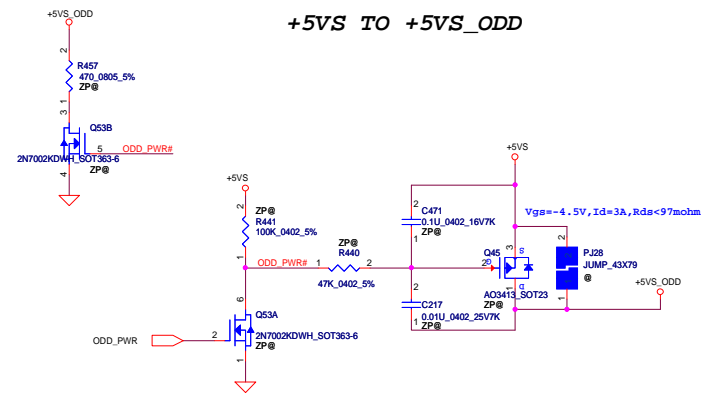


+1.1VALW to +1.1VS

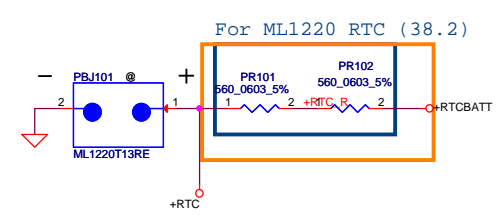
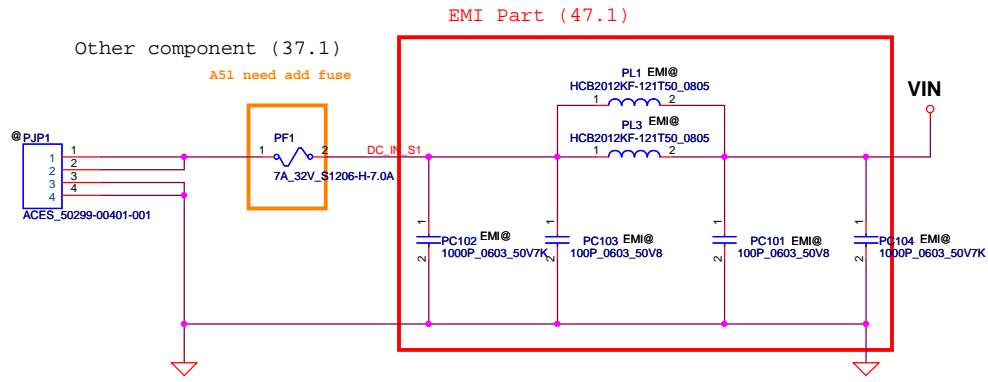


Need to delay after +3VS ramp up

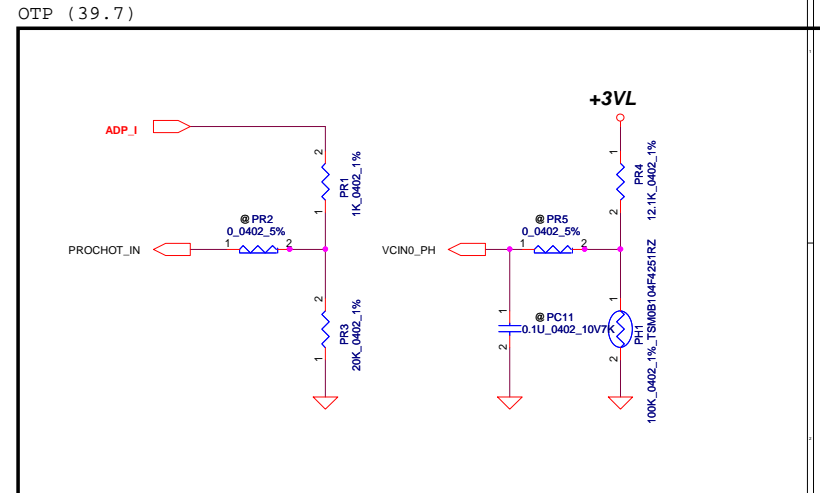
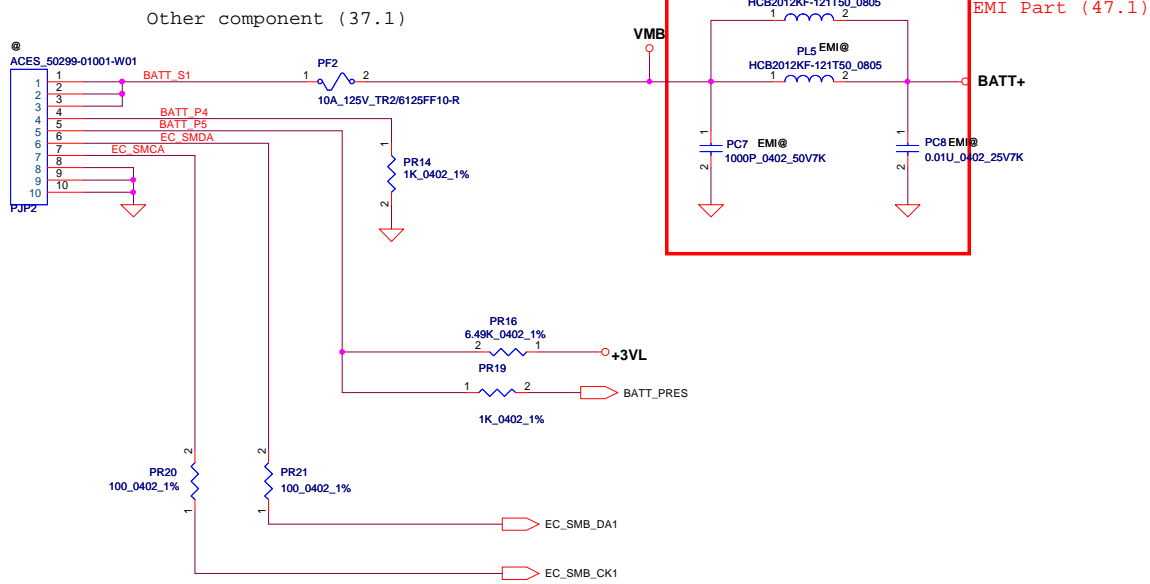
+5VS TO +5VS_ODD



| | | | |
|---|--------------------|-----------------|---|
| Security Classification | Compal Secret Data | | Title |
| Issued Date | 2013/03/20 | Deciphered Date | |
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| | | | Sheet 38 of 51 |



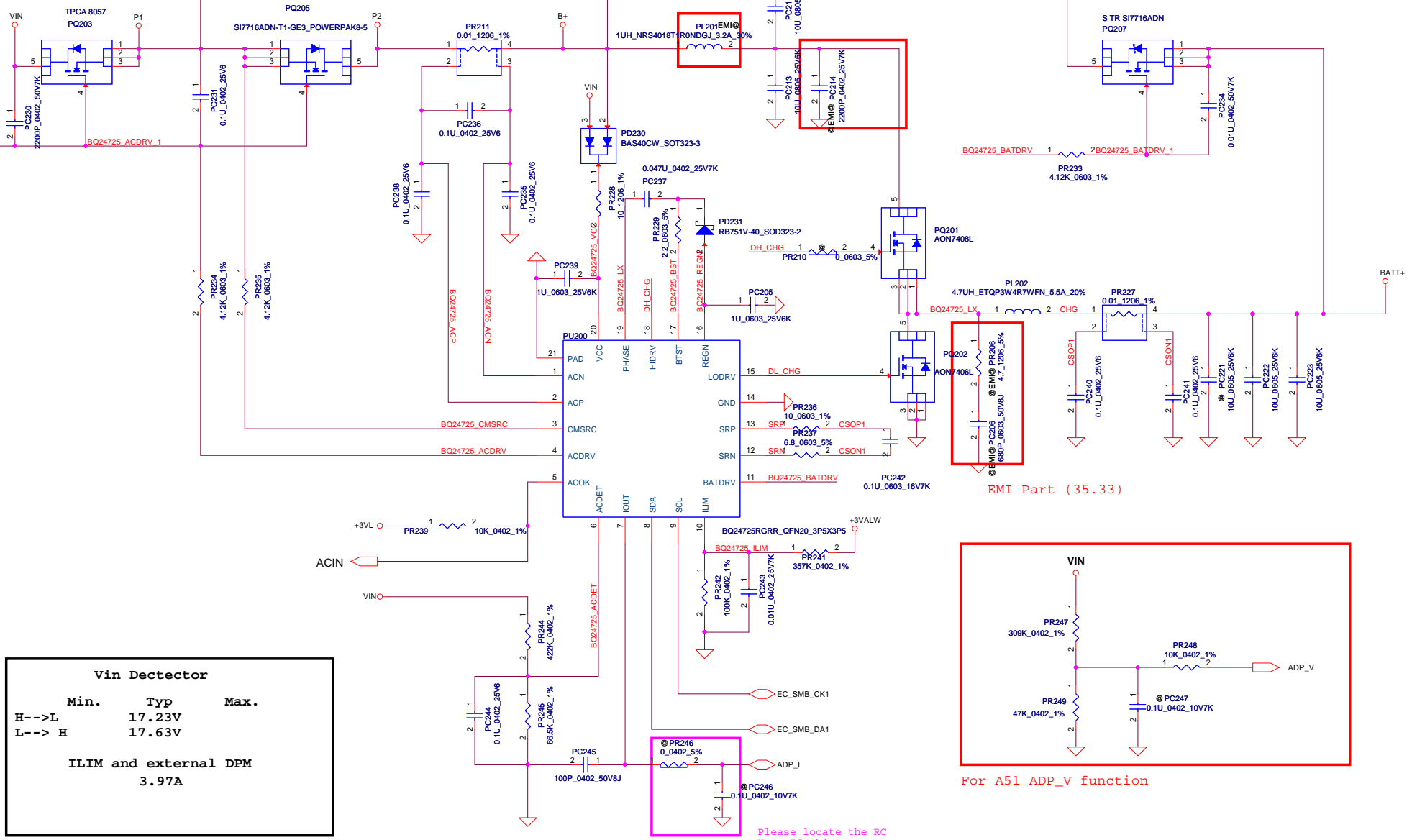
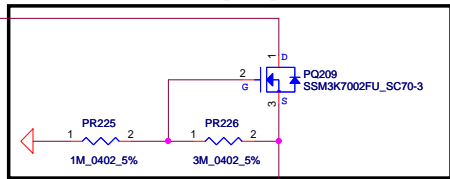
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| Date: | | | | Rev 1.0 |
| Sheet 39 of 51 | | | | |



| | | | | |
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| Date: | Sheet 40 of 51 | | | Rev 1.0 |

for reverse input protection

Charger controller (40.1), Support component (40.2)

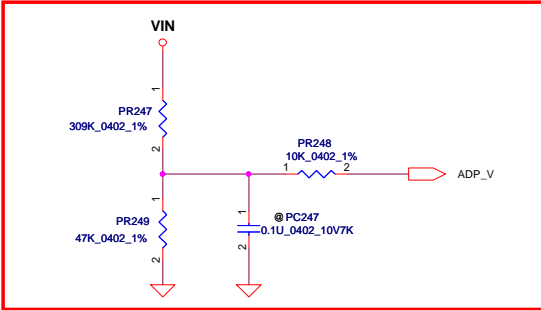


Vin Detector

| | Min. | Typ | Max. |
|-------|------|--------|------|
| H-->L | | 17.23V | |
| L-->H | | 17.63V | |

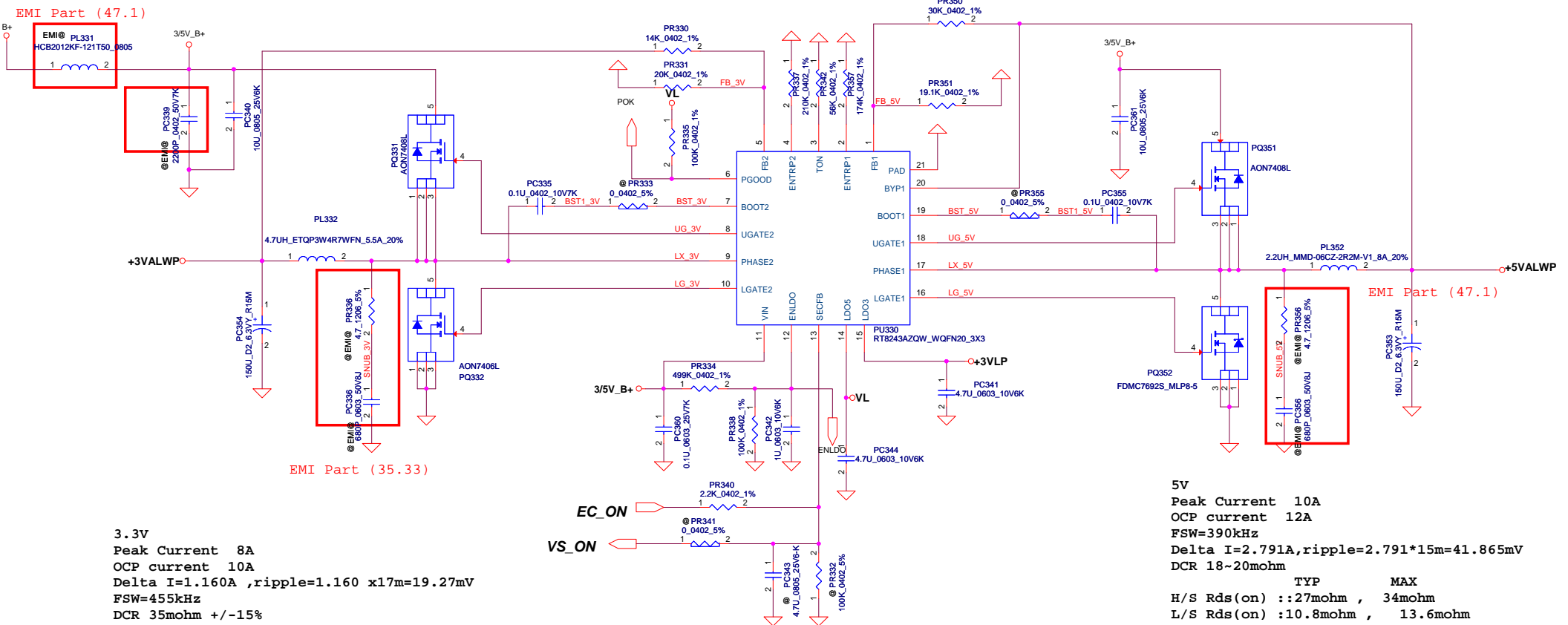
ILIM and external DPM
3.97A

Please locate the RC
Near EC chip
2011-02-22



For A51 ADP_V function

| | | | | |
|---|--------------------|-----------------|--------------------------|---|
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| Issued Date | 2013/03/20 | Deciphered Date | 2014/03/20 | Title |
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| Date: | | | | Sheet 41 of 51 |

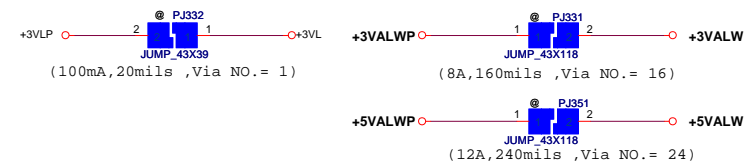


3.3V
 Peak Current 8A
 OCP current 10A
 Delta I=1.160A ,ripple=1.160 x17m=19.27mV
 FSW=455kHz
 DCR 35mohm +/-15%

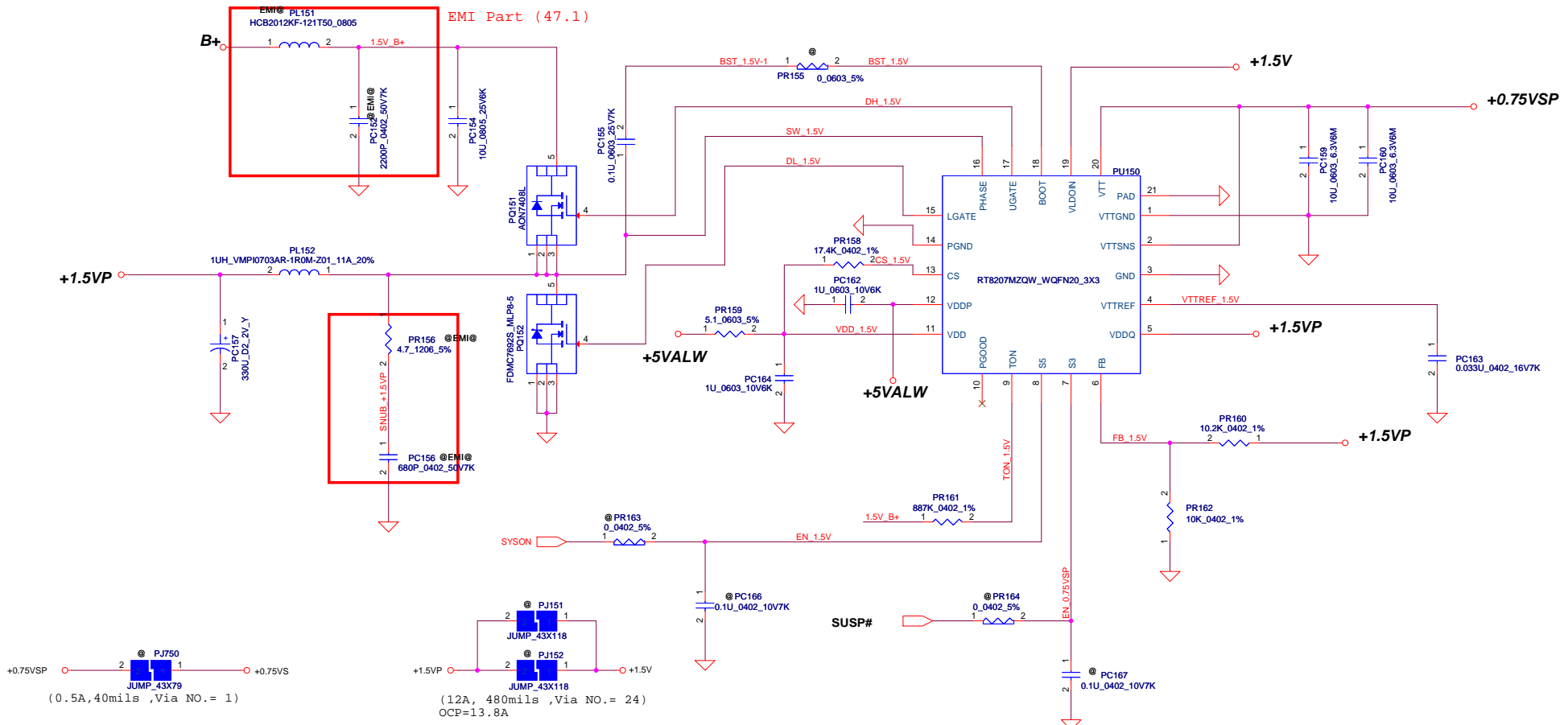
| | |
|-----------------------|----------|
| TYP | MAX |
| H/S Rds(on) :27mohm , | 34mohm |
| L/S Rds(on) :19mohm , | 23.5mohm |

5V
 Peak Current 10A
 OCP current 12A
 FSW=390kHz
 Delta I=2.791A,ripple=2.791*15m=41.865mV
 DCR 18~20mohm

| | |
|-------------------------|----------|
| TYP | MAX |
| H/S Rds(on) ::27mohm , | 34mohm |
| L/S Rds(on) :10.8mohm , | 13.6mohm |



| | | | | |
|---|--------------------|-----------------|--------------------------|-------------|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2013/03/20 | Deciphered Date | 2014/03/20 | Title |
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| Date: | | | Sheet 42 of 51 | Rev 1.0 |



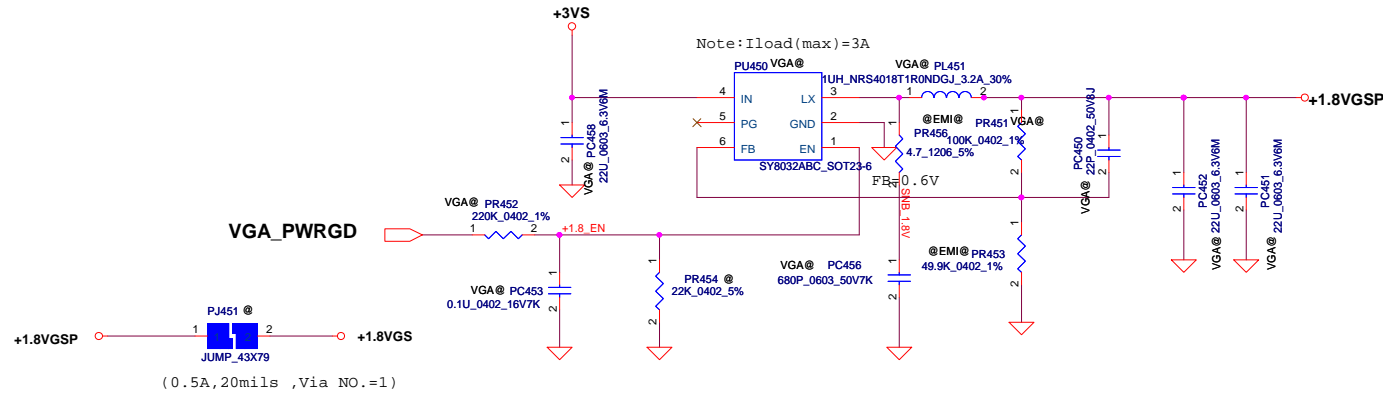
1.5V
 Peak Current 12A
 OCP current 13.34A
 FSW=300kHz
 DCR 8.3 ~ 10mohm
 TYP MAX
 H/S Rds(on) :27mohm , 34mohm
 L/S Rds(on) :10.8mohm , 13.6mohm

| STATE | S3 | S5 | 1.5VP | VTT_REFP | 0.75VSP |
|-------|----|----|--------------------|--------------------|--------------------|
| S0 | Hi | Hi | On | On | On |
| S3 | Lo | Hi | On | On | Off (Hi-Z) |
| S4/S5 | Lo | Lo | Off (Discharge) | Off (Discharge) | Off (Discharge) |

Note: S3 - sleep ; S5 - power off

| | | | | | |
|---|------------|--------------------|------------|--------------------------|-----------------|
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| Issued Date | 2013/03/20 | Deciphered Date | 2014/03/20 | Compal Electronics, Inc. | |
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| | | | | Custom | LA-9869P |
| Date: | | Sheet | 43 | of | 51 |

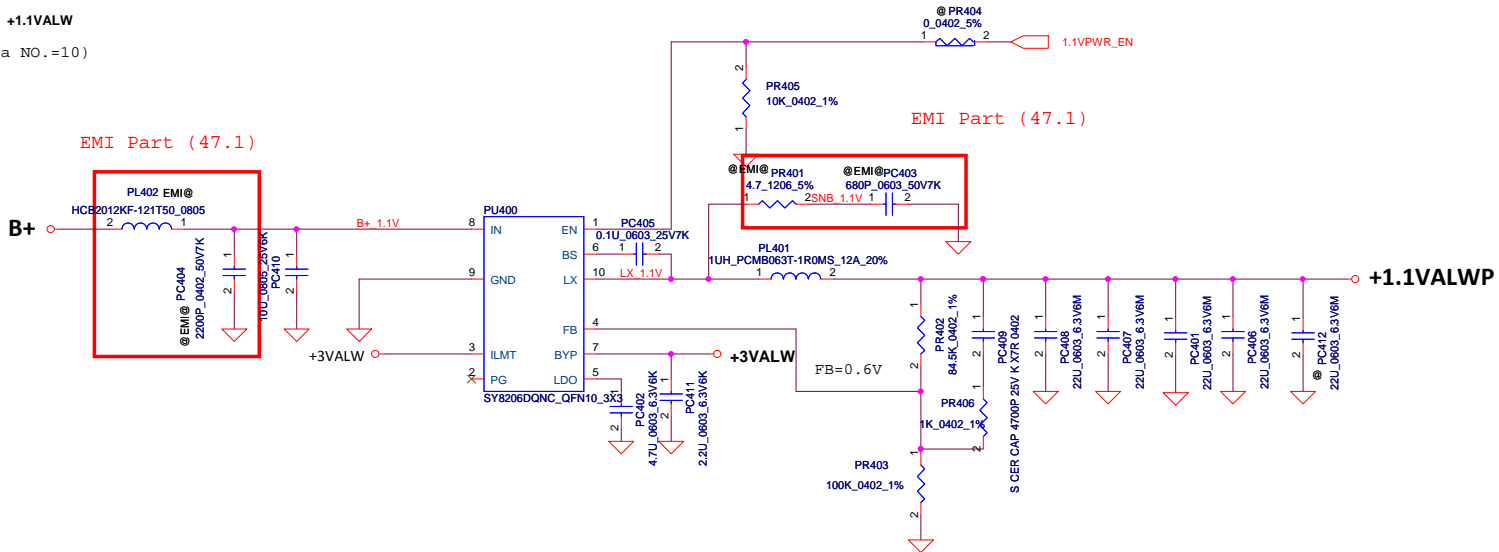
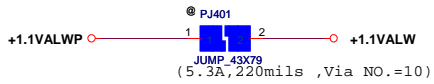
1.8V controller (35.15), Support component (35.16)



1.8V
 Peak Current 0.5A
 OCP current 3.5A
 FSW=800kHz

 H/S Rds(on) :100mohm ,
 L/S Rds(on) :80mohm ,

1.1V controller (35.27), Support component (35.28)



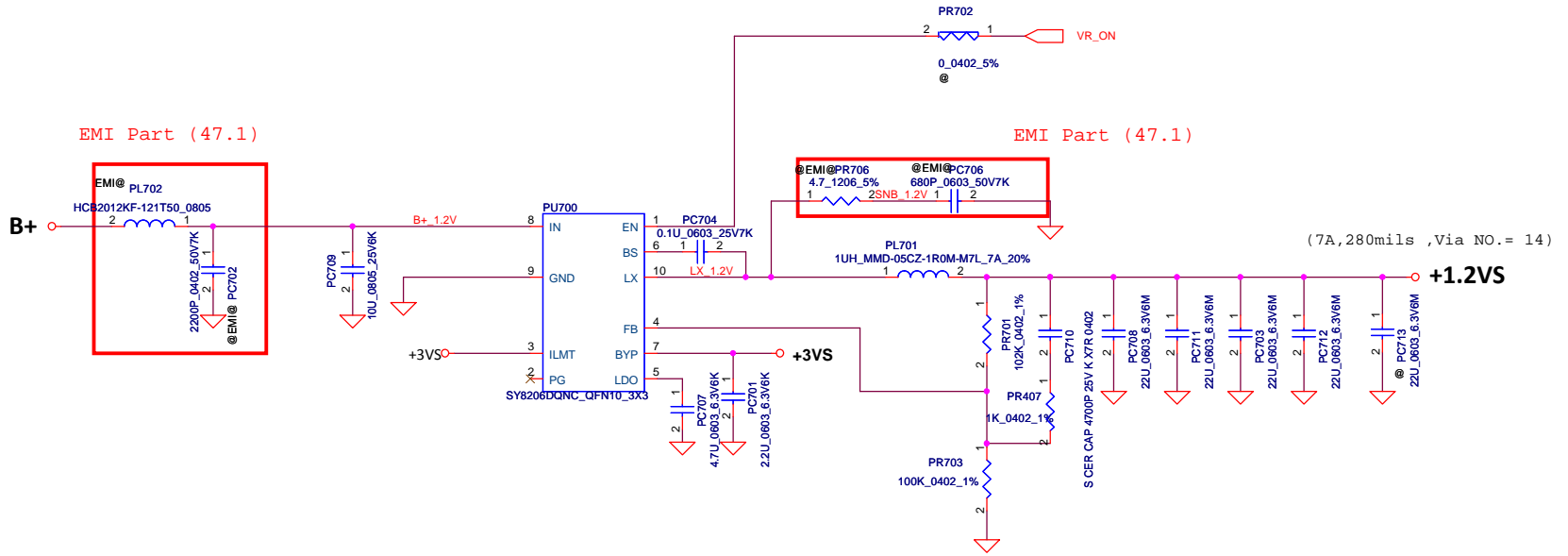
1.1V
 Peak Current 5.3A
 OCP current 12A
 FSW=800kHz

 H/S Rds(on) :22mohm ,
 L/S Rds(on) :11mohm ,

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high respectively.

| | | | | |
|---|--------------------|-----------------|--------------------------|--|
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| Issued Date | 2013/03/20 | Deciphered Date | 2014/03/20 | Title |
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| Size | Document Number | Rev | Sheet 44 of 51 | |
| Custom | LA-9869P | 1.0 | | |

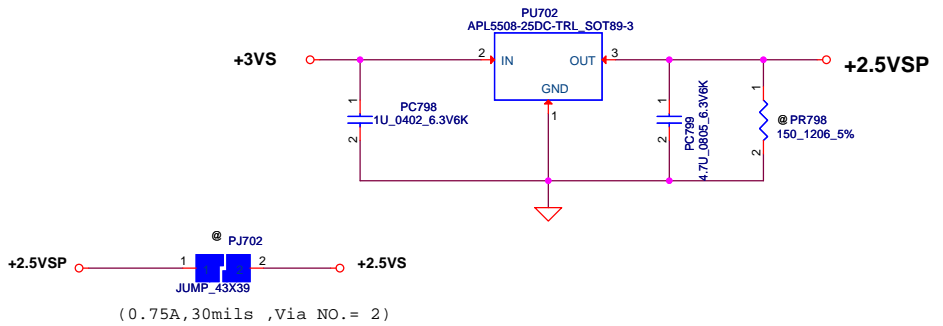
1.2V controller (35.7), Support component (35.8)



1.2V
 Peak Current 7A
 OCP current 12A
 FSW=800kHz

 H/S Rds(on) :22mohm ,
 L/S Rds(on) :11mohm ,

2.5V controller (35.13), Support component (35.14)

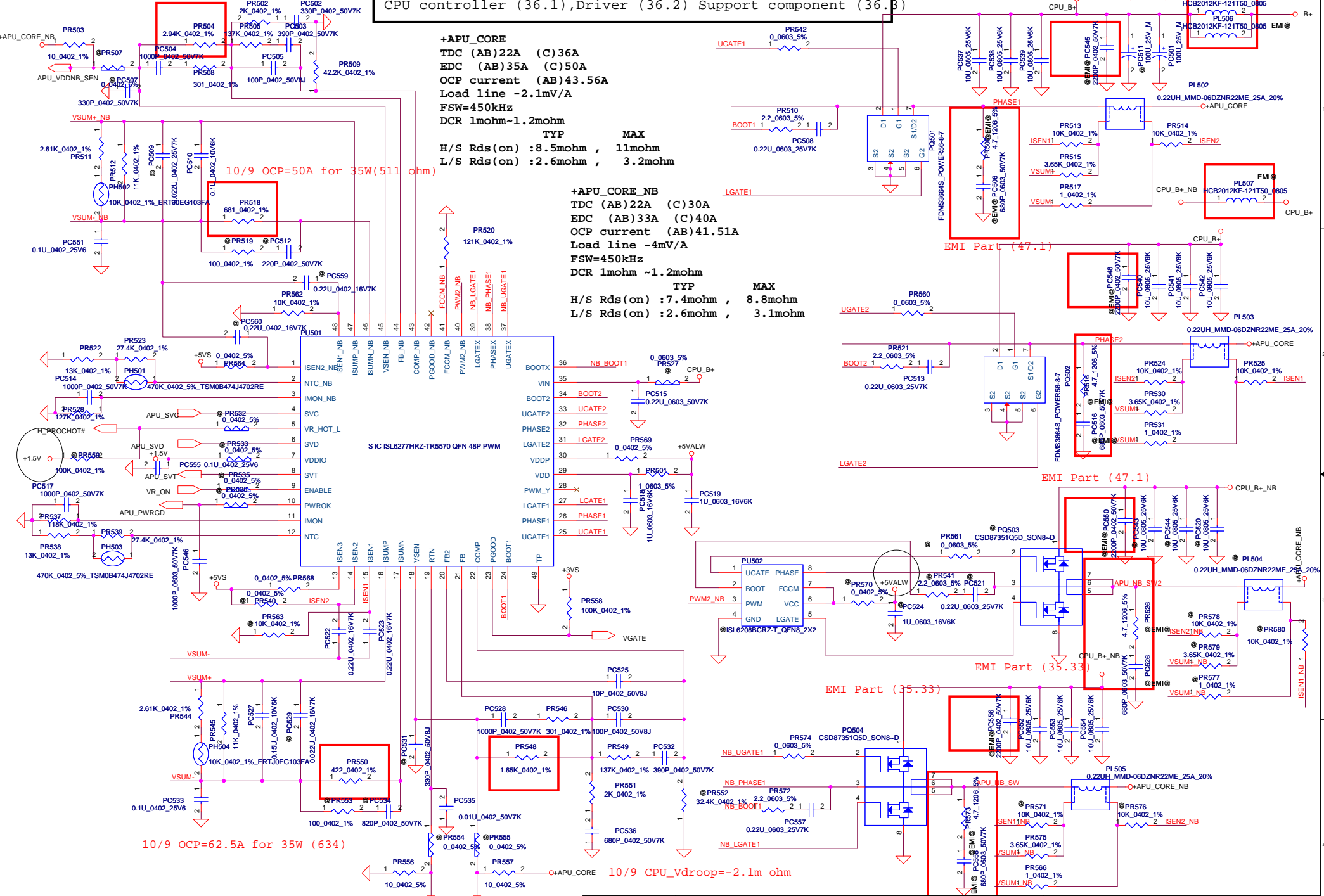


| | | | | |
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| Issued Date | 2013/03/20 | Deciphered Date | 2014/03/20 | Title |
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CPU controller (36.1), Driver (36.2) Support component (36.3)

+APU_CORE
 TDC (AB)22A (C)36A
 EDC (AB)35A (C)50A
 OCP current (AB)43.56A
 Load line -2.1mV/A
 FSW=450kHz
 DCR 1mohm~1.2mohm
 TYP MAX
 H/S Rds(on) :8.5mohm , 11mohm
 L/S Rds(on) :2.6mohm , 3.2mohm

+APU_CORE_NB
 TDC (AB)22A (C)30A
 EDC (AB)33A (C)40A
 OCP current (AB)41.51A
 Load line -4mV/A
 FSW=450kHz
 DCR 1mohm ~1.2mohm
 TYP MAX
 H/S Rds(on) :7.4mohm , 8.8mohm
 L/S Rds(on) :2.6mohm , 3.1mohm



10/9 OCP=62.5A for 35W (634)

10/9 CPU_Vdroop=-2.1m ohm

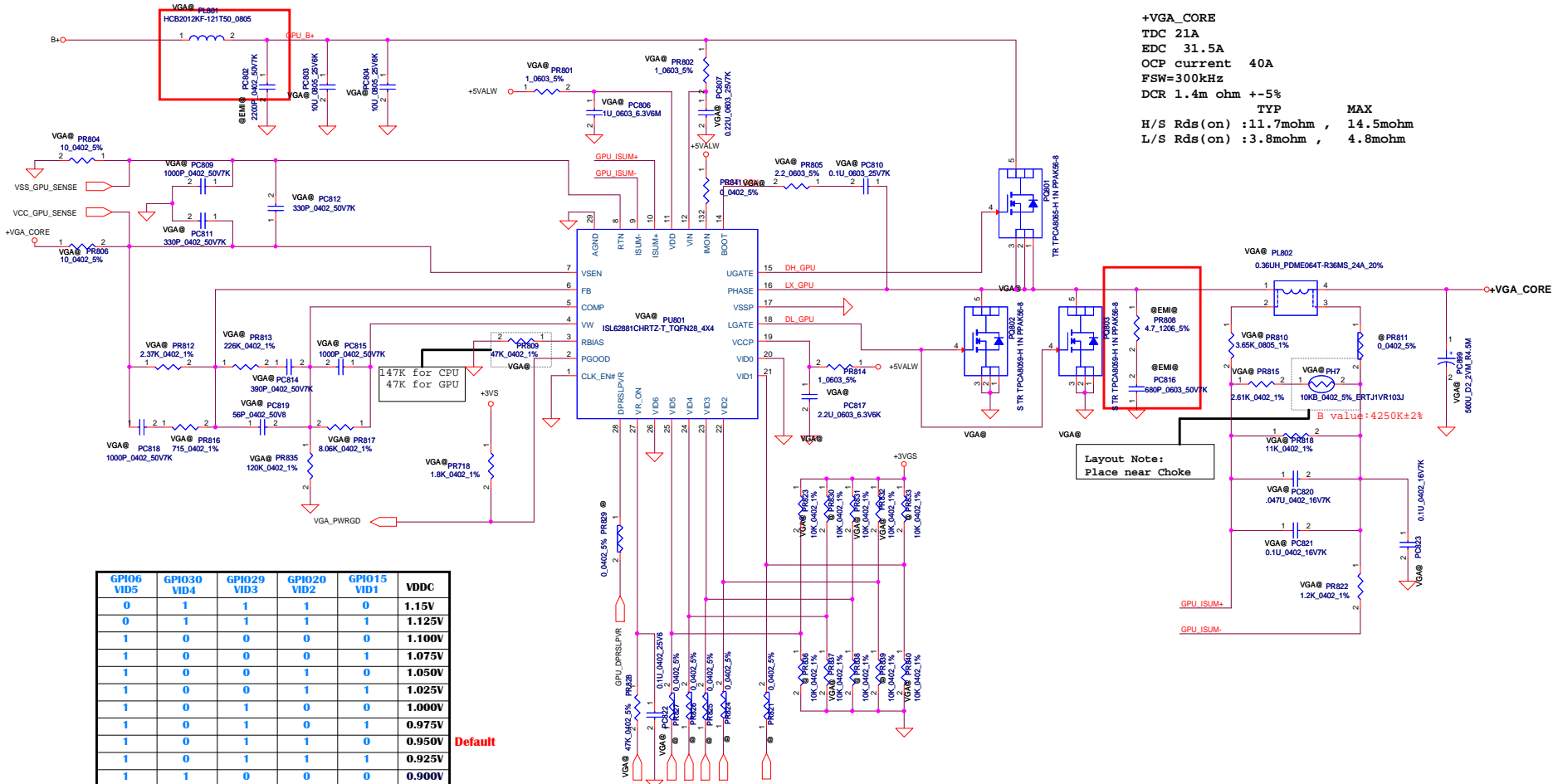
| Security Classification | Compal Secret Data | |
|---|--------------------|-----------------|
| Issued Date | 2013/03/20 | Deciphered Date |
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| Compal Electronics, Inc. | | |
|--------------------------|---------------------------|----------------|
| +CPU CORE/VDDNB | | |
| Title | Document Number | Rev |
| | LA-9869P | 1.0 |
| Date | Wednesday, March 20, 2013 | Sheet 46 of 51 |

VGA controller (43.1), Driver (43.2) Support component (43.3)

EMI Part (47.1)

+VGA_CORE
 TDC 21A
 EDC 31.5A
 OCP current 40A
 FSW=300kHz
 DCR 1.4m ohm +-5%
 TYP MAX
 H/S Rds(on) :11.7mohm , 14.5mohm
 L/S Rds(on) :3.8mohm , 4.8mohm

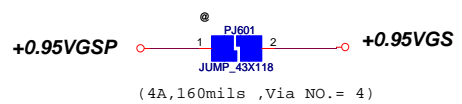
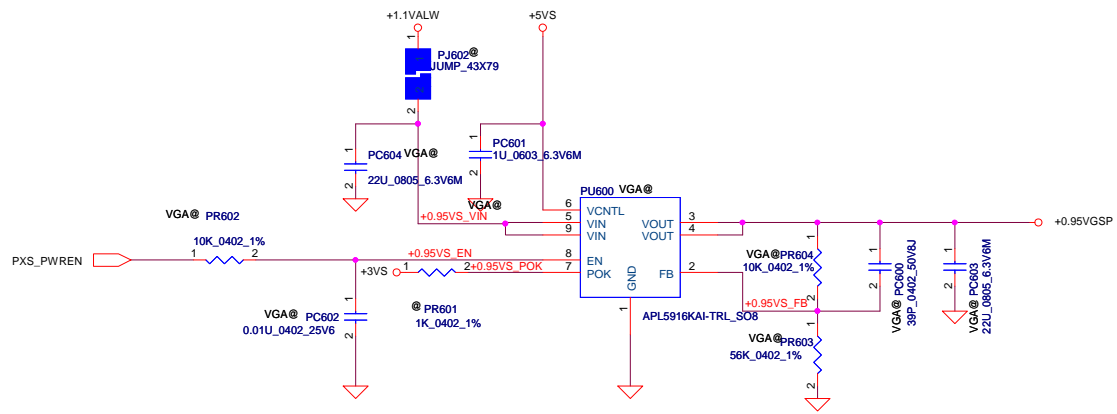


Layout Note:
Place near Choke

| GPI06 VID5 | GPI030 VID4 | GPI029 VID3 | GPI020 VID2 | GPI015 VID1 | VDDC |
|------------|-------------|-------------|-------------|-------------|--------|
| 0 | 1 | 1 | 1 | 0 | 1.15V |
| 0 | 1 | 1 | 1 | 1 | 1.125V |
| 1 | 0 | 0 | 0 | 0 | 1.100V |
| 1 | 0 | 0 | 0 | 1 | 1.075V |
| 1 | 0 | 0 | 1 | 0 | 1.050V |
| 1 | 0 | 0 | 1 | 1 | 1.025V |
| 1 | 0 | 1 | 0 | 0 | 1.000V |
| 1 | 0 | 1 | 0 | 1 | 0.975V |
| 1 | 0 | 1 | 1 | 0 | 0.950V |
| 1 | 0 | 1 | 1 | 1 | 0.925V |
| 1 | 1 | 0 | 0 | 0 | 0.900V |
| 1 | 1 | 0 | 0 | 1 | 0.875V |
| 1 | 1 | 0 | 1 | 0 | 0.850V |
| 1 | 1 | 1 | 0 | 1 | 0.825V |
| 1 | 1 | 1 | 0 | 0 | 0.800V |
| 1 | 1 | 1 | 0 | 1 | 0.775V |

Default

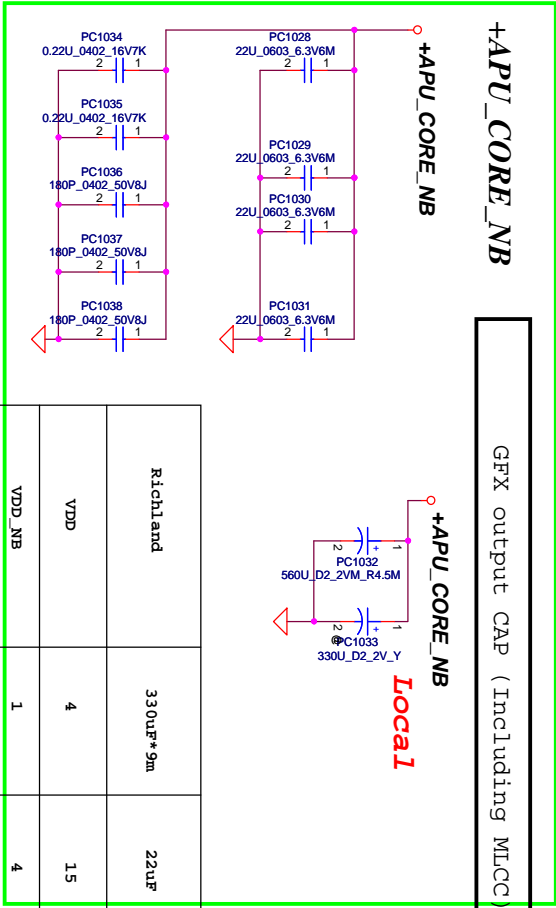
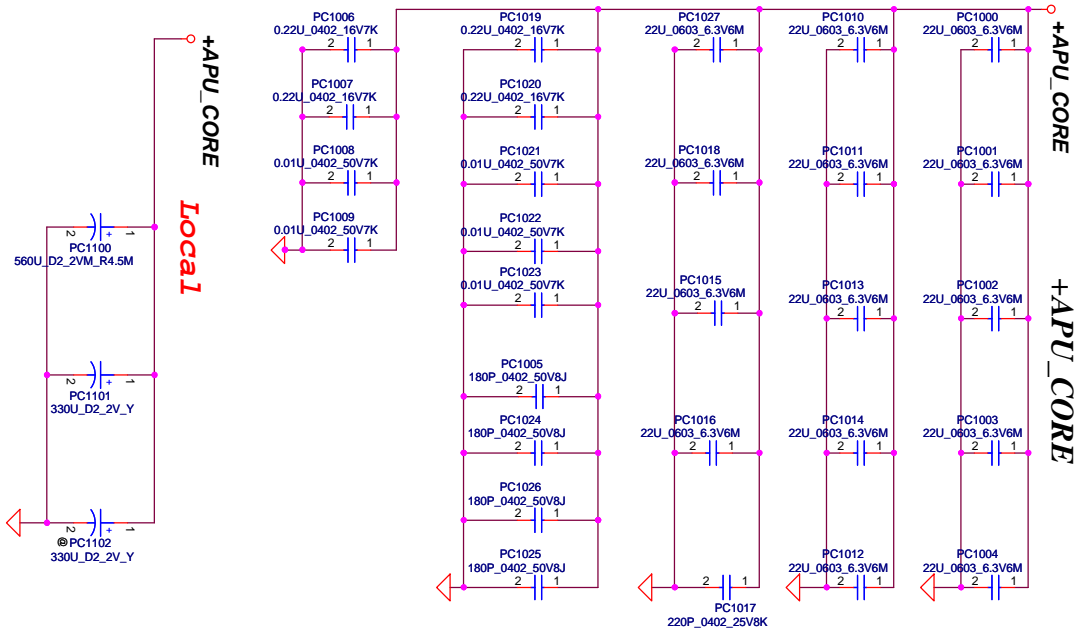
0.95V controller (35.11), Support component (35.12)



0.95V
 Peak Current 4A
 OCP current 16A
 FSW=800kHz

H/S Rds(on) : 22mohm ,
 L/S Rds(on) : 11mohm ,

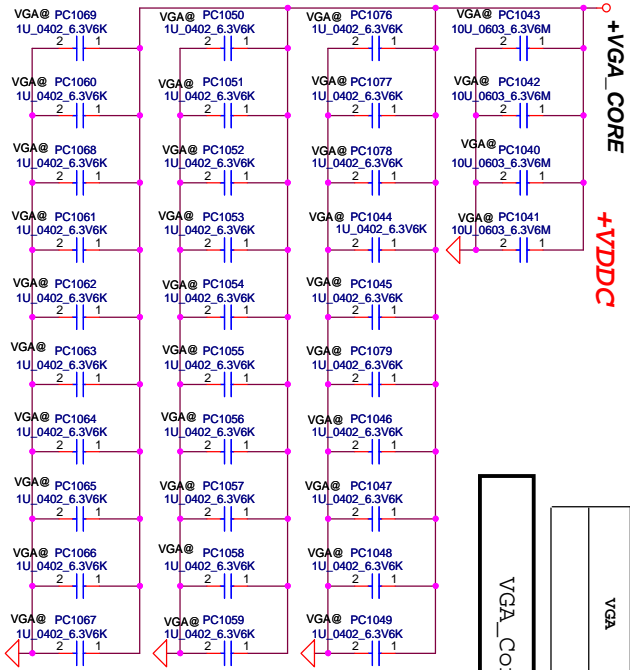
| | | | | | |
|---|------------|--------------------|------------|--------------------------|-----------------|
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| | | | | Size | Document Number |
| Date: Wednesday, March 20, 2013 | | | | Sheet | 48 of 51 |



| | | | | | |
|----------|----------|------|-------|--------|------|
| Richland | 330uF*9m | 22uF | 0.01u | 0.22uF | 180P |
| VDD | 4 | 15 | 5 | 4 | 4 |
| VDD_NB | 1 | 4 | 2 | 3 | |

| | | | |
|-----|---------|---------|--------|
| VGA | 560u x1 | 10u x 4 | 1u x30 |
|-----|---------|---------|--------|

VGA_Core output CAP (Including MLCC 43.9)



| | | | | |
|--|---------------------------|--------------------------|----------------------|-------|
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| Issued Date | 2013/03/20 | Deciphered Date | Compal Secret Data | |
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| The | | Compal Electronics, Inc. | | |
| Size | Document Number | 1A-9869P | PROCESSOR DECOUPLING | |
| Date | Wednesday, March 20, 2013 | Sheet | 49 | of 51 |
| Rev | 1.0 | | | |

Item Reason for change PG# Modify List Date Phase

| Item | Time (When) | Page (Where) | Location / Discription (How / What) | Request (Who) |
|------|----------------|----------------------------|---|---------------|
| 1 | EVT-2012/11/28 | P39-PWR-BATTERY CONN / OTP | change PF2 vendor for cost down plane | PWR |
| 2 | EVT-2012/11/28 | P41-PWR+3VALW/5VALW | change PR337 235K to 210K & PR5357 156k to 174k | PWR |
| 3 | EVT-2012/11/28 | P41-PWR+3VALW/5VALW | Delate PC351 add PC353 150u D2 cap | PWR |
| 4 | EVT-2012/11/28 | P43-PWR_+1.8VSGP/+1.1VALWP | change PC157 220u H=4.5mm to 330u D2 cap H=2mm | PWR |
| 5 | EVT-2012/11/28 | P43-PWR_+1.8VSGP/+1.1VALWP | change PR158 16.2K to 17.4K | PWR |
| 6 | EVT-2012/11/28 | P50-PWR-CPU_CORE | change the PC1101 560u to 330u | PWR |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

HW PIR (Product Improve Record)

VDKTE LA-9869P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.2

GERBER-OUT DATE: 2012/12/25

| Item | Page | Date | Request | Solution |
|------|------|-------------|----------------------------|---|
| 1) | 21 | 2012/12/04a | For CRT undershoot issue | Add R66 & R67 for CRT issue. |
| 2) | 14 | 2012/12/04a | For VGA_CORE display | unomunt CR103. |
| 3) | 22 | 2012/12/13a | For EMI request | Change L8/L9/L10/L11 part number for EMI request. |
| 4) | 34 | 2012/12/13a | For change EC PIN | Change 1.1VFWR_EN from pin 71 to pin 127 and USB_EN#0 from pin84 to pin 23. |
| 5) | 19 | 2012/12/14a | For LVDS translator | Delete all of RTD2132S components. |
| 6) | 31 | 2012/12/14a | For S&C port wake | Add CHG_PWR_GATE# on U15 pin 1 and connect to EC pin82. |
| 7) | 24 | 2012/12/17a | For leakage with PXS_PWREN | Change Power rail from +3VALW_FCH to +3VALW on R216 pin1 |
| 8) | 07 | 2012/12/22a | For leakage | Delete R47, D18. |
| 9) | 24 | 2012/12/22a | For NV suggestion | Add R283 & Q30. |
| 10) | 34 | 2012/12/25a | For S&C port wake | Add RB25. |

VDKTE LA-9869P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.3

GERBER-OUT DATE: 2013/02/04

| Item | Page | Date | Request | Solution |
|------|------|-------------|-----------------------|---|
| 1) | 24 | 2013/01/21a | For AMD suggestion | Update R288/R289 from 10K to 2.2K. |
| 2) | 22 | 2013/01/21a | For HDMILEAKAGE issue | Change R571 to +3VS power rail. |
| 3) | 34 | 2013/01/21a | For Audio noise | Add EC_MUTE_INT (GPIO5D) and add RB38(0 ohm) and RB37 (4.7K PD) |
| 4) | 20 | 2013/01/21a | For layout routing | SWAP L56. |
| 5) | 20 | 2013/01/21a | For EMI request | Add R155/156. |
| 6) | 13 | 2013/01/28a | For Safety | Add GPU_DOWN# connect to EC. |
| 7) | 25 | 2013/01/29a | For EMI request | Add C508(10P)/R118(0 ohm) with FCH_SPI_CLK_R. |
| 8) | 33 | 2013/01/30a | For ESD request | Reserve D27-D30 on SPK. |
| 9) | 07 | 2013/01/30a | For ESD request | Reserve D31 on APU_PROCHOT#. |
| 10) | 20 | 2013/01/30a | For ESD request | Add D32 on Int mic clk/data and USB. |
| 11) | 34 | 2013/01/30a | For ESD request | Reserve DB2 on H_PROCHOT_EC. |
| 12) | 36 | 2013/01/31a | For move JTP | SWAP JTP |
| 13) | 24 | 2013/02/01a | For ESD request | Add 1000p C505 on FCH_PWRGD. |
| 14) | 34 | 2013/02/01a | For ESD request | Add 1000p CB17 on FCH_PWRGD. |
| 15) | 34 | 2013/02/04a | For PWR | Add GPIO pin 99 of EC for power. |