VFKAA

Rosetta 10FG

LA-9863P REV 1.0 Schematics

Intel Processor(Ivy Bridge / Sandy Bridge)
PCH(Panther Point)

2013-01-14 Rev 1.0

Security Classification	Compal Secret Data		
Issued Date	2012/12/07	Deciphered Date	2013/12/07

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Title: *Cover Page*

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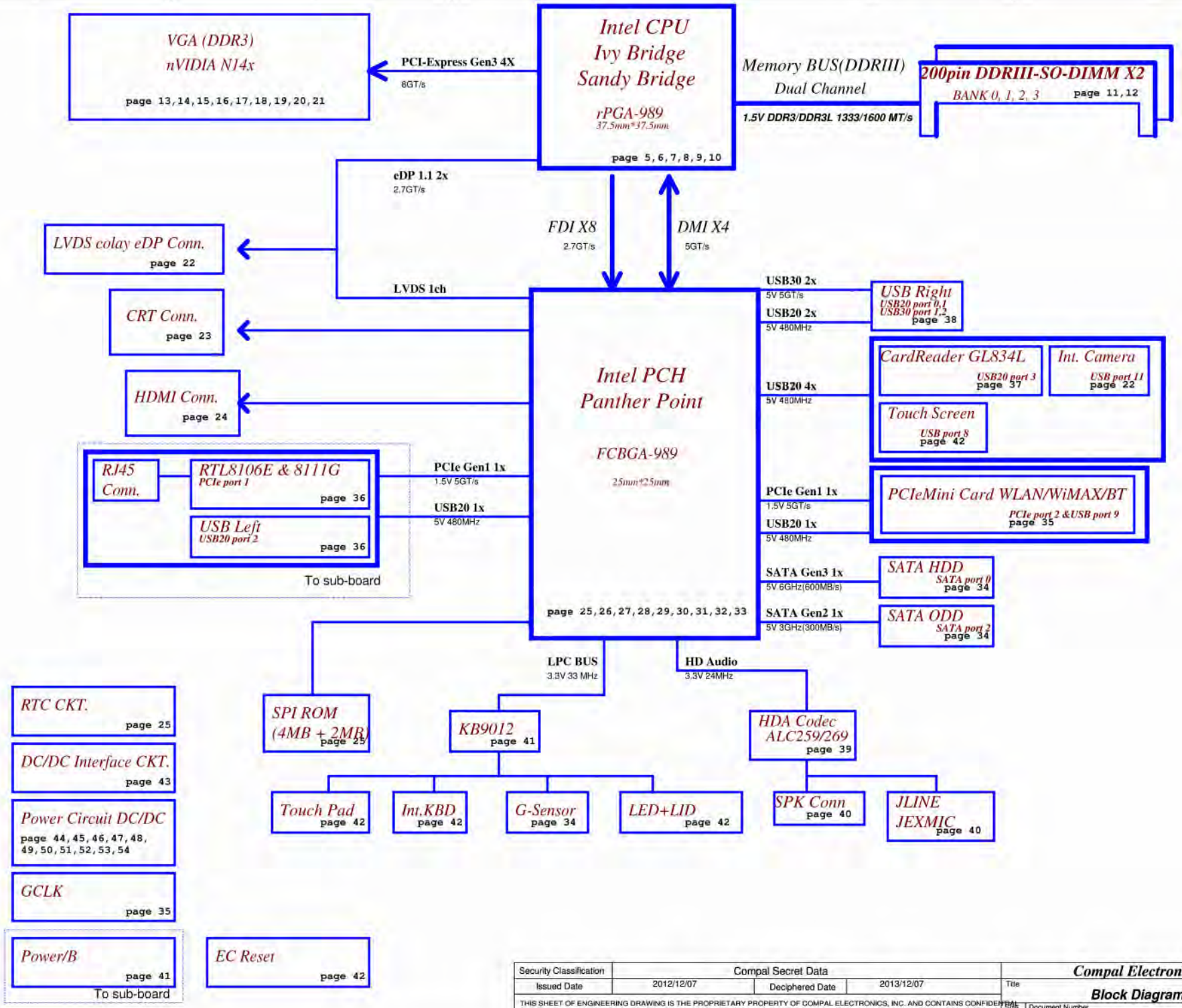

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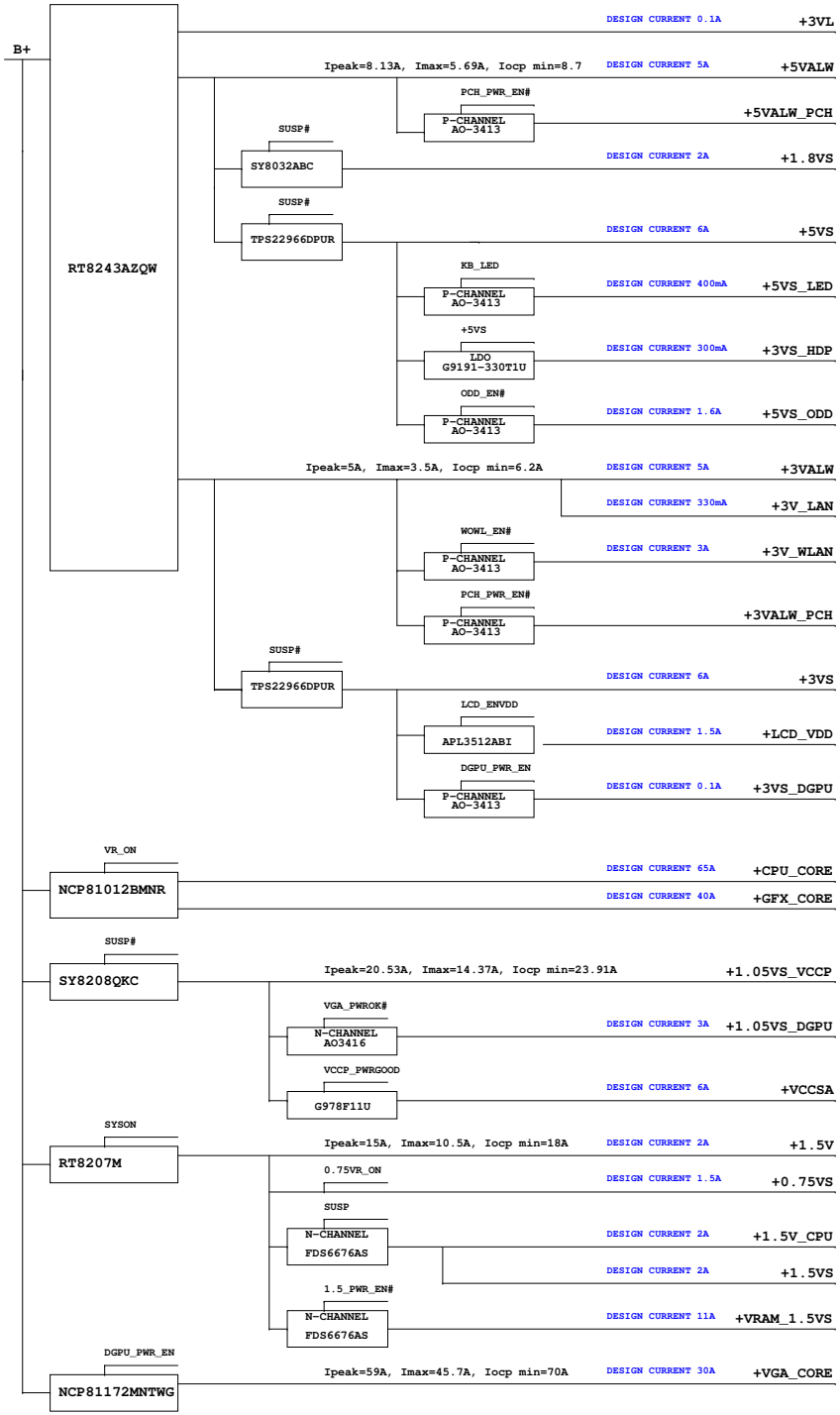

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

BTO Option Table

Function	SKU	PCH		GPU		VRAM	EC		ISPD
description	Optimus	Panther Point		N14M-GL	N14P-GV2	Dual Rank	EC		HDMI Logo
explain	Optimus	HM76	HM70	N14M-GL	N14P-GV2	Dual Rank	KB9012	NPCE885N	HDMI Logo
BTO	OPT@	HM76R1@ HM76R3@	HM70R1@ HM70R3@	N14MGL@ N14MGLR1@ N14MGLR3@	N14PGV2@ N14PGV2R1@ N14PGV2R3@	DRANK@	9012@	885@	HDMI45@

Function	LVDS-eDP		Camera & Mic	USB S&C		CRT			Touch Screen
description	LVDS-eDP		Camera & Mic	14640	14641	CRT			Touch Screen
explain	LVDS	eDP	Camera & Mic	14640	14641	w/ CRT		w/o CRT	Touch Screen
BTO	LVDS@	IEDP@	CAM_EMI@	14640@	14641@	CRT@	CRT_EMI@	NOCRT@	TOUCH_EMI@

Function	WOWL		G-SENSOR	ZPODD		GCLK		VRAM SKU for GV2	
description	WOWL		G-SENSOR	ZPODD		GCLK	non-GCLK	Single Rank	Dual Rank
explain	w/	w/o	G-SENSOR	w/	w/o	GCLK	non-GCLK	Single Rank	Dual Rank
BTO	WOWL@	NOWOWL@	GSENSOR@	ZPODD@	NONZP@	GCLK@	NOGCLK@	GVSR@	GVDR@

Function	Sleep & Music		KB Light	EMI/ESD part	
description	Sleep & Music		KB Light	EMI/ESD part	
explain	w/ S&M	w/o S&M	KB Light	EMI/ESD part	
BTO	269@	259@	KBL@	EMI@	ESD@

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	WLAN/WIMAX		
+3VS	Touch Pad	2C H	0010 1100 b

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	Smart Charger	12 H	0001 0010 b
+3VL	USB S&C 14640	35 H	0011 0101 b

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9E H	1001 1010 b
+3VS	G-Sensor	40 H	0100 0000 b

STATE / SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

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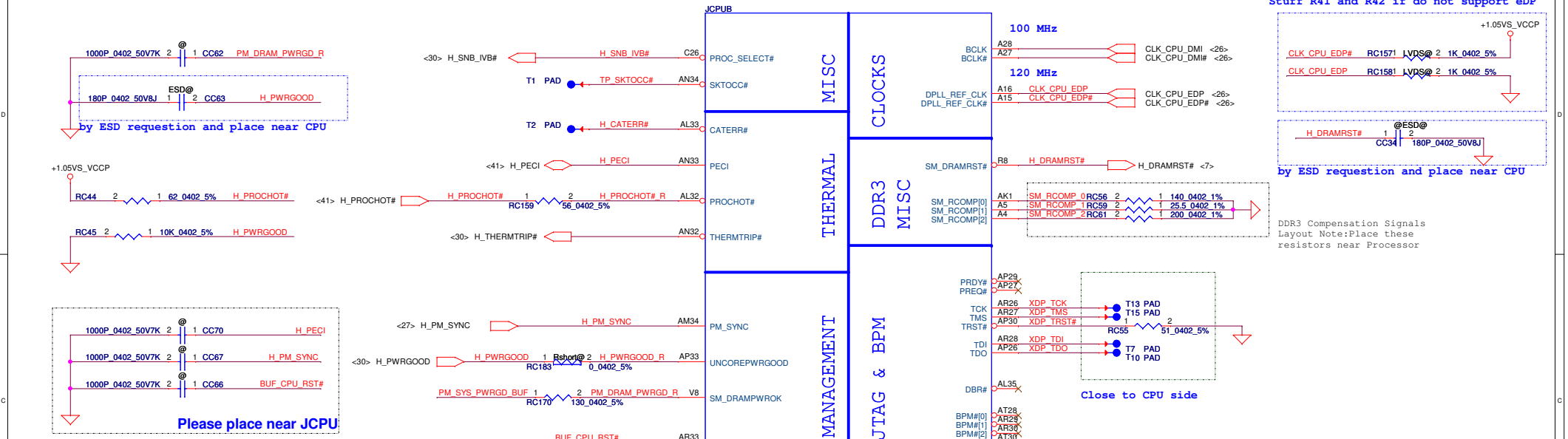
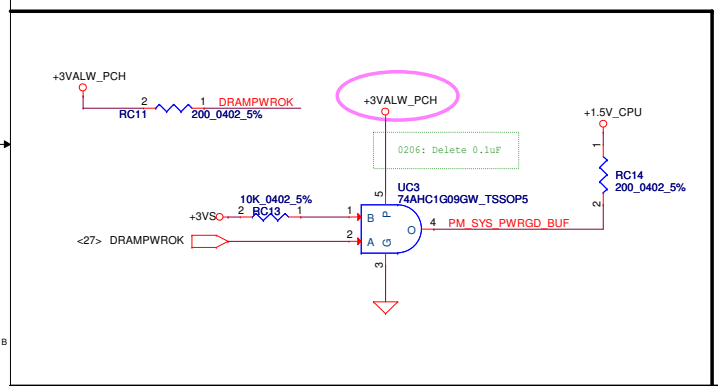
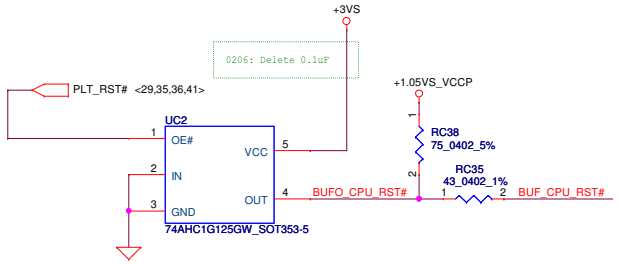
			Date: Monday, March 11, 2013; Sheet 4 of 56

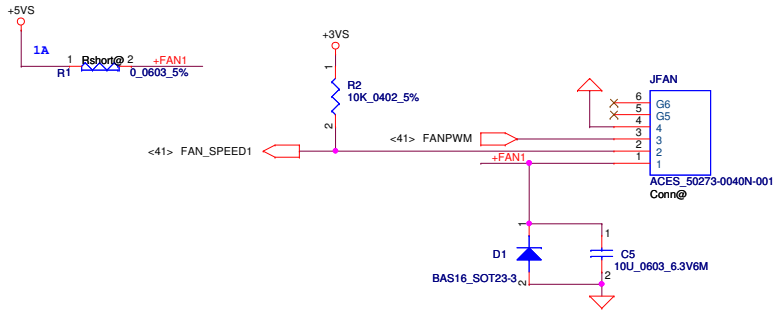




Buffered Reset to CPU



FAN Control Circuit



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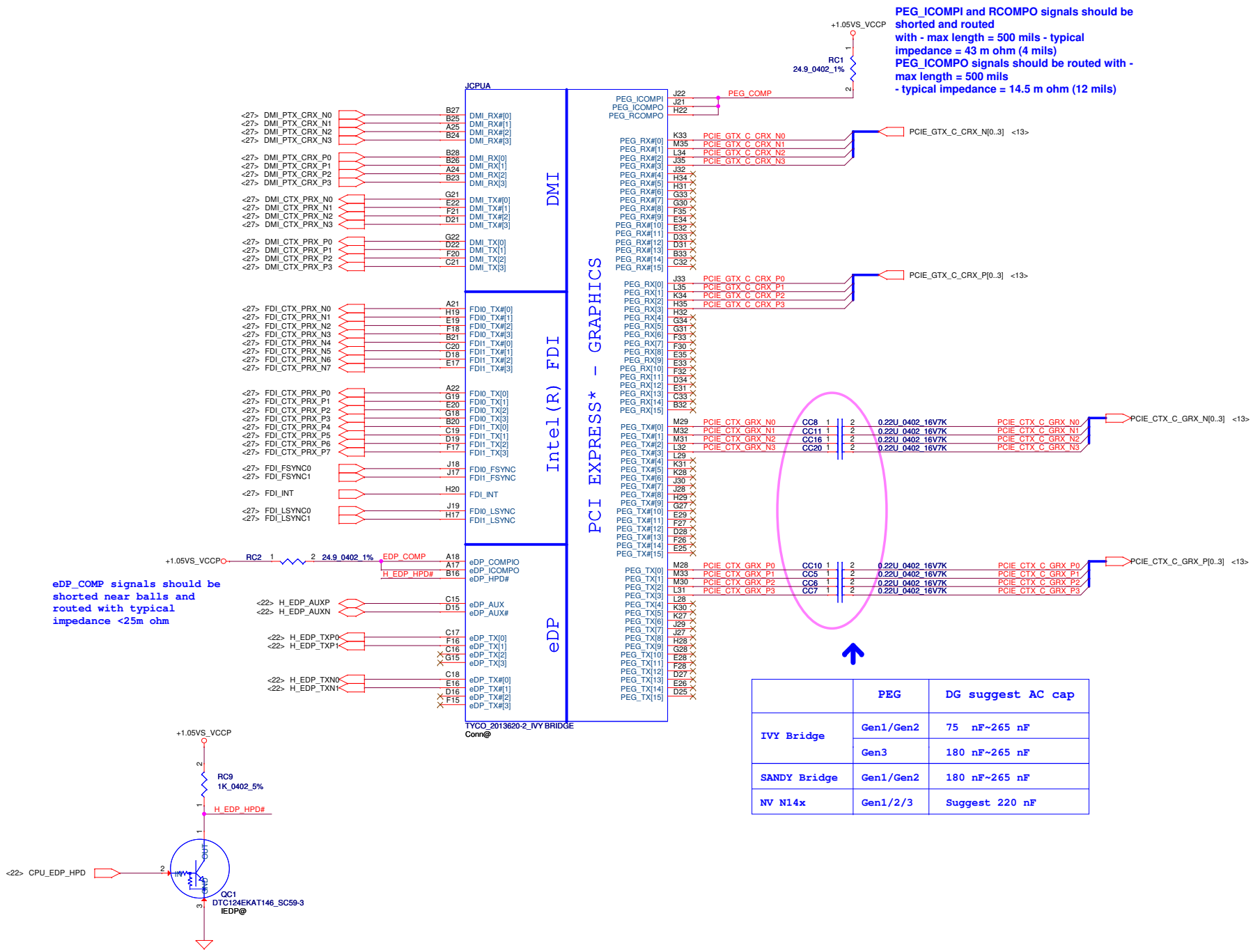

	PEG	DG suggest AC cap
IVY Bridge	Gen1/Gen2	75 nF~265 nF
	Gen3	180 nF~265 nF
SANDY Bridge	Gen1/Gen2	180 nF~265 nF
NV N14x	Gen1/2/3	Suggest 220 nF

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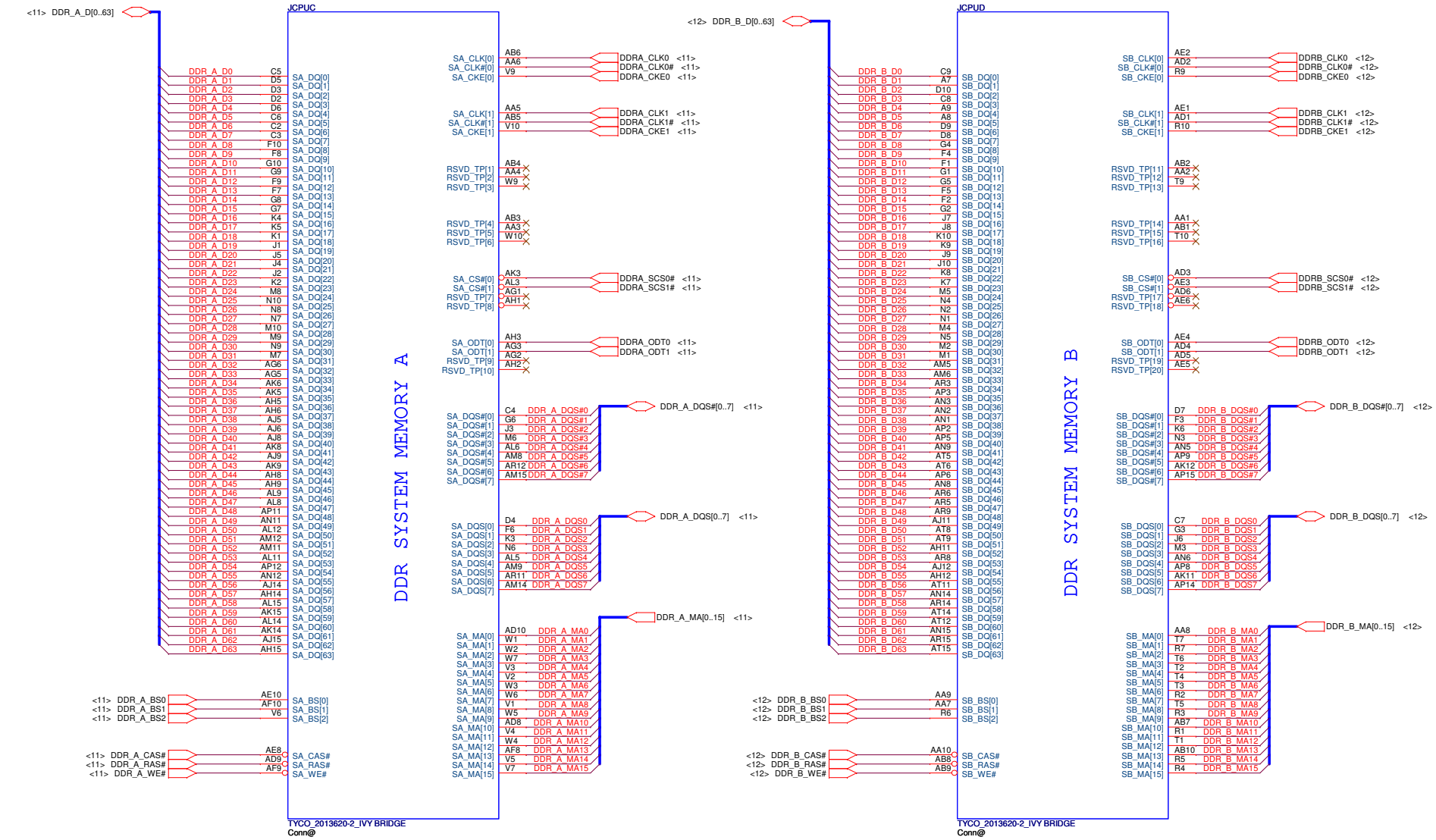

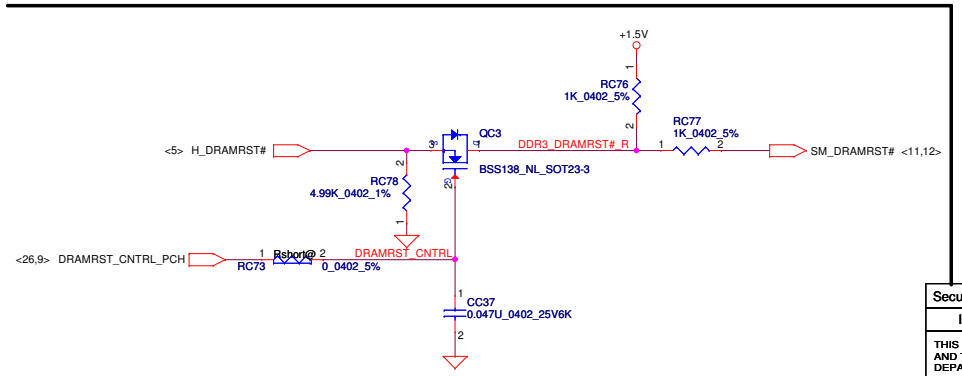

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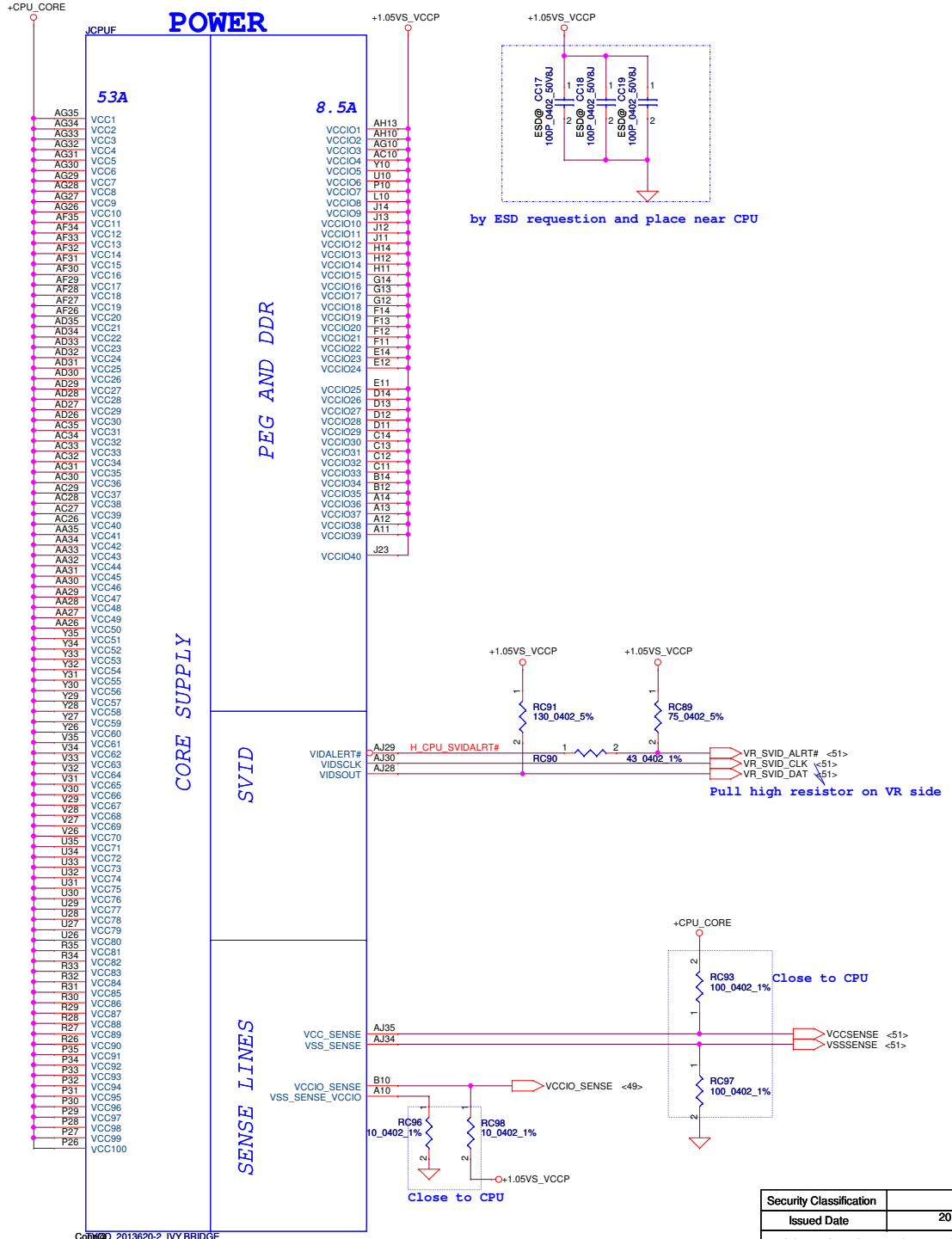

Compal_2013620-2_IVY BRIDGE

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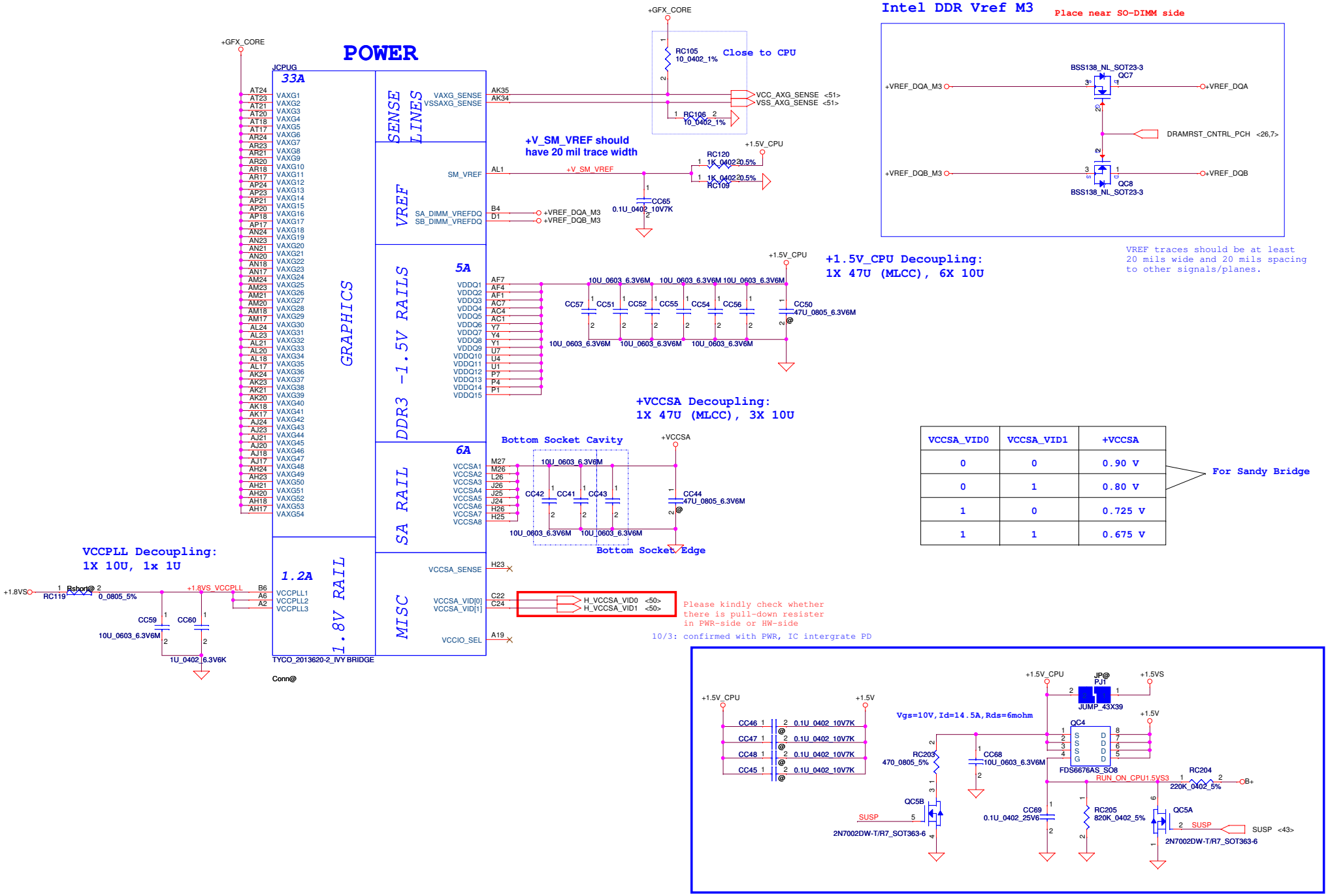
POWER



VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.90 V
0	1	0.80 V
1	0	0.725 V
1	1	0.675 V

For Sandy Bridge

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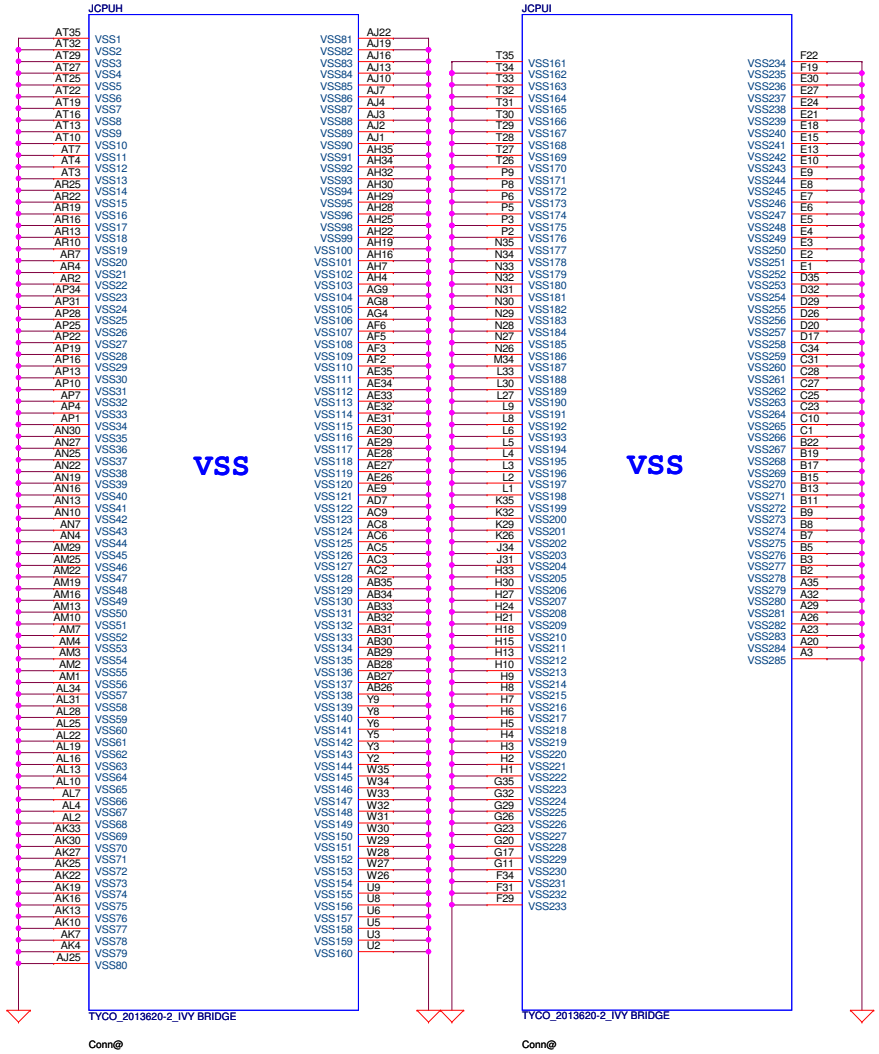
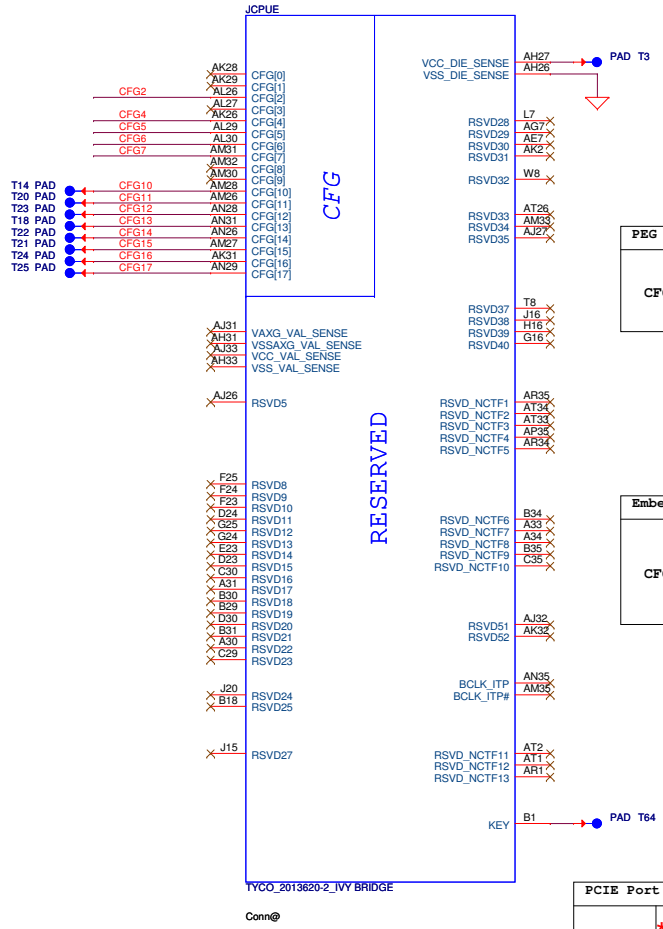
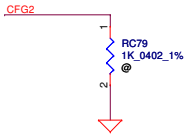


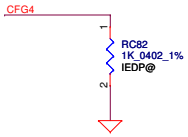


CFG Straps for Processor

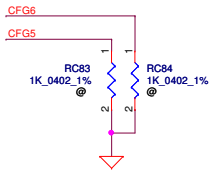
(CFG[17:0] internal pull high 5~15K to VCCIO)



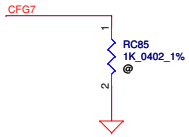
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Embedded Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: *Ivy Bridge_GND/RSVD/CFG*

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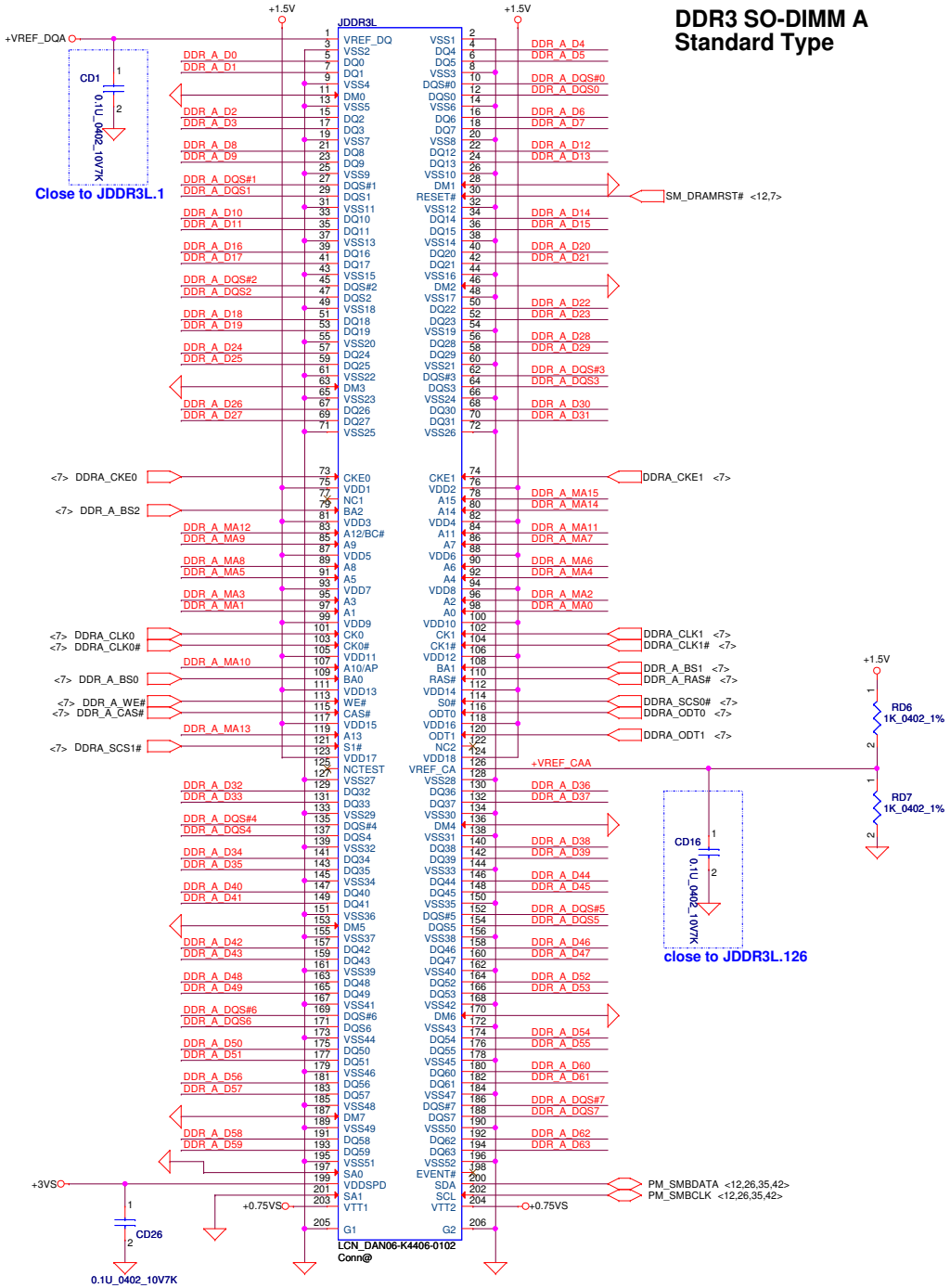
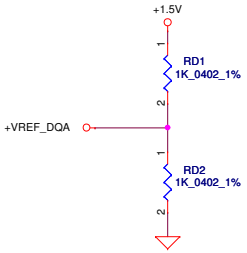
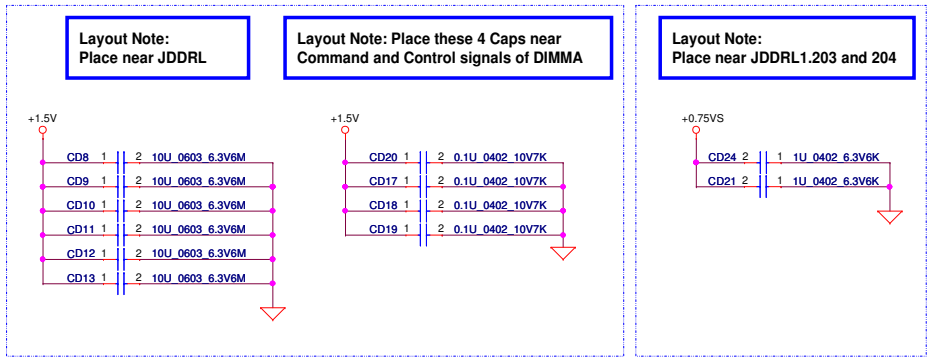
DDR3 SO-DIMM A
Standard Type







SPD setting (SA0, SA1)
PU/PD by Channel A/B
->Channel A 00
->Channel B 01

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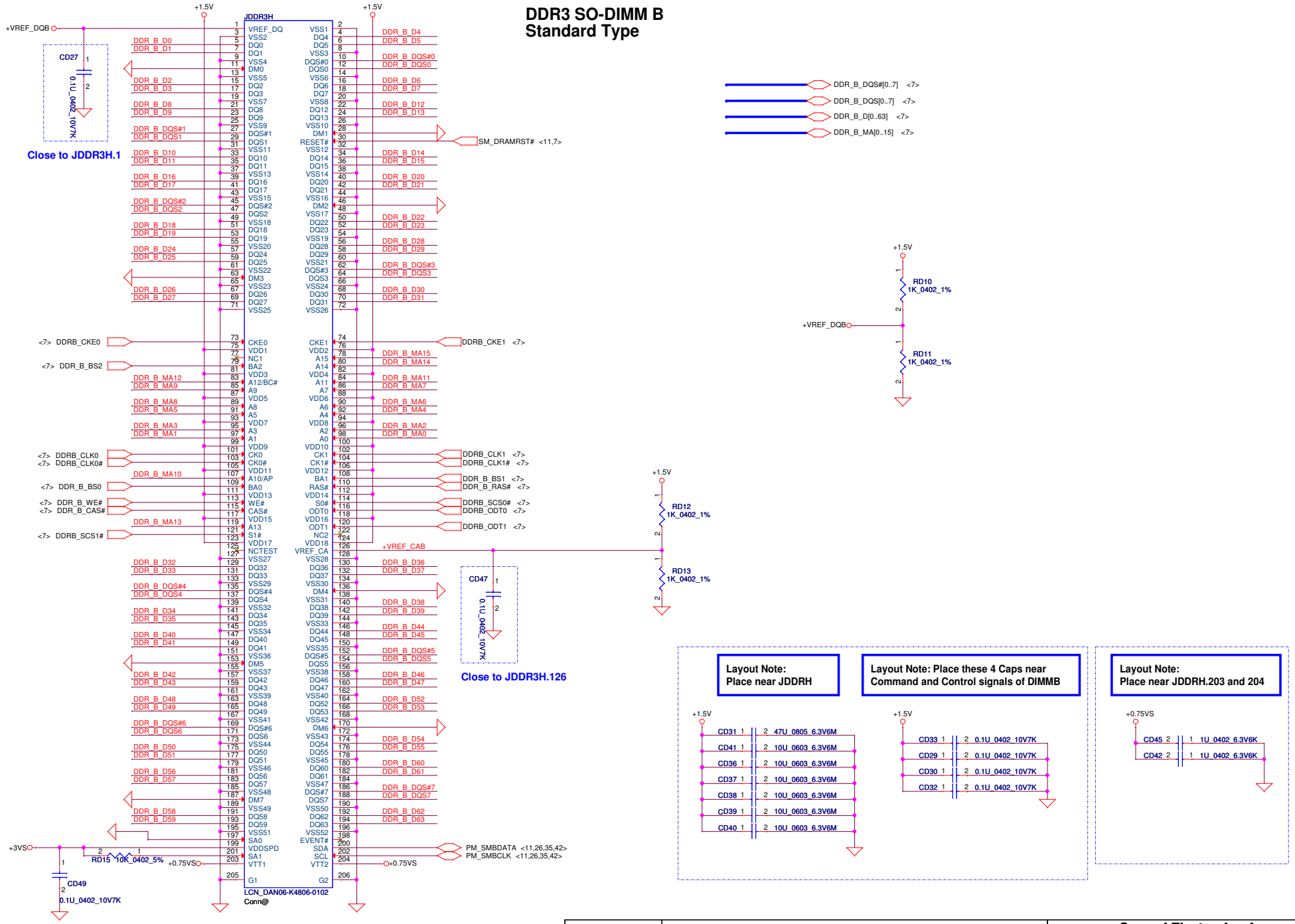
DDR3 SO-DIMM B
Standard Type



SPD setting (SA0, SA1)
PU/PD by Channel A/B
->Channel A 00
->Channel B 01

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Title: ***DDRIII-SODIMM1***

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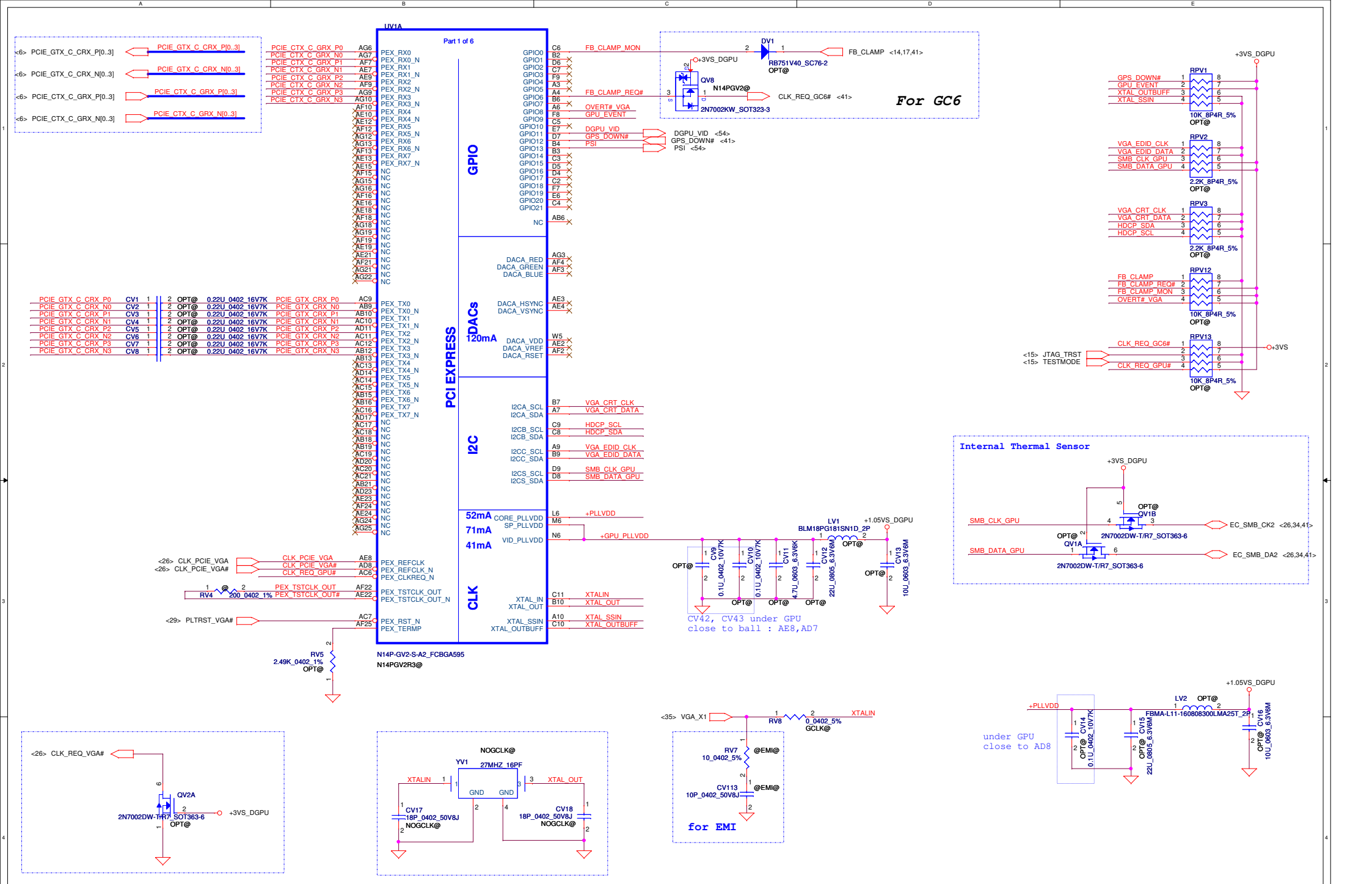

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Title: **VGA_N14x PEG & DAC**

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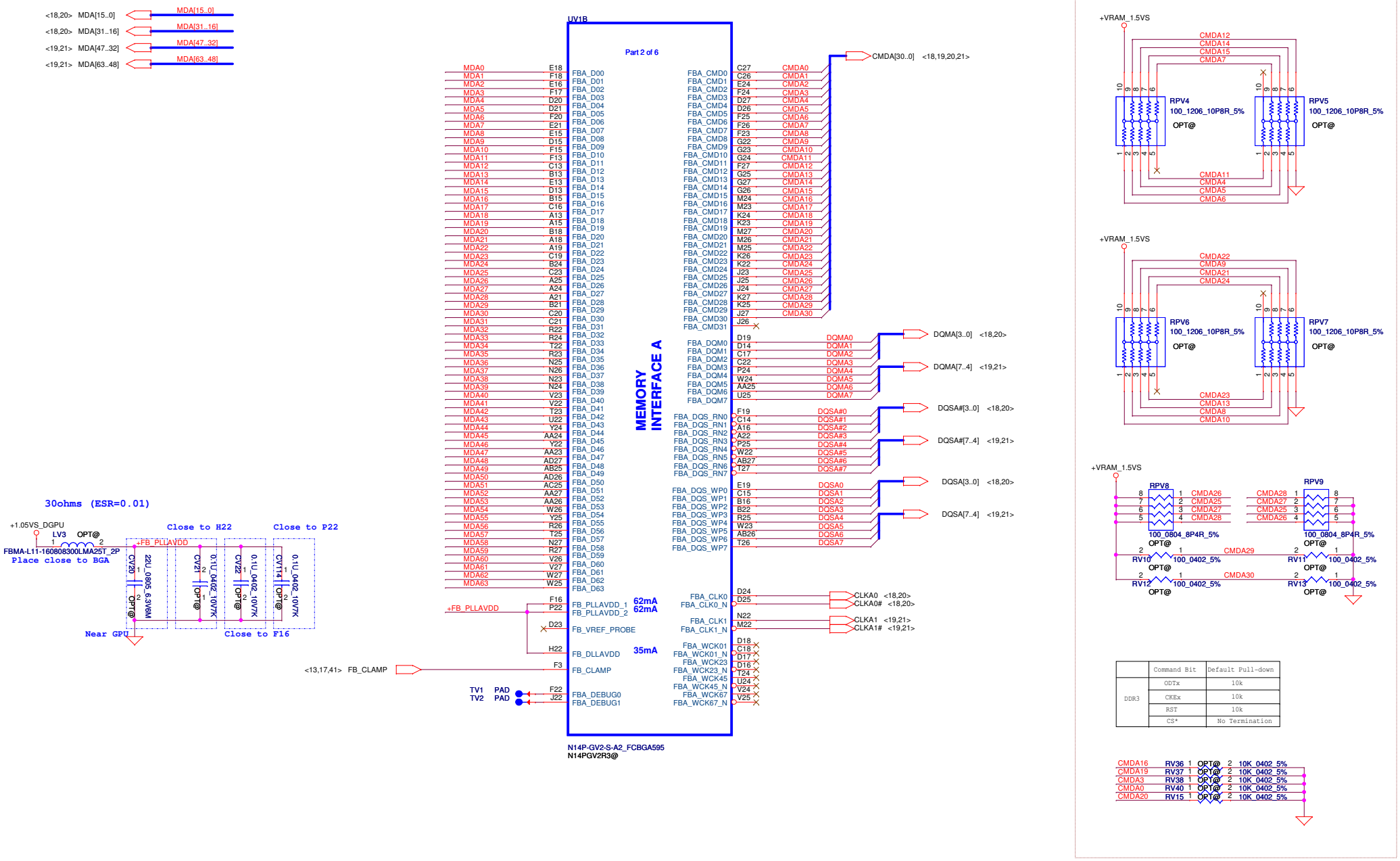
VRAM Interface



	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

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Title: **N14x VRAM Interface**

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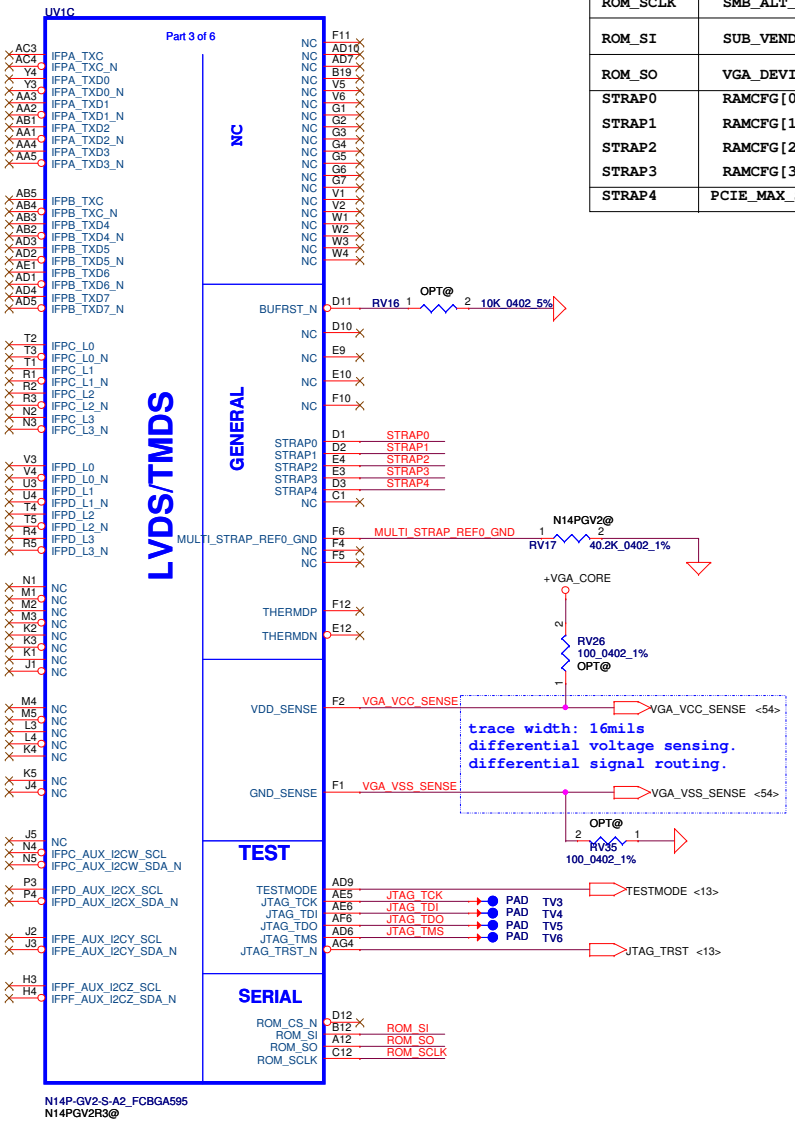


BINARY STRAPS (for N14M-GL)

Strap Pin	Strap Mapping	
ROM_SCLK	SMB_ALT_ADDR	PD 10k
ROM_SI	SUB_VENDOR	PU 10k if VBIOS ROM exists PD 10k if no VBIOS ROM
ROM_SO	VGA_DEVICE	PD 10k (no display)
STRAP0	RAMCFG[0]	Refer to RVL
STRAP1	RAMCFG[1]	
STRAP2	RAMCFG[2]	
STRAP3	RAMCFG[3]	
STRAP4	PCIE_MAX_SPEED	PD 10k

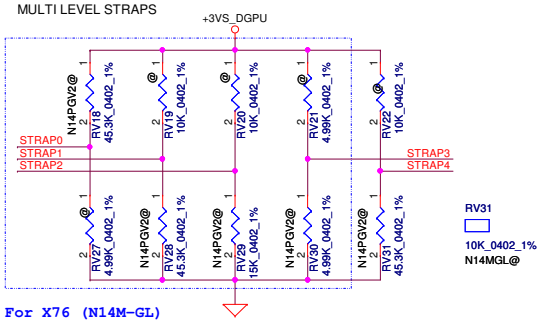
MULTI LEVEL STRAPS (for N14P-GV2)

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	**PCI_DEVID[4]**	SUB_VENDOR	**PCI_DEVID[5]**	PEX_PLLEN_TERM
ROM_SI	+3VS_DGPU	**RAMCFG[3]**	**RAMCFG[2]**	**RAMCFG[1]**	**RAMCFG[0]**
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VS_DGPU	**PCI_DEVID[3]**	**PCI_DEVID[2]**	**PCI_DEVID[1]**	**PCI_DEVID[0]**
STRAP3	+3VS_DGPU	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_DGPU	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

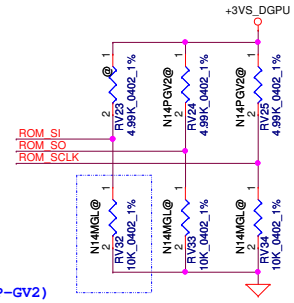
SKU	Device ID	biit5 to bit0
N14P-GV2	0x1292	010010
N14M-GL	0x1140	000000

Resistor Values	Pull-up to +3VS _DGPU	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

MULTI LEVEL STRAPS



For X76 (N14M-GL)



For X76 (N14P-GV2)

GPU		FB Memory gDDR3			ROM_SI
N14P-GV2	128Mx16	Samsung	900MHz	K4W2G1646E-BC11	PD 45.3K
			1GHz	K4W2G1646E-BC1A	
		Hynix	900MHz	H5TQ2G63DFR-11C	PD 34.8K
			1GHz	H5TQ2G63DFR-N0C	
		Micron	900MHz	MT41K128M16JT-107G	PD 30K
	256Mx16	Samsung	900MHz	K4W4G1646B-HC11	PD 20K
		Micron	900MHz	MT41K256M16HA-107G	PD 10K

GPU		FB Memory gDDR3			STRAP[3:0]
N14M-GL	128Mx16	Samsung	900MHz	K4W2G1646E-BC11	0101
			1GHz	K4W2G1646E-BC1A	
		Hynix	900MHz	H5TQ2G63DFR-11C	0110
			1GHz	H5TQ2G63DFR-N0C	
		Micron	900MHz	MT41K128M16JT-107G	0001
	256Mx16	Samsung	900MHz	K4W4G1646B-HC11	1011
		Micron	900MHz	MT41K256M16HA-107G	1101

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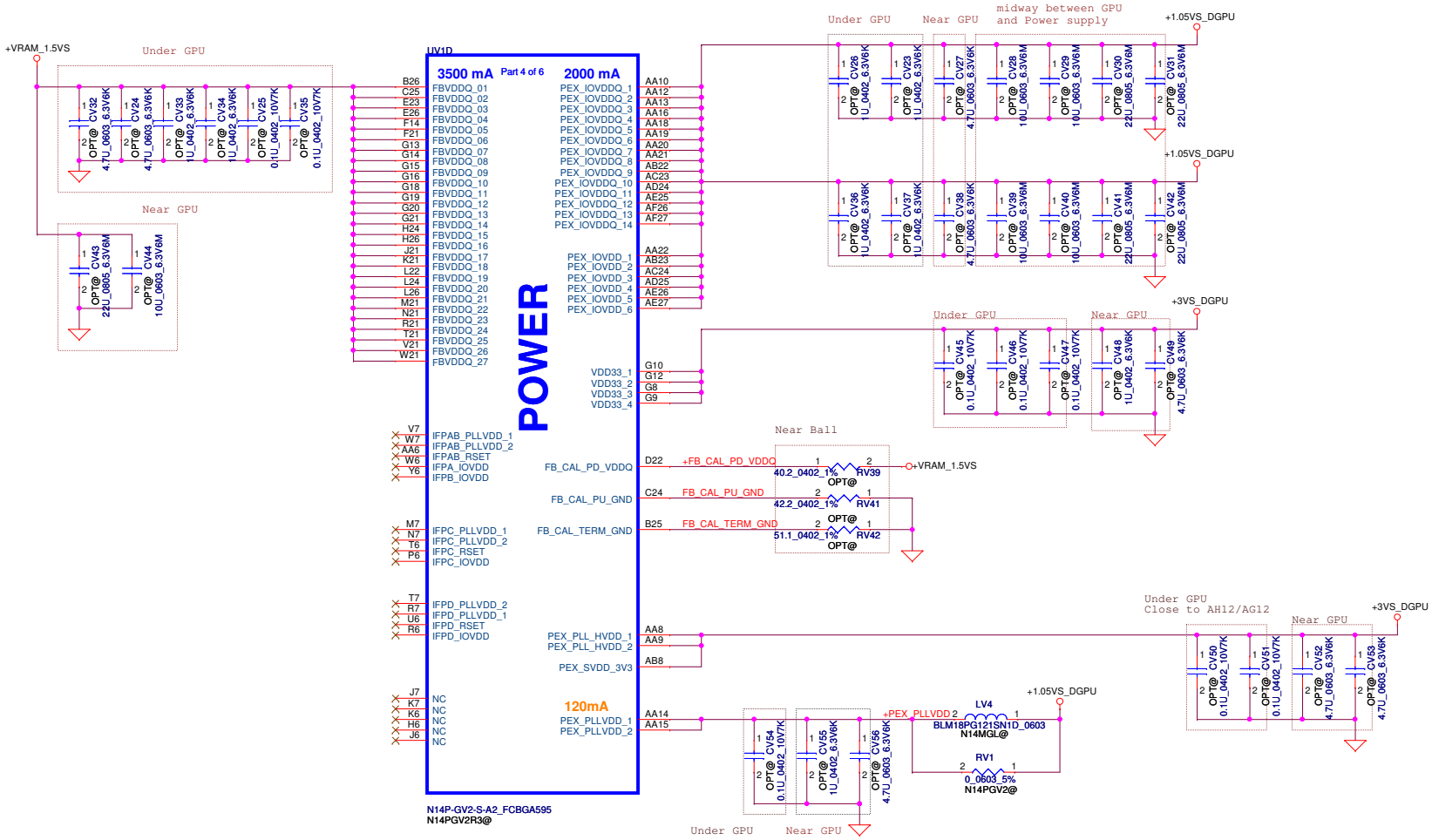

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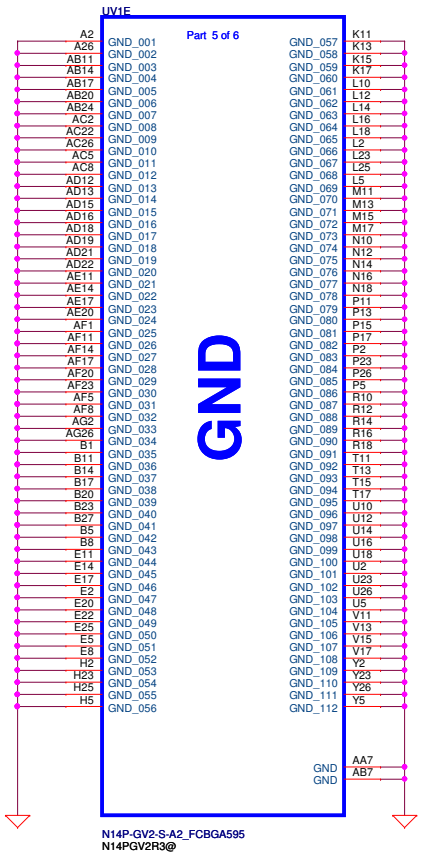
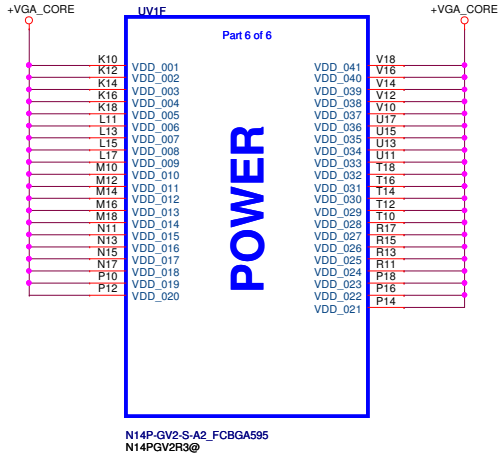
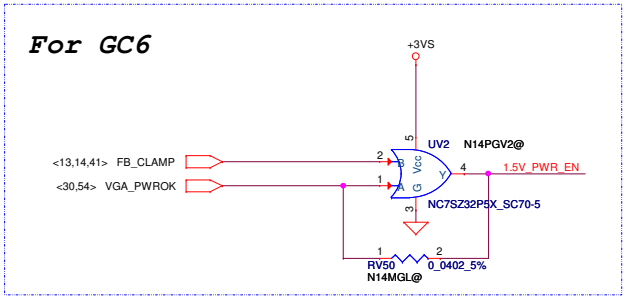
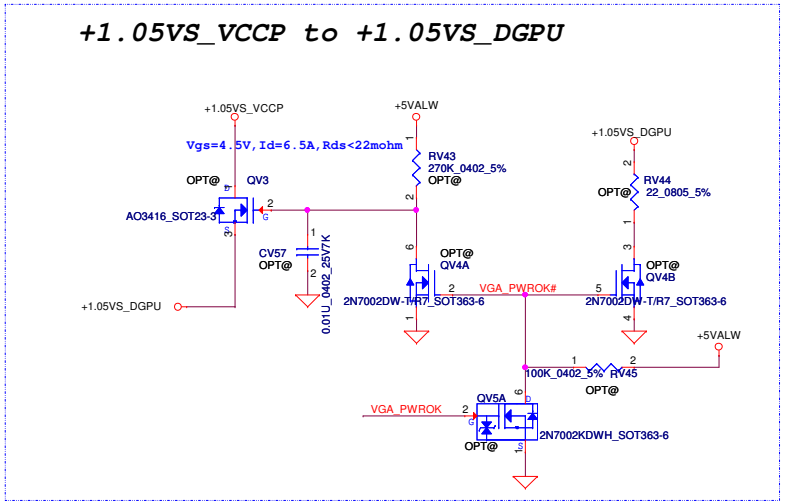
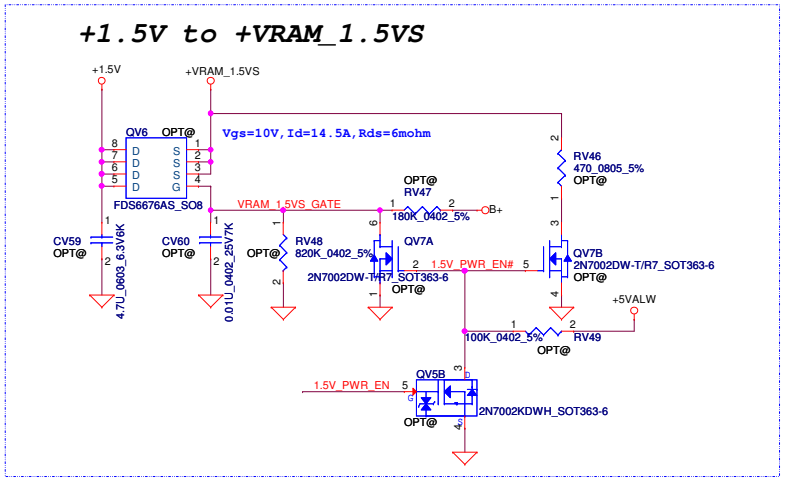
				Date: Monday, March 11, 2013; Sheet 16 of 56

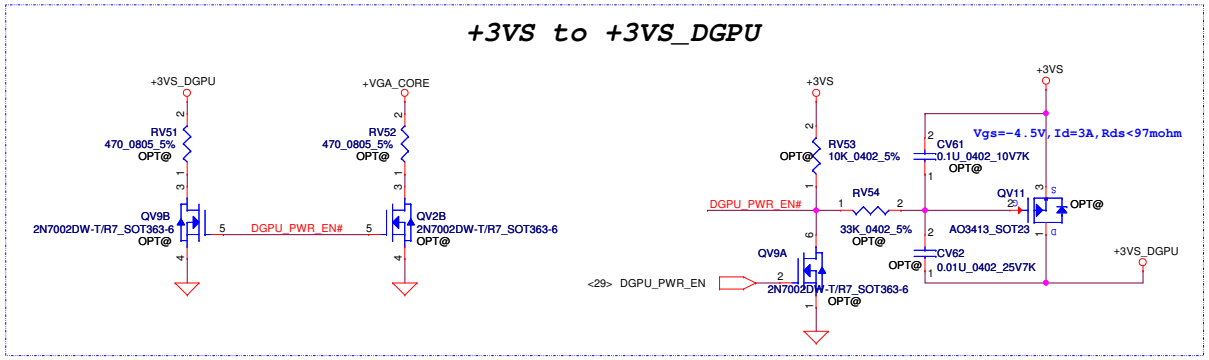












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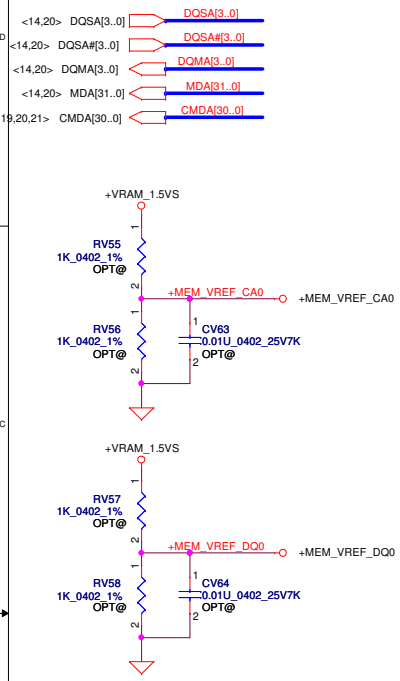
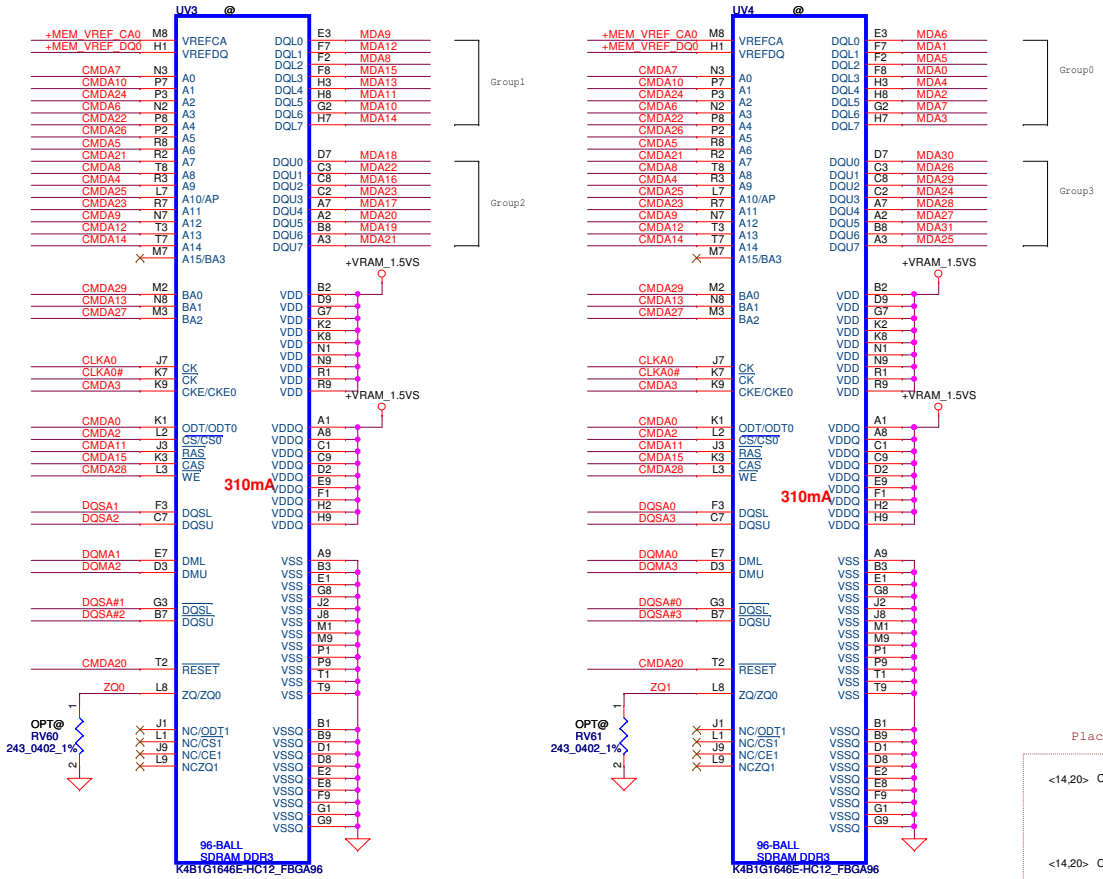
RANK 0 [31...0]

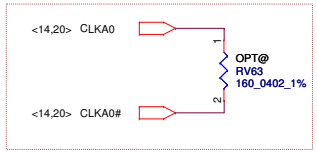
VRAM DDR3 Chips



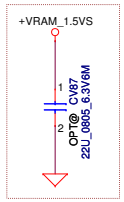


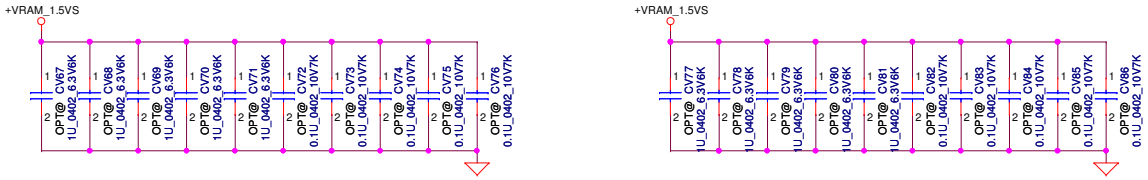
Mode E Address	Rank 0 0..31	Rank 0 32..63	Rank 1 0..31	Rank 1 32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

Place close to the first T point



Place close to RANK0 VRAM





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Title: **VGA_N14x VRAM RANK 0L**

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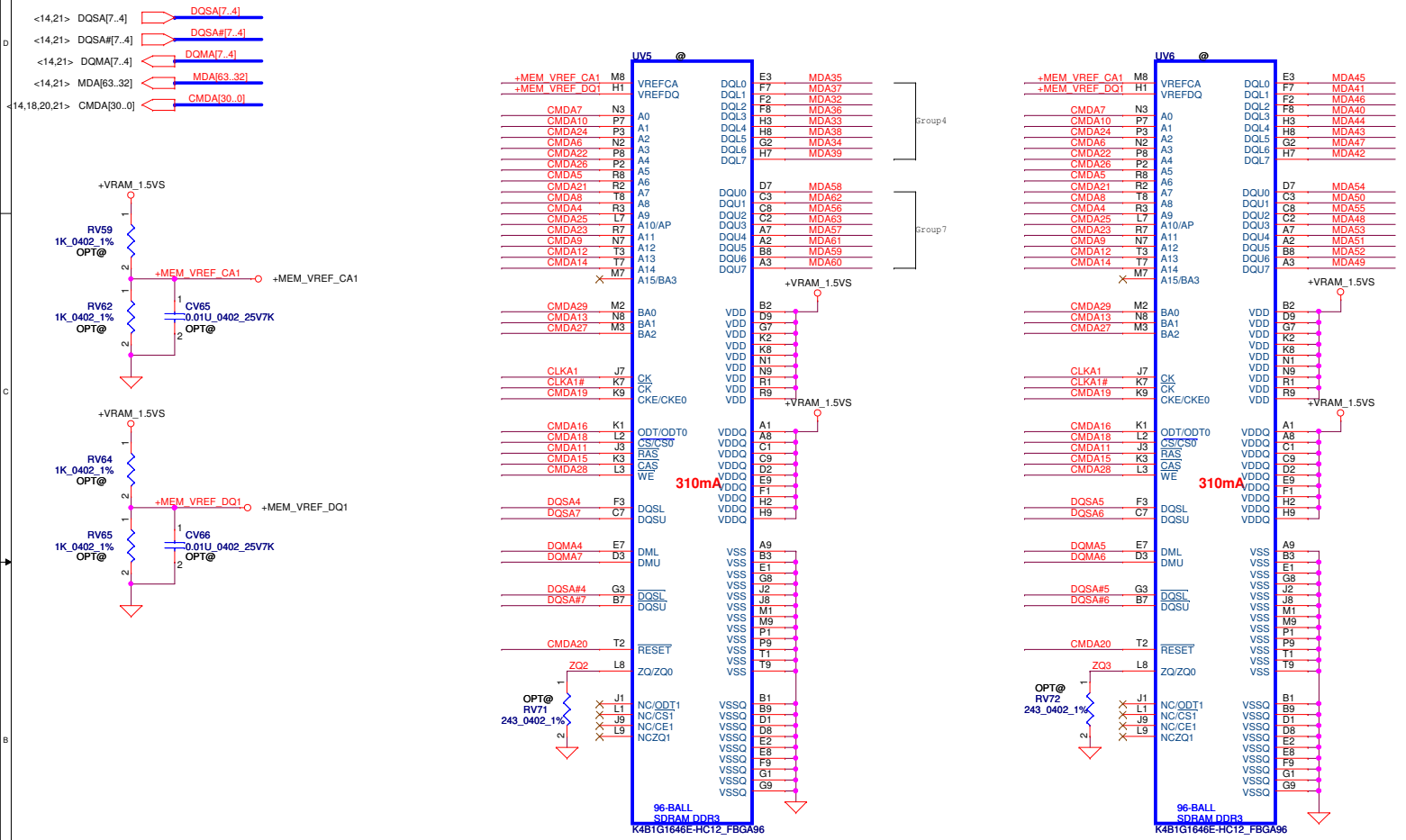
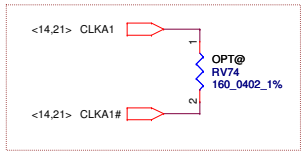
RANK 0 [63...32]

VRAM DDR3 Chips

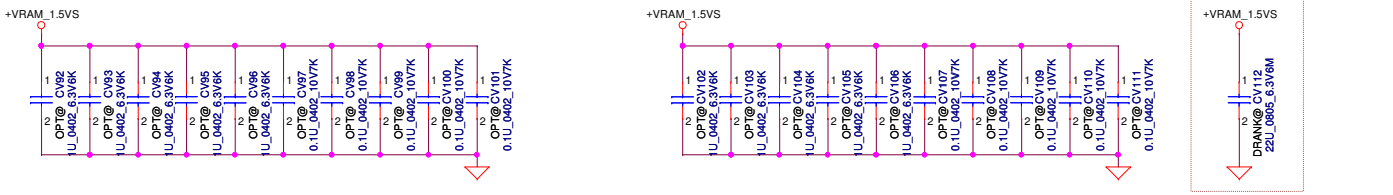


Mode E Address	Rank 0 0..31	Rank 0 32..63	Rank 1 0..31	Rank 1 32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

Place close to the first T point



Place close to RANK1 VRAM



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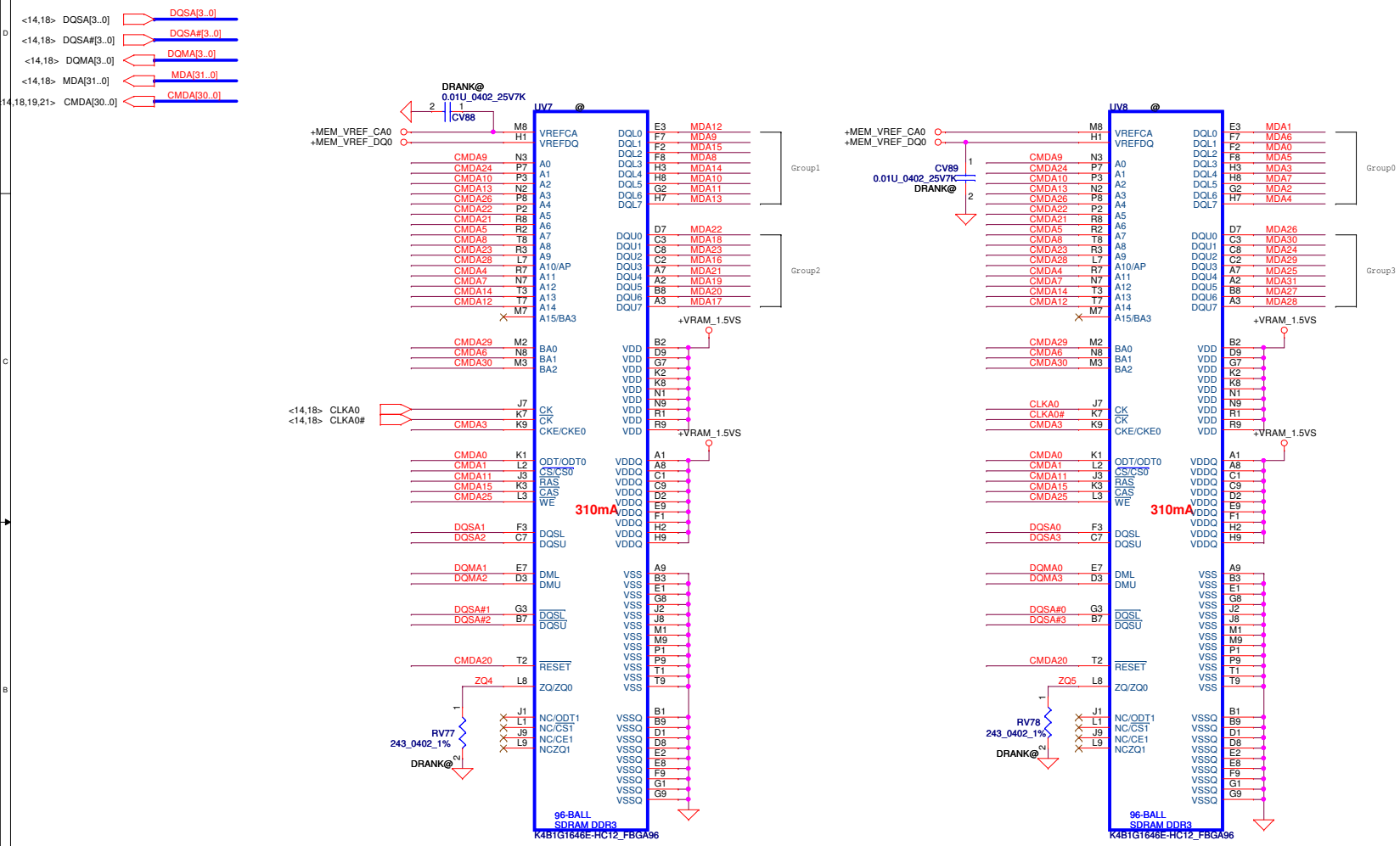
RANK 1 [31...0]

VRAM DDR3 Chips



Mode E Address	Rank 0		Rank 1	
	0..31	32..63	0..31	32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

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Title: **VGA_N14x VRAM RANK 1L**

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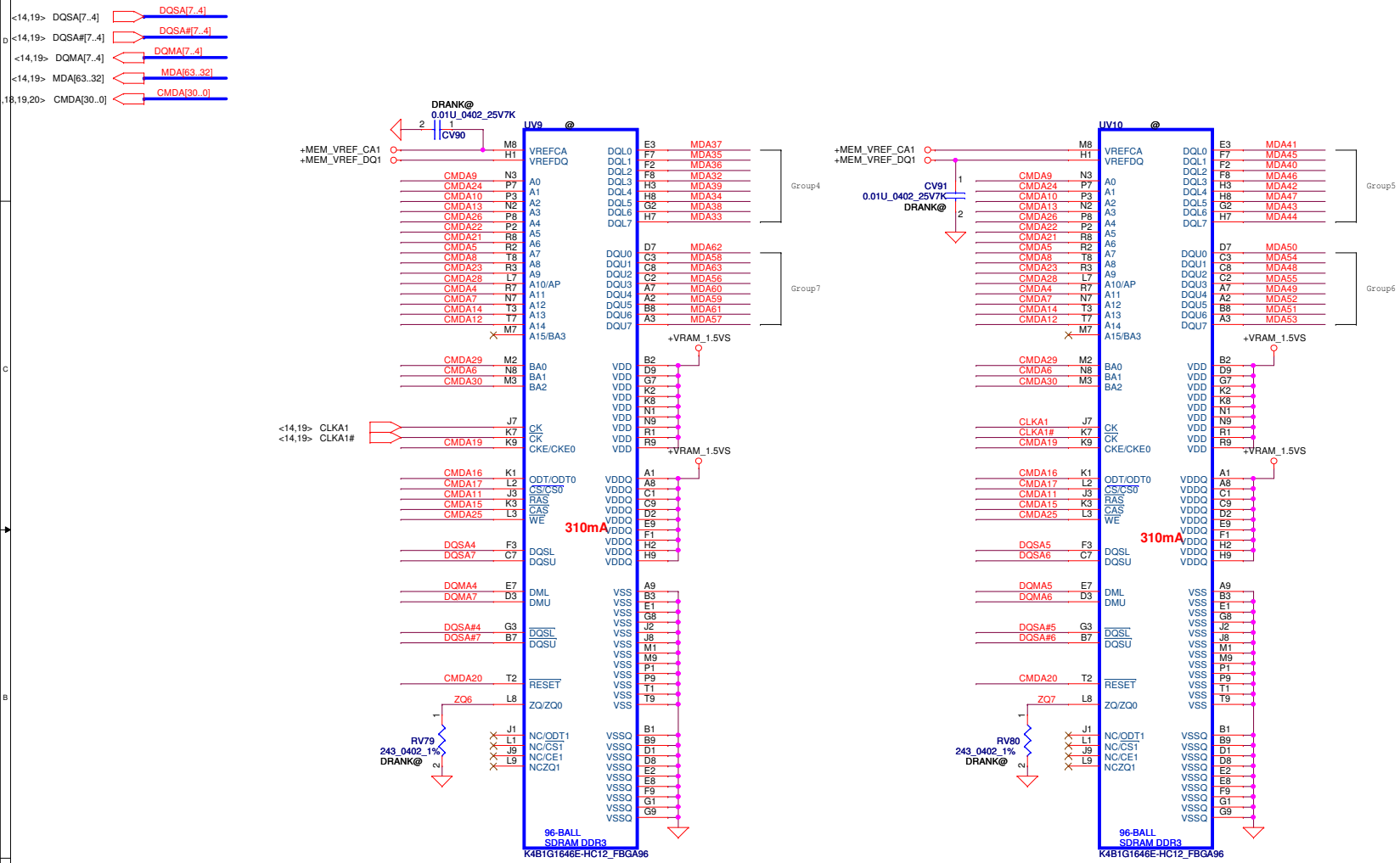
RANK 1 [63...32]

VRAM DDR3 Chips



Mode E Address	Rank 0 0..31	Rank 0 32..63	Rank 1 0..31	Rank 1 32..63
CMD0	ODT		ODT	
CMD1			CS1#	
CMD2	CS0#			
CMD3	CKE		CKE	
CMD4	A9	A9	A11	A11
CMD5	A6	A6	A7	A7
CMD6	A3	A3	BA1	BA1
CMD7	A0	A0	A12	A12
CMD8	A8	A8	A8	A8
CMD9	A12	A12	A0	A0
CMD10	A1	A1	A2	A2
CMD11	RAS#	RAS#	RAS#	RAS#
CMD12	A13	A13	A14	A14
CMD13	BA1	BA1	A3	A3
CMD14	A14	A14	A13	A13
CMD15	CAS#	CAS#	CAS#	CAS#
CMD16		ODT		ODT
CMD17				CS1#
CMD18		CS0#		
CMD19		CKE		CKE
CMD20	RST	RST	RST	RST
CMD21	A7	A7	A6	A6
CMD22	A4	A4	A5	A5
CMD23	A11	A11	A9	A9
CMD24	A2	A2	A1	A1
CMD25	A10	A10	WE#	WE#
CMD26	A5	A5	A4	A4
CMD27	BA2	BA2		
CMD28	WE#	WE#	A10	A10
CMD29	BA0	BA0	BA0	BA0
CMD30			BA2	BA2

Security Classification	Compal Secret Data		
Issued Date	2012/12/07	Deciphered Date	2013/12/07

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Title: VGA_N14x VRAM RANK 1H

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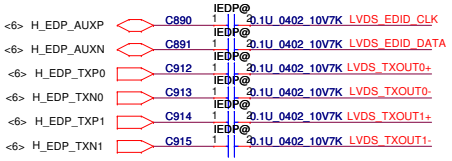
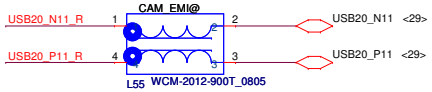
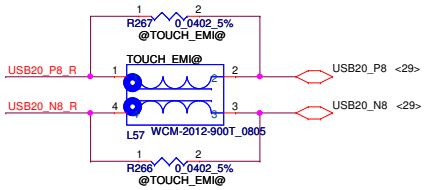
For eDP Panel





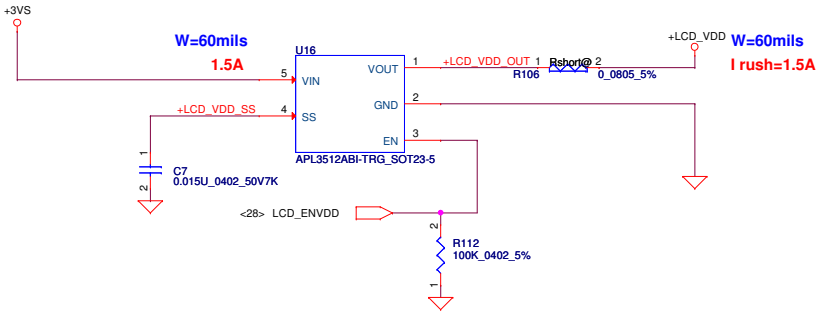
Reserve for EMI request



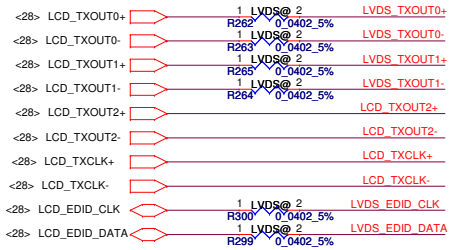
Reserve for EMI request

LCD POWER CIRCUIT

eDP&LVDS both 3V power rail



For LVDS 1ch Panel

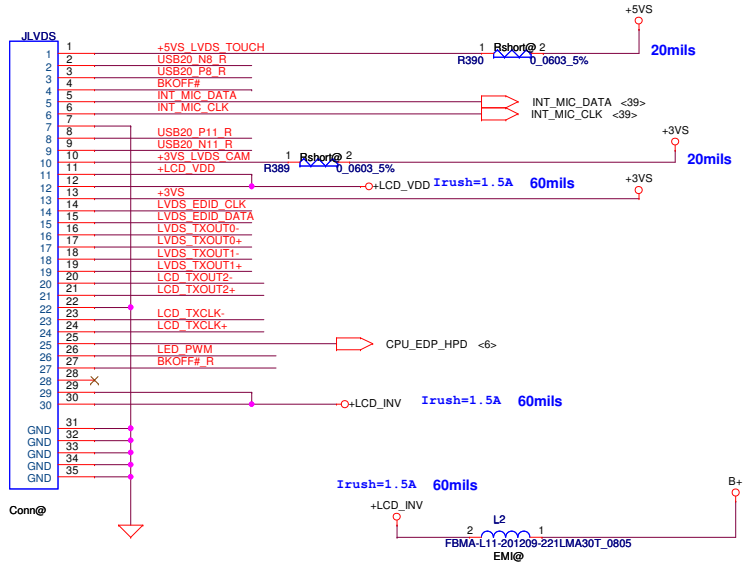


LVDS colay eDP cable

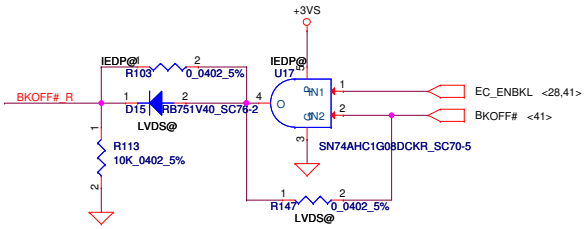
pin1-4 Touch function for panel

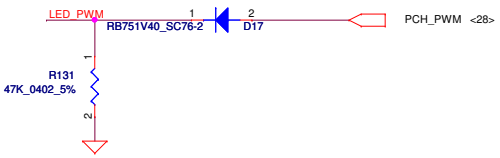
pin5-10 For Webcam with single or dual MIC

pin11-30 For LVDS or EDP panel



Reserve for eDP panel potential issue





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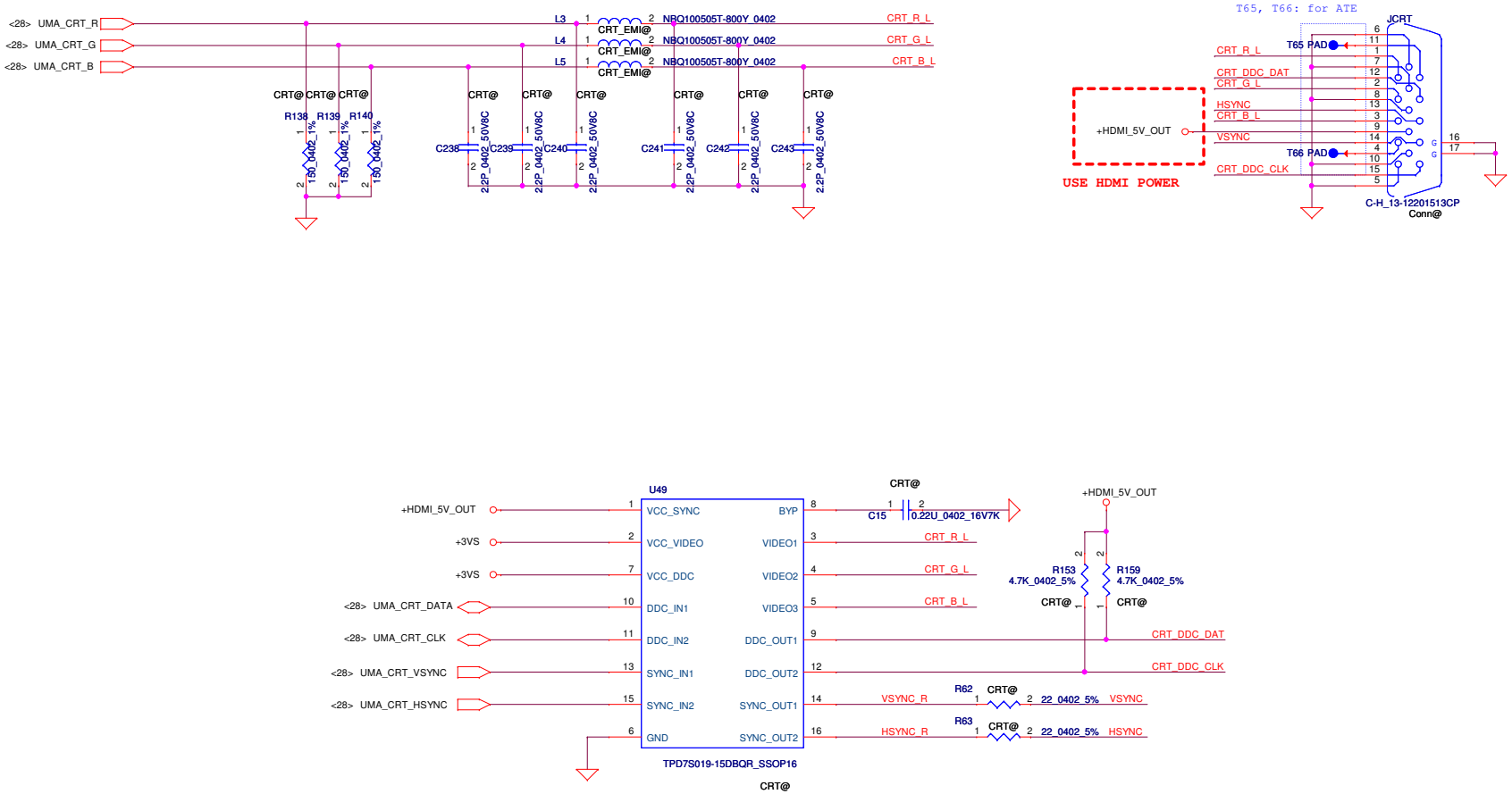
				Date: Monday, March 11, 2013; Sheet 22 of 56

CRT CONNECTOR



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Issued Date	2012/12/07	Deciphered Date	2013/12/07	Title: CRT
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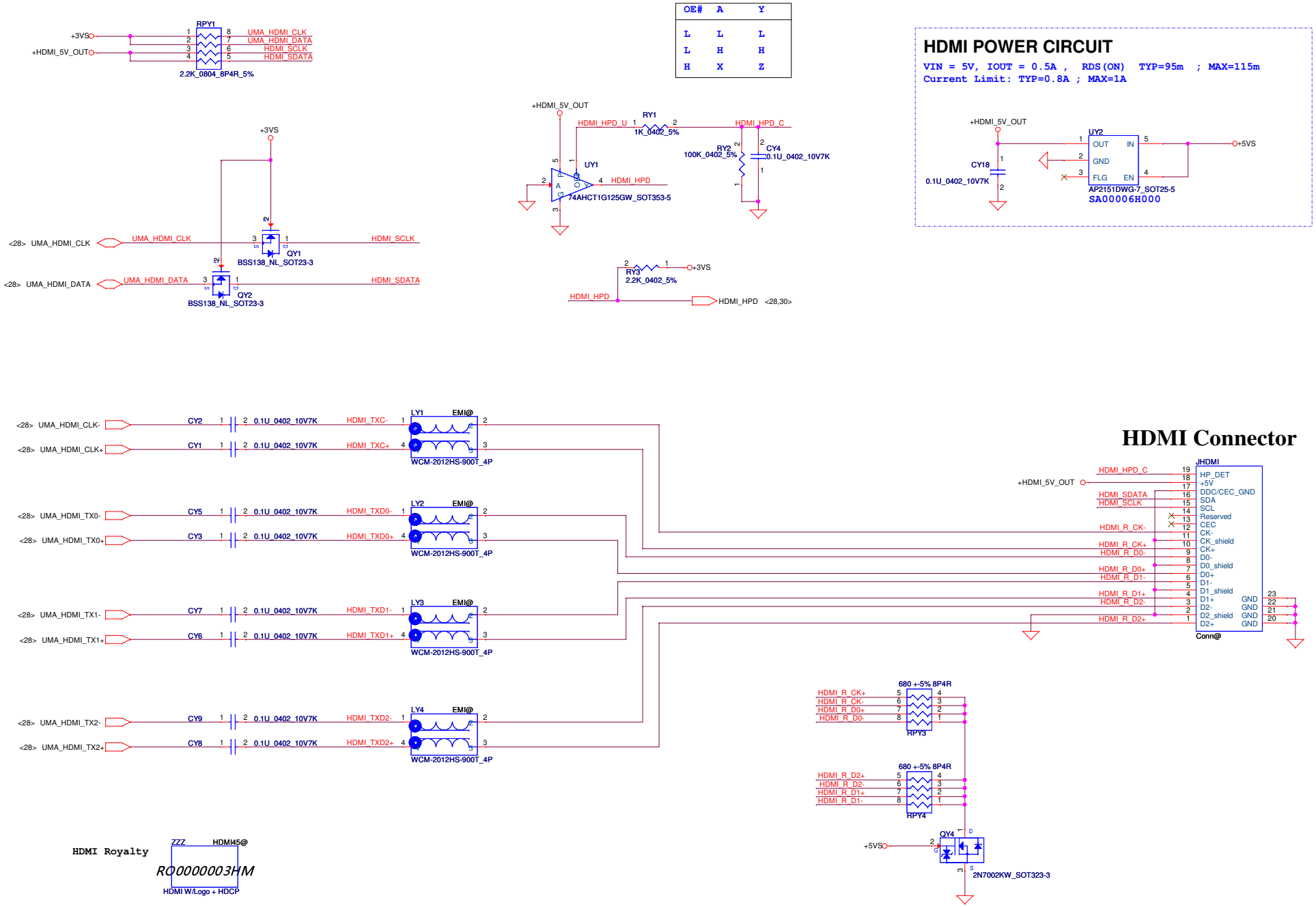
				Date: Monday, March 11, 2013 / Sheet 23 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/12/07	Deciphered Date	2013/12/07

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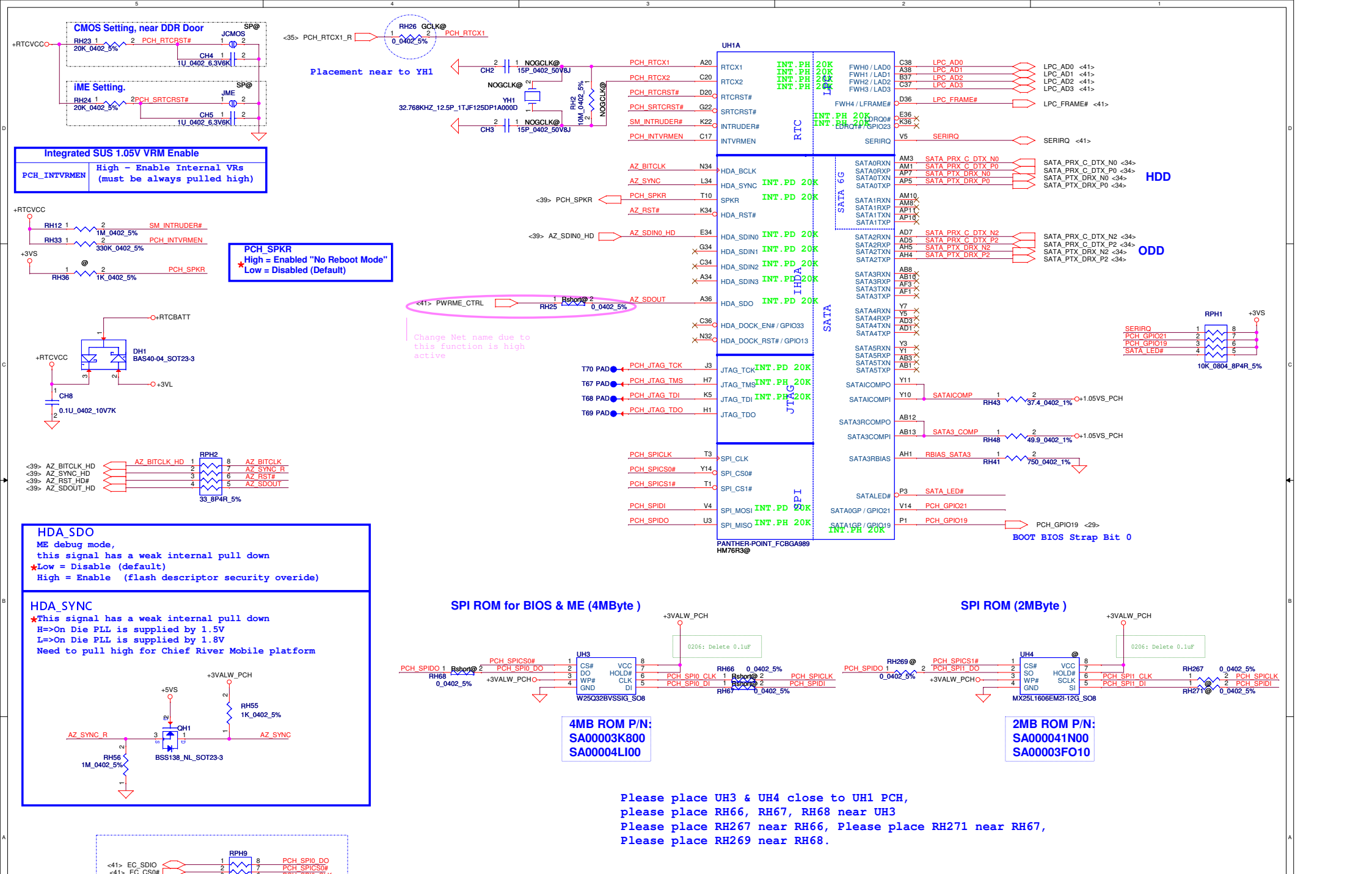
Compal Electronics, Inc.

Title: ***HDMI Conn.***

Size: B25 | Document Number: **VFKAA** | Rev: 0.2

Date: Monday, March 11, 2013 | Sheet 24 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/12/07	Deciphered Date	2013/12/07

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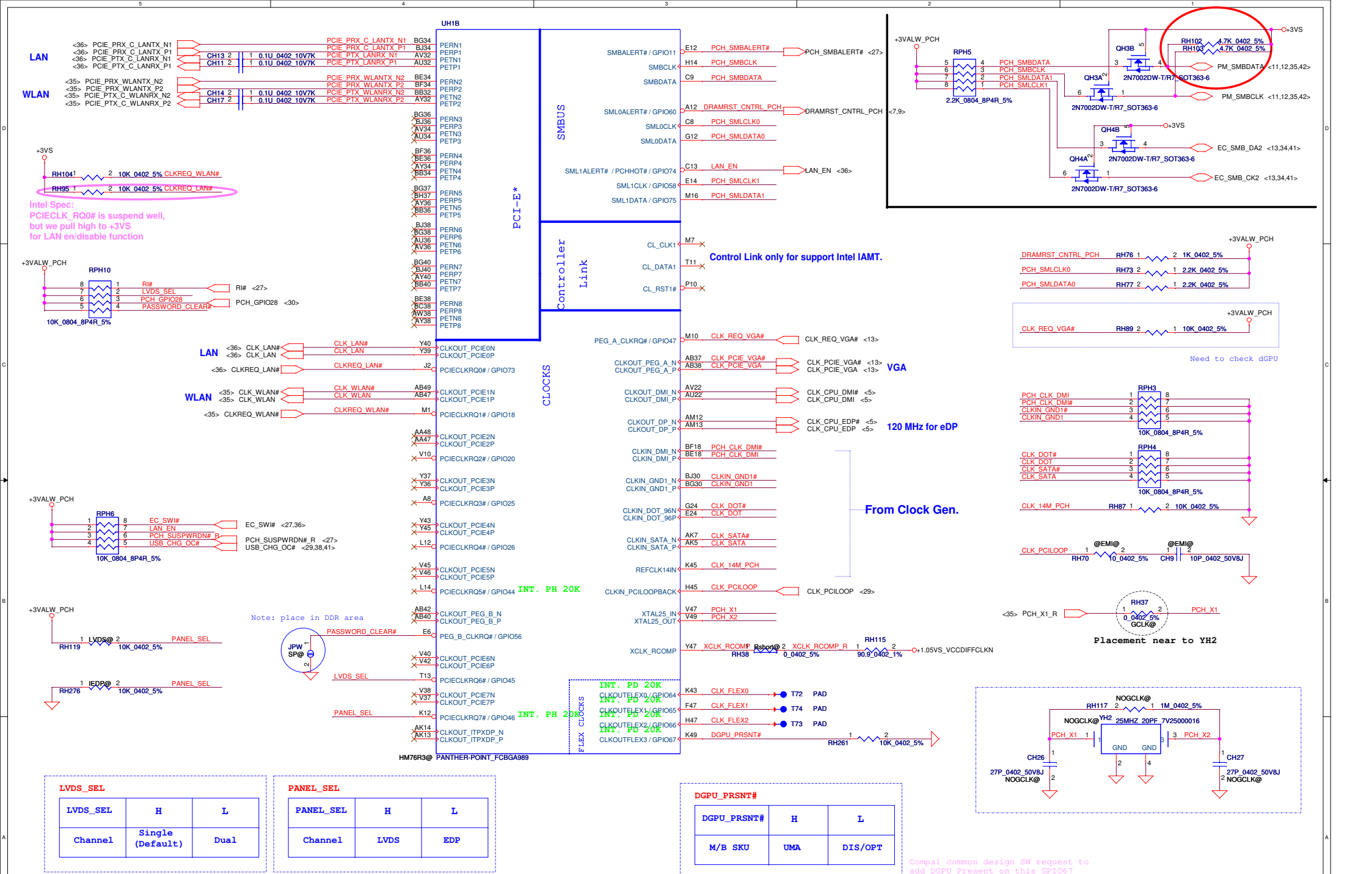
Compal Electronics, Inc.

Title: *PCH_HDA/JTAG/SATA/SPI/LPC*

Size: Custom | Document Number: VFKAA | Rev: 0.2

Date: Monday, March 11, 2013 | Sheet 25 of 56



LVDS_SEL

LVDS_SEL	H	L
Channel	Single (Default)	Dual

PANEL_SEL

PANEL_SEL	H	L
Channel	LVDS	EDP

DGPU_PRSNT#

DGPU_PRSNT#	H	L
M/B SKU	UMA	DIS/OPT

Compal common design SW request to add DGPU_Present on this GPIO67

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/12/07	Deciphered Date	2013/12/07	Title: PCH_PCI-E/SMBUS/CLK
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				Date: Monday, March 11, 2013; Sheet 26 of 56

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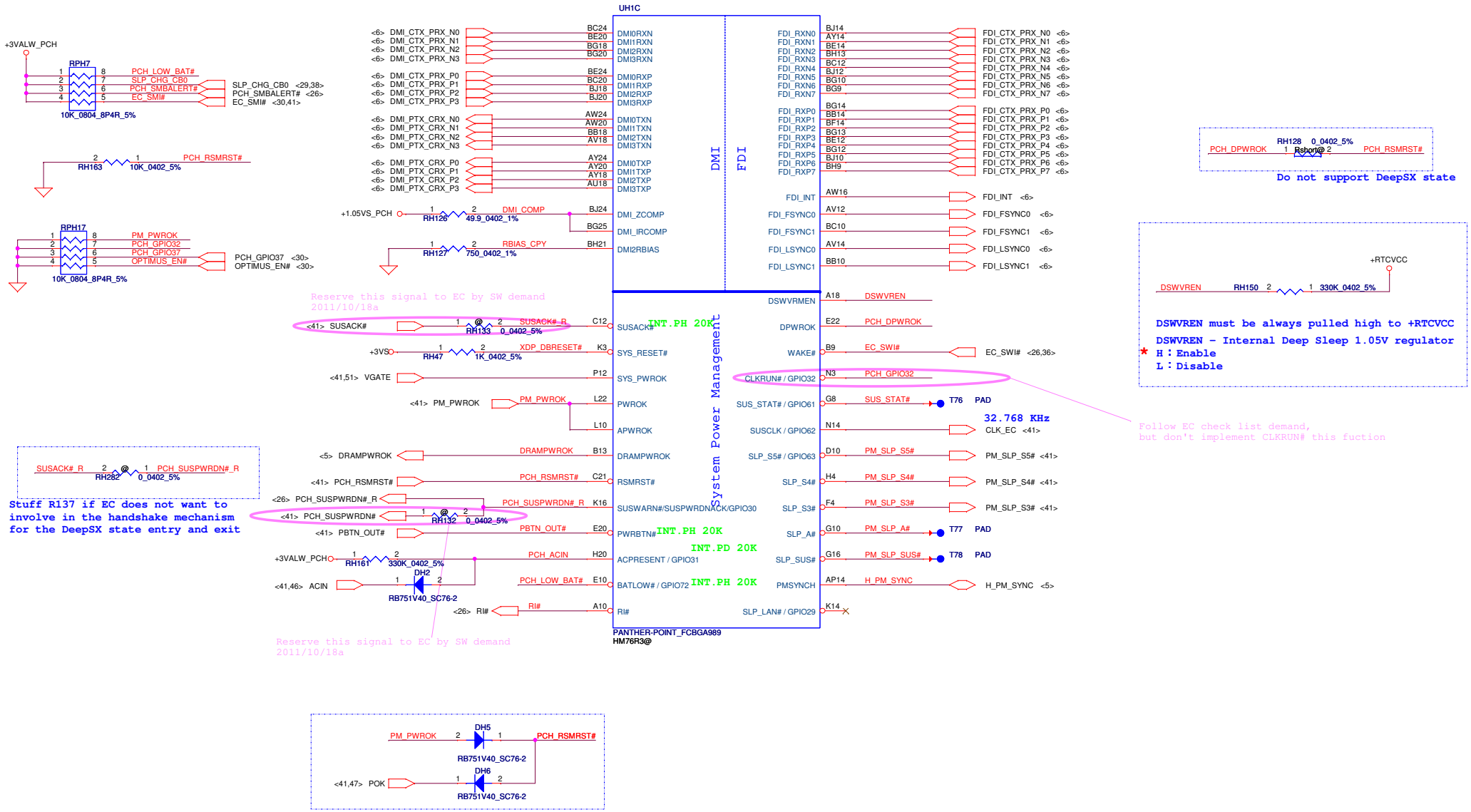

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/12/07	Deciphered Date	2013/12/07	Title: PCH_DMI/FDI/PM
				Size: Custom; Document Number: VFKAA; Rev: 0.2
				Date: Monday, March 11, 2013; Sheet 27 of 56

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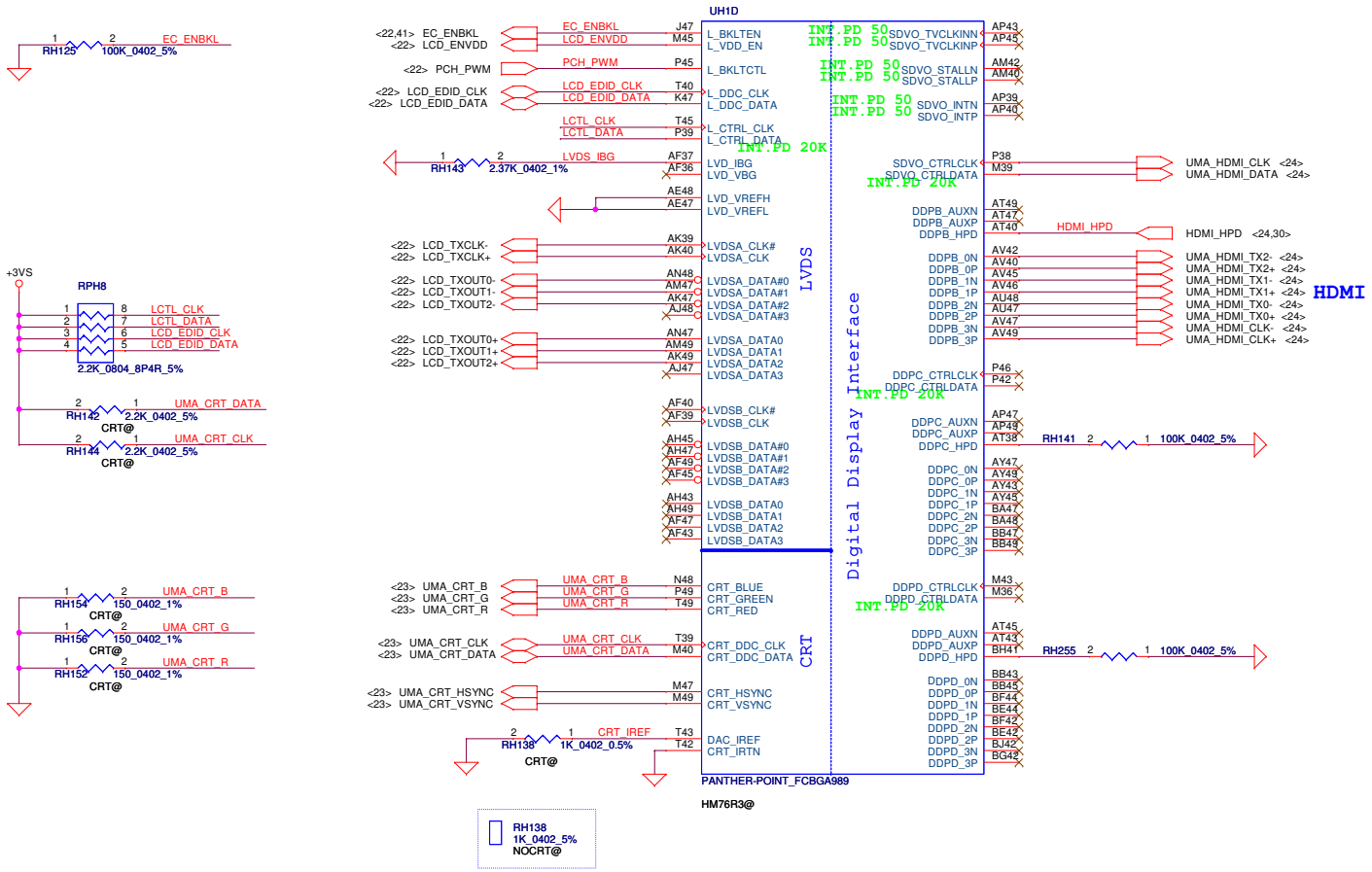

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/12/07	Deciphered Date	2013/12/07	Title: PCH_CRT/LVDS/HDMI
				Size: Custom; Document Number: VFKAA; Rev: 0.2
				Date: Monday, March 11, 2013; Sheet 28 of 56

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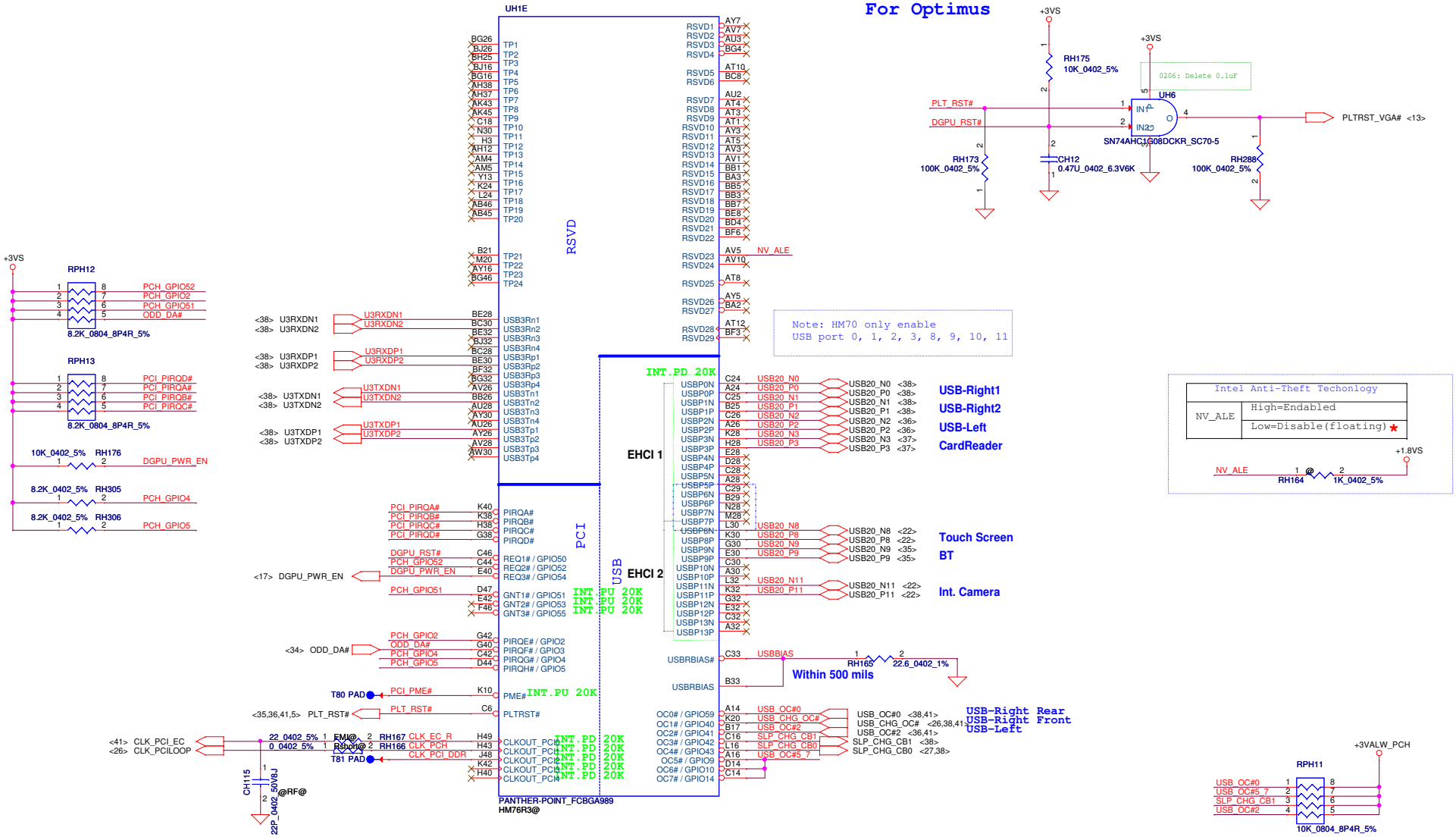

Boot BIOS Strap

PCH_GPIO51	PCH_GPIO19	Boot BIOS Loaction
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI ★

A16 Swap Override Strap

WL_OFF#	★	Low= A16 swap override Enable High= A16 swap override Disable

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/12/07	Deciphered Date 2013/12/07	Title: PCH_PCI/USB/NAND
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			Date: Monday, March 11, 2013; Sheet 29 of 56

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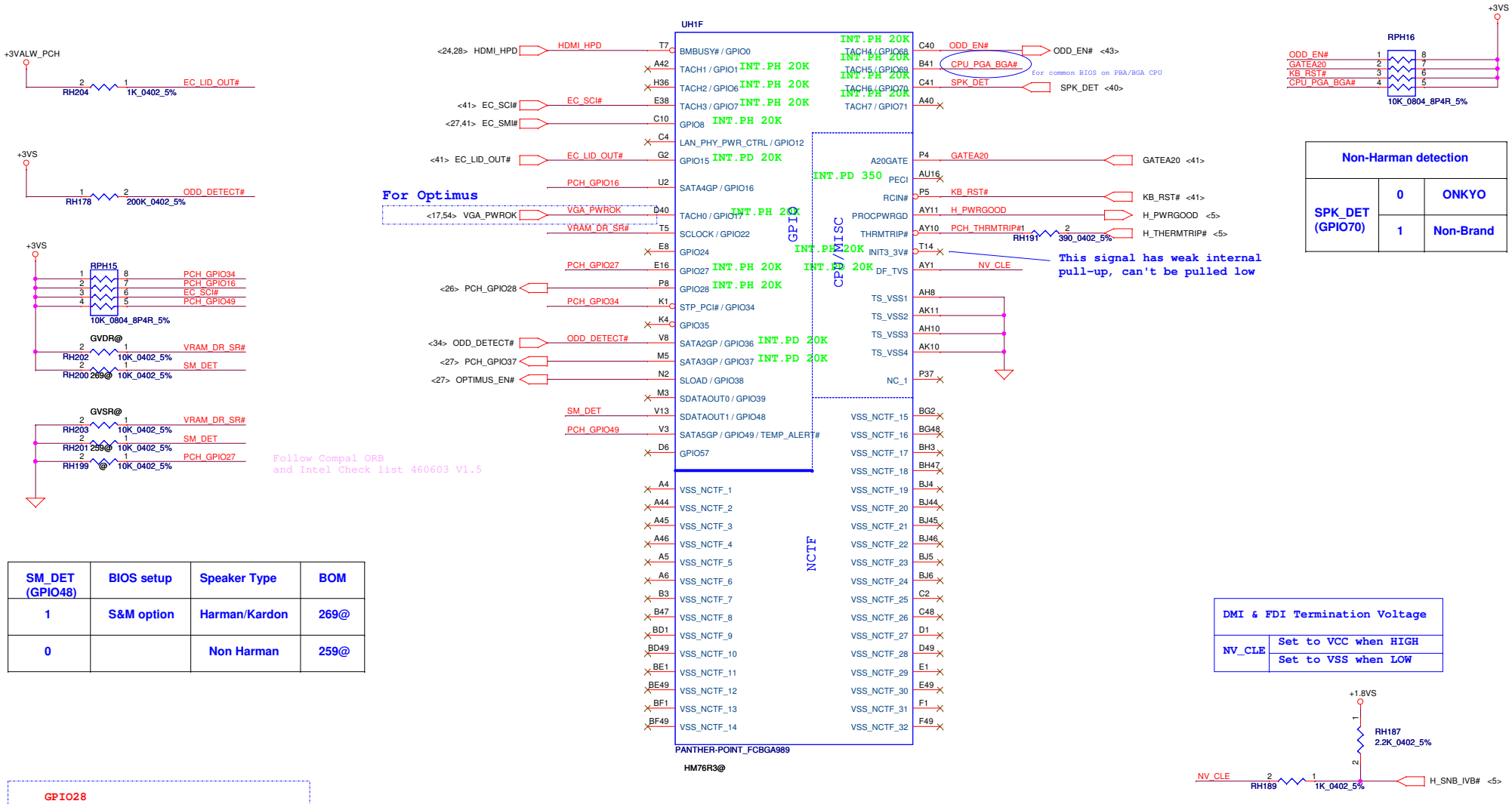

Non-Harman detection		
SPK_DET (GPIO70)	0	ONKYO
	1	Non-Brand

SM_DET (GPIO48)	BIOS setup	Speaker Type	BOM
1	S&M option	Harman/Kardon	269@
0		Non Harman	259@

DMI & FDI Termination Voltage	
NV_CLE	Set to VCC when HIGH
	Set to VSS when LOW

GPIO28

On-Die PLL Voltage Regulator
★ H: Enable
L: Disable

GPIO8

Integrated Clock Chip Enable (Removed)
H: Disable
★ L: Enable

Integrated clock enable functionality is achieved by soft-strap
The current default is clock enable

OPTIMUS_EN#

OPTIMUS_EN#	H	L
SKU	NonOPT	Optimus

Security Classification	Compal Secret Data		
Issued Date	2012/12/07	Deciphered Date	2013/12/07

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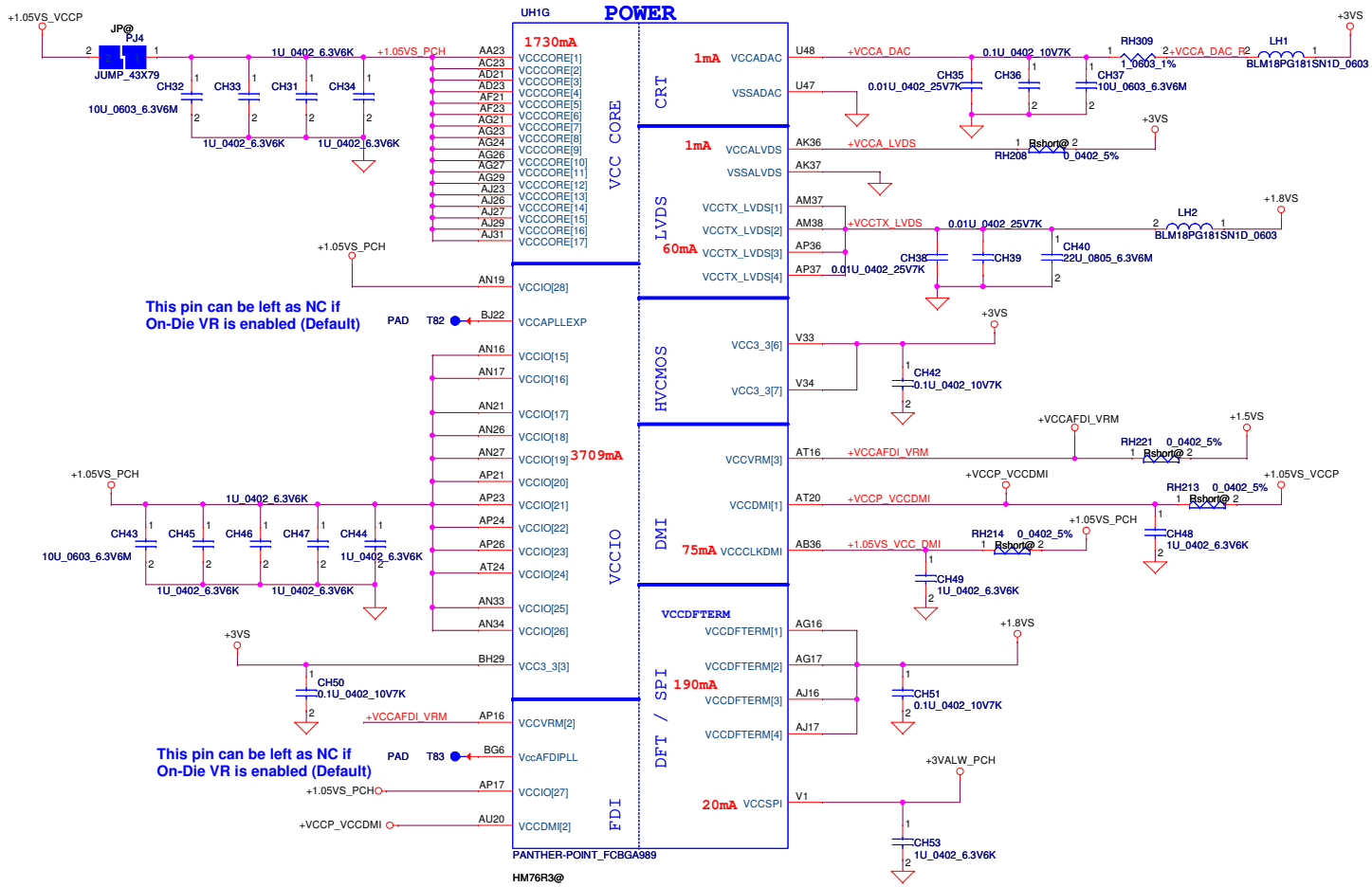
Compal Electronics, Inc.

Title: *PCH_CPU/GPIO*

Size: Custom | Document Number: VFKAA | Rev: 0.2

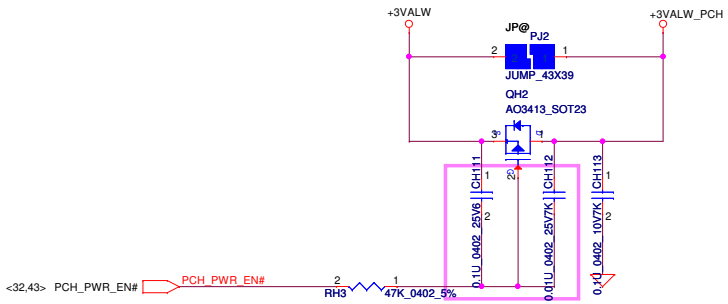
Date: Monday, March 11, 2013 | Sheet 30 of 56



PCH Power Rail Table
Refer to PCH EDS R1.0

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	N/A
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccCLKDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

+3VALW to +3VALW_PCH



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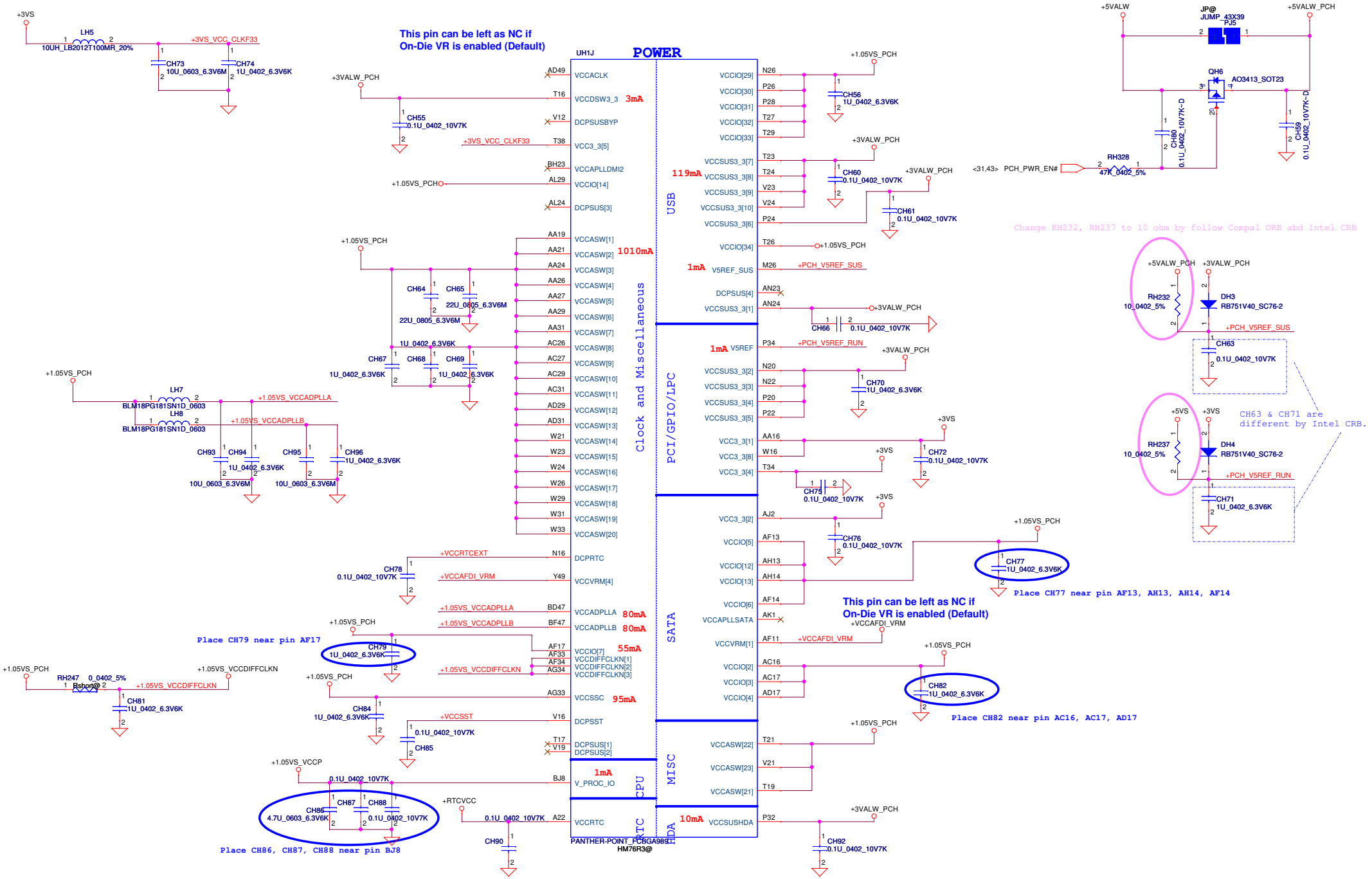
Compal Electronics, Inc.

Title: ***PCH_POWER-1***

Size: Custom | Document Number: **VFKAA** | Rev: 0.2

Date: Monday, March 11, 2013 | Sheet 31 of 56



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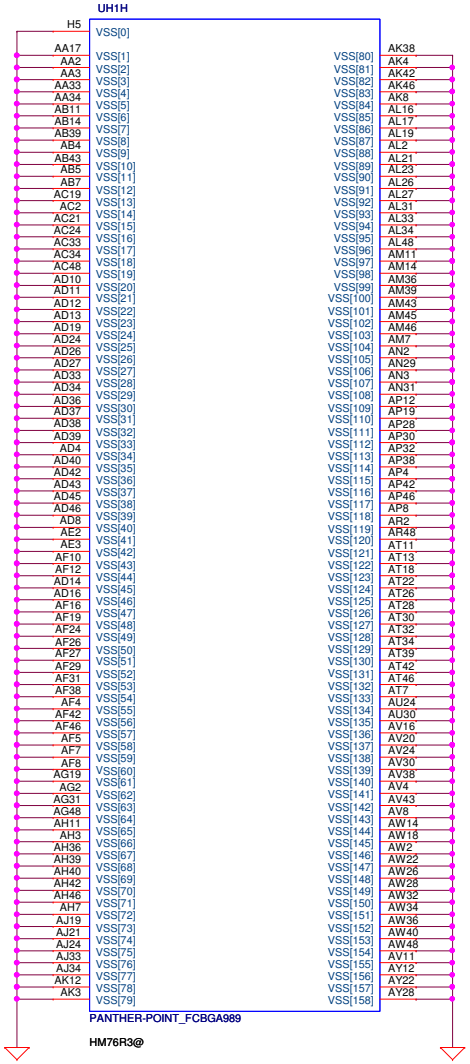
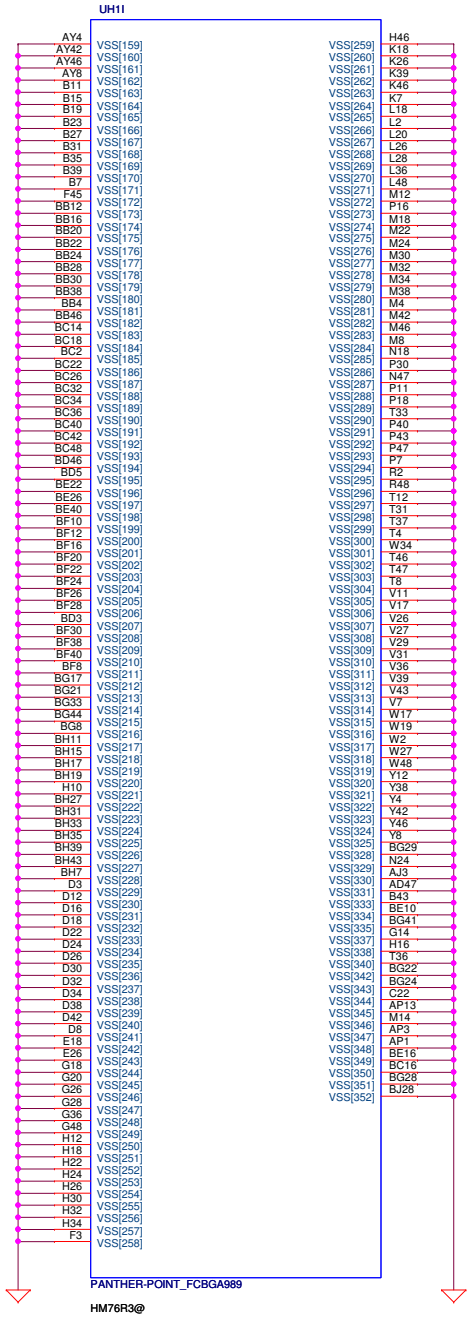
				Date: Monday, March 11, 2013; Sheet 32 of 56





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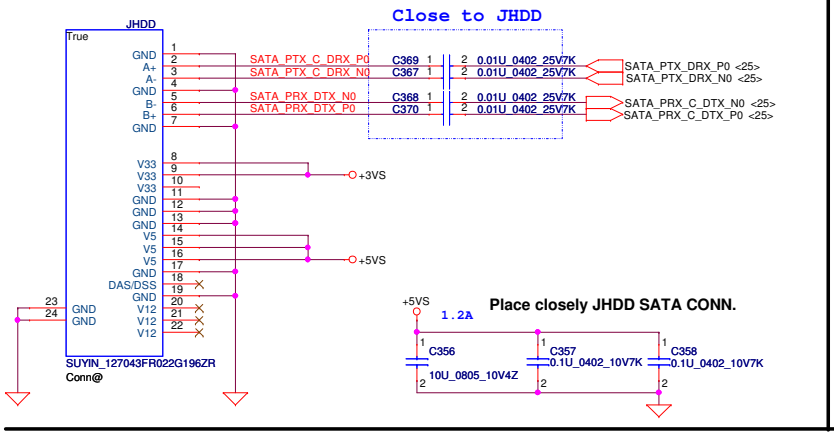
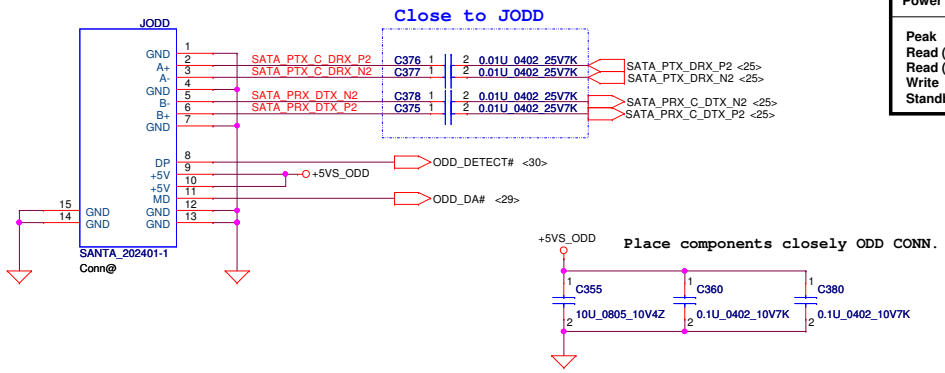
				Date: Monday, March 11, 2013; Sheet 33 of 56

SATA HDD Conn.

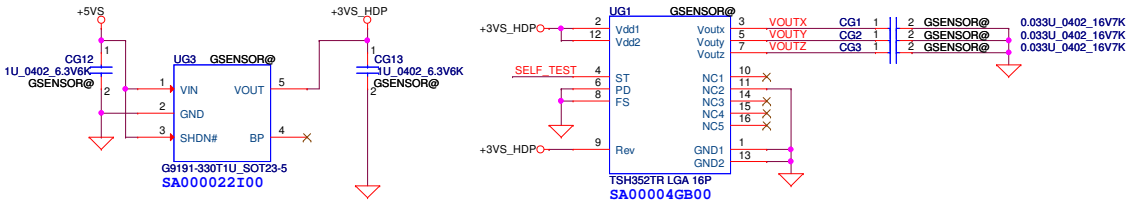


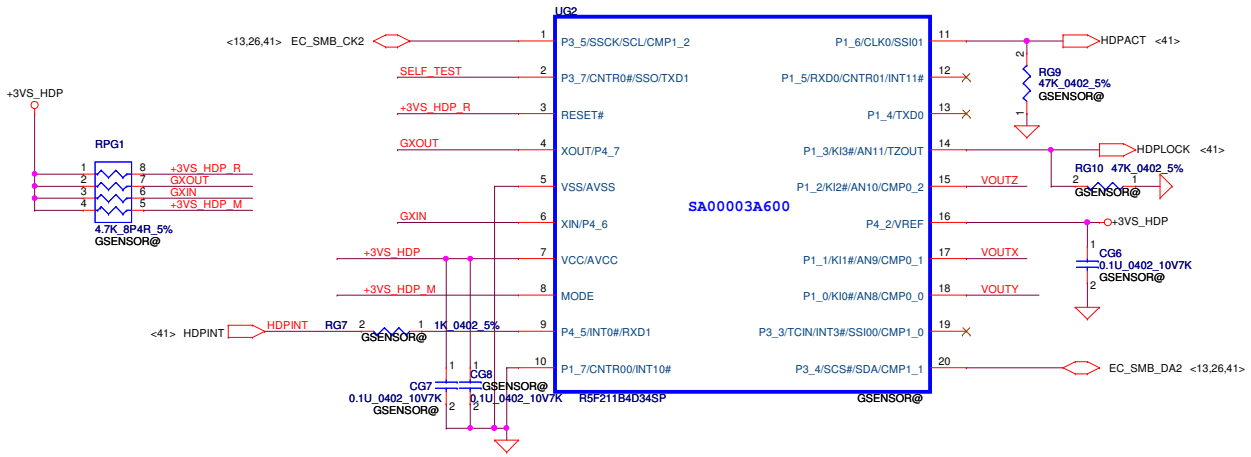
SATA ODD Conn



Power Consumption	
Peak	1800 mA
Read (CD)	1100 mA
Read (DVD)	950 mA
Write	1300 mA
Standby	20mA

G-Sensor





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Issued Date	2012/12/07	Deciphered Date	2013/12/07

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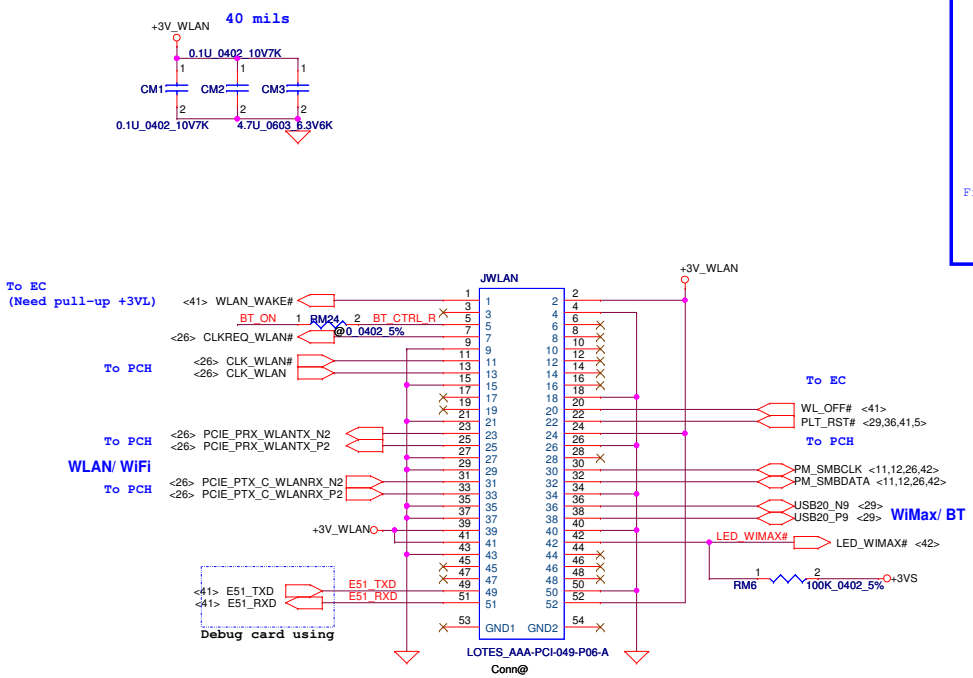
Compal Electronics, Inc.

Title: HDD/ODD/G-Sensor

Size | Document Number: VFKAA | Rev: 0.2

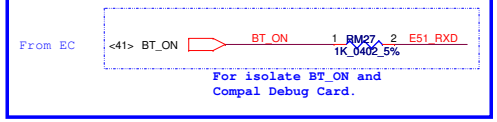
Date: Monday, March 11, 2013 | Sheet 34 of 56

Slot 1 Half PCIe Mini Card-WLAN

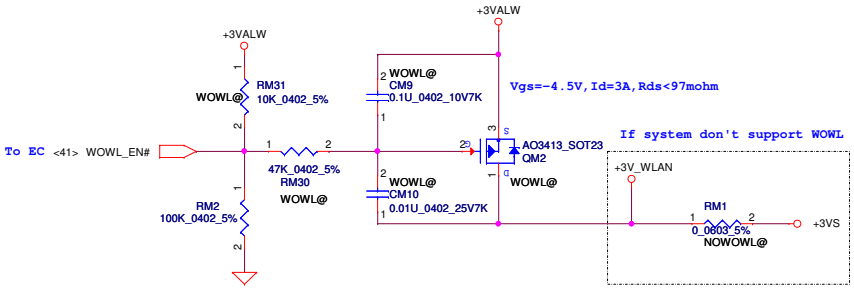


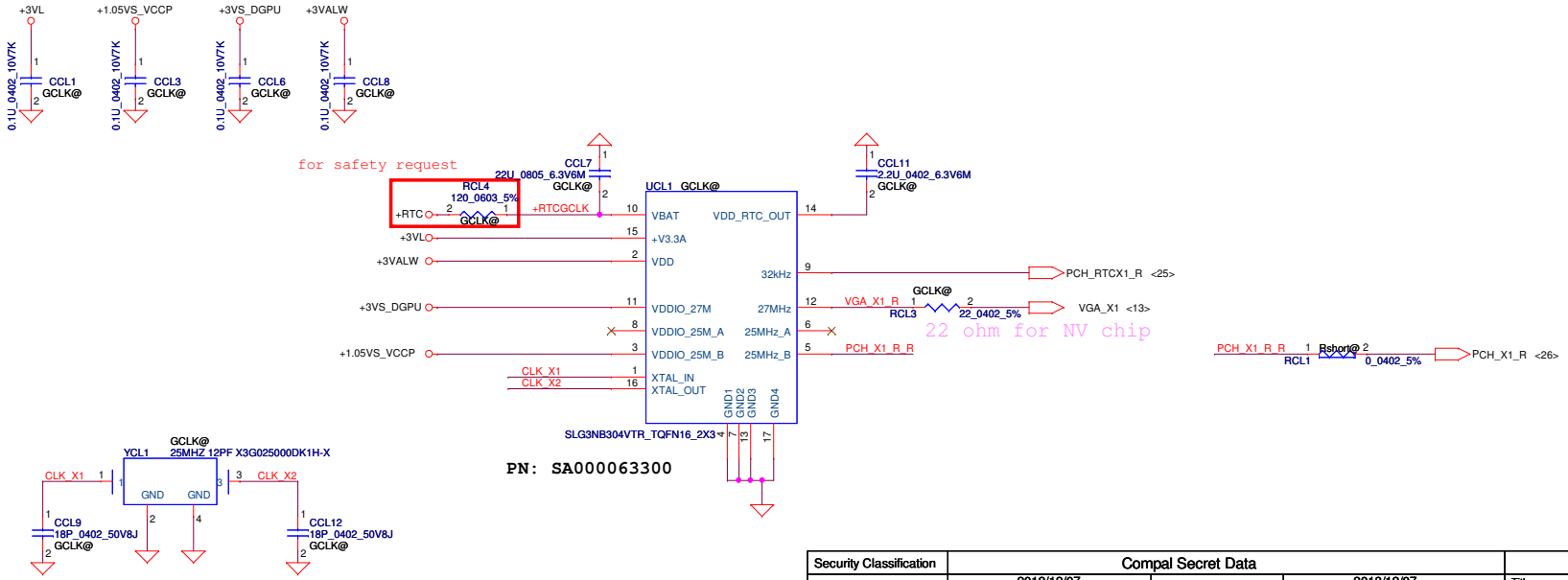
WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_ON	H	L



+3VALW TO +3V_WLAN for WOWL





PN: SA000063300

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Issued Date	2012/12/07	Deciphered Date	2013/12/07

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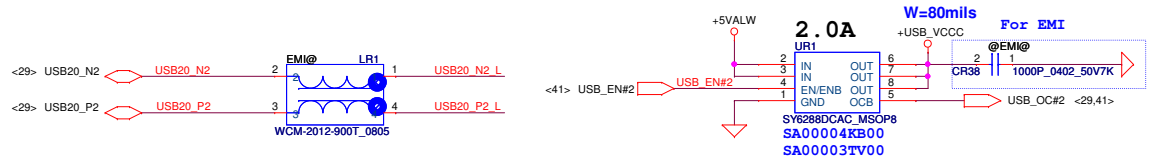
Compal Electronics, Inc.

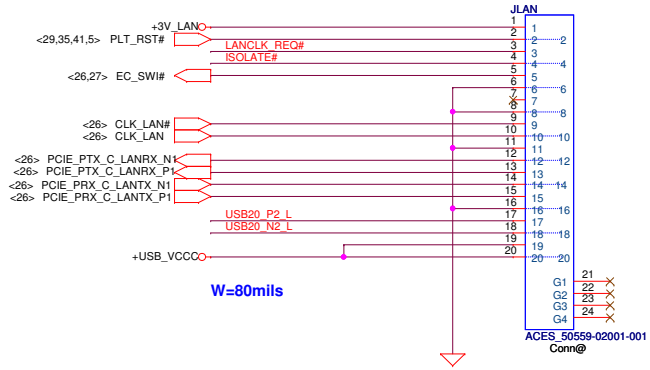
Title: WLAN/GCLK

Size: D25 | Document Number: VFKAA | Rev: 0.2

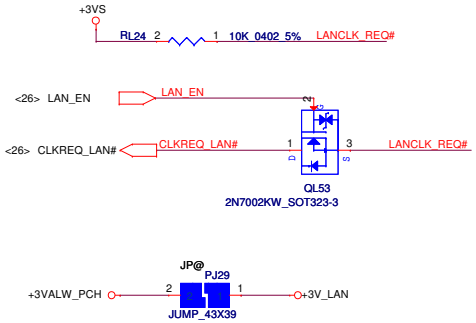
Date: Monday, March 11, 2013 | Sheet 35 of 56

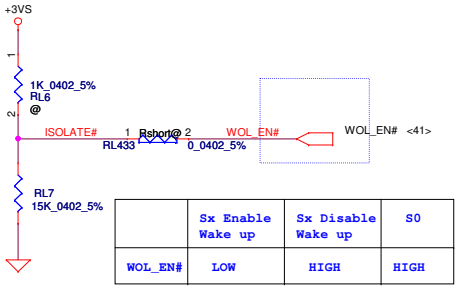
Left USB 2.0 x 1





For LAN function





	Sx Enable Wake up	Sx Disable Wake up	S0
WOL_EN#	LOW	HIGH	HIGH

+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

LAN	WOL	LAN_EN S0	LAN_EN Sx	ISOLATEB S0	ISOLATEB Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

*
S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/12/07	Deciphered Date 2013/12/07	Title: LUSB20/LAN conn.
			Size: Custom; Document Number: VFKAA; Rev: 0.2
			Date: Monday, March 11, 2013; Sheet 36 of 56

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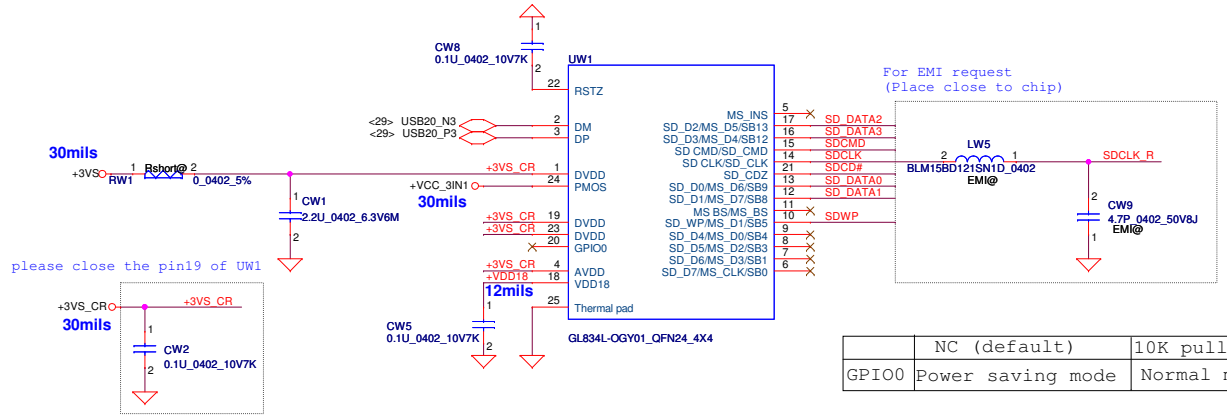
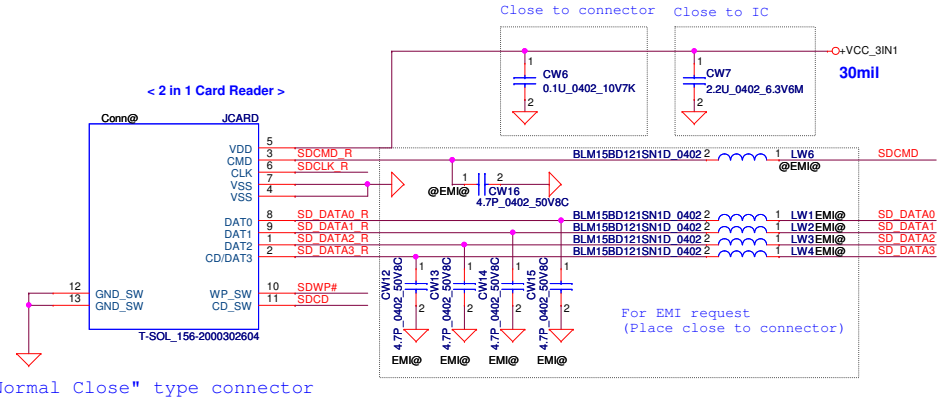


	NC (default)	10K pull down
GPIO0	Power saving mode	Normal mode

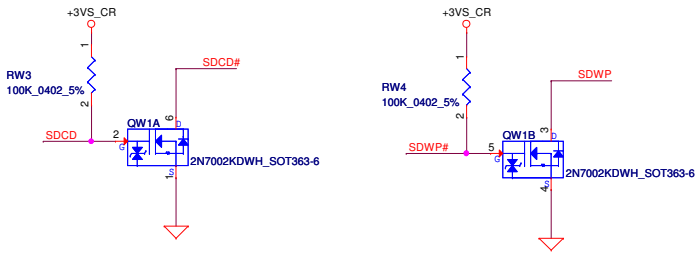
De-coupling and Bulk capacitor should place near to Cardreader chip and Combo Socket



"Normal Close" type connector

	CD_SW	WP_SW	
		Protect disable	Protect Enable
Card Uninsertion	Close	Close	Close
Card Insertion	Open	Open	Close

For normal close type connector invert circuit



Security Classification	Compal Secret Data		
Issued Date	2012/12/07	Deciphered Date	2013/12/07

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Compal Electronics, Inc.

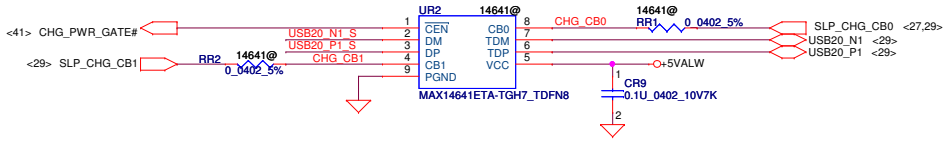
Title: **USB-CardReader GL834L**

Size: Custom | Document Number: **VFKAA** | Rev: 0.2

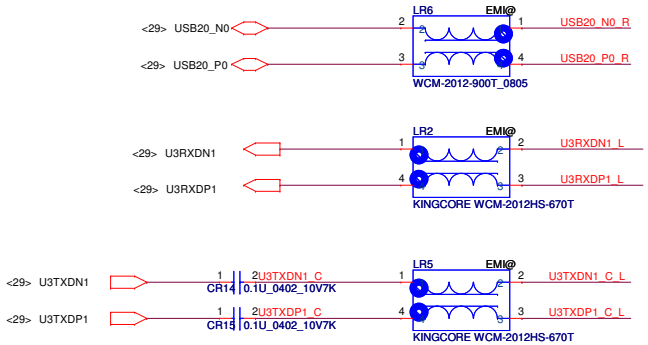
Date: Monday, March 11, 2013 | Sheet 37 of 56

USB Sleep & Charge

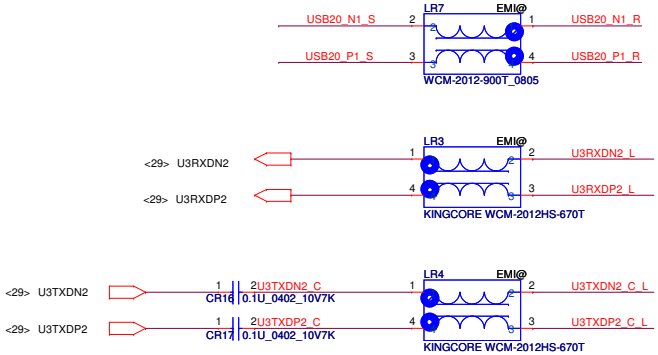
State table for MAX14641			
CB0	CB1	Mode	STATUS
0	0	AM2	2A auto-detection charger mode for Apple device. Resistor dividers are connected to DP/DM. Including DCP
0	1	AP1	Forced 1A charger mode for Apple devices. Resistor dividers are connected to DP/DM.
1	0	PM	USB pass-through mode.DP/DM are connected to TDP/TDM
1	1	CM	USB pass-through mode with CDP emulation. Auto connects DP/DM to TDP/TDM depending on CDP detection status.

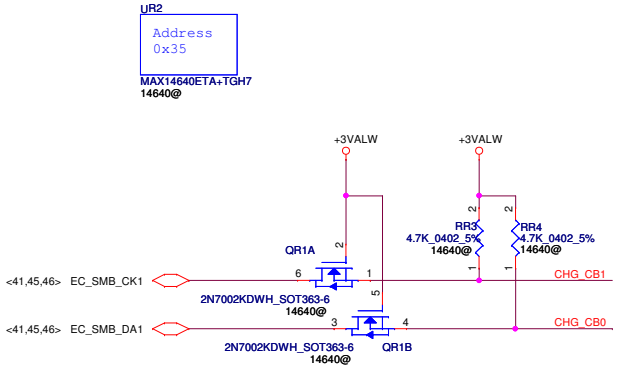


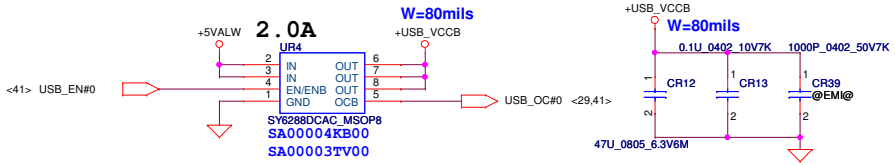
Right rear USB3.0 Conn.

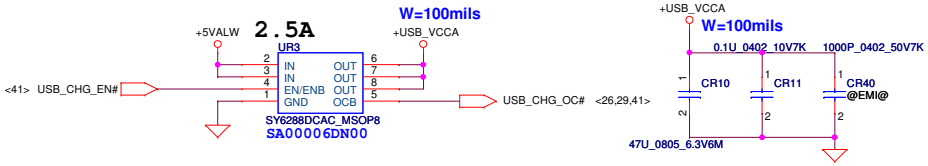


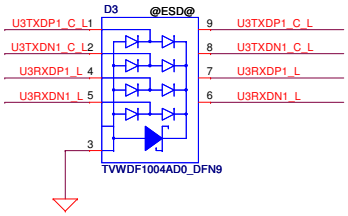
Right front USB3.0 Conn.
(Support S&C function)

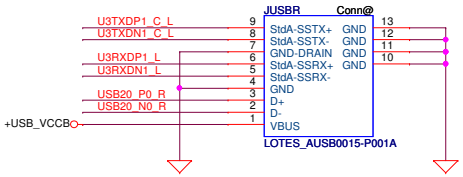


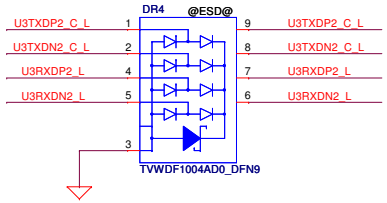


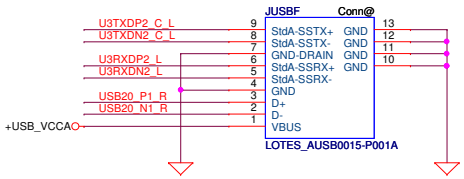












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Compal Electronics, Inc.

Title: **RUSB30/S&C**

Size: Custom | Document Number: **VFKAA** | Rev: 0.2

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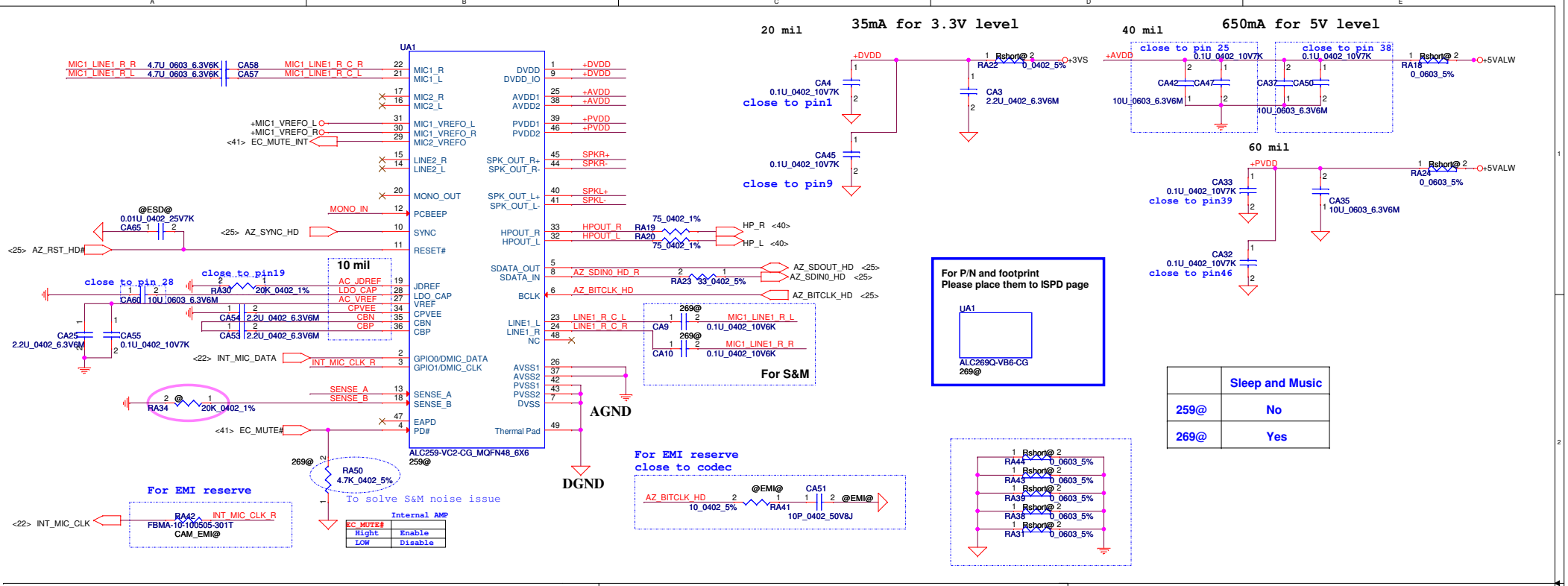
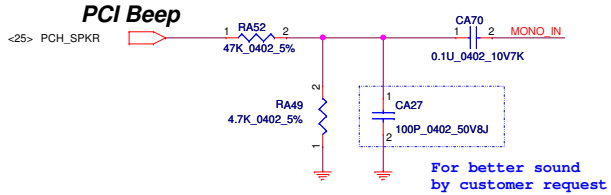
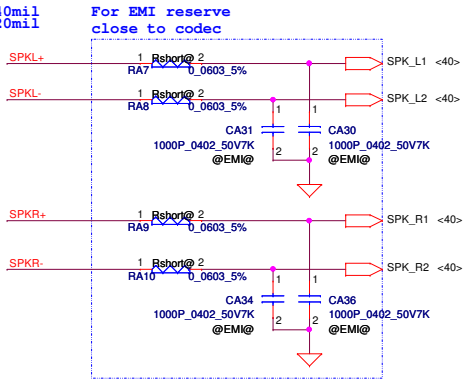


	Sleep and Music
259@	No
269@	Yes

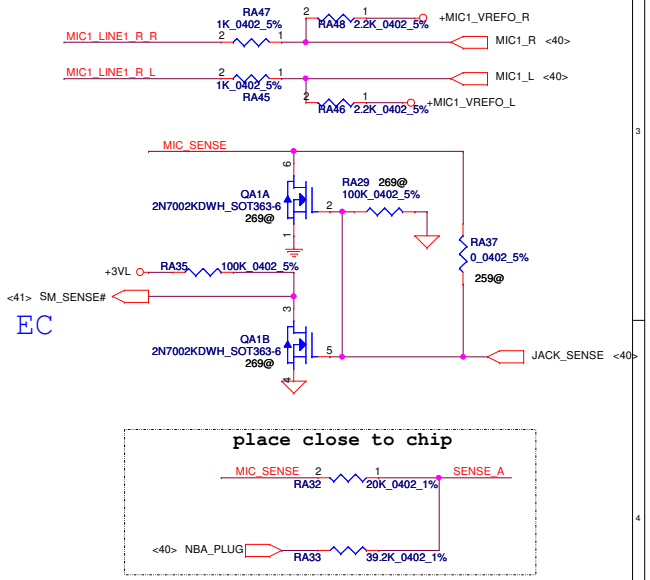
Beep sound



SPK



MIC/LINE IN



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

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Compal Electronics, Inc.

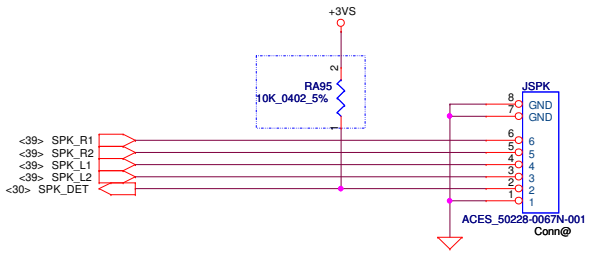
Title: ***HDA-ALC259-VC/269-VB***

Size: Custom | Document Number | Rev

Date: Monday, March 11, 2013 | Sheet 39 of 56

SPK Conn.

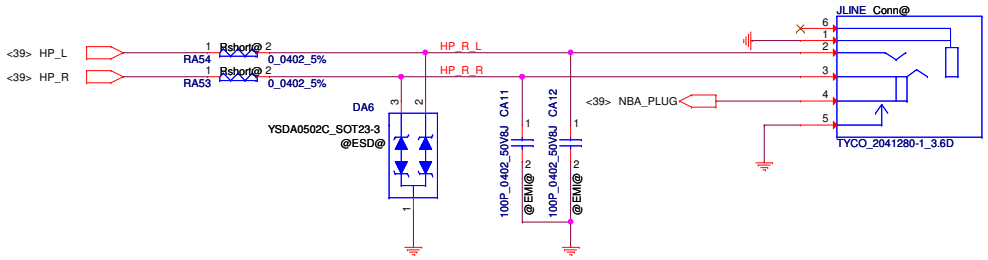
For common design,
pull-high resistor should be placed at connector side.



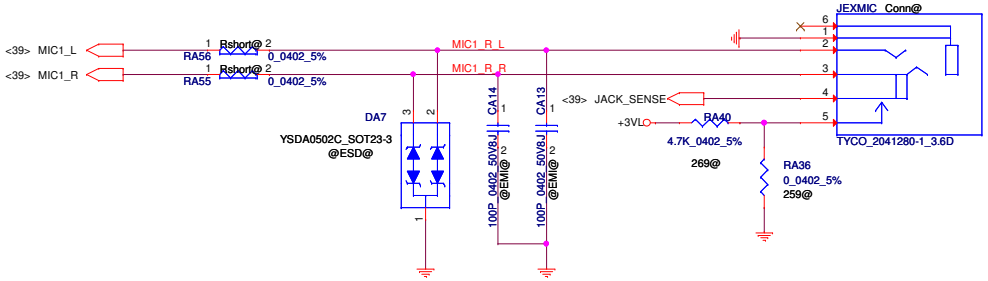
SM_DET (GPIO48)	BIOS setup	Speaker Type	BOM
1	S&M option	Harman/Kardon	269@
0		Non Harman	259@

Non-Harman detection		
SPK_DET (GPIO70)	0	ONKYO
	1	Non-Brand

HeadPhone/LINE Out JACK



MIC/LINE IN JACK



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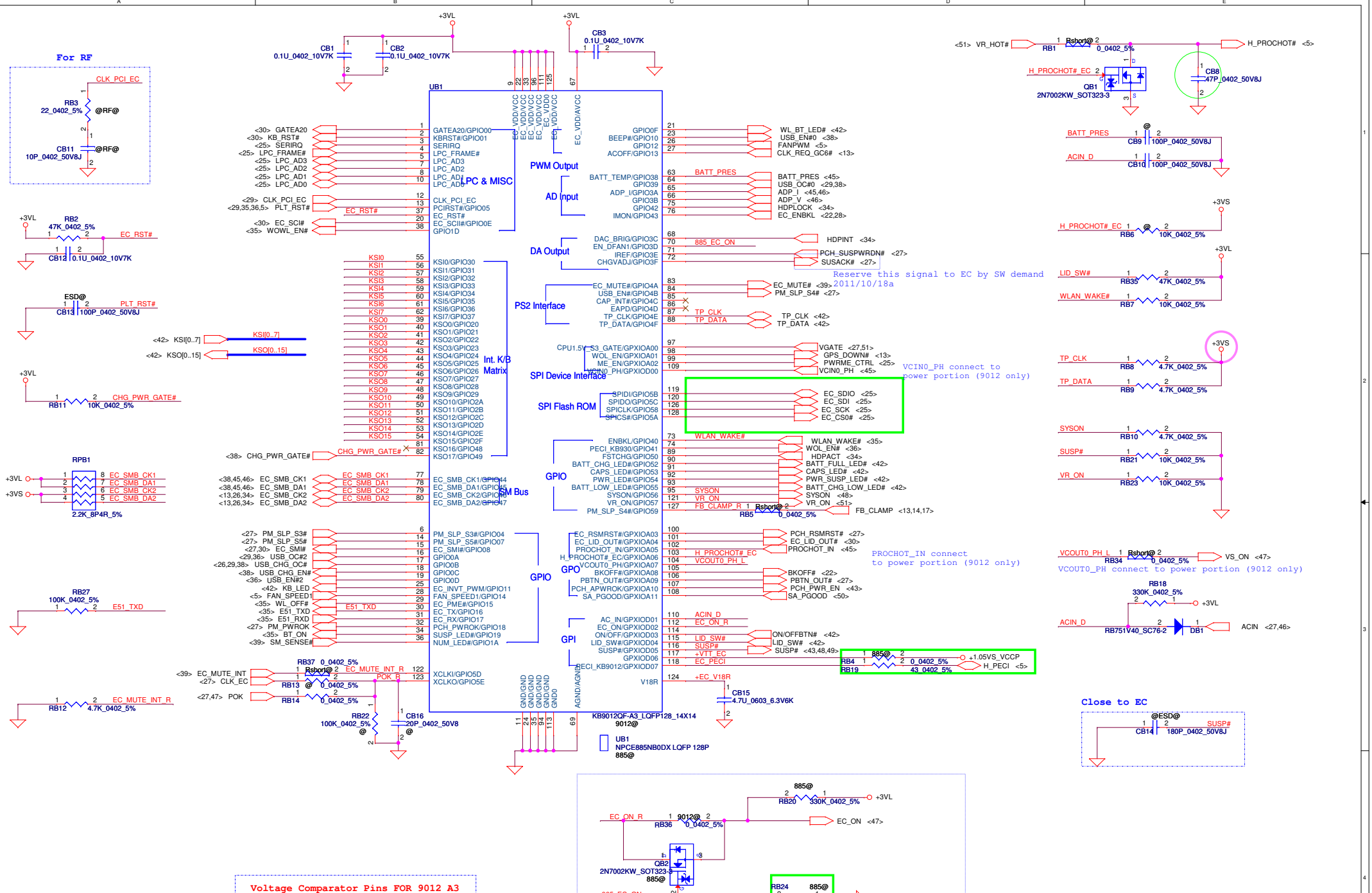
Compal Electronics, Inc.

Title: AUDIO CONN

Size | Document Number | Rev 0.2

Date: Monday, March 11, 2013 | Sheet 40 of 56



Voltage Comparator Pins FOR 9012 A3

VCIN0 pin109 VCIN1 pin102	>1.2V	<1.2V
VCOUT0 pin104	HIGH (default)	LOW
VCOUT1 pin103	HIGH	LOW (default)

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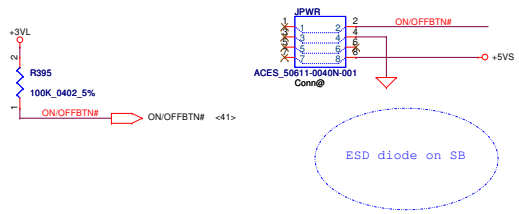
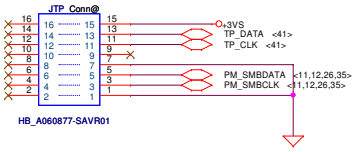
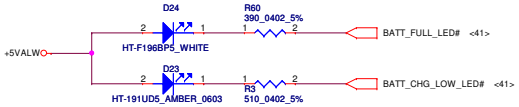
Power Button Conn.



Touchpad Connector

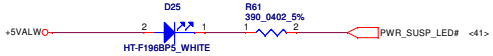


BATT CHARGE /FULL LED



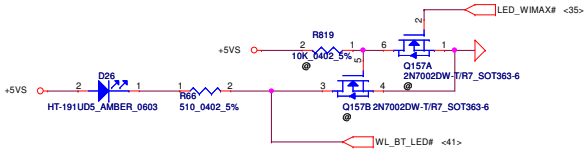
White LED bright when both AC-adaptor is plugged in and Battery is full charged
Amber LED bright while charging battery from AC-adaptor.
Amber LED blink during Critical Low Battery

POWER LED



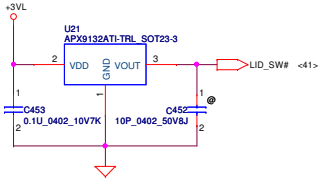
White LED bright when system is power on.
White LED blink when system is sleep mode.

WLAN/WiMAX LED

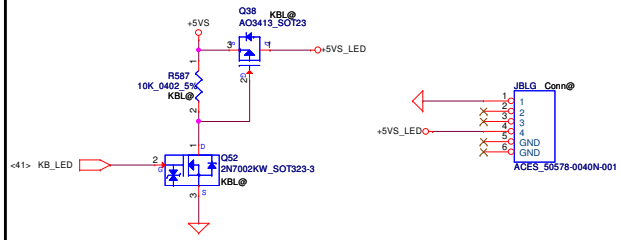


Amber LED bright while Wireless and/or WiMAX turns on.

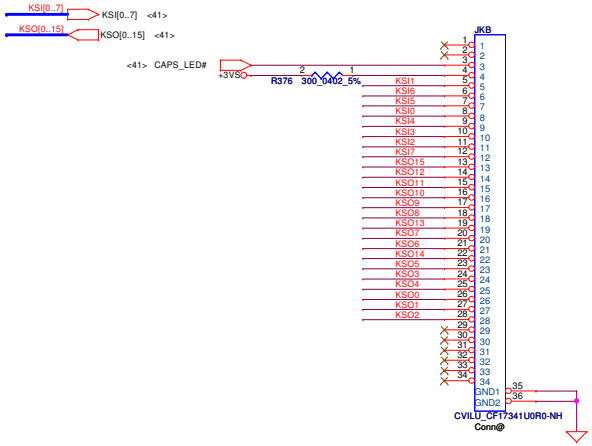
Lid SW



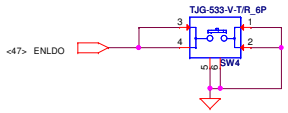
Keyboard LED



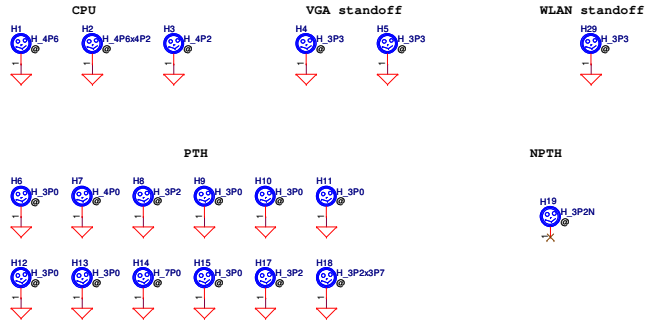
KEYBOARD CONN.



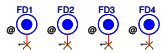
EC Reset



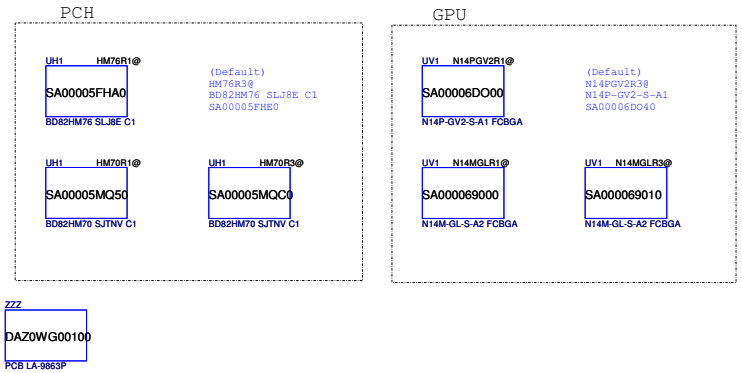
Screw Hole



PCB Fedical Mark PAD



ISPD



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Compal Electronics, Inc.

Title: TP/ISPD/KB/LED/Screw

Size: | Document Number: VFKAA | Rev: 0.2

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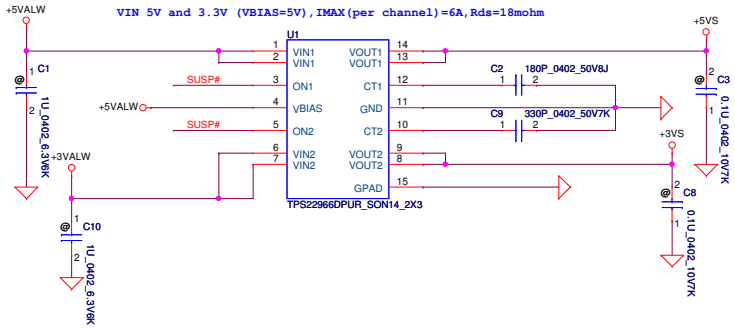
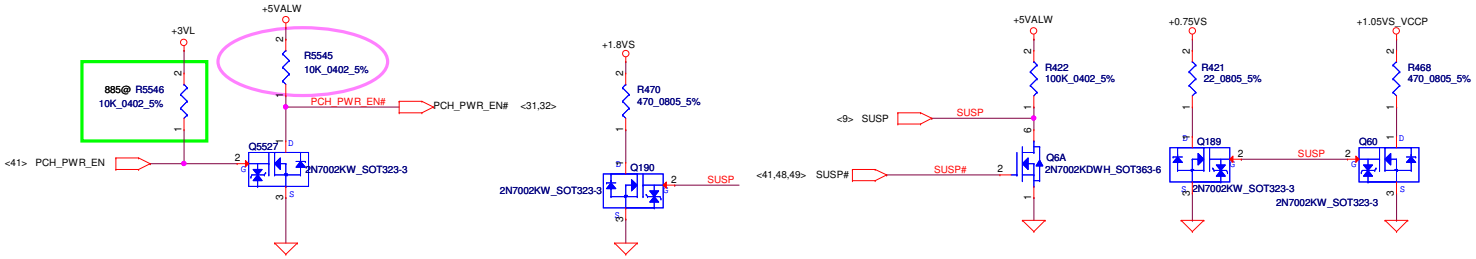
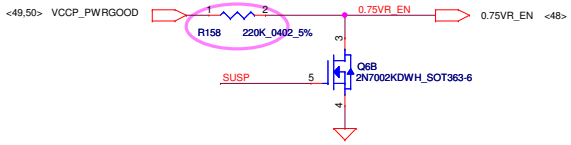
+5VALW TO +5VS
+3VALW TO +3VS
Load switch

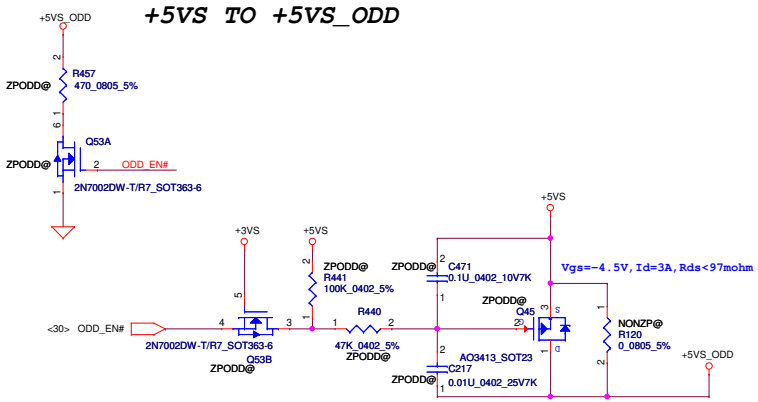




For S3 CPU Power Saving



+5VS TO +5VS_ODD



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/12/07	Deciphered Date	2013/12/07	Title: DC-DC INTERFACE
Size	Document Number: VFKAA			Rev: 0.2
Date: Monday, March 11, 2013	Sheet 43 of 56			

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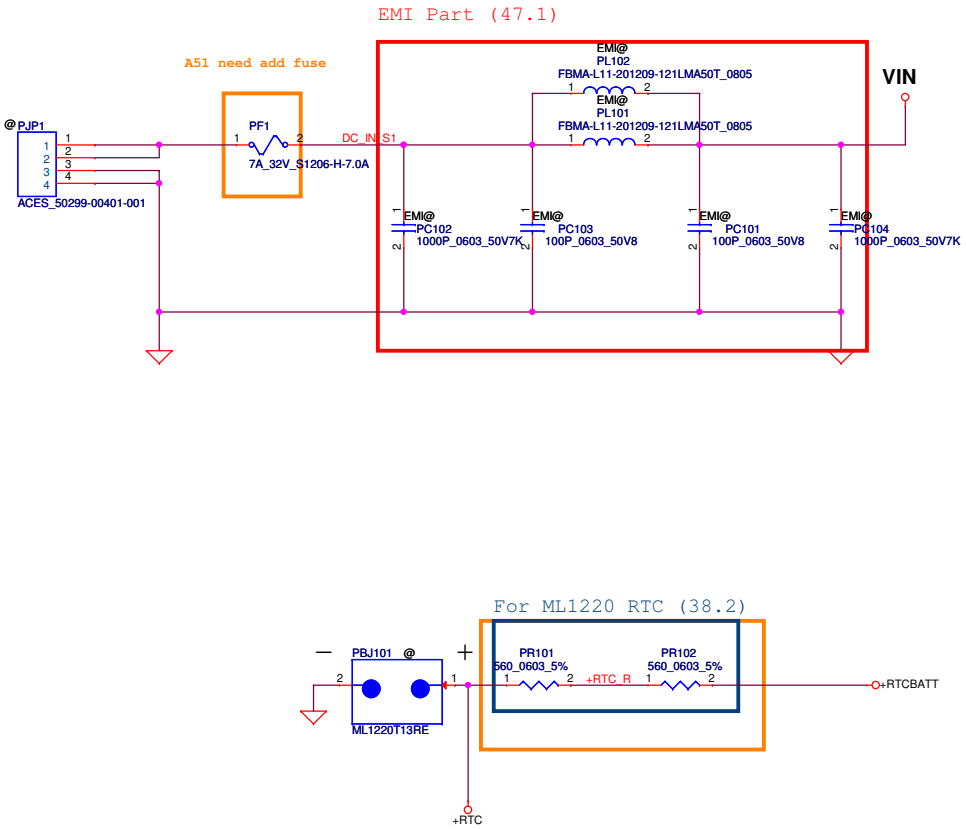

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/09/24	Deciphered Date	2013/09/24	Title: DCIN/PRECHARGE
				Size: Custom; Document Number: VFKAA; Rev: 0.1
				Date: ; Sheet 44 of 55

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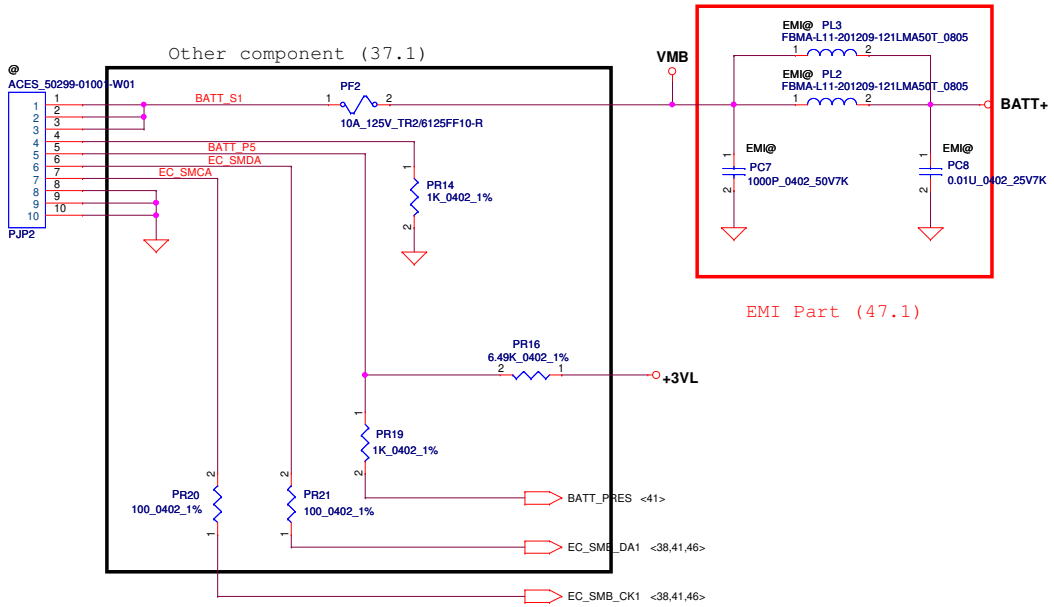

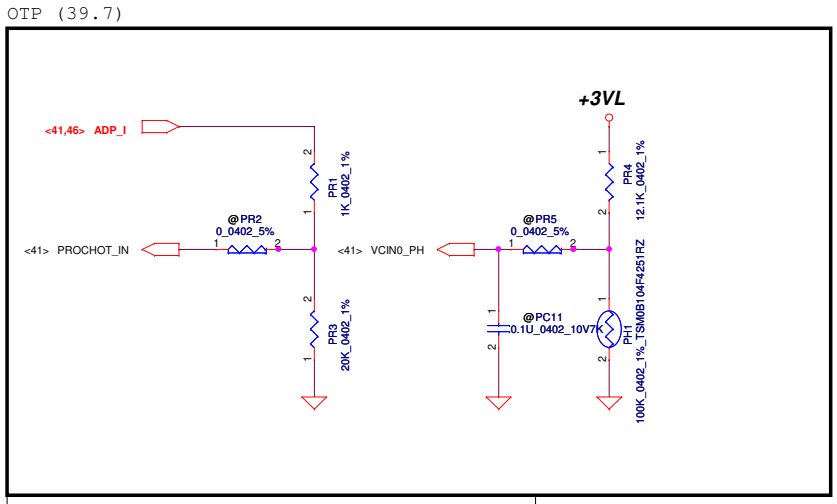

PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

	Initial	Protect	Recovery
65W	0.75V	0.752V	0.626V
75W	0.9V	0.902V	0.722V

	Initial	Protect	Recovery
CPU OTP	65W	93 C	56 C

Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

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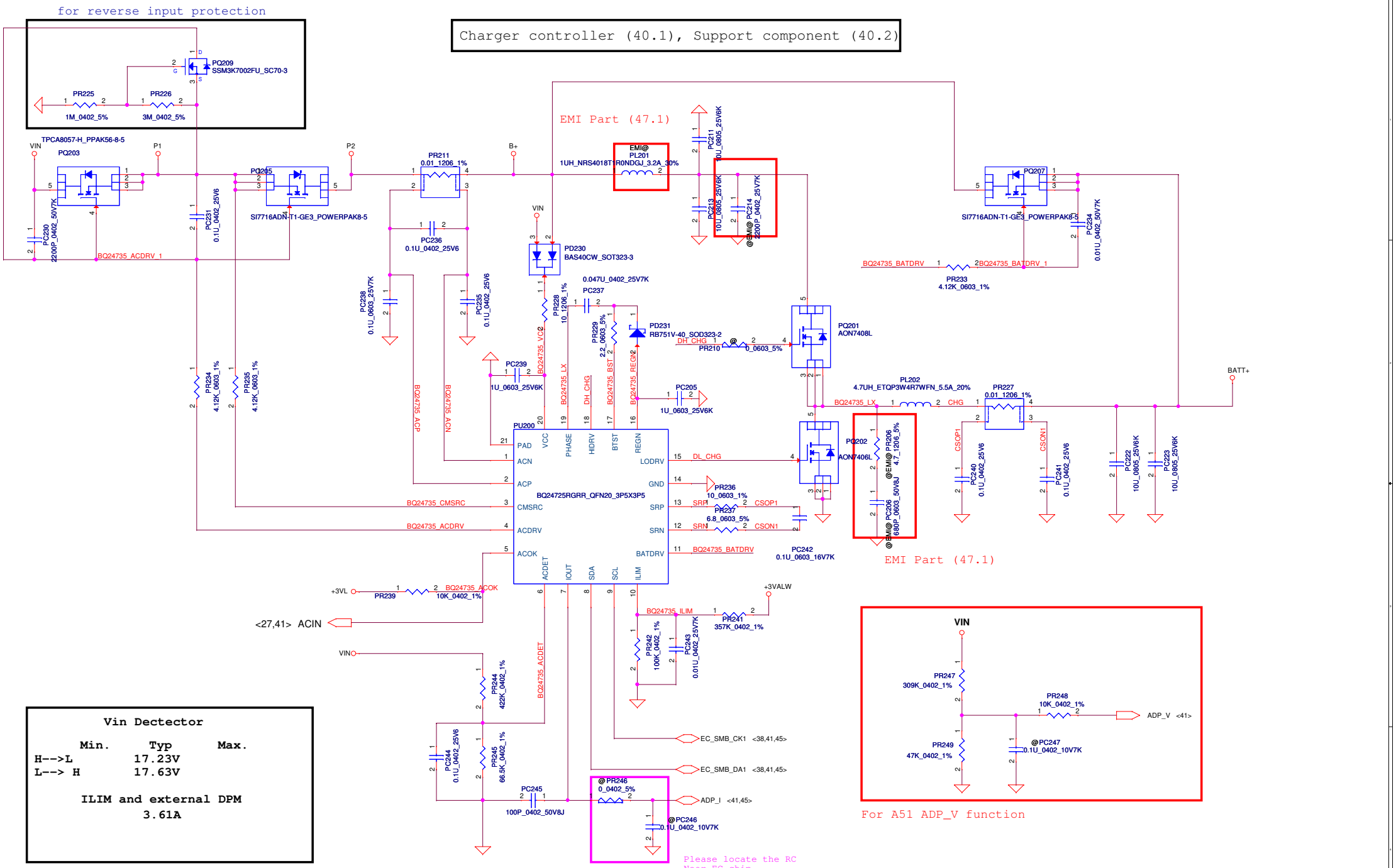
Compal Electronics, Inc.

Title: ***BATTERY CONN / OTP***

Size: Custom | Document Number: *VFKAA* | Rev: 0.1

Date: | Sheet 45 of 55



Vin Dectector

	Min.	Typ	Max.
H-->L		17.23V	
L--> H		17.63V	

ILIM and external DPM
3.61A

Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

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Compal Electronics, Inc.

Title: *CHARGER*

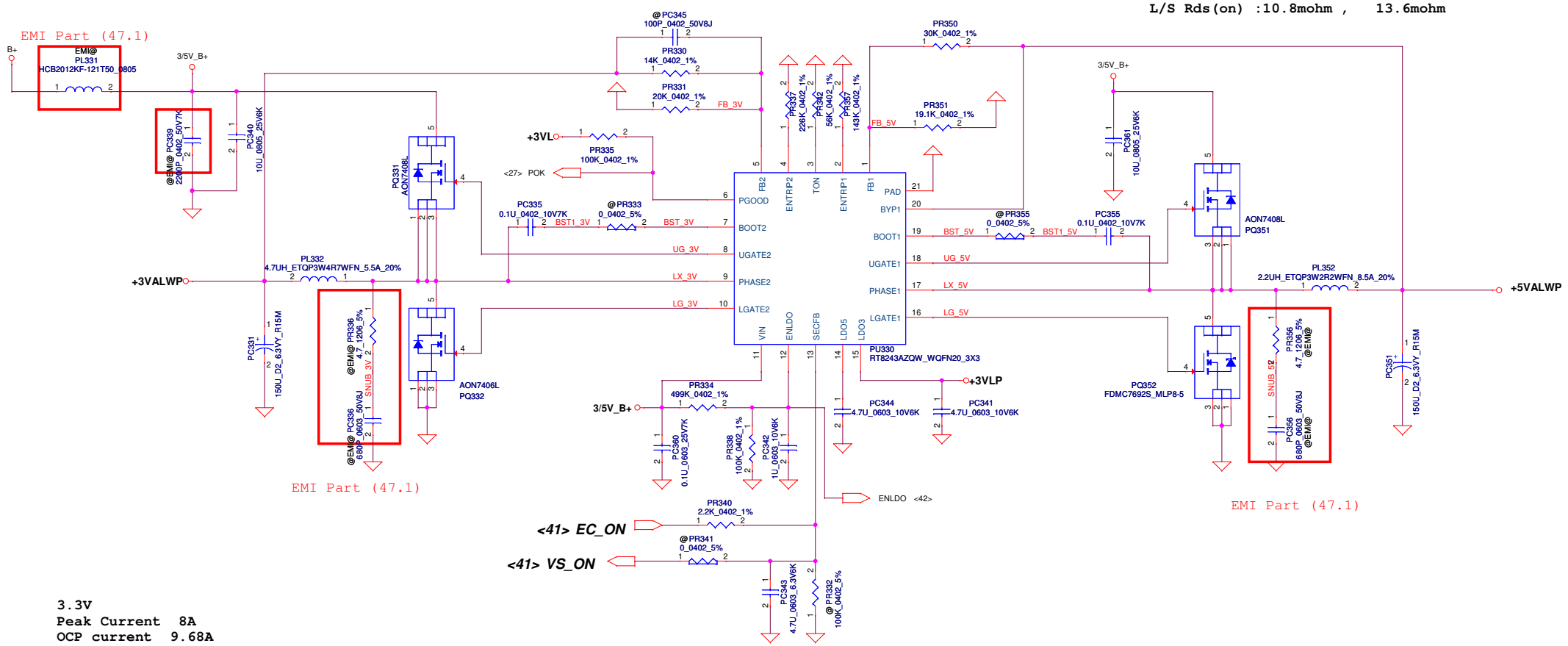
Size: Custom | Document Number: VFKAA | Rev: 0.1

Date: | Sheet 46 of 56

3/5VALW controller (35.1), Support component (35.2)

5V
Peak Current 10A
OCP current 12.03A
FSW=390kHz
Delta I=4.29A,ripple=4.29*17m=72.93mV
DCR 15.5mohm+/-15%
ESR 17mohm

	TYP	MAX
H/S Rds(on)	:27mohm ,	34mohm
L/S Rds(on)	:10.8mohm ,	13.6mohm



3.3V
Peak Current 8A
OCP current 9.68A
Delta I=1.28A ,ripple=1.28x15m=19.2mV
FSW=455kHz
DCR 35mohm +/-15%
ESR 15mohm

	TYP	MAX
H/S Rds(on)	:27mohm ,	34mohm
L/S Rds(on)	:19mohm ,	23.5mohm

Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

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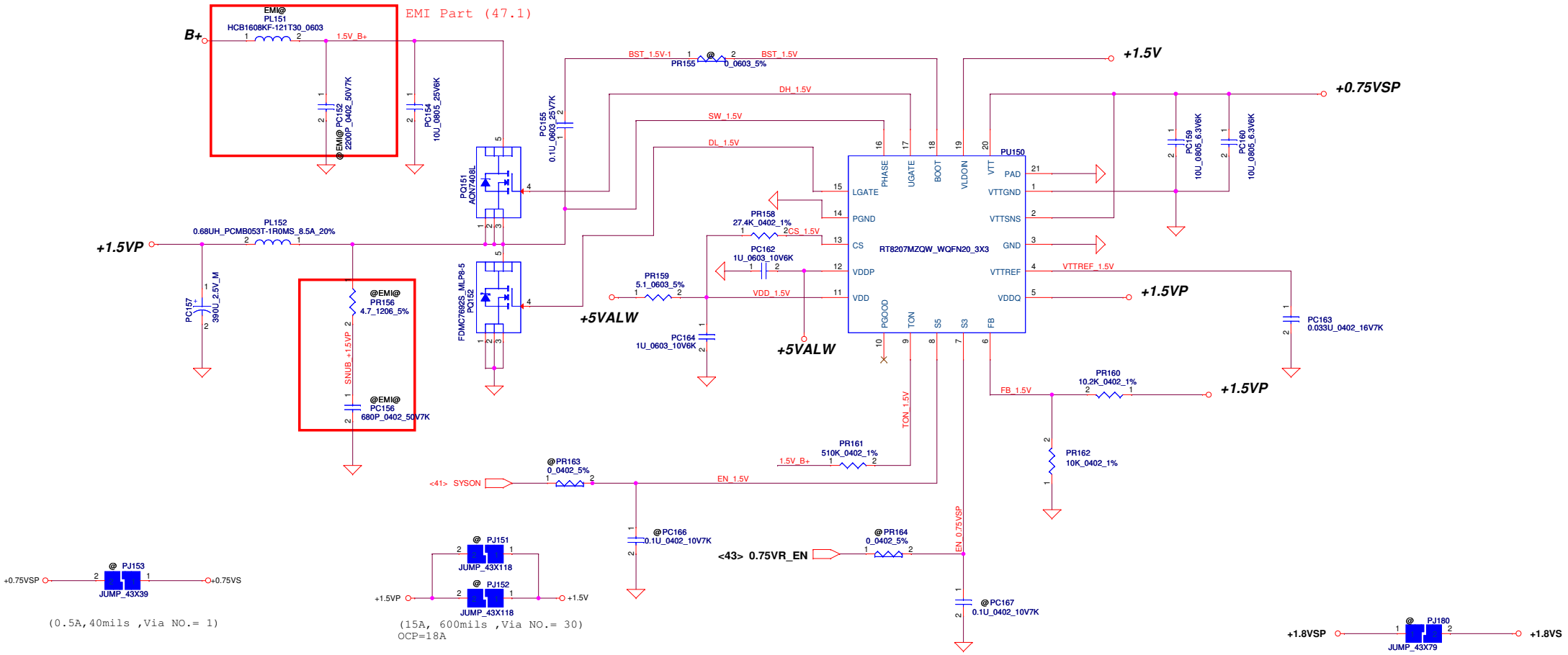
Compal Electronics, Inc.

Title: *3VALW/5VALW*

Size: Custom | Document Number: VFKAA | Rev: 0.1

Date: | Sheet 47 of 56

DDR controller (35.3), Support component (35.4)



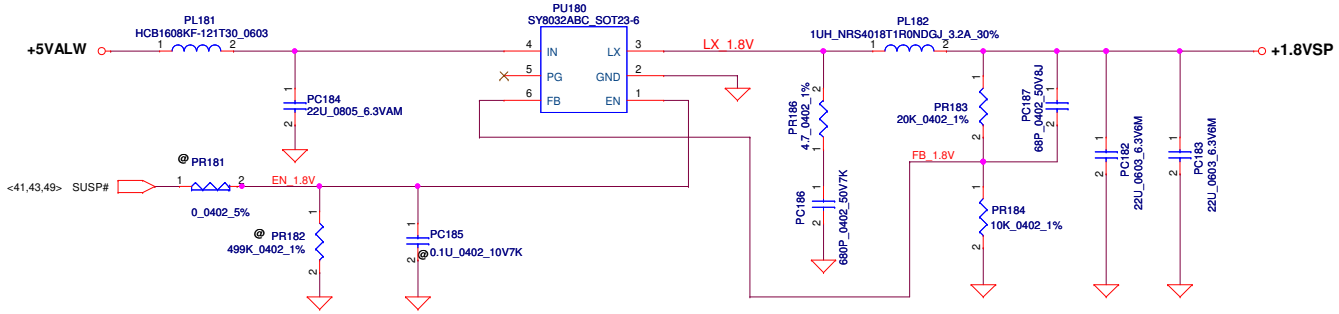
1.5V
Peak Current 16.8A
OCP current 20 A
FSW=495kHz
DCR 13mohm
ESR 9mohm

	TYP	MAX
H/S Rds(on)	:27mohm ,	34mohm
L/S Rds(on)	:10.8mohm ,	13.6mohm

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

1.8VS controller (35.15), Support component (35.16)



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Issued Date	2012/09/24	Deciphered Date	2013/09/24

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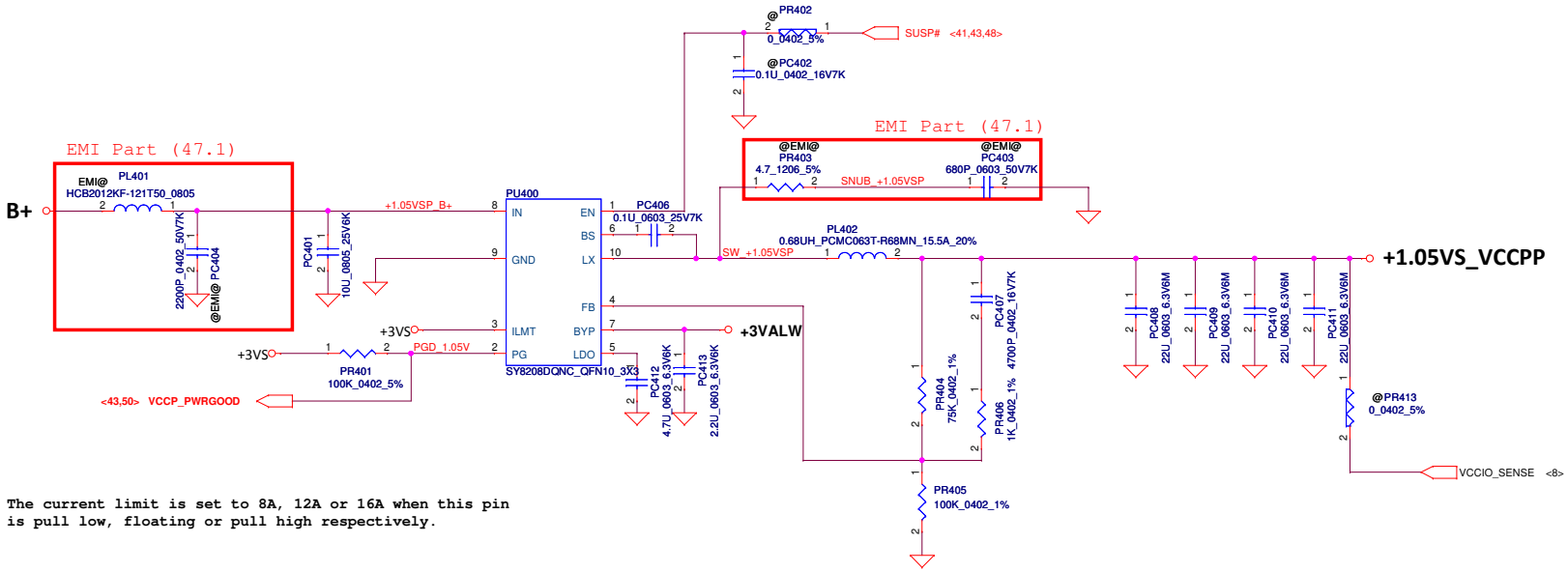
Compal Electronics, Inc.

Title: 1.5VP/0.75VSP/1.8VSP

Size: Custom | Document Number: VFKAA | Rev: 0.1

Date: | Sheet 48 of 56

1.05VCCP controller (35.5), Support component (35.6)



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high respectively.

(17A,680mils ,Via NO.=34)
OCP=23.91A

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/09/24	Deciphered Date	2013/09/24	Title: +1.05VS_VCCP
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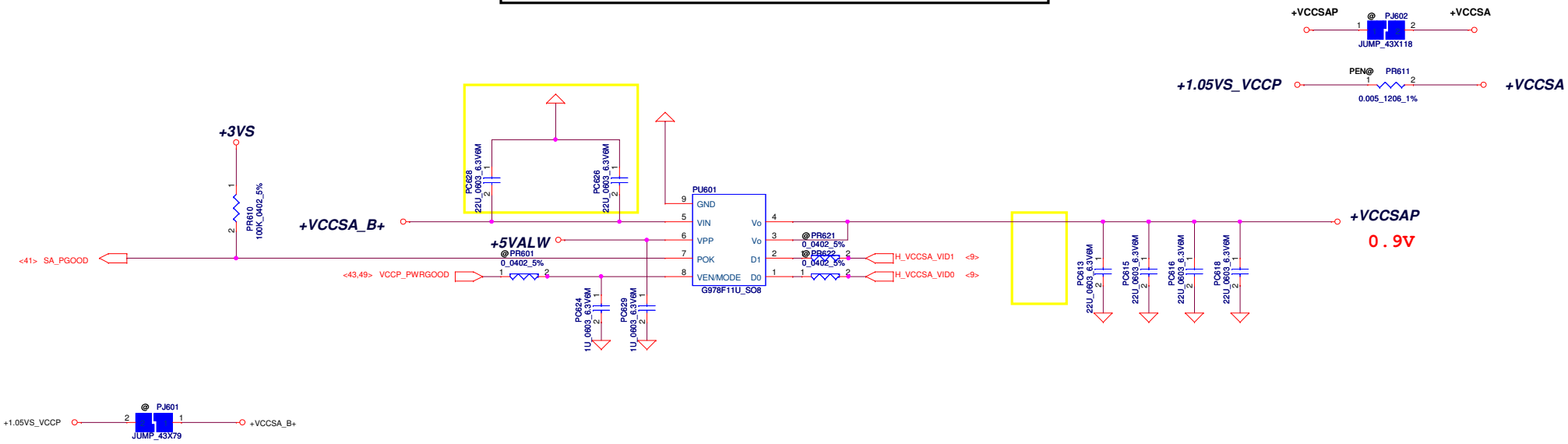
				Date: Monday, March 11, 2013 / Sheet 49 of 56

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

VCCSA controller (35.17), Support component (35.18)



(6A, 240mils ,Via NO.= 6)

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Issued Date	2012/09/24	Deciphered Date	2013/09/24

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Compal Electronics, Inc.

Title: *VCC_SAP*

Size: Custom | Document Number: *VFKAA* | Rev: 0.1

Date: | Sheet 50 of 56

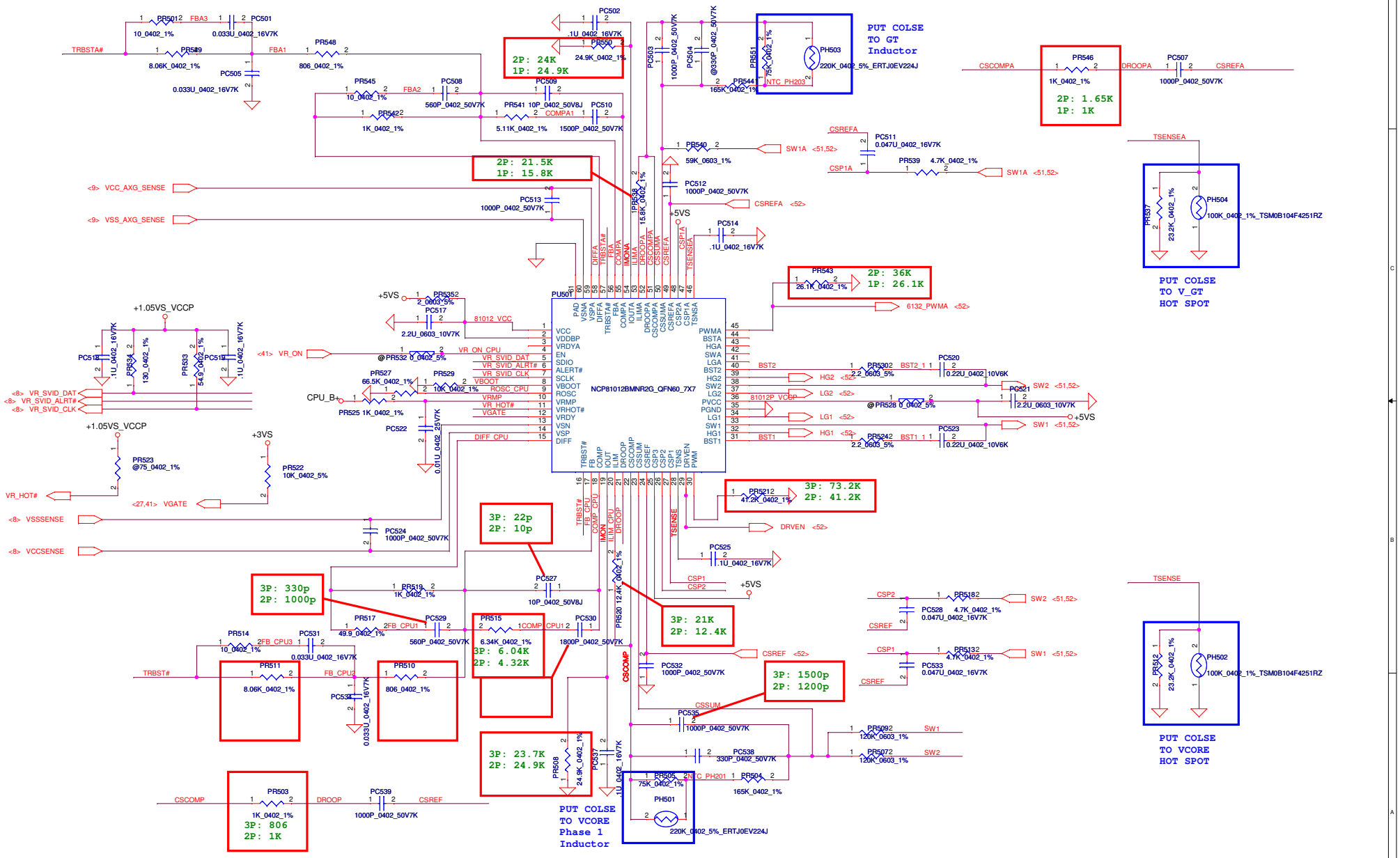
CSP1A, CSP2A to +5VS.

LGA, SWA, HGA, BSTA, DIFFA, TRBSTA#, ILIMA, PWMA are float.

VSPA, VSNA to GND (HW side).
CSREFA, TSNSA, IOUTA to GND.

FBA and COMPA are short.
CSCOMPA, CSSUMA, DROOPA are short.

DIS only:
All AXG components are @.
Except
PR272 and PR273 are 0ohm.
PC223, PC226, PR202 are 0ohm.
PC220, PC215, PR206 are 0ohm.



Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

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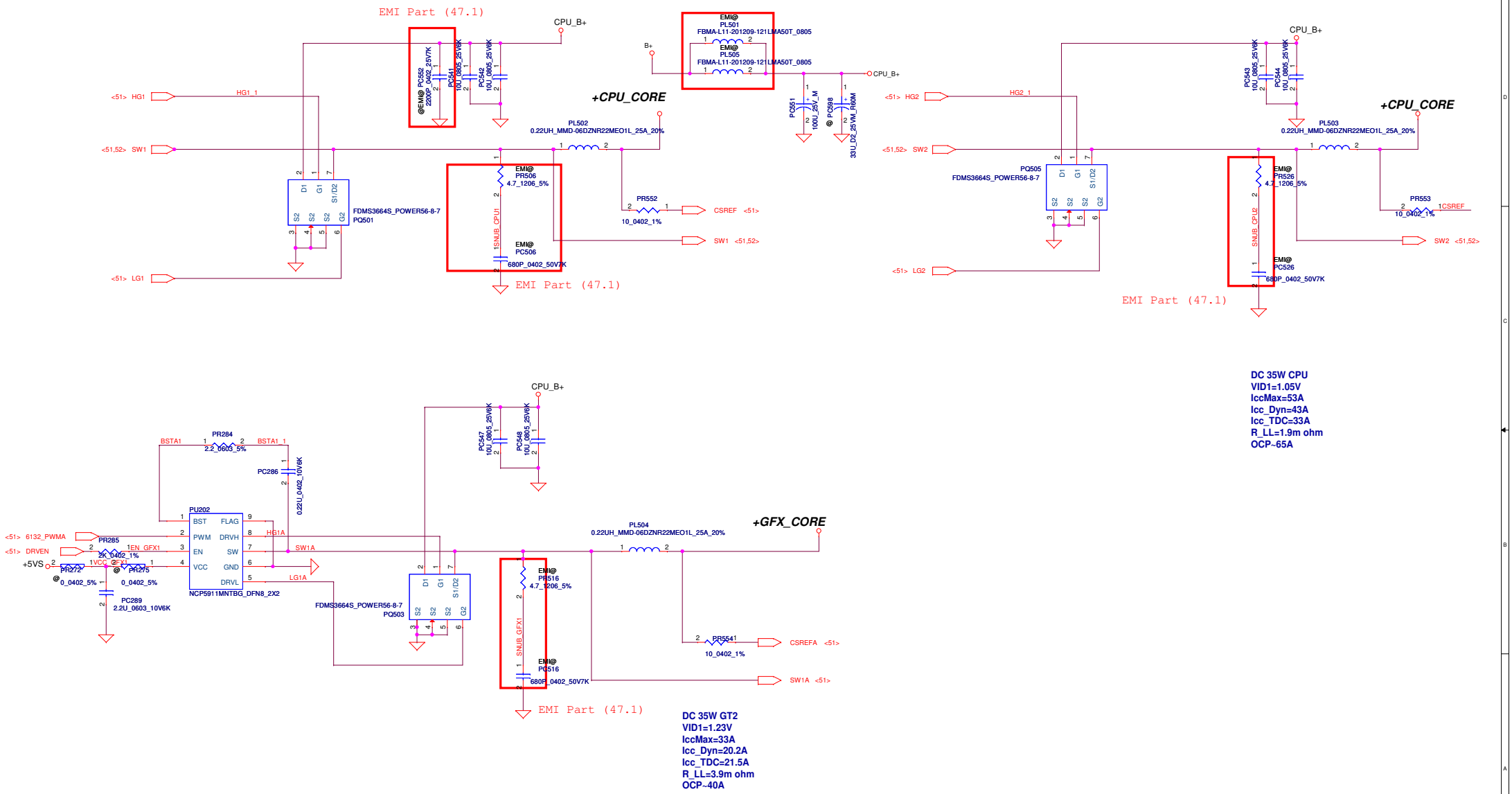
Compal Electronics, Inc.

Title: PWR-CPU_CORE

Size: Custom | Document Number: VFKAA | Rev: 0.1

Date: | Sheet 51 of 56



Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

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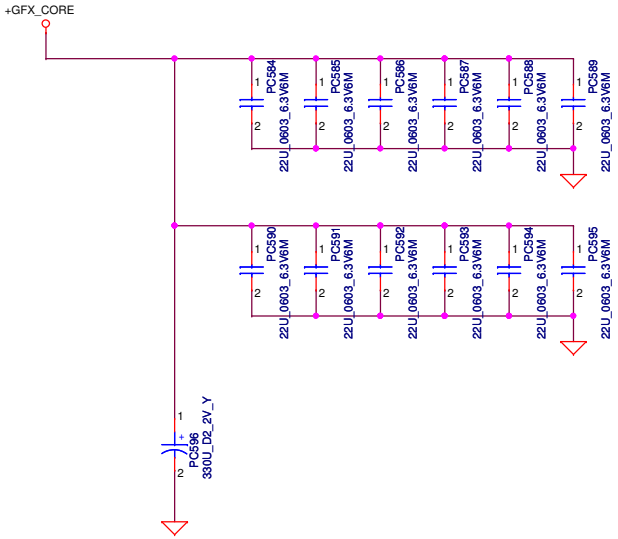
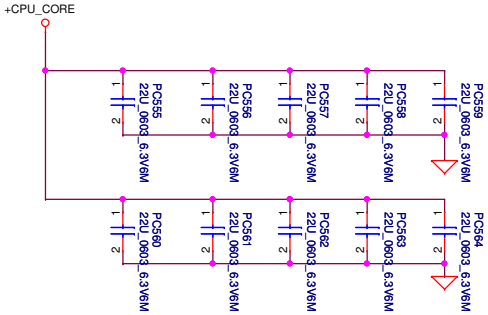
Title: **PWR-CPU_CORE**

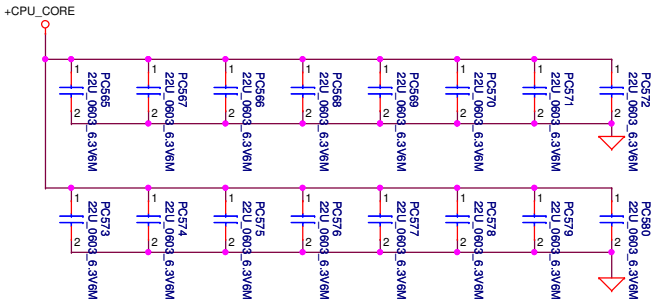
Size	Document Number	Rev
Custom	VFKAA	0.1

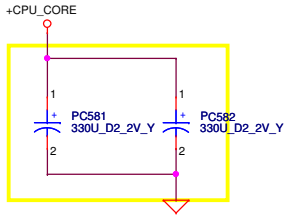
Date: Monday, March 11, 2013 | Sheet 52 of 56

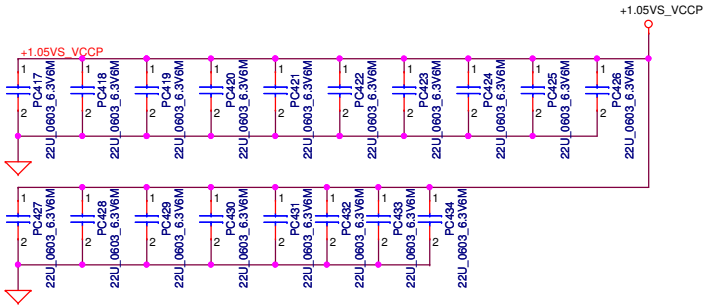
CPU_CORE output cap (36.4)
GFX_CORE output cap (36.5)
VCCP output cap (36.6)











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Issued Date	2012/09/24	Deciphered Date	2013/09/24

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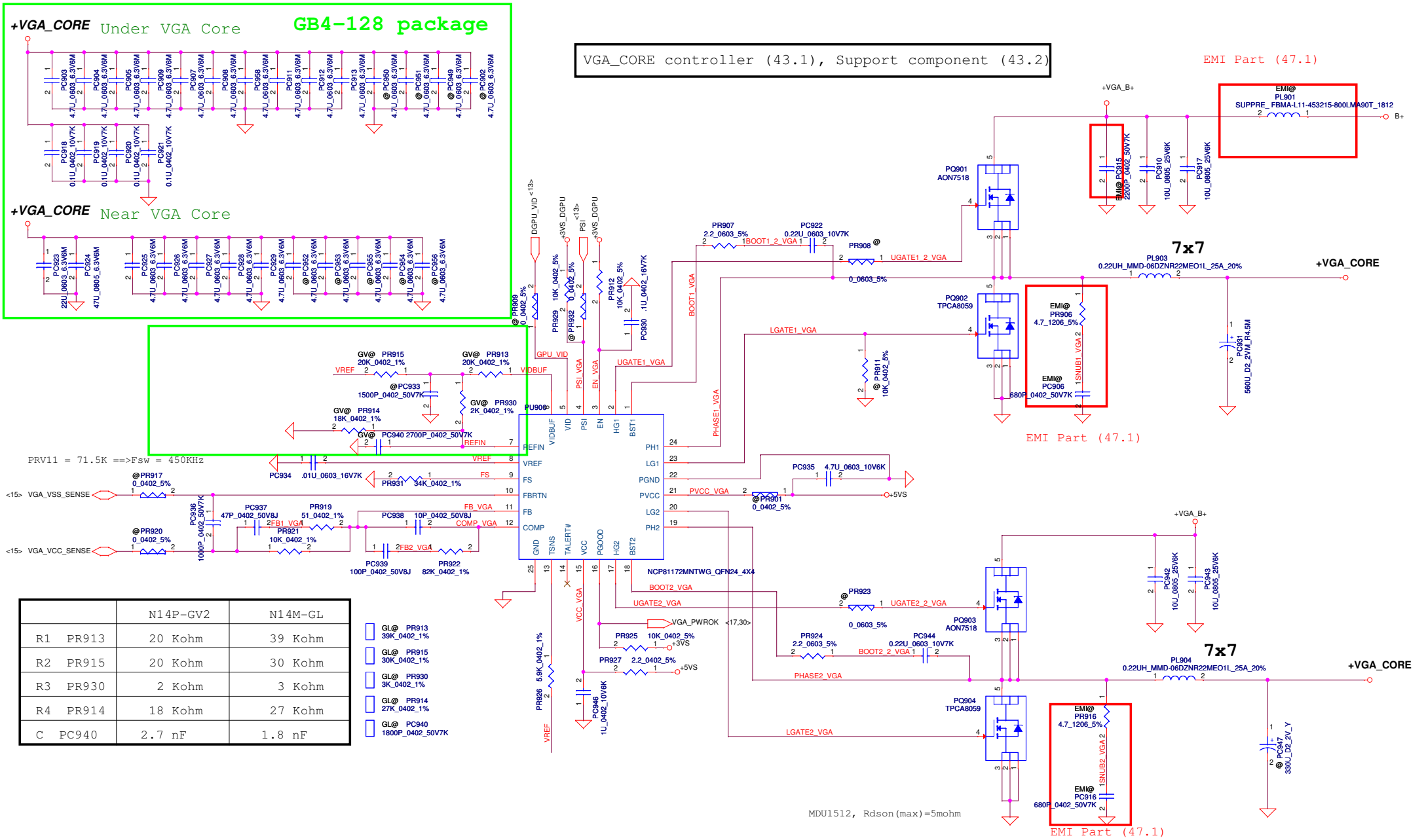
Compal Electronics, Inc.

Title: CPU_CORE_CAP

Size: Custom | Document Number: VFKAA | Rev: 0.1

Date: Monday, March 11, 2013 | Sheet 53 of 56



	N14P-GV2	N14M-GL
R1 PR913	20 Kohm	39 Kohm
R2 PR915	20 Kohm	30 Kohm
R3 PR930	2 Kohm	3 Kohm
R4 PR914	18 Kohm	27 Kohm
C PC940	2.7 nF	1.8 nF

GL@ PR913 39K_0402_1%
GL@ PR915 30K_0402_1%
GL@ PR930 3K_0402_1%
GL@ PR914 27K_0402_1%
GL@ PC940 1800P_0402_50V7K

Security Classification	Compal Secret Data		
Issued Date	2012/09/24	Deciphered Date	2013/09/24

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Compal Electronics, Inc.

Title: +VGA_COREP

Size: Custom | Document Number: VFKAA | Rev: 0.1

Date: | Sheet 54 of 56

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/10/26	Deciphered Date	2013/10/26	Title: Power PIR
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				Date: Monday, March 11, 2013; Sheet 55 of 56

HW PIR (Product Improve Record)

VFKAA LA-9863P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 to 0.2
GERBER-OUT DATE: 2012/12/06

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	11/20	06	Mount CC37	To solve S3 shutdown issue
2.	11/20	29	Change USB port 10 to NC	No support NFC
3.	11/20	42	Delete JNFC	No support NFC
4.	11/20	37	Add QW1, RW3, RW4; change JCARD.10 to SDWP# and JCARD.11 to SDCD	To solve card reader no function issue
5.	11/27	40	Change JSPK to ACES_50228-0067N-001_6P	For SPK recognize design
6.	11/28	08	Mount CC17, CC18, CC19	For ESD request
7.	11/28	29	Mount CB13	For ESD request
8.	11/28	05	Mount CC63	For ESD request
9.	12/03	38	Add S&C 14640/14641 co-layout circuit	Reserved for S&C SPEC update

VFKAA LA-9863P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2 to 0.3
GERBER-OUT DATE: 2013/01/23

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	12/19	41	Change CB13 to SE071101J80 (100pF)	ESD request
2.	12/26	17	Change RV43 to 270K, RV53 to 10K, RV54 to 33K	For VGA power sequence
3.	01/16	41	Add RB12, RB37, connect EC_MUTE_INT from codec to EC	To solve audio "bo" sound issue
4.	01/16	42	Modify JTP pin define	For ME drawing update
5.	01/16	13	Connect GPIO12 as GPS_DOWN# to EC	For GPS function
6.	01/16	26	Mount RH38	For EMI request
7.	01/16	22	Reserve R266, R267	For EMI request

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