

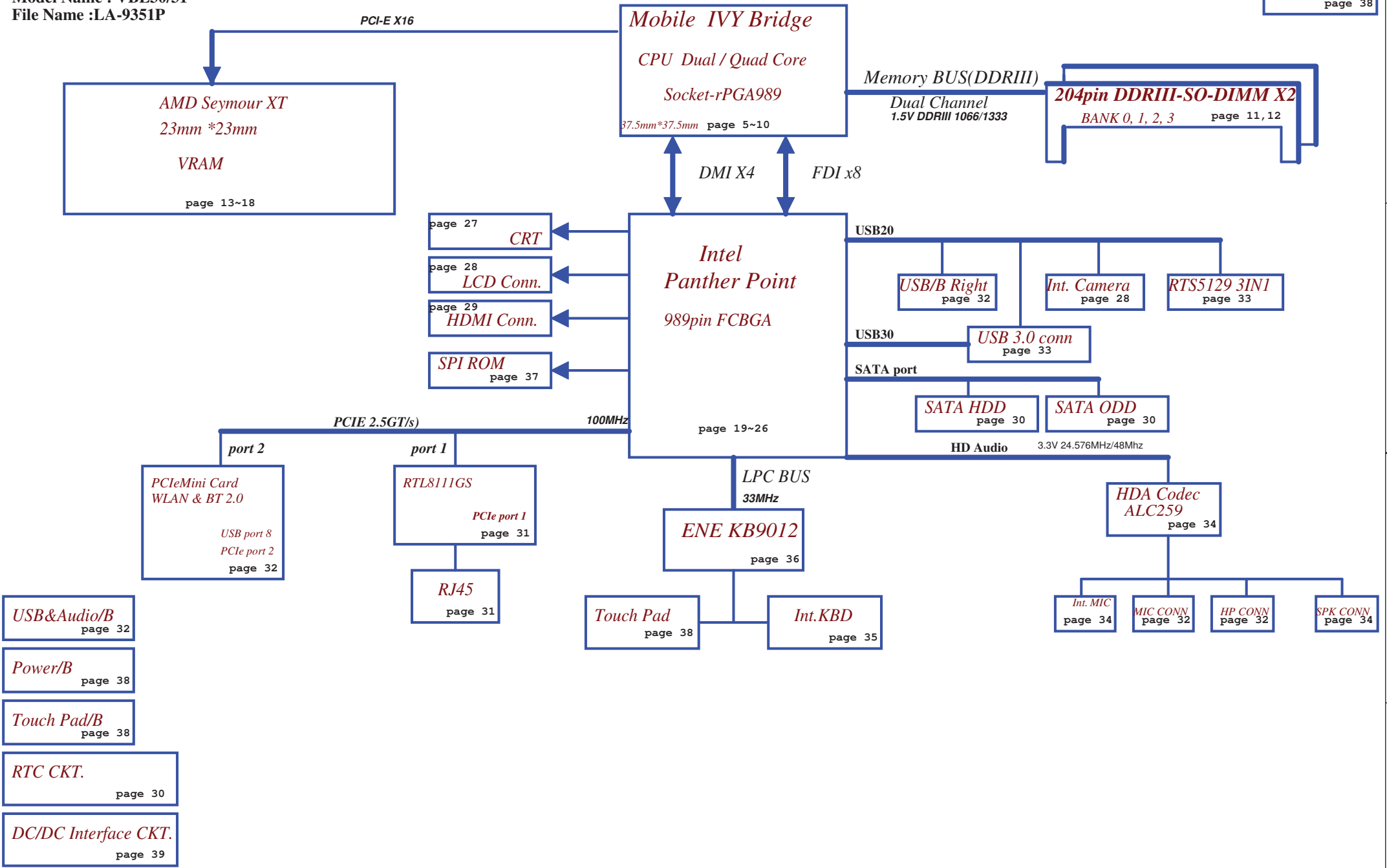
# Compal Confidential

## VBL30/31

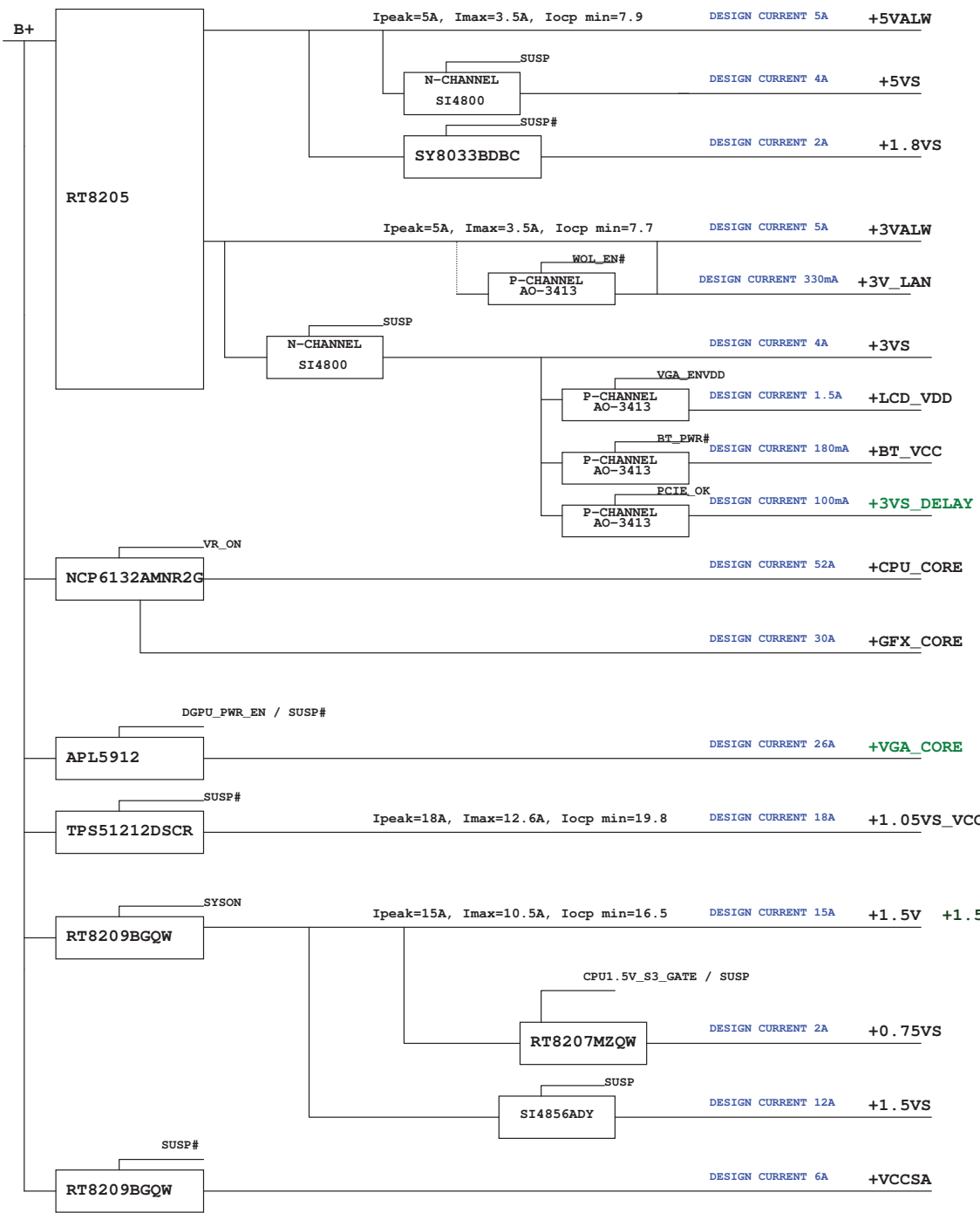
### LA-9351P REV0.1 Schematic

Intel Ivy Bridge/Panther Point  
AMD Seymour XT  
2012-05-08 Rev 0.1

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Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title	Cover Page
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### Voltage Rails

power plane	+B	+5VALW	+1.5V	+3VALW	+1.5V_IO	+5VS		+3VS		+1.5VS_VTT		+CPU_CORE		+VGA_CORE		+VCC_GFXCORE_AXG		+1.8VS		+0.75VS		
						State																
S0	○	○	○	○	○																	
S3	○	○	○	○	○																	X
S5 S4/AC	○	○	○	○	○																	X
S5 S4/ Battery only	○	○	○	○	○																	X
S5 S4/AC & Battery don't exist	X	X	X	X	X																	X

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

@	Reserve
CONN@	ME CONNECTOR
KB9012@	ENE EC
Nuvton@	Nuvton EC
NOW8@	not Support Win8
WIN8@	Support Win8
UMA@	UMA Sku
PX@	PX Sku

### EC SM Bus1 address

Power	Device	Address
+3VALW	Smart Battery	0001 011x b

### EC SM Bus2 address

Power	Device	Address
+3VS	VGA Internal thermal sensor	1001 111Xb (0x9E)

### PCH SM Bus address

Power	Device	Address
+3VS	DDR DIMMA	1001 000x b
+3VS	DDR DIMMB	1001 010x b

### SMBUS Control Table

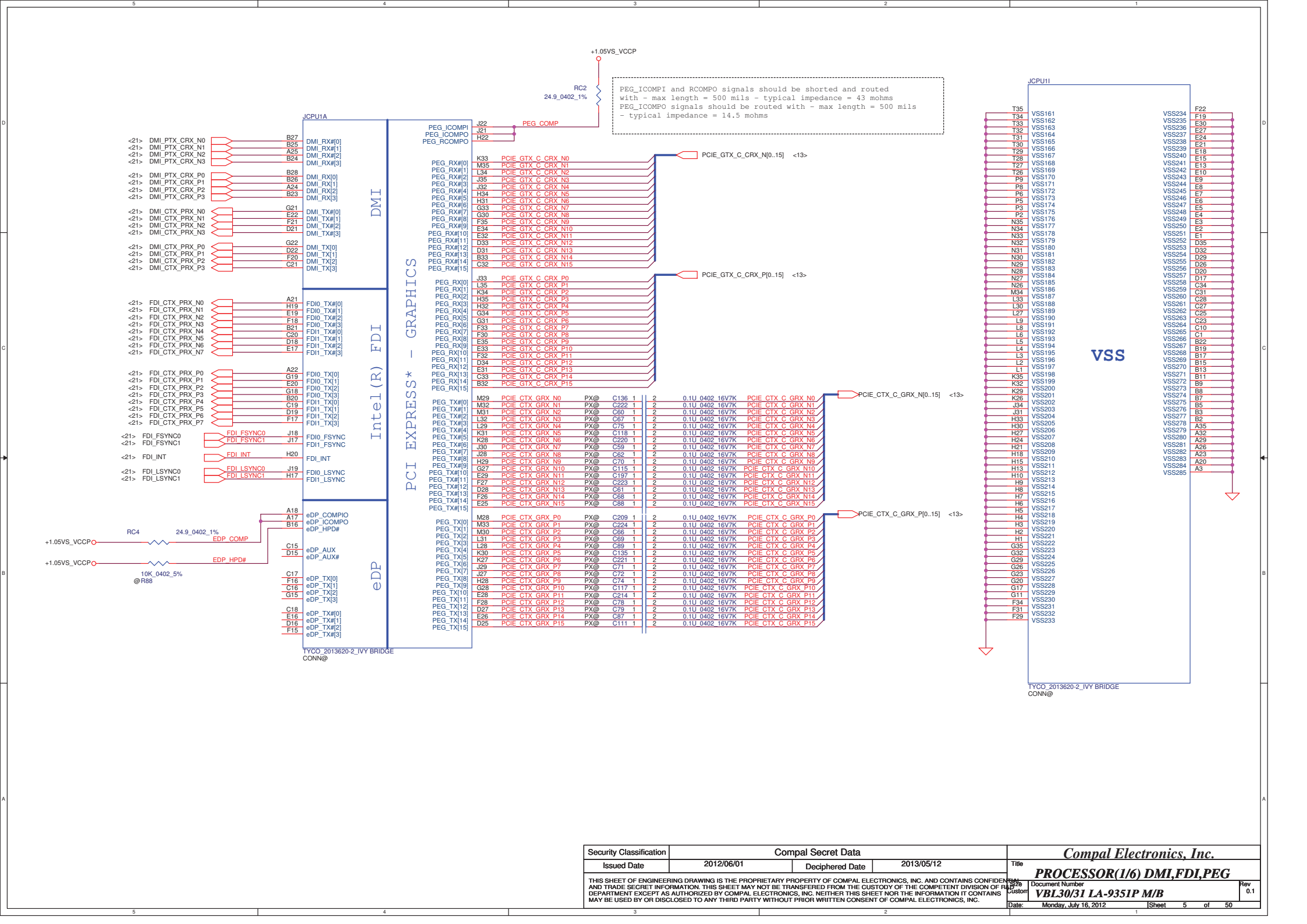
	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	X	V	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB9012	X	X	X	X	X	X	V
SMB_EC_DA2	+3VALW							+3VS
SMBCLK	PCH	X	X	X	V	V	X	X
SMBDATA	+3VALW				+3VS	+3VS		
SML0CLK	PCH	X	X	X	X	X	X	X
SML0DATA	+3VALW							
SML1CLK	PCH	V	X	V	X	X	V	X
SML1DATA	+3VALW	+3VS		+3VS			+3VS	

### PCH X76 and PCBA table

		config
X76	ZZZ X76@ HYN 1G	ZZZ @ HYN 1G
	ZZZ X76@ SAM 1G	R359 @ 10K_0402_5%
PCH	UH1 BD82HM70 QPXH C1 BGA 989P PCH@	R361 @ 10K_0402_5%
		R462 @ 10K_0402_5%
PCB	ZZZ DA2@	R360 @ 10K_0402_5%
	ZZZ DA8@	R361 @ 10K_0402_5%
	ZZZ DA4@	R461 @ 10K_0402_5%
	ZZZ DA2@	

(@/CONN@/DA2@/DA4@/DA8@/DAZ@/KB9012@/NOW8@/Nuvton@/PCH@/PX@/Rev01@/Rev02@/Rev03@/Rev04@/Rev10@/UMA@/WIN8@/X76@)

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PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
 PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

Intel(R) FDI  
 PCI EXPRESS\* - GRAPHICS

PEG\_ICOMPI  
 PEG\_ICOMPO  
 PEG\_RCOMPO

PEG\_RX#0  
 PEG\_RX#1  
 PEG\_RX#2  
 PEG\_RX#3  
 PEG\_RX#4  
 PEG\_RX#5  
 PEG\_RX#6  
 PEG\_RX#7  
 PEG\_RX#8  
 PEG\_RX#9  
 PEG\_RX#10  
 PEG\_RX#11  
 PEG\_RX#12  
 PEG\_RX#13  
 PEG\_RX#14  
 PEG\_RX#15

PEG\_TX#0  
 PEG\_TX#1  
 PEG\_TX#2  
 PEG\_TX#3  
 PEG\_TX#4  
 PEG\_TX#5  
 PEG\_TX#6  
 PEG\_TX#7  
 PEG\_TX#8  
 PEG\_TX#9  
 PEG\_TX#10  
 PEG\_TX#11  
 PEG\_TX#12  
 PEG\_TX#13  
 PEG\_TX#14  
 PEG\_TX#15

PEG\_TX#0  
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 PEG\_TX#2  
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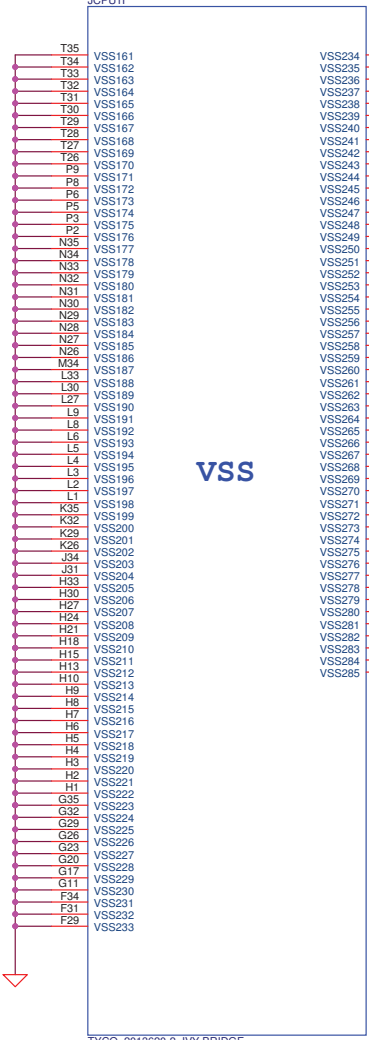
TYCO\_2013620-2\_IVY BRIDGE  
 CONN@

K33 PCIE GTX C CRX N0  
 M35 PCIE GTX C CRX N1  
 L34 PCIE GTX C CRX N2  
 J85 PCIE GTX C CRX N3  
 J82 PCIE GTX C CRX N4  
 H34 PCIE GTX C CRX N5  
 H31 PCIE GTX C CRX N6  
 G33 PCIE GTX C CRX N7  
 G30 PCIE GTX C CRX N8  
 F35 PCIE GTX C CRX N9  
 E34 PCIE GTX C CRX N10  
 E32 PCIE GTX C CRX N11  
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 B33 PCIE GTX C CRX N14  
 C32 PCIE GTX C CRX N15

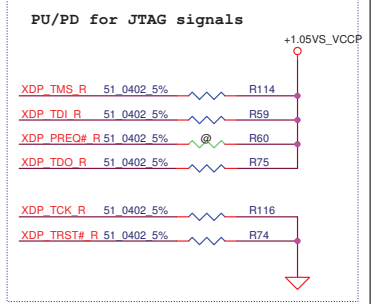
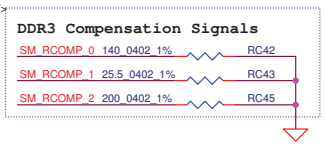
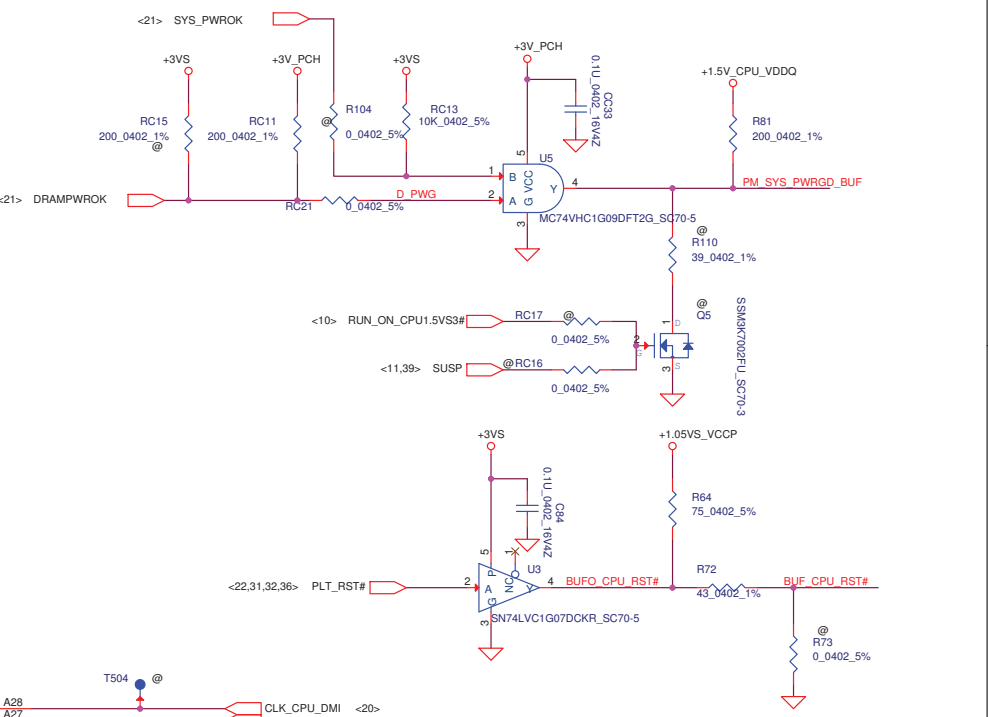
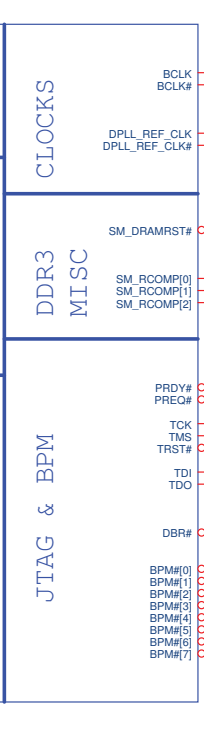
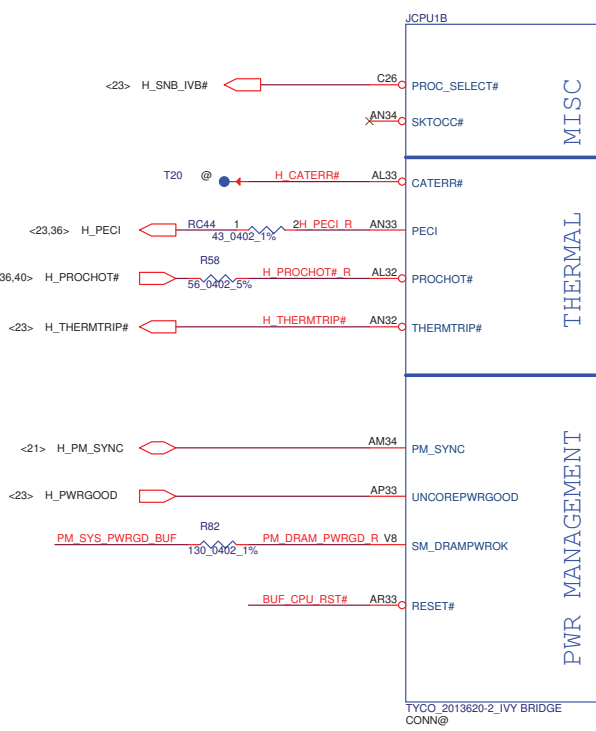
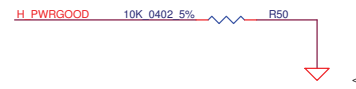
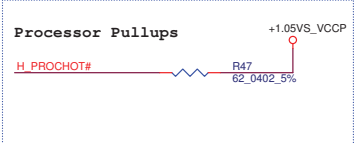
J33 PCIE GTX C CRX P0  
 L35 PCIE GTX C CRX P1  
 K34 PCIE GTX C CRX P2  
 H35 PCIE GTX C CRX P3  
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 G34 PCIE GTX C CRX P5  
 G31 PCIE GTX C CRX P6  
 F33 PCIE GTX C CRX P7  
 F30 PCIE GTX C CRX P8  
 E35 PCIE GTX C CRX P9  
 E33 PCIE GTX C CRX P10  
 F32 PCIE GTX C CRX P11  
 D34 PCIE GTX C CRX P12  
 E31 PCIE GTX C CRX P13  
 C33 PCIE GTX C CRX P14  
 B32 PCIE GTX C CRX P15

M29 PCIE CTX GRX N0 PX@ C136 1 2 0.1U 0402 16V7K PCIE CTX C GRX N0  
 M32 PCIE CTX GRX N1 PX@ C222 1 2 0.1U 0402 16V7K PCIE CTX C GRX N1  
 M31 PCIE CTX GRX N2 PX@ C60 1 2 0.1U 0402 16V7K PCIE CTX C GRX N2  
 L32 PCIE CTX GRX N3 PX@ C67 1 2 0.1U 0402 16V7K PCIE CTX C GRX N3  
 L29 PCIE CTX GRX N4 PX@ C75 2 2 0.1U 0402 16V7K PCIE CTX C GRX N4  
 K31 PCIE CTX GRX N5 PX@ C118 1 2 0.1U 0402 16V7K PCIE CTX C GRX N5  
 K28 PCIE CTX GRX N6 PX@ C220 1 2 0.1U 0402 16V7K PCIE CTX C GRX N6  
 J30 PCIE CTX GRX N7 PX@ C59 1 2 0.1U 0402 16V7K PCIE CTX C GRX N7  
 J28 PCIE CTX GRX N8 PX@ C62 1 2 0.1U 0402 16V7K PCIE CTX C GRX N8  
 H29 PCIE CTX GRX N9 PX@ C70 1 2 0.1U 0402 16V7K PCIE CTX C GRX N9  
 G27 PCIE CTX GRX N10 PX@ C115 1 2 0.1U 0402 16V7K PCIE CTX C GRX N10  
 E29 PCIE CTX GRX N11 PX@ C197 1 2 0.1U 0402 16V7K PCIE CTX C GRX N11  
 F27 PCIE CTX GRX N12 PX@ C223 1 2 0.1U 0402 16V7K PCIE CTX C GRX N12  
 D28 PCIE CTX GRX N13 PX@ C81 1 2 0.1U 0402 16V7K PCIE CTX C GRX N13  
 F26 PCIE CTX GRX N14 PX@ C68 1 2 0.1U 0402 16V7K PCIE CTX C GRX N14  
 E25 PCIE CTX GRX N15 PX@ C88 1 2 0.1U 0402 16V7K PCIE CTX C GRX N15

M28 PCIE CTX GRX P0 PX@ C209 1 2 0.1U 0402 16V7K PCIE CTX C GRX P0  
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 G28 PCIE CTX GRX P10 PX@ C117 1 2 0.1U 0402 16V7K PCIE CTX C GRX P10  
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 F28 PCIE CTX GRX P12 PX@ C78 1 2 0.1U 0402 16V7K PCIE CTX C GRX P12  
 D27 PCIE CTX GRX P13 PX@ C79 1 2 0.1U 0402 16V7K PCIE CTX C GRX P13  
 E26 PCIE CTX GRX P14 PX@ C87 1 2 0.1U 0402 16V7K PCIE CTX C GRX P14  
 D25 PCIE CTX GRX P15 PX@ C111 1 2 0.1U 0402 16V7K PCIE CTX C GRX P15



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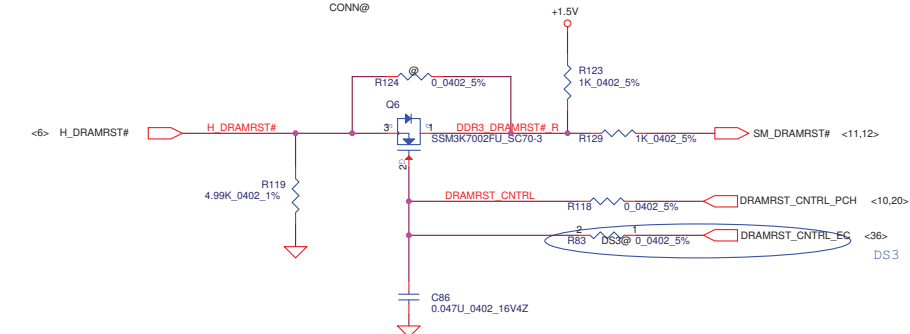
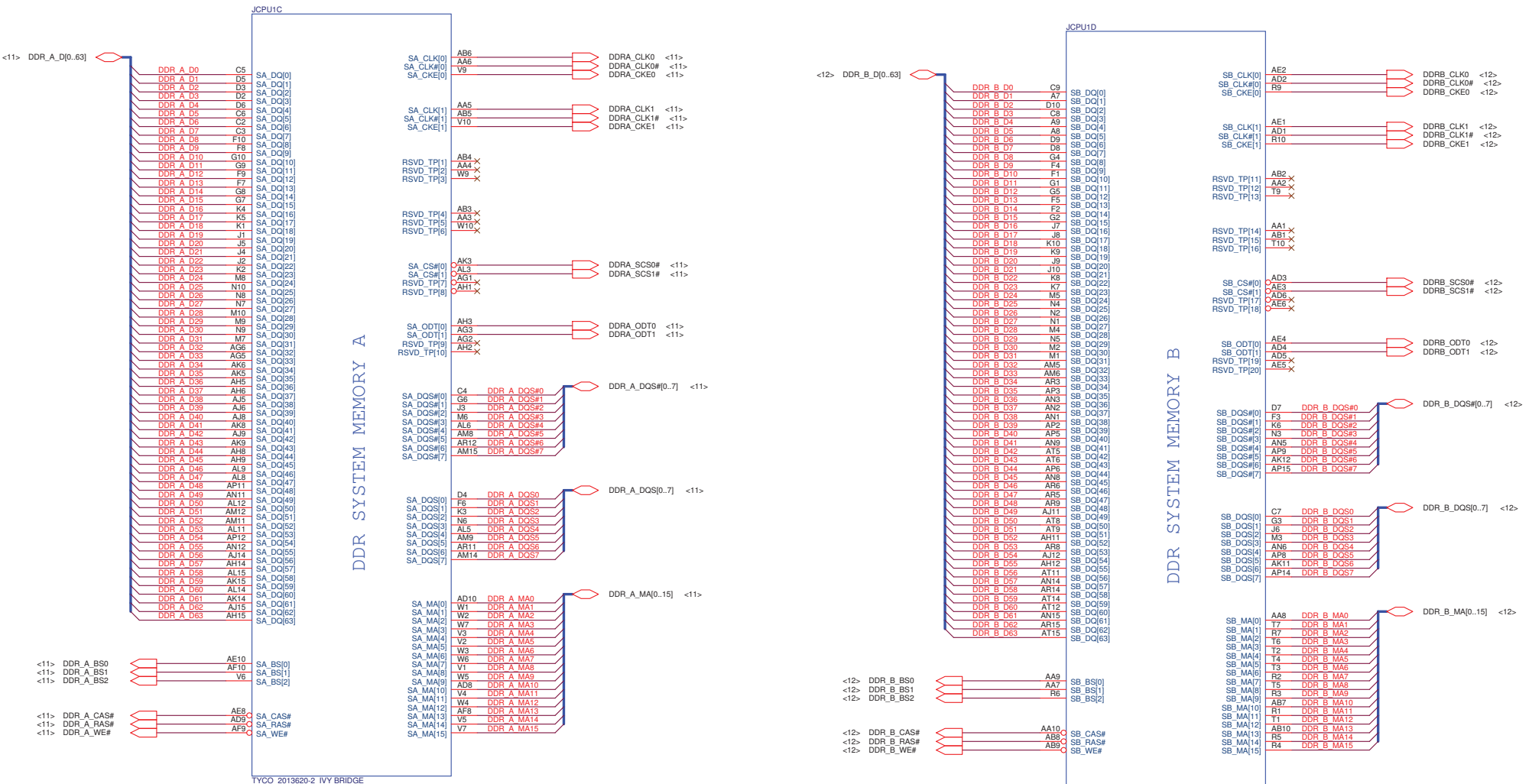


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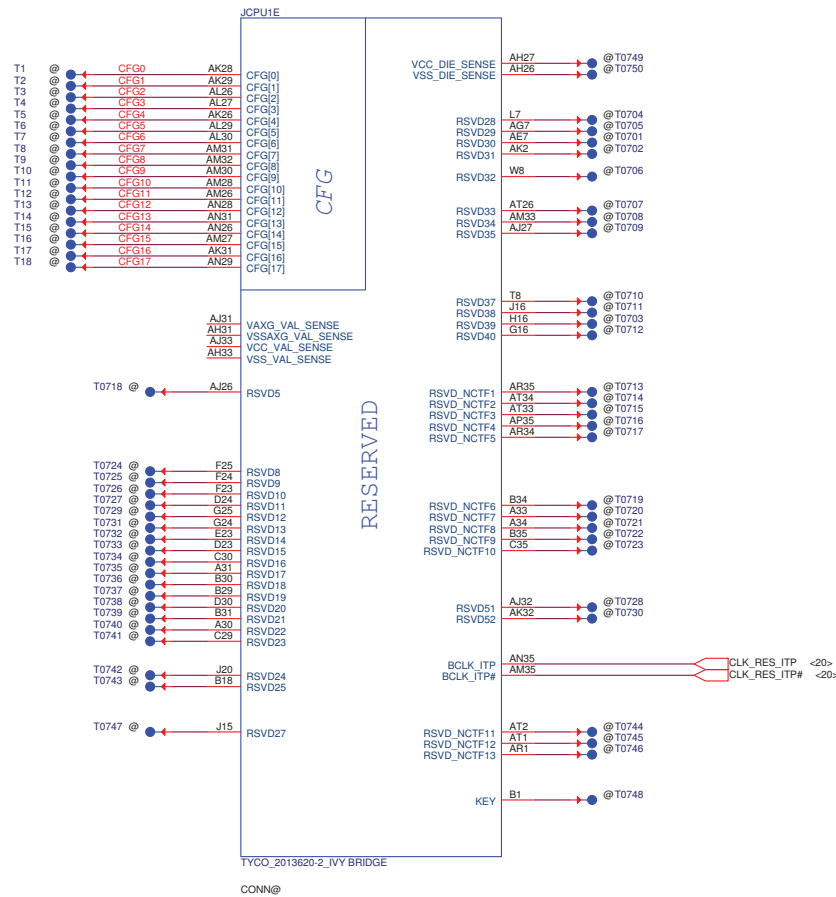
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Title	PROCESSOR(2/6) PM,XDP,CLK
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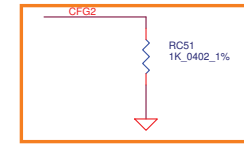
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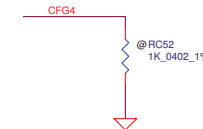
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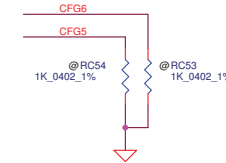
### CFG Straps for Processor



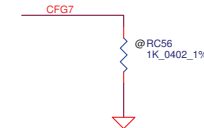
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

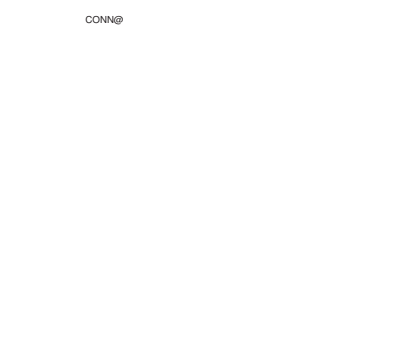
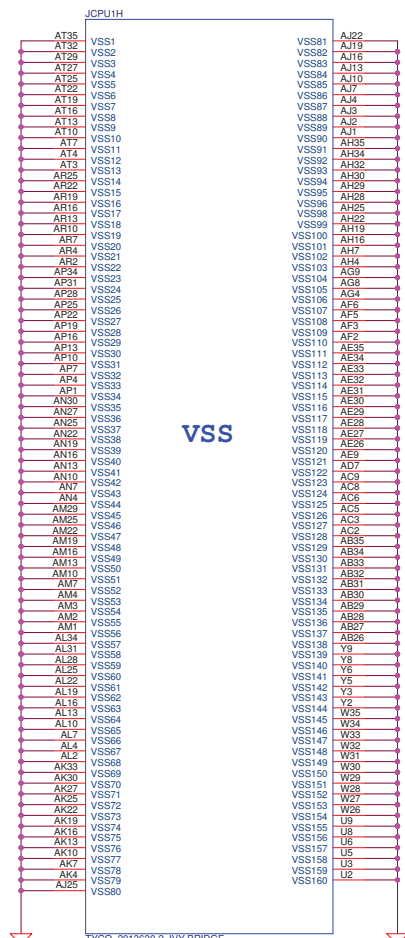


PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

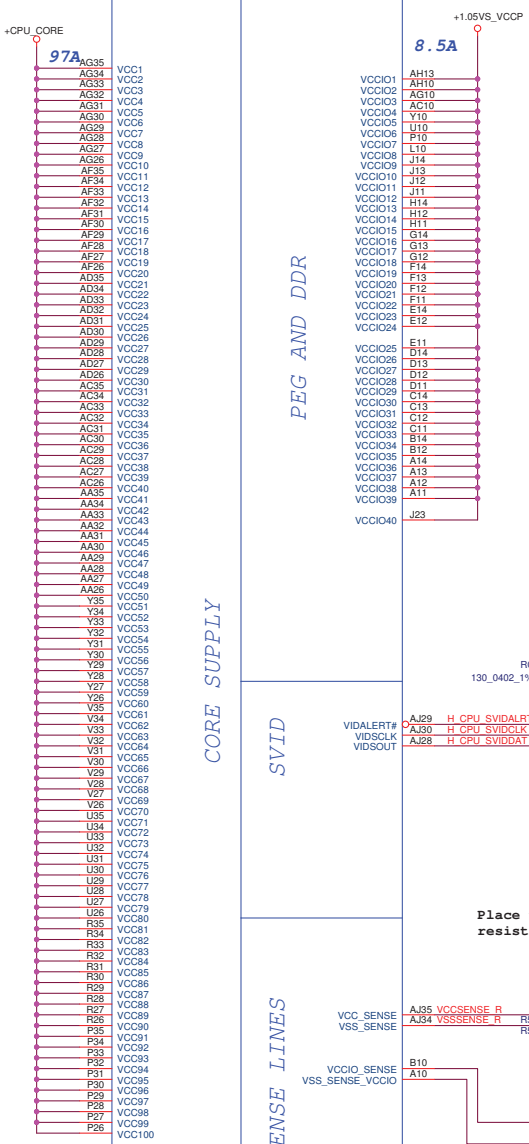


PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following RESETB de assertion 0: PEG Wait for BIOS for training





**POWER**

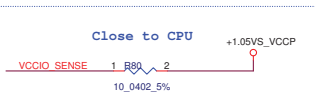
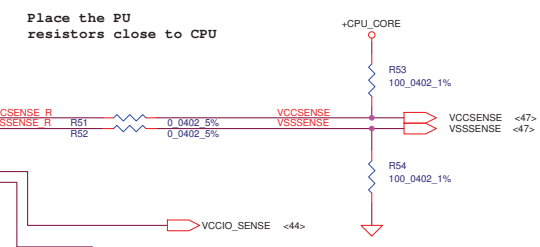
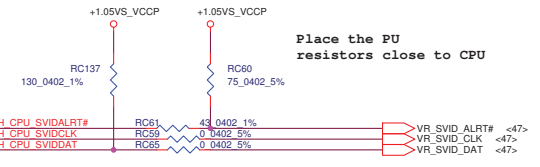


PEG AND DDR

CORE SUPPLY

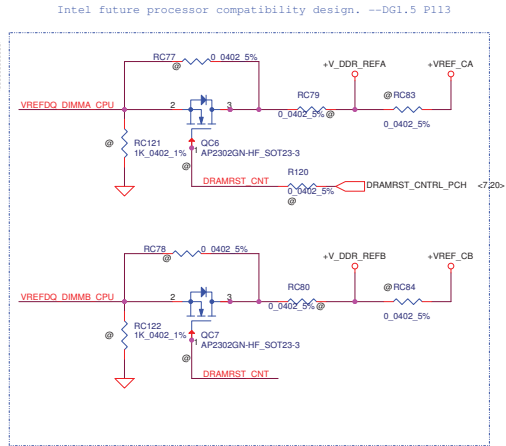
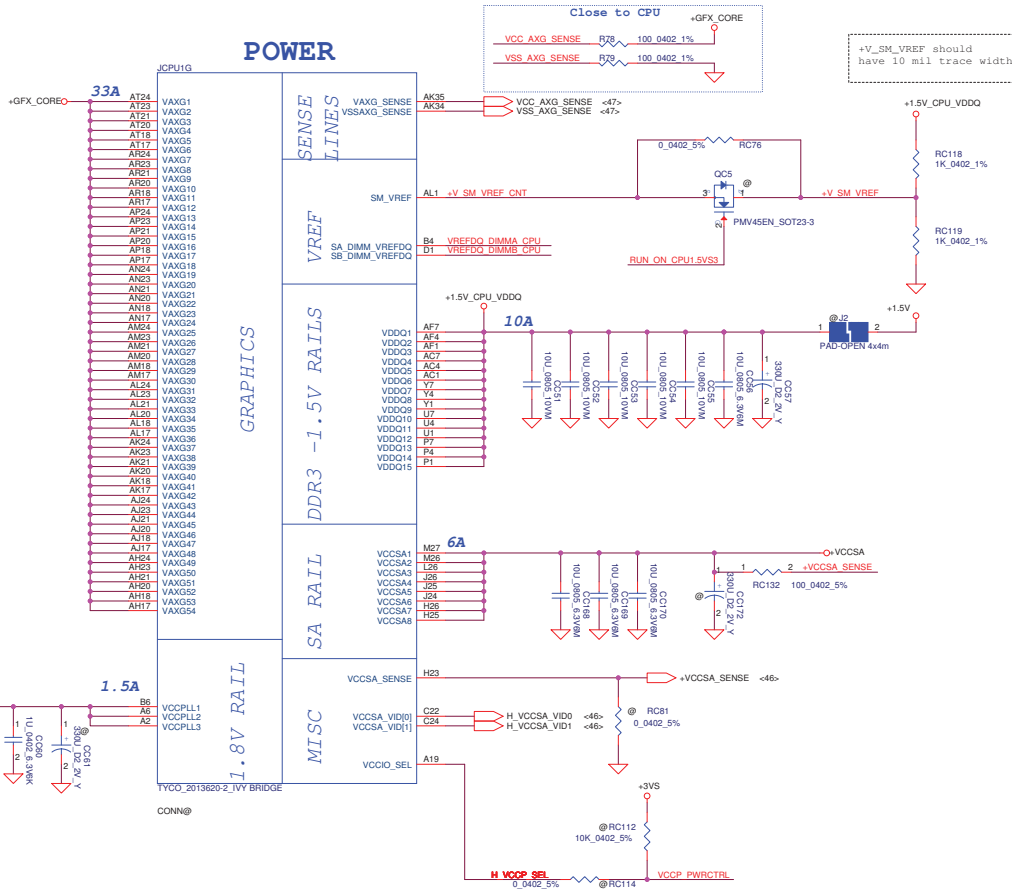
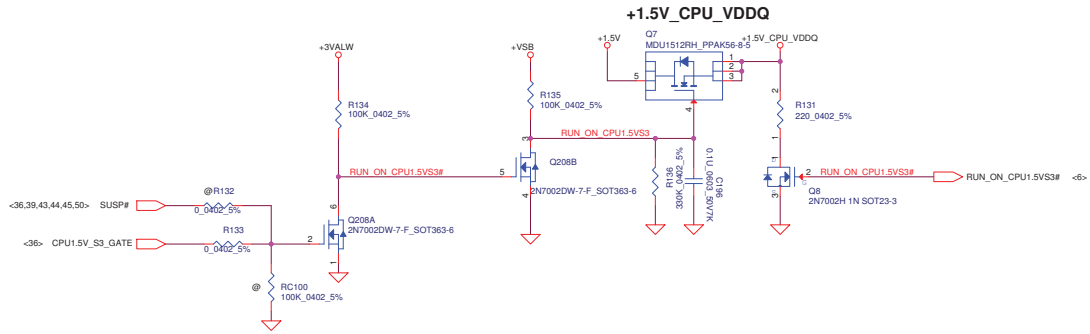
SVID

SENSE LINES



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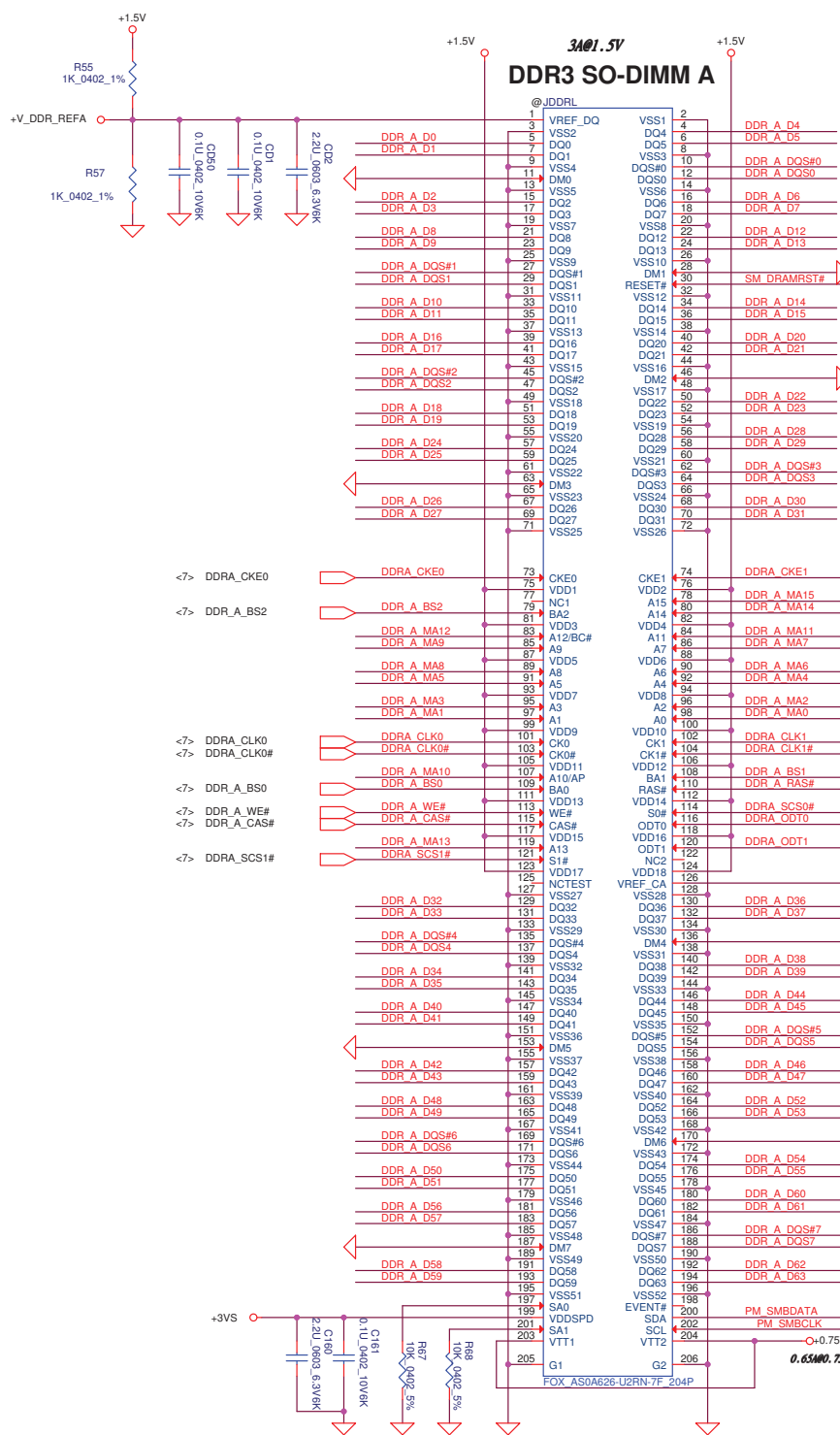
<b>Compal Electronics, Inc.</b>	
<b>PROCESSOR(5/6) PWR,BYPASS</b>	
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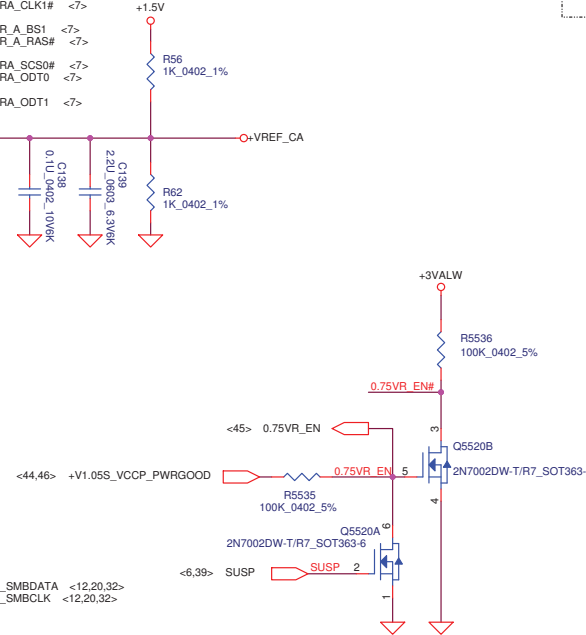
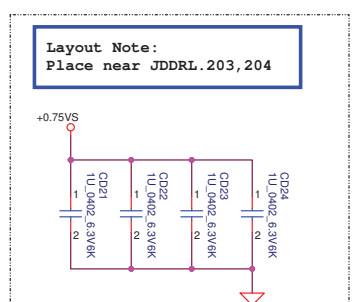
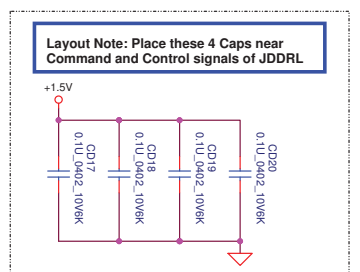
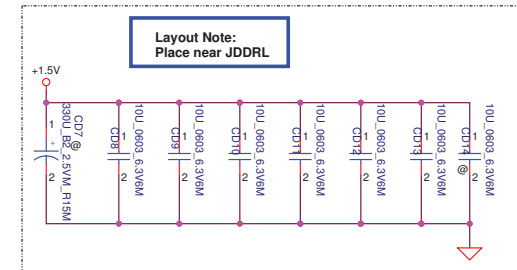
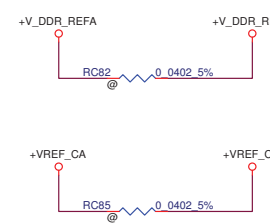
IVY Bridge drives VCCIO\_SEL low  
 VCCP\_PWRCTRL:0

Sandy Bridge is NC for A19  
 VCCP\_PWRCTRL:1

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VPL3031 LA-9351P M/B				0.1
Date: Monday, July 16, 2012				Sheet 10 of 50

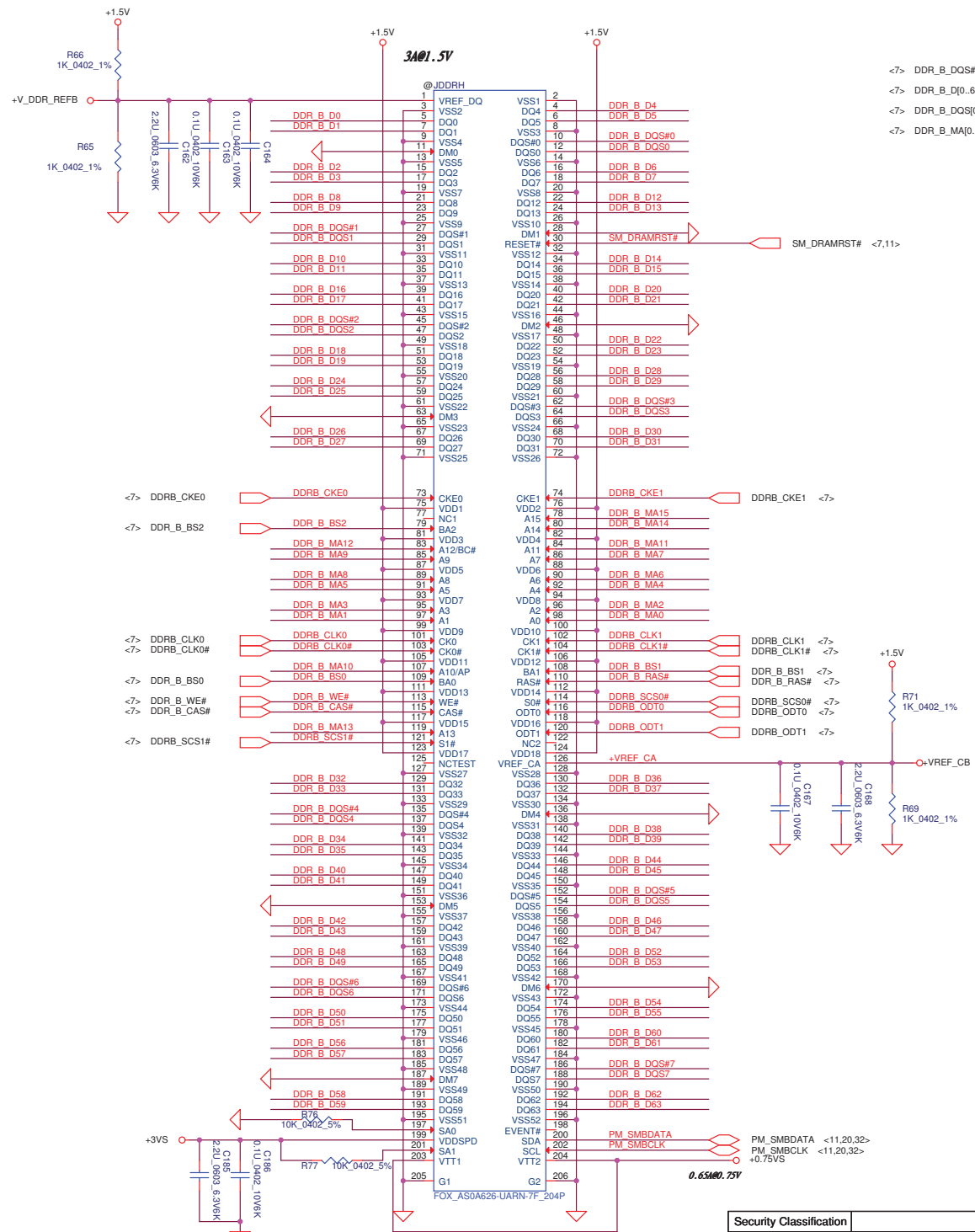


- <7> DDR\_A\_D[0..63]
- <7> DDR\_A\_DQS[0..7]
- <7> DDR\_A\_DQS#[0..7]
- <7> DDR\_A\_MA[0..15]

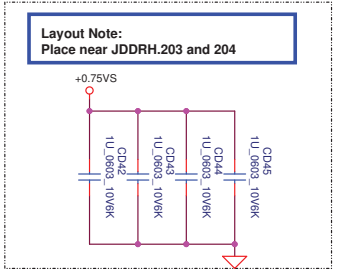
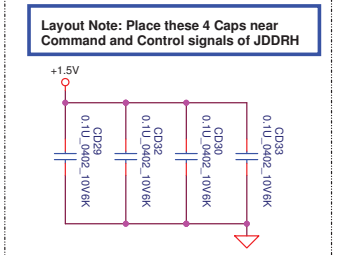
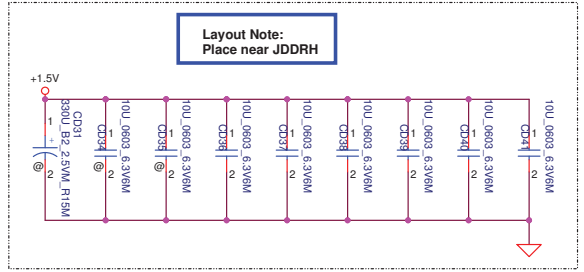


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Compal Electronics, Inc.	
Title	DDRIII-DDRLL
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- <7> DDR\_B\_DQS#[0..7]
- <7> DDR\_B\_D[0..63]
- <7> DDR\_B\_DQS[0..7]
- <7> DDR\_B\_MA[0..15]



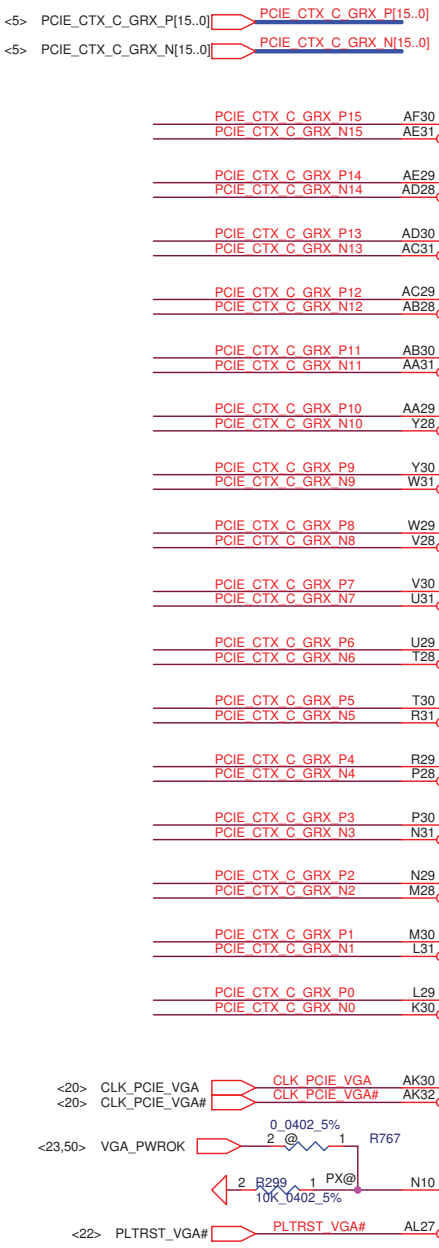
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Issued Date	2012/06/01	Deciphered Date	2013/05/12	DDDRIII-DDRH	
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**Compal Electronics, Inc.**

**DDDRIII-DDRH**

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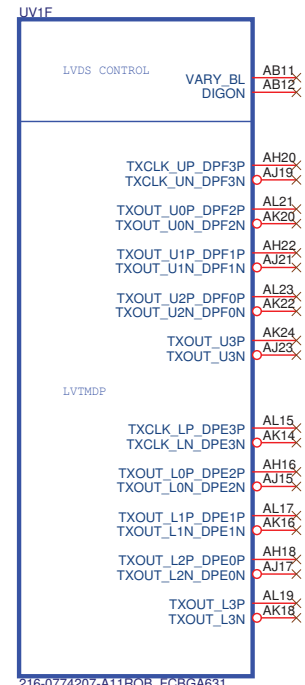
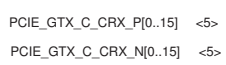
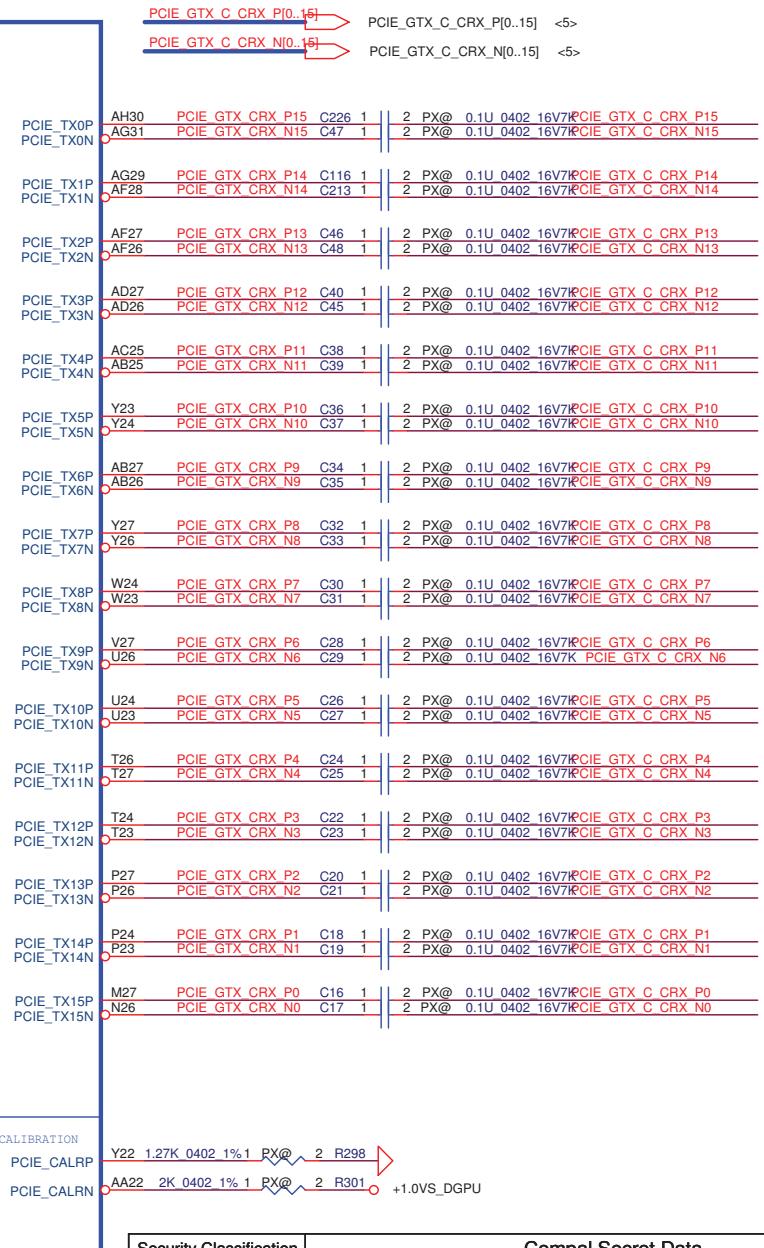


UV1A

216-0774207-A11ROB\_FCBGA631

PX@

PCI EXPRESS INTERFACE

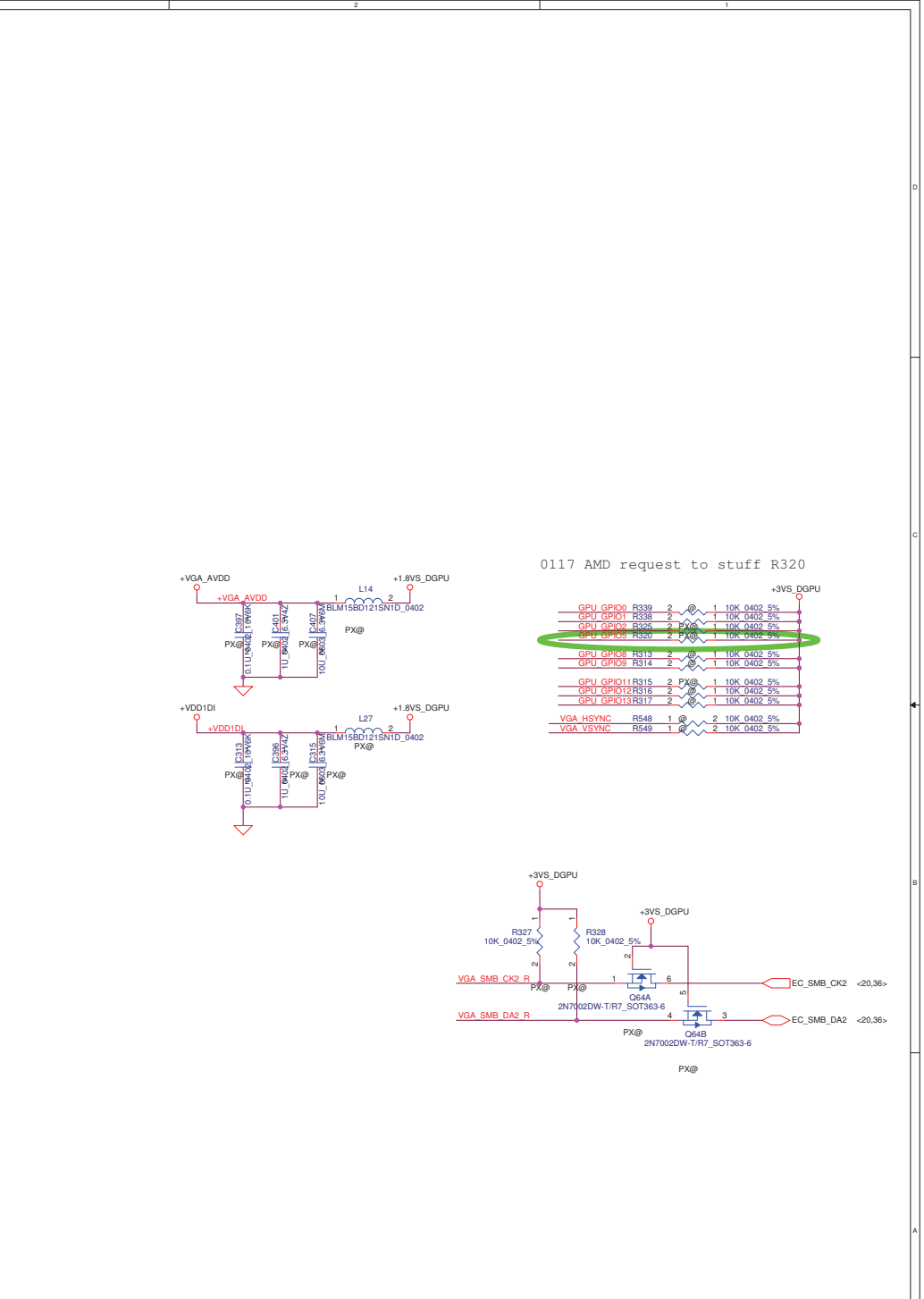
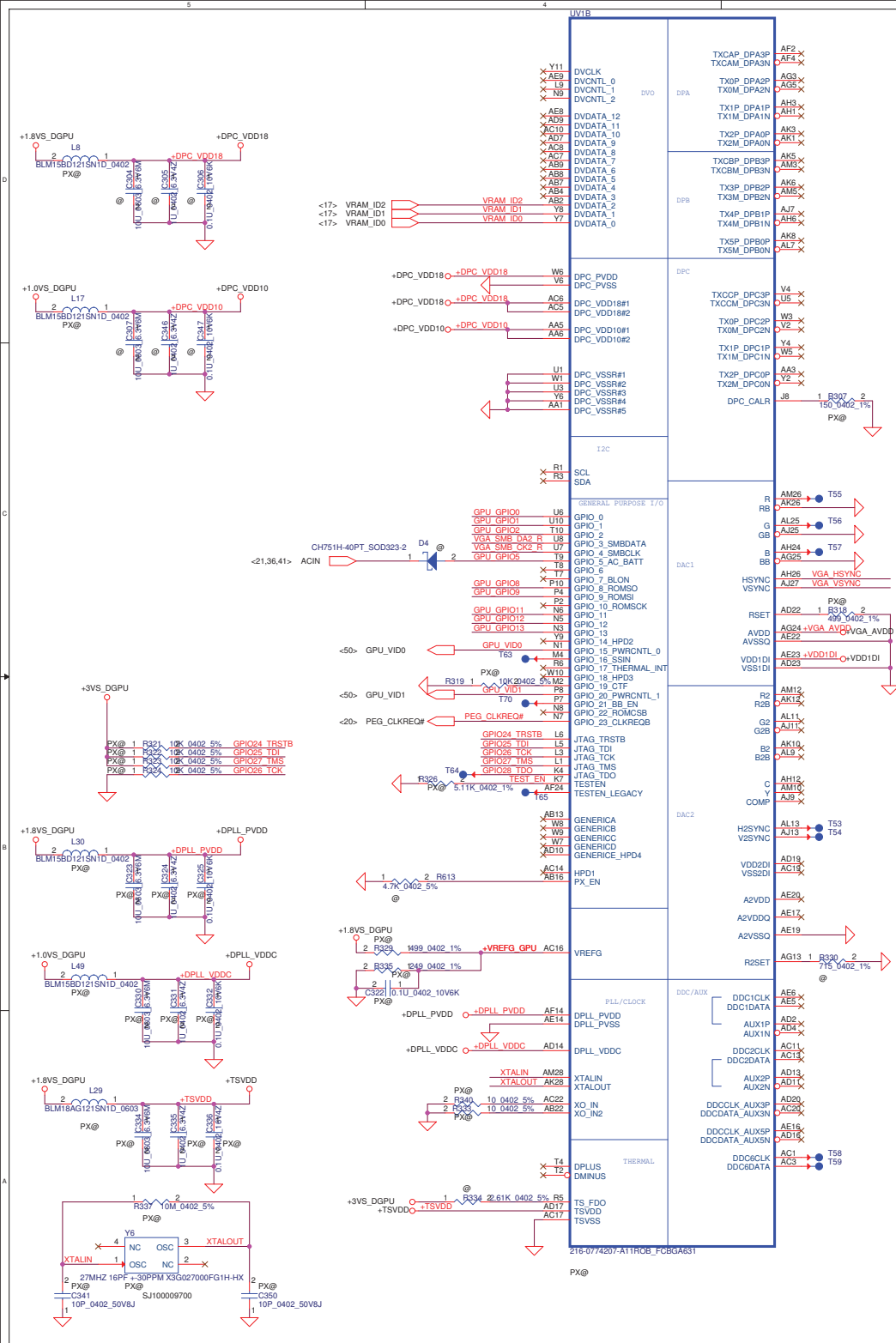


PX@

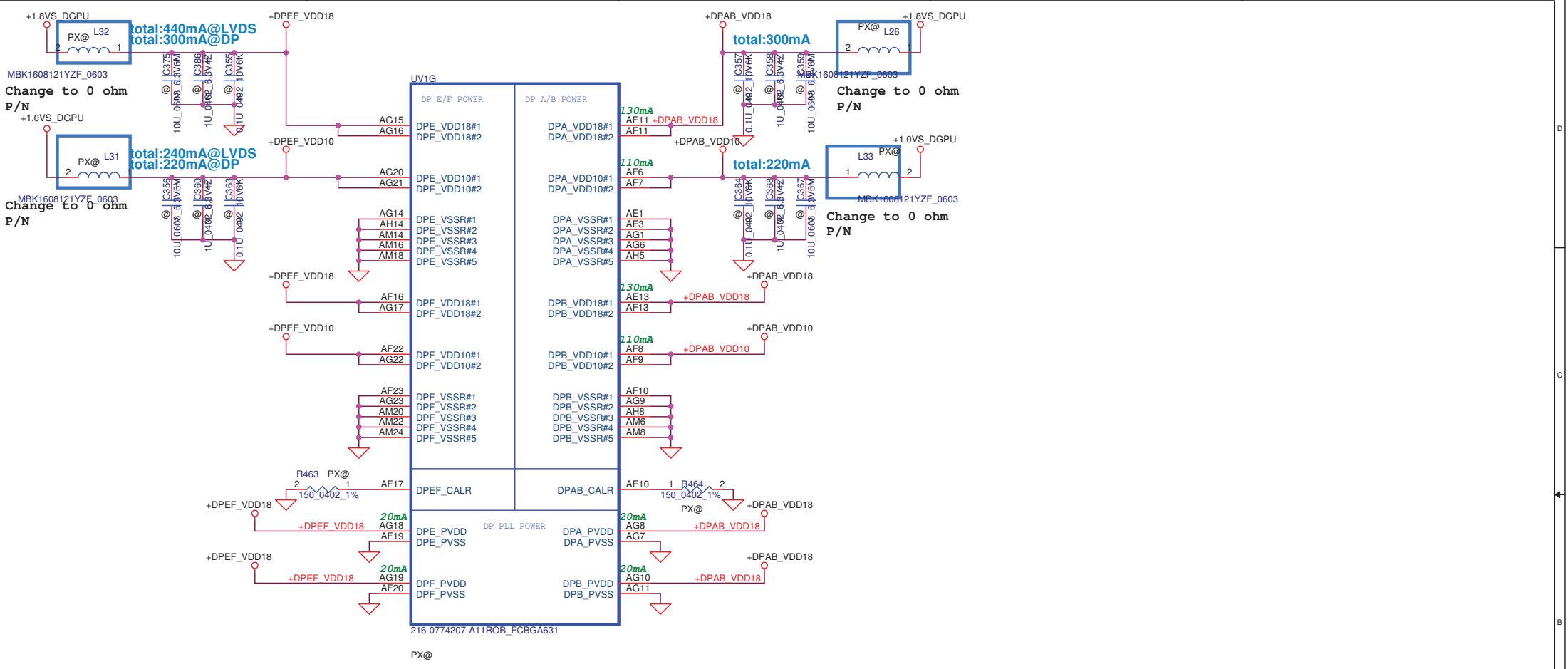
LVDS

PCIE LANE

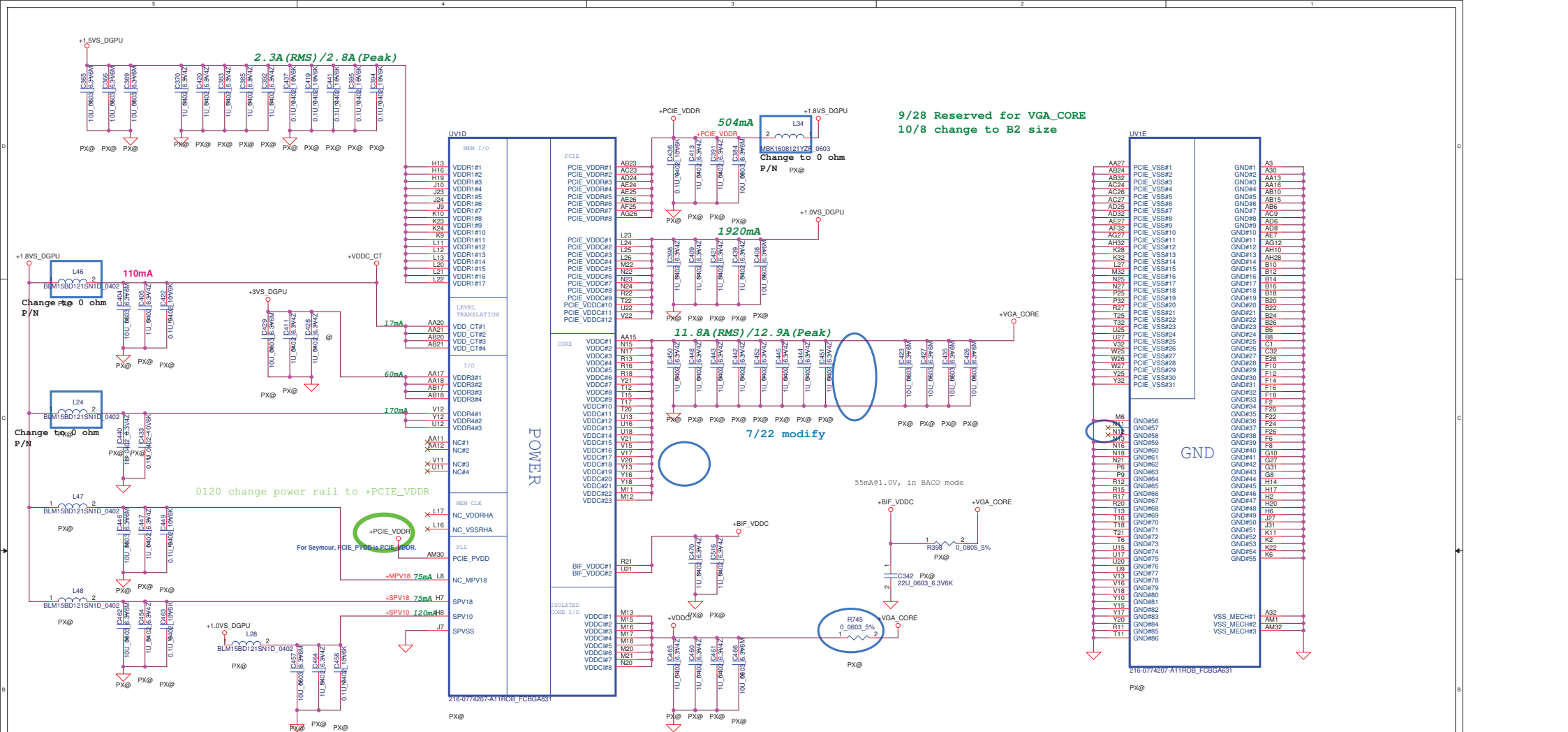
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title	
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Issued Date	2012/06/01	Deciphered Date	2013/05/12	SeymourXT-S3 Main Generic/MSIC	
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Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title	SeymourXT-S3 DP PWR
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				0.1	0.1
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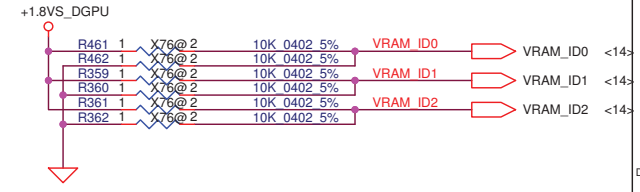
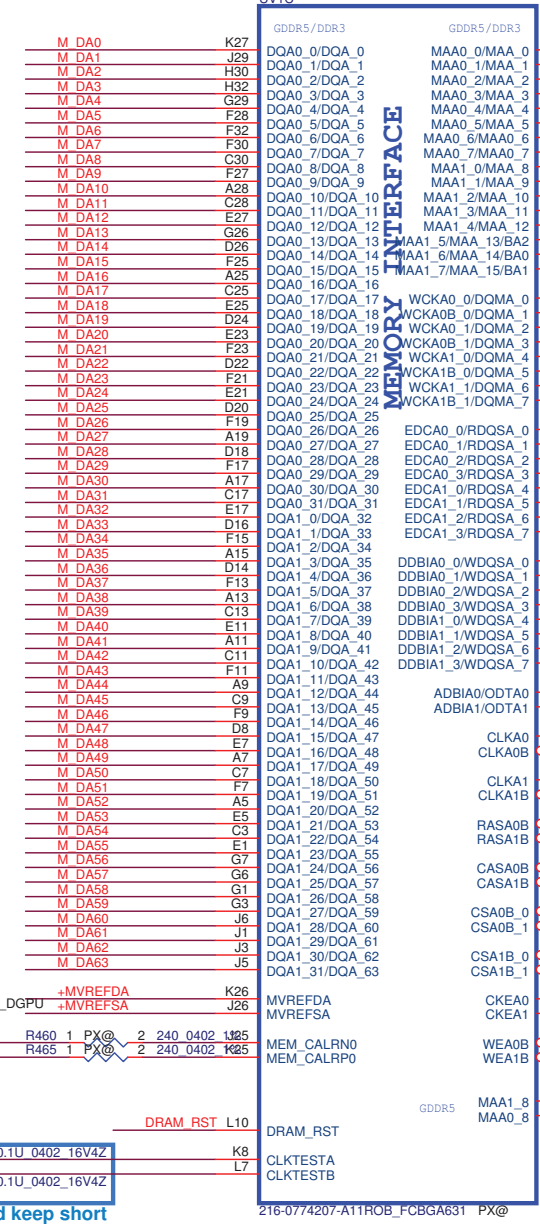
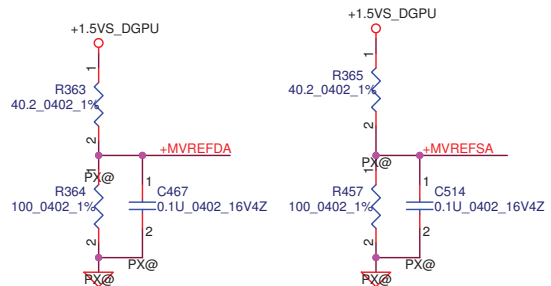
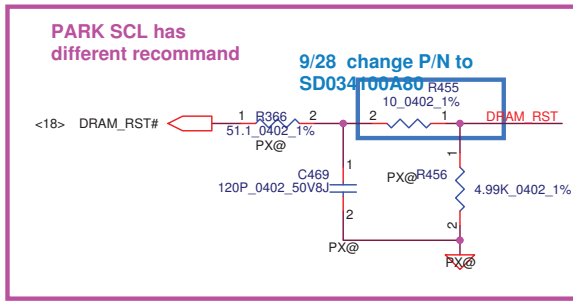


9/28 Reserved for VGA\_CORE  
10/8 change to B2 size

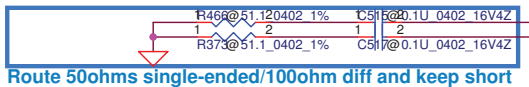
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Issued Date	2012/06/01	Deciphered Date	2013/05/12	SeymourXT-S3 PWR/GND	
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- <18> M\_DA[63..0] M\_DA[63..0]
- <18> M\_MA[13..0] M\_MA[13..0]
- <18> M\_DQM[7..0] M\_DQM[7..0]
- <18> M\_DQS[7..0] M\_DQS[7..0]
- <18> M\_DQS#[7..0] M\_DQS#[7..0]



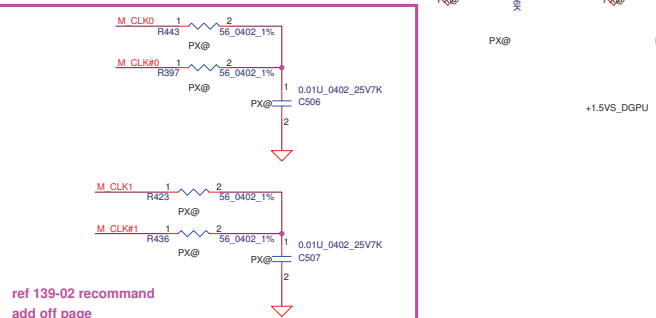
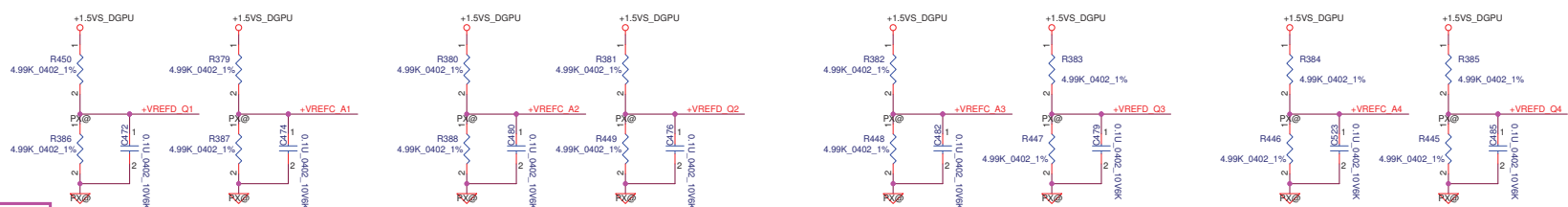
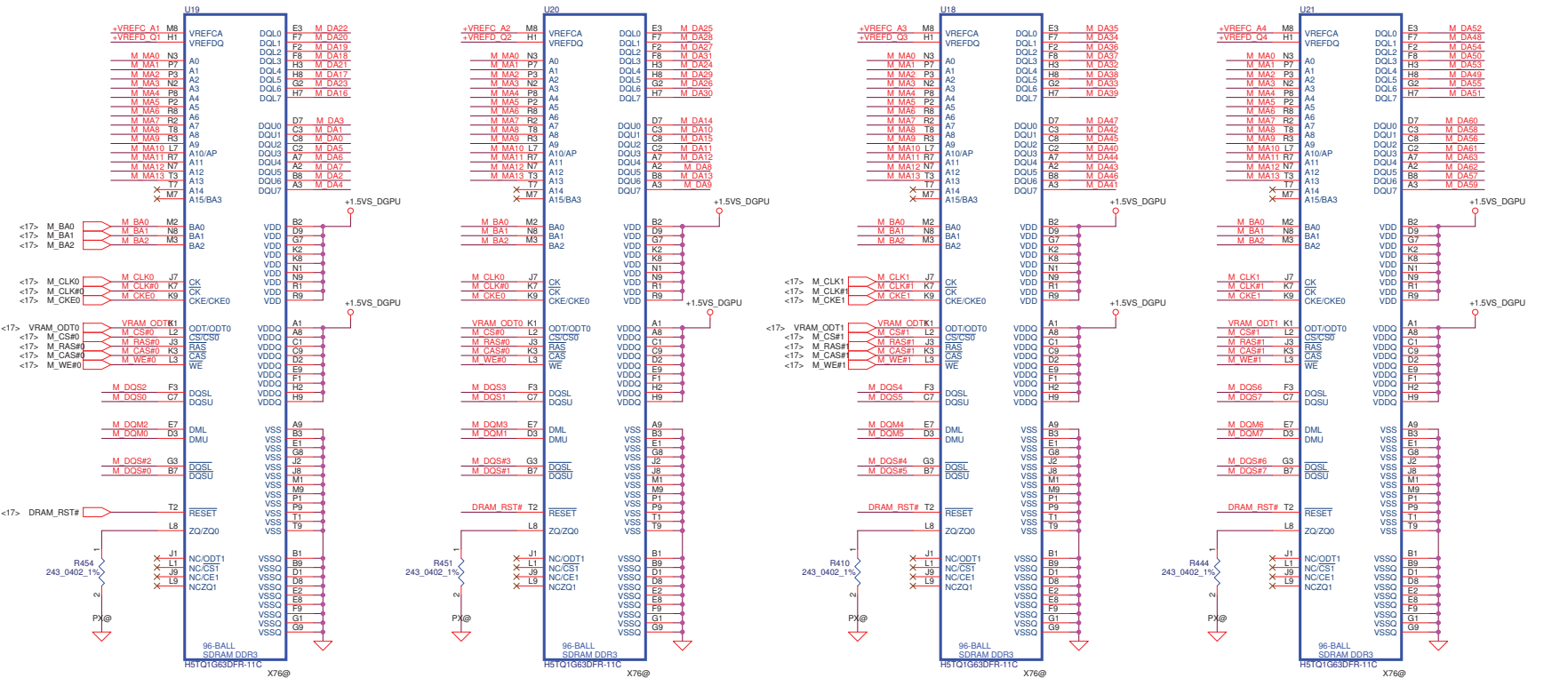
Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
K4W1G1646G-BC11 <b>Samsung 128MB</b> PN:SA00004GS00	R461	R360	R362
H5TQ1G63DFR-11C <b>Hynix 128MB</b> PN:SA000041S20	R462	R359	R362
K4W2G1646C-BC11 <b>Samsung 256MB</b> PN:SA000047Q00	R461	R360	R361
H5TQ2G63BFR-11C/H5TQ2G63DFR-11C <b>Hynix 256MB</b> PN:SA00003YO10/ SA00003YOAO	R462	R359	R361



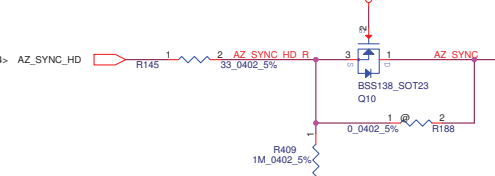
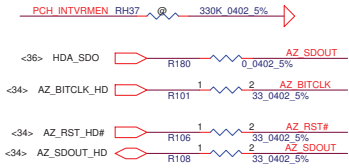
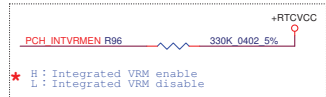
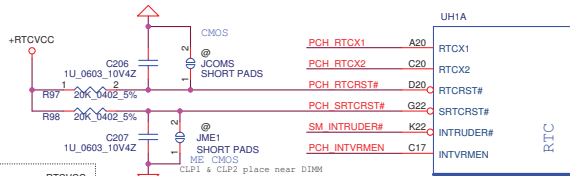
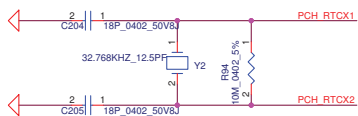
**Route 50ohms single-ended/100ohm diff and keep short debug only, for clock observation,if not need, DNI.**

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				<b>SeymourXT-S3 MEM Interface</b>
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				<b>Rev</b> 0.1
		<b>Date:</b>	Monday, July 16, 2012	<b>Sheet</b> 17 of 50

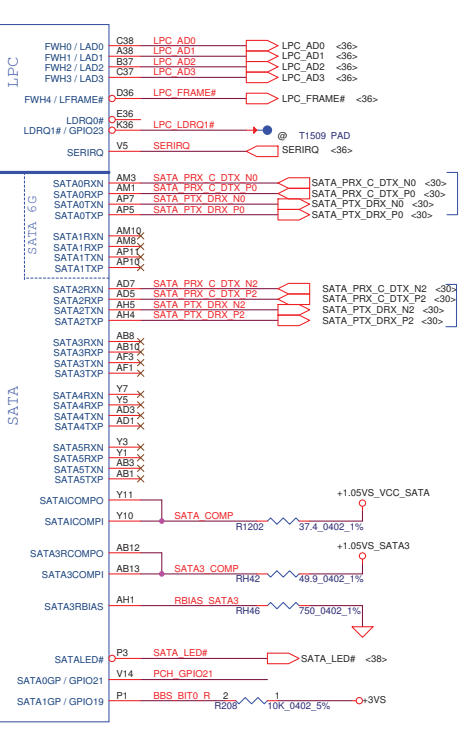
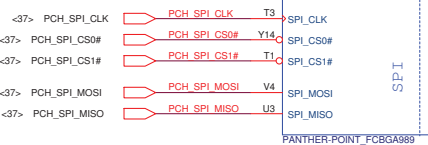
<17> M\_DA[63..0] <M\_DA63..0>  
 <17> M\_MA[13..0] <M\_MA13..0>  
 <17> M\_DQM[7..0] <M\_DQM7..0>  
 <17> M\_DQS[7..0] <M\_DQS7..0>  
 <17> M\_DQS# [7..0] <M\_DQS#7..0>



ref 139-02 recommend  
 add off page  
 Park SCL recommend pu 60.4  
 ohm to 1.5VGS 0619 update

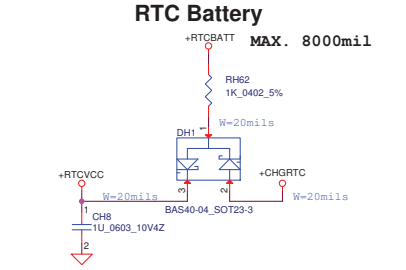
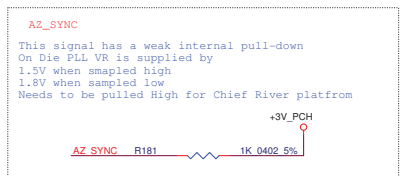


**SPI ROM FOR ME ( 4MByte )**

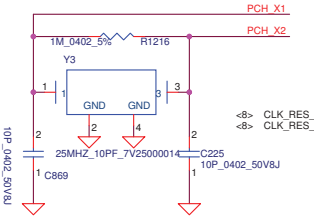
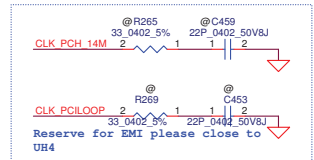
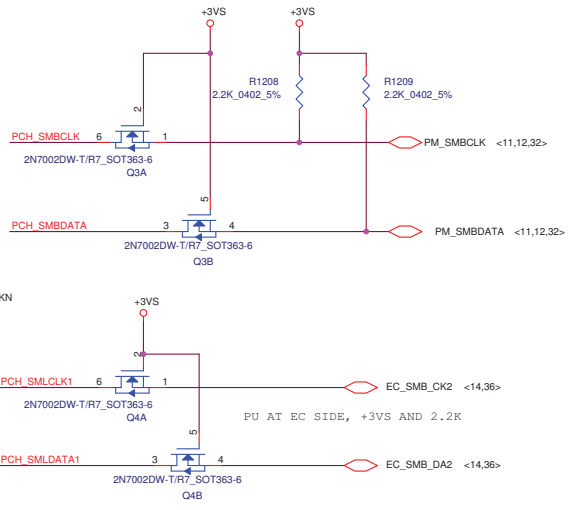
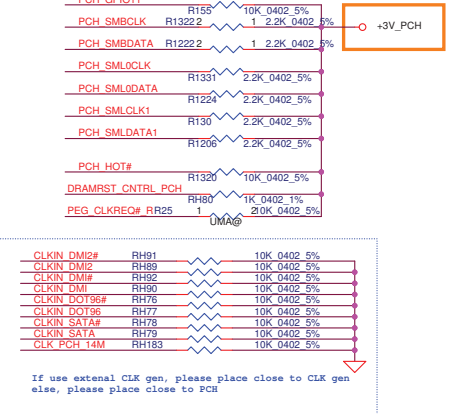
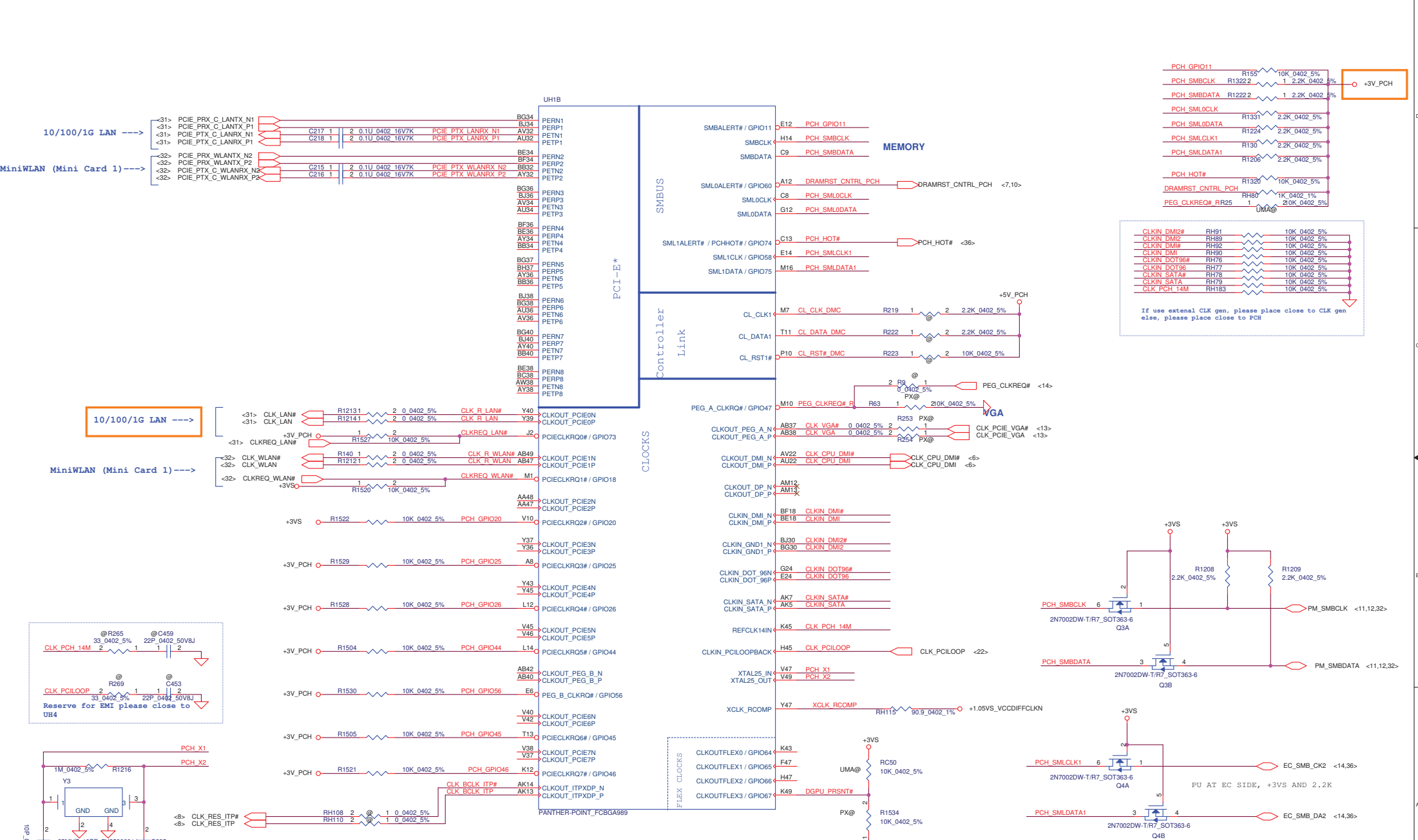


**HDA\_SDO**

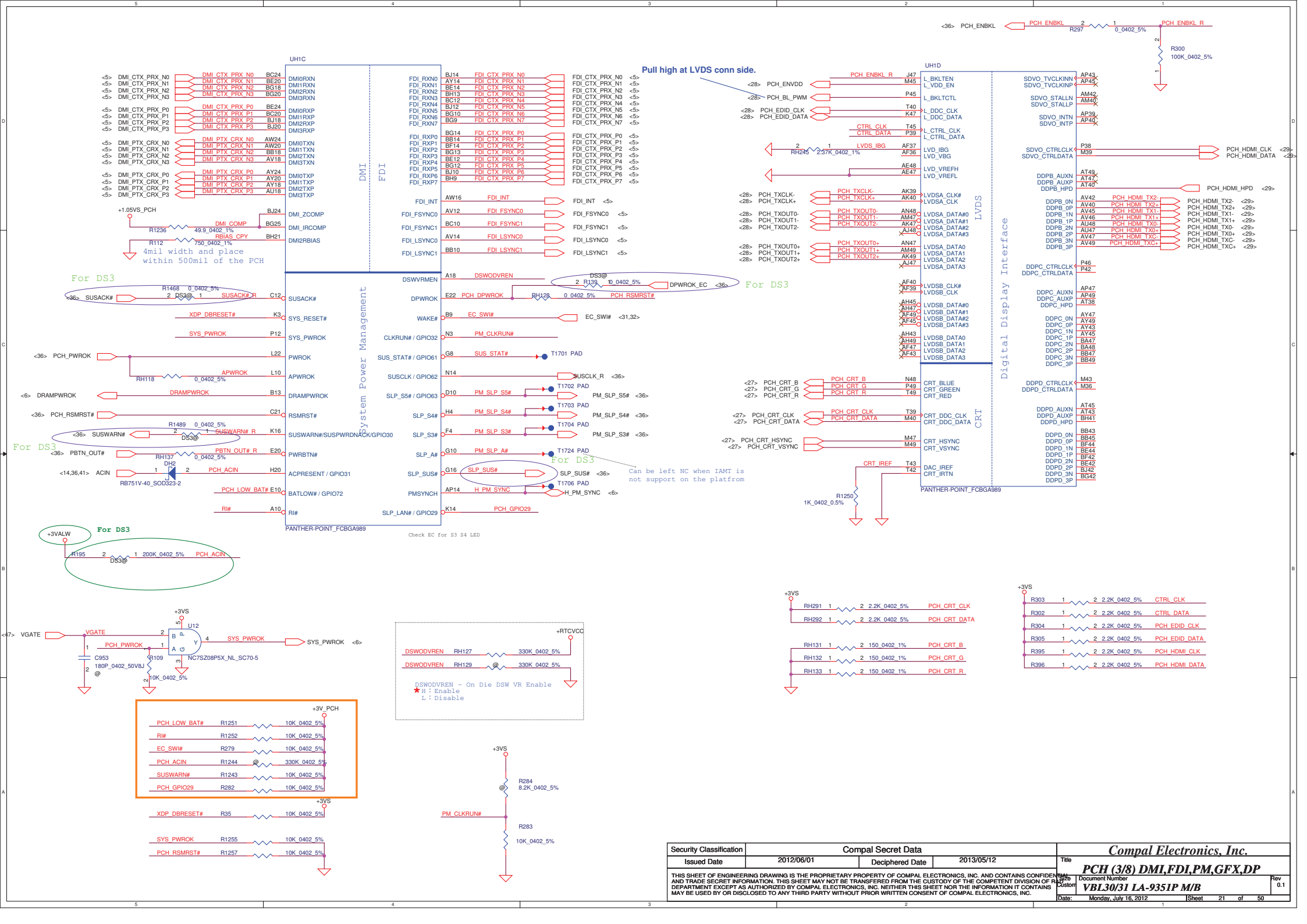
ME debug mode , this signal has a weak internal PD  
 L=>security measures defined in the Flash Descriptor will be in effect (default)  
 H=>Flash Descriptor Security will be overridden



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				Document Number	Rev
				VBL30/31 LA-931P M/B	0.1
				Date	Monday, July 16, 2012
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For DS3

For DS3

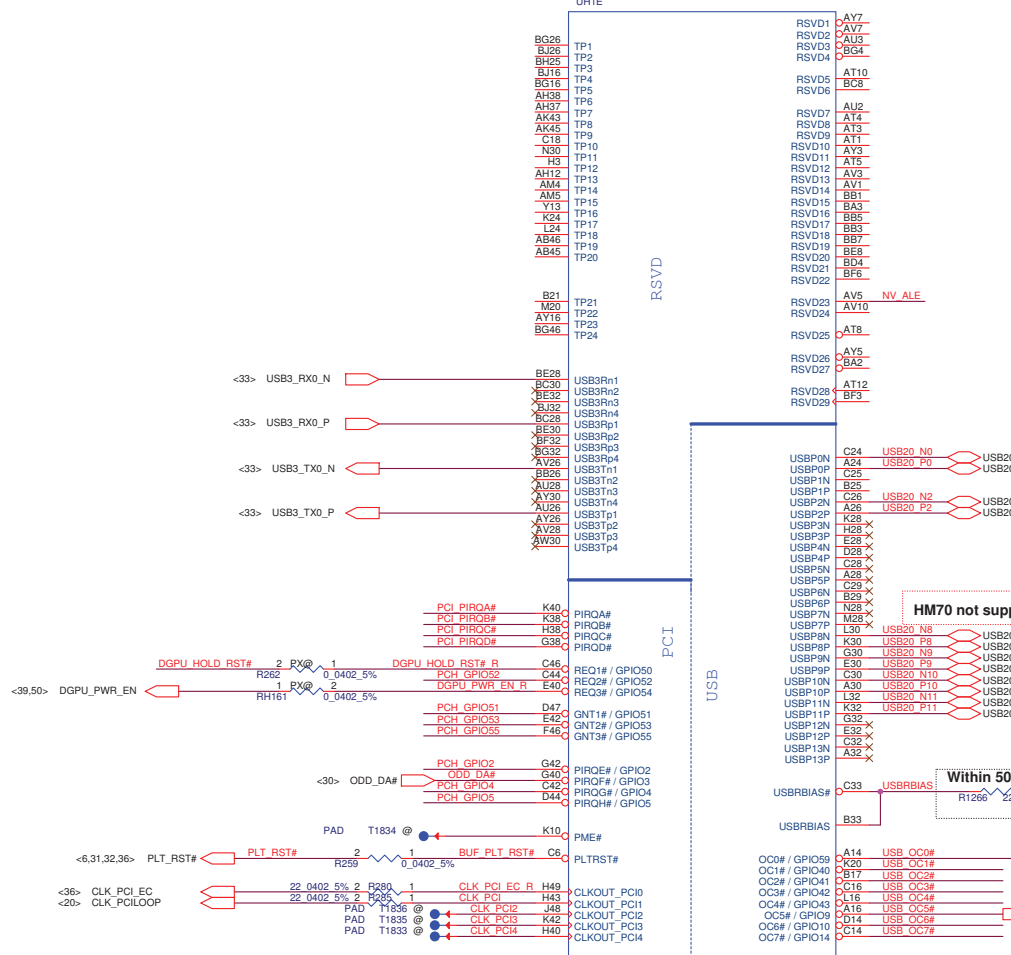
For DS3

Can be left NC when IAMT is not support on the platform

PCH_LOW_BAT#	R1251	10K	0.402 5%
RI#	R1252	10K	0.402 5%
EC_SWI#	R279	10K	0.402 5%
PCH_ACIN	R1244	330K	0.402 5%
SUSWARN#	R1243	10K	0.402 5%
PCH_GPIO29	R282	10K	0.402 5%
XDP_DBRESET#	R35	10K	0.402 5%
SYS_PWROK	R1255	10K	0.402 5%
PCH_RSMRST#	R1257	10K	0.402 5%

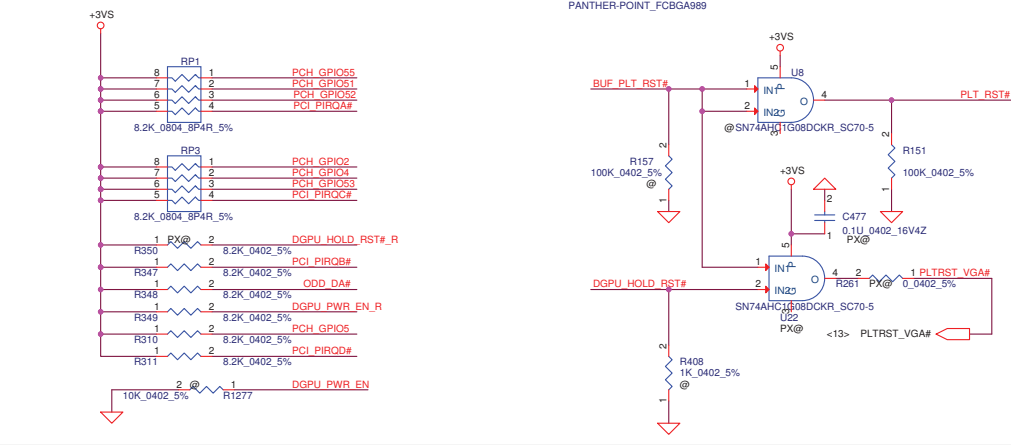
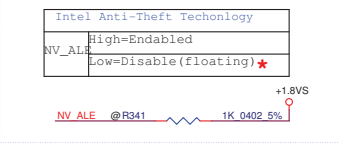
DSWODVREN - On Die DSW VR Enable  
 \* H : Enable  
 L : Disable

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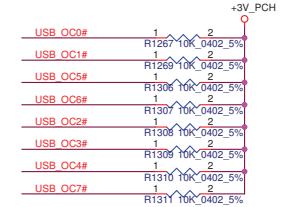


GPI019 => BBS\_BIT0  
GPI051 => BBS\_BIT1

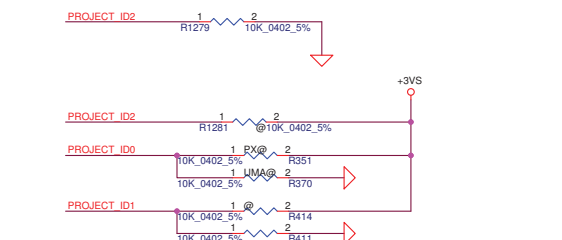
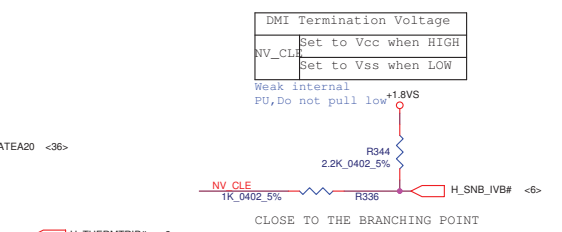
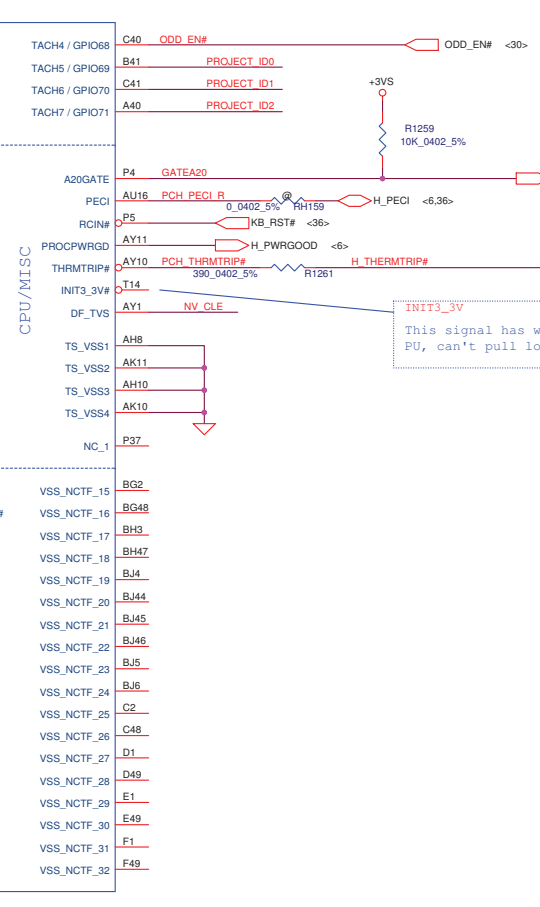
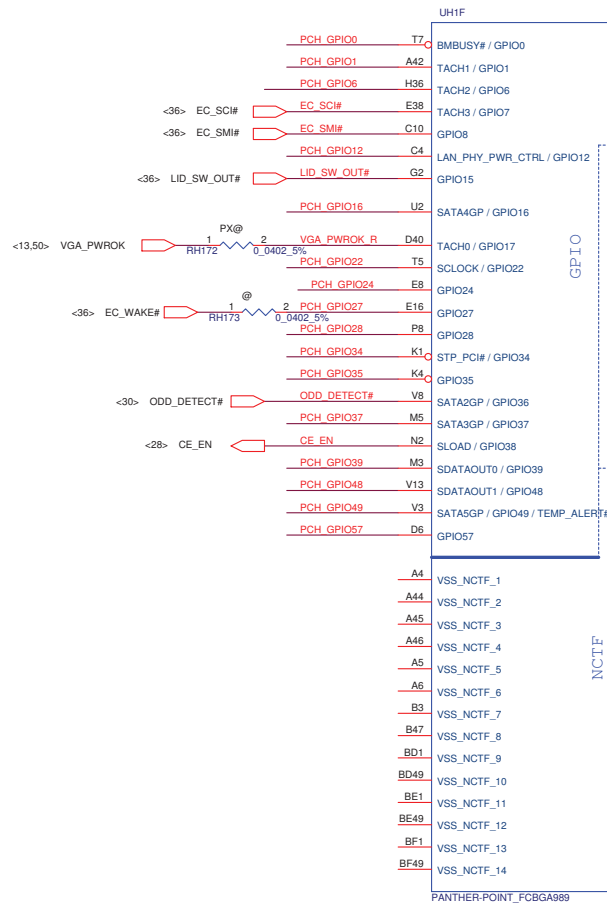
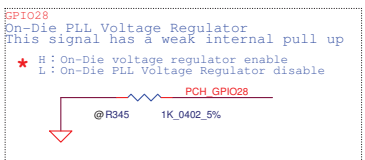
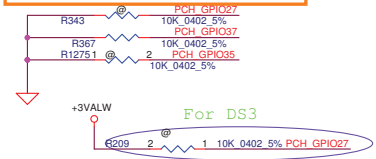
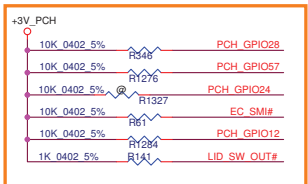
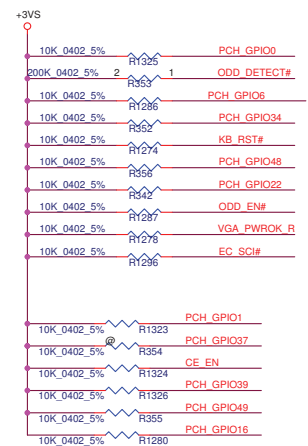
Boot BIOS Strap		
BBS_BIT0	BBS_BIT1	Boot BIOS Location
0	0	LPC
0	1	Reserved(NAND)
1	0	Reserved
1	1	SPT *



HM70 not support USB port 4,5,6,7,12,13



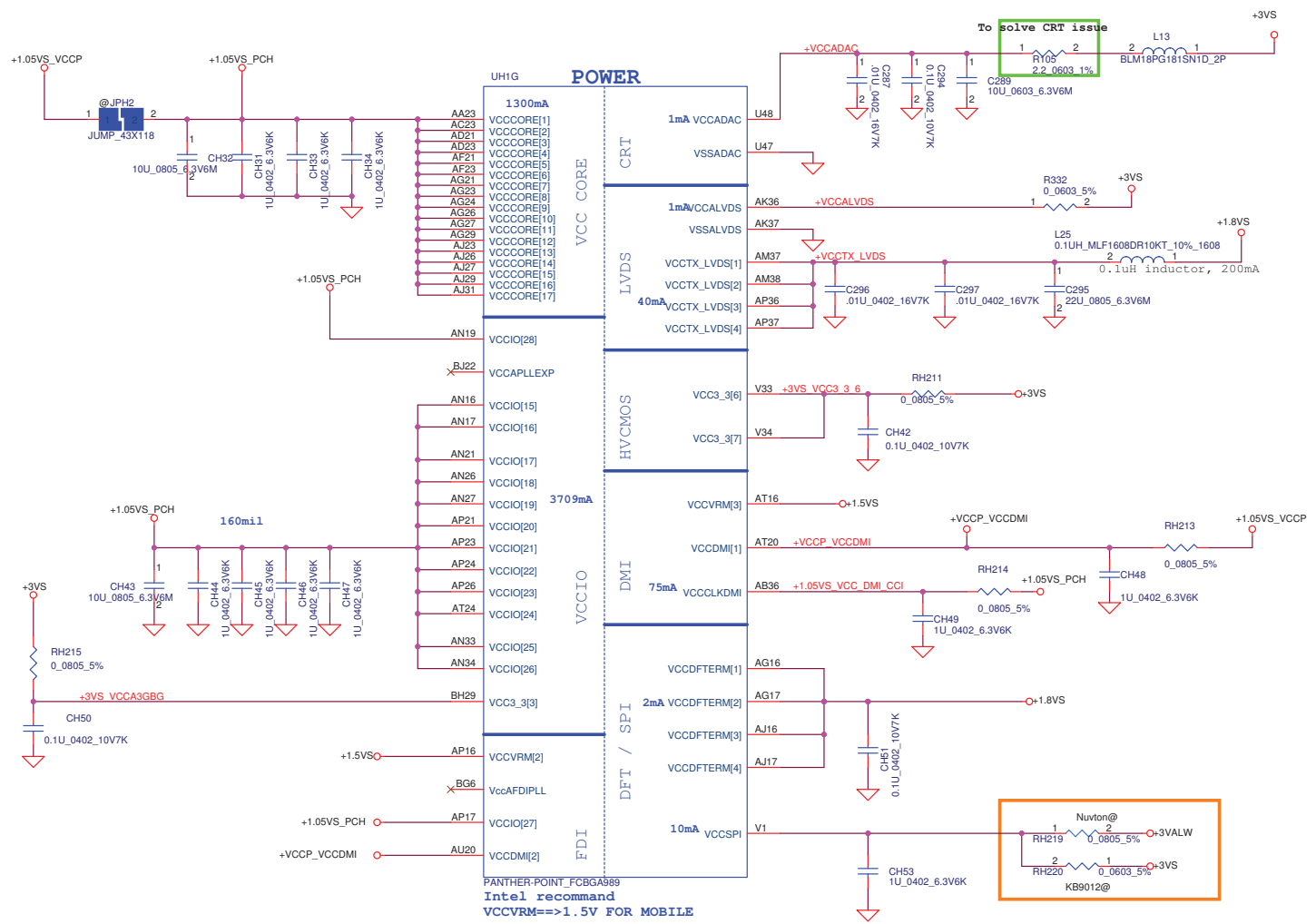
Security Classification	Compal Secret Data		Title <b>PCH (4/8) PCI, USB, NVRAM</b>
Issued Date	2012/06/01	Deciphered Date	
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Customer <b>VBL30/31 LA-9351P M/B</b>			Rev 0.1
Date:	Monday, July 16, 2012	Sheet	22 of 50



	PROJECT_ID2	PROJECT_ID1	PROJECT_ID0
VBL30 (UMA)	0	0	0
VBL31 (PX)	0	0	1

PCH\_GPIO28 needs to be connected to XDP\_FN8  
PCH\_GPIO35 needs to be connected to XDP\_FN9  
PCH\_GPIO15 needs to be connected to XDP\_FN16  
Please refer to Huron River Debug Board DG 1.2

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Issued Date	2012/06/01	Deciphered Date	2013/05/12	Compal Electronics, Inc.
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				Rev 0.1
				Sheet 23 of 50



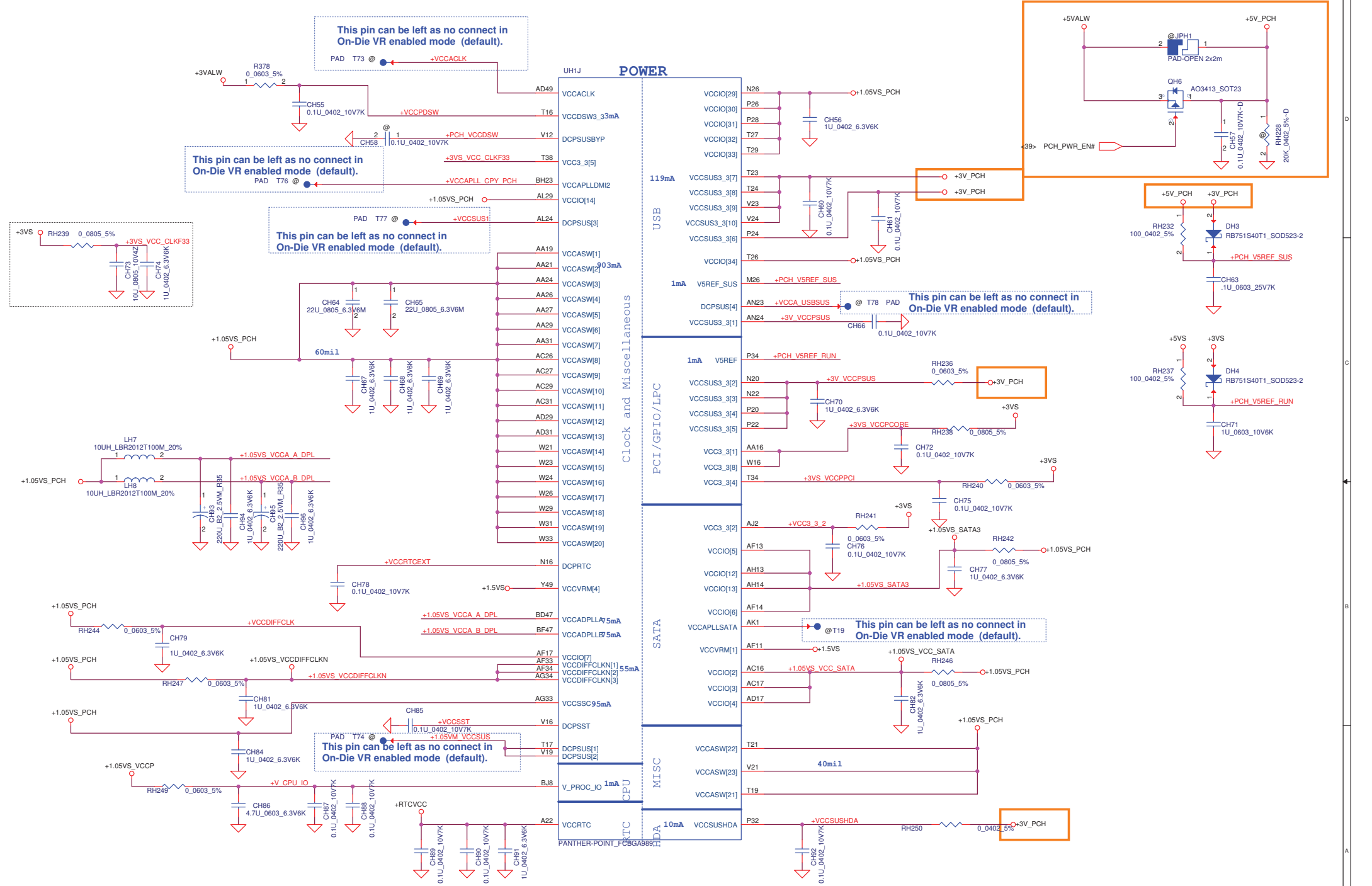
PCH Power Rail Table Refer to CPU EDS R1.5		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

PANTHER-POINT\_FCBGA89  
**Intel recommend**  
**VCCVRM==>1.5V FOR MOBILE**

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<b>Compal Electronics, Inc.</b>	
Title	<b>PCH (6/8) PWR</b>
Document Number	<b>VBL30/31 LA-9351P M/B</b>
Date	Monday, July 16, 2012
Sheet	24 of 50

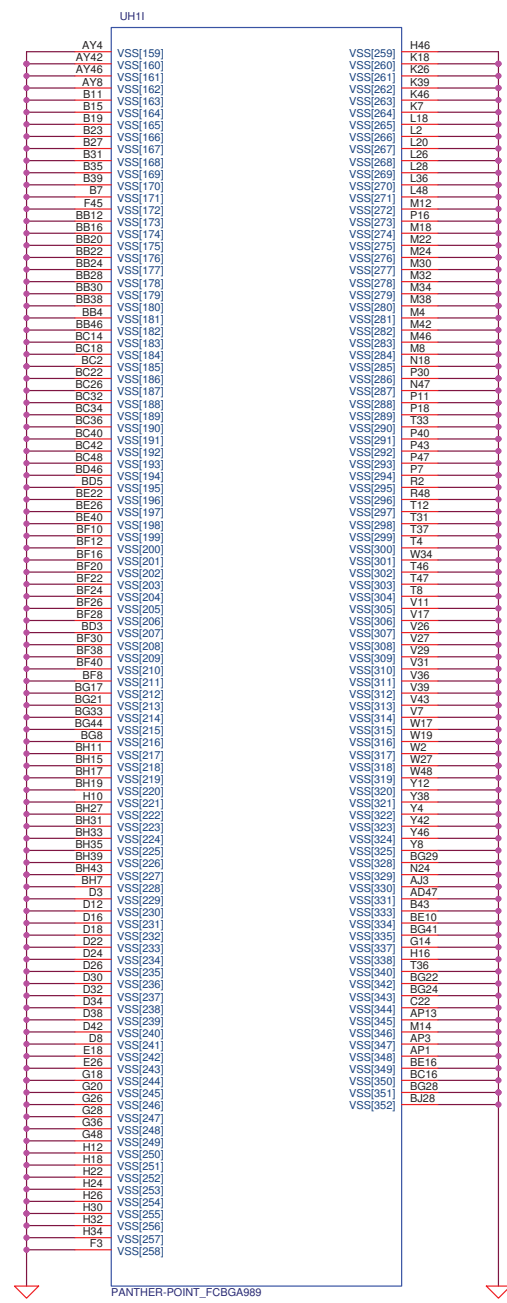
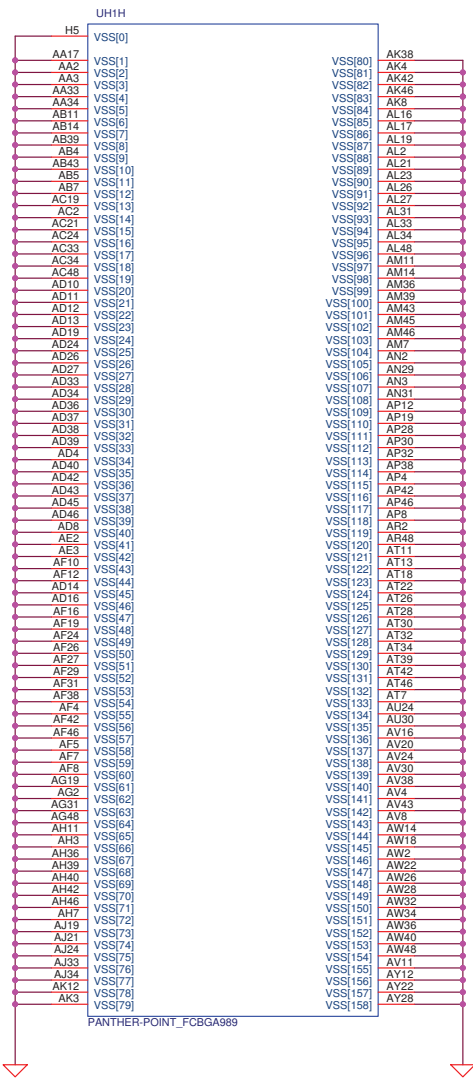




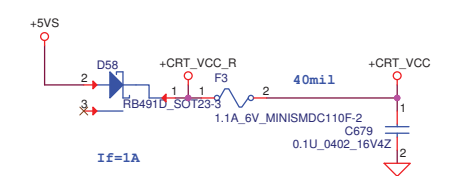
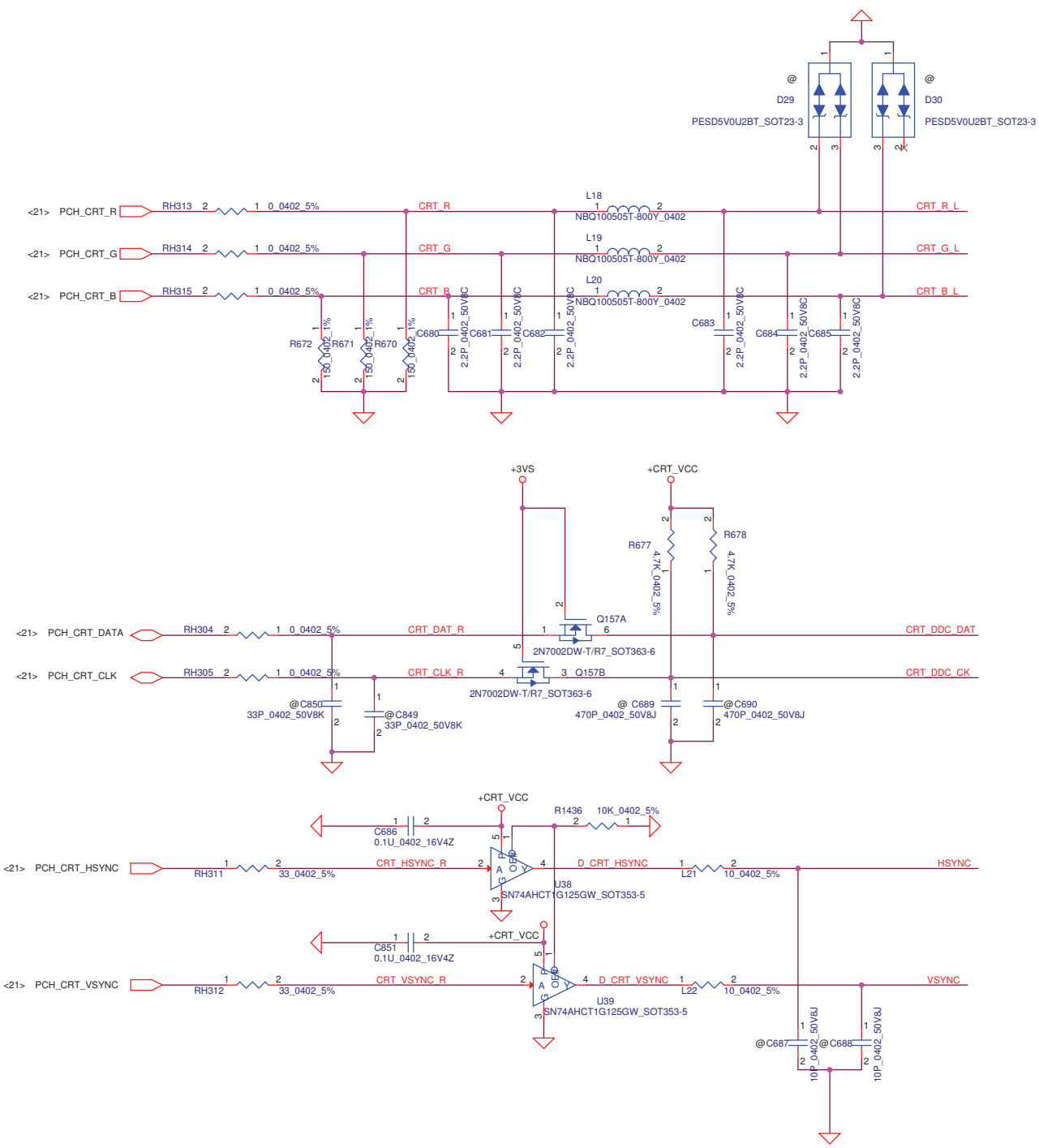
Security Classification	Compal Secret Data	
Issued Date	2012/06/01	Deciphered Date
		2013/05/12

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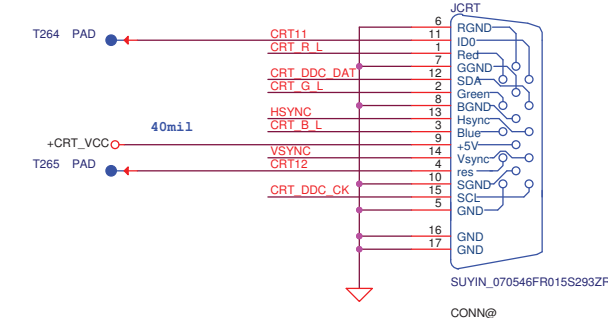
Compal Electronics, Inc.	
Title	<b>PCH (7/8) PWR</b>
Customer	<b>VBL30/31 LA-9351P M/B</b>
Date	Monday, July 16, 2012
Sheet	25 of 50
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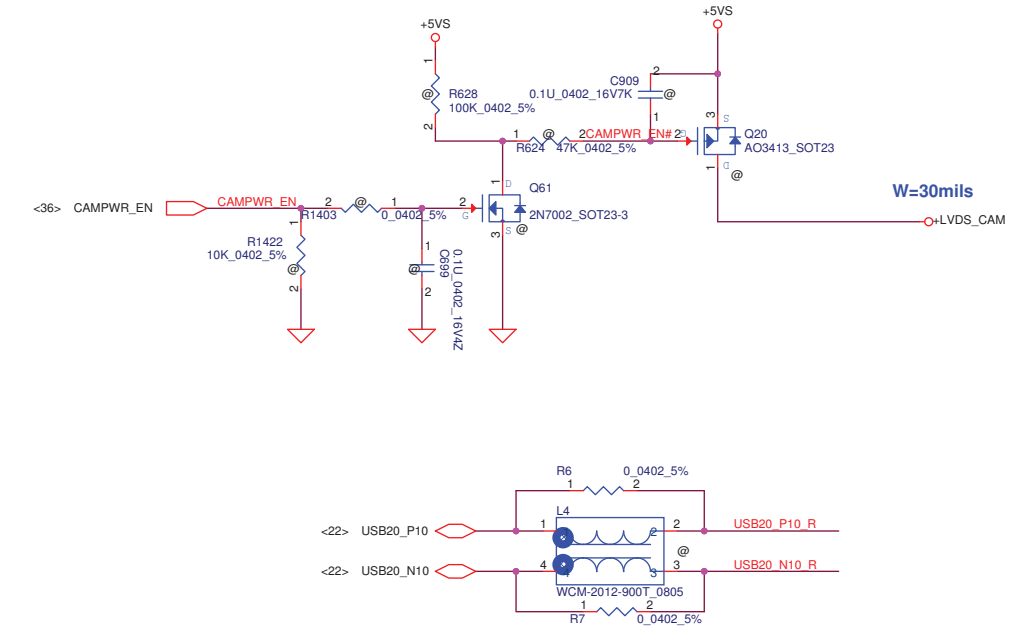
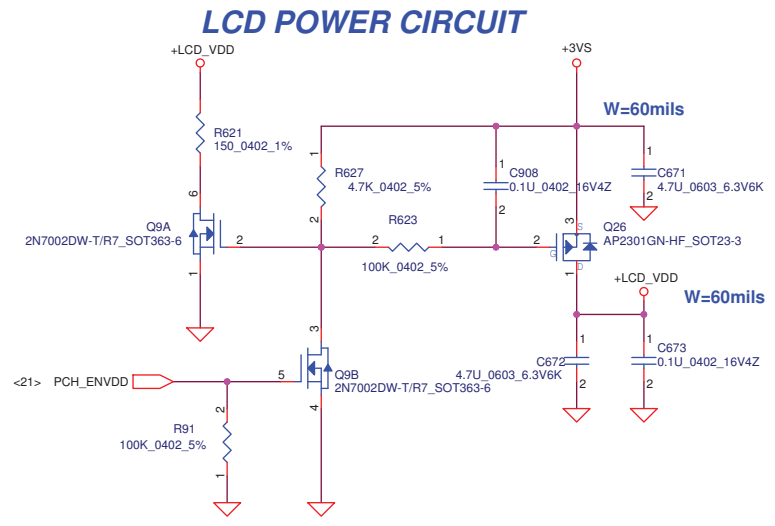
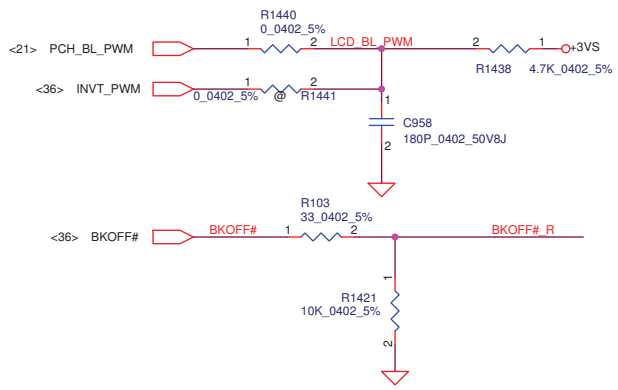
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title
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				Rev 0.1
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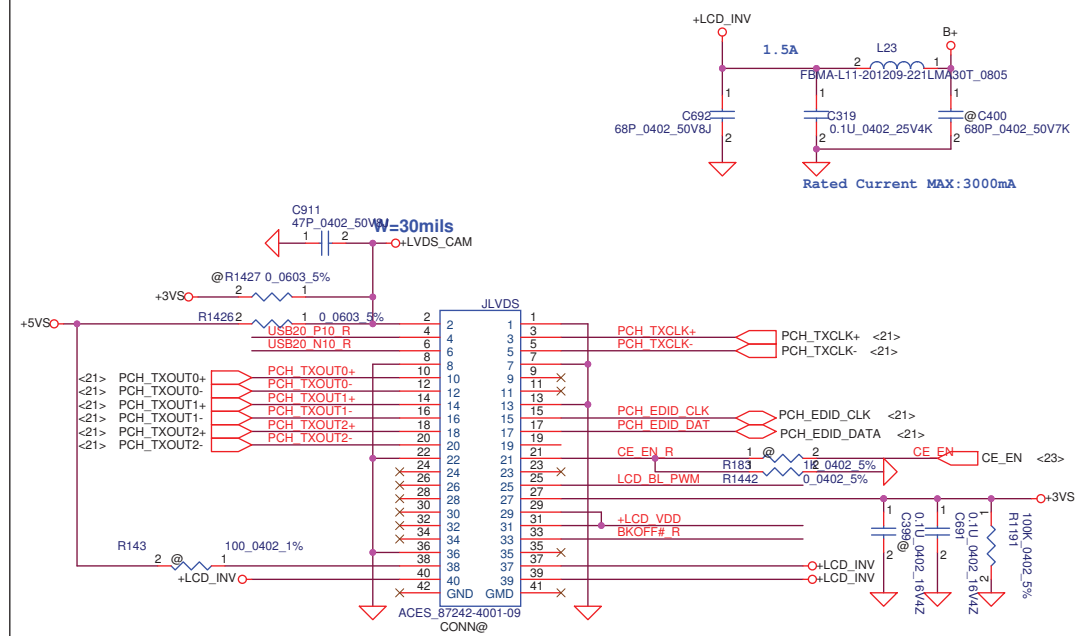
### CRT CONNECTOR



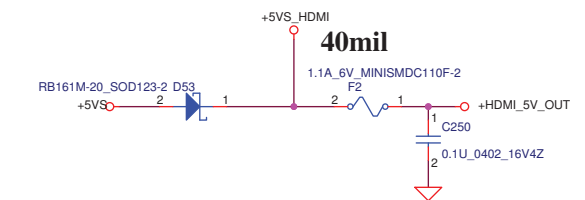
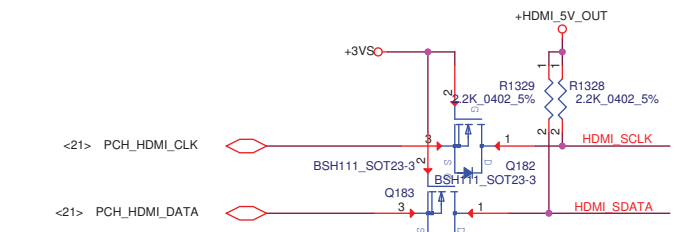
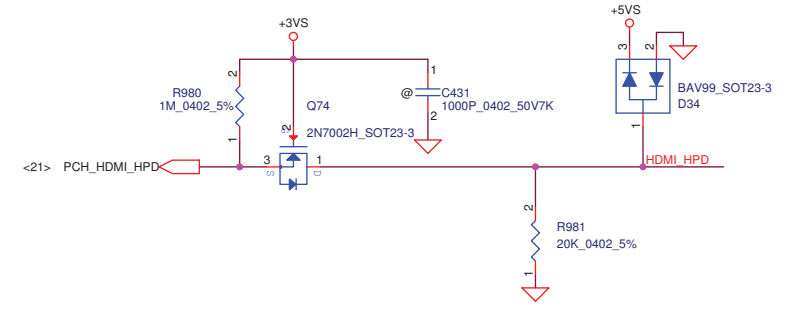
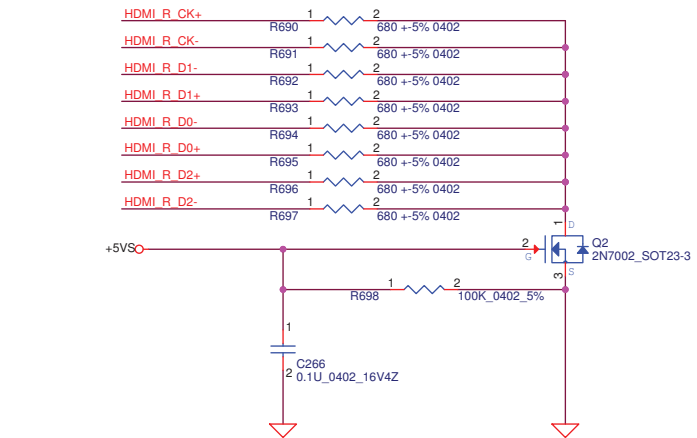
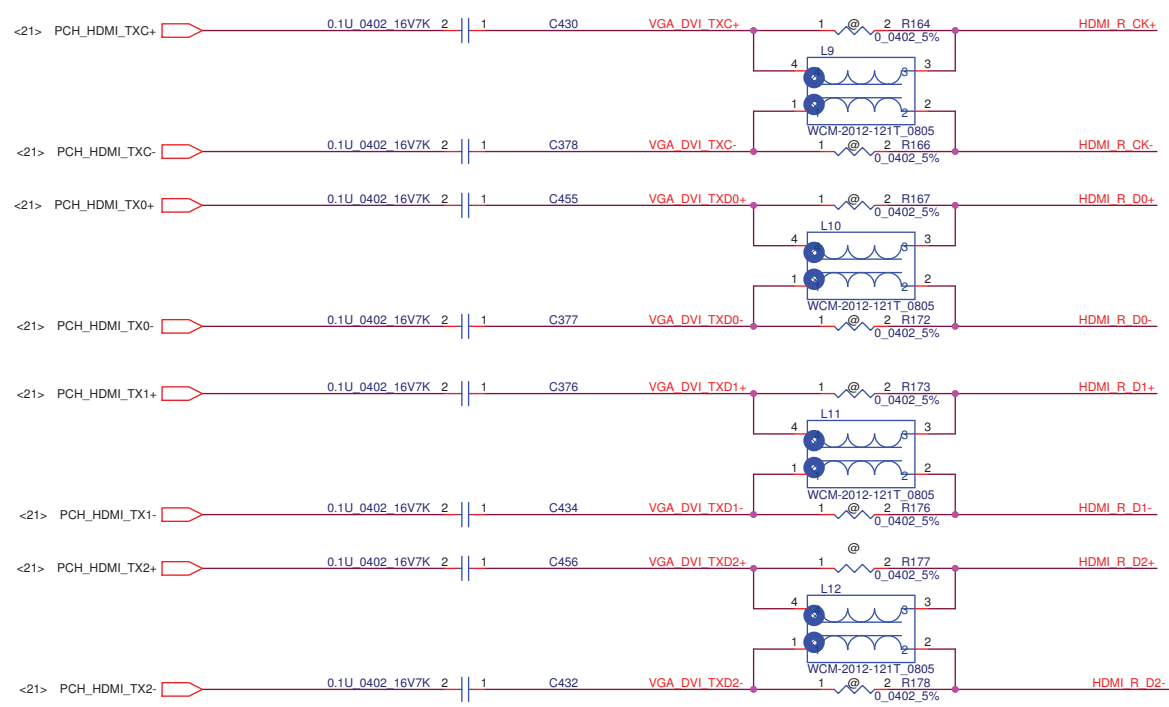
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>CRT</b>	
Issued Date	2012/06/01	Deciphered Date	2013/05/12		
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Date: Monday, July 16, 2012				Sheet 27	of 50



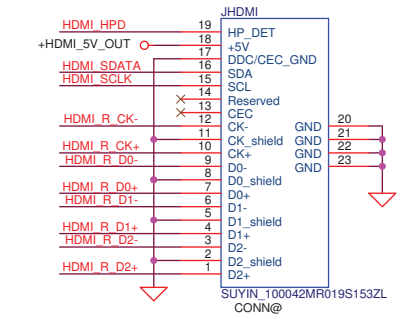
### LCD/PANEL BD. Conn.



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Issued Date	2012/06/01	Deciphered Date	2013/05/12	LVDS			
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Date	Monday, July 16, 2012	Sheet	28	of	50	Rev	0.1

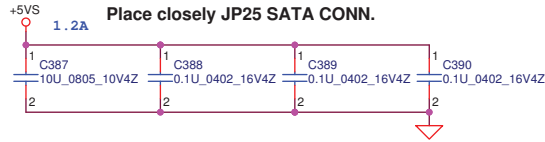


### HDMI Connector

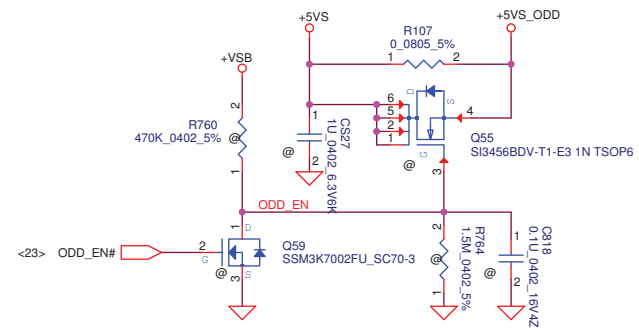
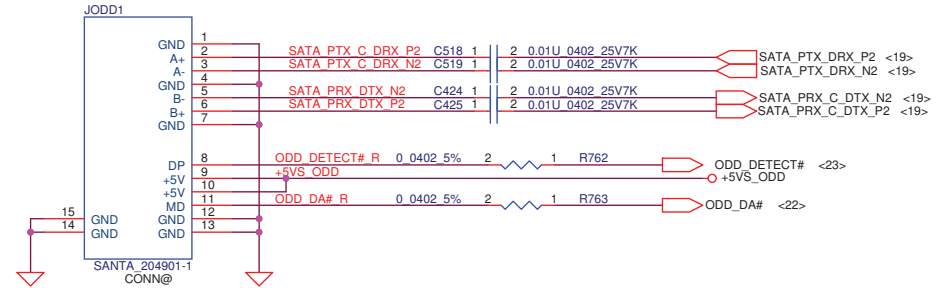
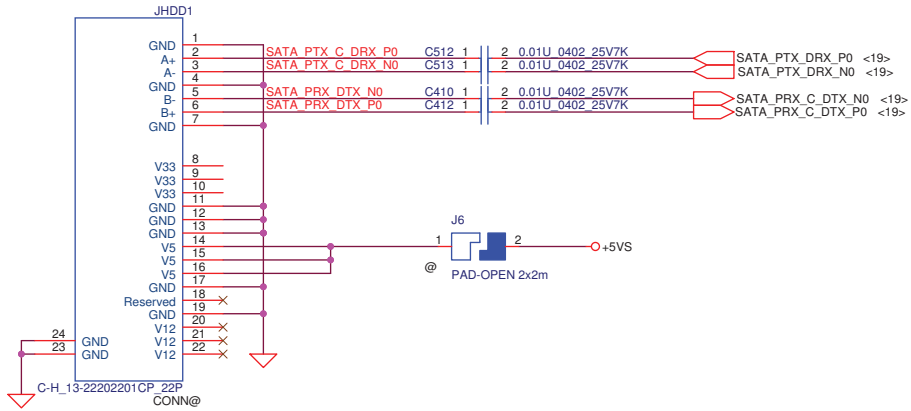
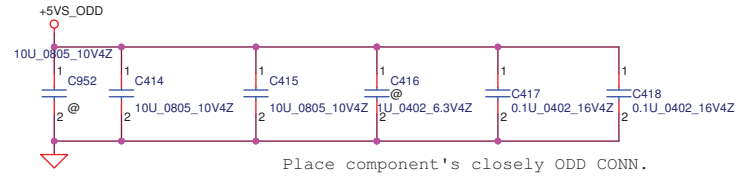


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Issued Date	2012/06/01	Deciphered Date	2013/05/12	HDMI Connector			
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Date:	Monday, July 16, 2012	Sheet	29	of	50		

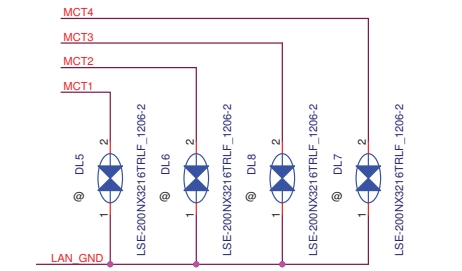
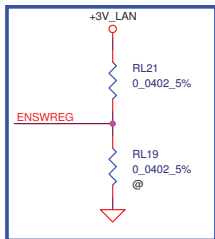
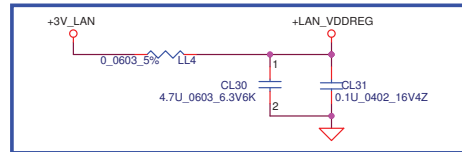
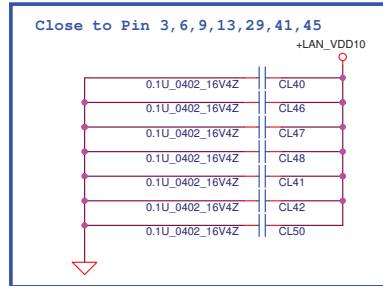
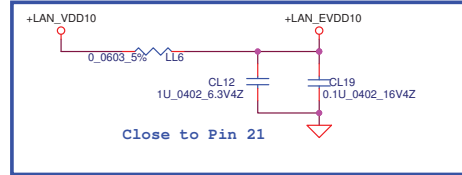
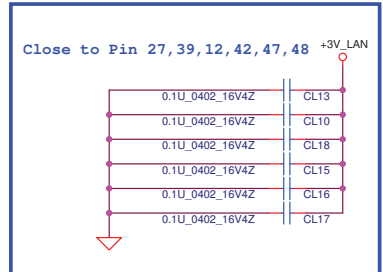
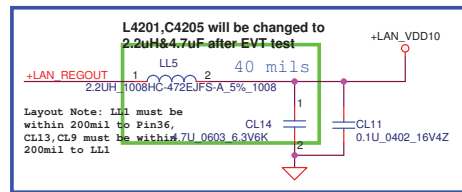
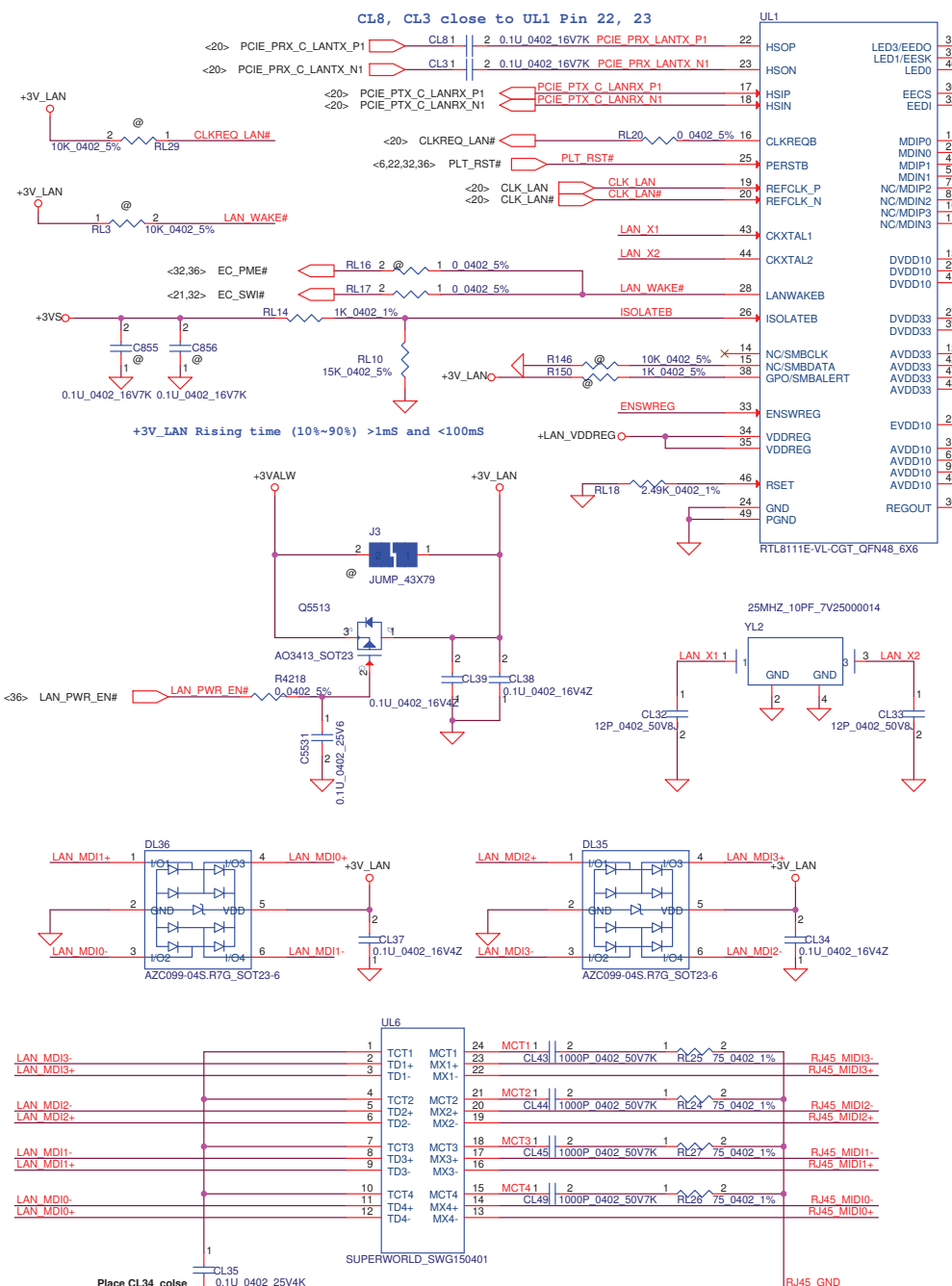
### SATA HDD1 Conn.



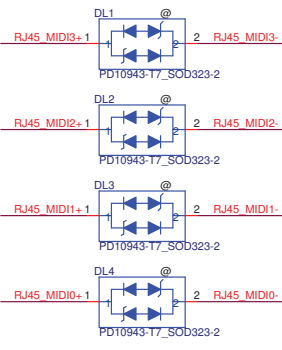
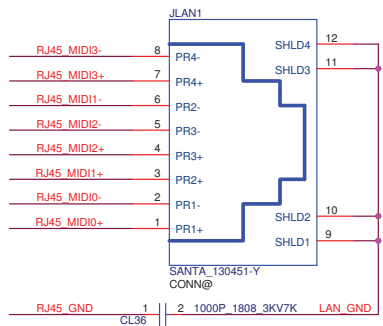
### SATA ODD Conn



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**LAN Conn.**

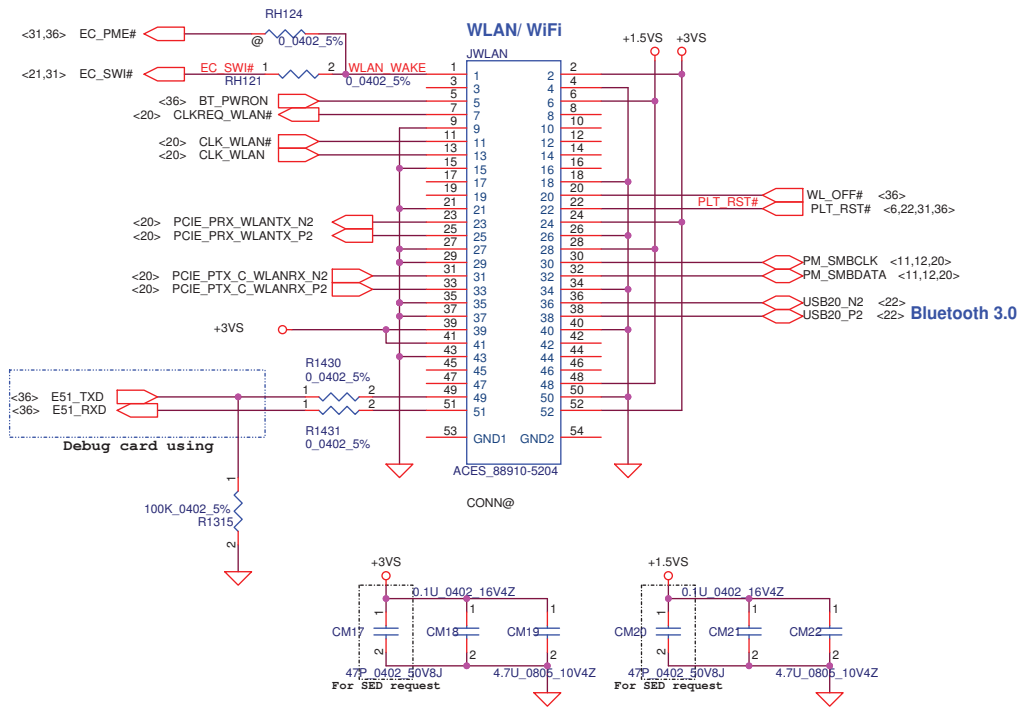


Security Classification	Compal Secret Data	
Issued Date	2012/06/01	Deciphered Date
		2011/05/17

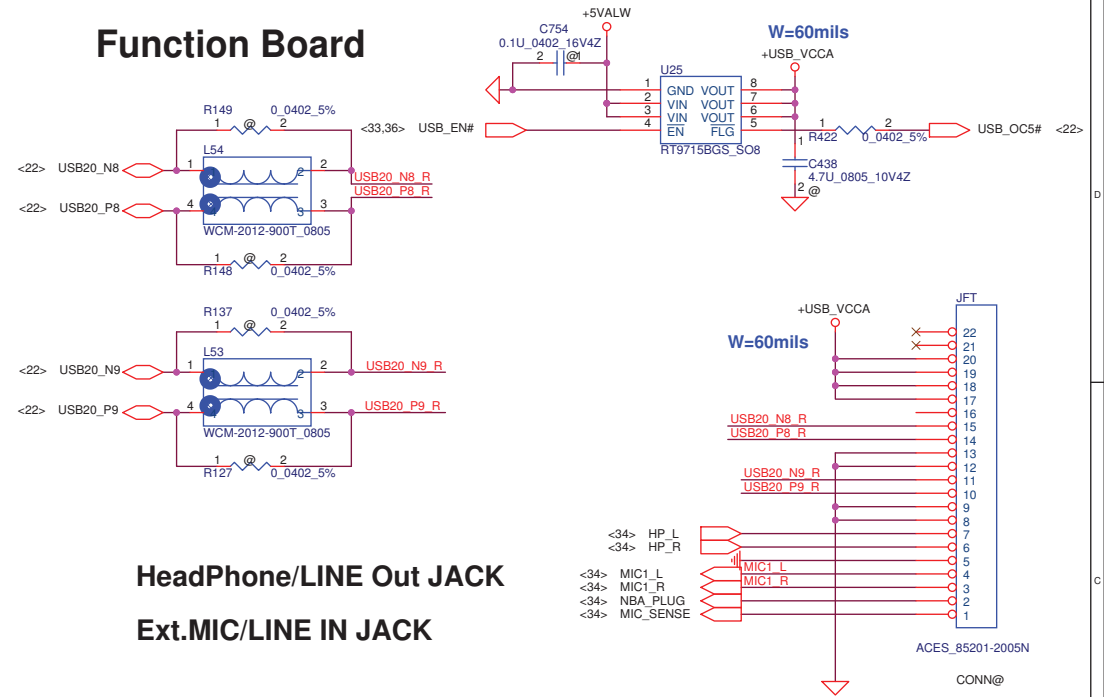
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Part Number		<b>RTL8111F</b>	
Customer	Document Number	<b>VBL30/31 LA-9351P M/B</b>	
Date:	Monday, July 16, 2012	Sheet	31 of 50

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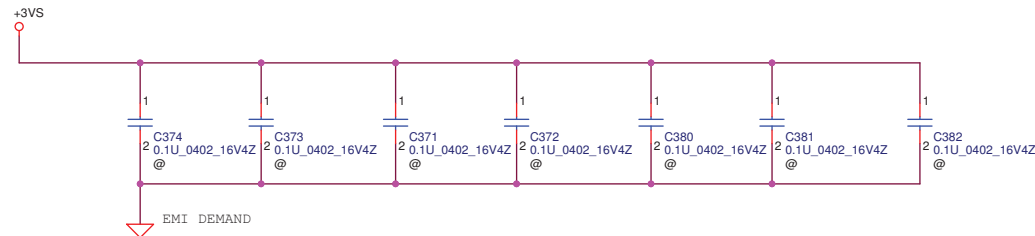
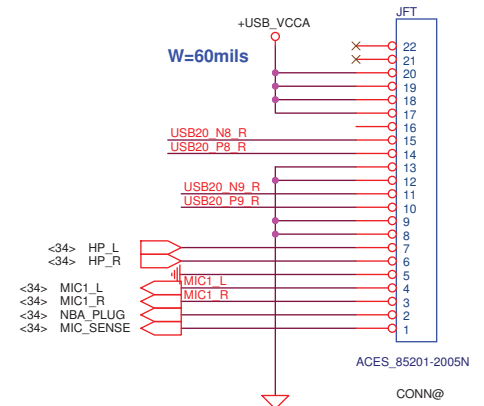
# Slot 1 Half PCIe Mini Card-WLAN & BT3.0



# Function Board



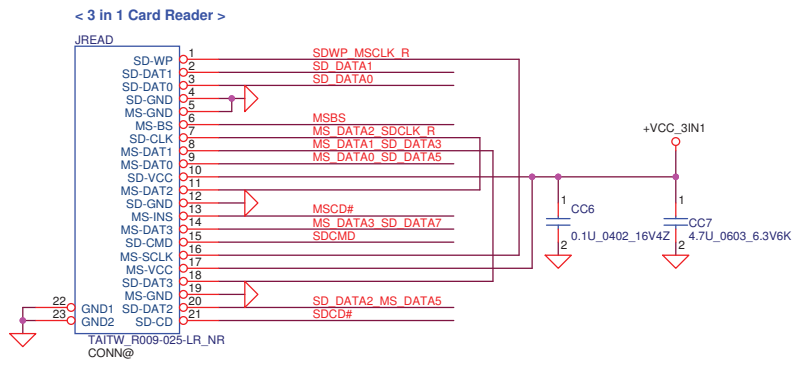
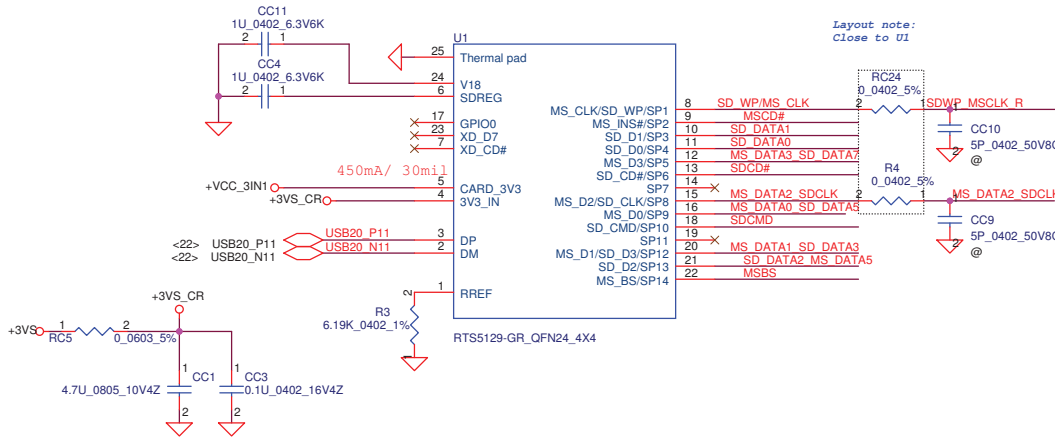
# HeadPhone/LINE Out JACK Ext.MIC/LINE IN JACK



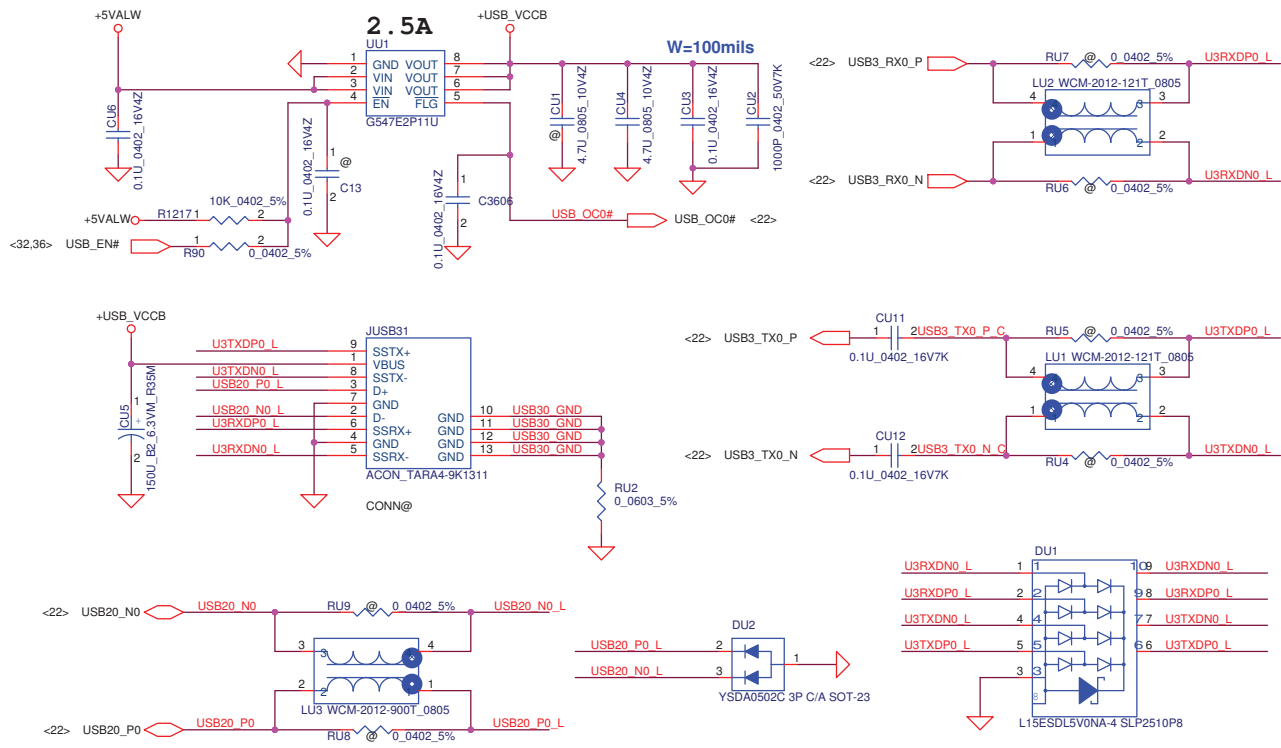
Security Classification		Compal Secret Data		Title	
Issued Date	2012/06/01	Deciphered Date	2013/05/12	WLAN/USB	
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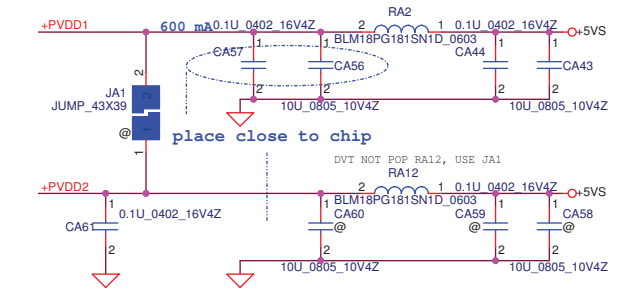
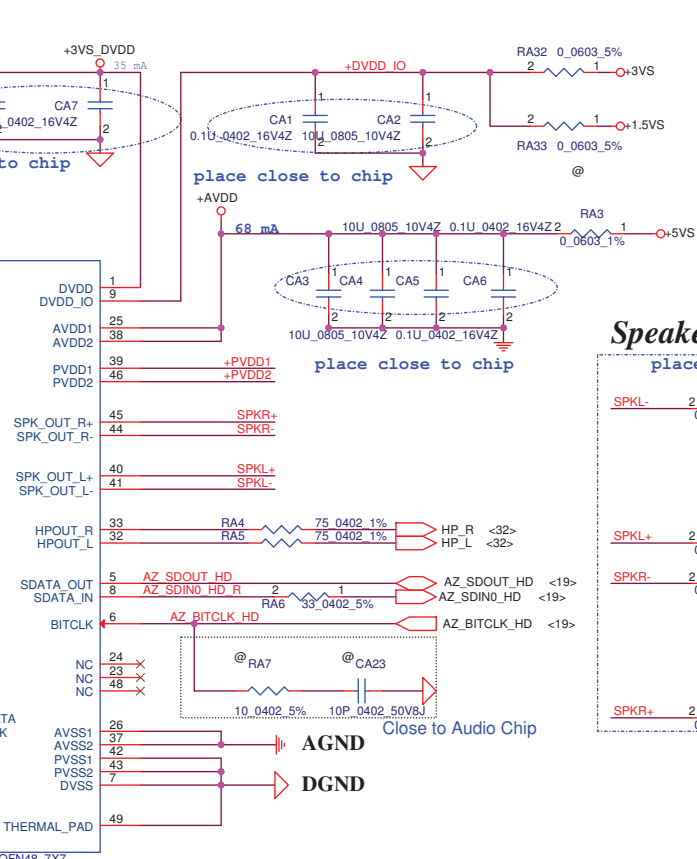
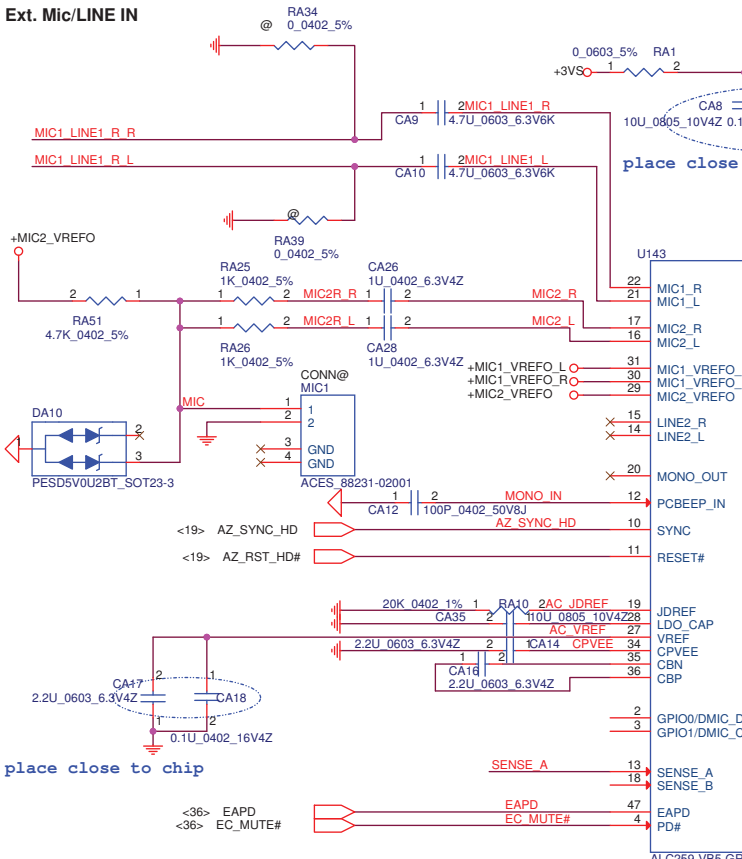
# Card Reader



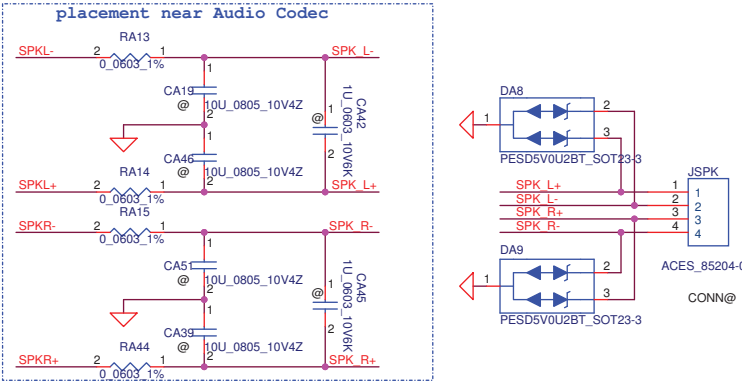
# USB3.0 Port



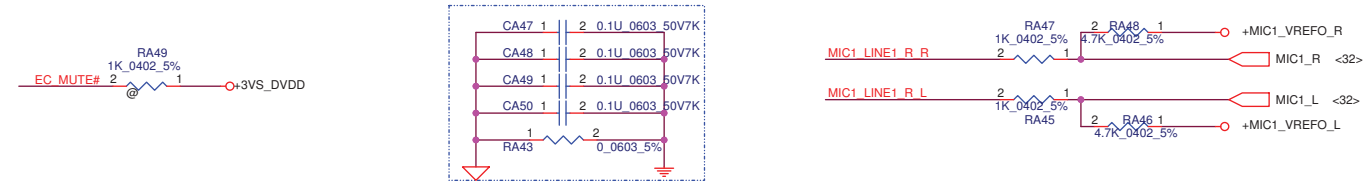
Security Classification	Compal Secret Data		Title	
Issued Date	2012/06/01	Deciphered Date	2013/05/12	USB-Card Reader-RTS5129
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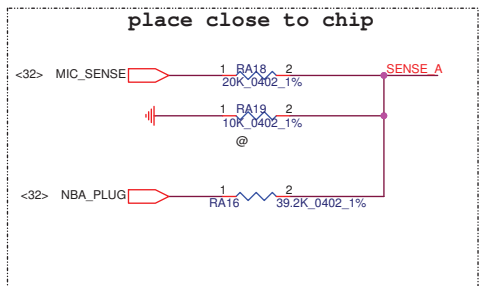
**Speaker Connector**



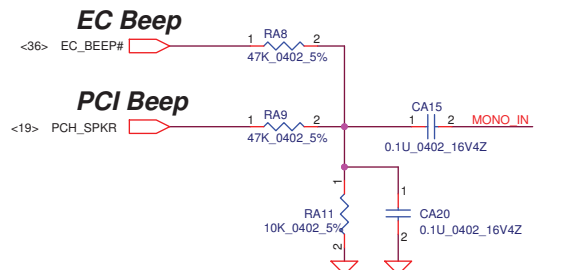
**Ext. MIC/LINE IN JACK**



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
SENSE B	5.1K	PORT-D (PIN 35, 36)	SPK out
	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
5.1K	PORT-I (PIN 32, 33)	Headphone out	



**Beep sound**

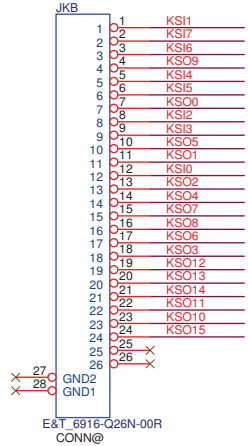


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Document Number				Rev	
VBL30/31 LA-9351P M/B				0.1	
Date: Monday, July 16, 2012				Sheet 34 of 50	

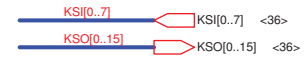
# KEYBOARD CONN.

For EMC

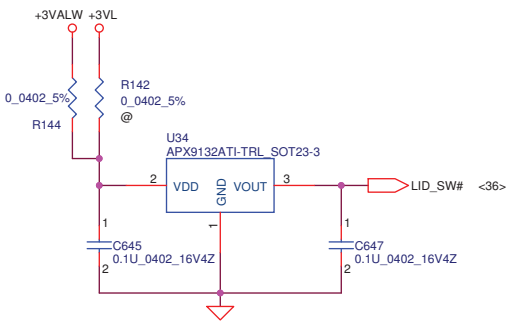
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KSO11	2	100P_0402_50V8J
C804	2	100P_0402_50V8J
KSO12	1	100P_0402_50V8J
C805	1	100P_0402_50V8J
KSO15	2	100P_0402_50V8J
C807	2	100P_0402_50V8J
KSI7	1	100P_0402_50V8J
C808	1	100P_0402_50V8J
KSI2	2	100P_0402_50V8J
C810	2	100P_0402_50V8J
KSI3	1	100P_0402_50V8J
C811	1	100P_0402_50V8J
KSI4	2	100P_0402_50V8J
C812	2	100P_0402_50V8J
KSI0	1	100P_0402_50V8J
C813	1	100P_0402_50V8J
KSI5	2	100P_0402_50V8J
C814	2	100P_0402_50V8J
KSI6	1	100P_0402_50V8J
C815	1	100P_0402_50V8J
KSI1	2	100P_0402_50V8J
C816	2	100P_0402_50V8J
KSO2	1	100P_0402_50V8J
C793	1	100P_0402_50V8J
KSO1	2	100P_0402_50V8J
C790	2	100P_0402_50V8J
KSO0	1	100P_0402_50V8J
C791	1	100P_0402_50V8J
KSO4	2	100P_0402_50V8J
C792	2	100P_0402_50V8J
KSO3	1	100P_0402_50V8J
C795	1	100P_0402_50V8J
KSO5	2	100P_0402_50V8J
C796	2	100P_0402_50V8J
KSO14	1	100P_0402_50V8J
C797	1	100P_0402_50V8J
KSO6	2	100P_0402_50V8J
C798	2	100P_0402_50V8J
KSO7	1	100P_0402_50V8J
C799	1	100P_0402_50V8J
KSO13	2	100P_0402_50V8J
C800	2	100P_0402_50V8J
KSO8	1	100P_0402_50V8J
C801	1	100P_0402_50V8J
KSO9	2	100P_0402_50V8J
C802	2	100P_0402_50V8J



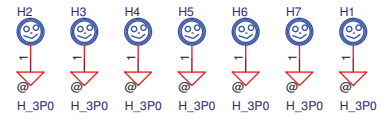
13.3" and 14"



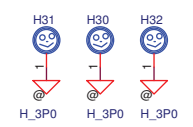
# Lid SW



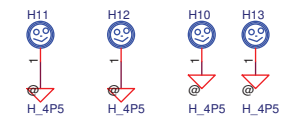
# Screw Hole



# Break hole



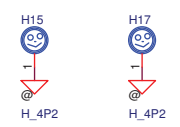
# CPU



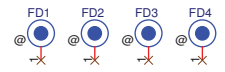
# JWLAN



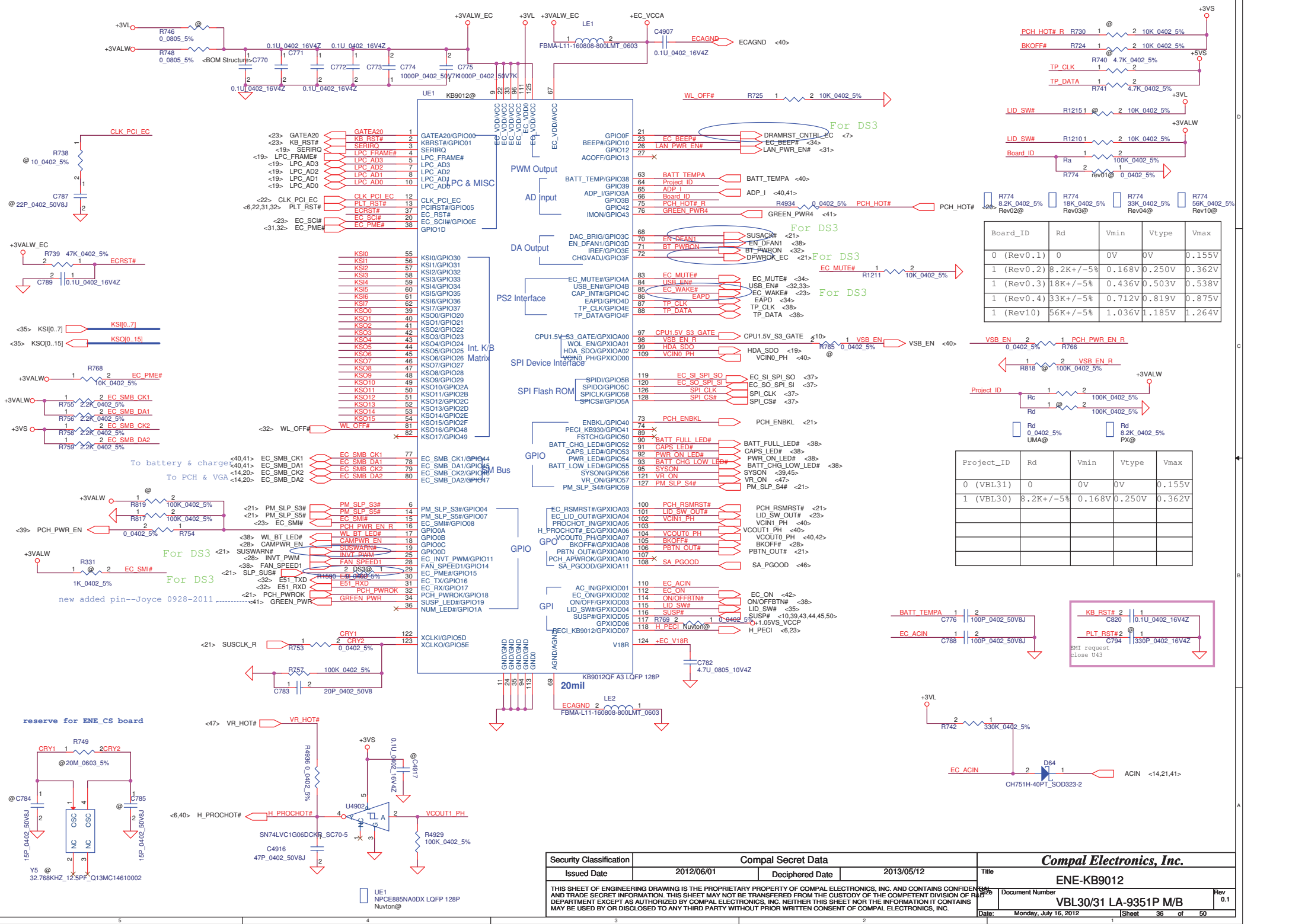
# VGA



# PCB Federal Mark PAD



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Pin	Signal	Component
55	KSIO/GPIO30	KSIO
56	KS11/GPIO31	KS11
57	KS12/GPIO32	KS12
58	KS13/GPIO33	KS13
59	KS14/GPIO34	KS14
60	KS15/GPIO35	KS15
61	KS16/GPIO36	KS16
62	KS17/GPIO37	KS17
63	KS00/GPIO20	KS00
64	KS01/GPIO21	KS01
65	KS02/GPIO22	KS02
66	KS03/GPIO23	KS03
67	KS04/GPIO24	KS04
68	KS05/GPIO25	KS05
69	KS06/GPIO26	KS06
70	KS07/GPIO27	KS07
71	KS08/GPIO28	KS08
72	KS09/GPIO29	KS09
73	KS10/GPIO30	KS10
74	KS11/GPIO31	KS11
75	KS12/GPIO32	KS12
76	KS13/GPIO33	KS13
77	KS14/GPIO34	KS14
78	KS15/GPIO35	KS15
79	KS16/GPIO36	KS16
80	KS17/GPIO37	KS17

Pin	Signal	Component
77	EC SMB CK1	EC SMB CK1
78	EC SMB DA1	EC SMB DA1
79	EC SMB CK2	EC SMB CK2
80	EC SMB DA2	EC SMB DA2
6	PM_SLP_S3#	PM_SLP_S3#
14	PM_SLP_S5#	PM_SLP_S5#
15	EC_SMI#	EC_SMI#
16	PCH_PWR_EN_R	PCH_PWR_EN_R
17	WL_BT_LED#	WL_BT_LED#
18	CAMPWR_EN	CAMPWR_EN
19	SUSWARN#	SUSWARN#
25	INVT_PWM	INVT_PWM
28	FAN_SPEED1	FAN_SPEED1
29	FAN_SPEED2	FAN_SPEED2
30	E51_TXD	E51_TXD
31	E51_RXD	E51_RXD
32	PCH_PWROK	PCH_PWROK
34	GREEN_PWR	GREEN_PWR
36	NUM_LED#	NUM_LED#
122	XCLKI/GPIO5D	XCLKI/GPIO5D
123	XCLKO/GPIO5E	XCLKO/GPIO5E

Board_ID	Rd	Vmin	Vtype	Vmax
0 (Rev0.1)	0	0V	0V	0.155V
1 (Rev0.2)	8.2K+/-5%	0.168V	0.250V	0.362V
1 (Rev0.3)	18K+/-5%	0.436V	0.503V	0.538V
1 (Rev0.4)	33K+/-5%	0.712V	0.819V	0.875V
1 (Rev1.0)	56K+/-5%	1.036V	1.185V	1.264V

Project_ID	Rd	Vmin	Vtype	Vmax
0 (VBL31)	0	0V	0V	0.155V
1 (VBL30)	8.2K+/-5%	0.168V	0.250V	0.362V

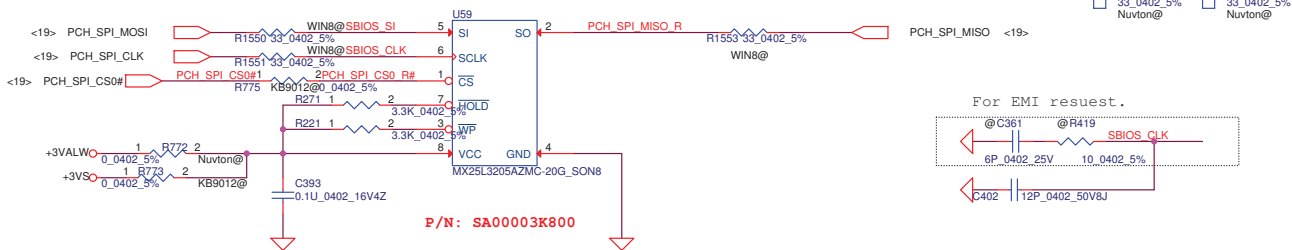
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# BIOS Bus switch

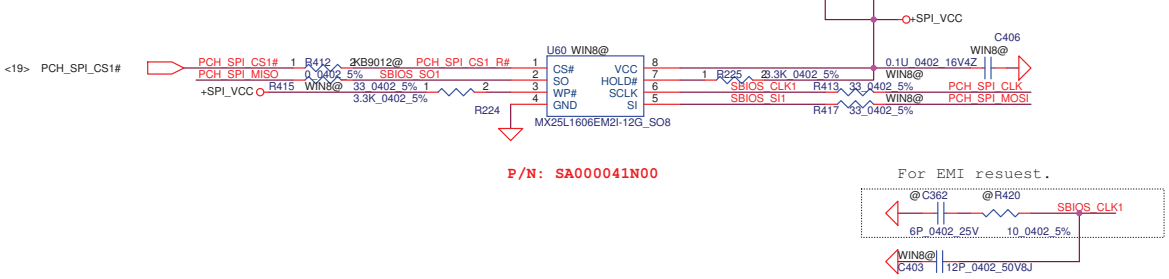
<36> EC\_SI SPI SO R266 1 Nuvton@23 0402 5%PCH\_SPI\_MISO R  
 <36> EC\_SO SPI SI R267 1 Nuvton@23 0402 5%SBIOS\_SI  
 <36> SPI\_CLK R268 1 Nuvton@23 0402 5%SBIOS\_CLK  
 <36> SPI\_CS# R270 1 Nuvton@23 0402 5%PCH\_SPI\_CS0\_R#

R1550 0\_0402 5% R1551 0\_0402 5% R1553 0\_0402 5%  
 NOW8@ NOW8@ NOW8@  
**When use single ROM, R1550 R1551 R1553use 0 ohm.**

## BIOS SPI Flash (4MByte\*1)

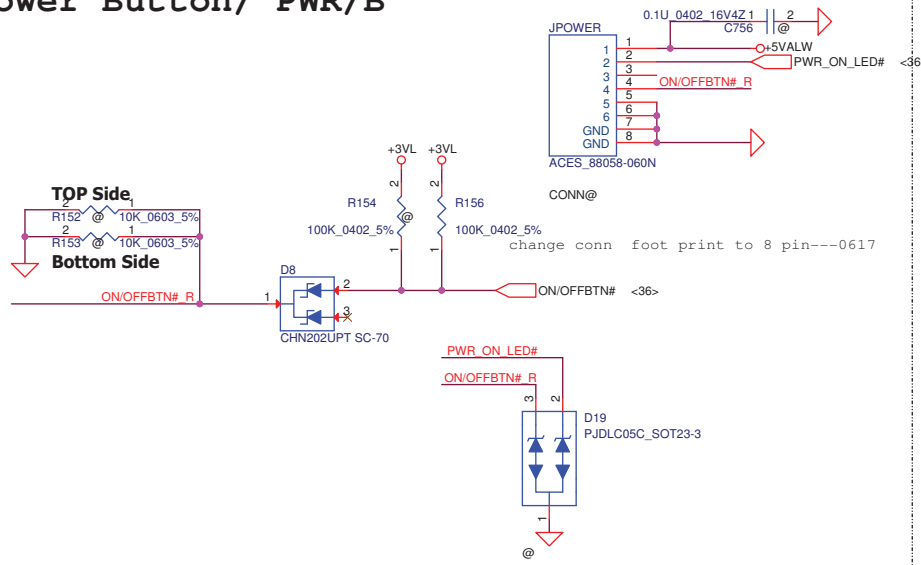


## BIOS SPI Flash (2MByte\*1) For Win8

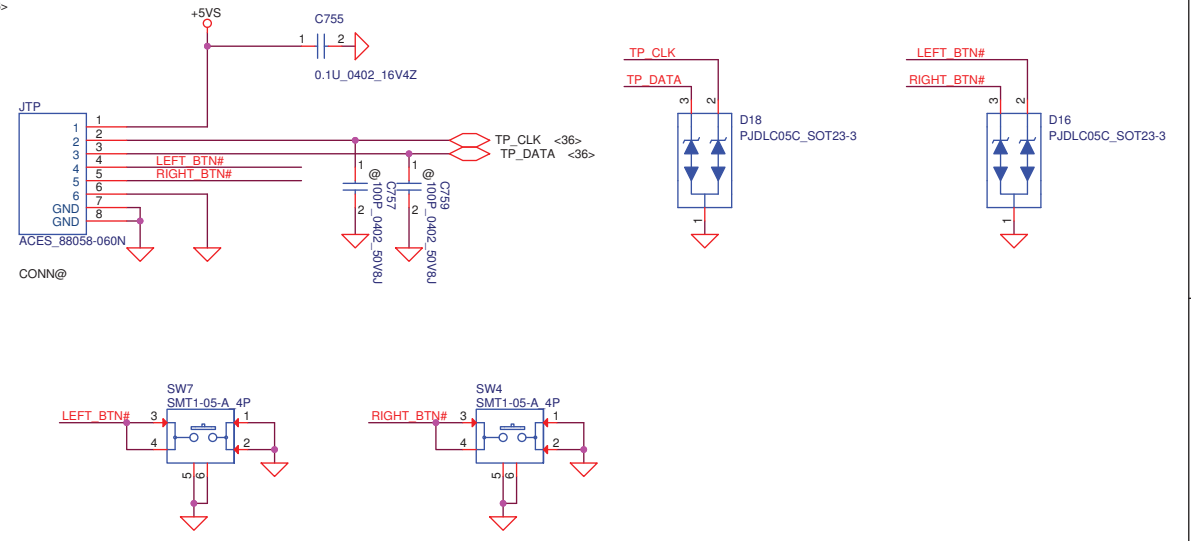


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Title <b>SBIOS &amp; EC ROM</b>		Document Number <b>VBL30/31 LA-9351P M/B</b>		Rev <b>0.1</b>	

# Power Button/ PWR/B



# Touch/B Connector



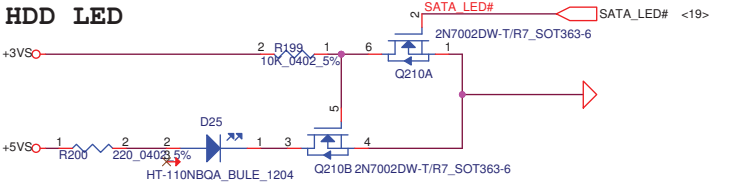
# DC-IN LED



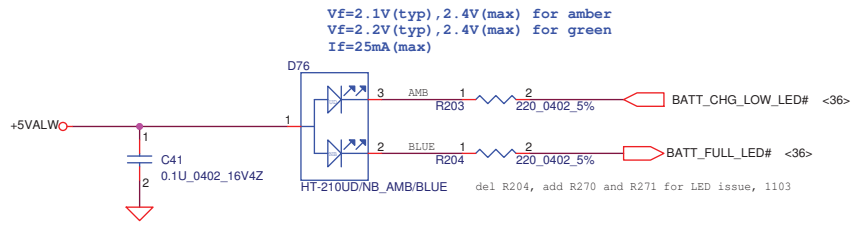
# WL&BT LED



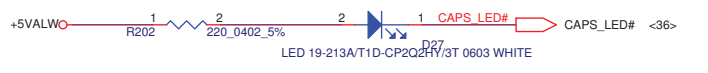
# HDD LED



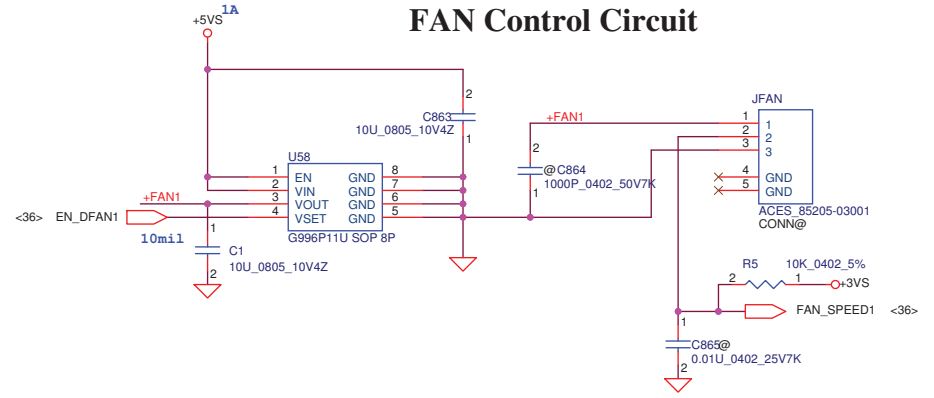
# BATT CHARGE/FULL LED



# CAP LOCK LED

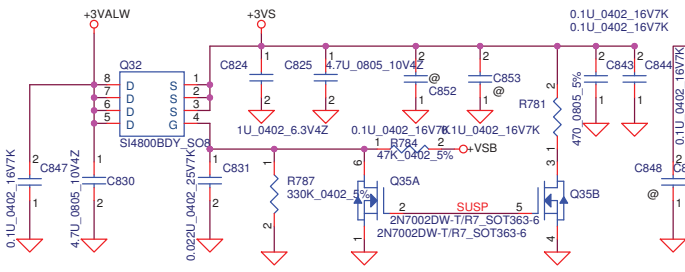


# FAN Control Circuit

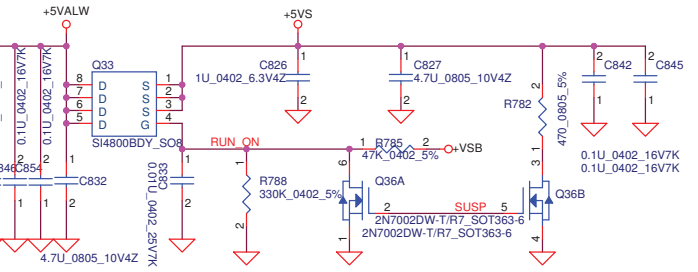


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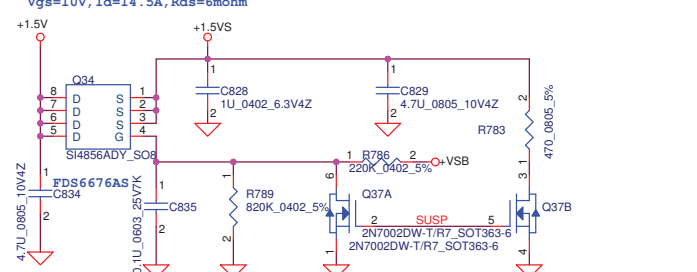
**+3VALW TO +3VS**  
Vgs=-0V, Id=9A, Rds=18.5mohm



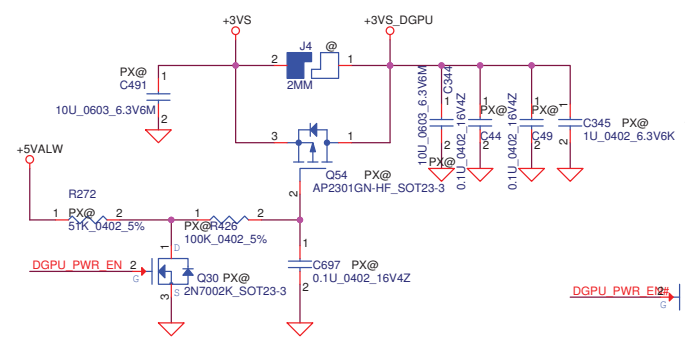
**+5VALW TO +5VS**



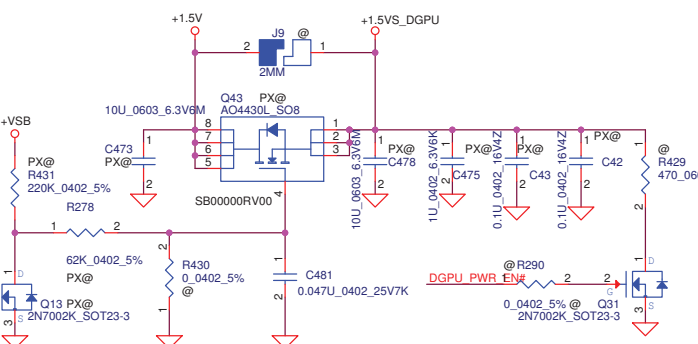
**+1.5V to +1.5VS**  
Vgs=10V, Id=14.5A, Rds=6mohm



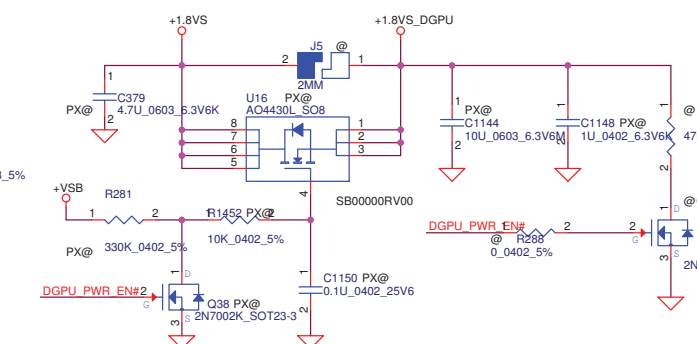
**+3VS TO +3VS\_DGPU**



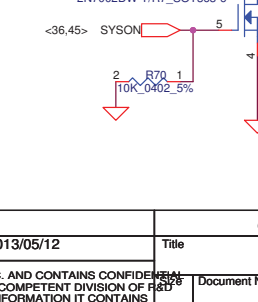
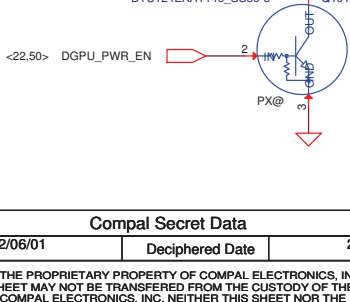
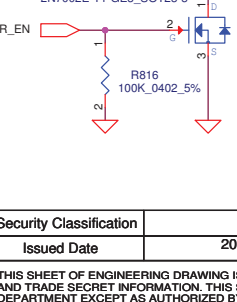
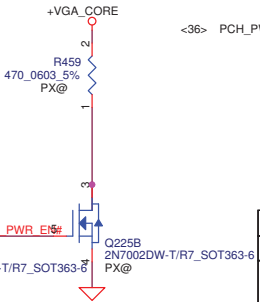
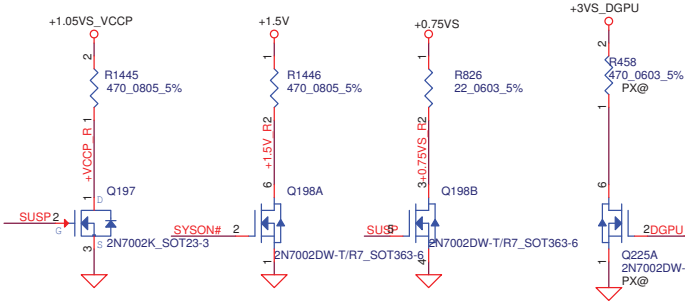
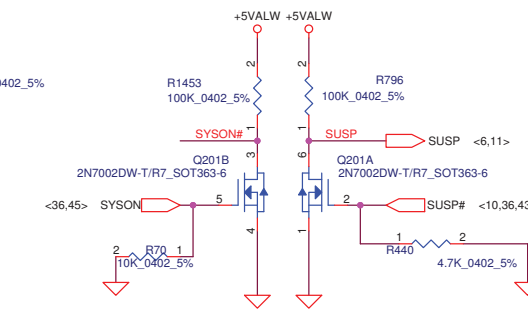
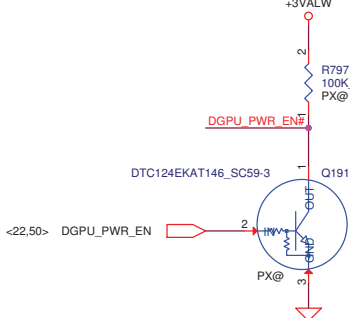
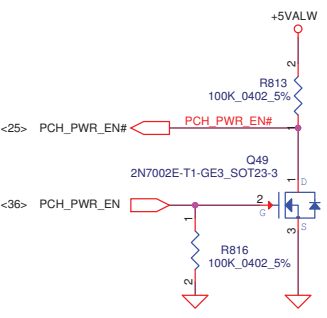
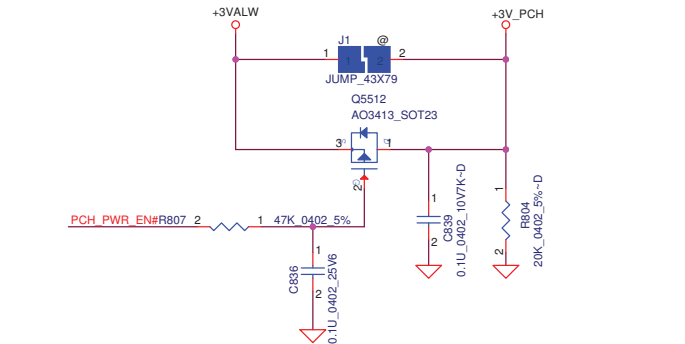
**+1.5V TO +1.5VS\_DGPU**



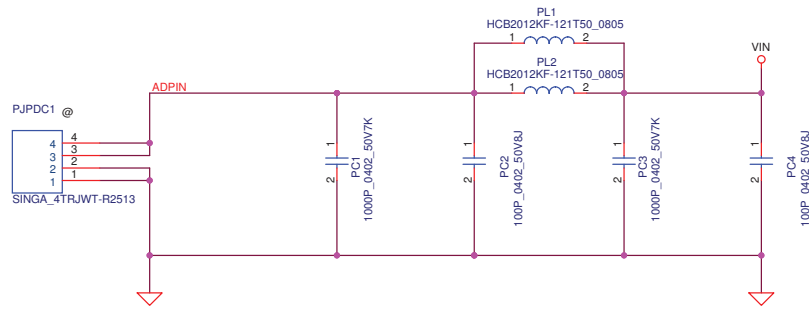
**+1.8VS TO +1.8VS\_DGPU**



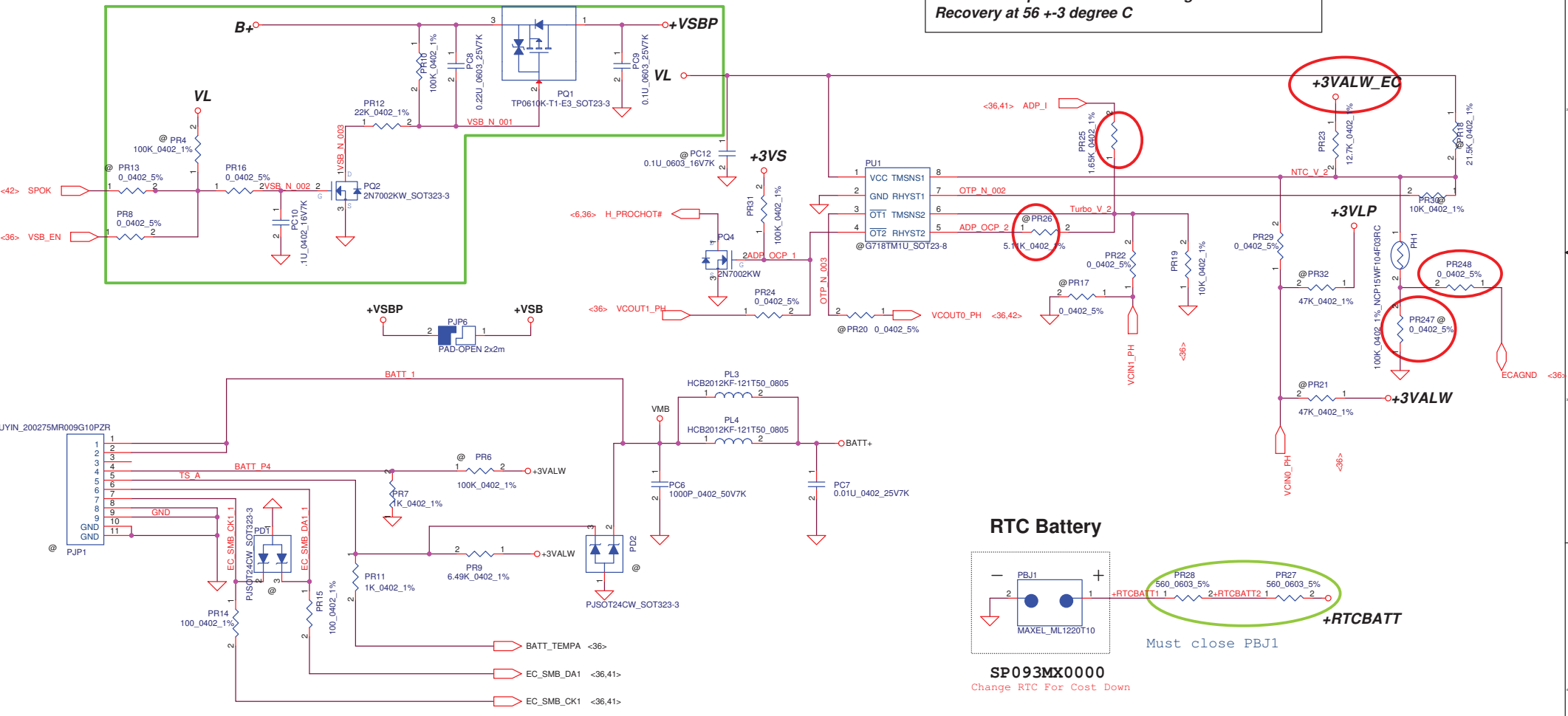
**+3VALW to +3V\_PCH**



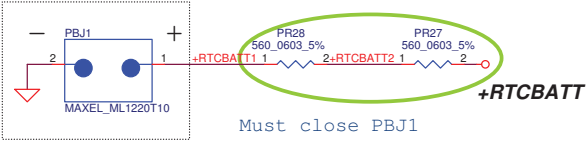
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**PH1 under CPU bottom side :**  
**CPU thermal protection at 93 +3 degree C**  
**Recovery at 56 +3 degree C**



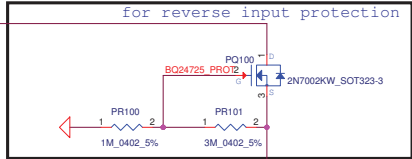
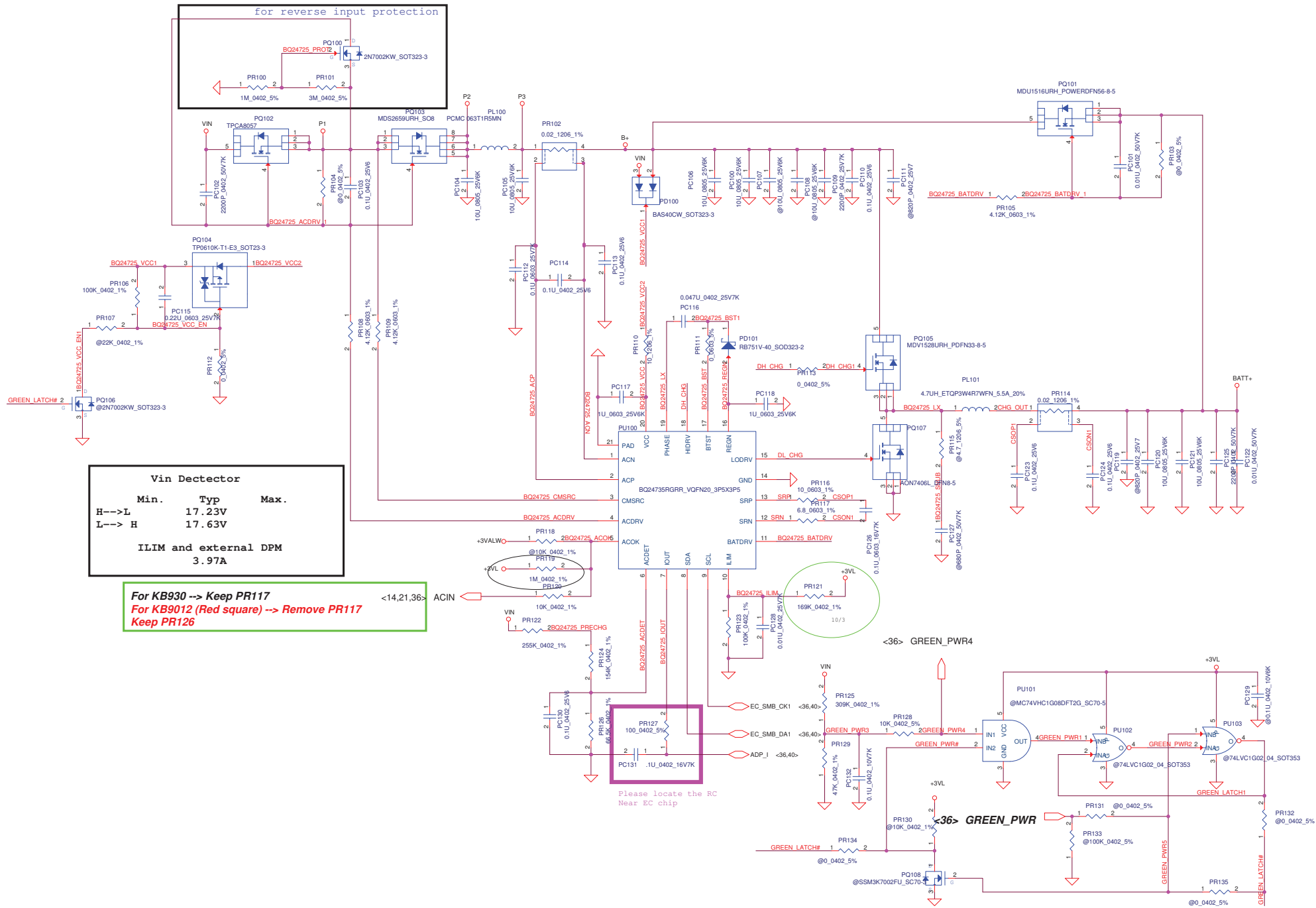
**RTC Battery**



**SP093MX0000**  
 Change RIC For Cost Down

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**Vin Detector**

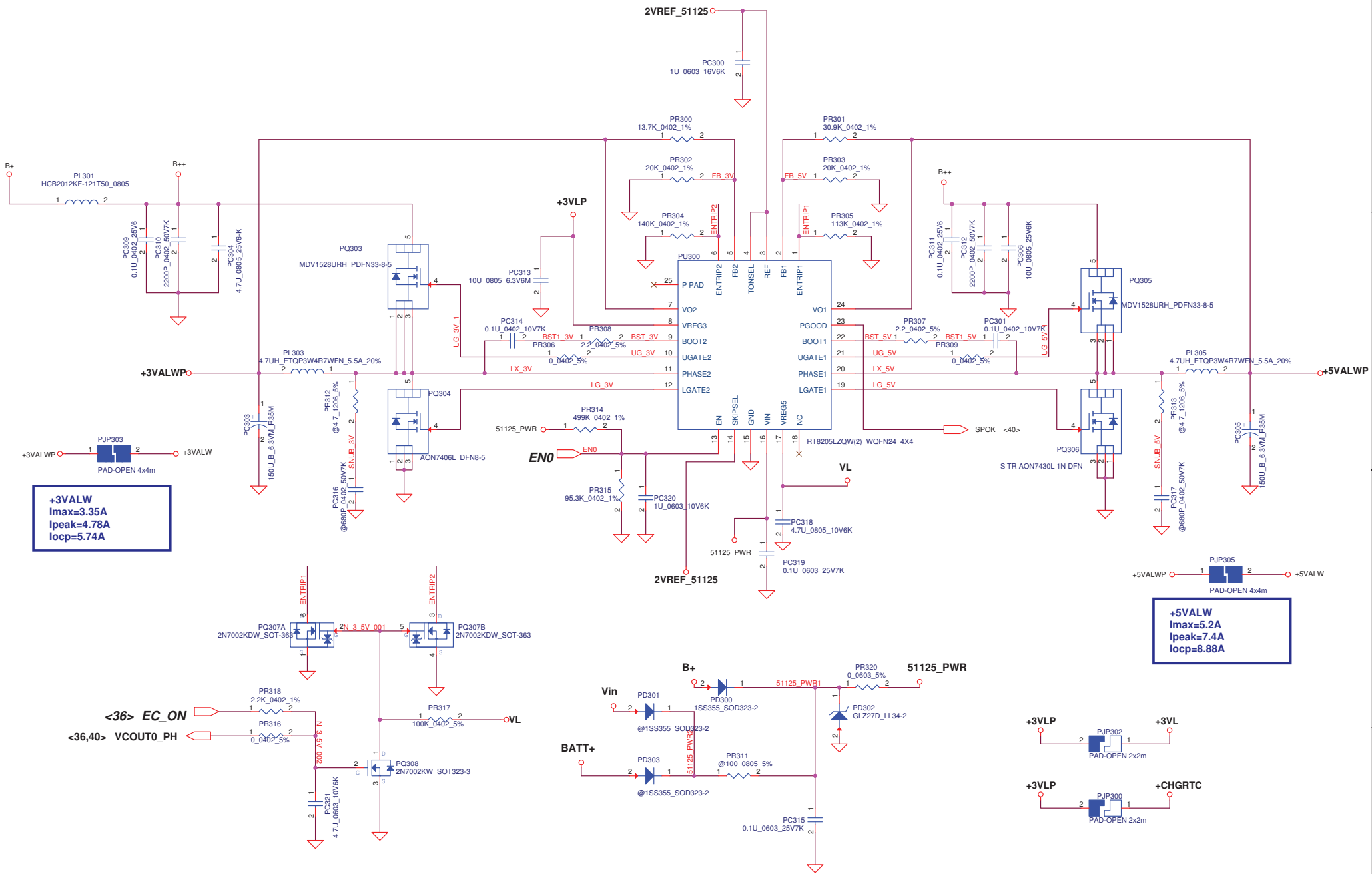
	Min.	Typ	Max.
H-->L		17.23V	
L-->H		17.63V	

**ILIM and external DPM**  
3.97A

For KB930 --> Keep PR117  
For KB9012 (Red square) --> Remove PR117  
Keep PR126

Please locate the RC  
Near EC chip

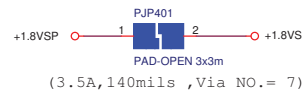
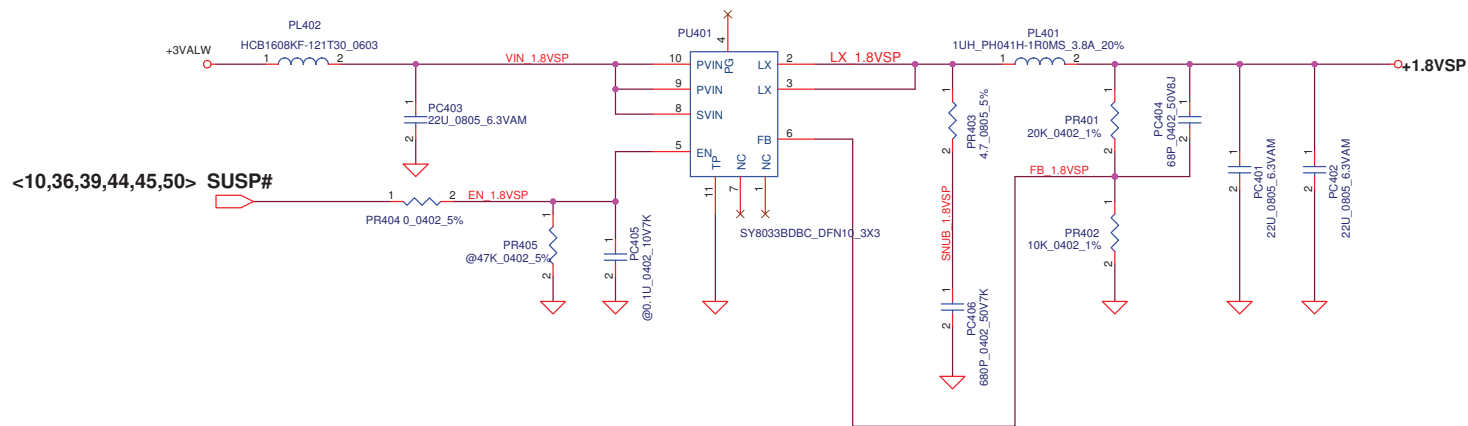
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2009/01/23	Deciphered Date	2012/12/31	PWR-CHARGER	
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**+3VALW**  
 $I_{max}=3.35A$   
 $I_{peak}=4.78A$   
 $I_{ocp}=5.74A$

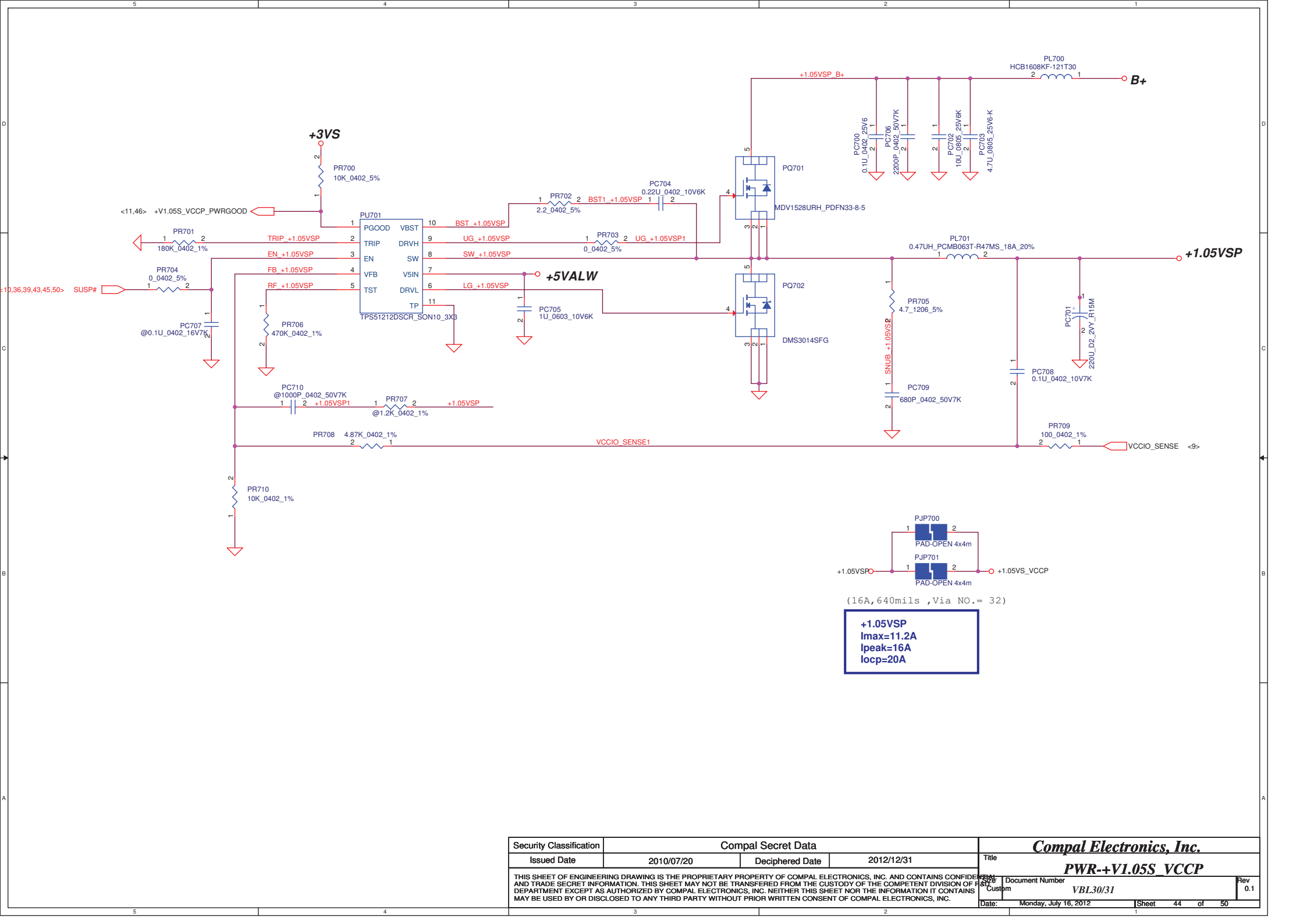
**+5VALW**  
 $I_{max}=5.2A$   
 $I_{peak}=7.4A$   
 $I_{ocp}=8.88A$

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**+1.8V**  
**I<sub>max</sub>=2.25A**  
**I<sub>peak</sub>=3.22A**

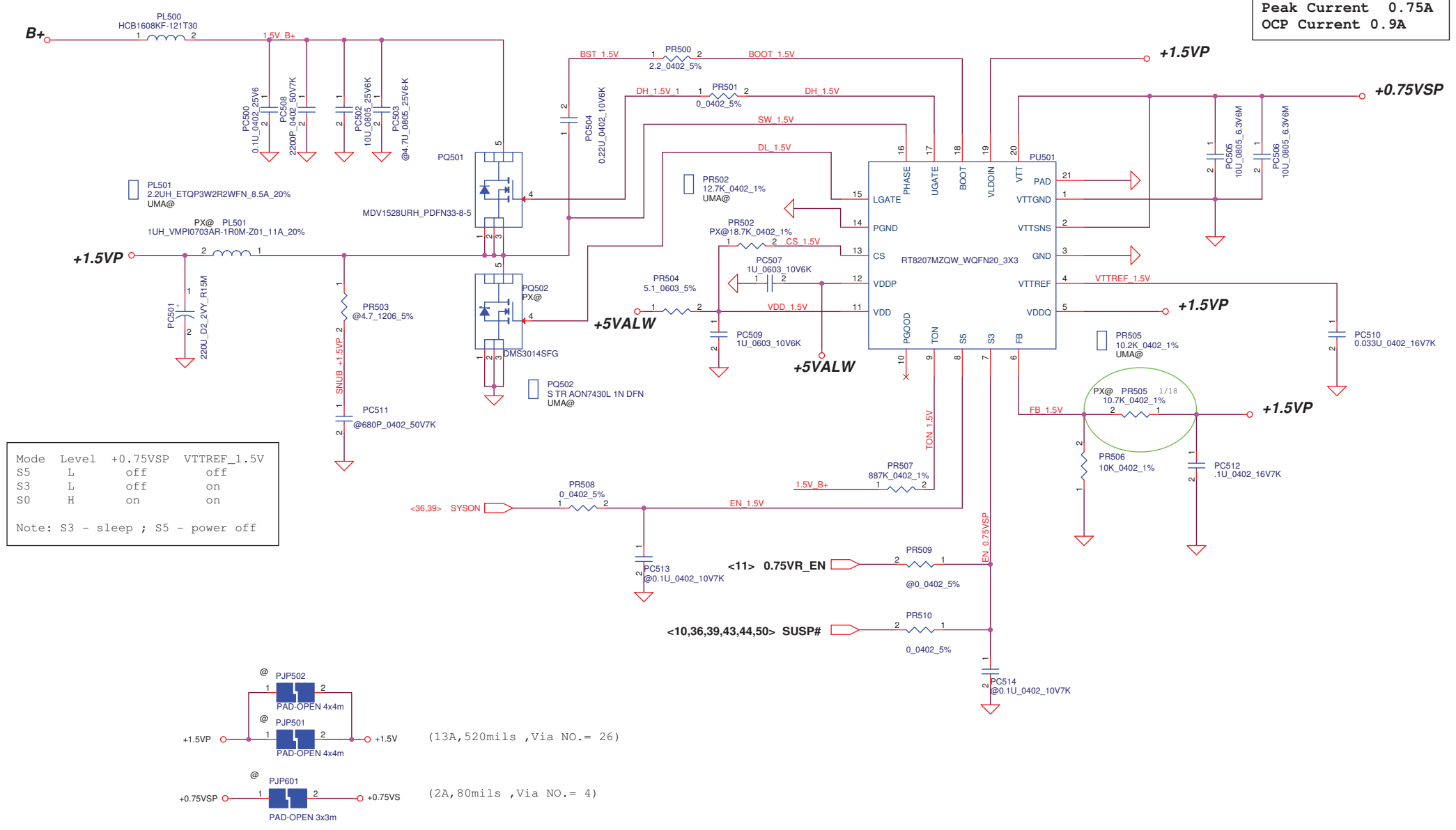
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Issued Date	2009/01/23	Deciphered Date	2012/12/31	<b>PWR-1.8VSP</b>	
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PJP700  
 PAD-OPEN 4x4m  
 PJP701  
 PAD-OPEN 4x4m  
 +1.05VSP  
 +1.05VS\_VCCP  
 (16A, 640mils, Via NO. = 32)  
**+1.05VSP**  
**I<sub>max</sub>=11.2A**  
**I<sub>peak</sub>=16A**  
**I<sub>ocp</sub>=20A**

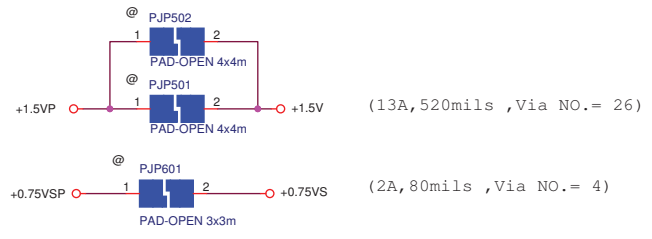
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		PWR-+V1.05S VCCP	
2010/07/20		2012/12/31		Document Number	
				VBL30/31	
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0.75Volt +/- 5%  
 TDC 0.525A  
 Peak Current 0.75A  
 OCP Current 0.9A



Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off



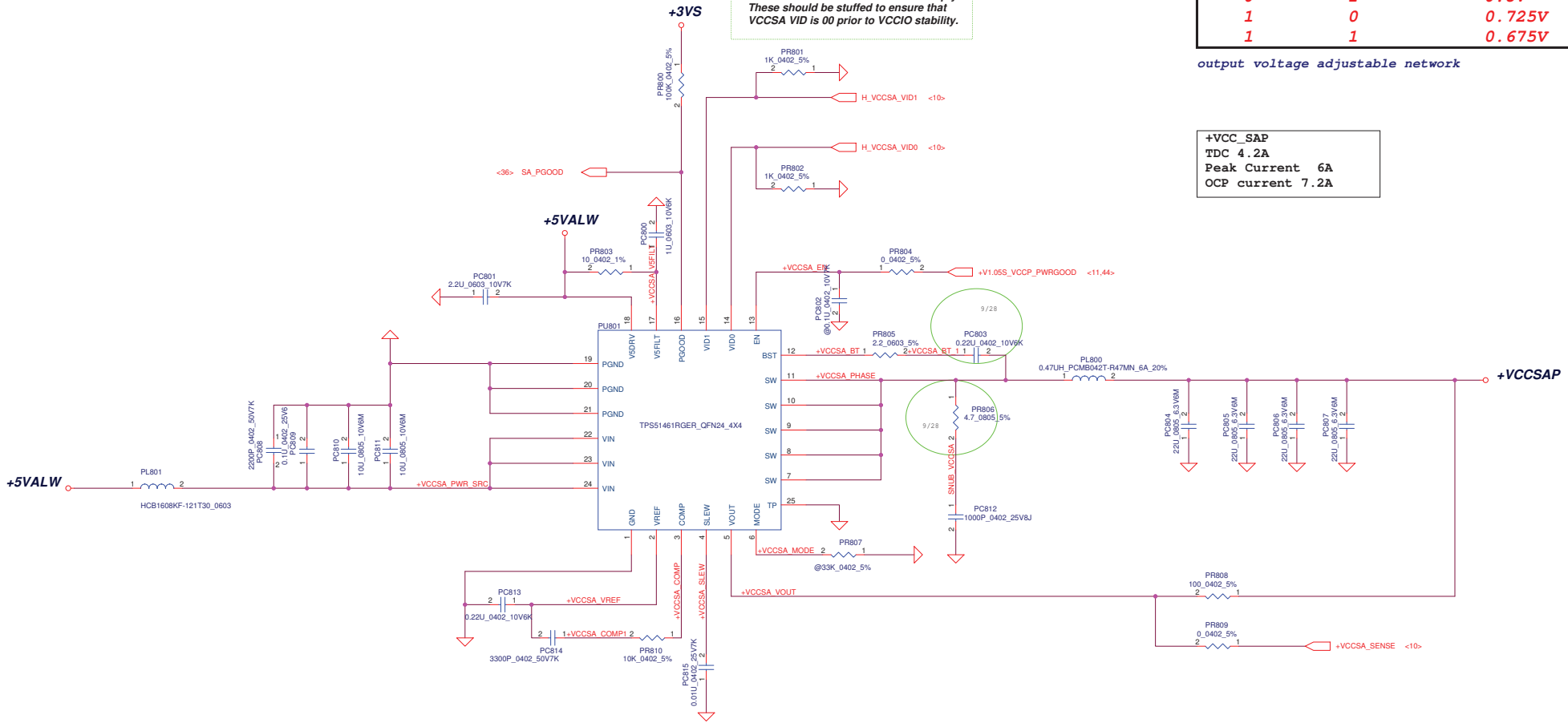
Security Classification		Compal Secret Data		Title	
Issued Date	2010/07/20	Deciphered Date	2012/12/31	PWR-1.5VP / +0.75VSP	
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VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

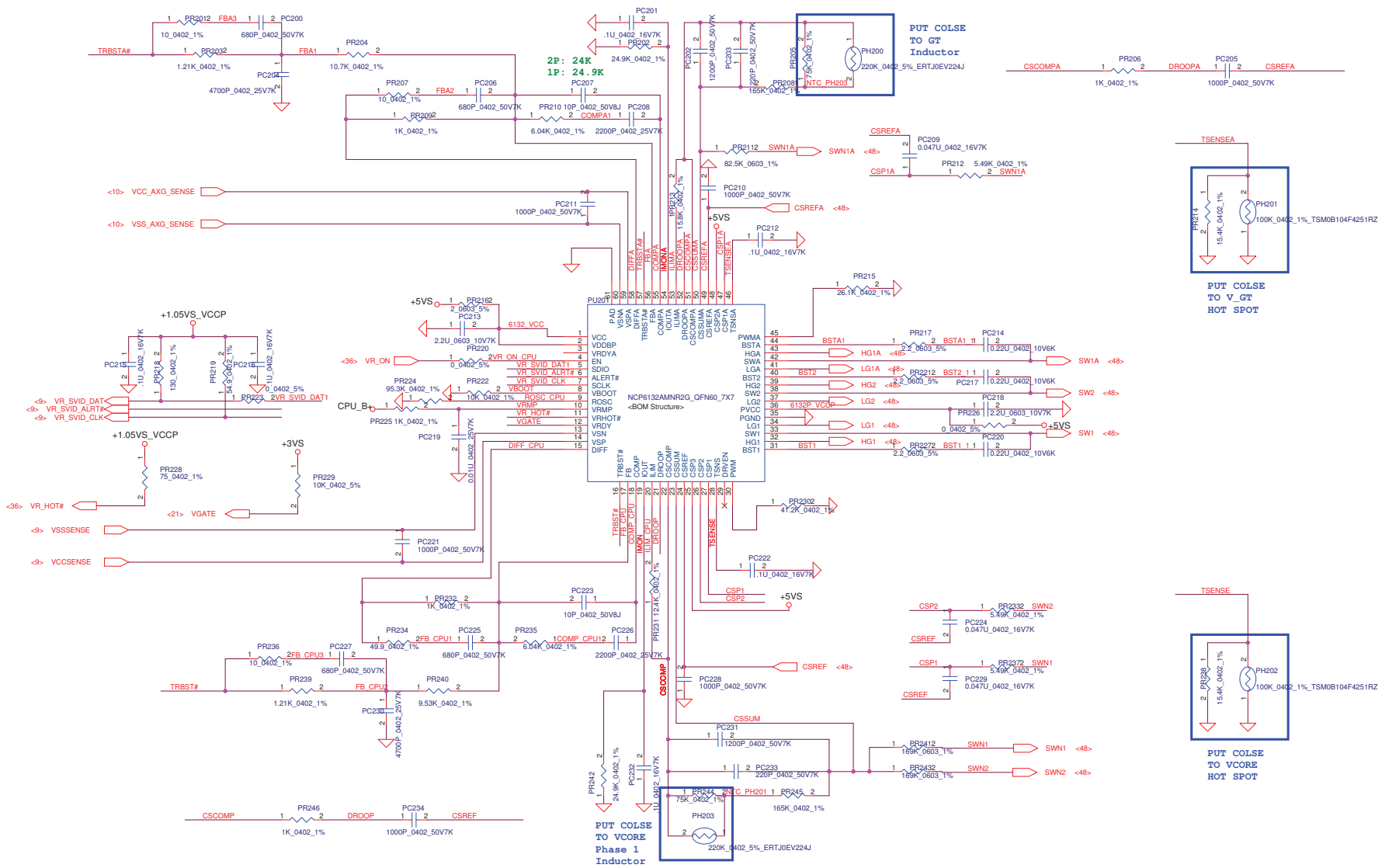
**+VCC\_SAP**  
TDC 4.2A  
Peak Current 6A  
OCP current 7.2A

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

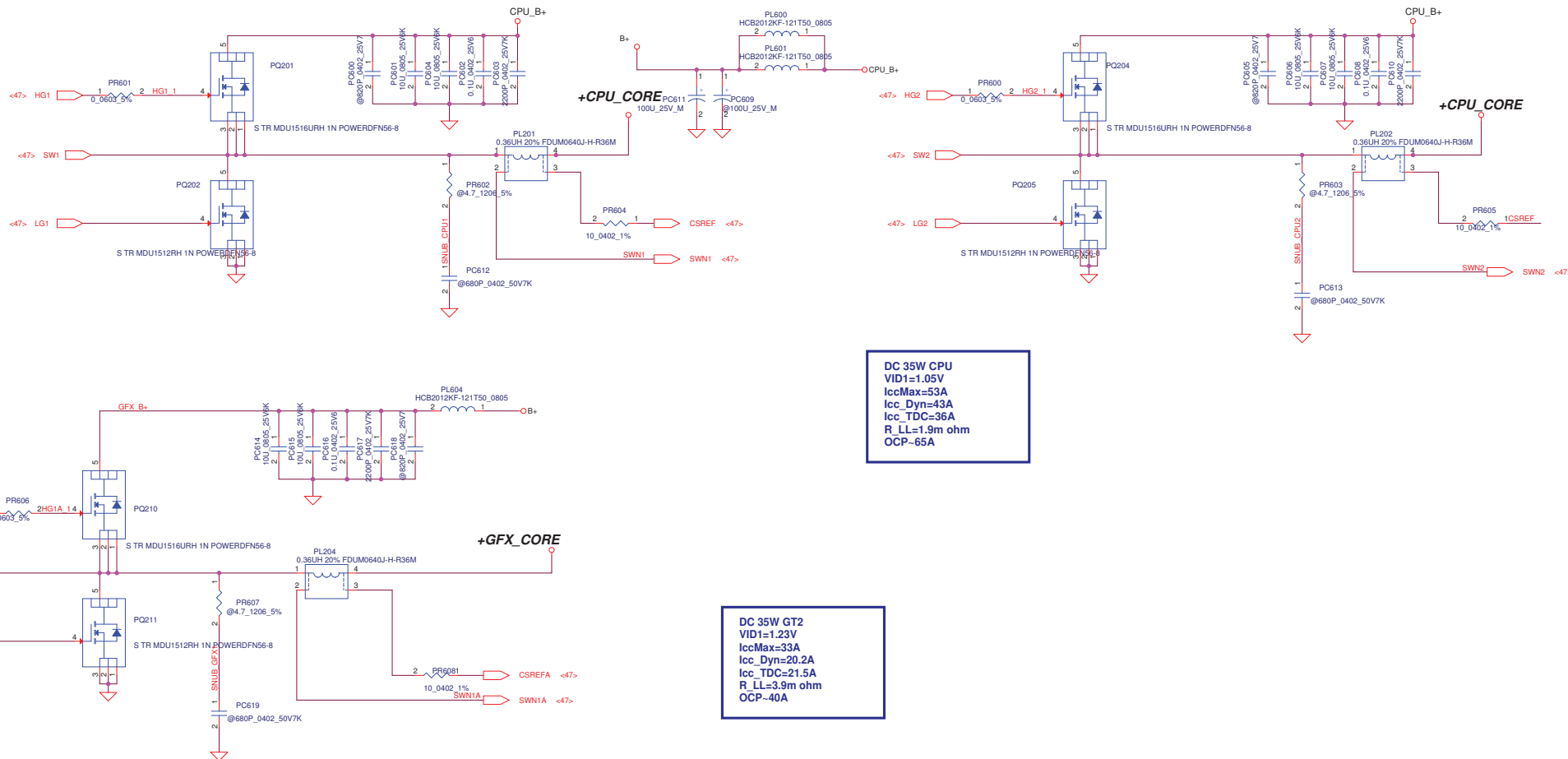


(6A, 240mils, Via NO. = 12)

**+VCCSA**  
Imax=4.2A  
Ipeak=6A  
Iocp=7.2



Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2011/10/31	Deciphered Date	2012/12/31	Title	<b>PWR-CPU CORE</b>	
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Document Number	VBL30/31				Rev	0.1
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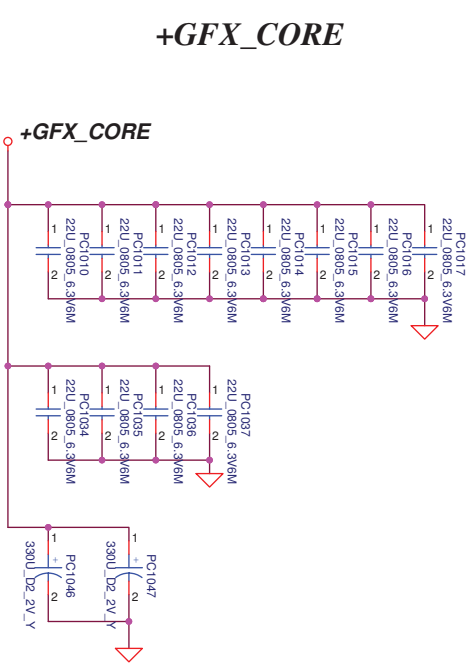
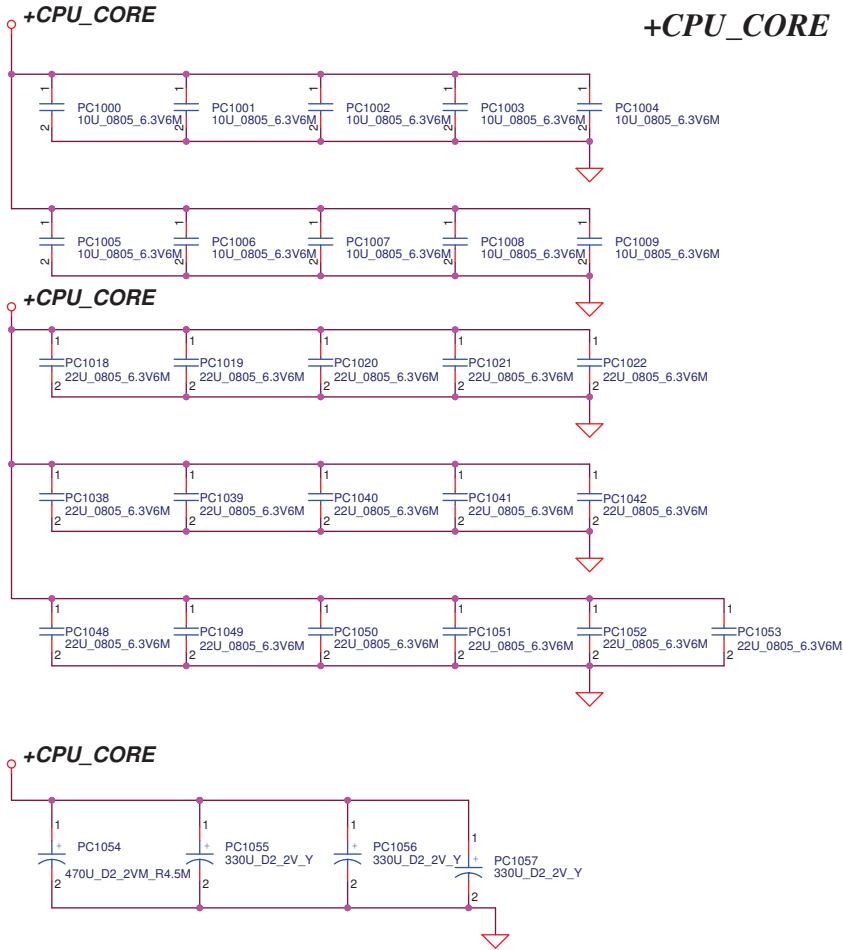


DC 35W CPU  
 VID1=1.05V  
 IccMax=53A  
 Icc\_Dyn=43A  
 Icc\_TDC=36A  
 R\_LL=1.9m ohm  
 OCP=65A

DC 35W GT2  
 VID1=1.23V  
 IccMax=33A  
 Icc\_Dyn=20.2A  
 Icc\_TDC=21.5A  
 R\_LL=3.9m ohm  
 OCP=40A

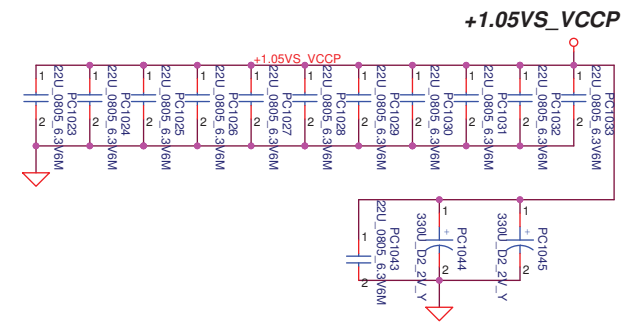
Security Classification		Compal Secret Data		Title	
Issued Date	2011/10/31	Deciphered Date	2012/12/31	PWR-VCC CORE	
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Below is 458544\_CRV\_PDDG\_0.5 Table 5-8.

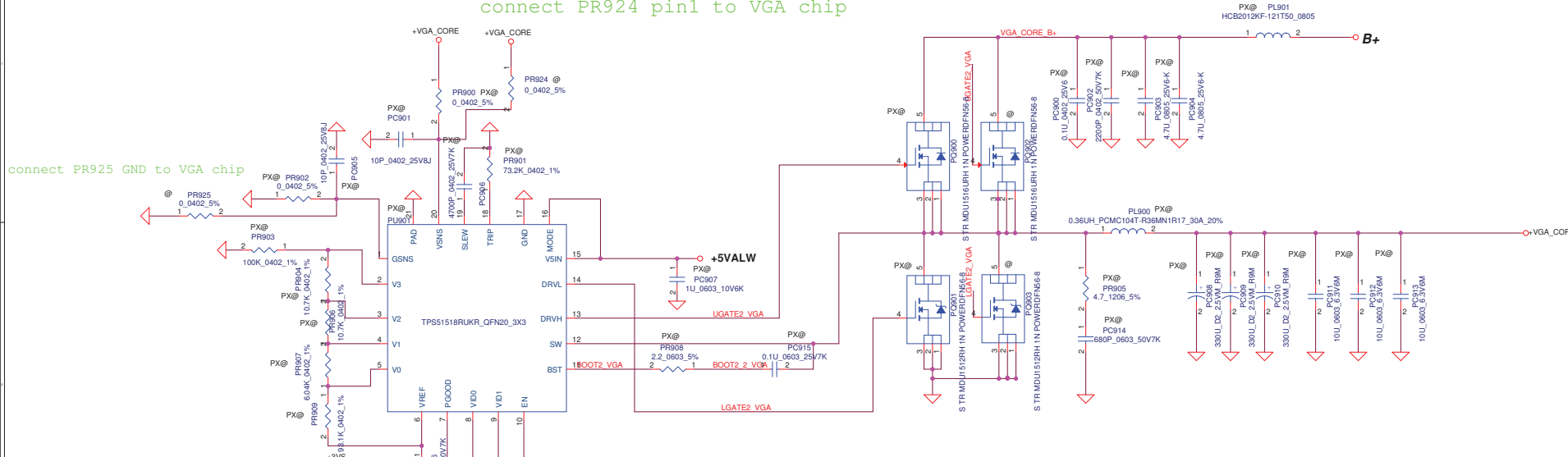
Socket Bottom	5 x 22 $\mu$ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 $\mu$ F (0805) 2 x (0805) no-stuff sites



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				Document Number	Rev
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				Date	Monday, July 16, 2012
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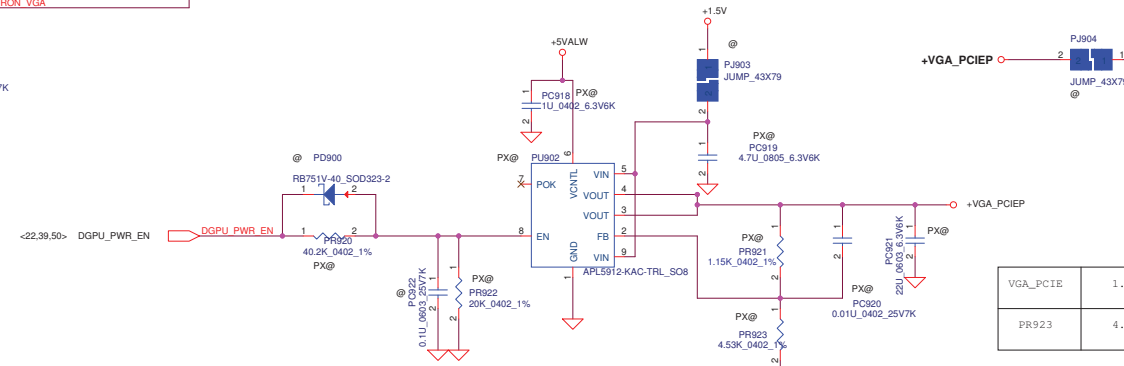
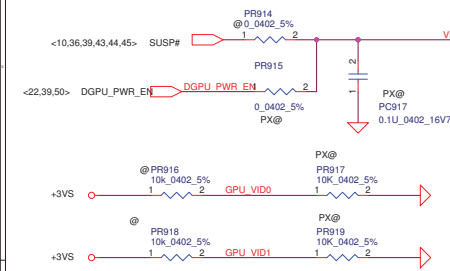
connect PR924 pin1 to VGA chip

connect PR925 GND to VGA chip



Seymour XT		
GPU_VID1	GPU_VID0	Core Voltage Level
1	1	0.9V
1	0	1.0V
0	1	1.1V
0	0	1.15V

**+VGA\_CORE**  
 Boot Voltage=(0:0) 1.15V  
 I<sub>max</sub>=13.4A  
 I<sub>peak</sub>=19.16A  
 I<sub>oqp</sub>=24A



**+VGA\_PCIE**  
 VGA\_PCIE=1.0V  
 I<sub>max</sub>=2.058A  
 I<sub>peak</sub>=2.94A  
 I<sub>oqp</sub>=3.528A

VGA_PCIE	1.0V	1.1 V
PR923	4.53K	3K