Compal Confidential

Intel Haswell rPGA Processor with Lynx Point-H

Afterburn MXM

LA-9371P

2012-09-28

REV : 0.2

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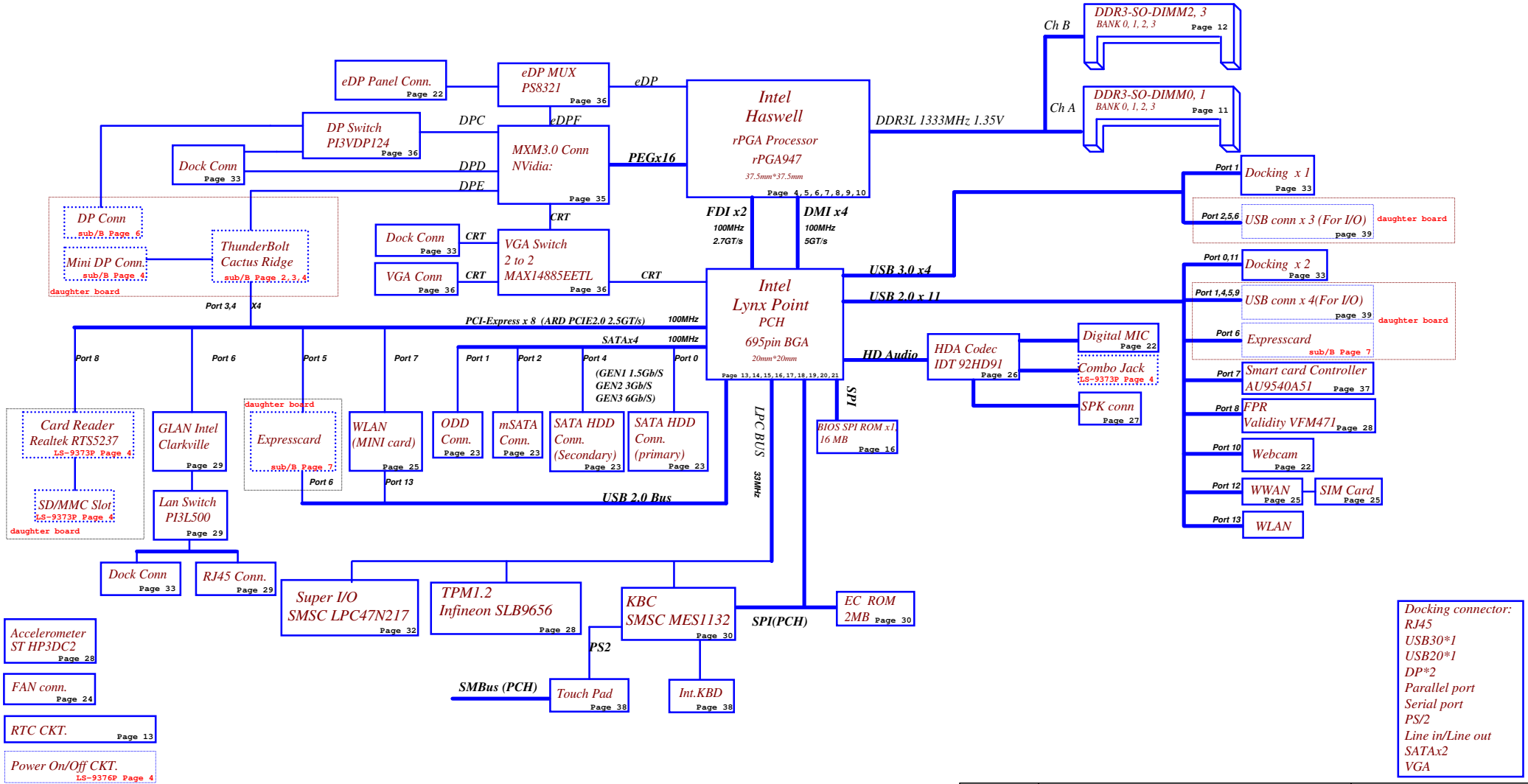
Model Name : Afterburn

File Name : LA-9371P



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title: Block Diagrams
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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane / State	+RTCVCC	B+	+5VDS +3VDS	+1.35V +0.675VS	+5VS +3VS +1.5VS +VCC_CORE +1.05VS +1.05VM	
S0	O	O	O	O	O	
S1	O	O	O	O	O	
S3	O	O	O	O	X	
S5 S4/AC	O	O	O	X	X	
S5 S4/ Battery only	O	O	X	X	X	
S5 S4/AC & Battery don't exist	O	X	X	X	X	

SMBUS Control Table

	SOURCE	BATT	2nd BATT	XDP	SODIMM	G-SENSOR	TP	NIC	NFC	EC	MXM
I2C_MAIN_CLK I2C_MAIN_DAT	SMSC1126	V	X	X	X	X	X	X	X	X	X
I2C_BAY_CLK I2C_BAY_DAT	SMSC1126	X	V	X	X	X	X	X	X	X	X
MEM_SMBCLK MEM_SMBDATA	Haswell	X	X	V	V	V	V	X	X	X	X
LAN_SMBCLK LAN_SMBDATA	Haswell	X	X	X	X	X	X	V	V	X	X
SML1_SMBCLK SML1_SMBDATA	Haswell	X	X	X	X	X	X	X	X	V	V

Stapping Options Flash

GPIO 51 Bit 1	GPIO 19 Bit 0	Boot BIOS Destination
0	0	Reserved
0	1	RSVD
1	0	SPI
1	1	LPC

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build

AMT@ : means just install for support iAMT
CONN@ : means ME part.

Layout Notes

07/24 update

: Question Area Mark.(Wait check)

Install below 45 level BOM structure for ver. 0.1

45@ : means just put it in the BOM of 45 level.

Install below 43 level BOM structure for ver. 0.1

DEBUG@ : means just build when PCIE port 80 CARD function enable.*Remove before MP*

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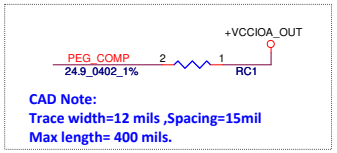

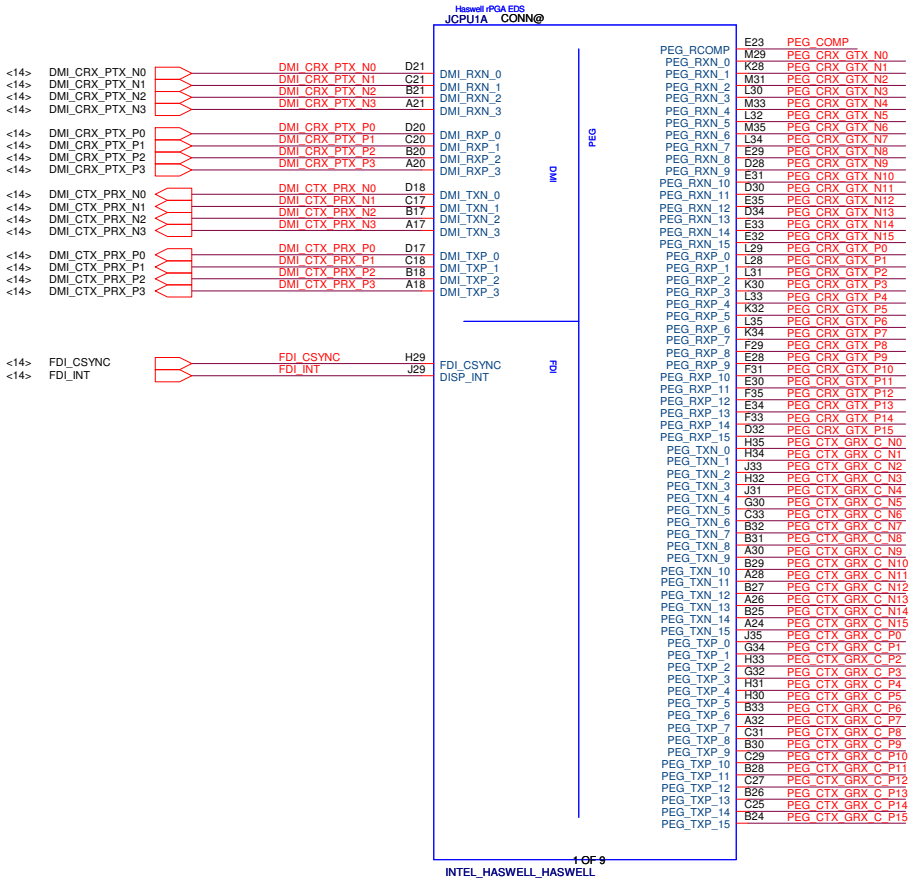

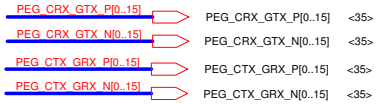

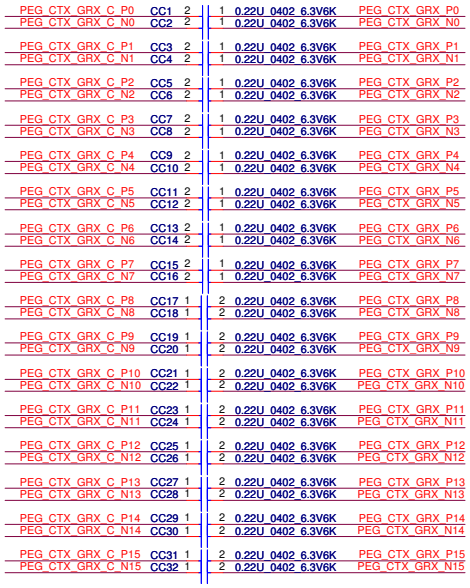

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Compal Electronics, Inc.

Title: DMI,PEG

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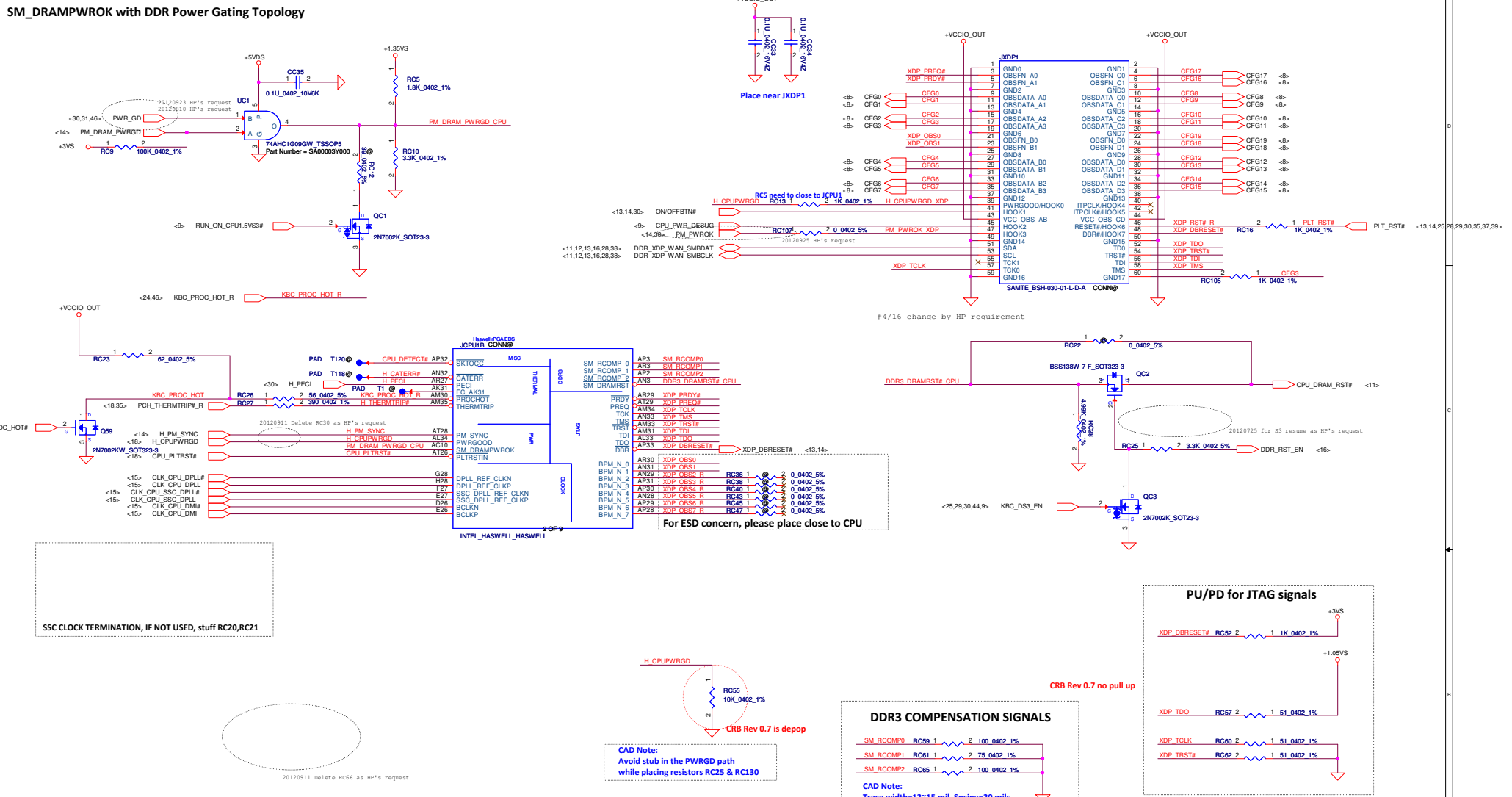
Date: Friday, September 28, 2012 | Sheet 4 of 53

SM_DRAMPWROK with DDR Power Gating Topology



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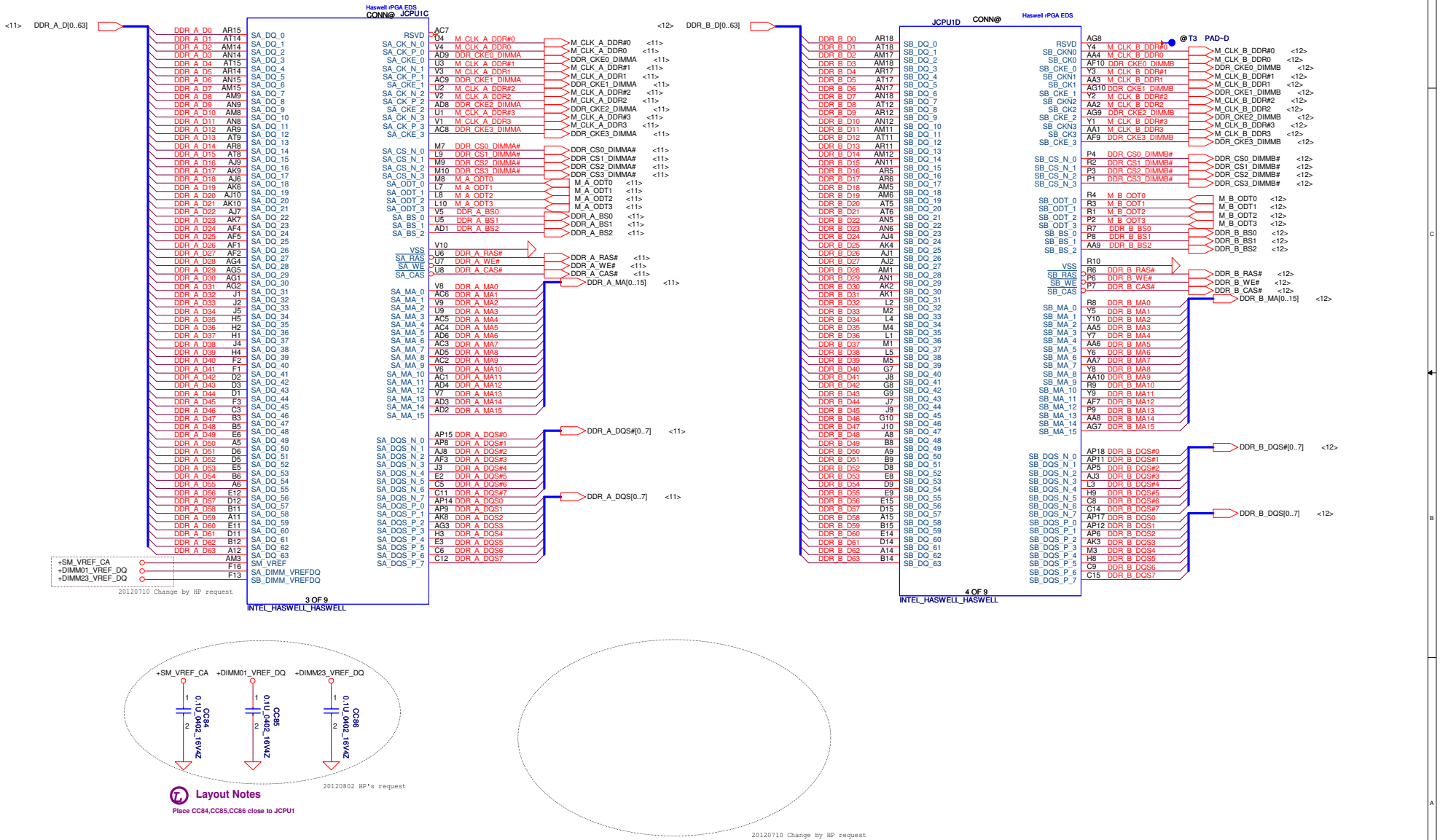
Compal Electronics, Inc.

Title: PM,XDP,CLK

Size: Custom | Document Number: LA-9371P | Rev: 0.2

Date: Friday, September 28, 2012 | Sheet 5 of 53



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Compal Electronics, Inc.

Title: DDRIII

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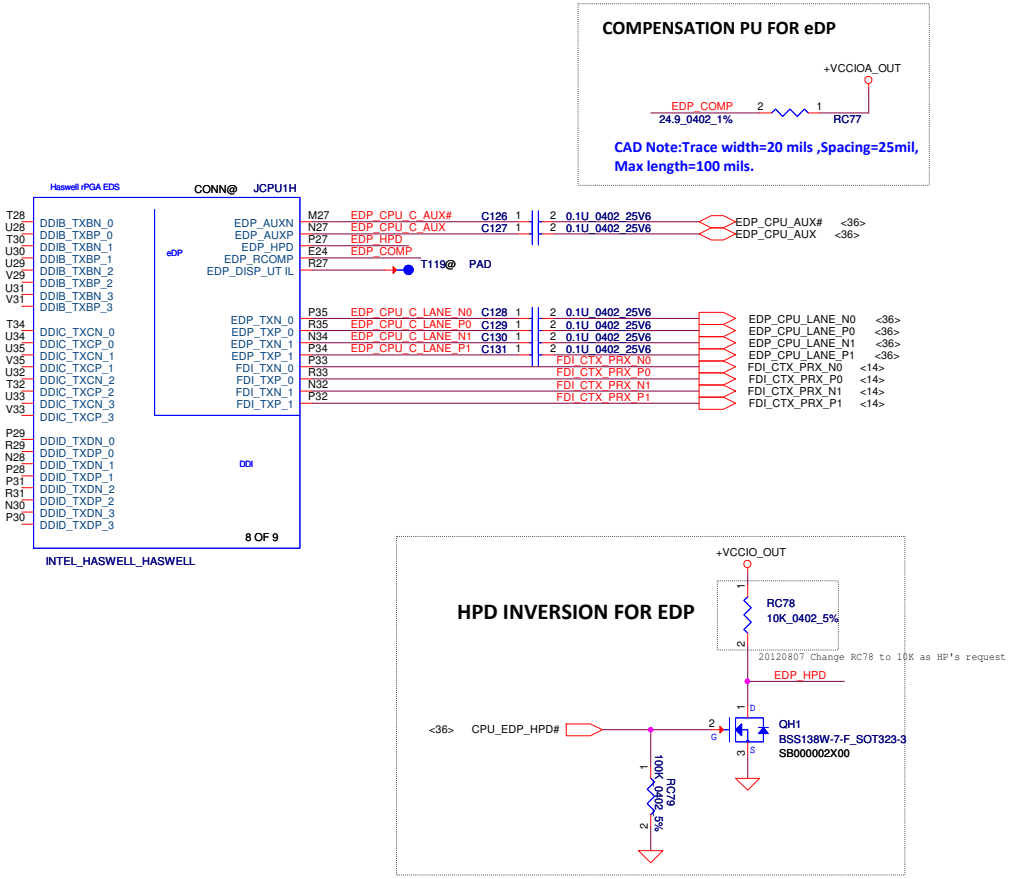
Date: Friday, September 28, 2012 | Sheet 6 of 53



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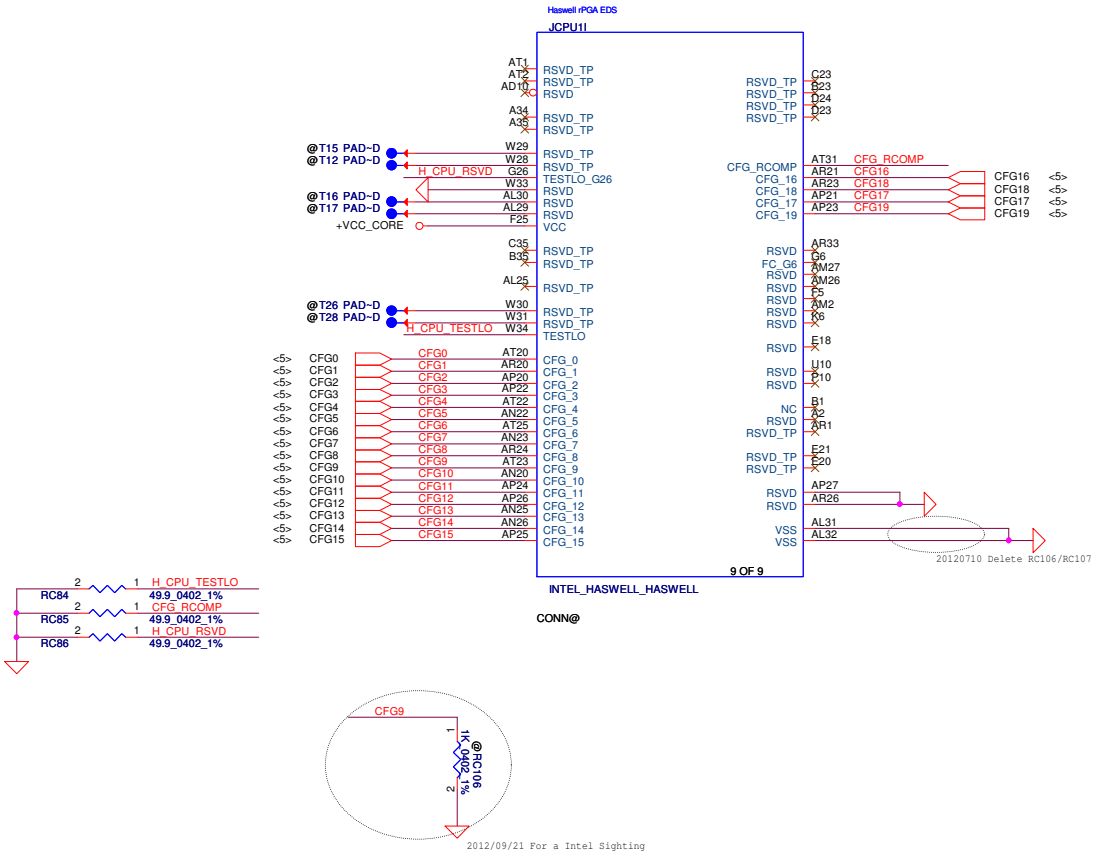
Compal Electronics, Inc.

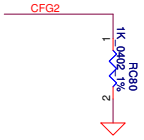
Title: CPU-FDI,eDP,DDI

Size: Custom | Document Number: LA-9371P | Rev: 0.2

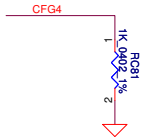
Date: Friday, September 28, 2012 | Sheet 7 of 53

CFG STRAPS for CPU

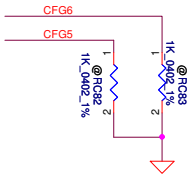




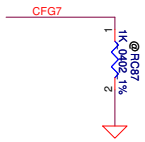
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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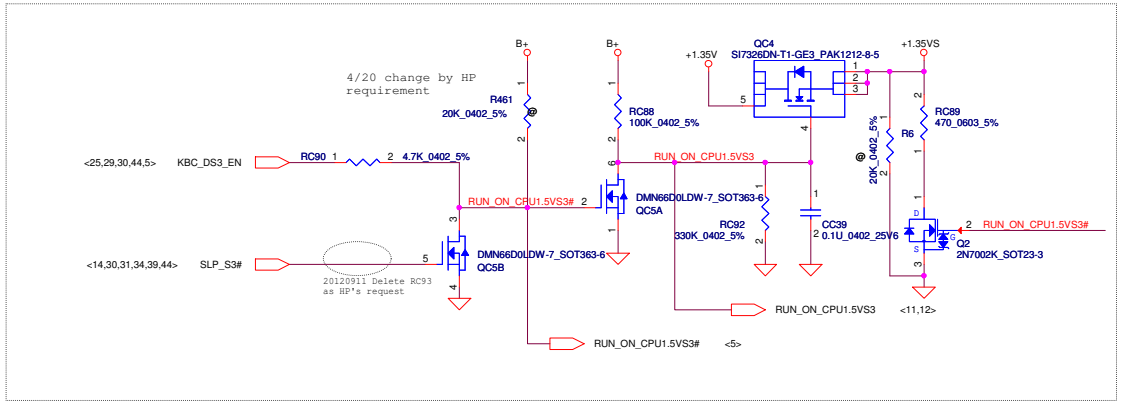
+1.35VS Source



SVID ALERT

CAD Note: Place the PU resistors close to CPU
RC60 close to CPU 300 - 1500mils

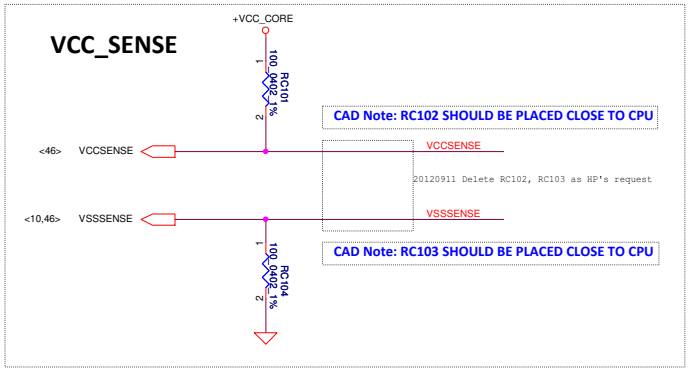
SVID DATA

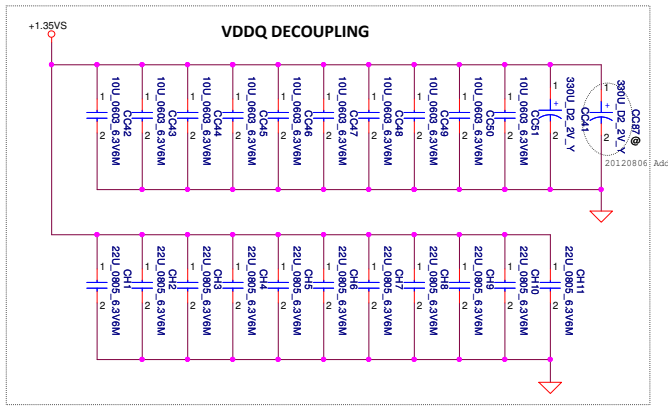
CAD Note: Place the PU resistors close to CPU
RC63 close to CPU 300 - 1500mils

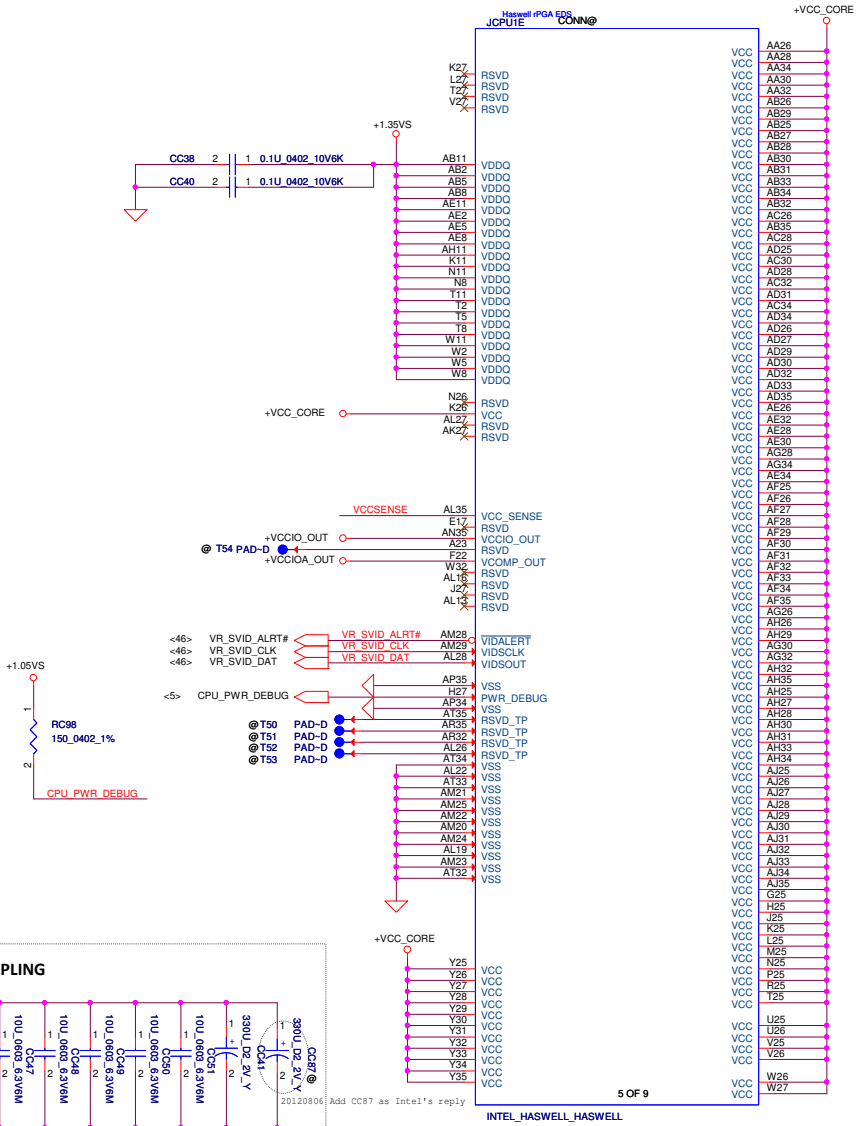
20120725 HP's request

RESISTOR STUFFING OPTIONS ARE PROVIDED FOR TESTING PURPOSES

VCC_SENSE







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Title: CPU- PWR

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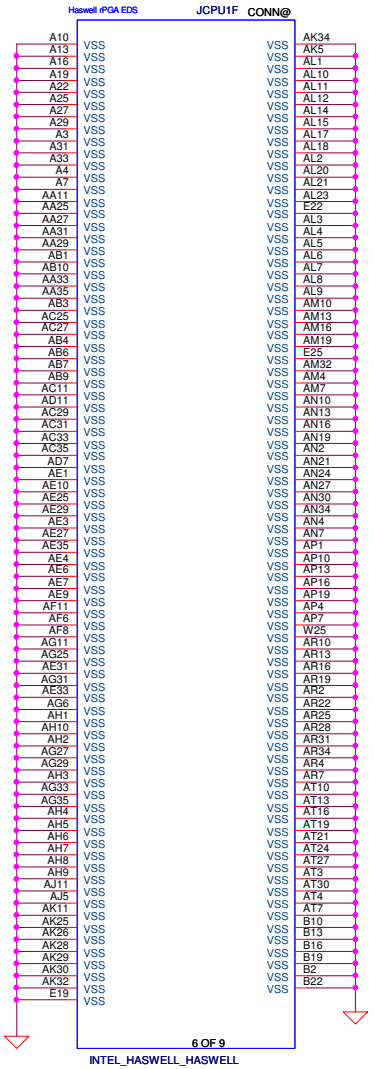

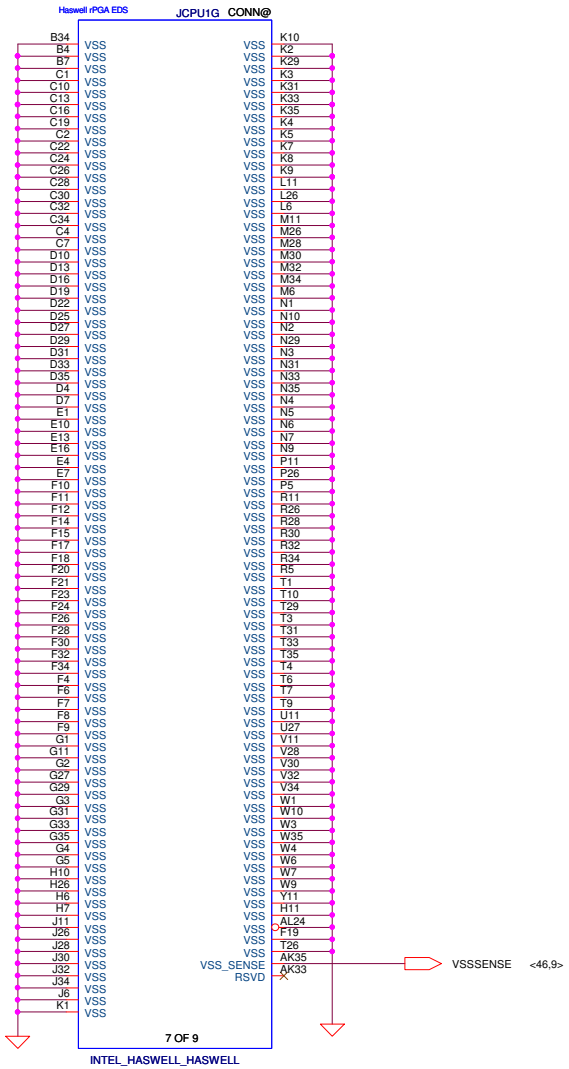

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Title: CPU-VSS

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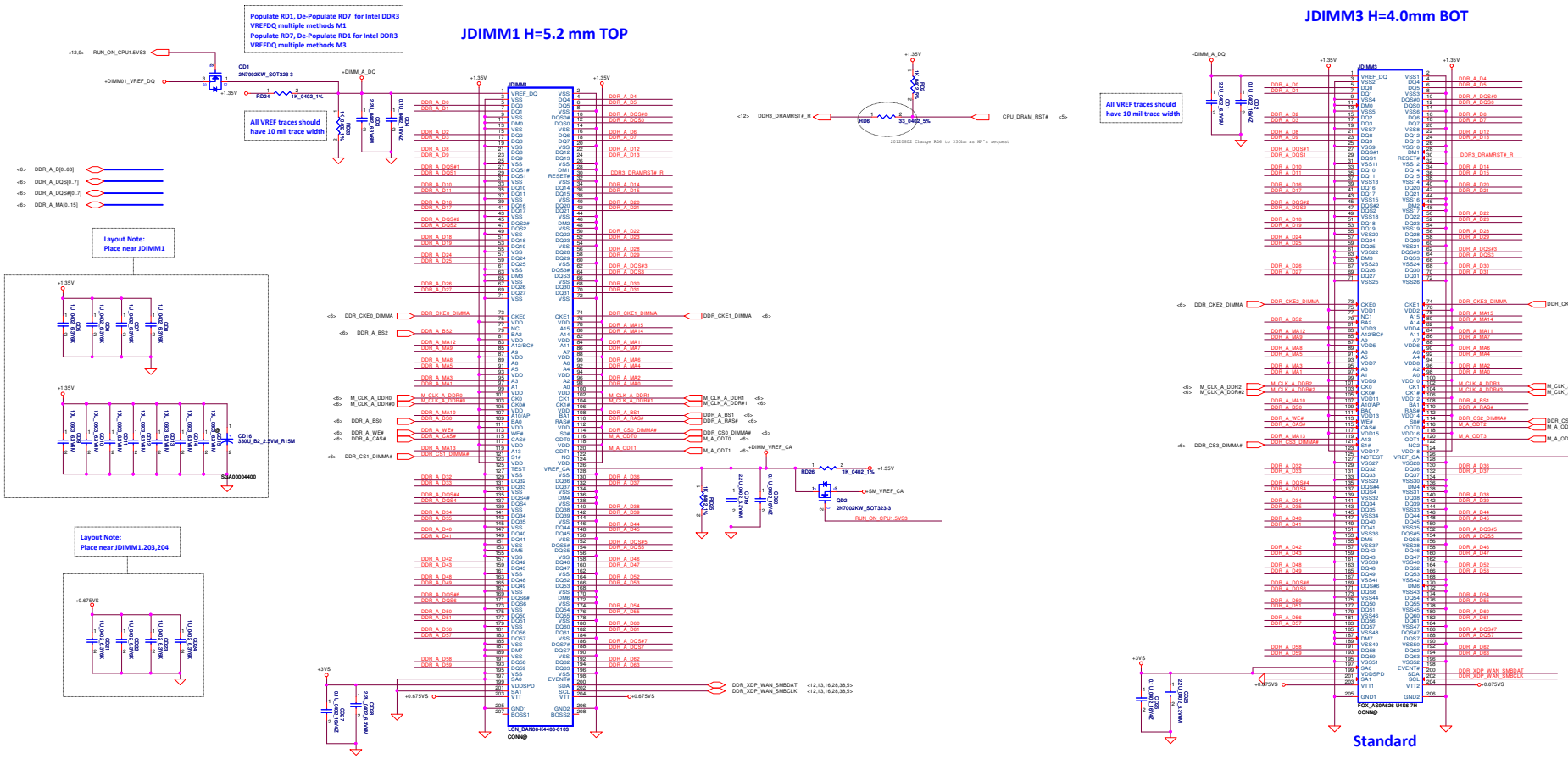

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DDRIII DIMM1&2

Size	Document Number	Rev
Custom	LA-9371P	0.2

Date: Friday, September 28, 2012 | Sheet 11 of 53

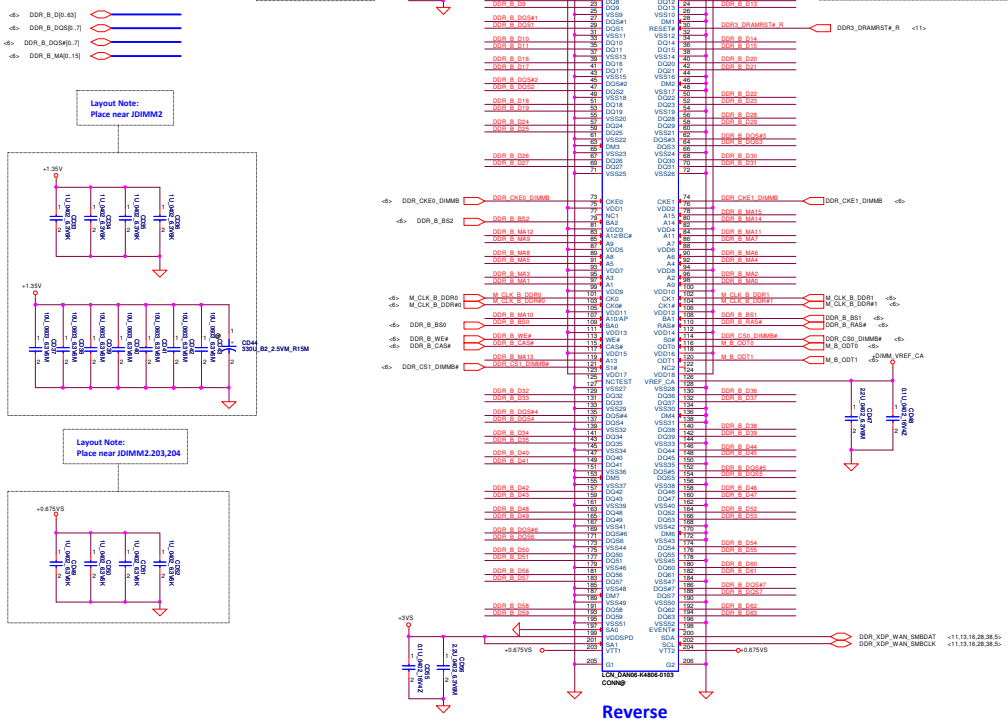
Populate RD4, De-Populate RD8 for Intel DDR3
VREFDQ multiple methods M1
Populate RD8, De-Populate RD4 for Intel DDR3
VREFDQ multiple methods M3

JDIMM2 H=9.2mm TOP

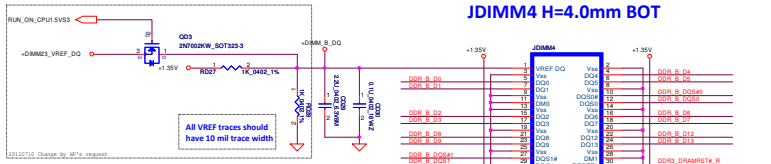
All VREF traces should have 10 mil trace width

Layout Note: Place near JDIMM2

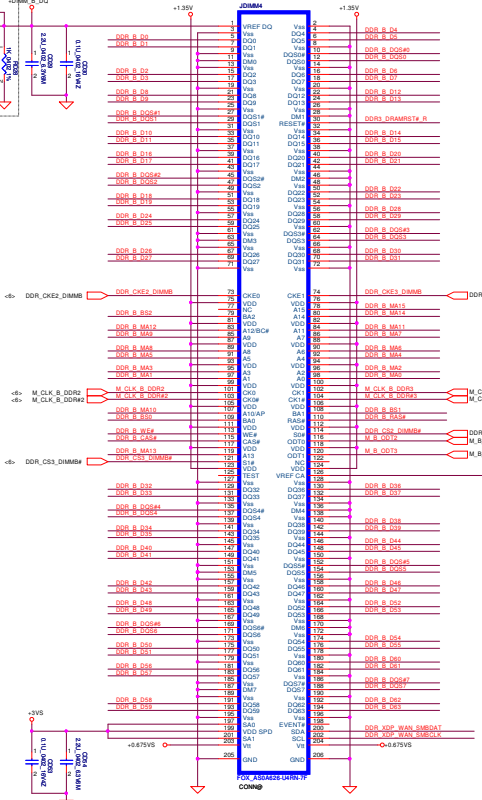
Layout Note: Place near JDIMM2.203,204



Reverse



JDIMM4 H=4.0mm BOT



Reverse

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DDRIII DIMM3&4

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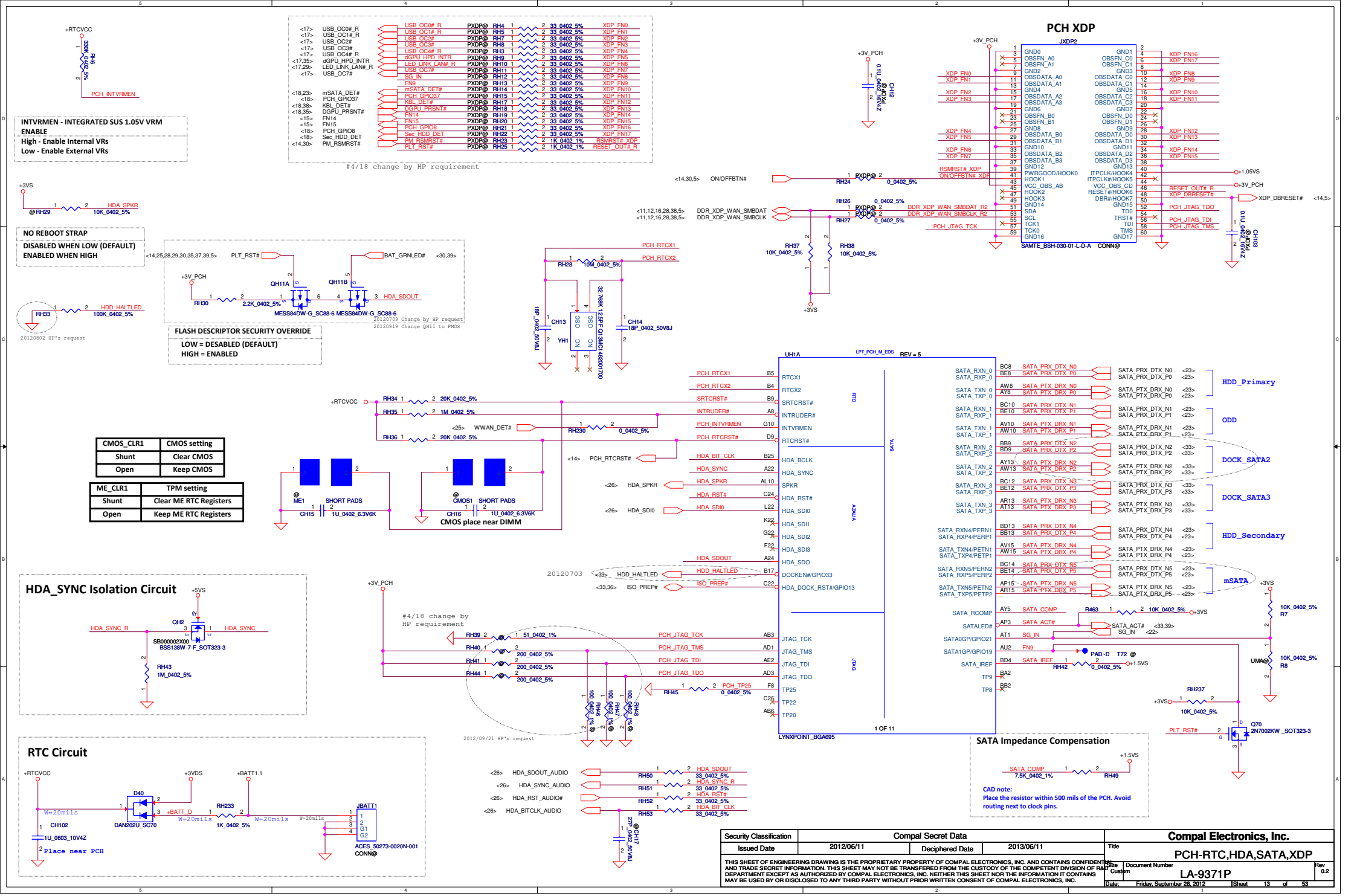
PCH XDP
JXDP2
SAMTE_BSH-030-01-L-D-A CONN@
UH1A
LPT_PCH_M_EDS REV = 5
LYNXPOINT_BGA695
1 OF 11
HDD_Primary
ODD
DOCK_SATA2
DOCK_SATA3
HDD_Secondary
mSATA
HDA_SYNC Isolation Circuit
RTC Circuit
SATA Impedance Compensation
CMOS place near DIMM
INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs
NO REBOOT STRAP
DISABLED WHEN LOW (DEFAULT)
ENABLED WHEN HIGH
FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DESABLED (DEFAULT)
HIGH = ENABLED
CMOS_CLR1 | CMOS setting
Shunt | Clear CMOS
Open | Keep CMOS
ME_CLR1 | TPM setting
Shunt | Clear ME RTC Registers
Open | Keep ME RTC Registers
#4/18 change by HP requirement
20120703
2012/09/21 HP's request
20120802 HP's request
20120709 Change by HP request
20120919 Change QH11 to PMOS
Place near PCH
CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.
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Issued Date
2012/06/11
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2013/06/11
Title
PCH-RTC,HDA,SATA,XDP
Size
Custom
Document Number
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Rev
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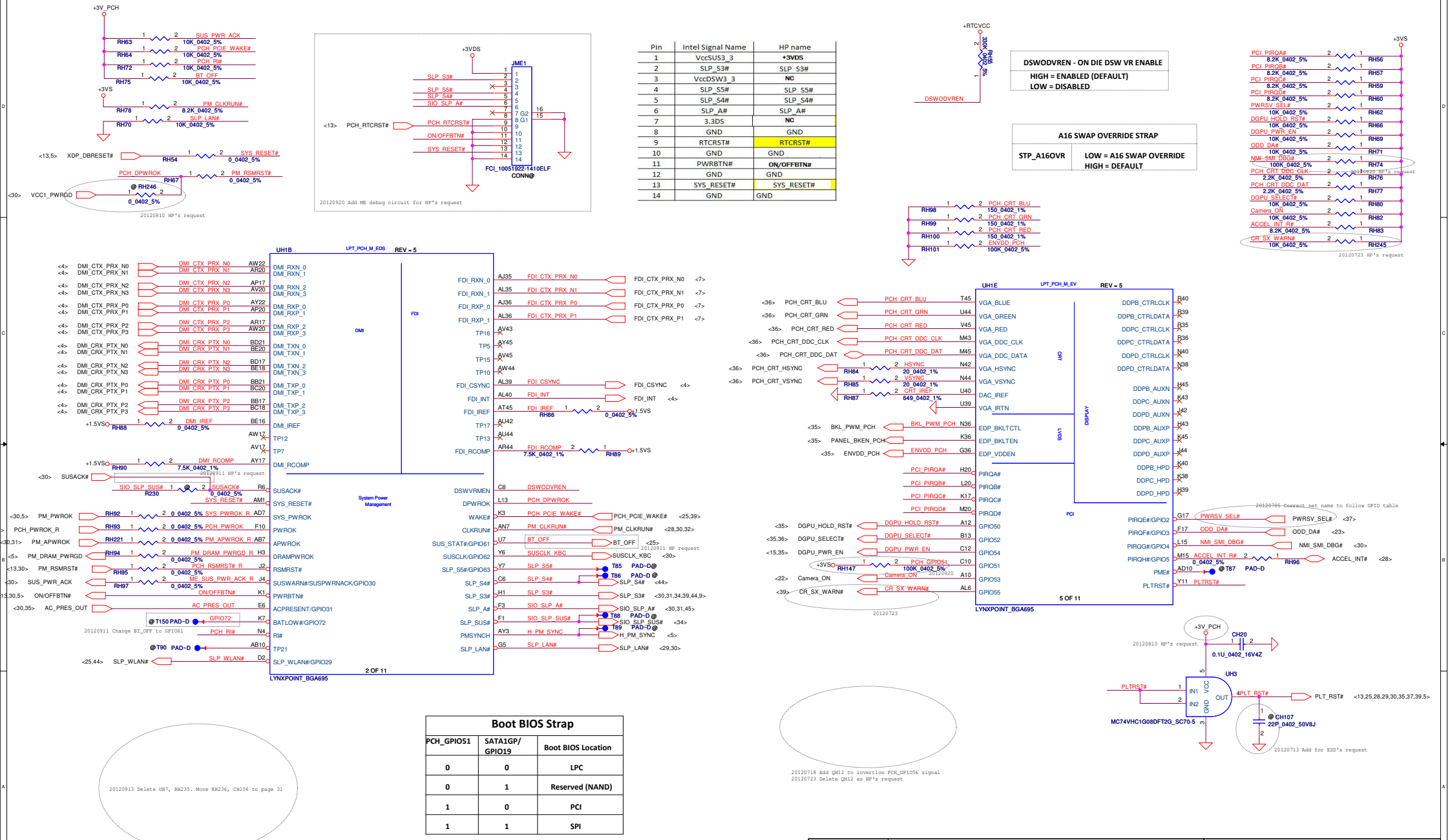
Date:
Friday, September 28, 2012
Sheet
13
of
53



Pin	Intel Signal Name	HP name
1	VccSUS3_3	+3VDS
2	SLP_S3#	SLP_S3#
3	VccDSW3_3	NC
4	SLP_S5#	SLP_S5#
5	SLP_S4#	SLP_S4#
6	SLP_A#	SLP_A#
7	3.3DS	NC
8	GND	GND
9	RTCRST#	RTCRST#
10	GND	GND
11	PWRBTN#	ON/OFFBTN#
12	GND	GND
13	SYS_RESET#	SYS_RESET#
14	GND	GND

Boot BIOS Strap

PCH_GPIO51	SATA1GP/ GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

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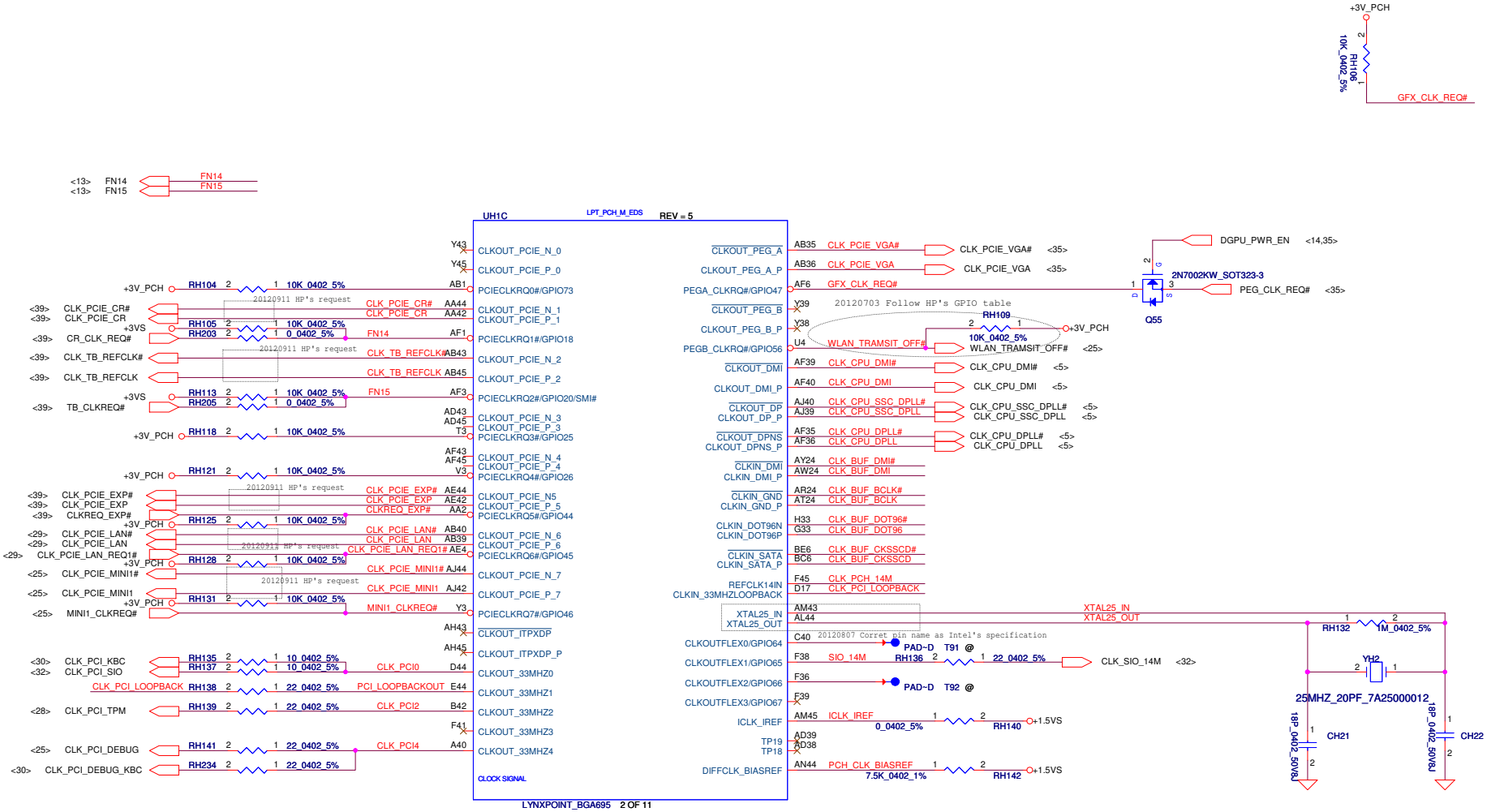
Compal Electronics, Inc.

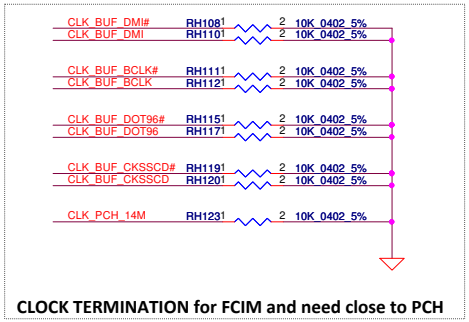
Title: PCH -DMI,FDI,PM,DP,CRT

Size: Custom | Document Number: LA-9371P | Rev: 0.2

Date: Friday, September 28, 2012 | Sheet 14 of 53



PCIECLK REQ Pull UP Power Rail:
SUS Rail : 0 3 4 5 6 7
Core Rail: 1 2



CLOCK TERMINATION for FCIM and need close to PCH

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Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title: PCH- CLK
				Size: Custom; Document Number: LA-9371P; Rev: 0.2
				Date: Friday, September 28, 2012; Sheet 15 of 53

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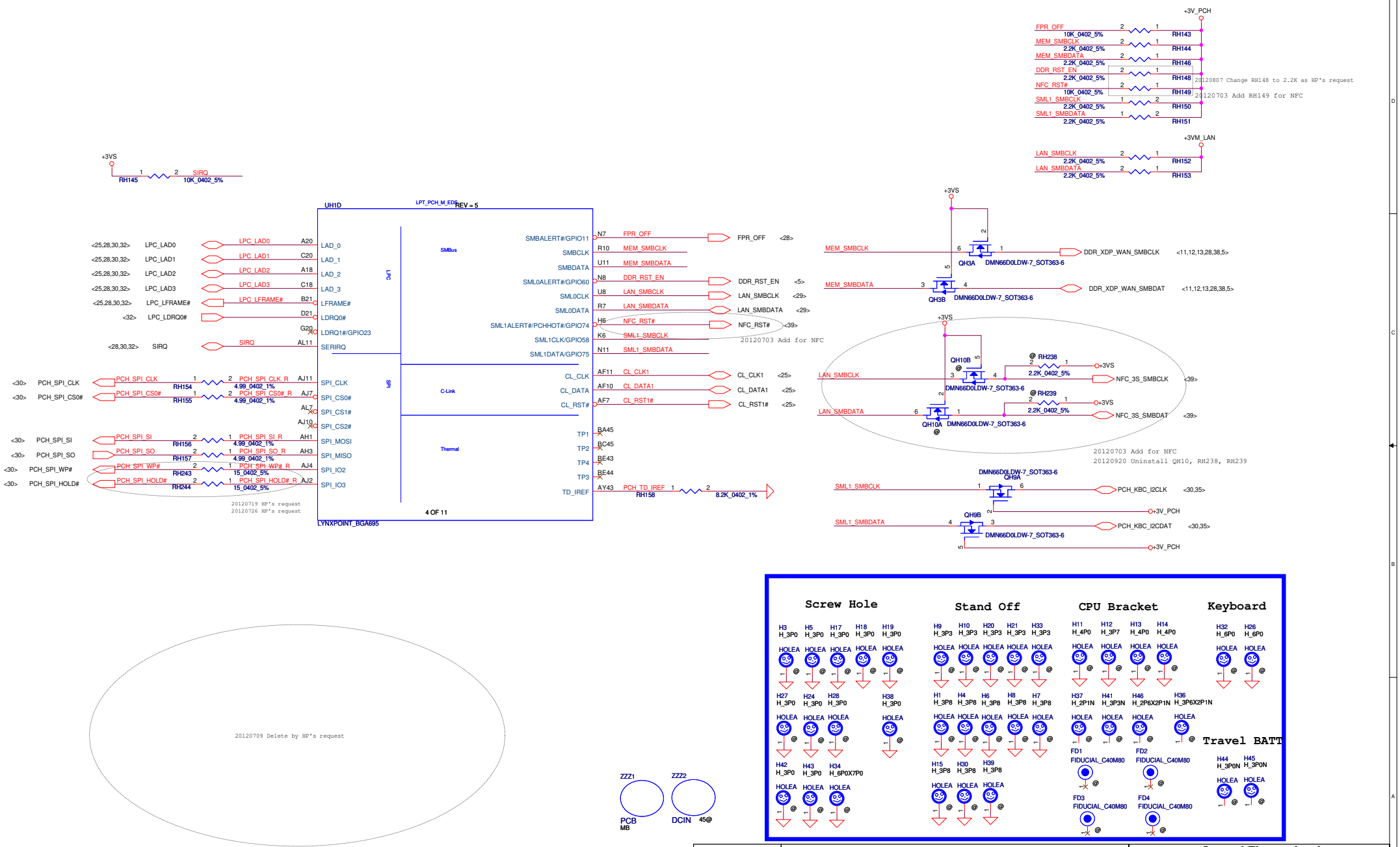

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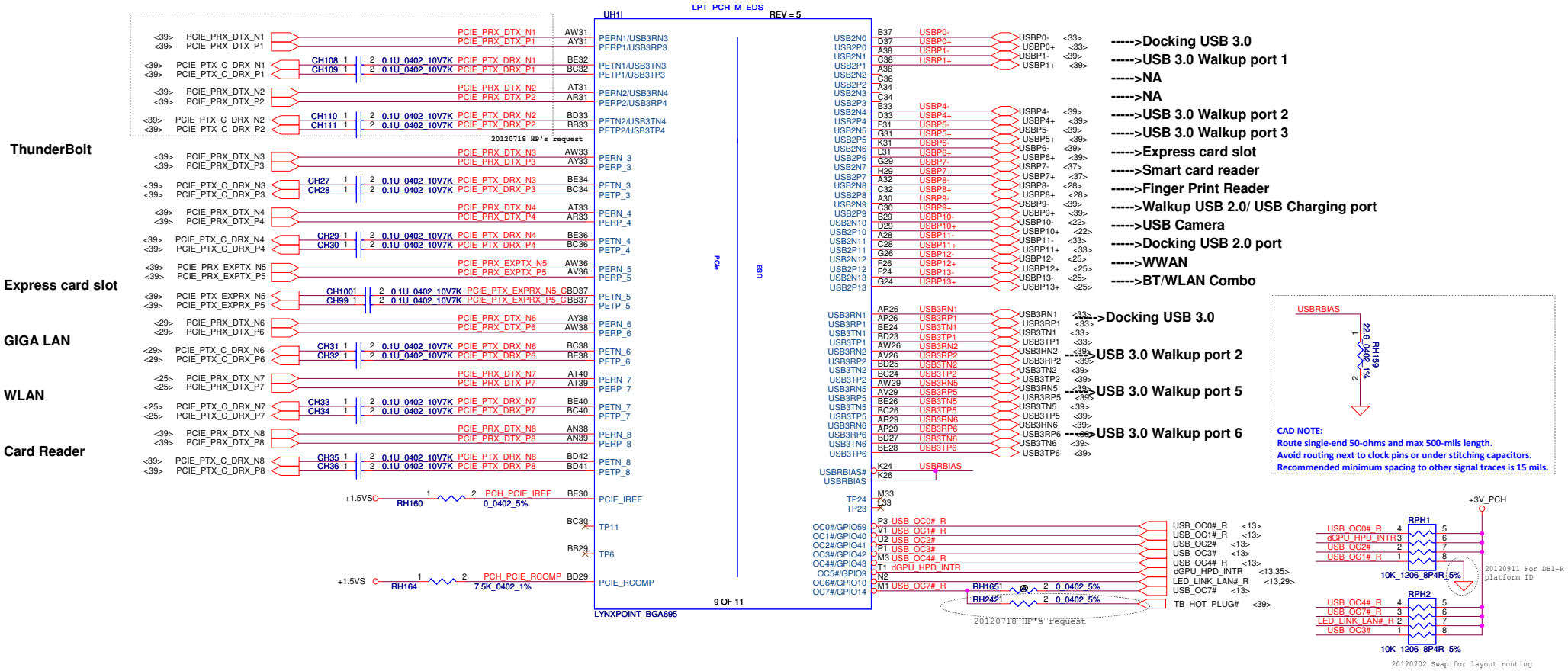
Compal Electronics, Inc.

Title: PCH - SPI, SMBUS,LPC

Size: Custom | Document Number: LA-9371P | Rev: 0.2

Date: Friday, September 28, 2012 | Sheet 16 of 53



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Issued Date	2012/06/11	Deciphered Date	2013/06/11

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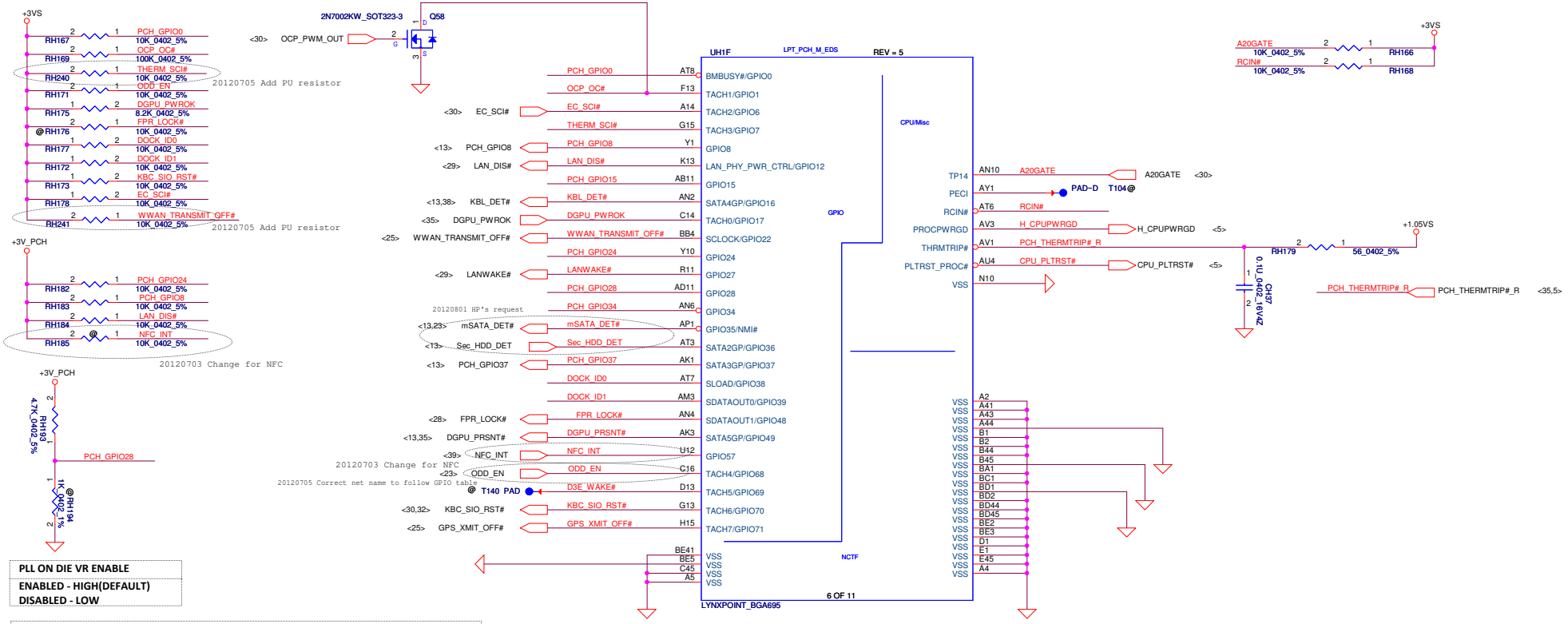
Compal Electronics, Inc.

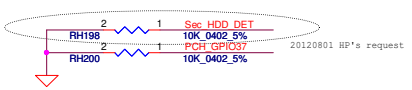
Title: PCH-PCIE,USB

Size: Custom | Document Number: LA-9371P | Rev: 0.2

Date: Friday, September 28, 2012 | Sheet 17 of 53

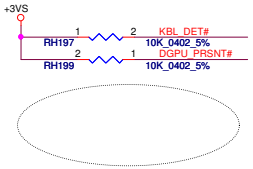


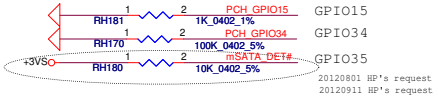
PLL ON DIE VR ENABLE
ENABLED - HIGH(DEFAULT)
DISABLED - LOW



SATA2GP/GPIO36 , SATA3GP/GPIO37 SAMPLED AT RISING EDGE OF PWROK.
WEAK INTERNAL PULL-DOWN.(WEAK INTERNAL PULL-DOWN IS DISABLED AFTER PLRST_N DE-ASSERTS).
NOTE: THIS SIGNAL SHOLD NOT BE PULLED HIGH WHEN STRAP IS SAMPLED.

Config	GPIO16,49
USB X4,PCIEX8,SATAX6	11
USB X6,PCIEX8,SATAX4	01





Board ID	BRD_ID1 GPIO15	BRD_ID2 GPIO34	BRD_ID3 GPIO35	BRD_ID4 GPIO40
DB0	0	0	0	0
DB1	0	0	0	1
DB2	0	0	1	0
SI1	0	1	0	0
SI1B	0	1	0	1
SI2	0	1	1	0
PV1	1	0	0	0
MV	1	1	0	0

Fixed Signals				Muxed Signals		Fixed Signals						Muxed Signals		Fixed Signals			
USB3 1	USB3 2	USB3 5	USB3 6	PCIE 1 (00)	PCIE 2 (00)	PCIE 3	PCIE 4	PCIE 5	PCIE 6	PCIE 7	PCIE 8	SATA 4 (00)	SATA 5 (00)	SATA 0	SATA 1	SATA 2	SATA 3
				USB3 3 (01)	USB3 4 (01)							PCIE 1 (01)	PCIE 2 (01)				

Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

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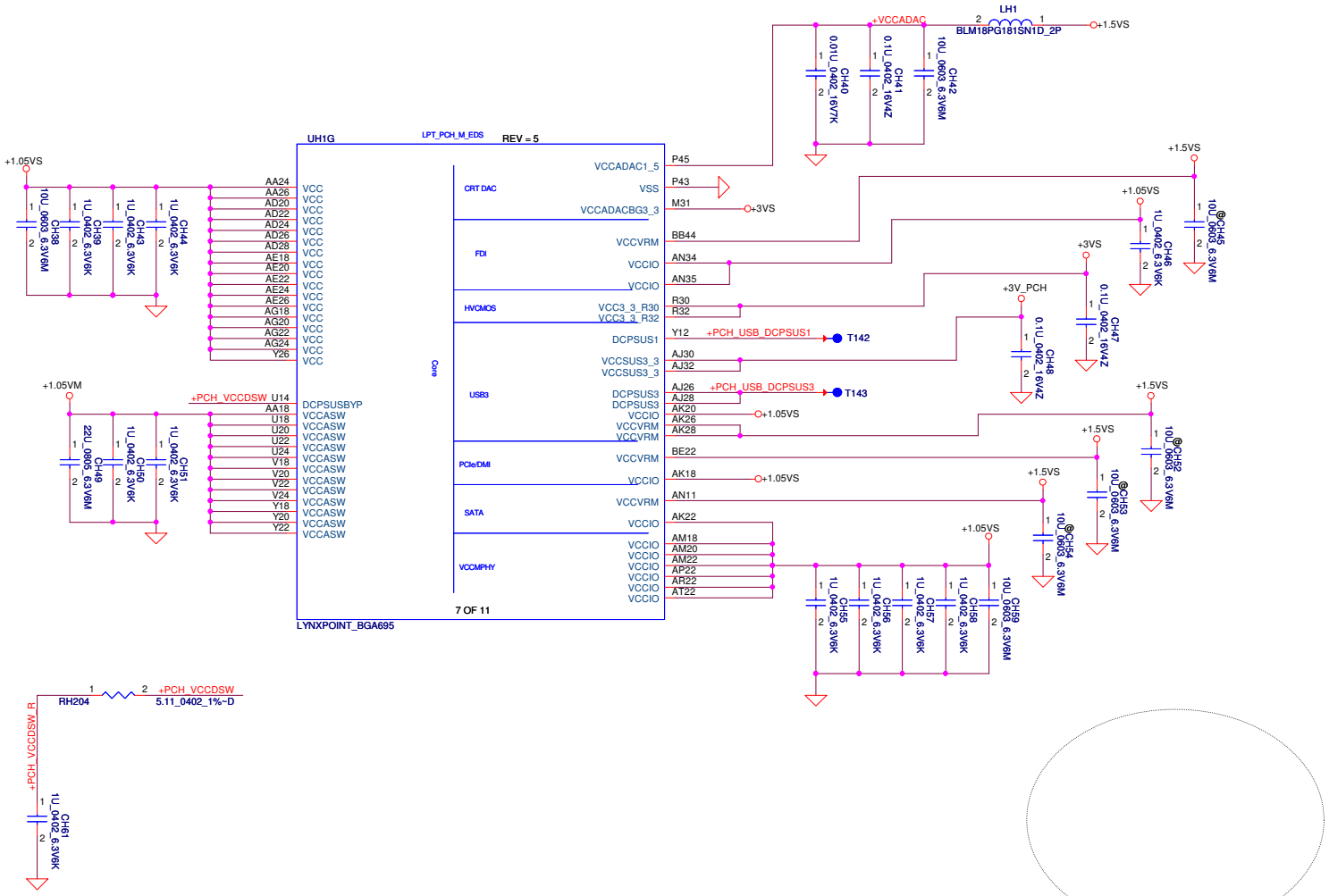
Compal Electronics, Inc.

Title: PCH -GPIO,MISC,NTFC

Size: Custom | Document Number: LA-9371P | Rev: 0.2

Date: Friday, September 28, 2012 | Sheet 18 of 53



20120720 Delete CH60, CH62, CH63 as HP's request

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title: PCH- Power
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				Date: Friday, September 28, 2012; Sheet 19 of 53

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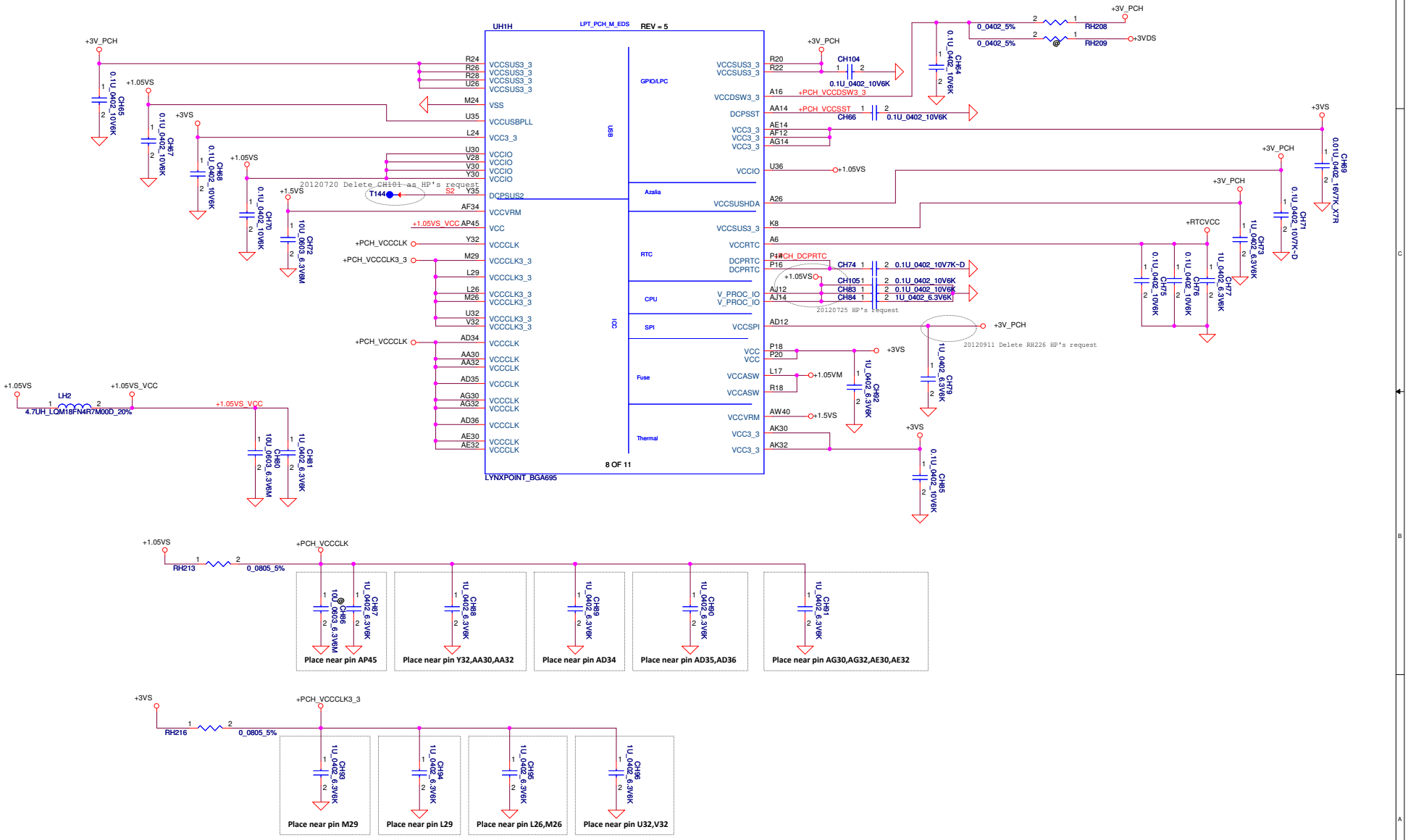

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title: PCH - Power
				Size: Custom; Document Number: LA-9371P; Rev: 0.2
				Date: Friday, September 28, 2012; Sheet 20 of 53

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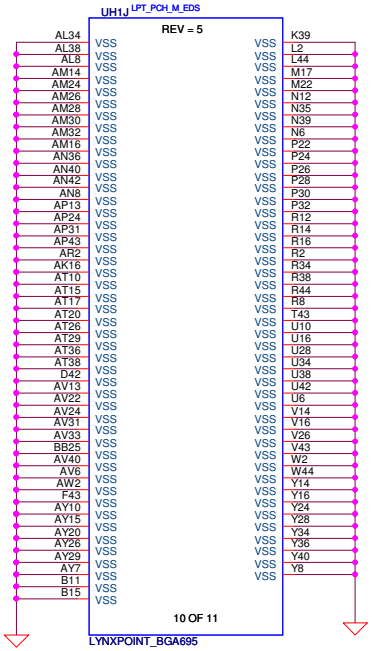

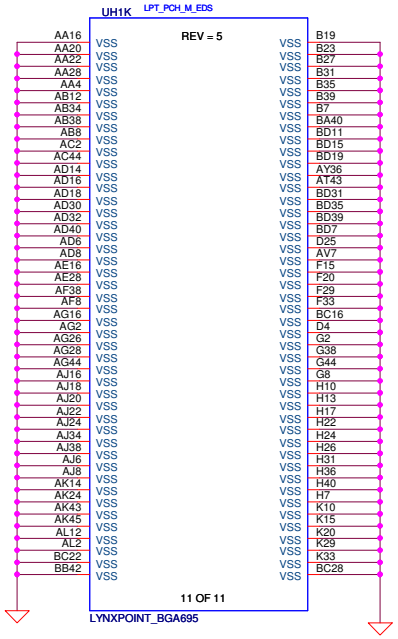

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Issued Date	2012/06/11	Deciphered Date 2013/06/11	Title PCH - GND
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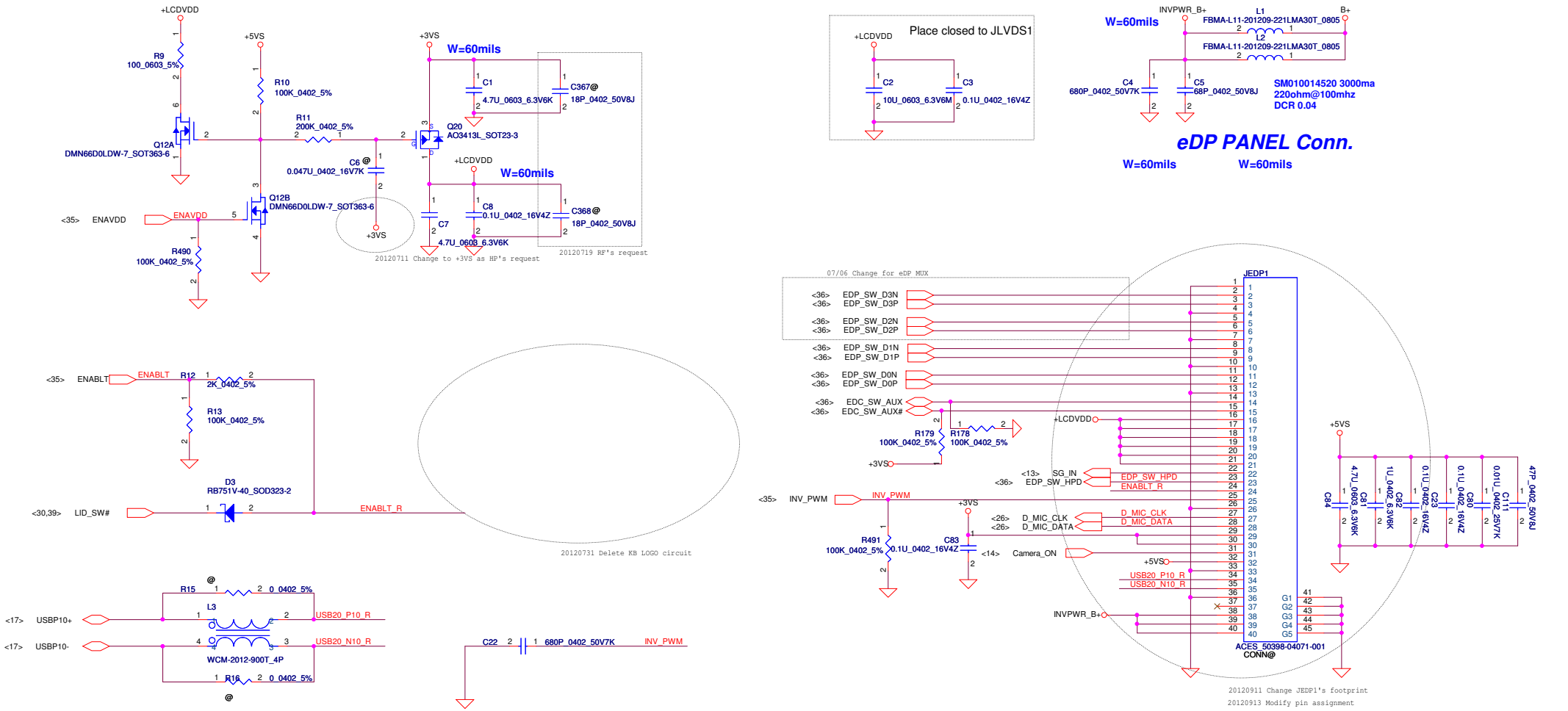
			Date: Friday, September 28, 2012 / Sheet 21 of 53

LCD POWER CIRCUIT



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Issued Date	2012/06/11	Deciphered Date	2013/06/11

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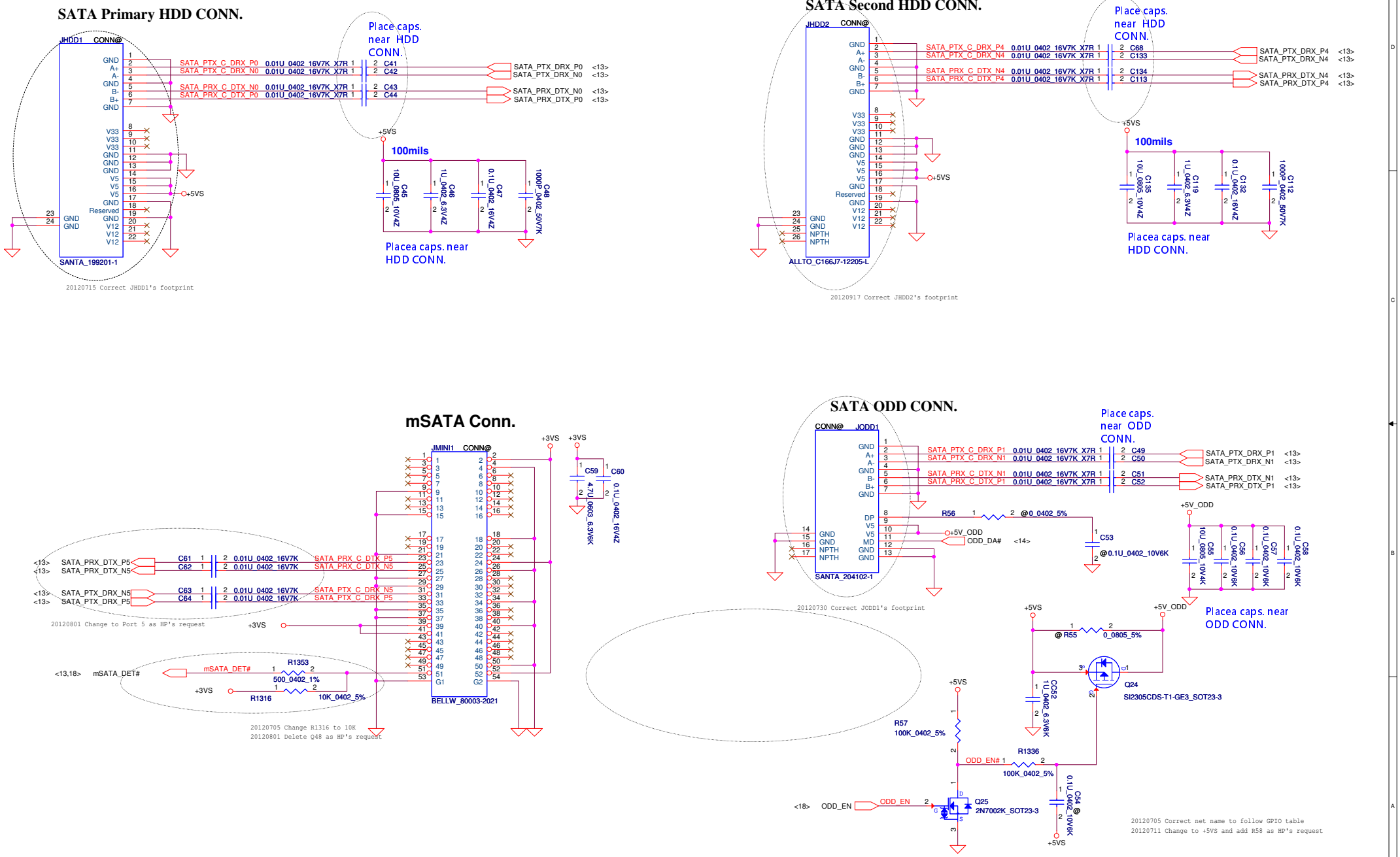
Compal Electronics, Inc.

Title: **eDP/LVDS CONN & Camera**

Size | Document Number: **LA-9371P** | Rev 0.2

Date: Friday, September 28, 2012 | Sheet 22 of 53



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title: IBEX-M(1/6)-HDA/JTAG/SATA
				Size: Custom; Document Number: LA-9371P; Rev: 0.2
				Date: Friday, September 28, 2012; Sheet 23 of 53

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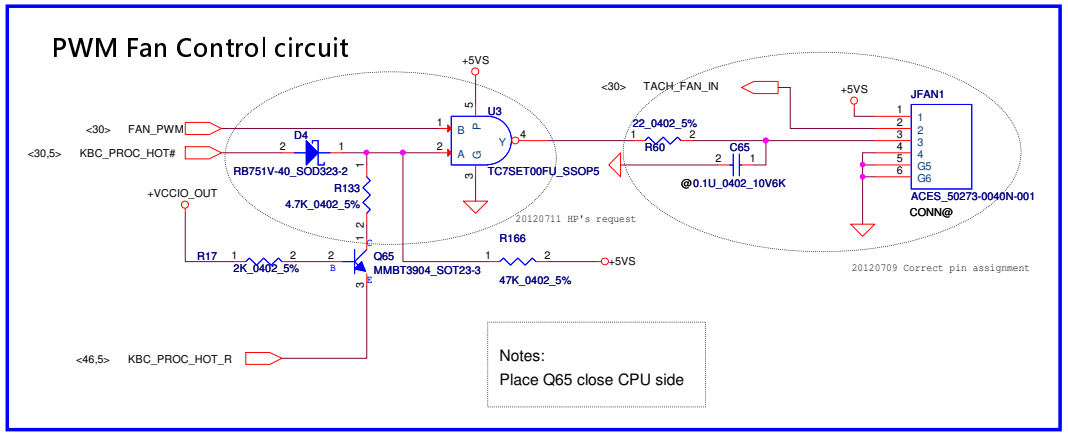

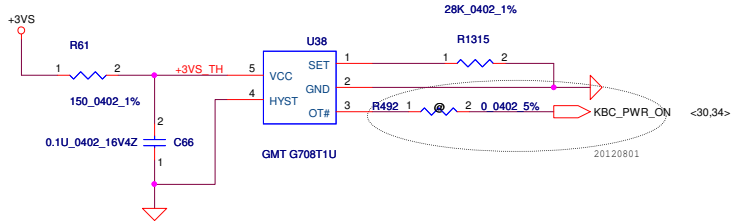

Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

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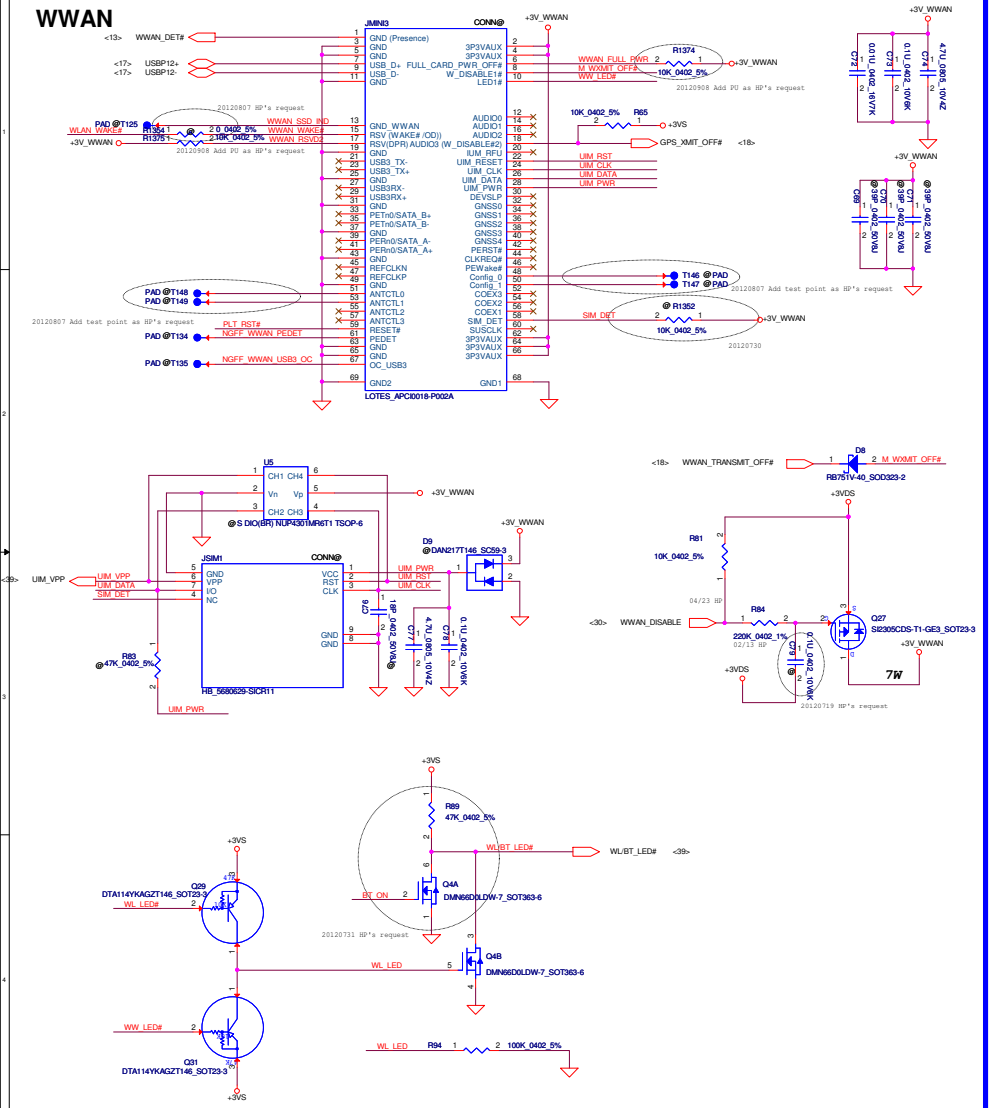
Compal Electronics, Inc.

Title: **Sandy(2/7) PM,XDP,Thermal**

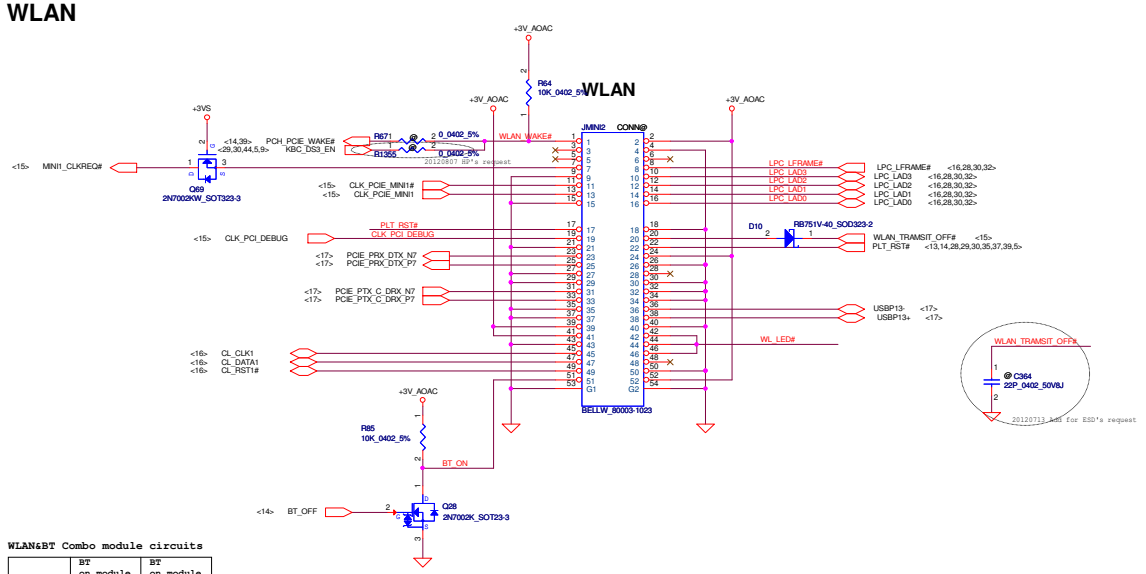
Size: Custom | Document Number: LA-9371P | Rev: 0.2

Date: Friday, September 28, 2012 | Sheet 24 of 53

WWAN



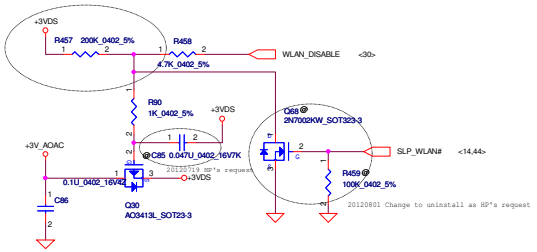
WLAN



WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CRTL	HI	LO
BT_ON#	LO	HI

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title: WWAN/NAND mini

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Document Number	Rev
LA-9371P	0.2

Date: Friday, September 28, 2012 Sheet 25 of 53

Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

Place AVDD ,PVDD,and DVDD capacitor close to Codec

CA8,CA10 near UA5 PIN45
CA9,CA21 near UA5 PIN39

PLACE CLOSE TO U1 PIN 13

If Sense_A total length is greater than 6 inches, chagne C12 to 0.1uF

RA3 2.49K_0402_1% SENSE_A CA1 1000P_0402_50V7K +AVDD_CODEC

SENSE_B RA4 2.49K_0402_1% +AVDD_CODEC CA13 1000P_0402_50V7K

PLACE CLOSE TO U1 PIN 14

If Sense_B is un-used, then pull high Sense_B to AVDD by 10Kohm resistor

External MIC
Combo Jack
Headphone

Internal SPKR(front stereo speaker)

20120702 Delete MIC_SENSE# circuit

20120702 Delete MUTE circuit

Place C209,C210,CA87,CA89 close to Codec

20120920 HP's request

20120719 HP's request

SB Beep

RA53 need under or near UA1

GND GNDA

Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

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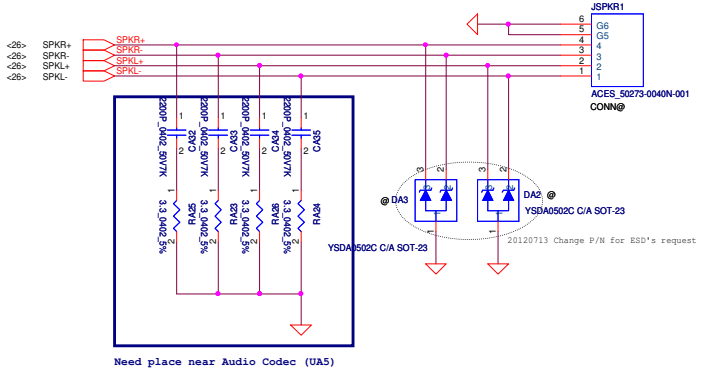
Compal Electronics, Inc.

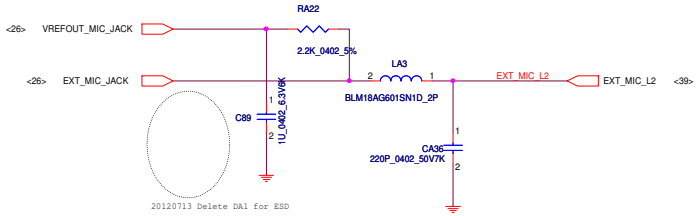
Title: Audio IDT 92HD91

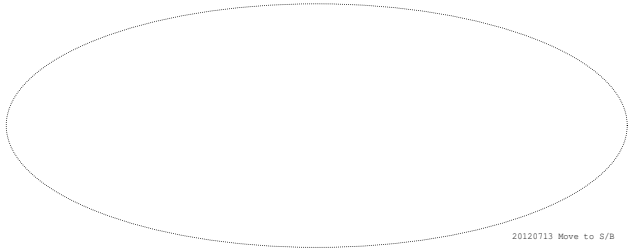
Size: Custom | Document Number: LA-XXXXP | Rev: 0.2

Date: Friday, September 28, 2012 | Sheet 26 of 53

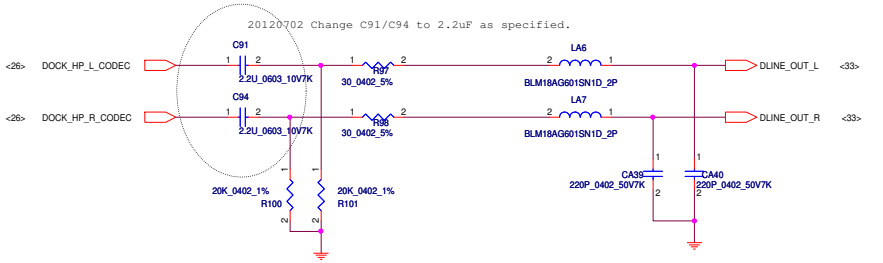
Speaker Connector

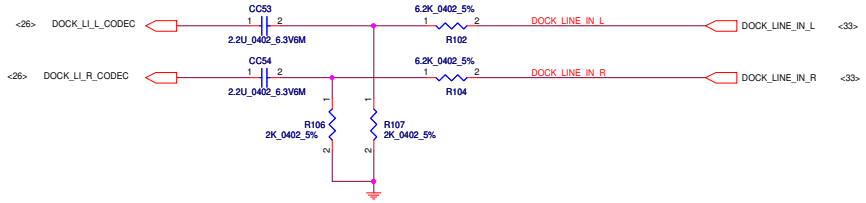


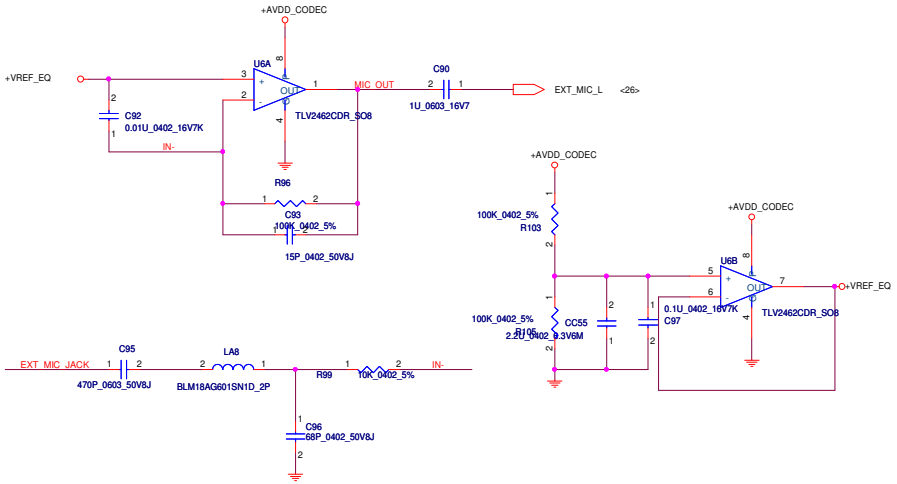


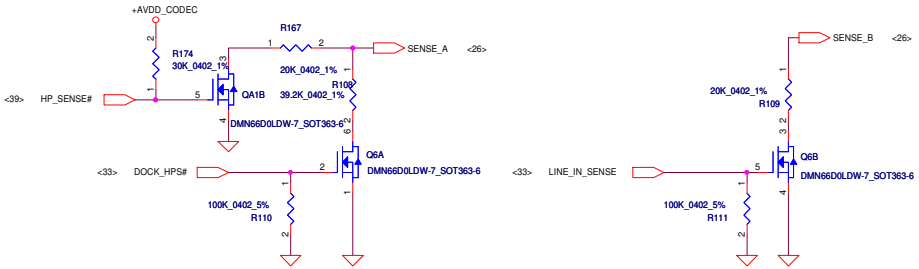


DOCK Audio









Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title: Audio SPK Conn/Jack/MIC
				Size: C; Document Number: LA-9371P; Rev: 0.2
				Date: Friday, September 28, 2012; Sheet 27 of 53

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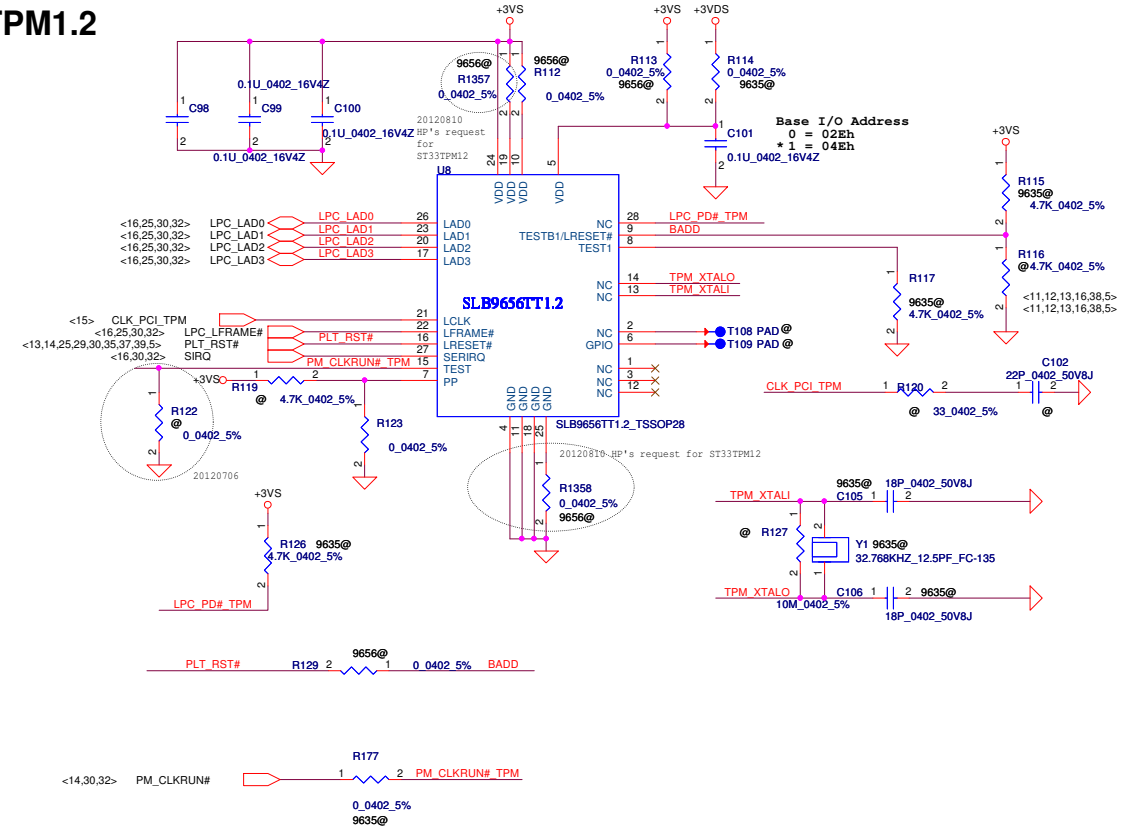
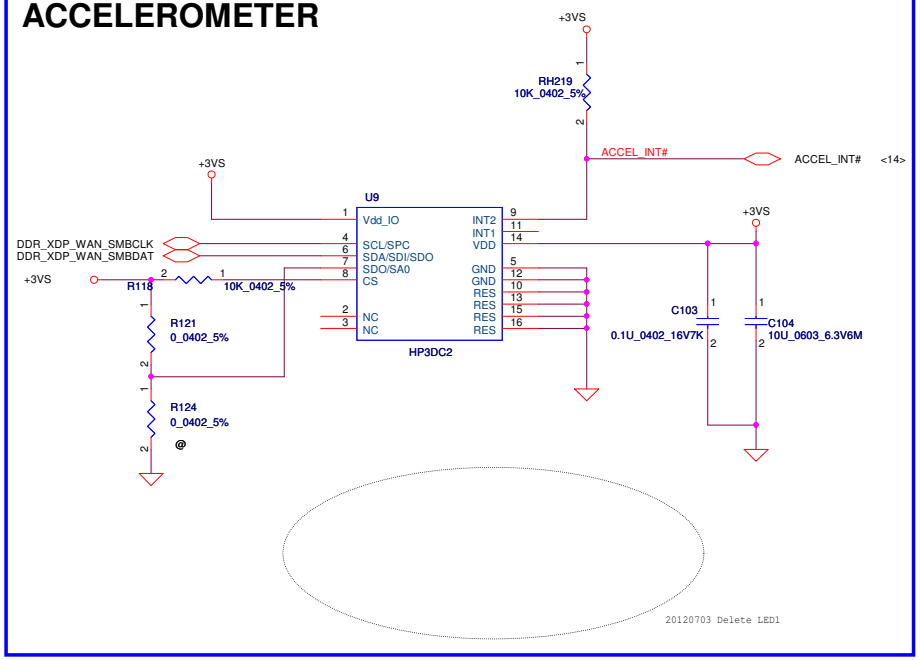
TPM1.2

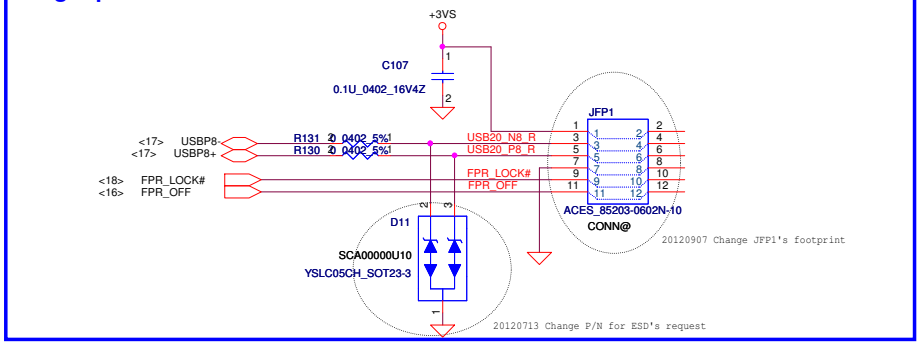


TPM	BOM Option (Not Install)
SLB9635	R112, R113, R129
SLB9656	R114, R115, R117, R126, R177, C105, C106, Y1
ST33TPM12	R113, R129,R114, R115, R117, R126, R177, R1357, R1358,R127,R122,R116,R120, C102, C101, C105, C106, Y1

ACCELEROMETER



Finger printer



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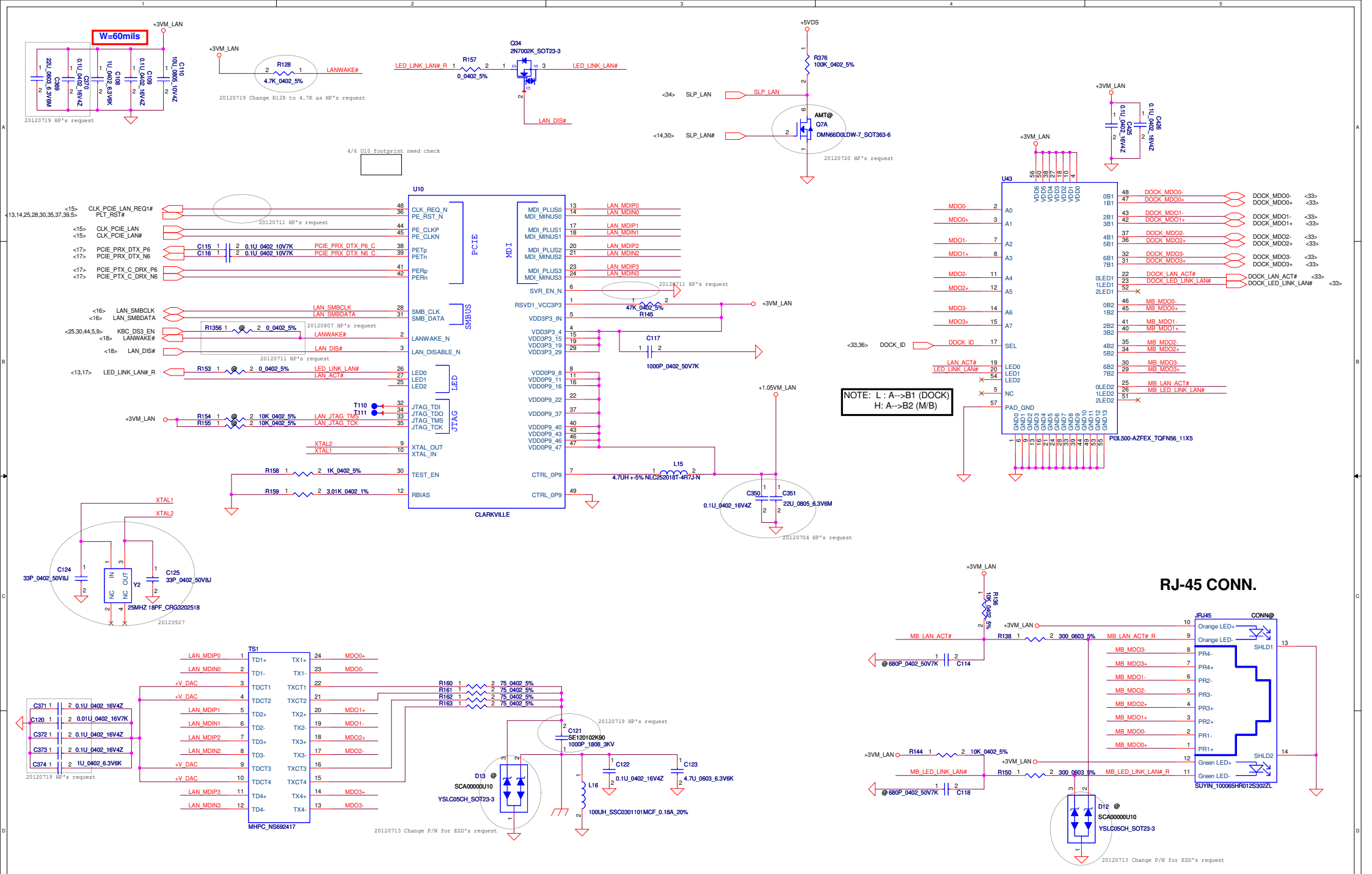
Compal Electronics, Inc.

Title: TPM/Gsensor

Size: A3 | Document Number: LA-9371P | Rev: 0.2

Date: Friday, September 28, 2012 | Sheet 28 of 53



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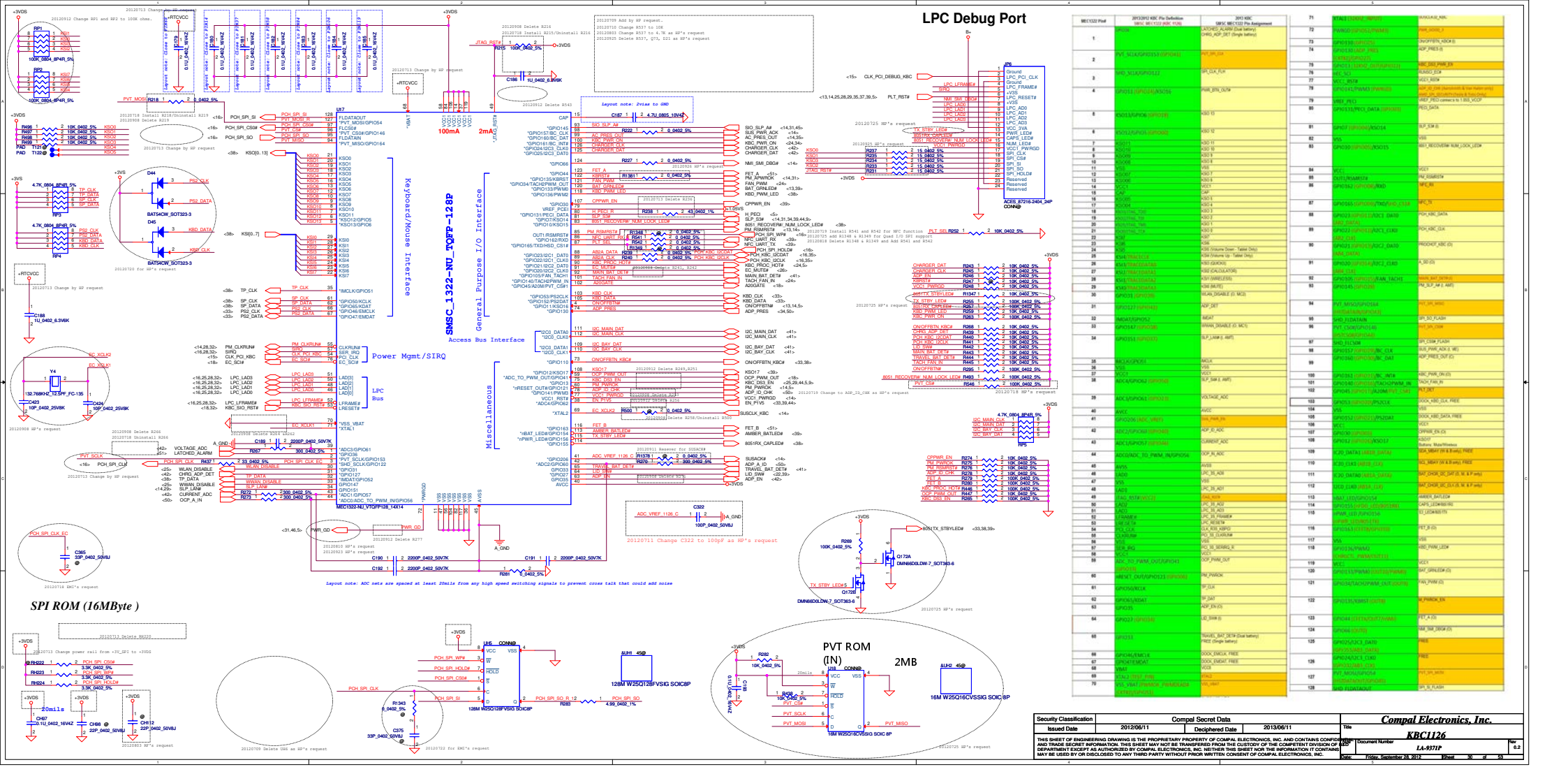
Compal Electronics, Inc.

Title: **Intel 82566 Nineveh**

Size: | Document Number: *LA-9371P* | Rev: 0.2

Date: Friday, September 28, 2012 | Sheet 29 of 53



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Issued Date	2012/06/11	Deciphered Date	2013/06/11

Title: KBC1126

Compal Electronics, Inc.

Document Number: LA-9371P

Rev: 0.2

Date: Friday, September 28, 2012 Sheet 30 of 53

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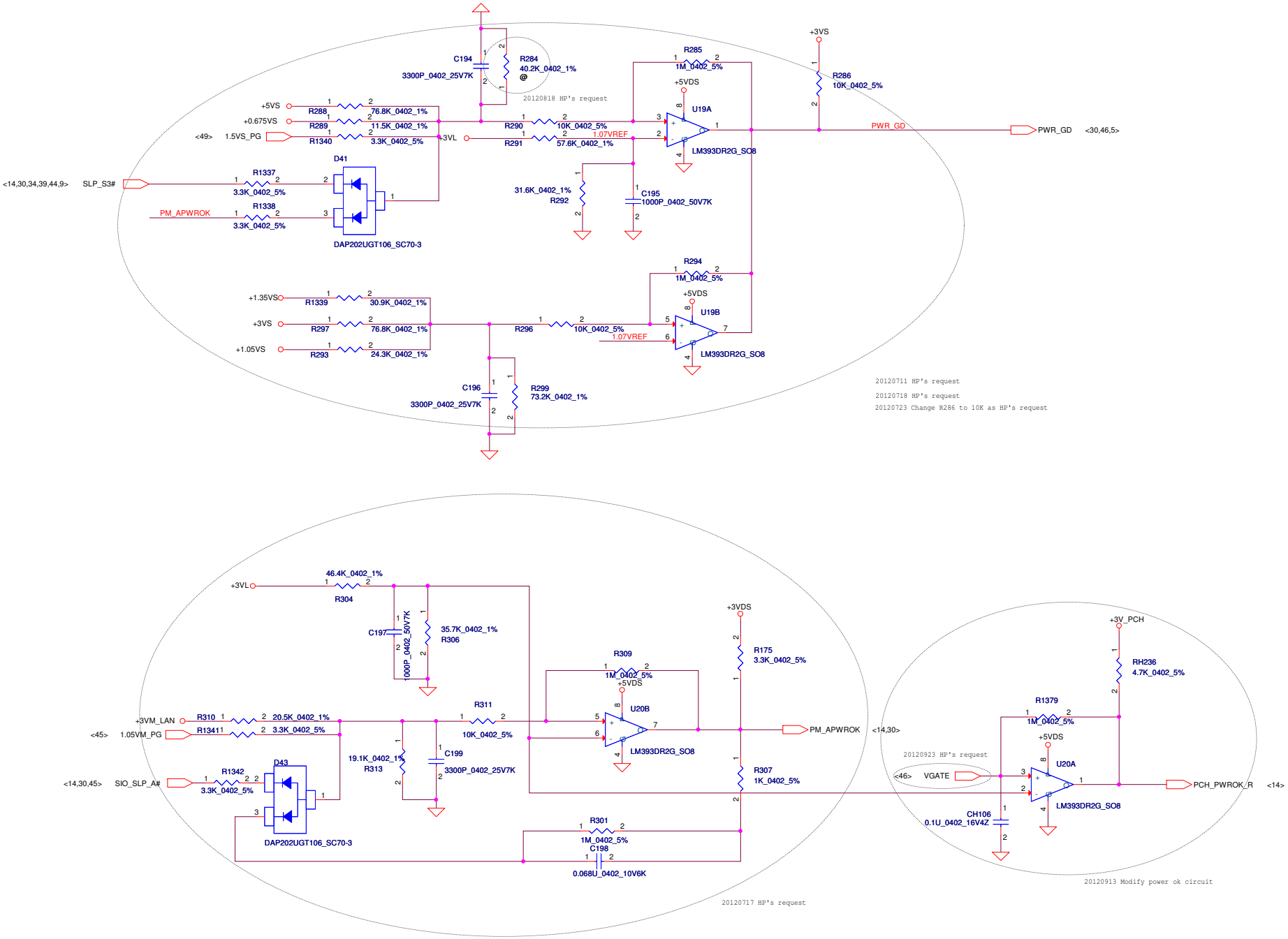

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Issued Date	2012/06/11	Deciphered Date	2013/06/11	Title: POK CKT
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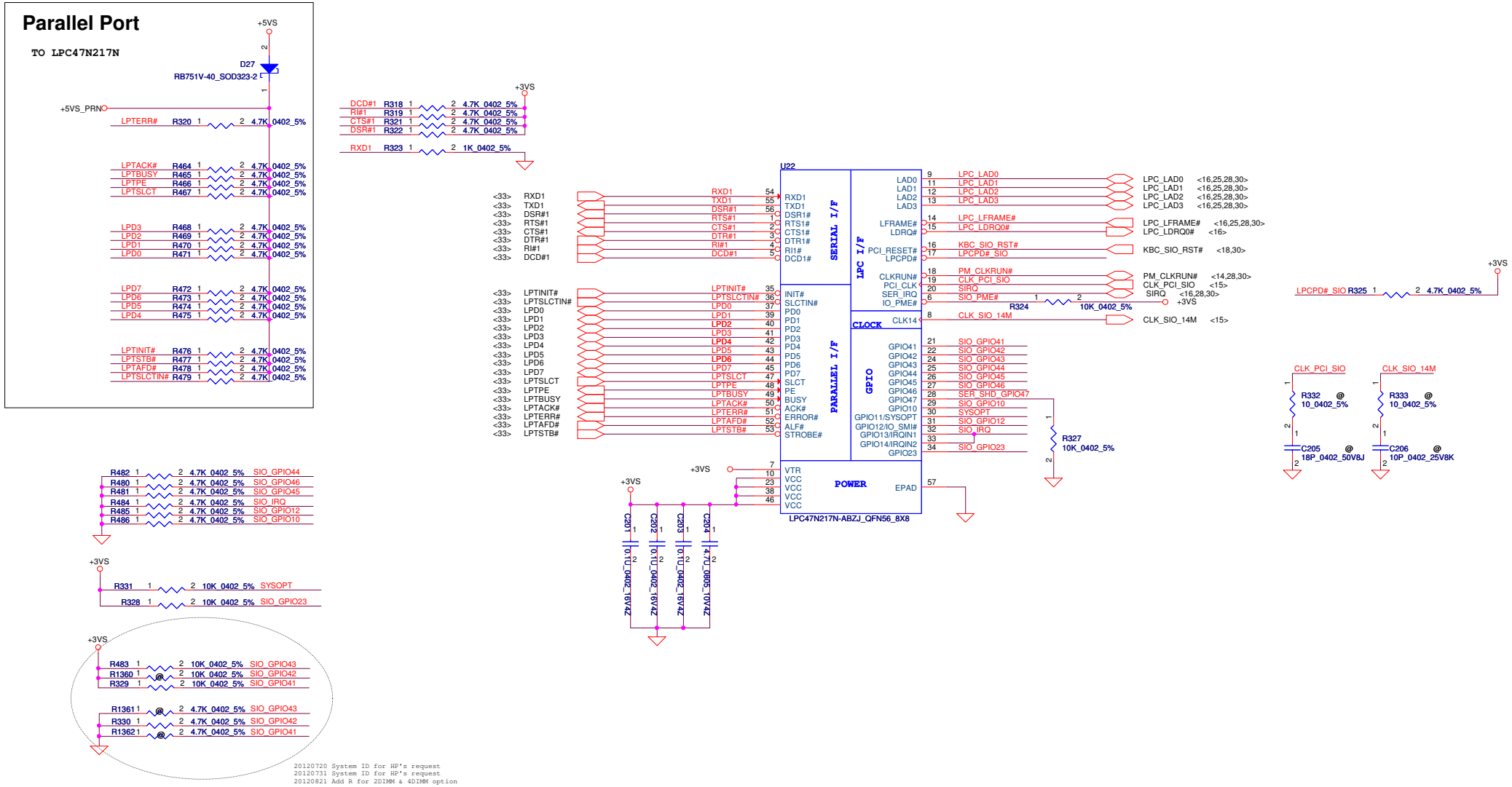
				Date: Friday, September 28, 2012; Sheet 31 of 53



Platform IDs (Super I/O GPIOs)

PLT_ID1	PLT_ID2	PLT_ID3					
GPIO43	GPIO42	GPIO41	SYSTEM ID	Series	CPU	Dock	COMMON BIOS
1	0	1	Afterburner 17" 4 DIMM	W	Haswell	Common	8
1	1	1	Afterburner 17" 2 DIMM	W	Haswell	Common	8

Security Classification	Compal Secret Data		
Issued Date	2012/06/11	Deciphered Date	2013/06/11

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Compal Electronics, Inc.

Title: **SUPER I/O LPC47N217N-ABZJ**

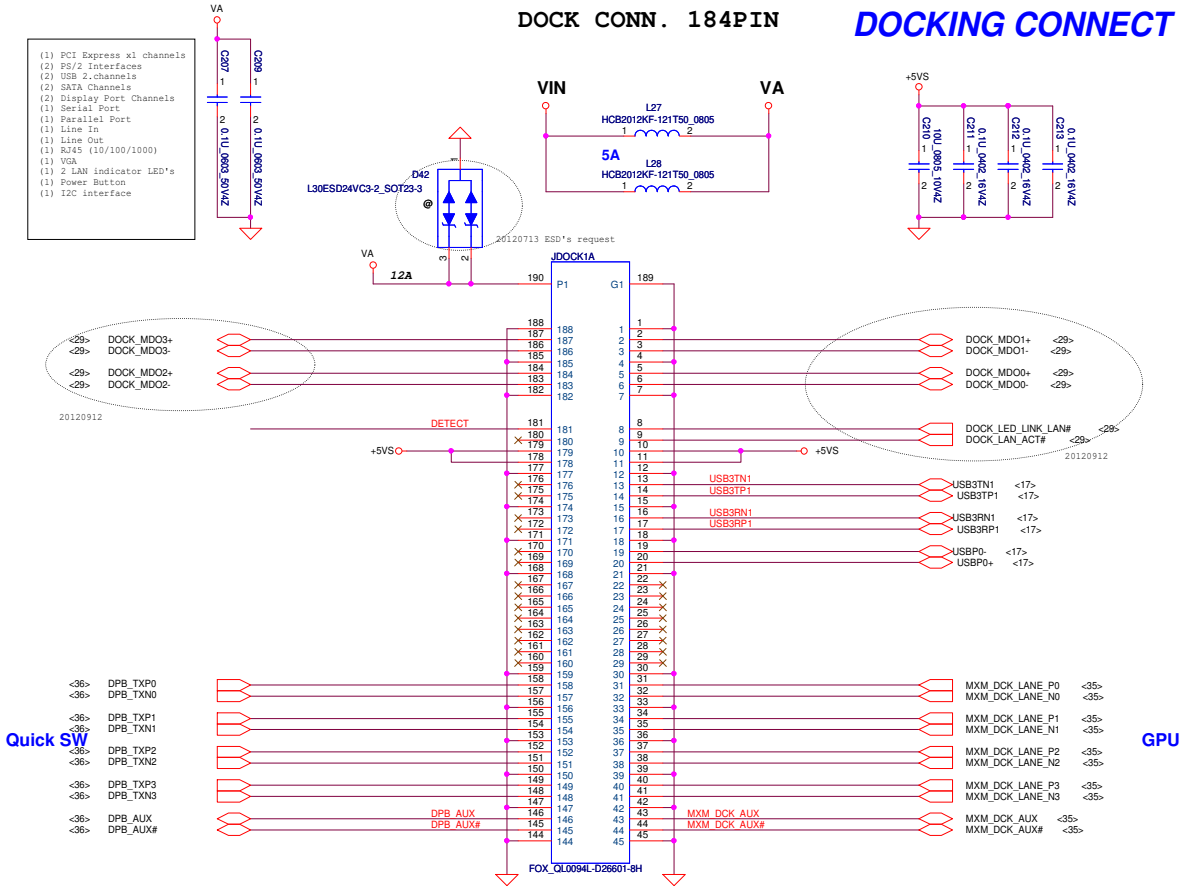
Document Number: LA-9371P | Rev: 0.2

Date: Friday, September 28, 2012 | Sheet 32 of 53

DOCK CONN. 184PIN

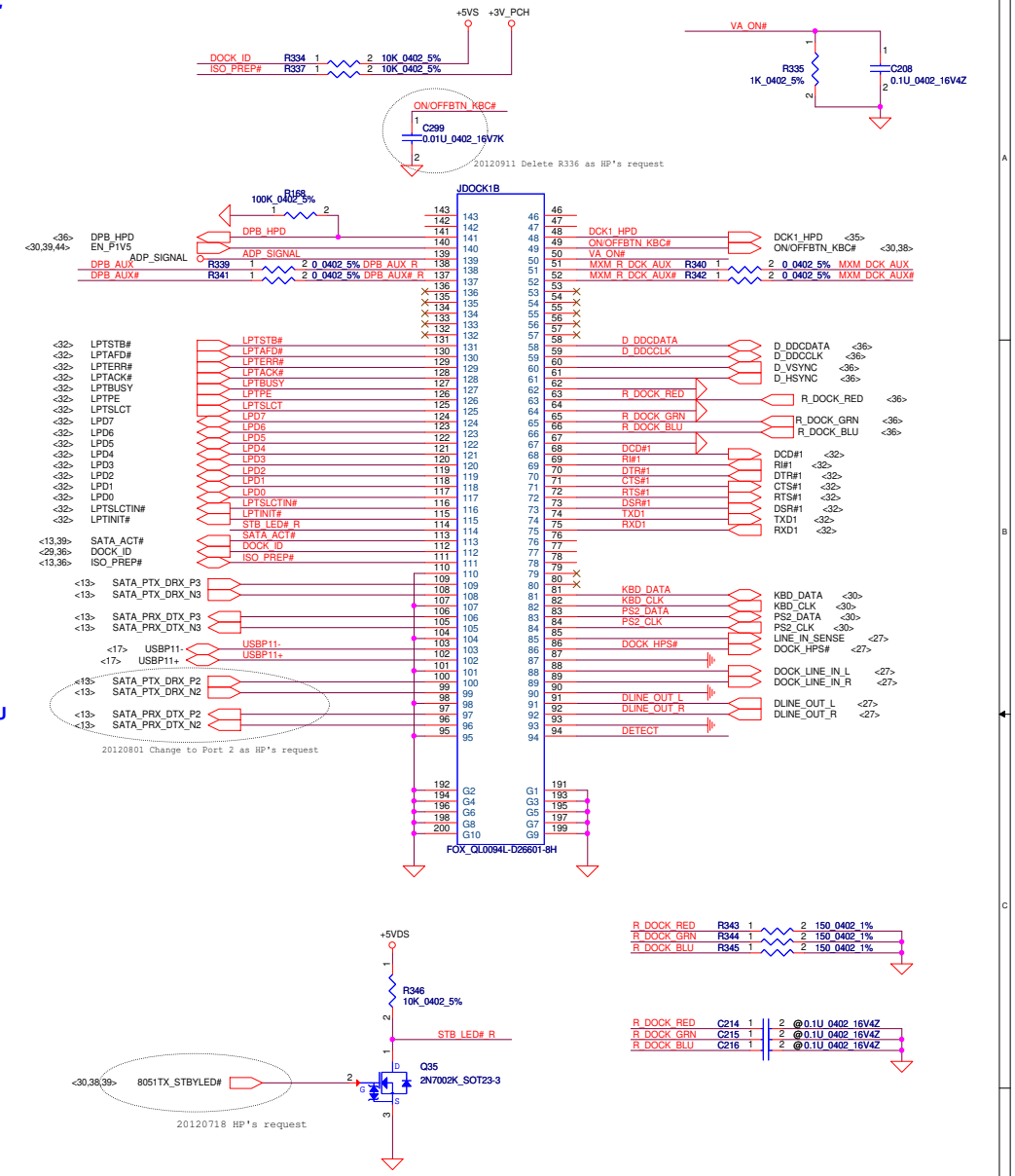
DOCKING CONNECT

(1) PCI Express x1 channels
(2) PS/2 Interfaces
(2) USB 2.channels
(2) SATA Channels
(2) Display Port Channels
(1) Serial Port
(1) Parallel Port
(1) Line In
(1) Line Out
(1) RJ45 (10/100/1000)
(1) VGA
(1) 2 LAN indicator LED's
(1) Power Button
(1) I2C interface



Quick SW

GPU



IN	NC<-->COM	NO<-->COM
L	ON	OFF
H	OFF	ON

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Compal Electronics, Inc.

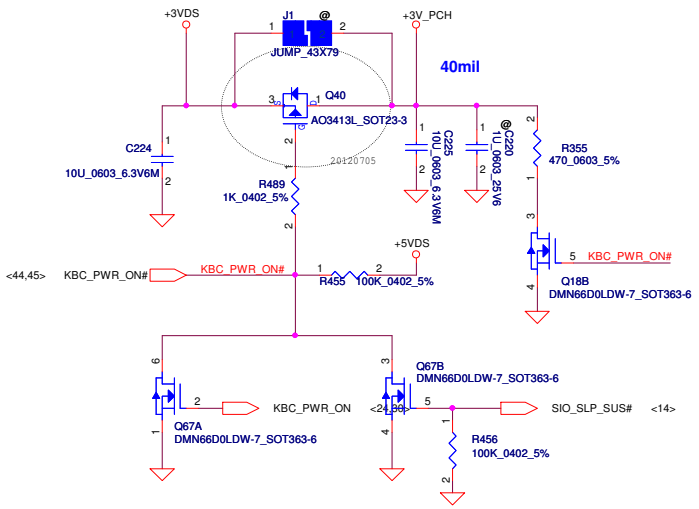
Title: DOCK CONN

Size: Custom | Document Number: LA-9371P | Rev: 0.2

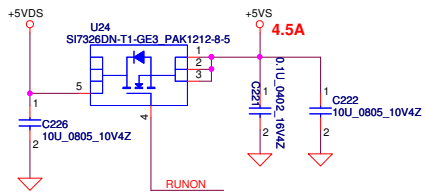
Date: Friday, September 28, 2012 | Sheet 33 of 53

+3VALW TO +3VALW(PCH AUX Power)

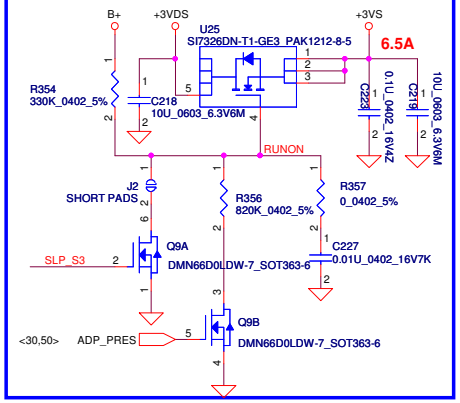
Short J1 for PCH VCCSUS3.3



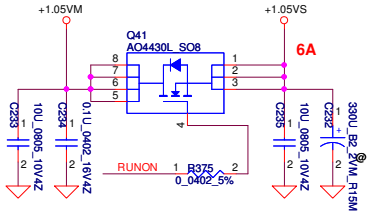
+5VALW to +5VS Transfer



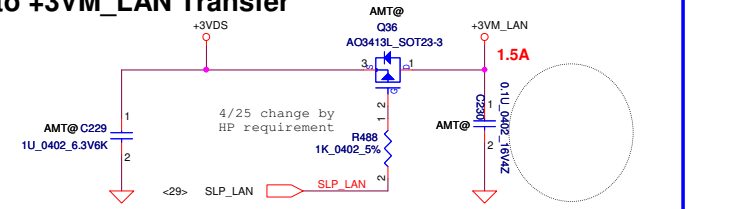
+3VALW to +3VS Transfer

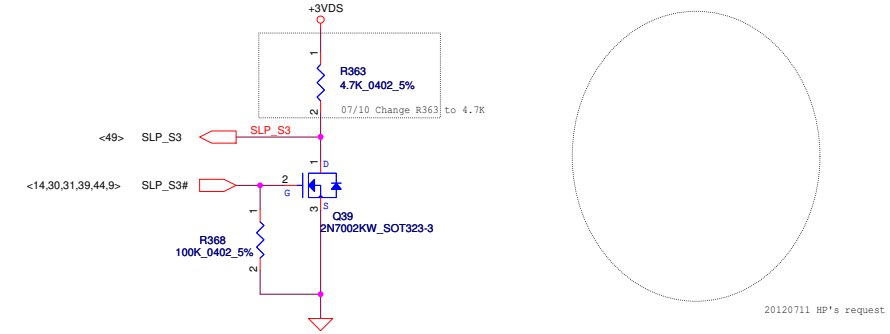


+1.05VM to +1.05VS Transfer

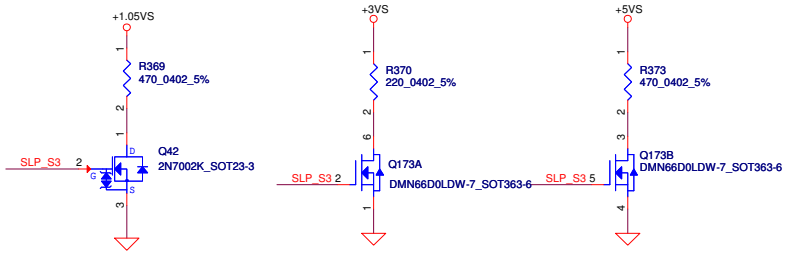


+3VALW to +3VM_LAN Transfer

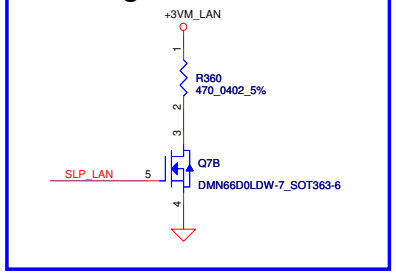


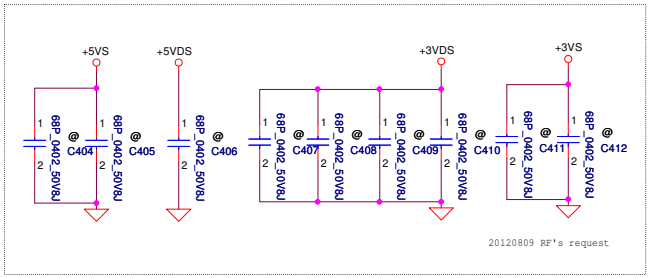


Discharge circuit-1



Discharge circuit-2 for V-M





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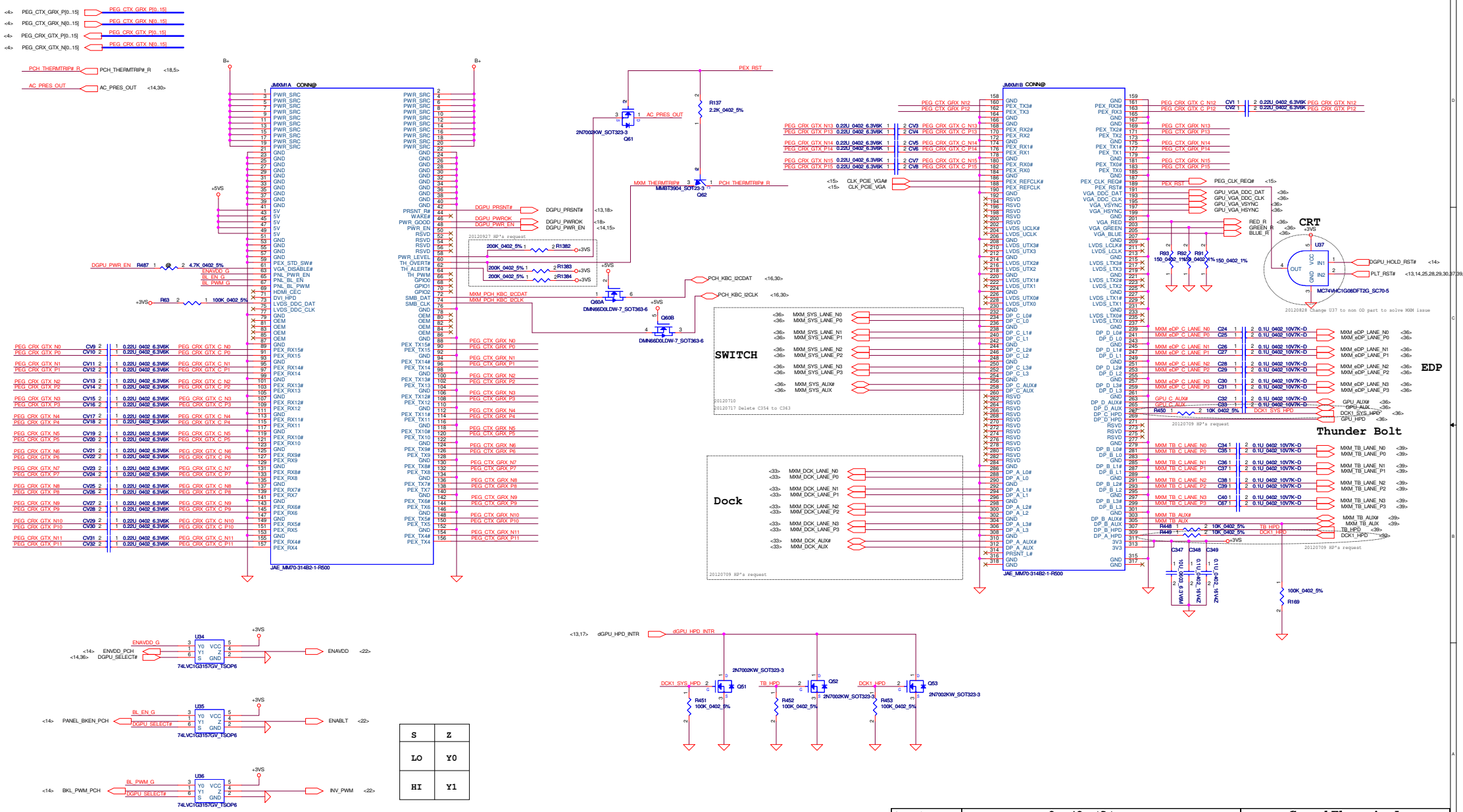
Compal Electronics, Inc.

Title: **DC/DC Circuits**

Size | Document Number: LA-9371P | Rev: 0.2

Date: Friday, September 28, 2012 | Sheet 34 of 53



S	Z
LO	Y0
HI	Y1

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Compal Electronics, Inc.

Title: **MXM**

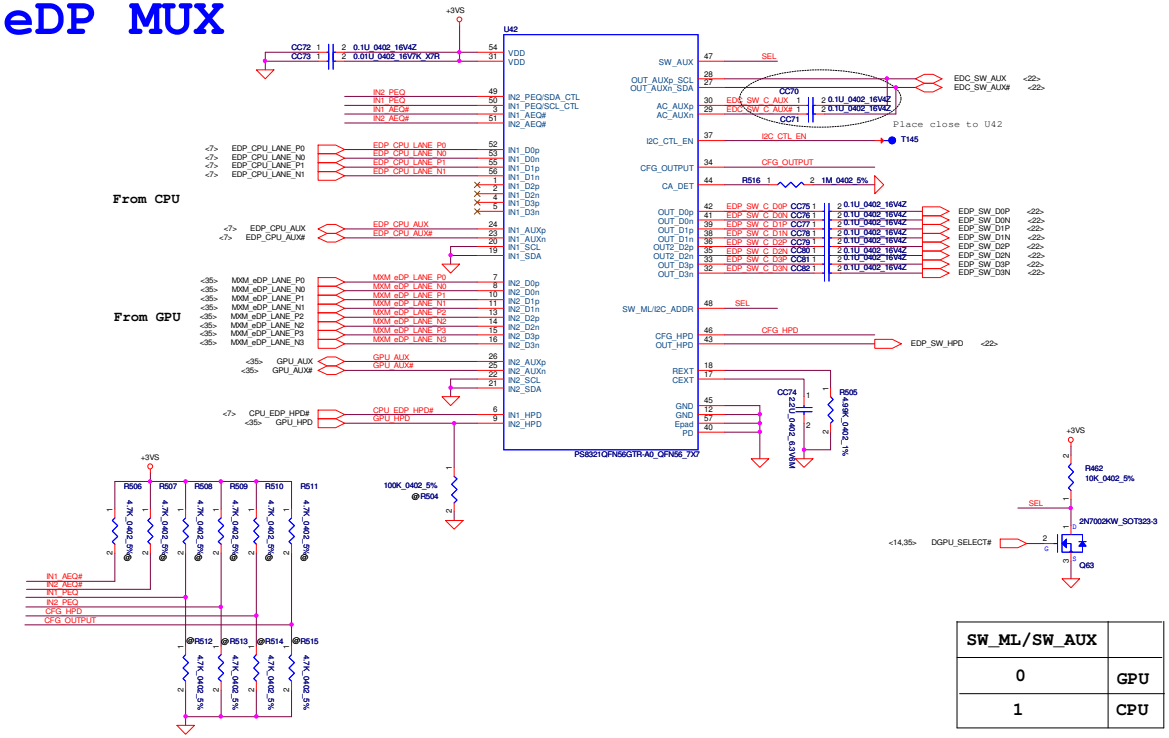
Document Number: LA-9371P

Rev: 0.2

Date: Friday, September 28, 2012

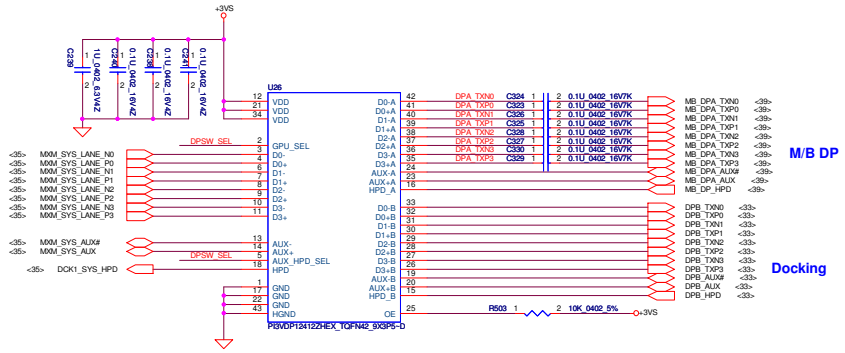
Sheet 35 of 53

eDP MUX



SW_ML/SW_AUX	
0	GPU
1	CPU

DP Switch



Truth Table for 42 pin package

OE	GPU_SEL	AUX_HPD_SEL	Function
High	Low	Low	Port A active for all channels
High	Low	High	Port A for HS, port B for HPD/AUX
High	High	Low	Port B for HS, port A for HPD/AUX
High	High	High	Port B active for all channels
Low	x	x	All I/O's are hi-z and IC is power down

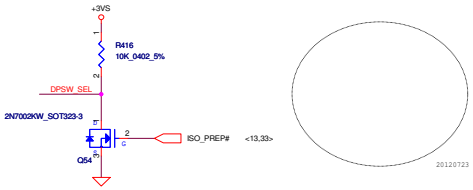


Table 1. DDC Truth Table

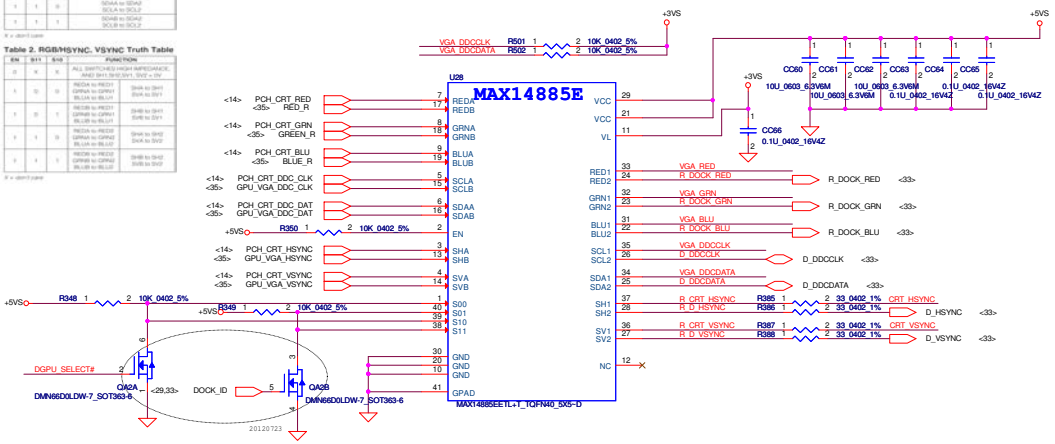
EN	SS1	SS0	FUNCTION
0	X	X	ALL SWITCHES HIGH IMPEDANCE
1	0	0	SDAA to SDA1 SCLA to SCL1
1	0	1	SDAB to SDA1 SCLB to SCL1
1	1	0	SDAA to SDA2 SCLA to SCL2
1	1	1	SDAB to SDA2 SCLB to SCL2

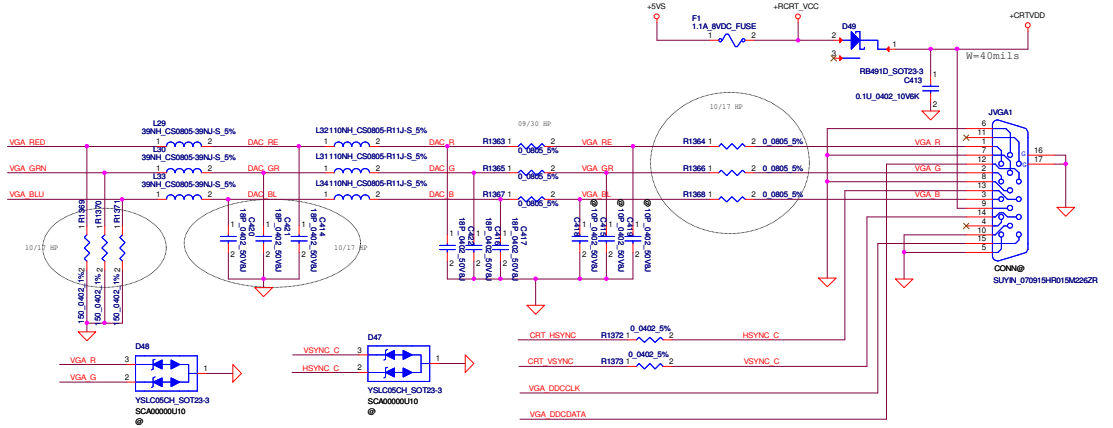
X = don't care

Table 2. RGB/HSYNC, VSYNC Truth Table

EN	SV1	SV0	FUNCTION	
0	X	X	ALL SWITCHES HIGH IMPEDANCE, AND SH1 SH2 SV1, SV2 = 0V	
1	0	0	RED4 to RED1 GRN4 to GRN1 BLU4 to BLU1	SH4 to SH1 SV4 to SV1
1	0	1	RED8 to RED1 GRN8 to GRN1 BLU8 to BLU1	SH8 to SH1 SV8 to SV1
1	1	0	RED4 to RED2 GRN4 to GRN2 BLU4 to BLU2	SH4 to SH2 SV4 to SV2
1	1	1	RED8 to RED2 GRN8 to GRN2 BLU8 to BLU2	SH8 to SH2 SV8 to SV2

X = don't care





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Title: Compal Electronics, Inc. — Switch/MUX

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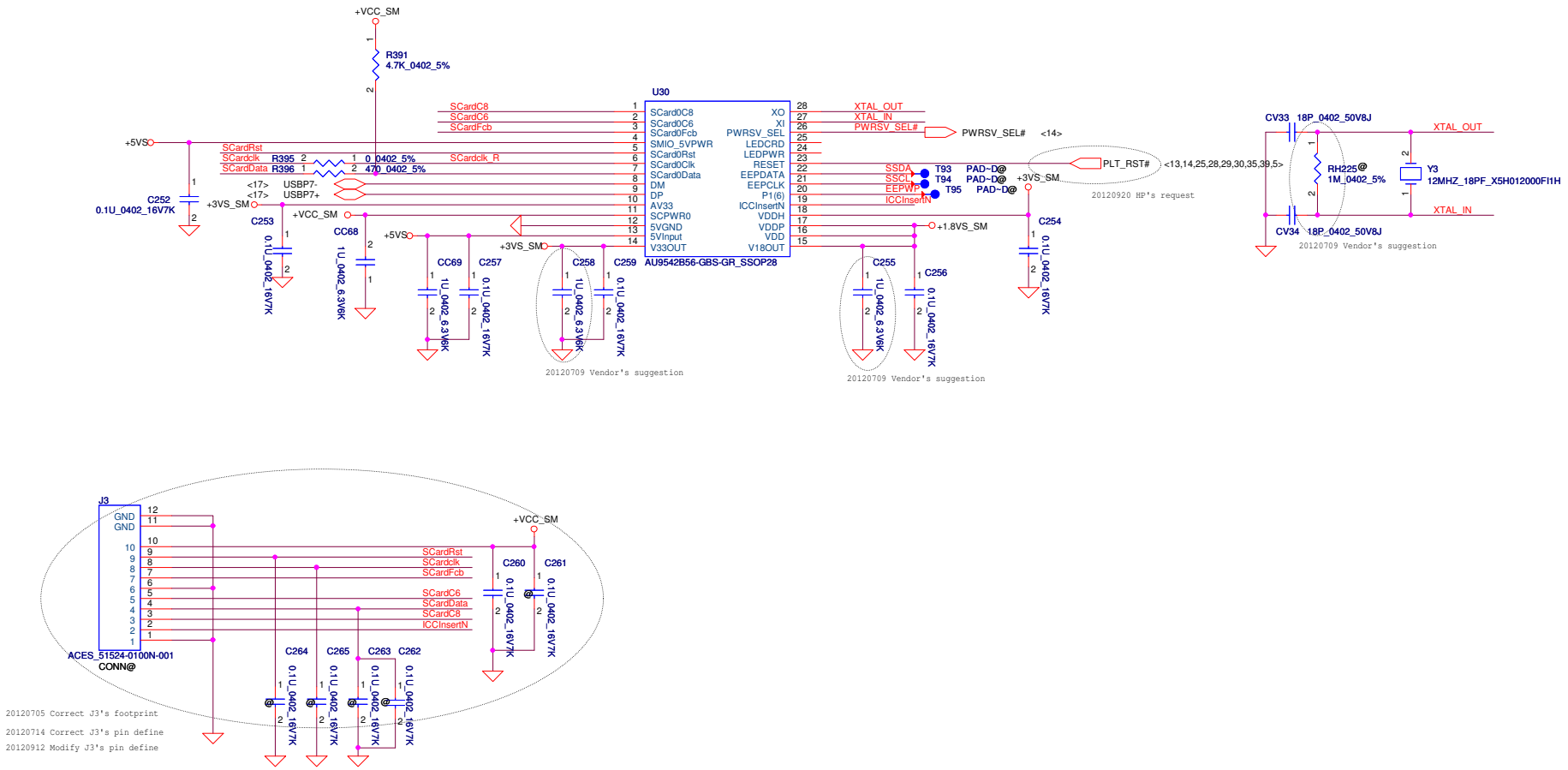
Document Number: LA-9371P — Rev: 0.2

Date: Friday, September 28, 2012 — Sheet 36 of 53



20120705 Correct J3's footprint

20120714 Correct J3's pin define

20120912 Modify J3's pin define

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				Size: Custom; Document Number: ; Rev: 0.2
				Date: Friday, September 28, 2012; Sheet 37 of 53

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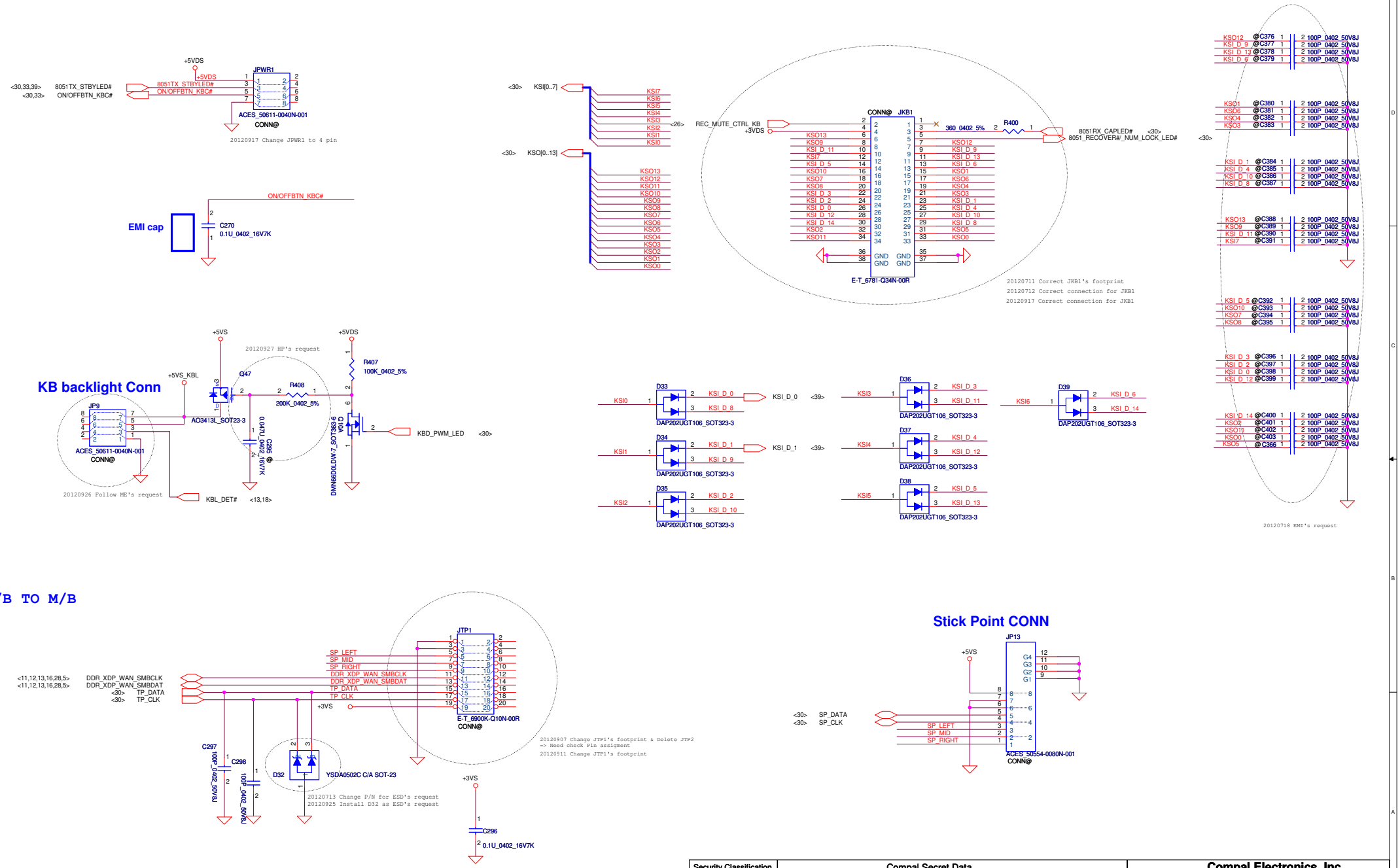

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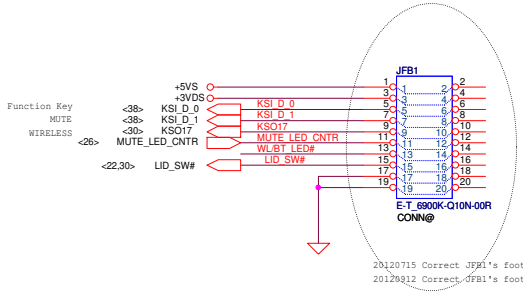
Compal Electronics, Inc.

Title: KB/TP/PWR CONN

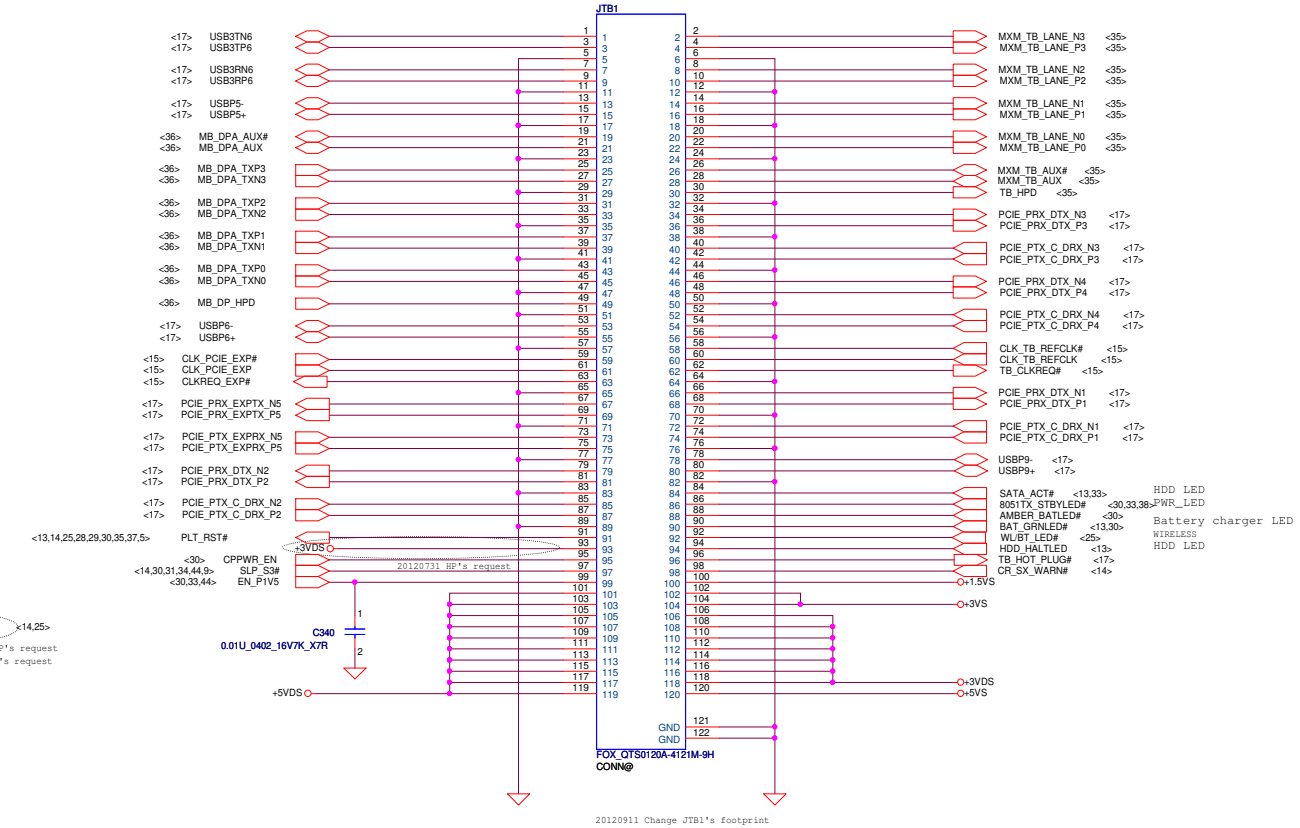
Size: Custom | Document Number | Rev: 0.2

Date: Friday, September 28, 2012 | Sheet 38 of 53

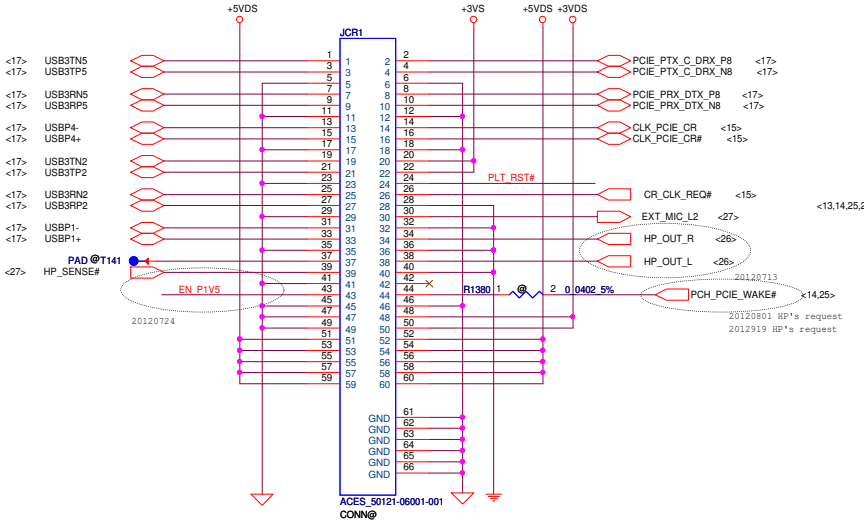
Function Board

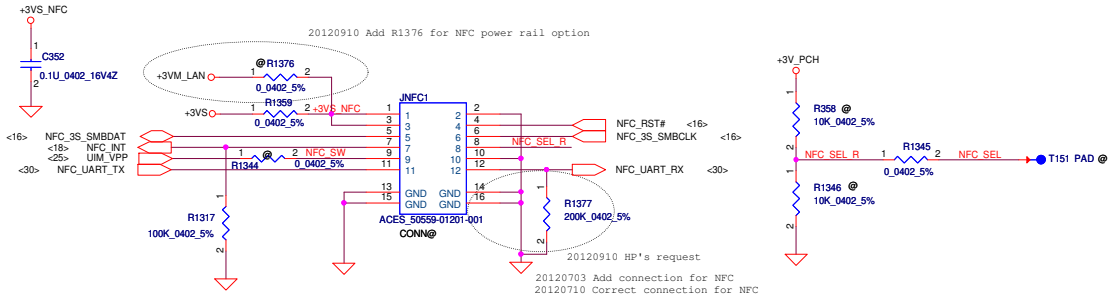


Thunderbolt



USB & Card Reader Board





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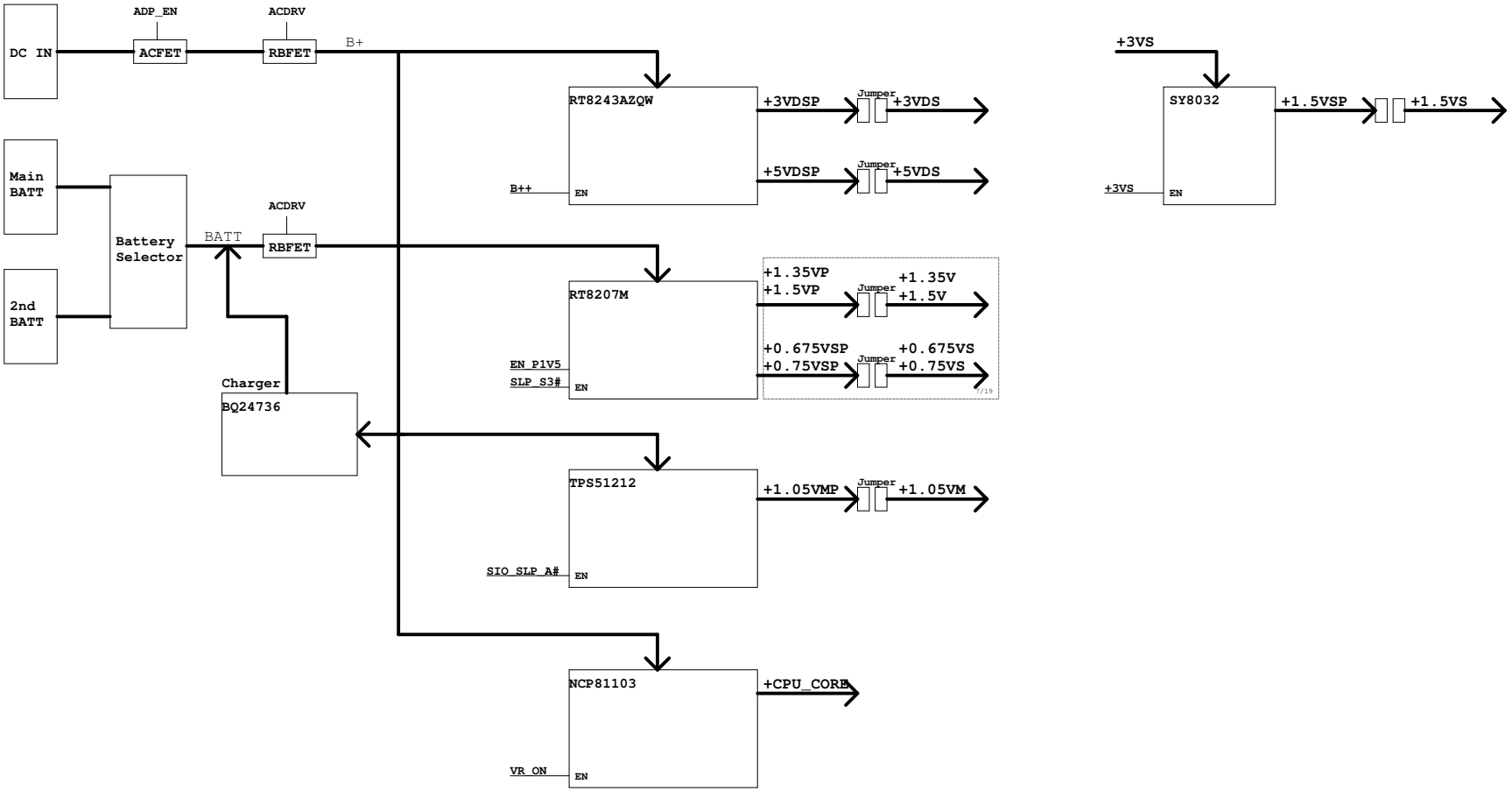
Compal Electronics, Inc.

Title: CONN

Size: | Document Number: LA-9371P | Rev: 0.2

Date: Friday, September 28, 2012 | Sheet 39 of 53


DC IN
ADP_EN
ACFET
ACDRV
RBFET
B+
Main BATT
2nd BATT
Battery Selector
BATT
ACDRV
RBFET
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RT8243AZQW
B++
EN
+3VDSP
Jumper
+3VDS
+5VDSP
Jumper
+5VDS
RT8207M
EN_P1V5
SLP_S3#
EN
+1.35VP
+1.5VP
Jumper
+1.35V
+1.5V
+0.675VSP
+0.75VSP
Jumper
+0.675VS
+0.75VS
TPS51212
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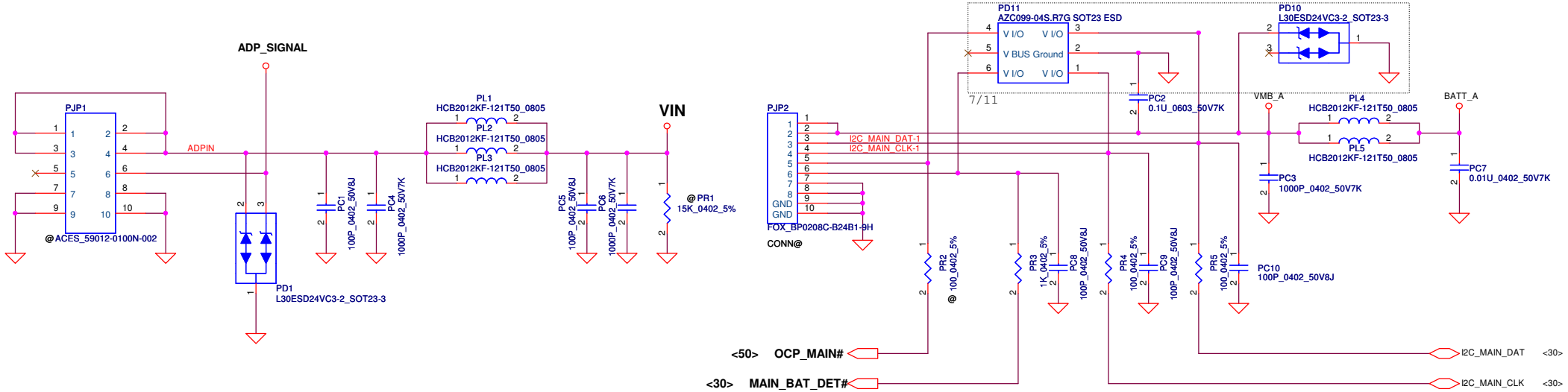
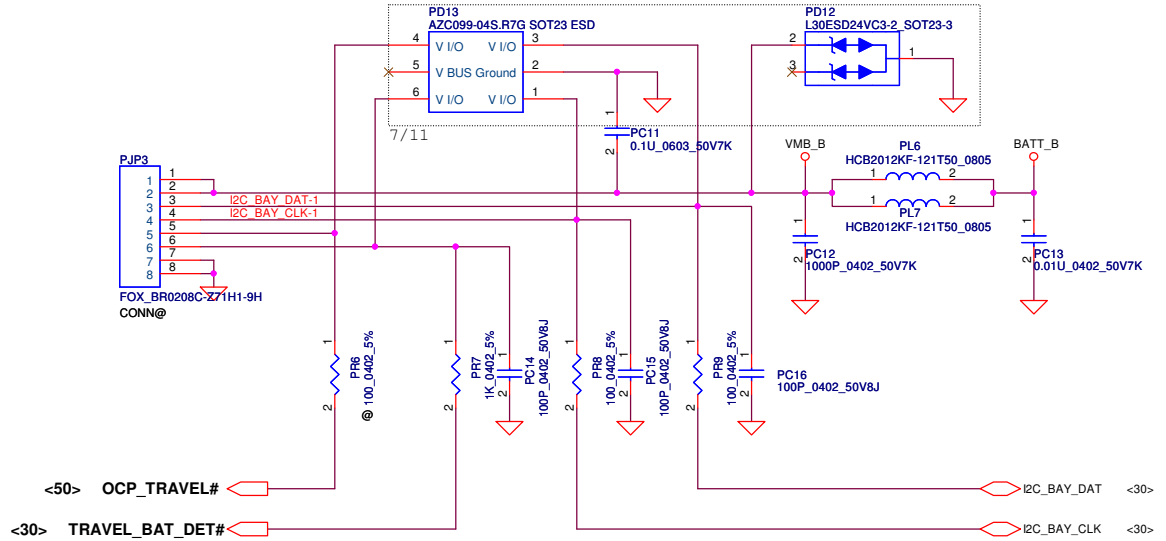
EN
+1.05VMP
Jumper
+1.05VM
NCP81103
VR_ON
EN
+CPU_CORE
+3VS
SY8032
+3VS
EN
+1.5VSP
+1.5VS





Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/04/03	Deciphered Date	2014/12/31	Title: *DC Conn/BATT Conn*
				Size: Document Number: 15W — Rev: 0.2
				Date: Friday, September 28, 2012 — Sheet 41 of 53

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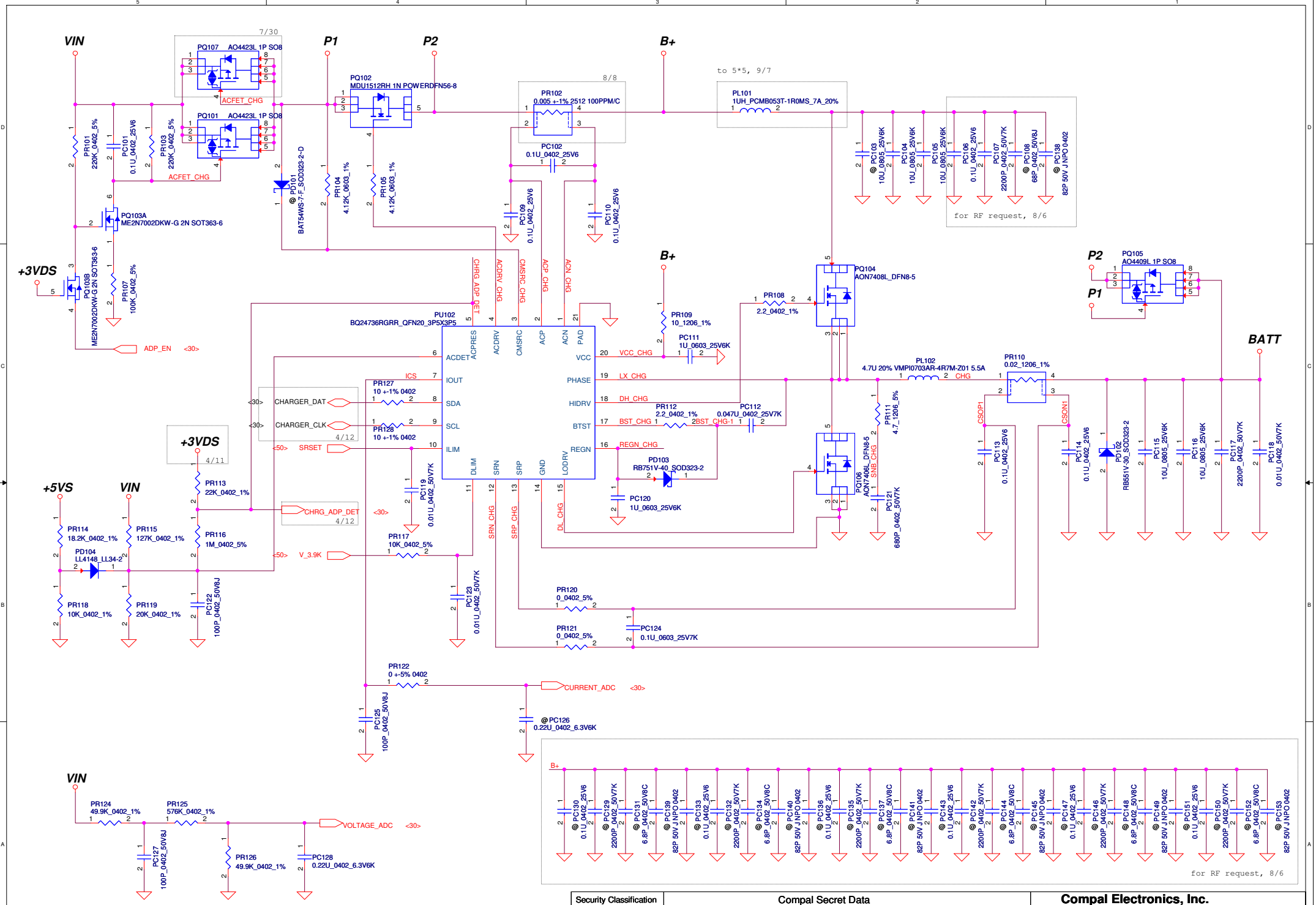

Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

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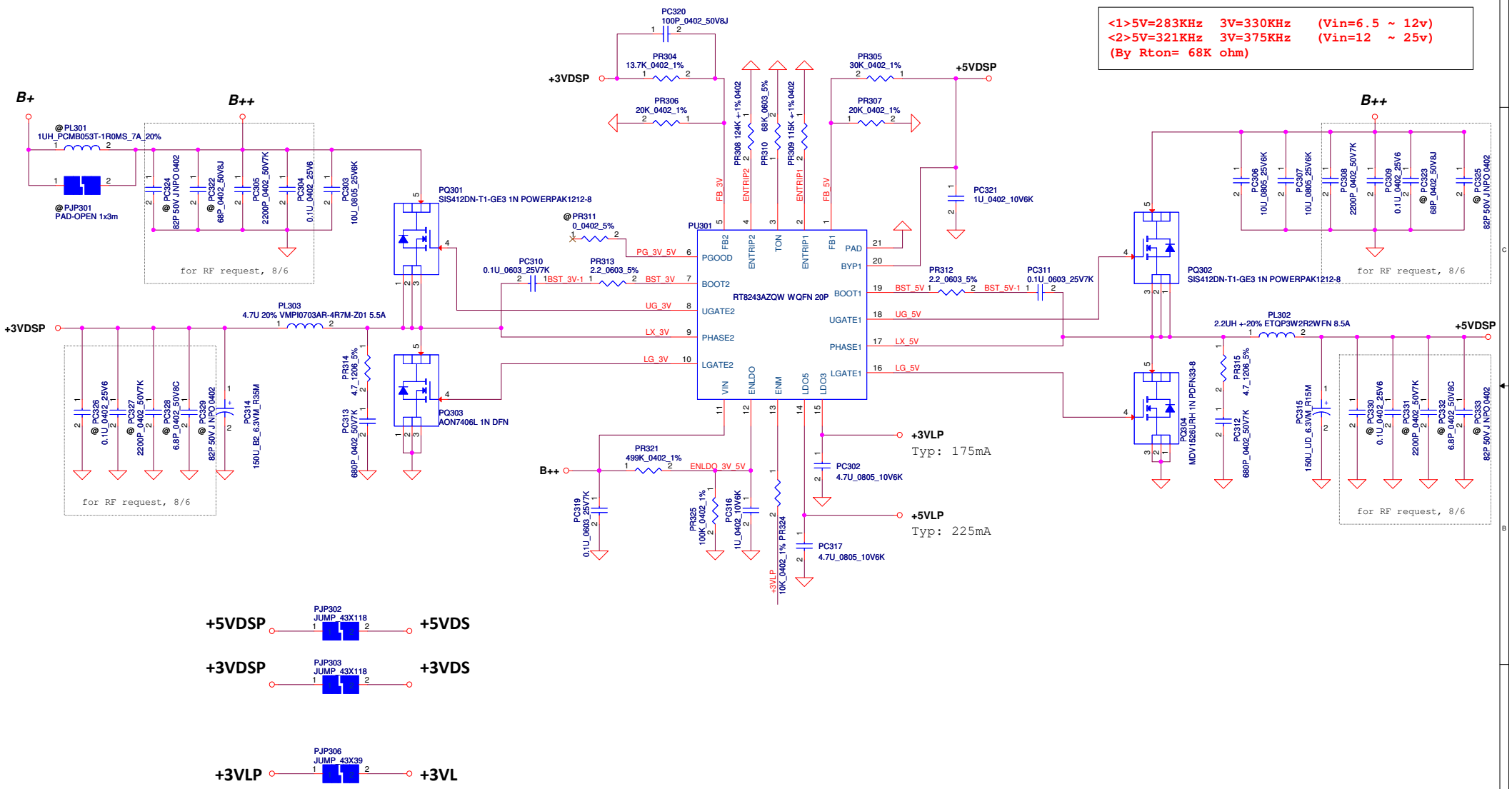
Compal Electronics, Inc.

Title: ***CHARGER***

Size: | Document Number: **15W** | Rev: 0.2

Date: Friday, September 28, 2012 | Sheet 42 of 53



Security Classification	Compal Secret Data		
Issued Date	2011/06/13	Deciphered Date	2012/06/13

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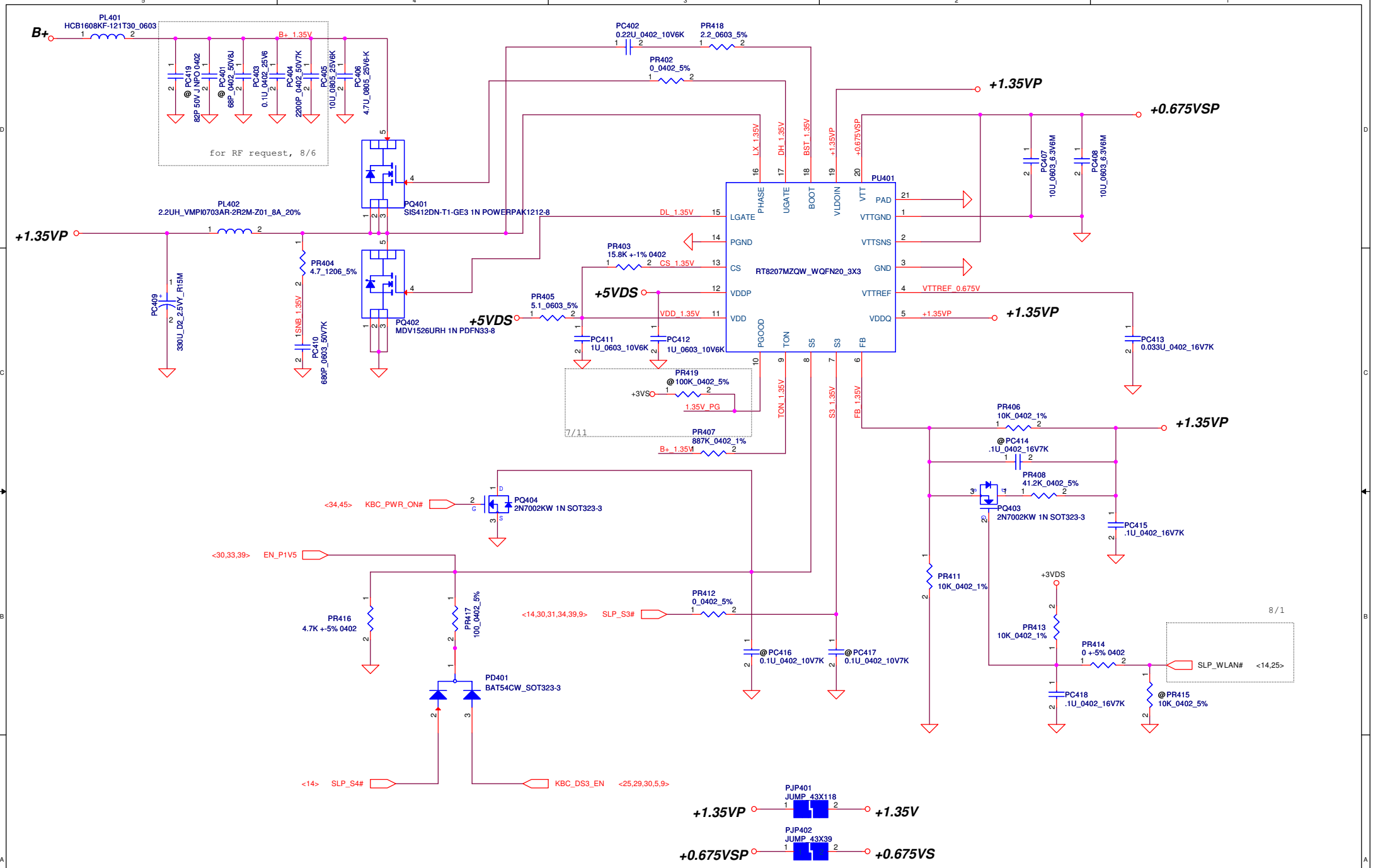
Compal Electronics, Inc.

Title: 3VDSP/5VDSP

Size: Custom | Document Number: 15W | Rev: 0.2

Date: Friday, September 28, 2012 | Sheet 43 of 53



Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

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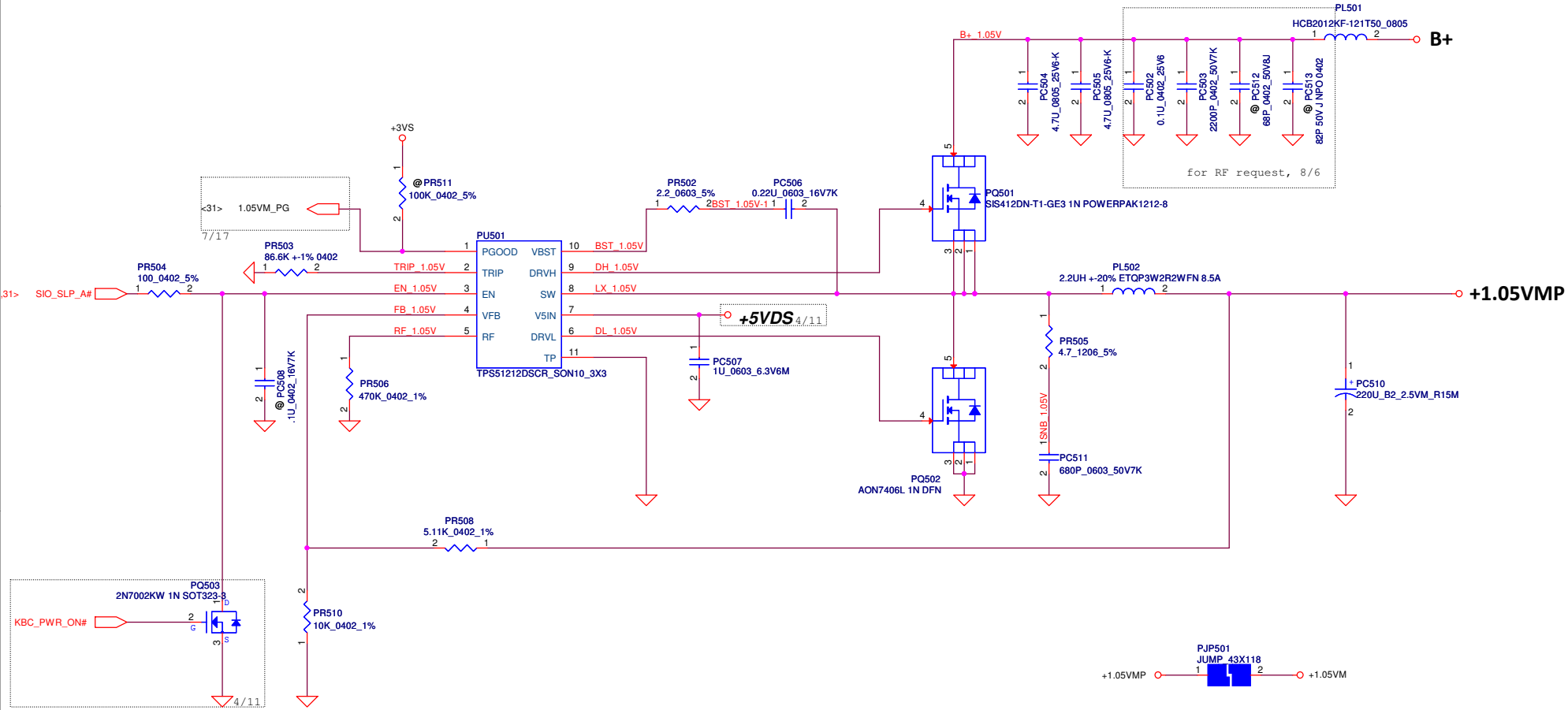
Compal Electronics, Inc.

Title: ***DDR Power***

Size: | Document Number: **15W** | Rev: 0.2

Date: Friday, September 28, 2012 | Sheet 44 of 53



Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

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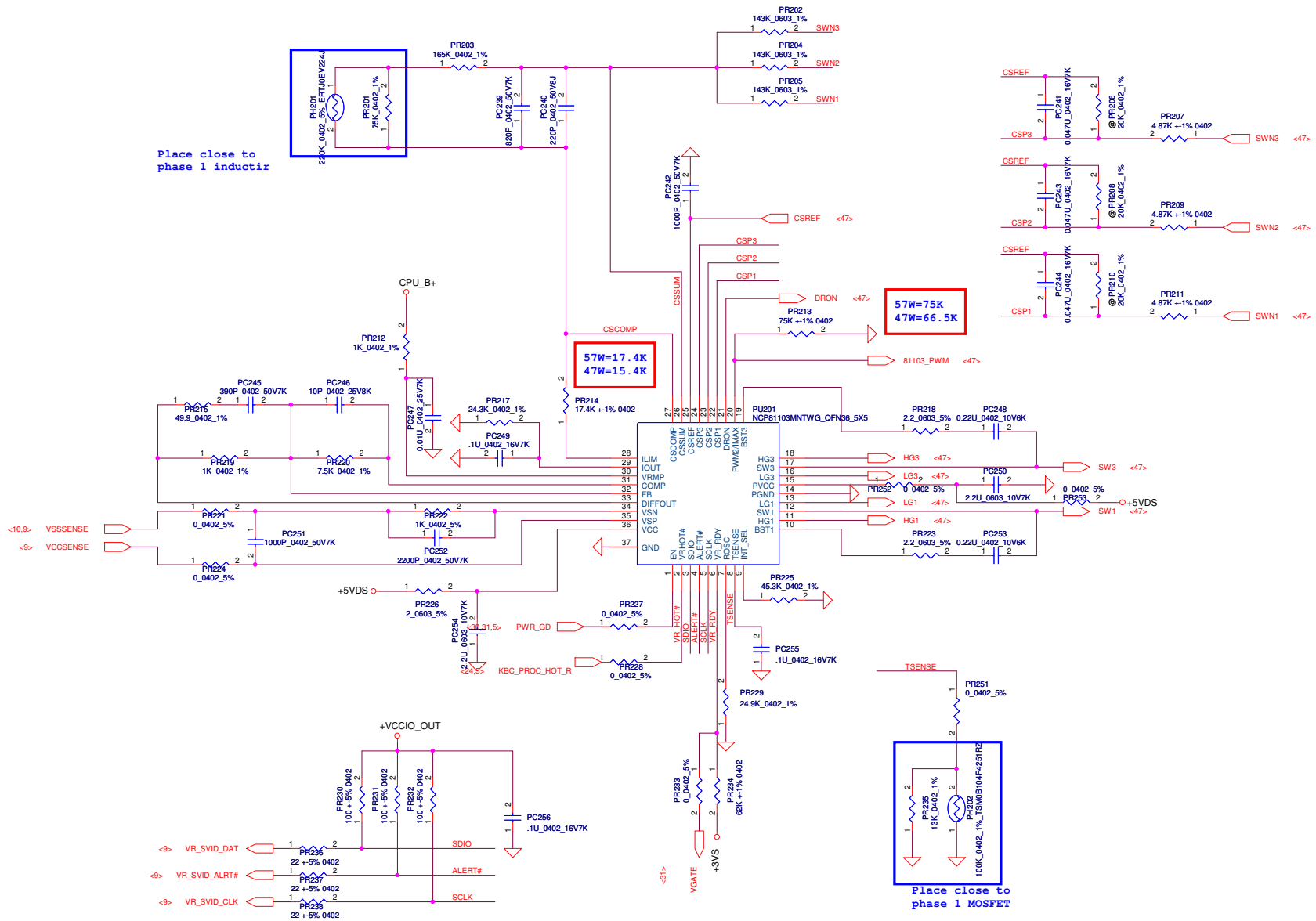
Compal Electronics, Inc.

Title: *1.05VMP*

Size: | Document Number: 15W | Rev: 0.2

Date: Friday, September 28, 2012 | Sheet 45 of 53



Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

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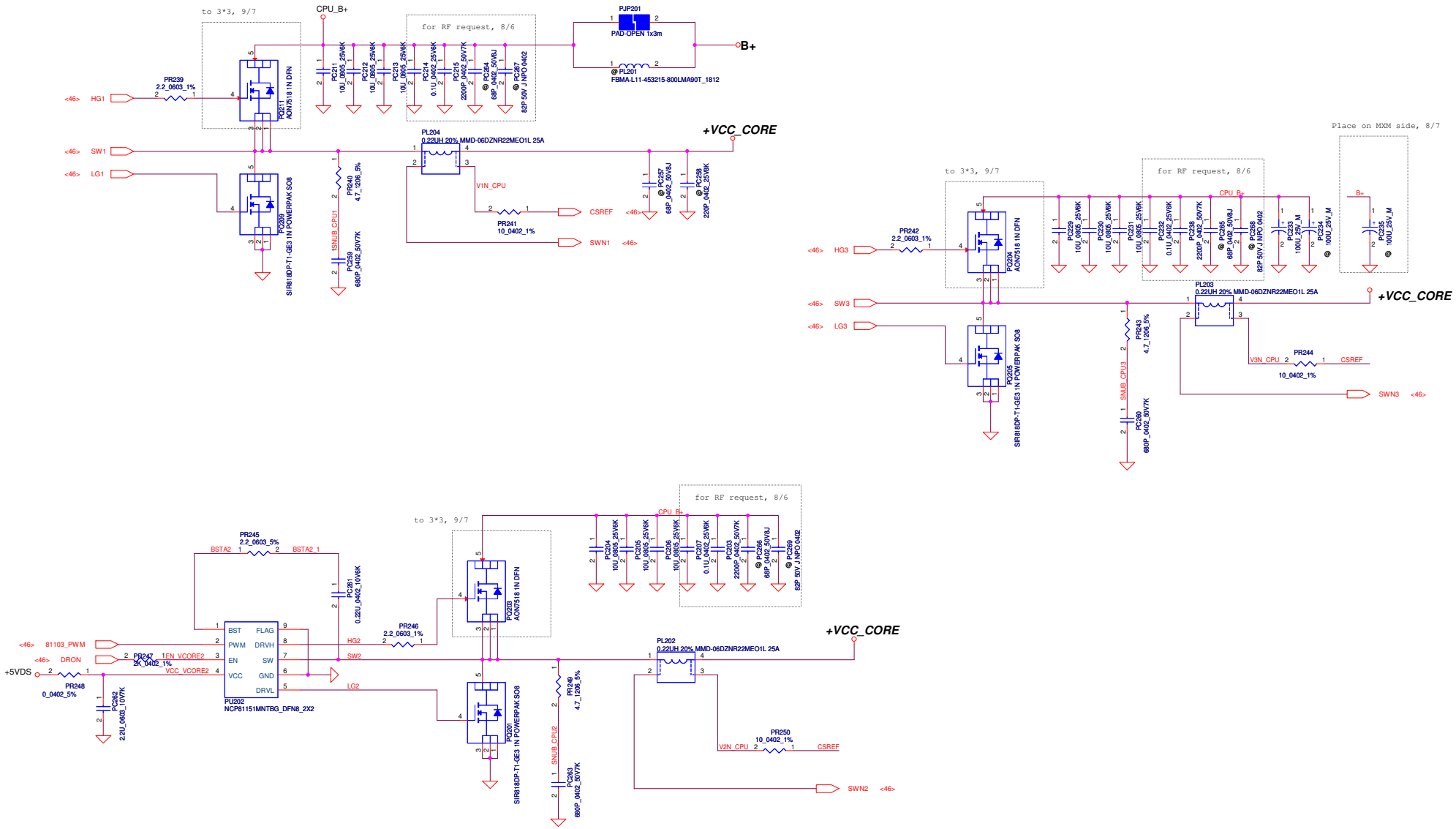
Compal Electronics, Inc.

Title: **PWR-+CPU_CORE**

Size: Custom | Document Number: **QFKAA** | Rev: 0.2

Date: Friday, September 28, 2012 | Sheet 46 of 53



Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

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Compal Electronics, Inc.

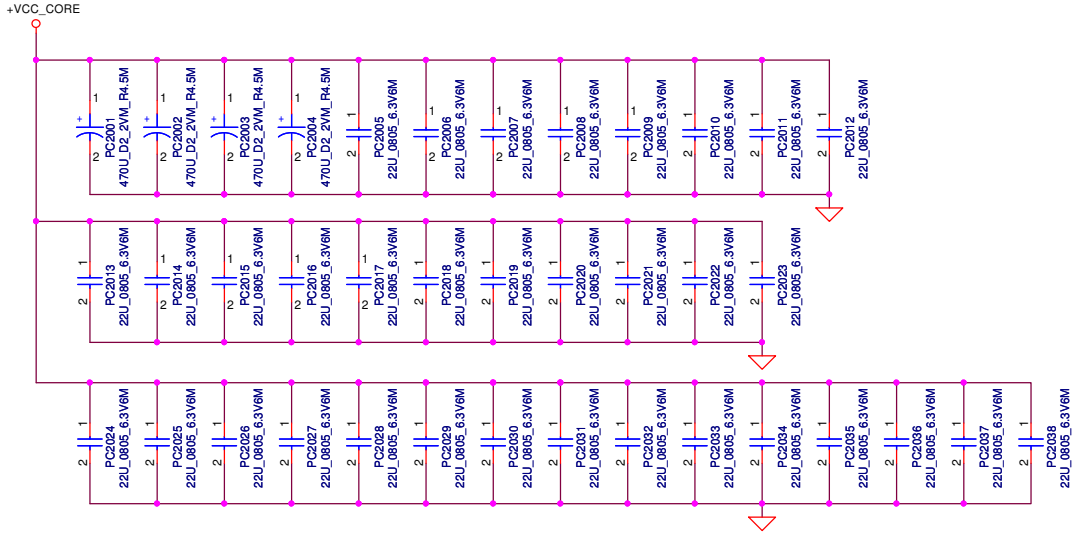
Title: **PWR-CPU_CORE**

Size: C | Document Number: QFKAA | Rev: 0.2

Date: Friday, September 28, 2012 | Sheet 47 of 53

+VCC_CORE

4 X 470u/4m
34X 22u/0805



Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

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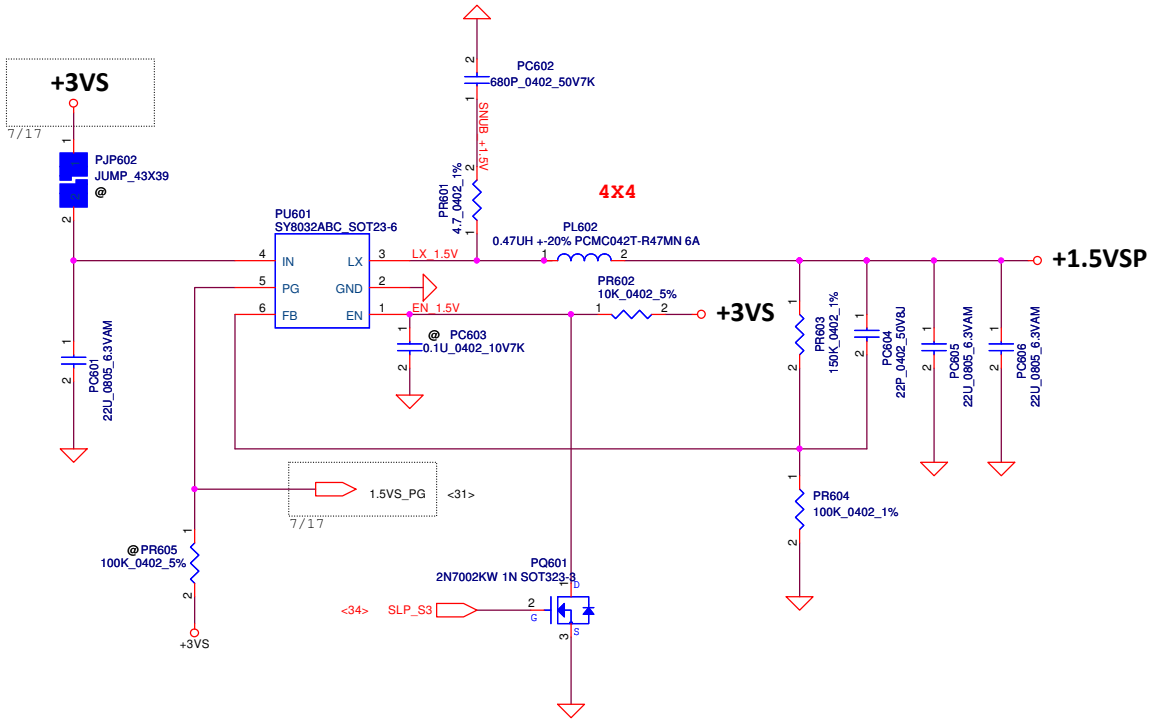
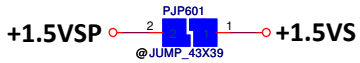
Compal Electronics, Inc.

Title: ***PROCESSOR DECOUPLING***

Size: | Document Number: **15W** | Rev: 0.2

Date: Friday, September 28, 2012 | Sheet 48 of 53





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Peak Current=0.66A

Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

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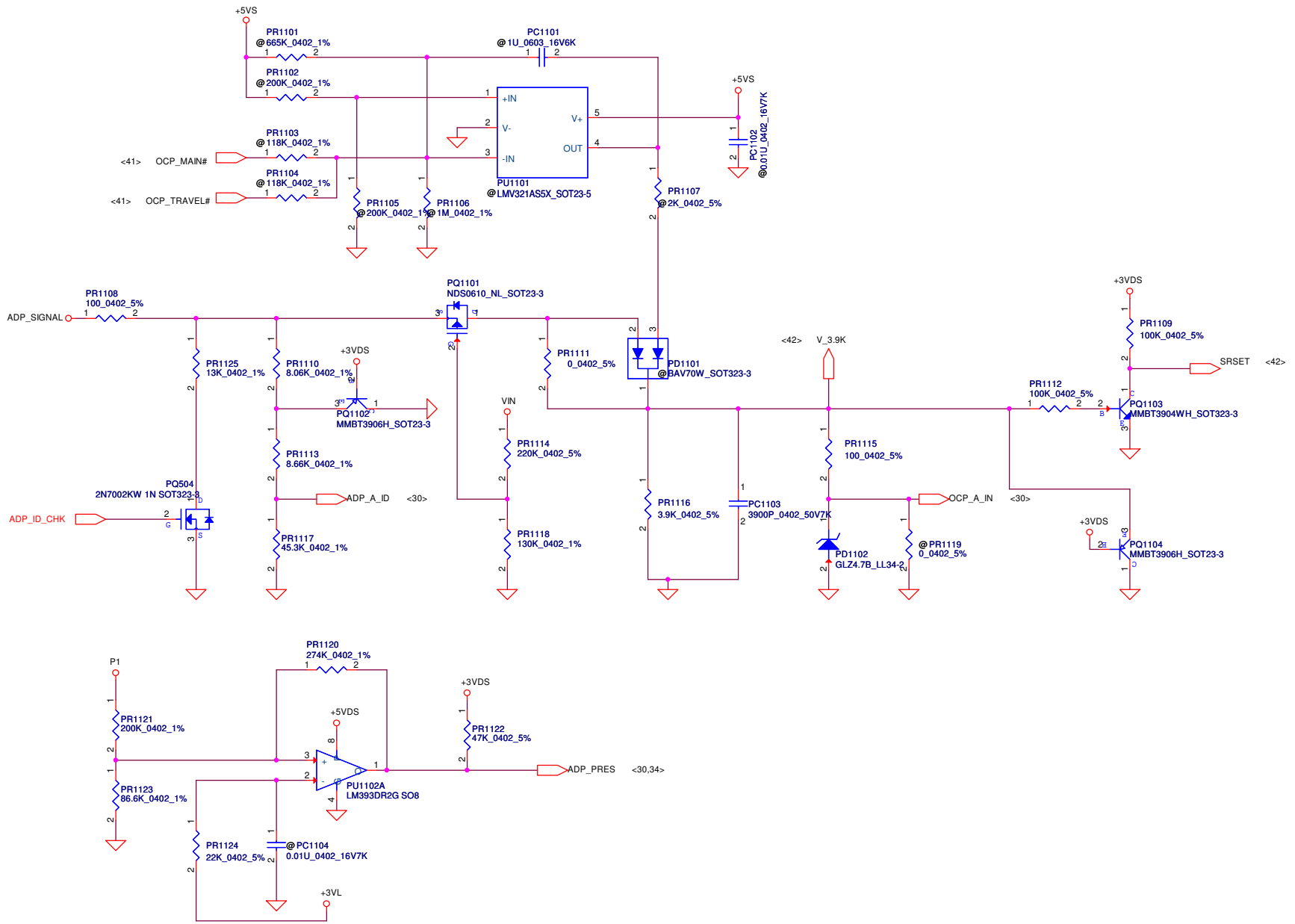
Compal Electronics, Inc.

Title: *1.5VSP*

Size: Document Number: **15W** Rev: 0.2

Date: Friday, September 28, 2012 Sheet 49 of 53



Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

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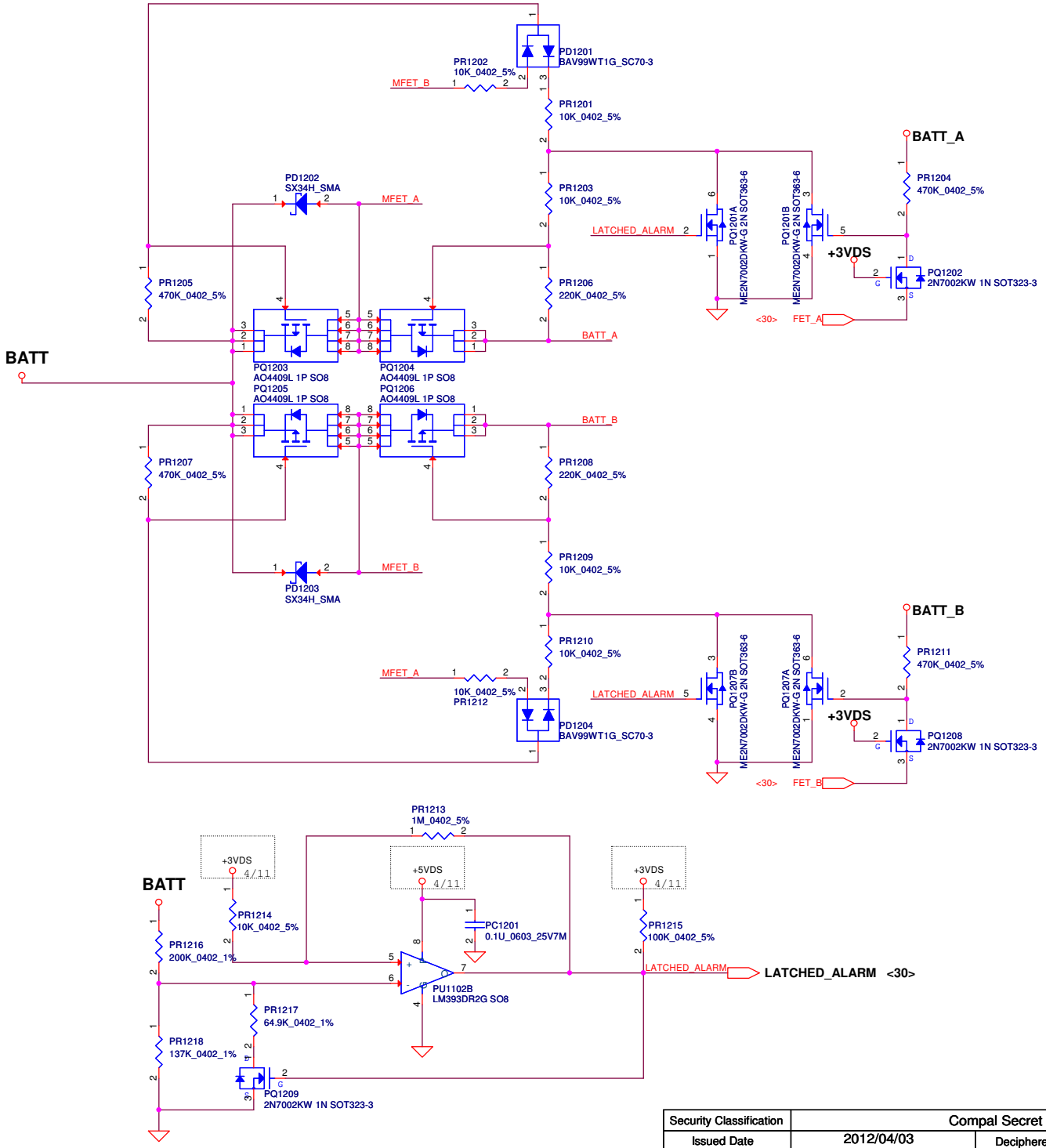
Compal Electronics, Inc.

Title: ***ADP_OCP***

Size: | Document Number: **15W** | Rev: 0.2

Date: Friday, September 28, 2012 | Sheet 50 of 53



Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

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Compal Electronics, Inc.

Title: ***Battery selector***

Size: | Document Number: **15W** | Rev: 0.2

Date: Friday, September 28, 2012 | Sheet 51 of 53

Version Change List (P. I. R. List) for HW Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	30	KBC	08/18	HP	The quad-mode does not require any GPIO from KBC	Delete R1348 & R1349 and Add R541 and R542	0.2
2	31	PWR OK	08/18	HP	Makes the power good circuit working.	Non-install R284	0.2
3	26	MXM	08/28	Compal	MXM Card can't be recognized in OS.	Change U37 to MC74VHC1G08DFT2G (Non-OD type)	0.2
4	36	Switch/MUX	09/07	HP	Move D-Sub connector on M/B	Add VGA filter circuit and connector	0.2
5	30	KBC	09/08	HP	SUSCLK is off during DS3 condition	Add Y4, C423, C424 ; Delete R258, R264	0.2
6	30	KBC	09/08	HP	Simplify the KBC solution for MEC1322	Delete R262,R266,R219,R216,R241,R242,R271,R253	0.2
7	25	NGFF	09/08	HP		Add PU resistor for WWAN_FULL_PWR/WWAN_RSVD2	0.2
8	39	NFC	09/10	HP	KBC detection of NFC module	Add 200K (R1377) PD resistor to NFC_UART_RX	0.2
9	39	NFC	09/10	HP	Power rail option for NFC module	Add +3VM_LAN (R1376) for NFC module	0.2
10	9	CPU	09/11	HP		Remove RC102 and RC103	0.2
11	20	PCH	09/11	HP	Connect PCH's pin AD12 to +3V_PCH directly	Remove RH226	0.2
12	5	CPU	09/11	HP	Connect CPU AT26 pin to CPU_PLTRST# directly	Remove RC66	0.2
13	5	CPU	09/11	HP	Connect CPU AL34 pin to H_CPUPWRGD directly	Remove RC30	0.2
14	9	CPU	09/11	HP	Connect SLP_S3# to QC5.5 direcly.	Remove RC93	0.2
15	33	DOCKING	09/11	HP	Connect EN_P1V5 to JDOCK1.140 directly.	Remove R351	0.2
16	33	DOCKING	09/11	HP	Connect ON/OFFBTN_KBC# to Docking directly.	Remove R336	0.2
17	15	PCH	09/11	HP	Simplify PCH solution for PCIE CLK Group	Remove RH107,RH103,RH114,RH116,RH122 RH124,RH126,RH127,RH129,RH130	0.2
18	14	PCH	09/11	HP	Reassignement GPIO for "BT_OFF"	Change it from GPIO72 to GPIO61	0.2
19	30	KBC	09/11	HP	Reserve for SUSACK# signal	Uninstall R436 and add R1378	0.2
20	18	PCH	09/11	HP	Reassigned BRD_ID4 to GPIO40 for CP support and update table for DB1-R	Connect RH180.1 to +3VS & RPH1.8 to GND	0.2
21	30	KBC	09/12	HP	Simplify the KBC solution for MEC1322	Delete R249,R251,R256,R277	0.2
22	36	Switch/MUX	09/12	HP	eDP trace length over Intel's specification	Change solution to PS8321	0.2

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Issued Date	2012/04/03	Deciphered Date 2014/12/31	Title: HW Changed-List History-1
Size	Document Number: LA-9371P		Rev 0.2
Date: Friday, September 28, 2012	Sheet 52 of 53		

Version Change List (P. I. R. List) for HW Circuit

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
23	29	LAN	09/12	HP	Avoid IEEE failure with trace stub lines	Add Lan switch solution PI3L500-AZFEX (U43)	0.2
24	39	I/O CONN	09/12	HP	Move Hall sensor IC on Function board	Add +3VDS & LID_SW# pin to JFB1	0.2
25	22	eDP	09/13	Compal	Avoid LVDS Burn out Risk	Rearrange pin assignment of JEDP1	0.2
26	31	POK CKT	09/13	HP	Modify Power OK circuit	Delete UH7, RH235 ; Add R1379	0.2
27	39	I/O CONN	09/19	HP	Prevent Card Reader can't be recognized issue	Add R1380 for PCH_PCIE_WAKE#	0.2
28	13	PCH	09/19	HP	Disable the unlock of ME descriptor	Change QH11 to P-MOSFET	0.2
29	37	Smart Card	09/20	HP	RC delay is NOT good as reset	Delete CC67,R393, then connect U30.23 to PLT_RST#.	0.2
30	26	CODEC	09/20	HP		Uninstall RA13 and CA20	0.2
31	14	PCH	09/20	HP	KBC appears drives high during S3, so the change to aviod the leakage without losing functionality.	Change RH74 from 10K to 100K Ohm	0.2
32	31	PWR OK	09/23	HP	Modify net name for easy read	Modify VR_ON to PWR_GD and PWR_GOOD_3 to VGATE	0.2
33	5	XDP	09/25	HP		Connect PM_PWROK to JXDP1.47 via 0 Ohm (RC107)	0.2
34	30	KBC	09/25	HP	Resolve ME LAN failures	Delete R537, Q73, D21	0.2
35	35	MXM	09/27	HP	There is yellow bang in device manager	Add pull high resistor (R1382,R1383 & R1384) to +3VS	0.2
36	38	KB Backlight	09/27	HP		Change R408 to 200K Ohm, and uninstall C295	0.2

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/04/03	Deciphered Date 2014/12/31	Title HW Changed-List History-1
			Size Document Number LA-9371P Rev 0.2
			Date: Friday, September 28, 2012 Sheet 53 of 53

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