Compal Confidential

VBL30/31

LA-9351P REV0.1 Schematic

Intel Ivy Bridge/Panther Point

AMD Seymour XT

2012-05-08 Rev 0.1

Security Classification	Compal Secret Data		
Issued Date	2012/06/01	Deciphered Date	2013/05/12

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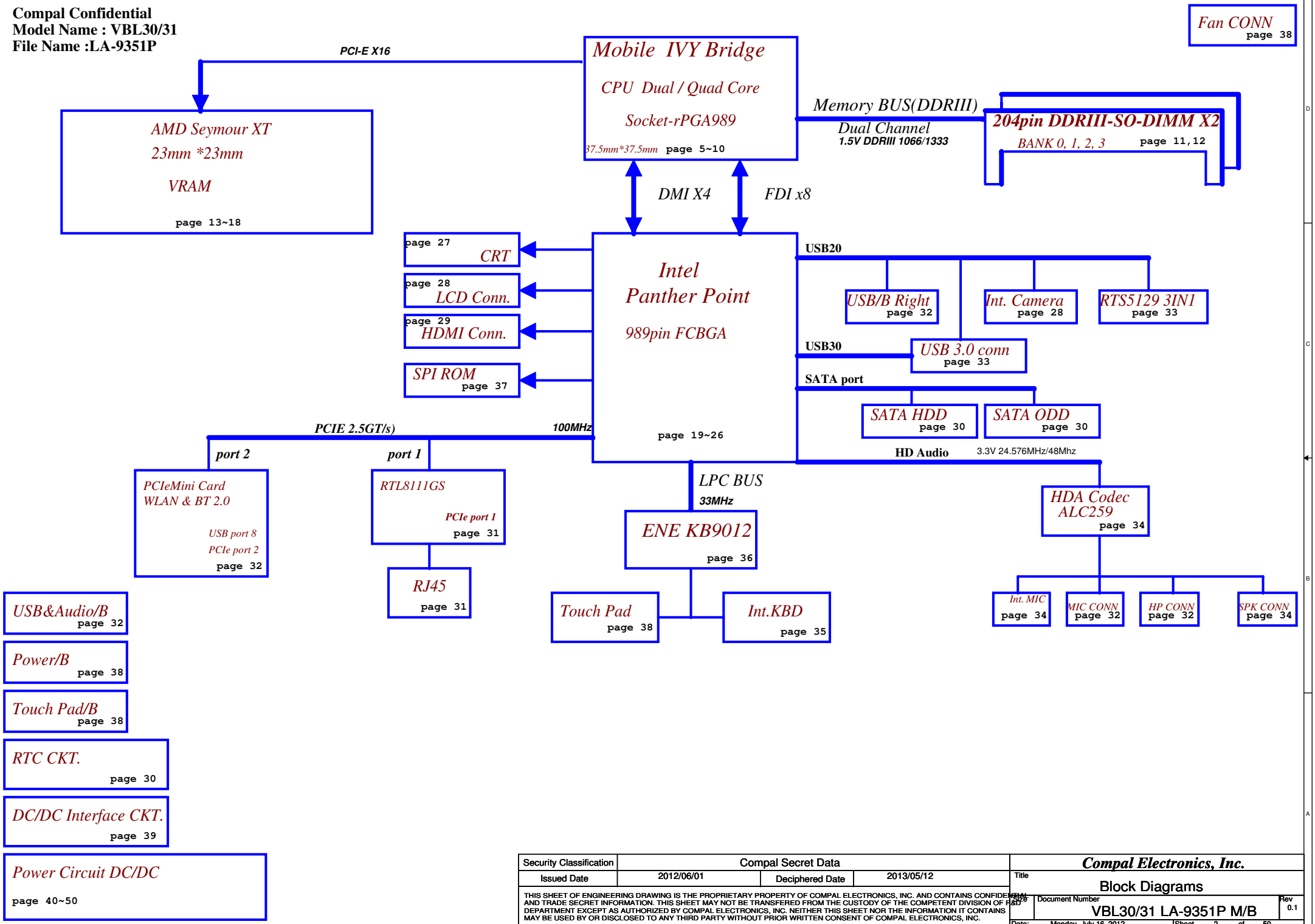
Title: Cover Page

Size: D | Document Number: VBL30/31 LA-9351P M/B | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 1 of 50

Compal Confidential
Model Name : VBL30/31
File Name :LA-9351P



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Title: Block Diagrams

Document Number: VBL30/31 LA-9351P M/B

Rev: 0.1

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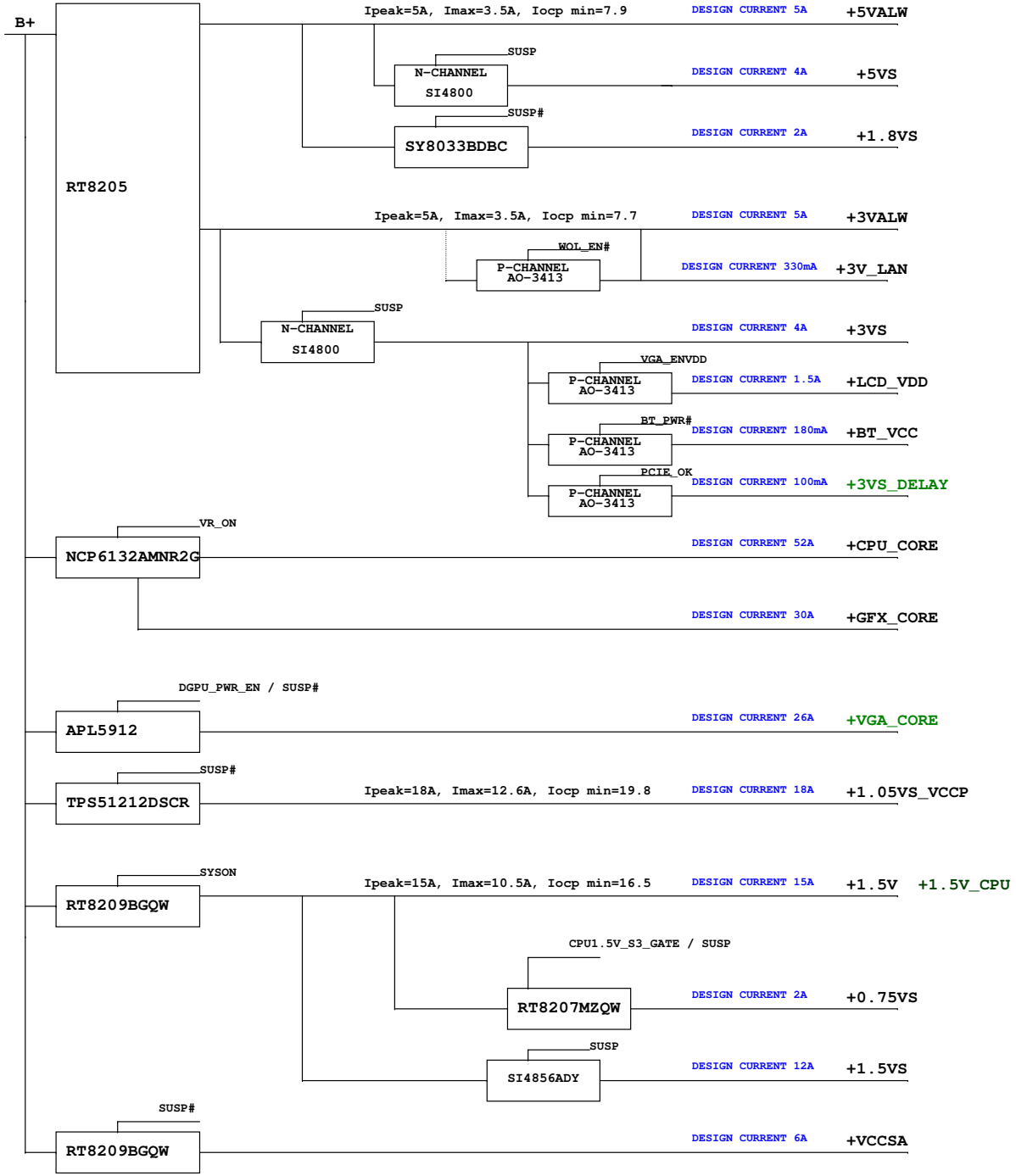

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Title: Power Map

Size | Document Number: VBL30/31 LA-9351P M/B | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 3 of 50

Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V +1.5V_IO	+5VS +3VS +1.5VS +1.05VS_VTT +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

@	Reserve
CONN@	ME CONNECTOR
KB9012@	ENE EC
Nuvton@	Nvuton EC
NOW8@	not Support Win8
WIN8@	Support Win8
UMA@	UMA Sku
PX@	PX Sku

EC SM Bus1 address

Power	Device	Address
+3VALW	Smart Battery	0001 011x b

EC SM Bus2 address

Power	Device	Address
+3VS	VGA Internal thermal sensor	1001 111Xb (0x9E)

PCH SM Bus address

Power	Device	Address
+3VS	DDR DIMMA	1001 000x b
+3VS	DDR DIMMB	1001 010x b

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

PCH X76 and PCBA table

		config
X76	ZZZ X76@ HYN 1G	ZZZ @ HYN 1G; R359 @ 10K_0402_5%; R361 @ 10K_0402_5%; R462 @ 10K_0402_5%
	ZZZ X76@ SAM 1G	ZZZ @ SAM 1G; R360 @ 10K_0402_5%; R361 @ 10K_0402_5%; R461 @ 10K_0402_5%
PCH	UH1 BD82HM70 QPXH C1 BGA 989P PCH@	
PCB	ZZZ DAZ@ PCB LA-6732P REV10; ZZZ DA8@ PCB LA-9351P REV01; ZZZ DA4@ PCB LS-6732P REV10; ZZZ DA2@ PCB LS-6731P REV10	

(@/CONN@/DA2@/DA4@/DA8@/DAZ@/KB9012@/NOW8@/Nuvton@/PCH@/PX@/Rev01@/Rev02@/Rev03@/Rev04@/Rev10@/UMA@/WIN8@/X76@)

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Title: Notes List

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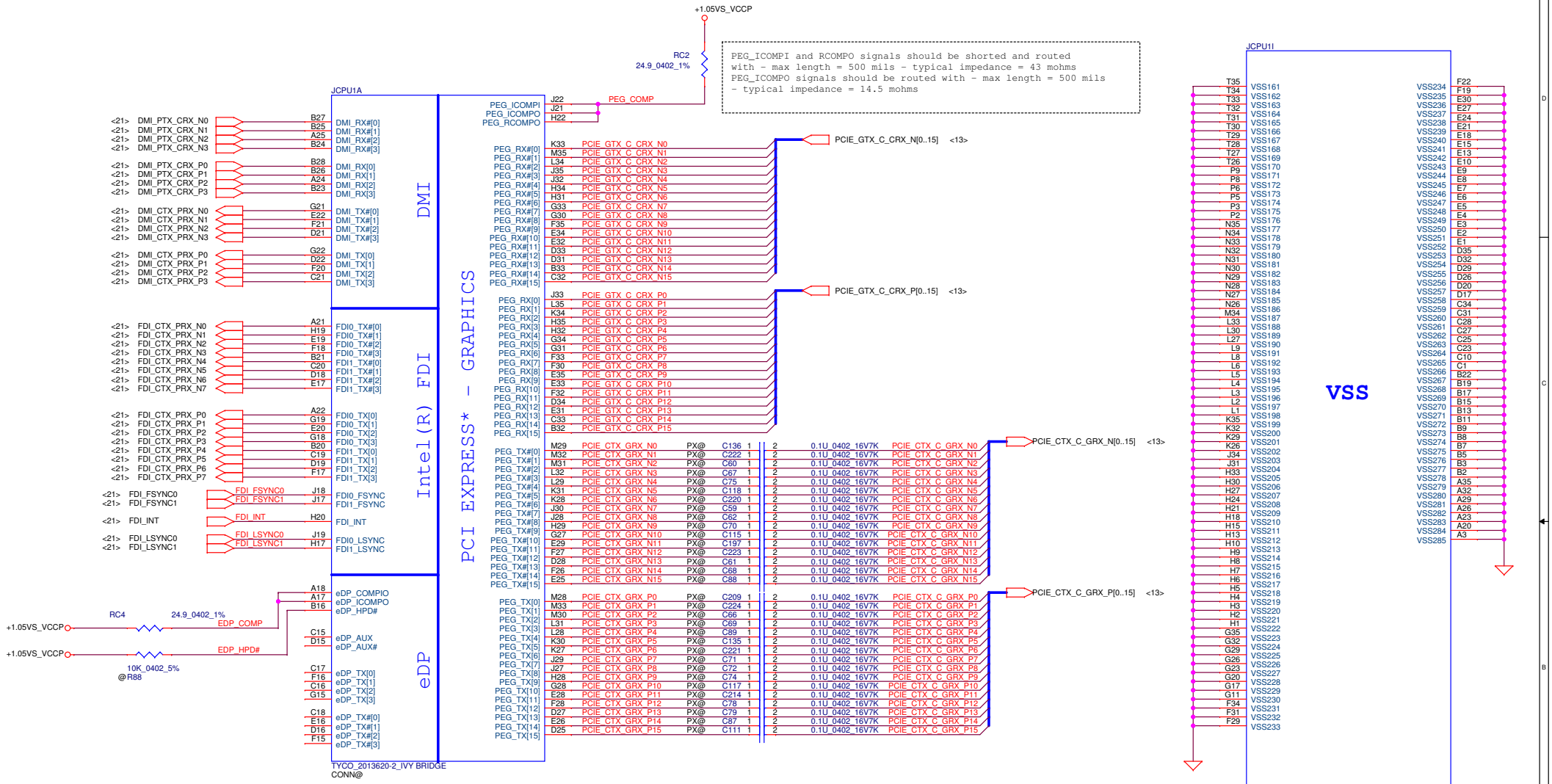
Date: Monday, July 16, 2012 | Sheet 4 of 50



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Compal Electronics, Inc.

Title: **PROCESSOR(1/6) DMI,FDI,PEG**

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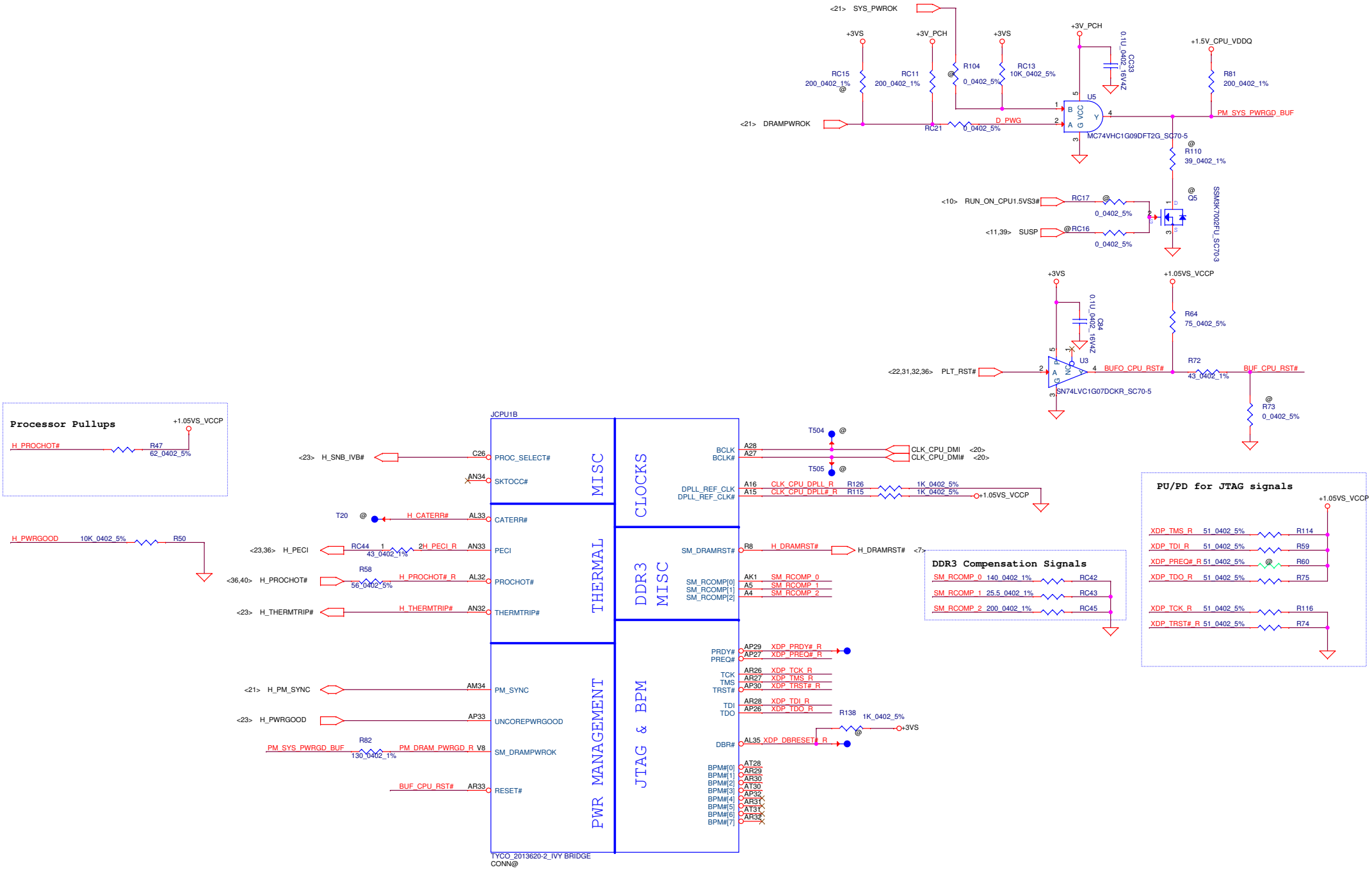
Date: Monday, July 16, 2012 | Sheet 5 of 50



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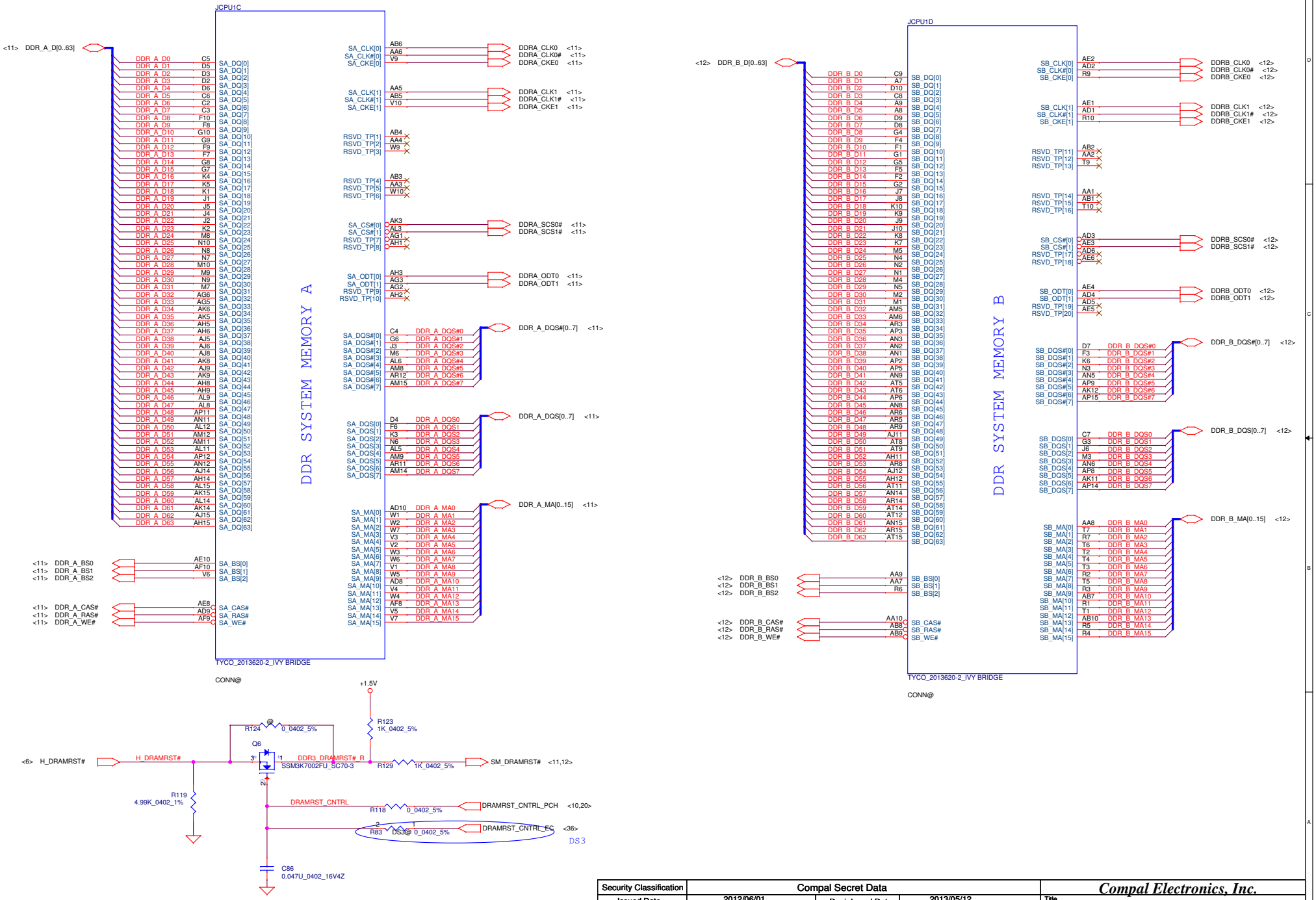
Compal Electronics, Inc.

Title: **PROCESSOR(2/6) PM,XDP,CLK**

Size: Custom | Document Number: **VBL30/31 LA-9351P M/B** | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 6 of 50



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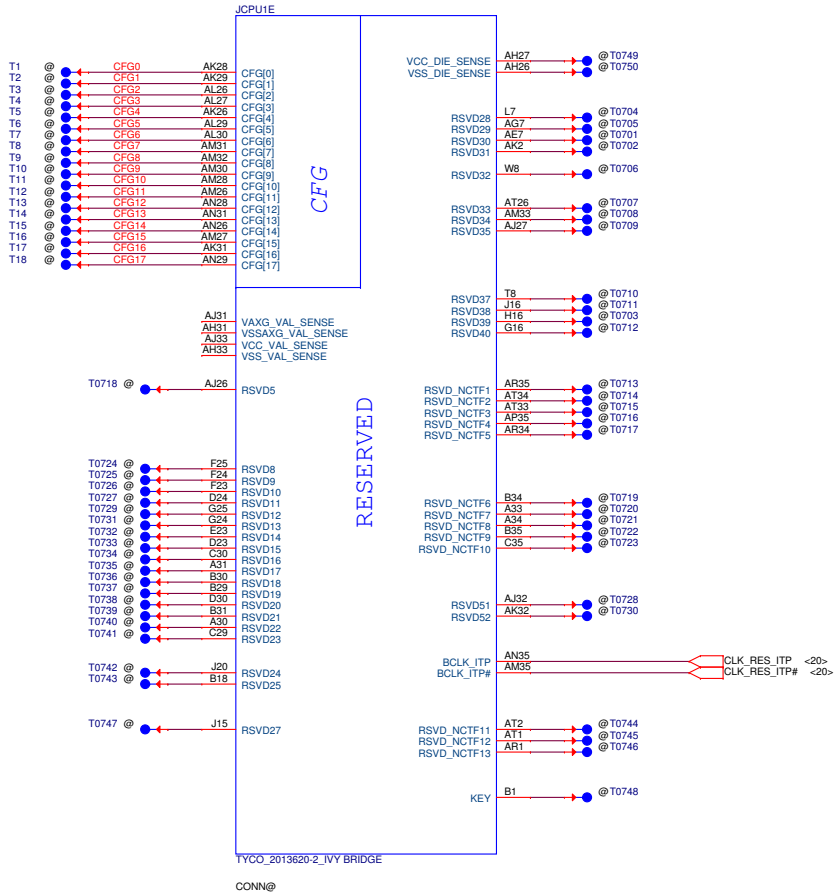
Compal Electronics, Inc.

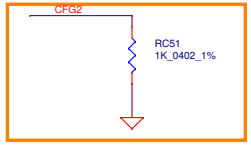
Title: **PROCESSOR(3/6) DDRIII**

Size: Custom | Document Number: **VBL30/31 LA-9351P M/B** | Rev: 0.1

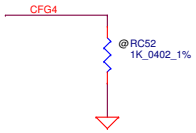
Date: Monday, July 16, 2012 | Sheet 7 of 50



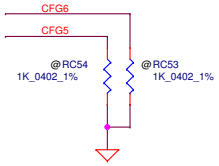
CFG Straps for Processor



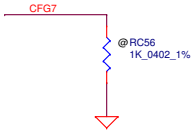
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following RESETB de assertion 0: PEG Wait for BIOS for training

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Compal Electronics, Inc.

Title: PROCESSOR(4/6) RSVD,CFG

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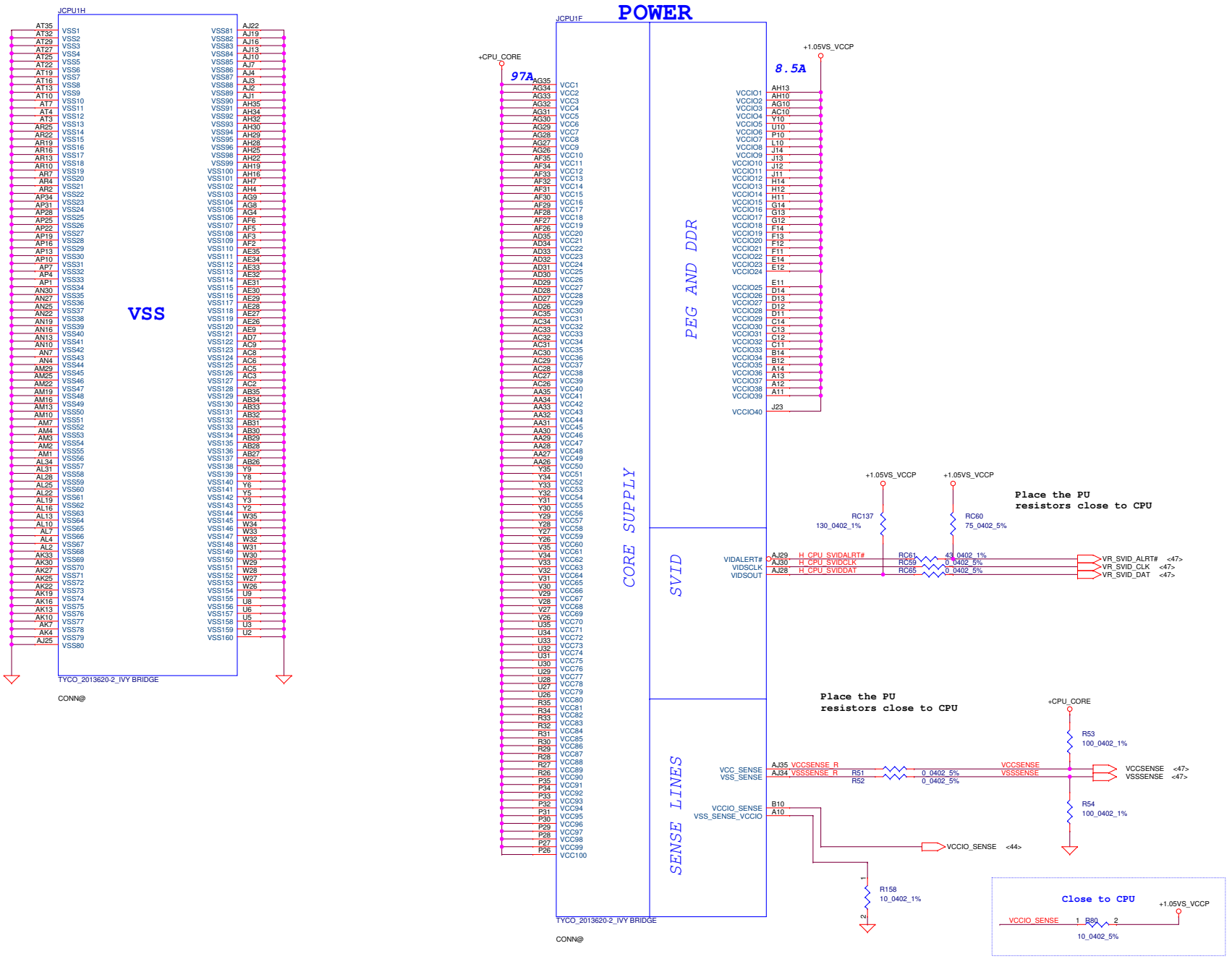
Date: Monday, July 16, 2012 | Sheet 8 of 50



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Compal Electronics, Inc.

Title: PROCESSOR(5/6) PWR,BYPASS

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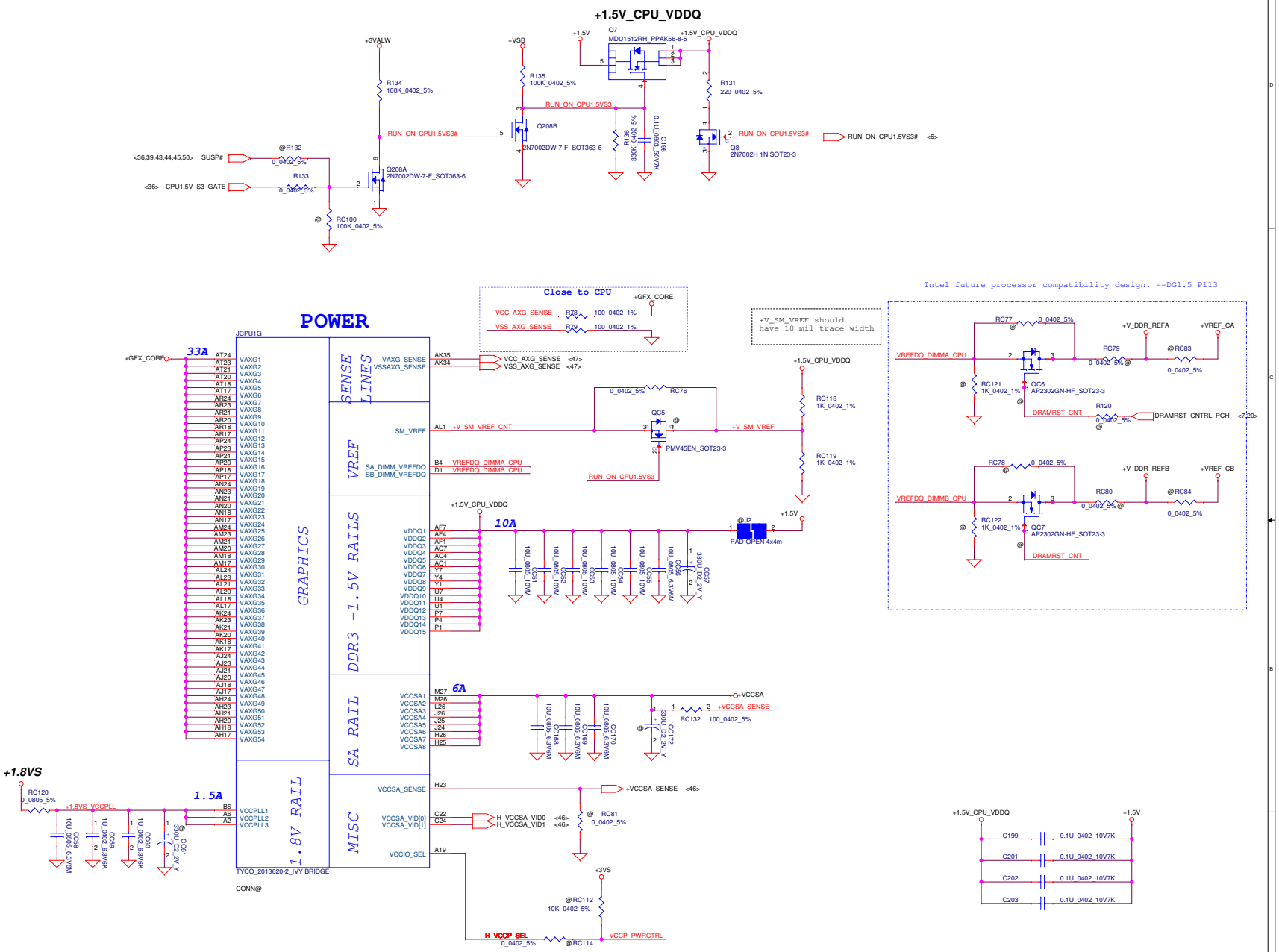
Date: Monday, July 16, 2012 | Sheet 9 of 50



IVY Bridge drives VCCIO_SEL low
VCCP_PWRCTRL:0

Sandy Bridge is NC for A19
VCCP_PWRCTRL:1

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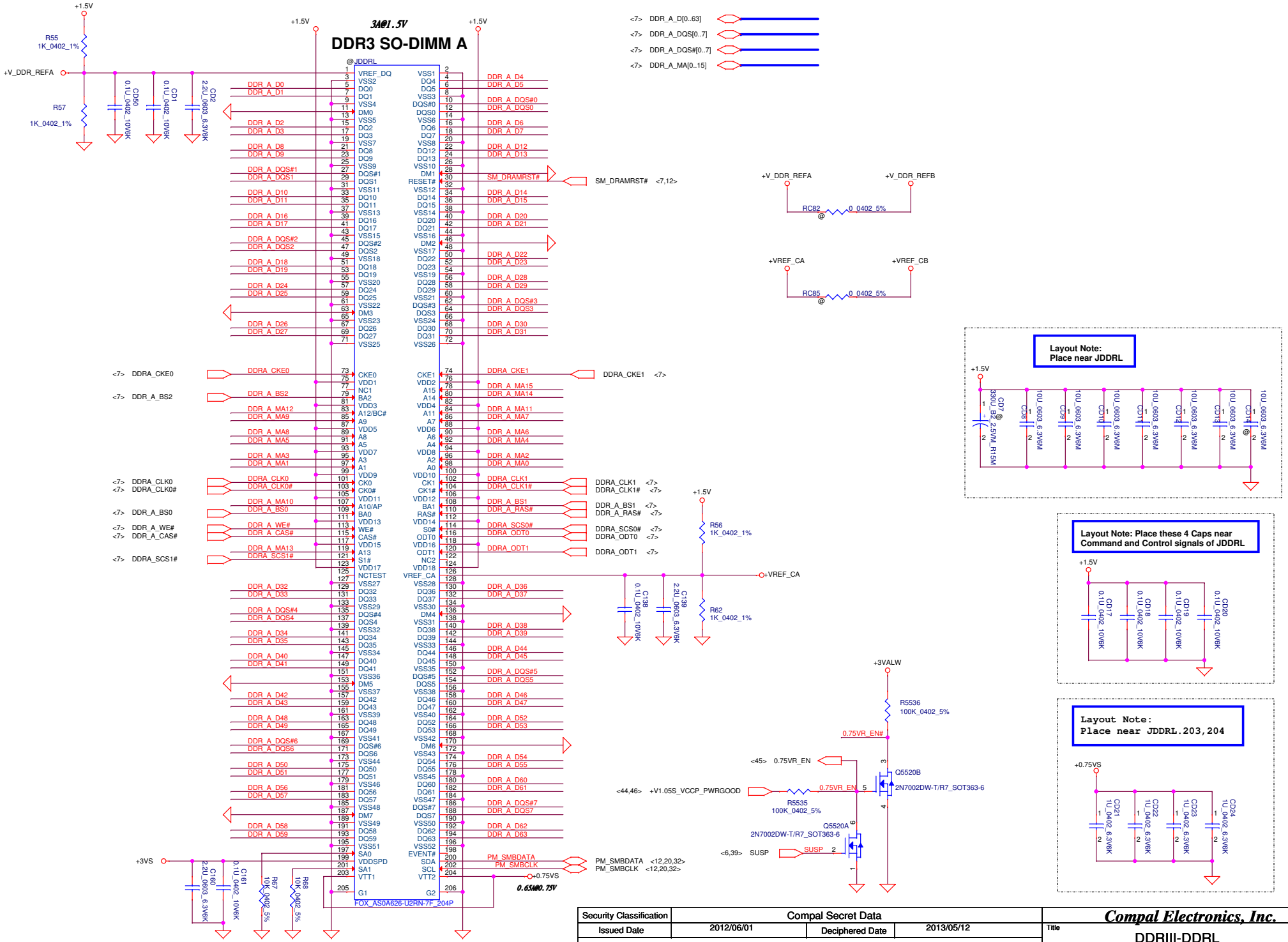
Compal Electronics, Inc.

Title: *PROCESSOR(6/6) PWR,VSS*

Size: Custom | Document Number: *VBL30/31 LA-9351P M/B* | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 10 of 50



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				Date: Monday, July 16, 2012; Sheet 11 of 50

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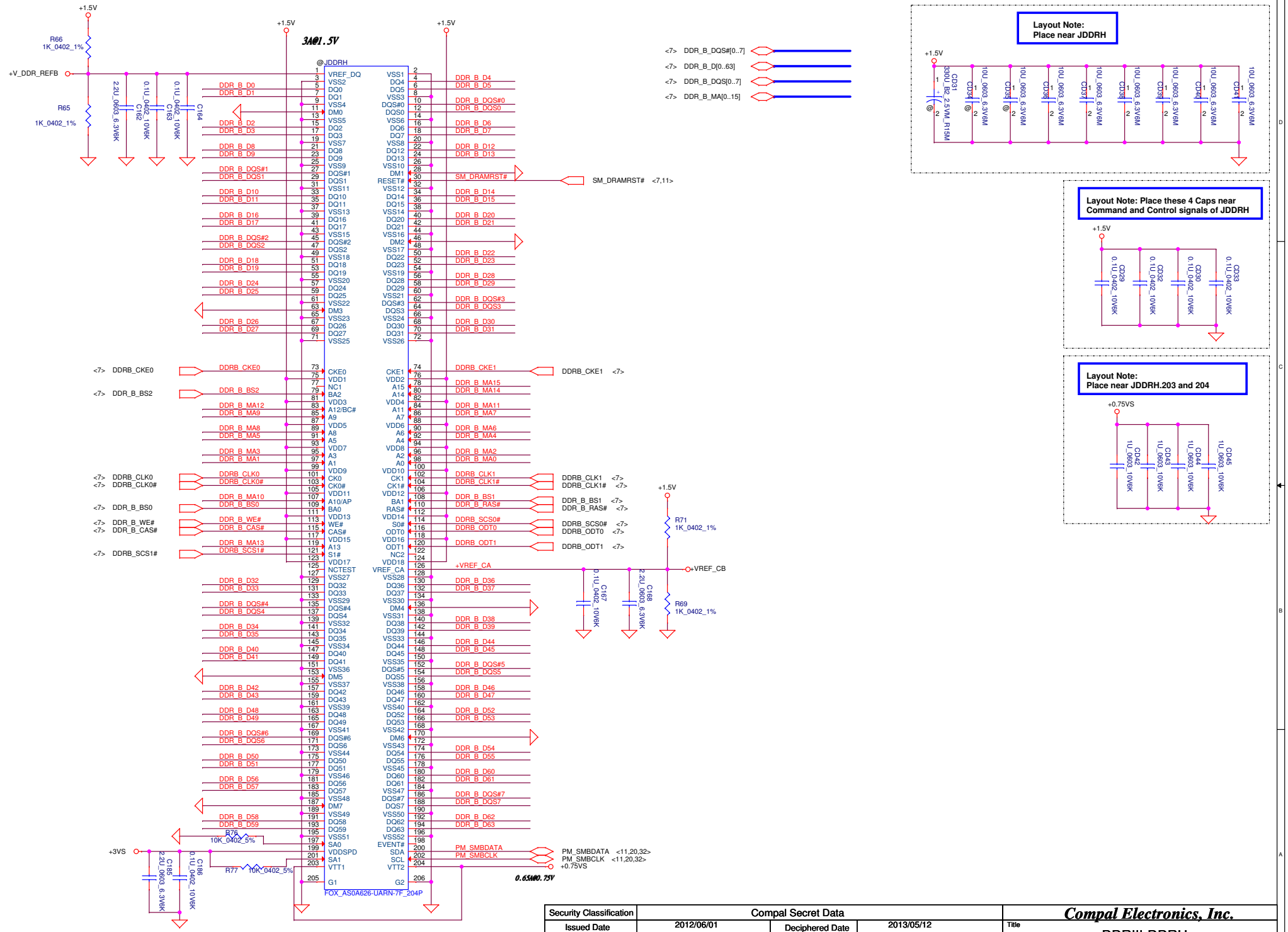

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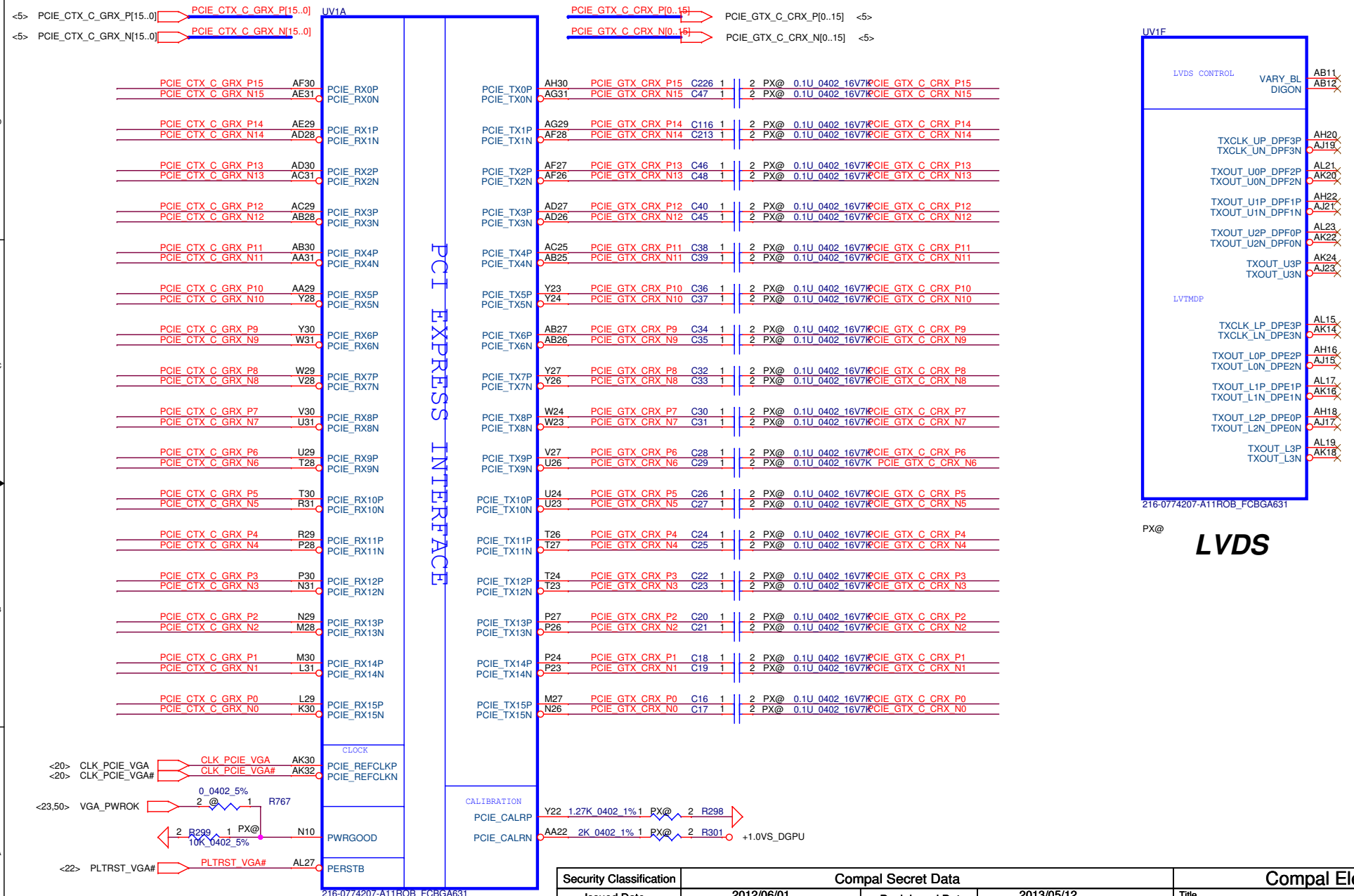
Compal Electronics, Inc.

Title: DDRIII-DDRH

Size | Document Number: VBL30/31 LA-9351P M/B | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 12 of 50



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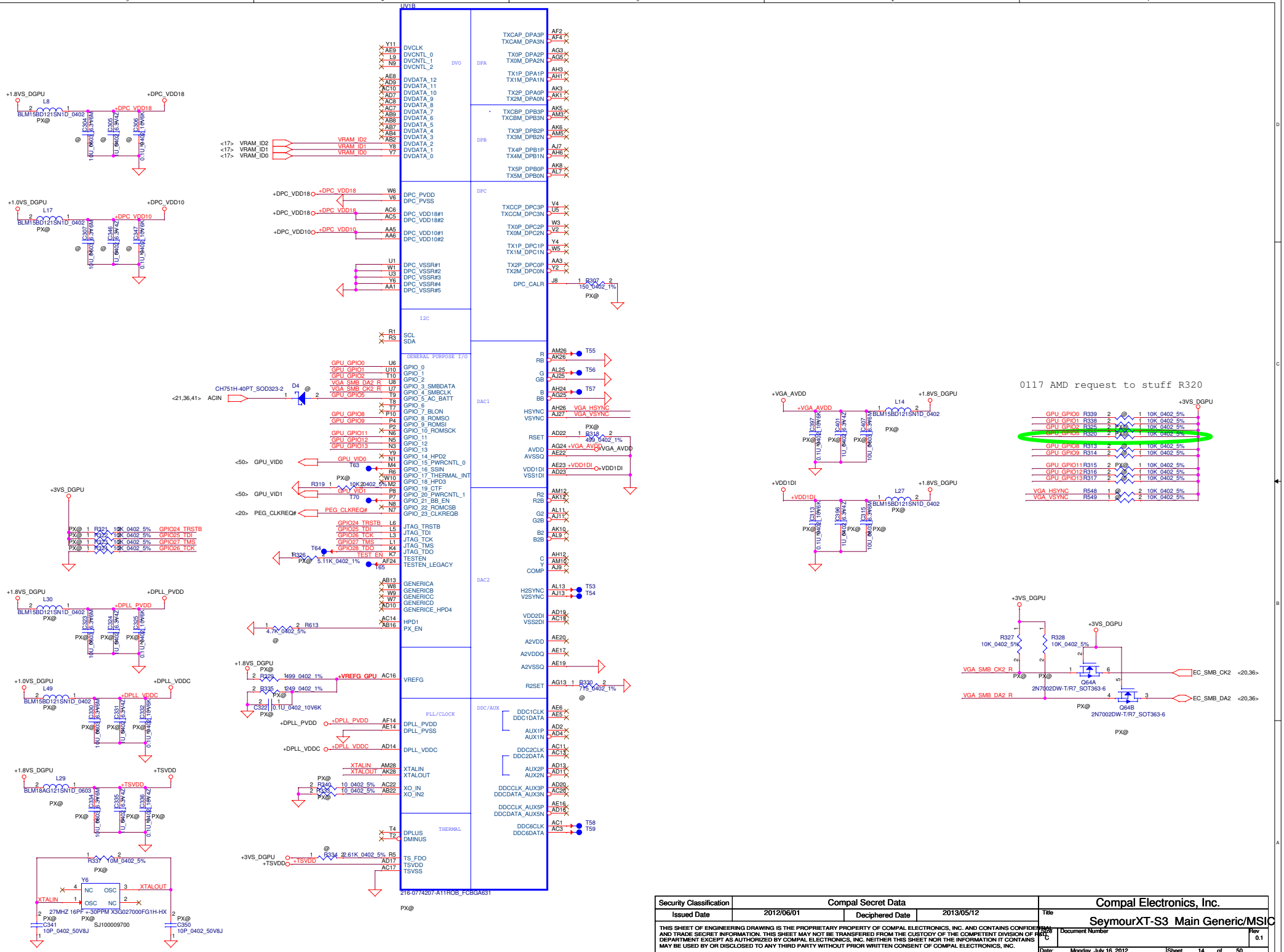
Compal Electronics, Inc.

Title: SeymourXT-S3 PCIE/LVDS

Size: B | Document Number | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 13 of 50



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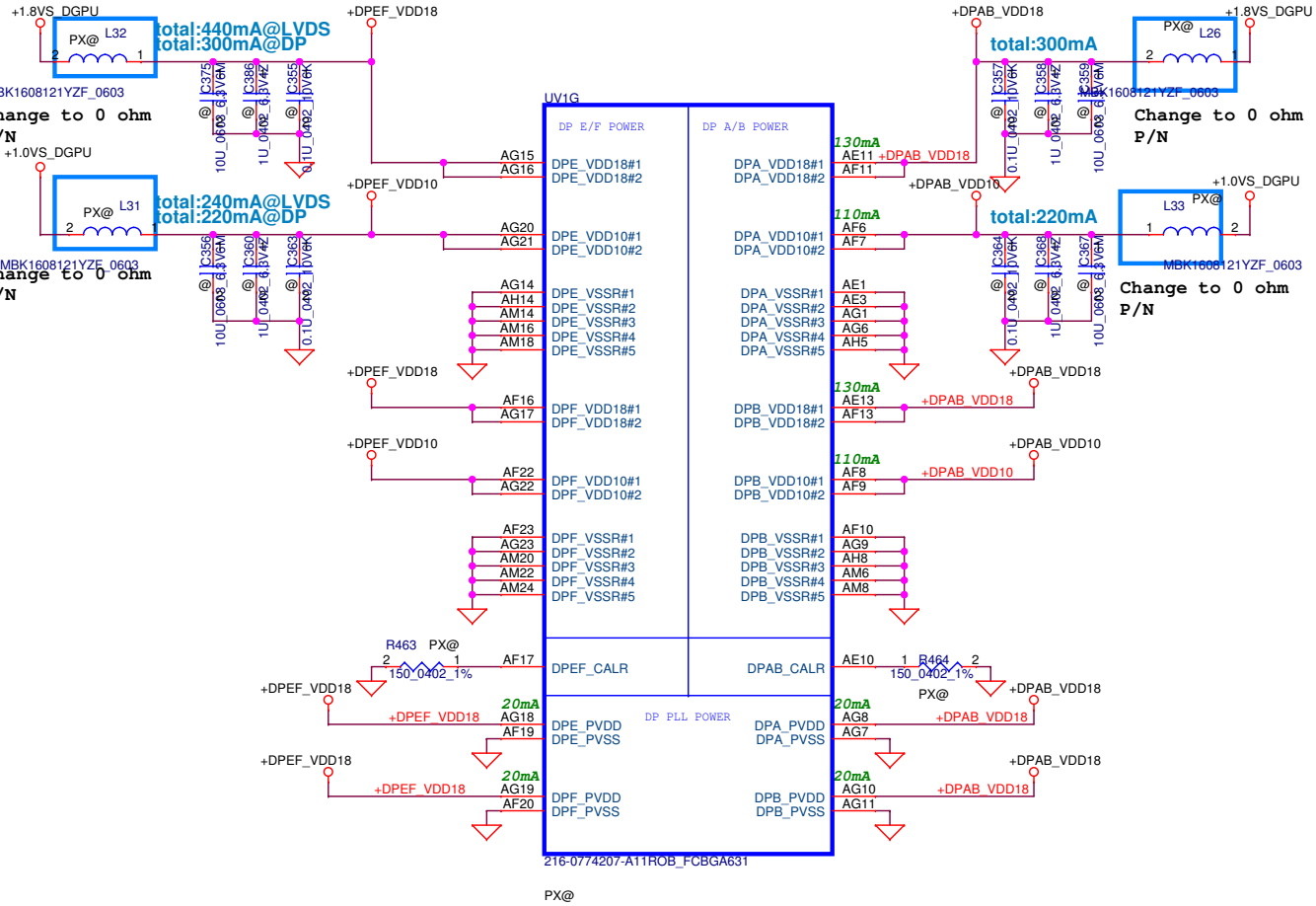
Compal Electronics, Inc.

Title: SeymourXT-S3 Main Generic/MSIC

Size: C | Document Number | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 14 of 50



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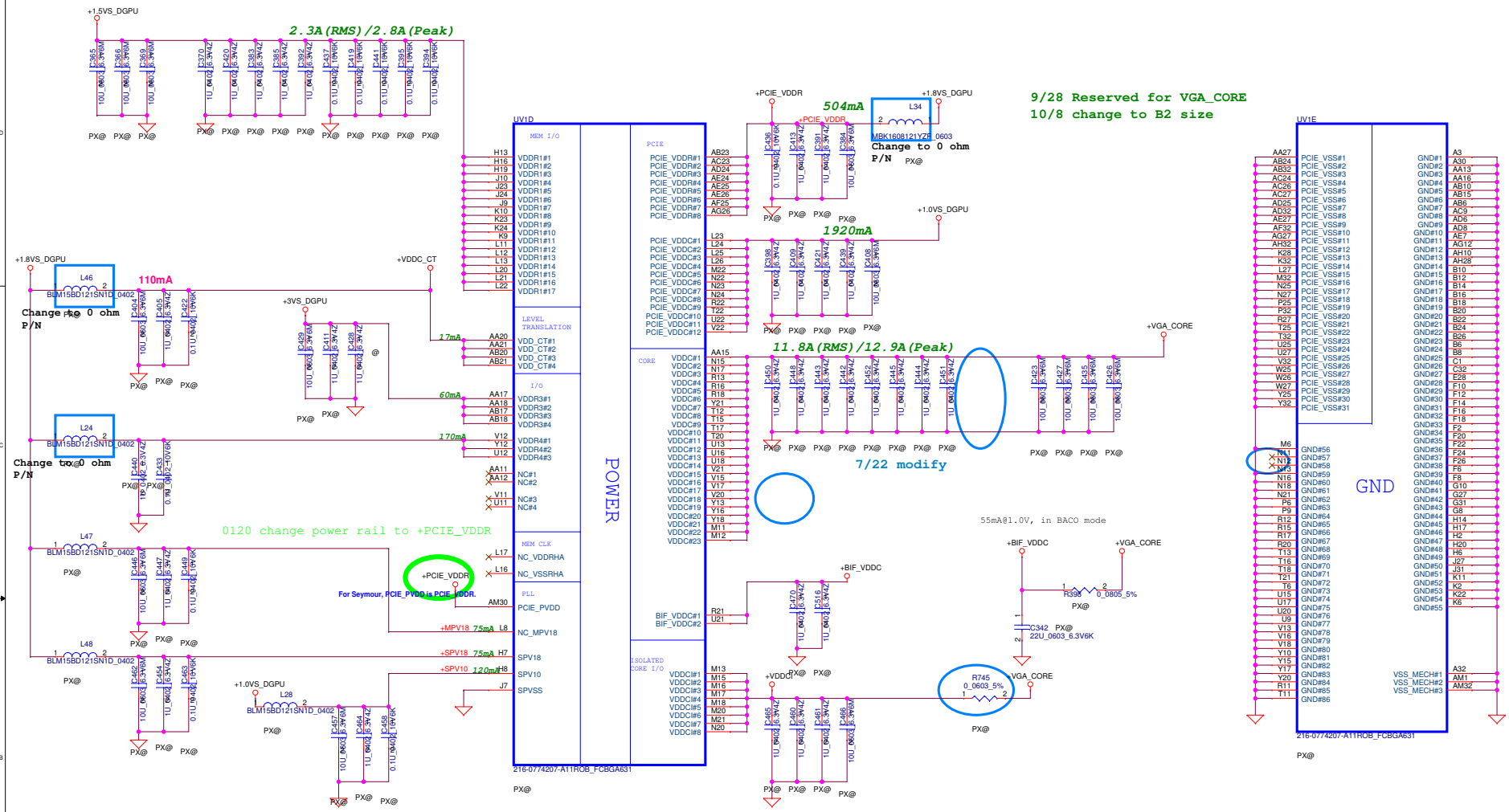
				Date: Monday, July 16, 2012; Sheet 15 of 50



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Compal Electronics, Inc.

Title: SeymourXT-S3 PWR/GND

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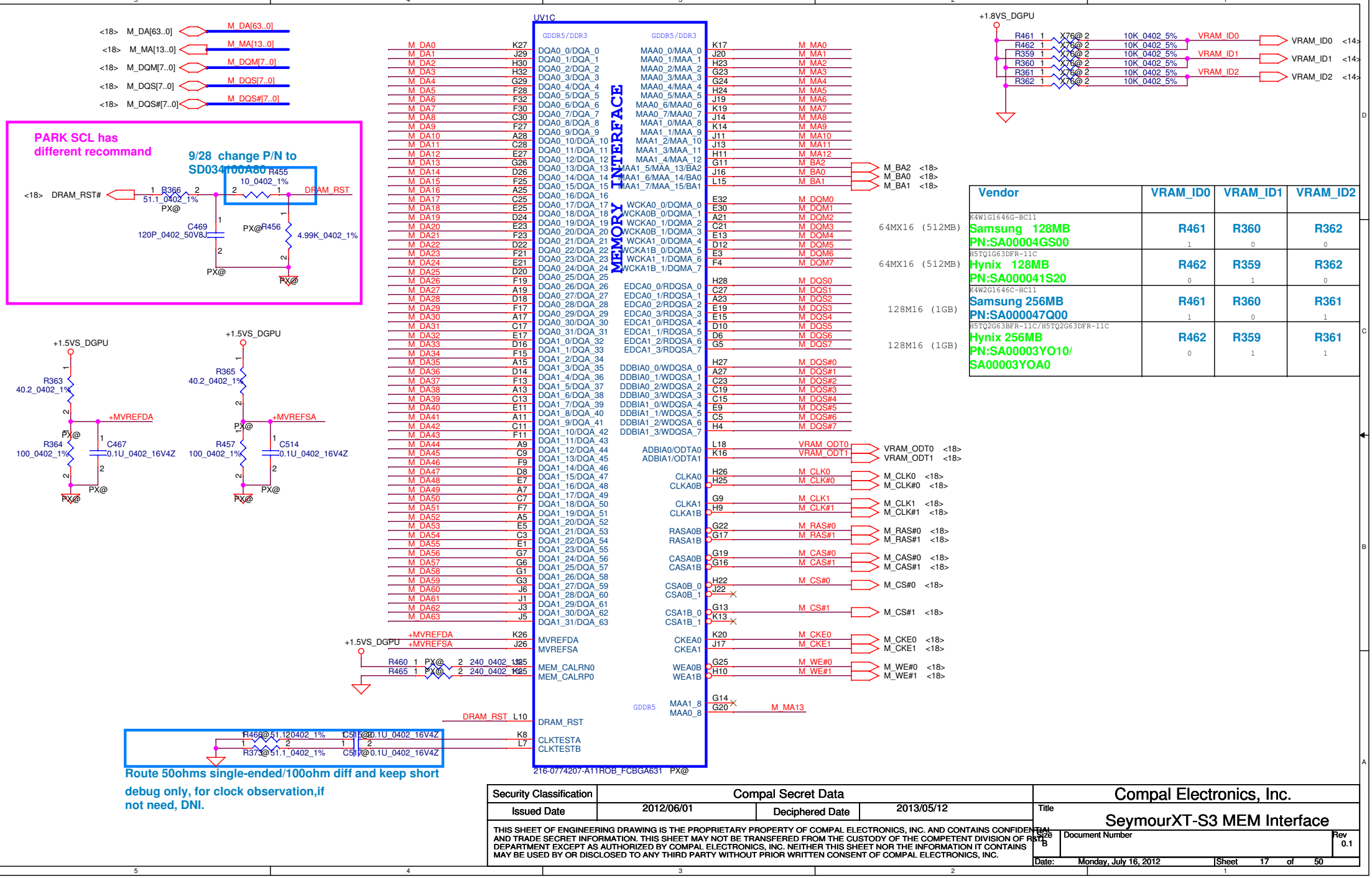
Date: Monday, July 16, 2012 | Sheet 16 of 50



Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
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H5TQ1G63DFR-11C Hynix 128MB PN:SA000041S20	R462 0	R359 1	R362 0
K4W2G1646C-HC11 Samsung 256MB PN:SA000047Q00	R461 1	R360 0	R361 1
H5TQ2G63BFR-11C/H5TQ2G63DFR-11C Hynix 256MB PN:SA00003YO10/ SA00003YOA0	R462 0	R359 1	R361 1

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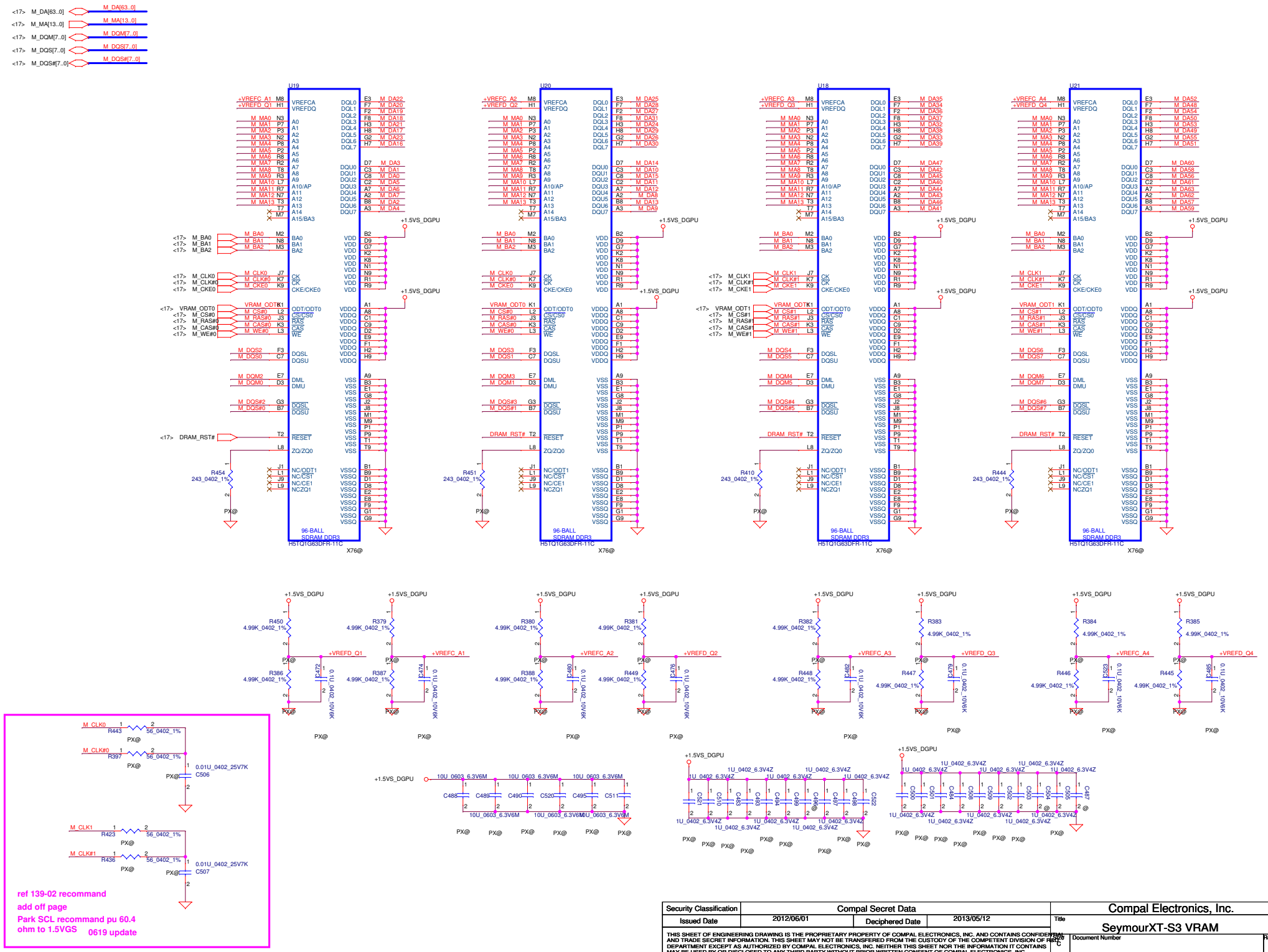
Title: SeymourXT-S3 MEM Interface

Size: B | Document Number | Rev 0.1

Date: Monday, July 16, 2012 | Sheet 17 of 50



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title: SeymourXT-S3 VRAM
				Size: C; Document Number; Rev: 0.1
				Date: Monday, July 16, 2012; Sheet 18 of 50

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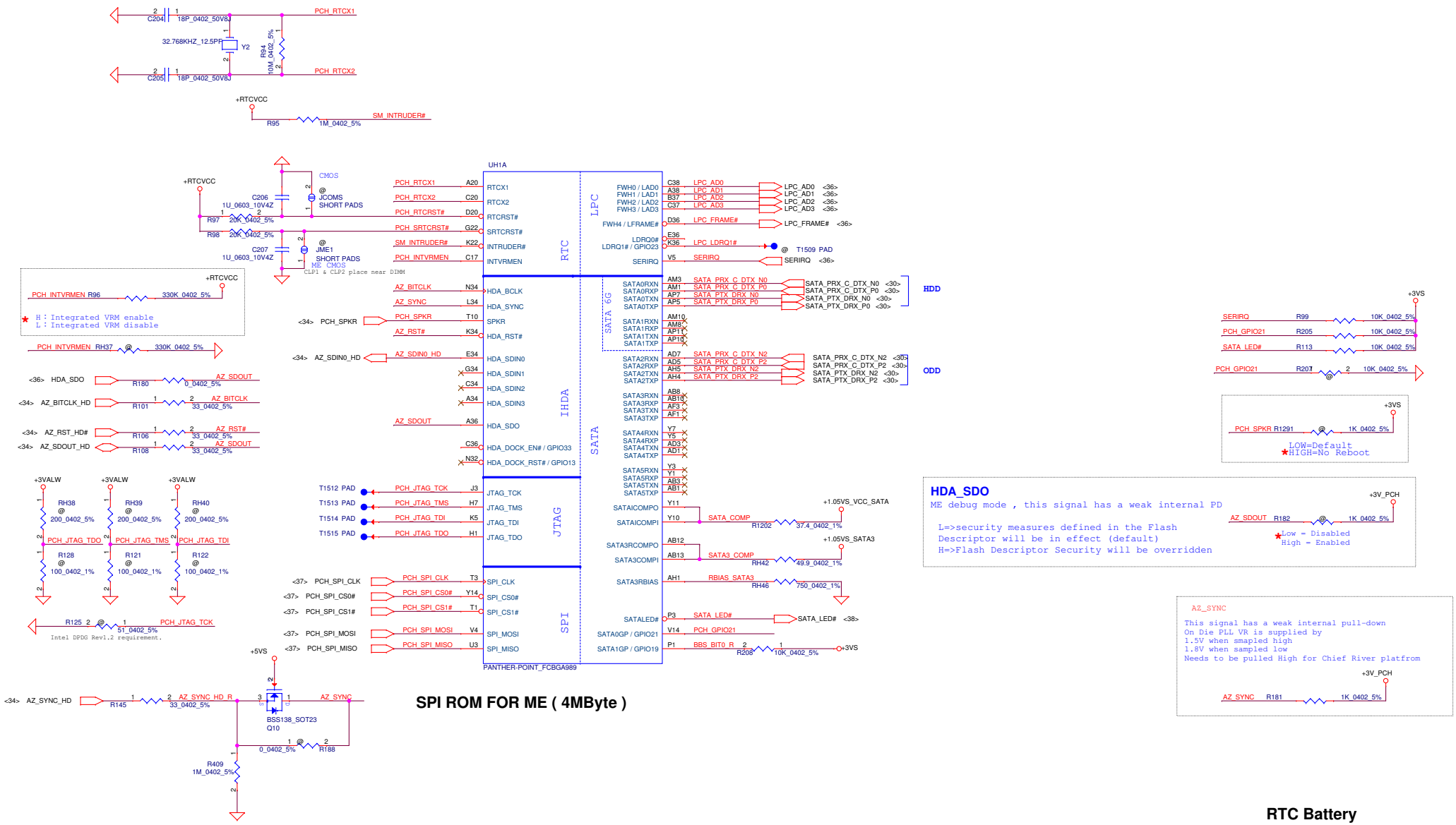

HDA_SDO

ME debug mode , this signal has a weak internal PD

L=>security measures defined in the Flash Descriptor will be in effect (default)
H=>Flash Descriptor Security will be overridden

AZ_SYNC

This signal has a weak internal pull-down
On Die PLL VR is supplied by
1.5V when smapled high
1.8V when sampled low
Needs to be pulled High for Chief River platfrom

SPI ROM FOR ME (4MByte)

RTC Battery

MAX. 8000mil

Security Classification	Compal Secret Data		
Issued Date	2012/06/01	Deciphered Date	2013/05/12

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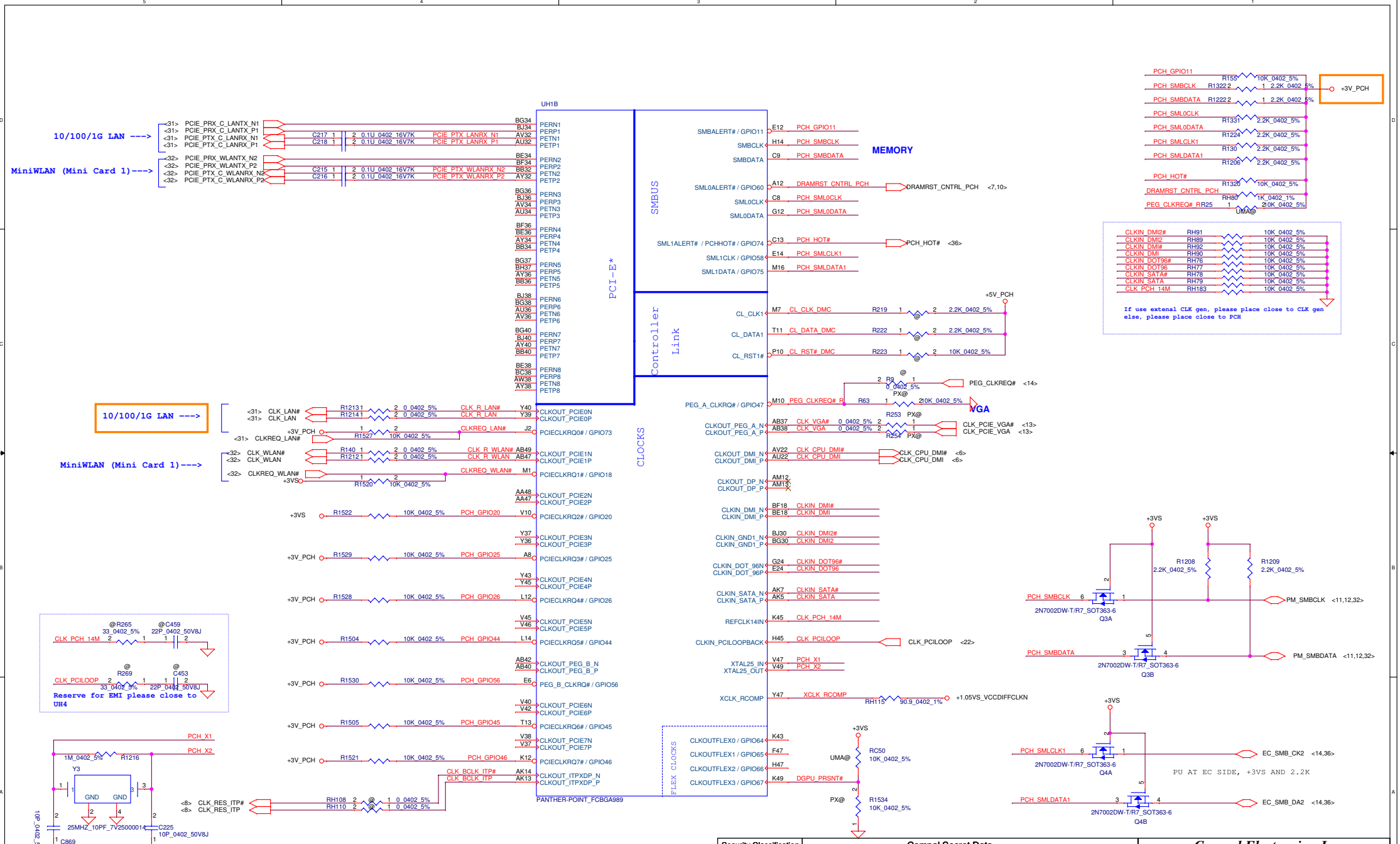
Compal Electronics, Inc.

Title: PCH (1/8) SATA,HDA,SPI, LPC

Size: A | Custom | Document Number: VBL30/31 LA-9351P M/B | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 19 of 50



Security Classification	Compal Secret Data		
Issued Date	2012/06/01	Deciphered Date	2013/05/12

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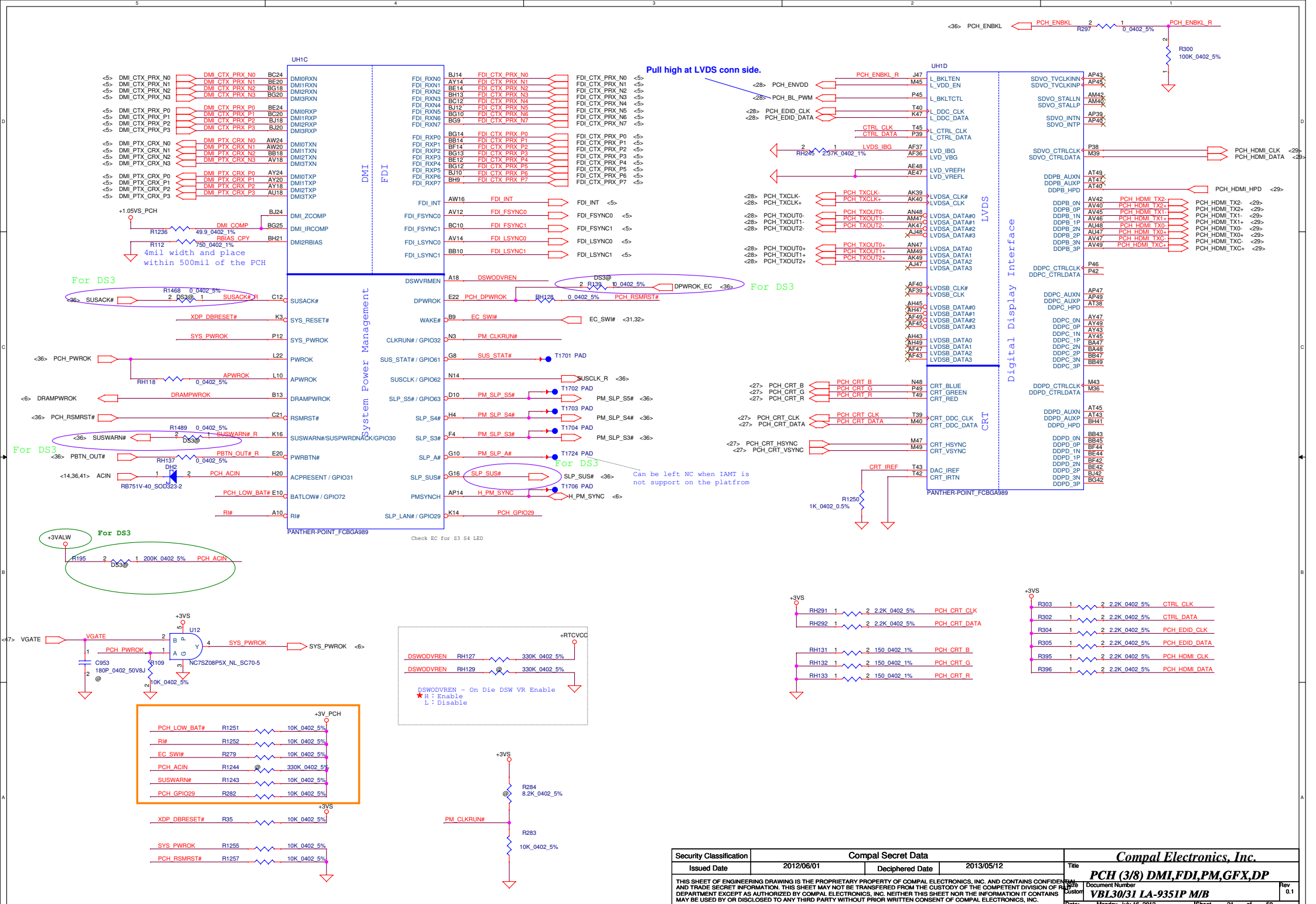
Compal Electronics, Inc.

Title: **PCH (2/8) PCIE, SMBUS, CLK**

Size: Custom | Document Number: **VBL30/31 LA-9351P M/B** | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 20 of 50



Security Classification	Compal Secret Data		
Issued Date	2012/06/01	Deciphered Date	2013/05/12

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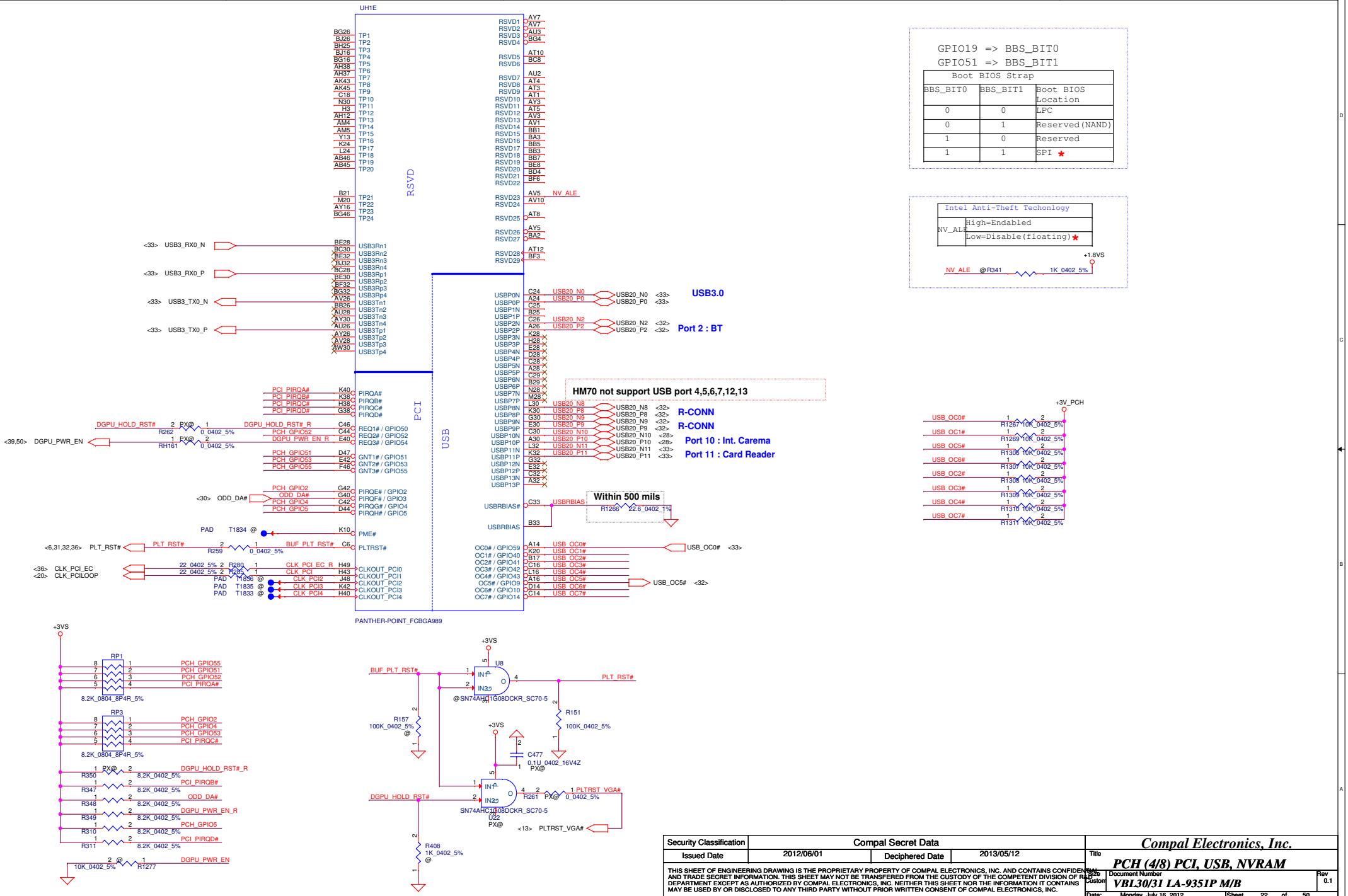
Compal Electronics, Inc.

Title: PCH (3/8) DMI,FDI,PM,GFX,DP

Size: Custom | Document Number: VBL30/31 LA-9351P M/B | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 21 of 50



Security Classification	Compal Secret Data		
Issued Date	2012/06/01	Deciphered Date	2013/05/12

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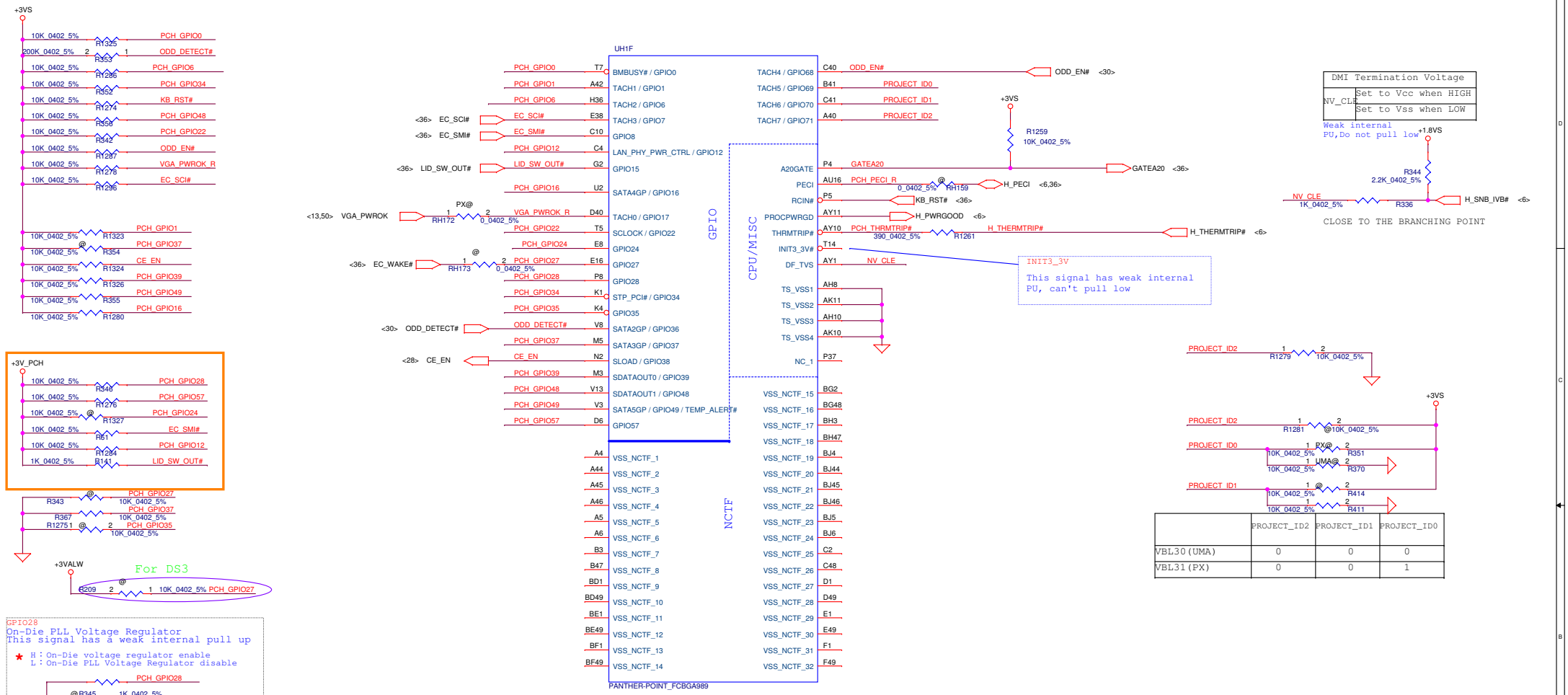
Compal Electronics, Inc.

Title: **PCH (4/8) PCI, USB, NVRAM**

Size: Custom | Document Number: **VBL30/31 LA-9351P M/B** | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 22 of 50



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VBL31(PX)	0	0	1

Security Classification	Compal Secret Data		
Issued Date	2012/06/01	Deciphered Date	2013/05/12

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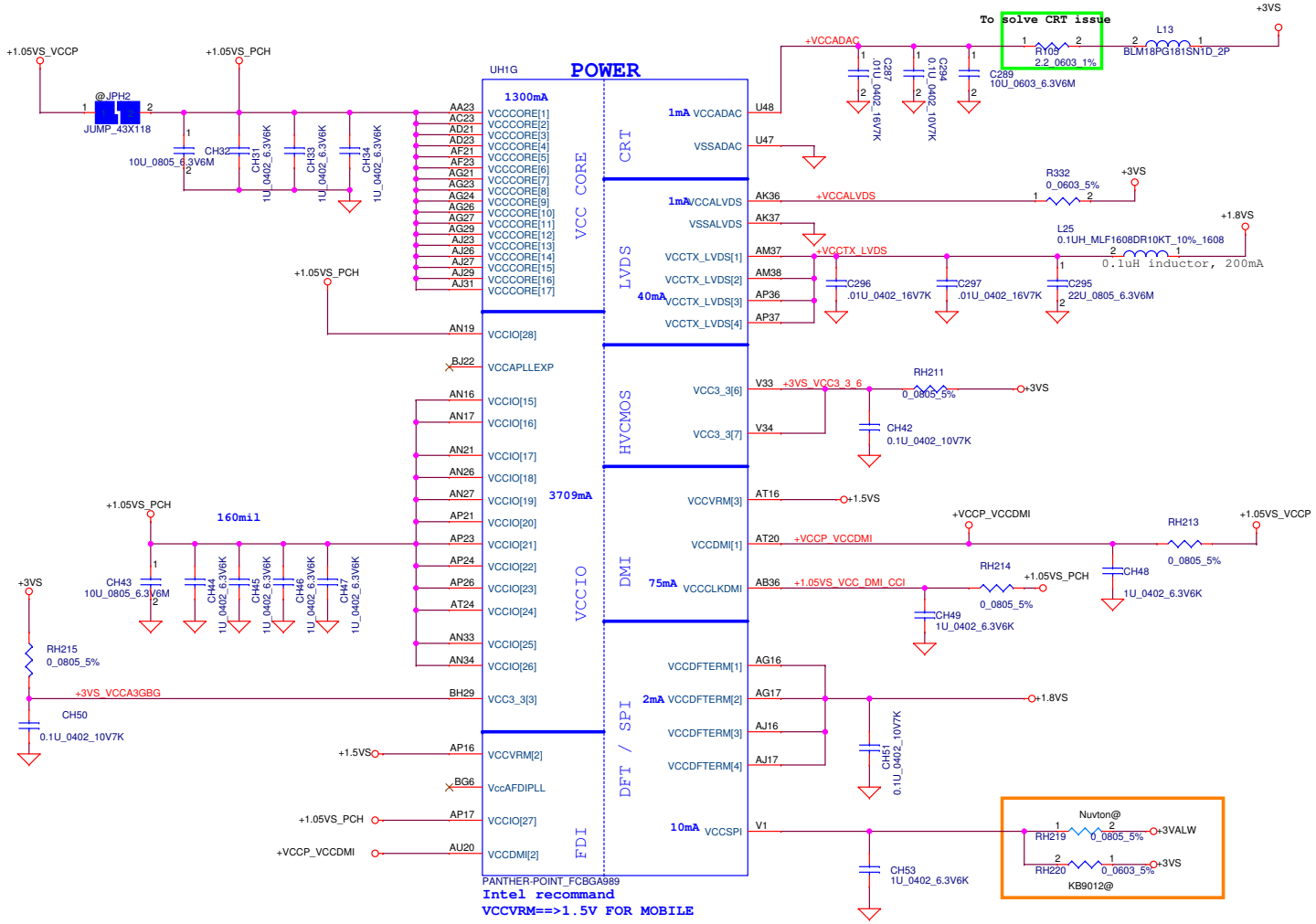
Compal Electronics, Inc.

Title: PCH (5/8) GPIO, CPU, MISC

Size: Custom | Document Number: VBL30/31 LA-9351P M/B | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 23 of 50



PCH Power Rail Table
Refer to CPU EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

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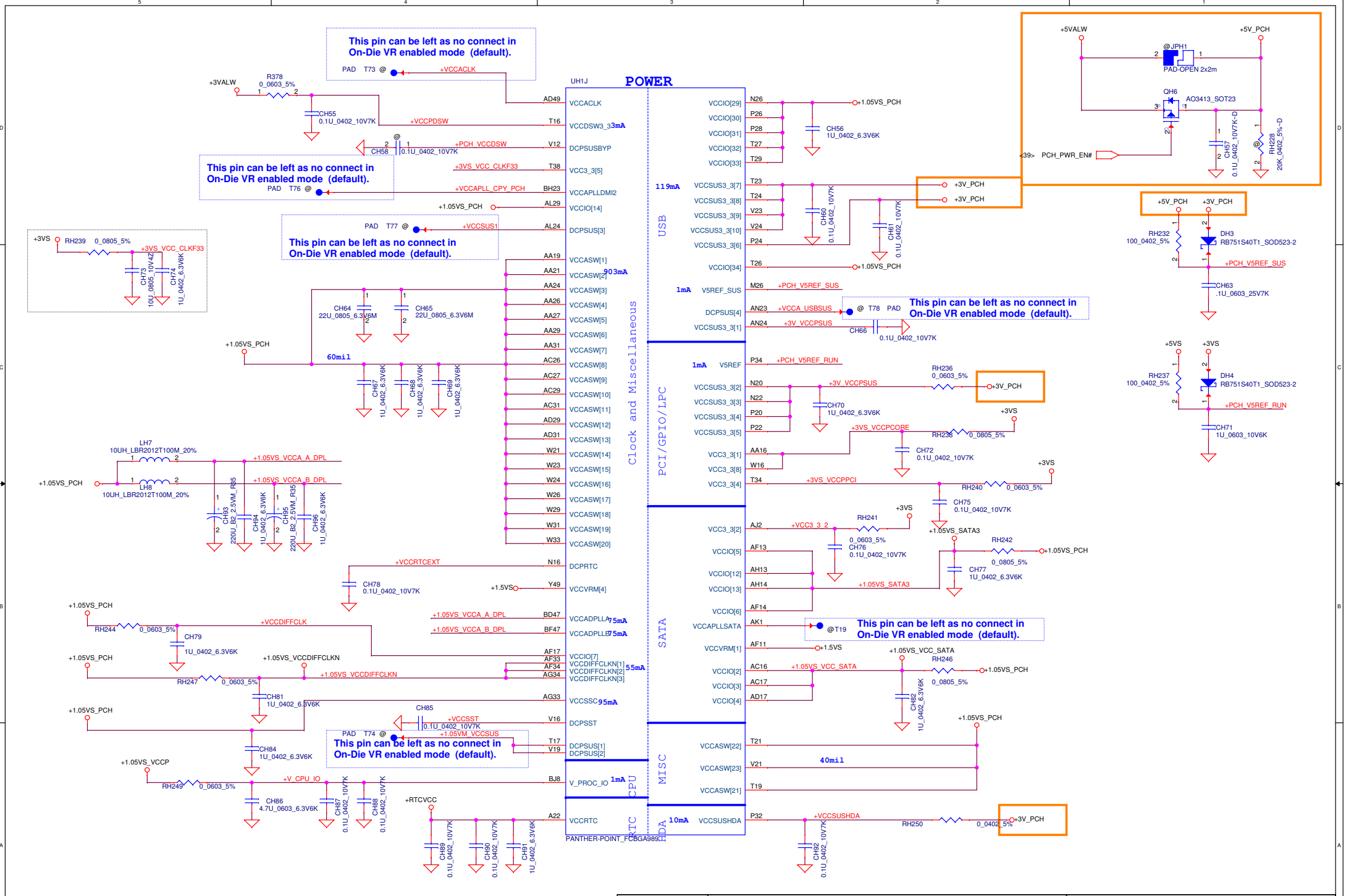
Compal Electronics, Inc.

Title: PCH (6/8) PWR

Size: Custom | Document Number: VBL30/31 LA-9351P M/B | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 24 of 50



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Issued Date	2012/06/01	Deciphered Date	2013/05/12

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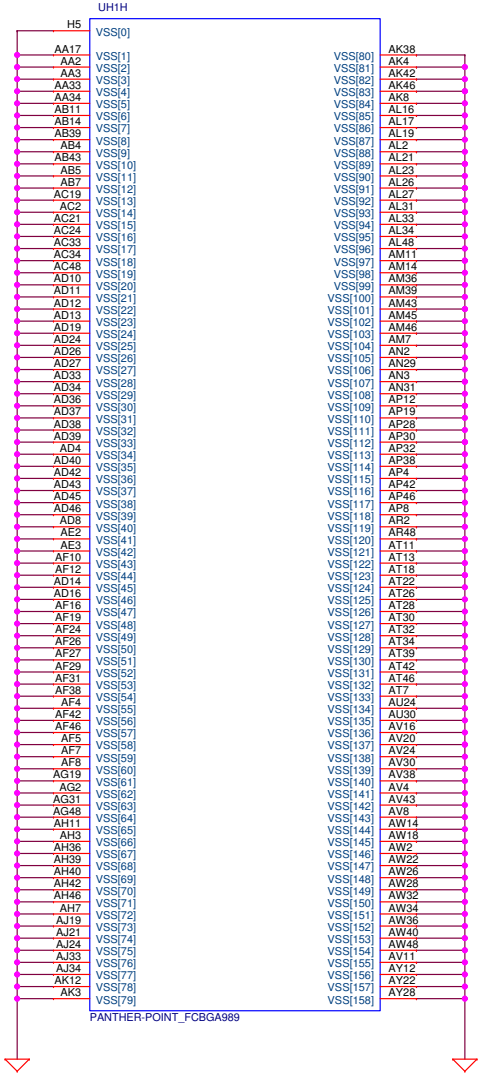
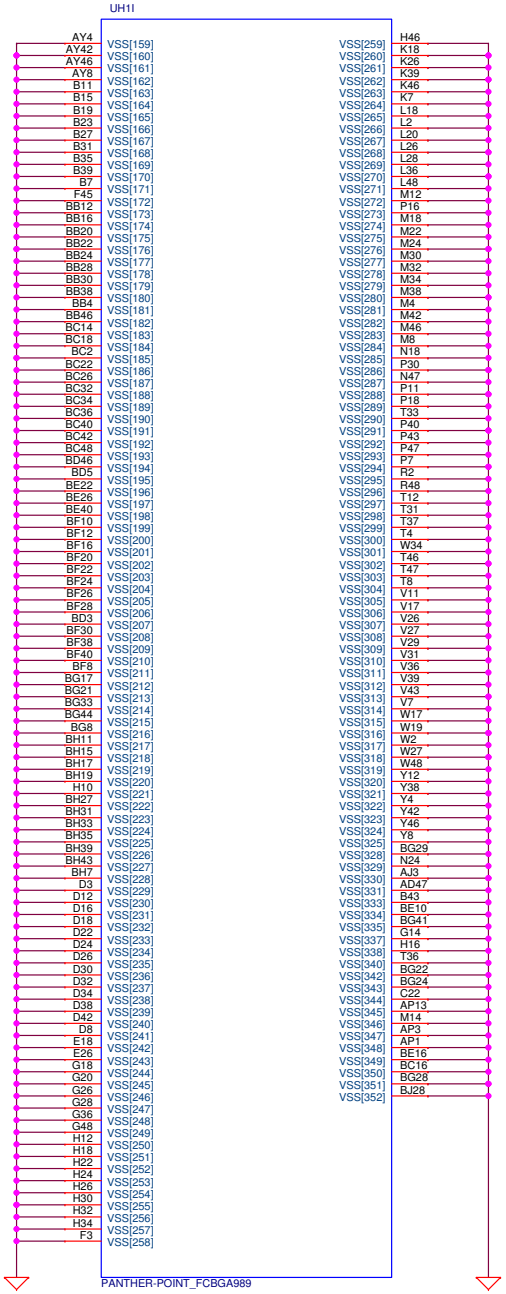
Compal Electronics, Inc.

Title: **PCH (7/8) PWR**

Size: Custom | Document Number: **VBL30/31 LA-9351P M/B** | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 25 of 50





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Issued Date	2012/06/01	Deciphered Date	2013/05/12

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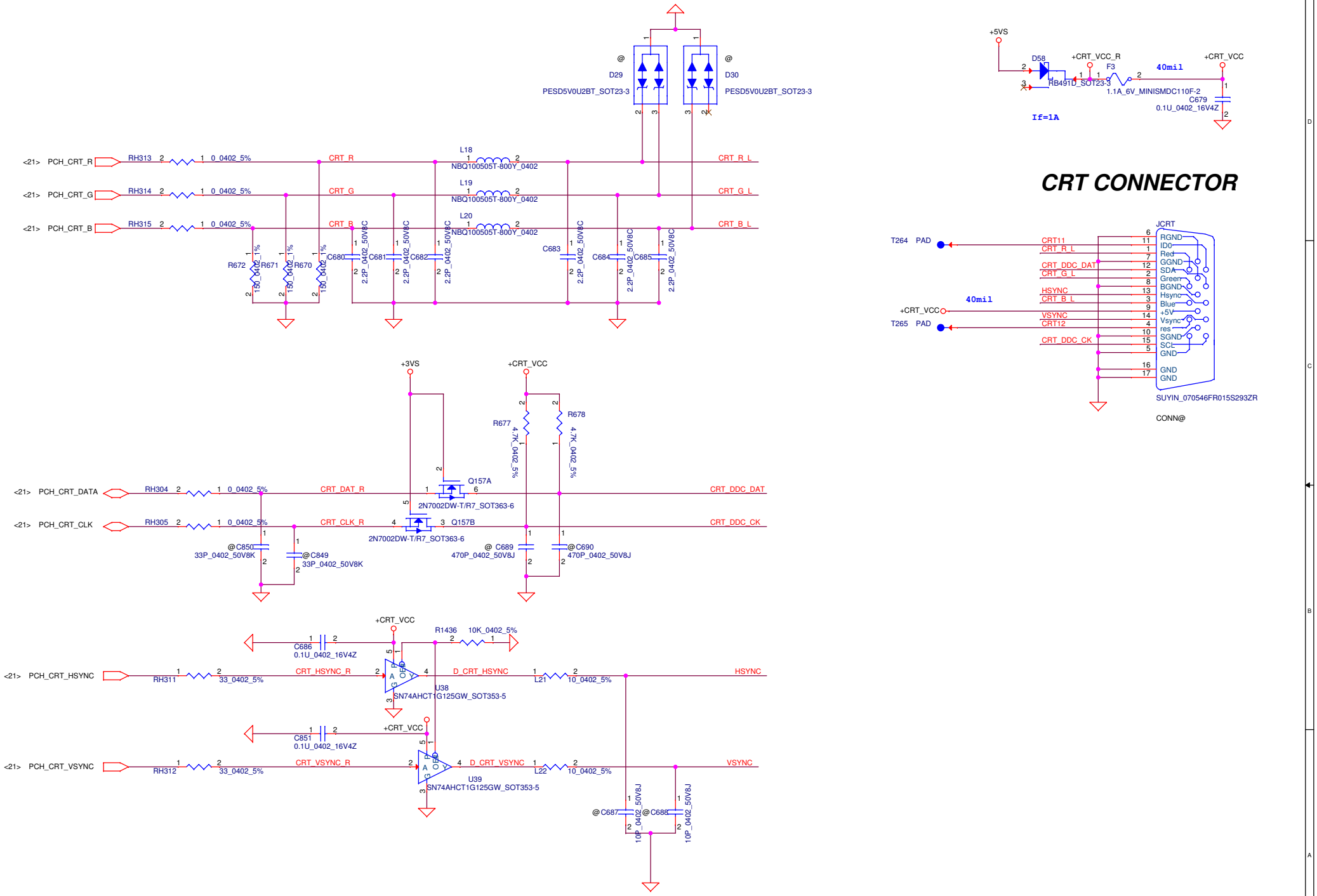
Compal Electronics, Inc.

Title: **PCH (8/8) VSS**

Size: Custom | Document Number: **VBL30/31 LA-9351P M/B** | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 26 of 50



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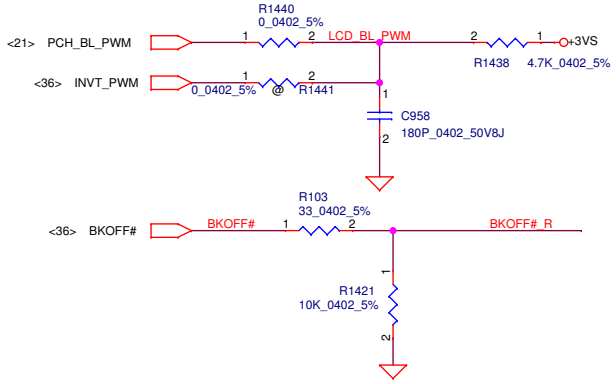
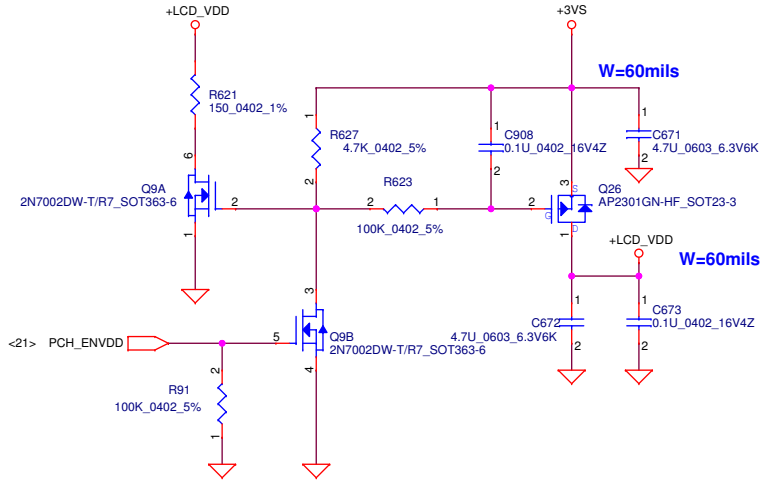
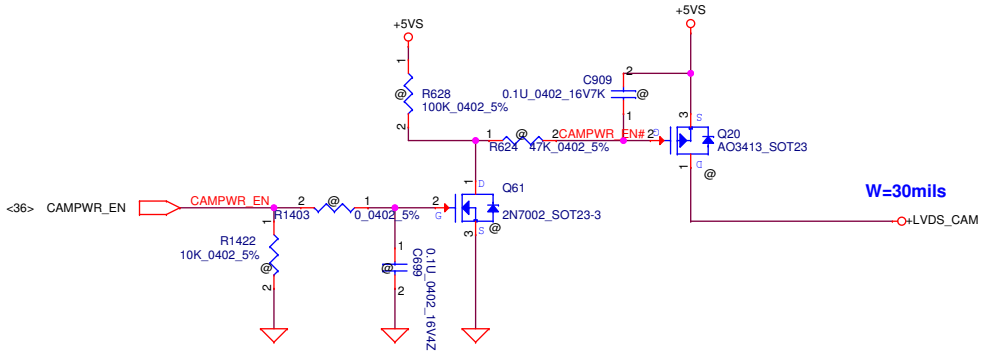
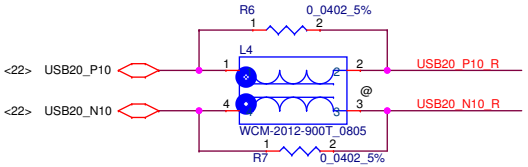
				Date: Monday, July 16, 2012 — Sheet 27 of 50



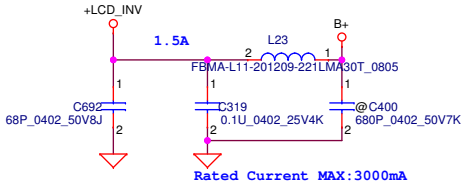
LCD POWER CIRCUIT

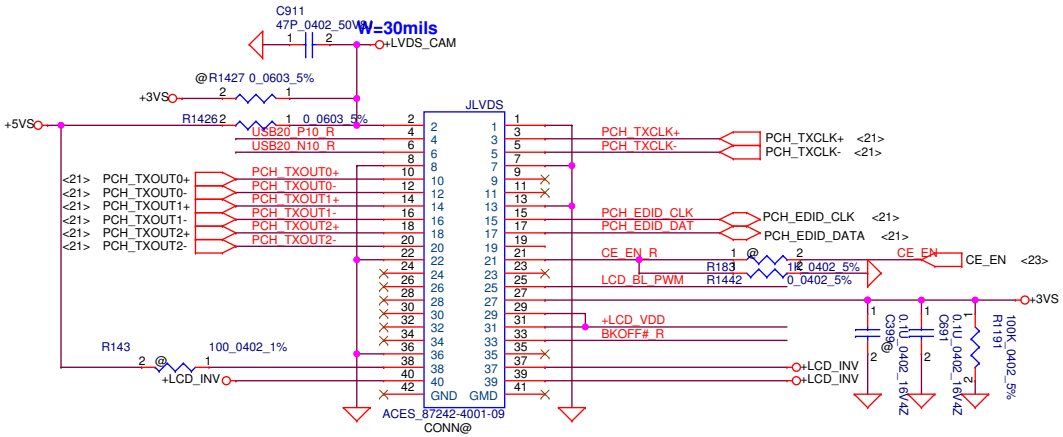






LCD/PANEL BD. Conn.





Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title: LVDS
				Document Number: VBL30/31 LA-9351P M/B — Rev 0.1
				Date: Monday, July 16, 2012 — Sheet 28 of 50

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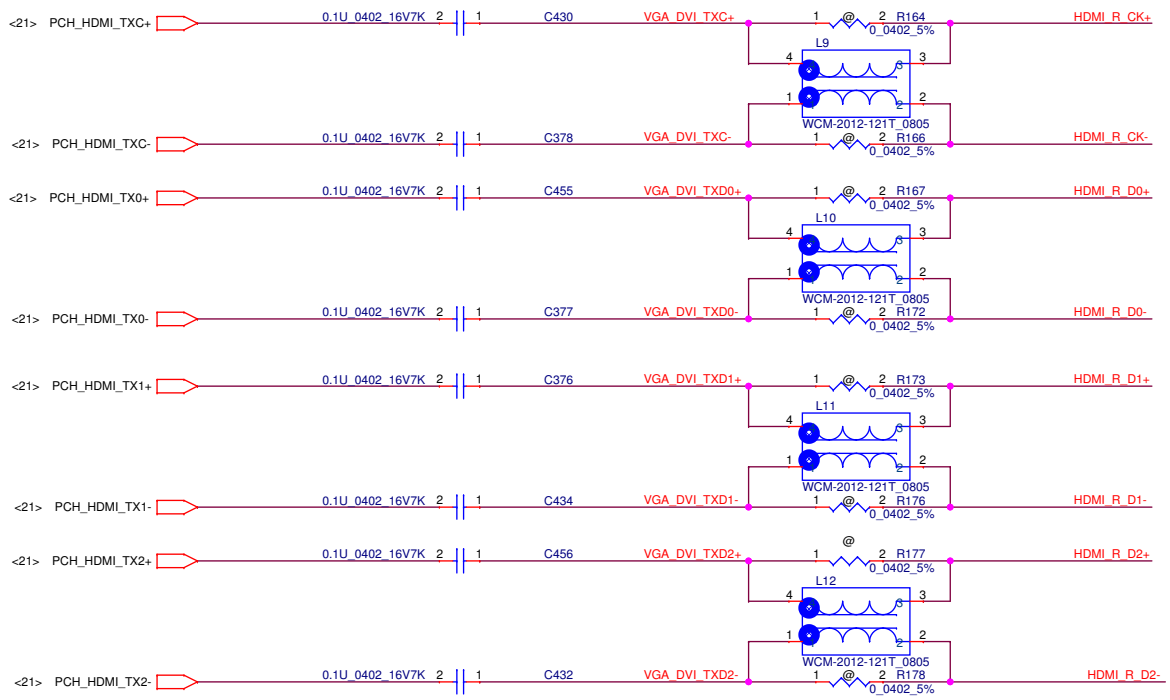
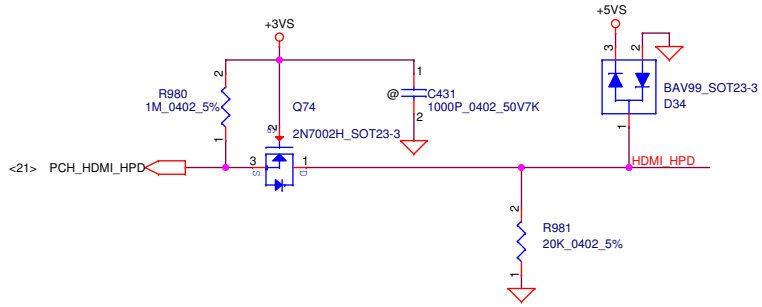
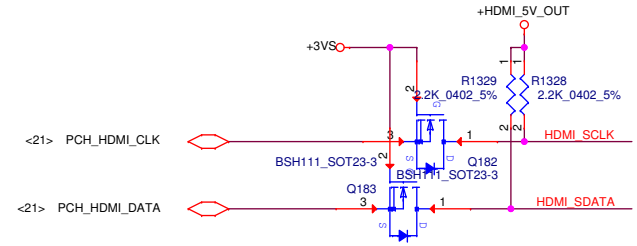
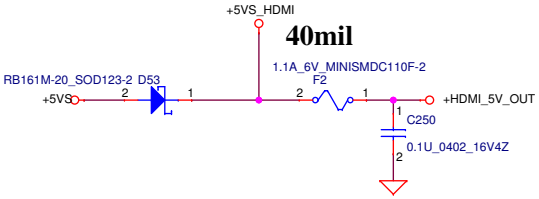
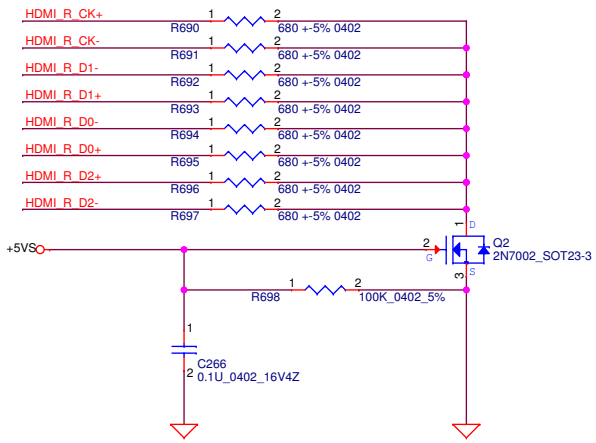


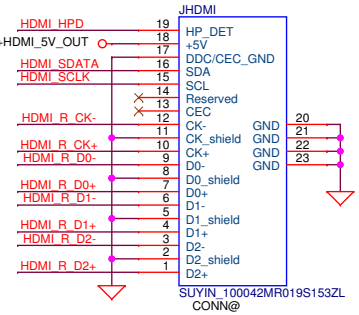






HDMI Connector





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Issued Date	2012/06/01	Deciphered Date	2013/05/12

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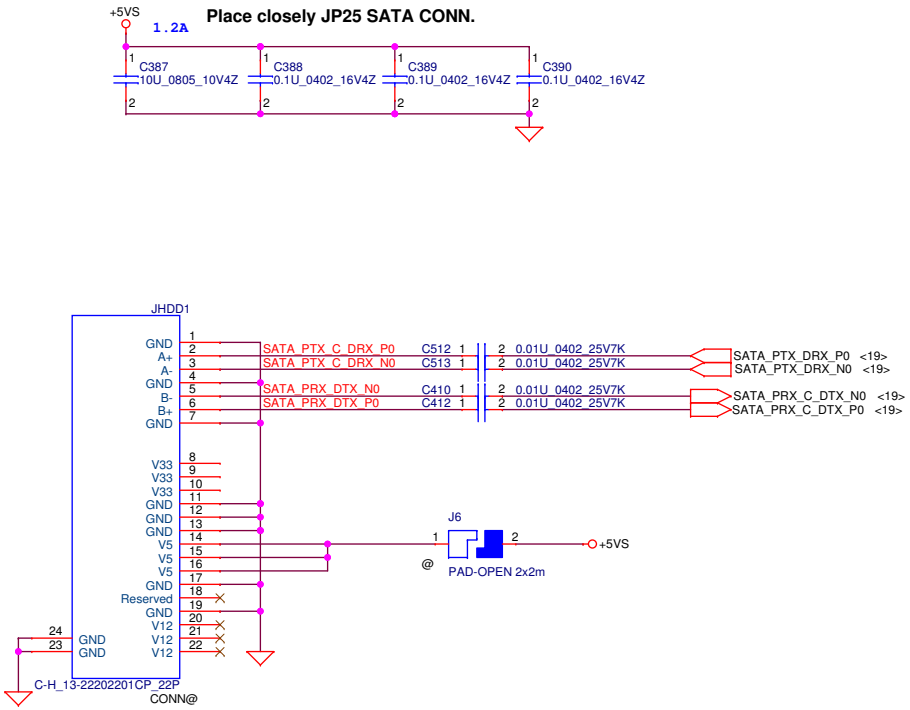
Compal Electronics, Inc.

Title: HDMI Connector

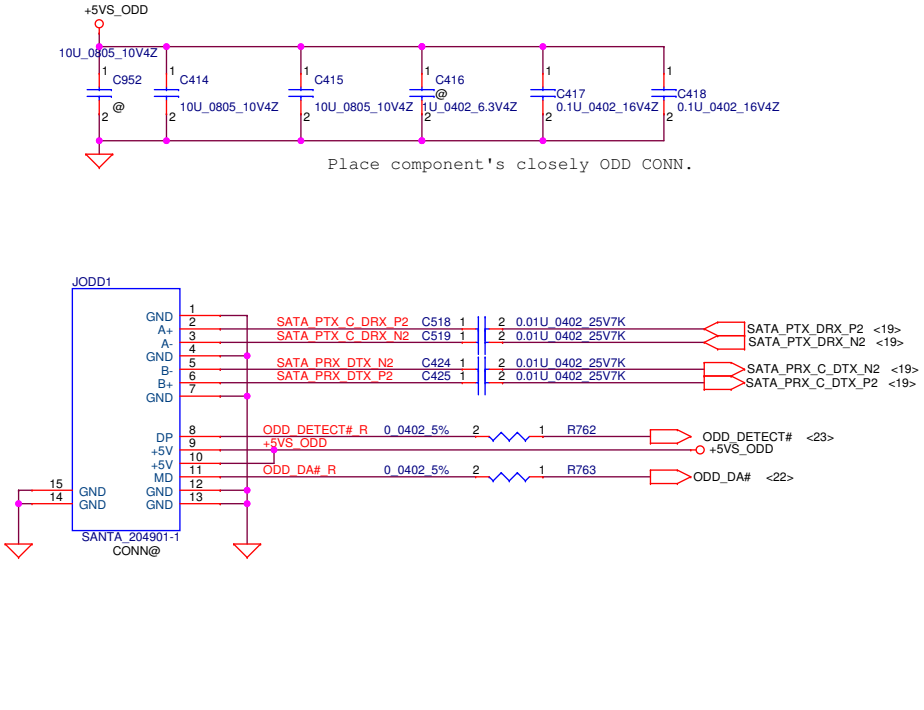
Size: B | Document Number: VBL30/31 LA-9351P M/B | Rev: 0.1

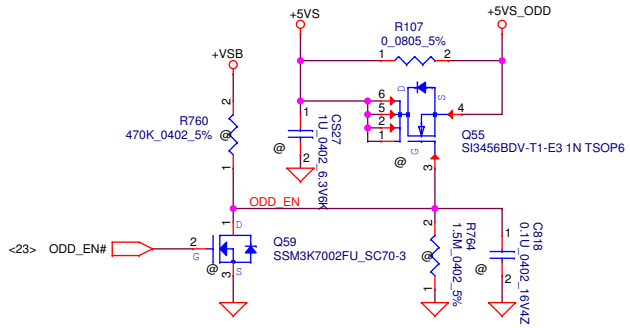
Date: Monday, July 16, 2012 | Sheet 29 of 50

SATA HDD1 Conn.



SATA ODD Conn





Security Classification	Compal Secret Data		
Issued Date	2012/06/01	Deciphered Date	2013/05/12

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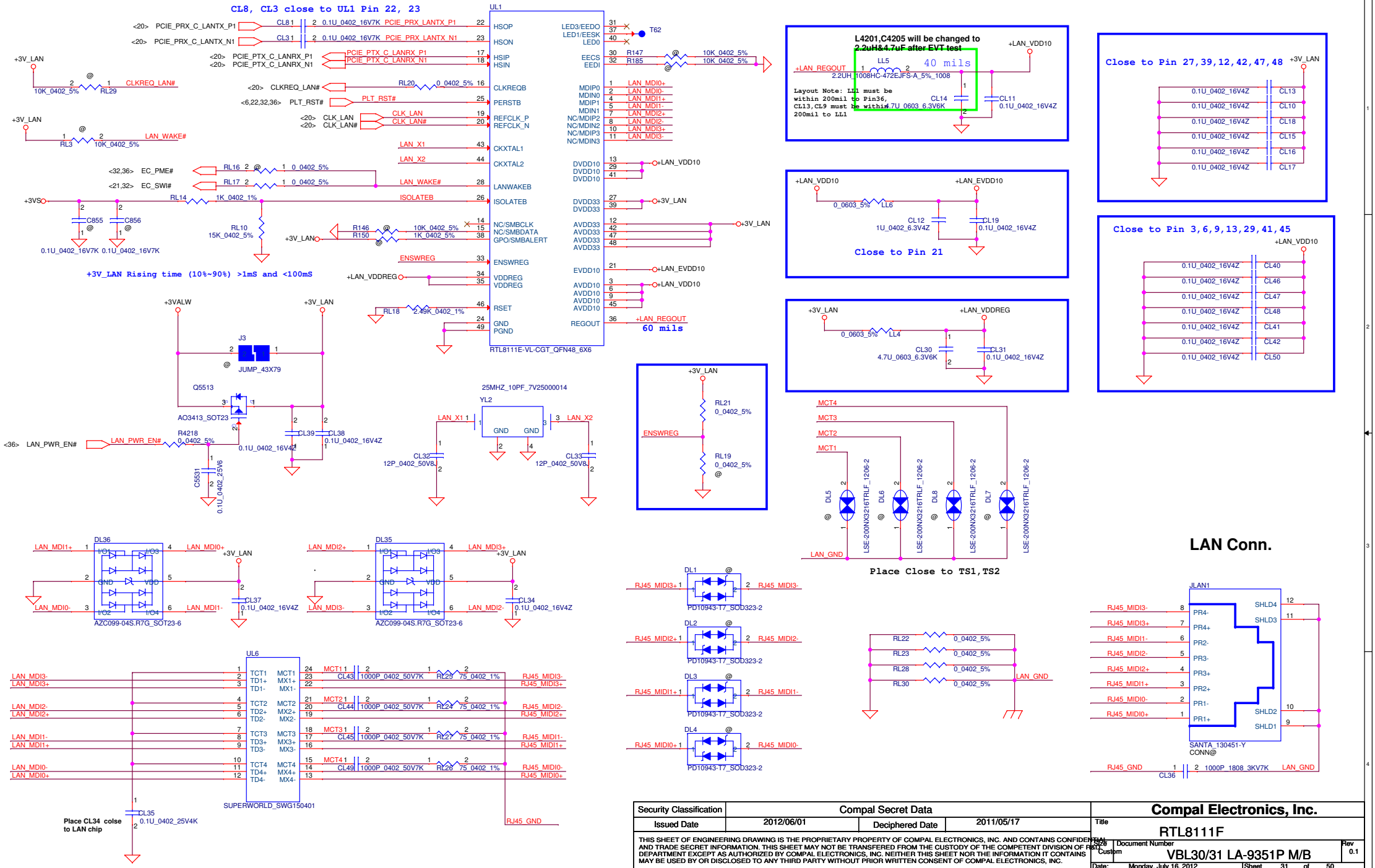
Compal Electronics, Inc.

Title: SATA-HDD/ODD

Document Number: VBL30/31 LA-9351P M/B

Rev: 0.1

Date: Monday, July 16, 2012



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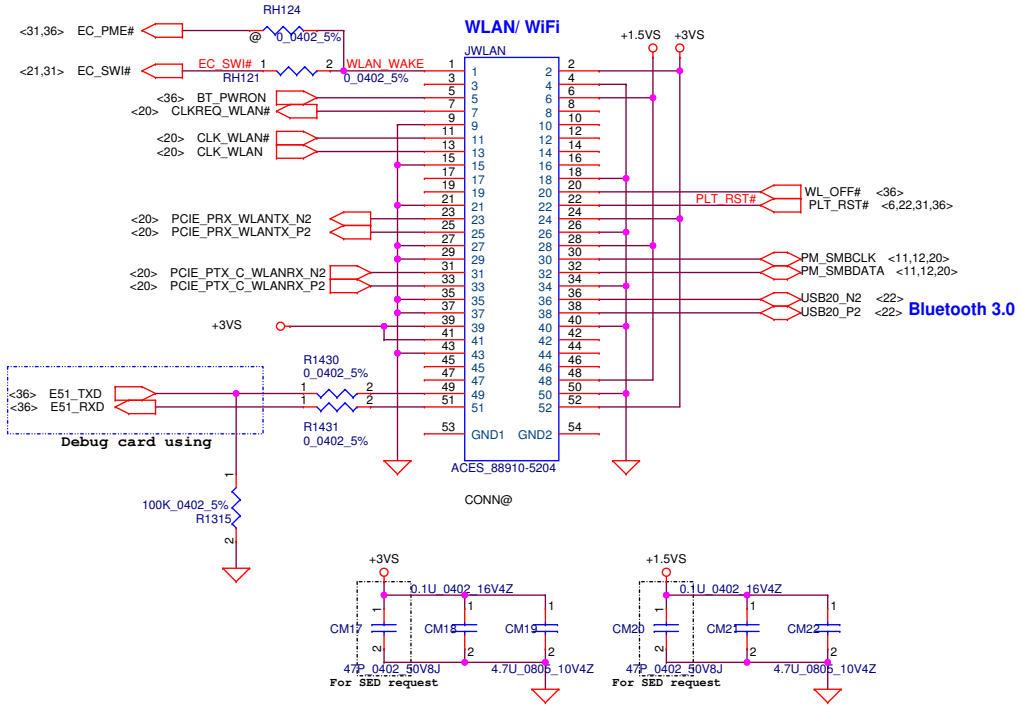
Compal Electronics, Inc.

Title: RTL8111F

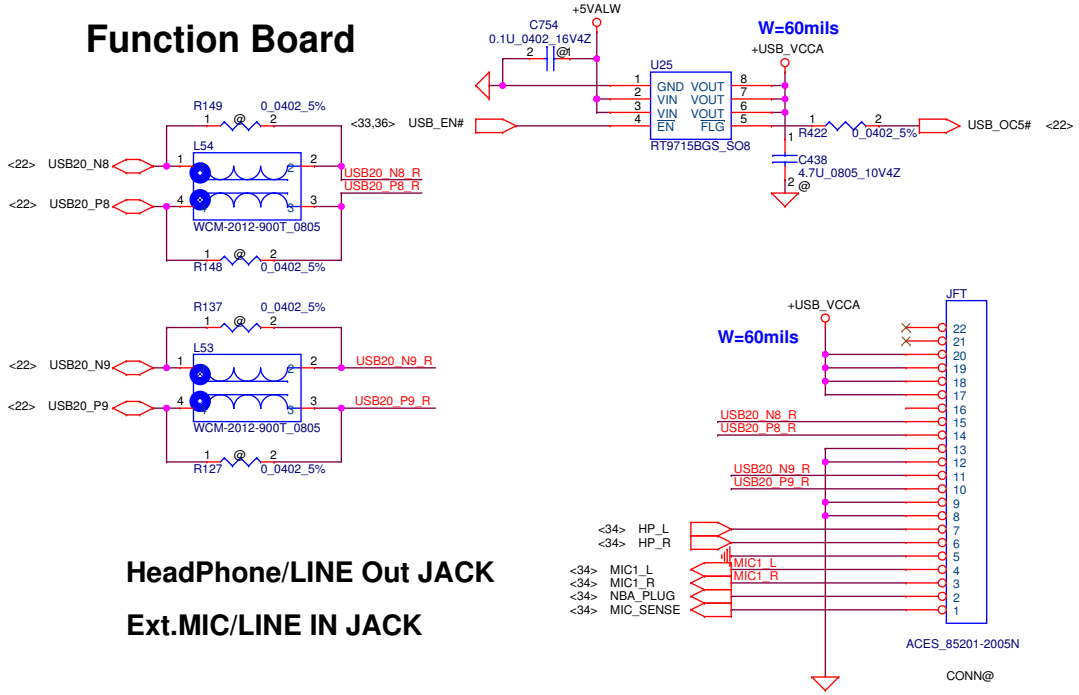
Size: Custom | Document Number: VBL30/31 LA-9351P M/B | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 31 of 50

Slot 1 Half PCIe Mini Card-WLAN & BT3.0

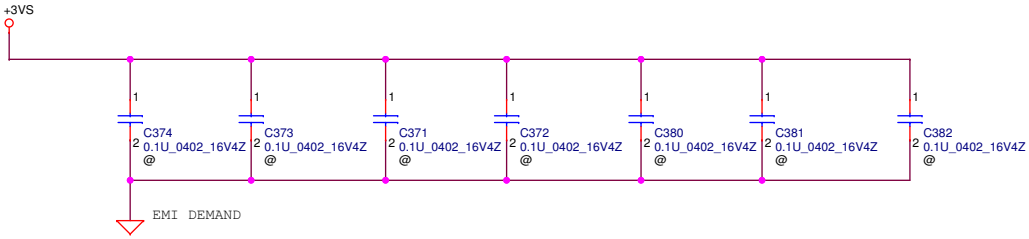


Function Board



HeadPhone/LINE Out JACK

Ext.MIC/LINE IN JACK



Security Classification	Compal Secret Data		
Issued Date	2012/06/01	Deciphered Date	2013/05/12

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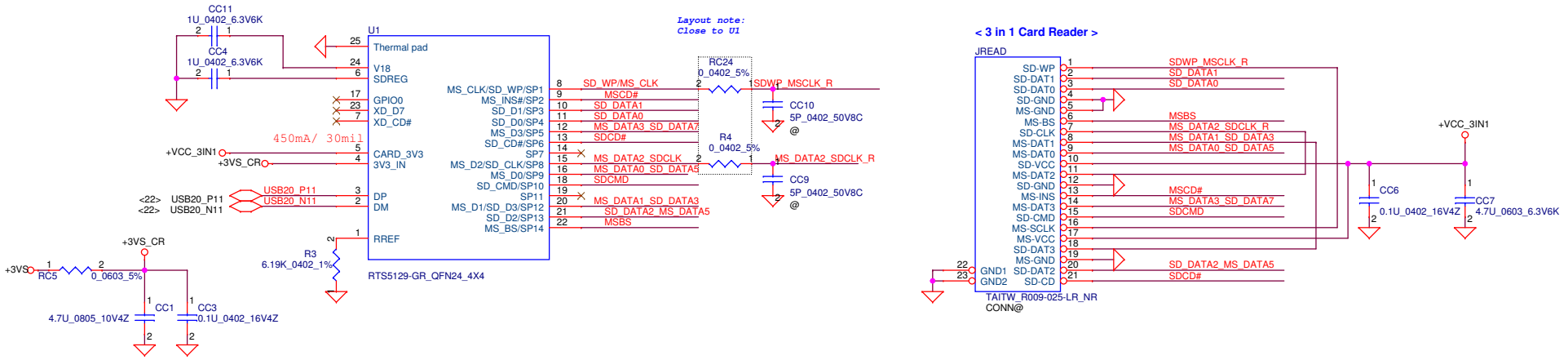
Compal Electronics, Inc.

Title: WLAN/USB

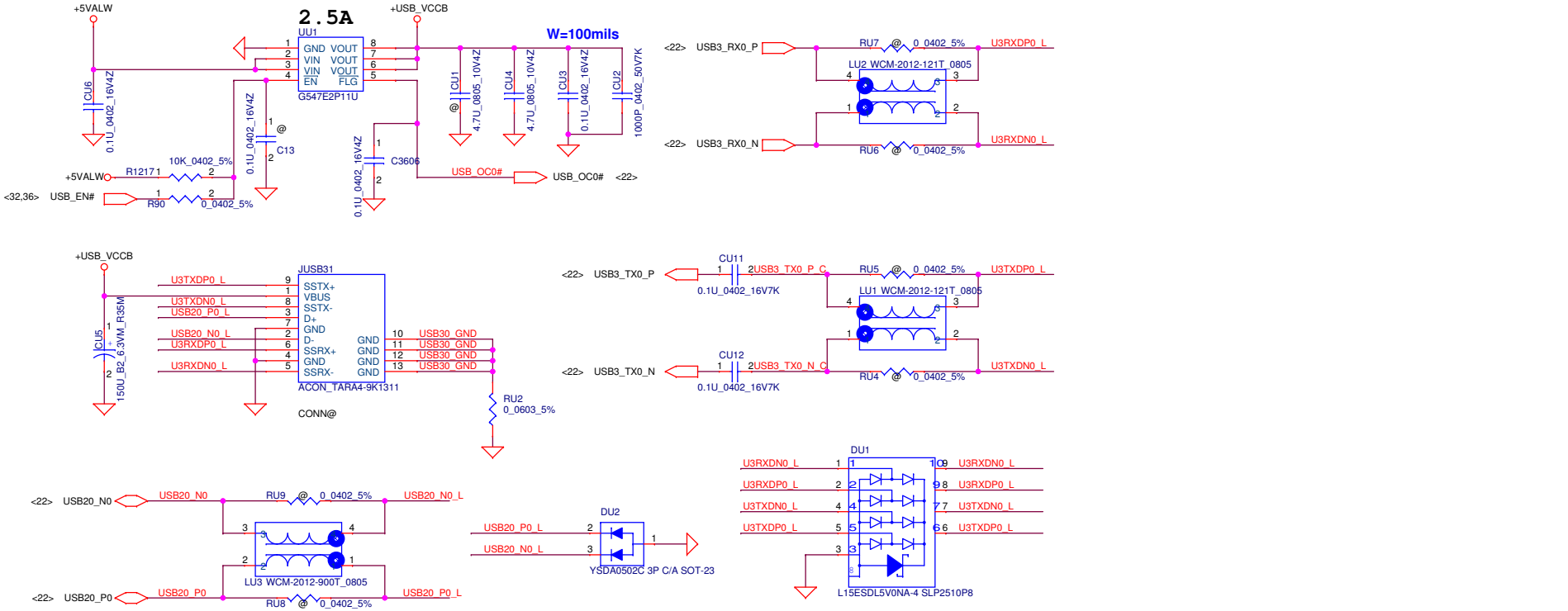
Size: D | Document Number: VBL30/31 LA-9351P M/B | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 32 of 50

Card Reader



USB3.0 Port



Security Classification	Compal Secret Data		
Issued Date	2012/06/01	Deciphered Date	2013/05/12

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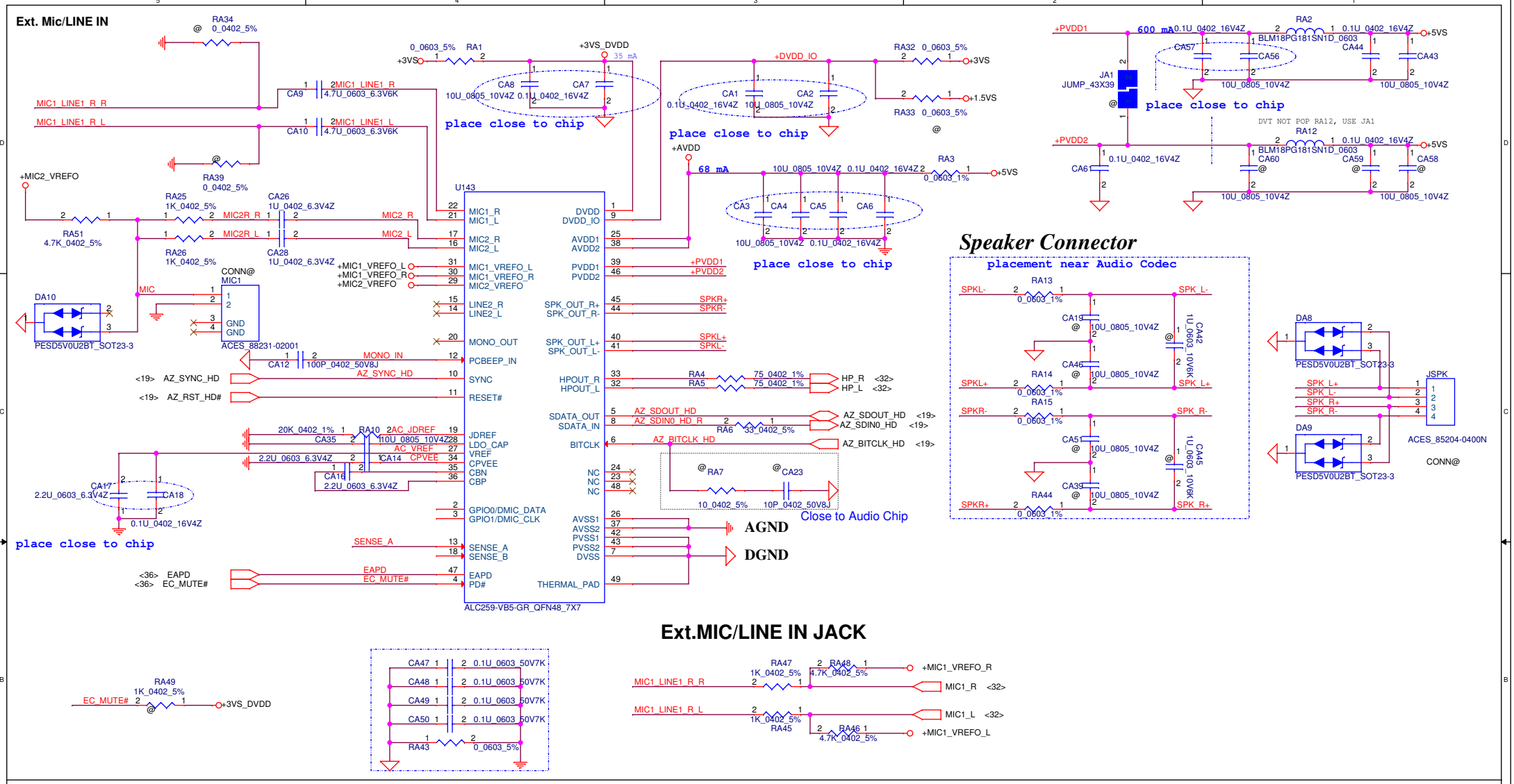
Compal Electronics, Inc.

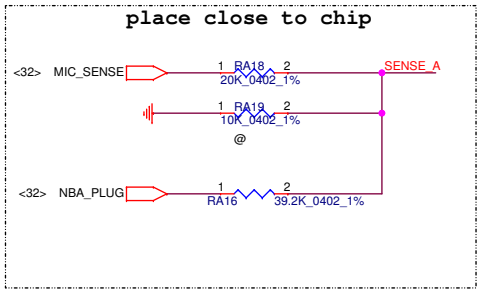
Title: USB-Card Reader-RTS5129

Size | Document Number: VBL30/31 LA-9351P M/B | Rev: 0.1

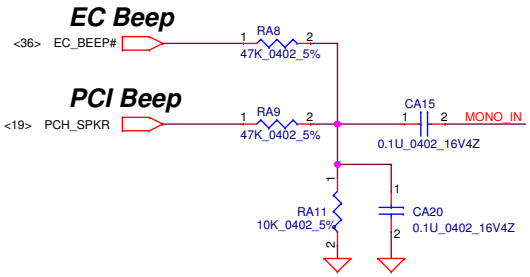
Date: Monday, July 16, 2012 | Sheet 33 of 50



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out



Beep sound



Security Classification	Compal Secret Data		
Issued Date	2012/06/01	Deciphered Date	2013/05/12

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Compal Electronics, Inc.

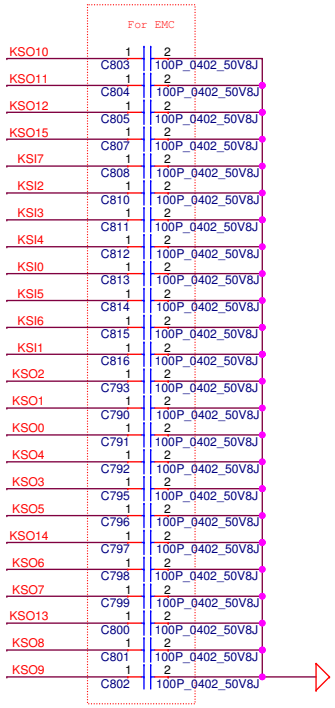
Title: HD CODEC ALC259

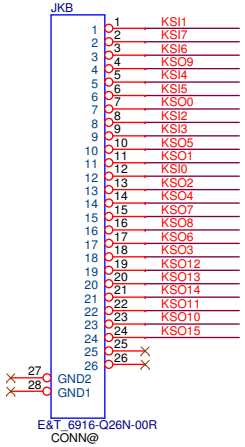
Document Number: VBL30/31 LA-9351P M/B

Rev: 0.1

Date: Monday, July 16, 2012

KEYBOARD CONN.



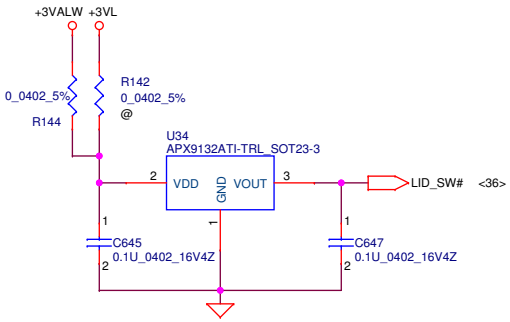


13.3" and 14"

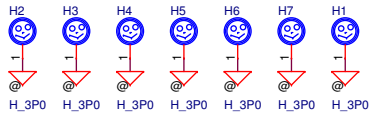
KSI[0..7] — KSI[0..7] <36>

KSO[0..15] — KSO[0..15] <36>

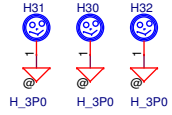
Lid SW



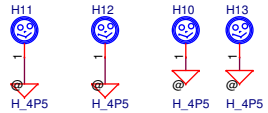
Screw Hole



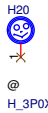
Break hole



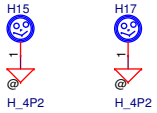
CPU



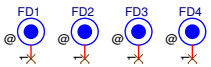
JWLAN

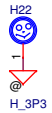


VGA



PCB Fedical Mark PAD





Security Classification	Compal Secret Data		
Issued Date	2012/06/01	Deciphered Date	2013/05/12

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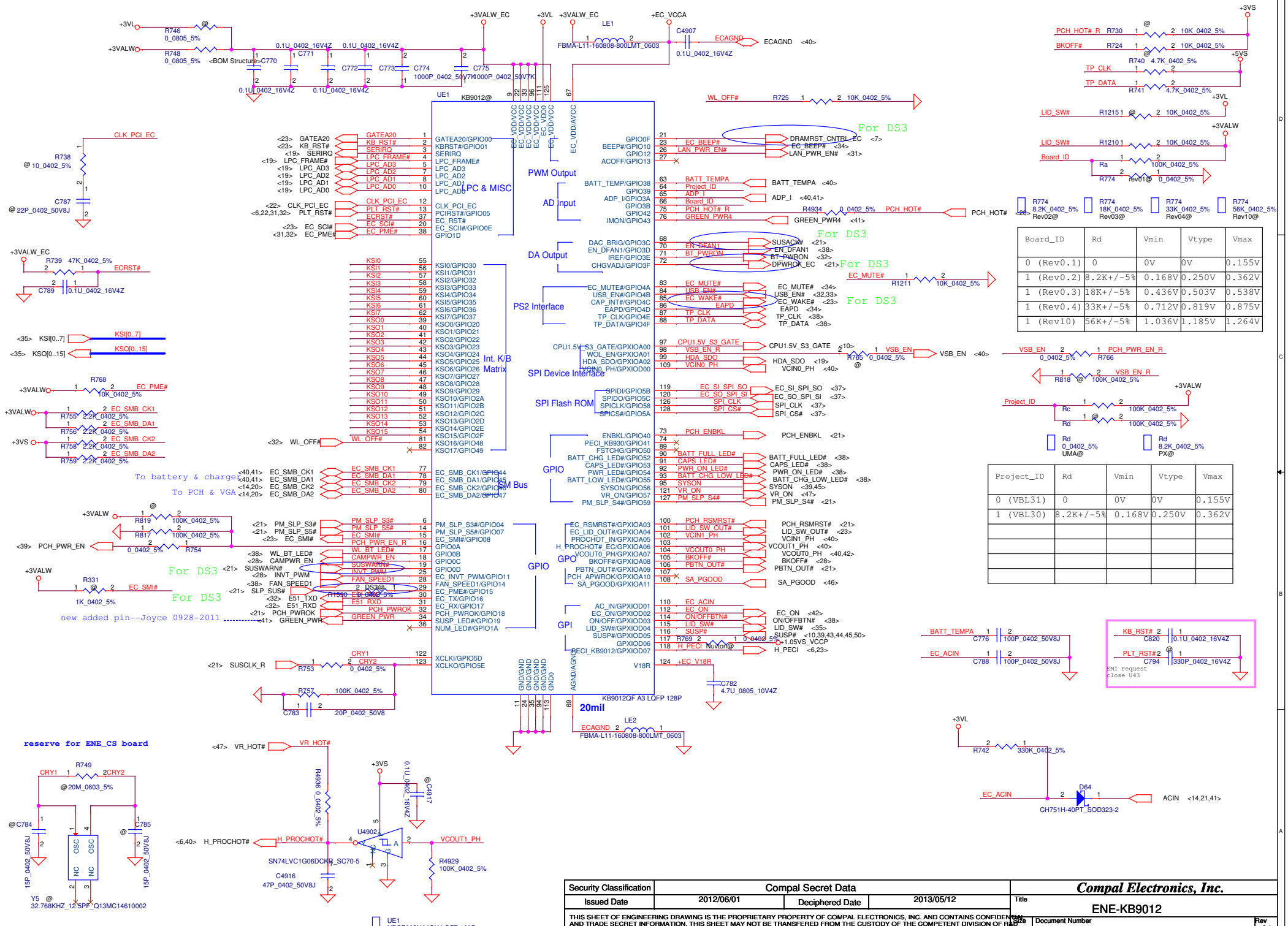
Compal Electronics, Inc.

Title: KB/PAD/ISPD/LID/ECROM

Size: D | Document Number: VBL30/31 LA-9351P M/B | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 35 of 50



Board_ID	Rd	Vmin	Vtype	Vmax
0 (Rev0.1)	0	0V	0V	0.155V
1 (Rev0.2)	8.2K+/-5%	0.168V	0.250V	0.362V
1 (Rev0.3)	18K+/-5%	0.436V	0.503V	0.538V
1 (Rev0.4)	33K+/-5%	0.712V	0.819V	0.875V
1 (Rev10)	56K+/-5%	1.036V	1.185V	1.264V

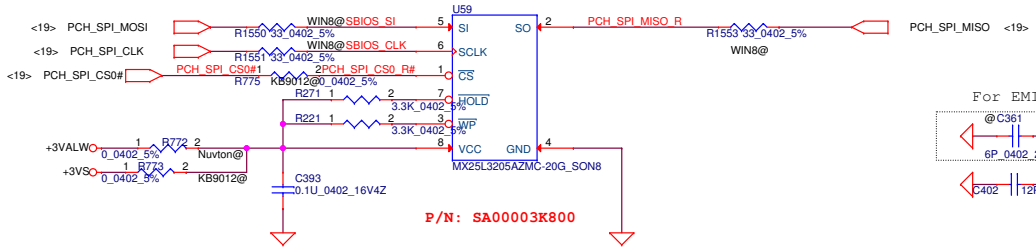
Project_ID	Rd	Vmin	Vtype	Vmax
0 (VBL31)	0	0V	0V	0.155V
1 (VBL30)	8.2K+/-5%	0.168V	0.250V	0.362V

BIOS Bus switch

R1550 0_0402_5% NOW8@ R1551 0_0402_5% NOW8@ R1553 0_0402_5% NOW8@

When use single ROM, R1550 R1551 R1553use 0 ohm.

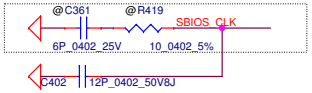
BIOS SPI Flash (4MByte*1)



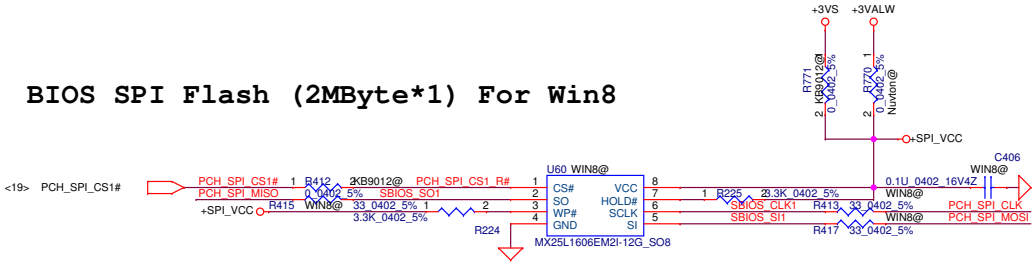
P/N: SA00003K800

R412 33_0402_5% Nuvton@ R775 33_0402_5% Nuvton@

For EMI resuest.

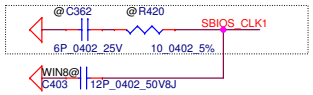


BIOS SPI Flash (2MByte*1) For Win8



P/N: SA000041N00

For EMI resuest.



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/06/01	Deciphered Date	2013/05/12	Title: SBIOS & EC ROM
				Size / Document Number: VBL30/31 LA-9351P M/B — Rev 0.1
				Date: Monday, July 16, 2012 — Sheet 37 of 50

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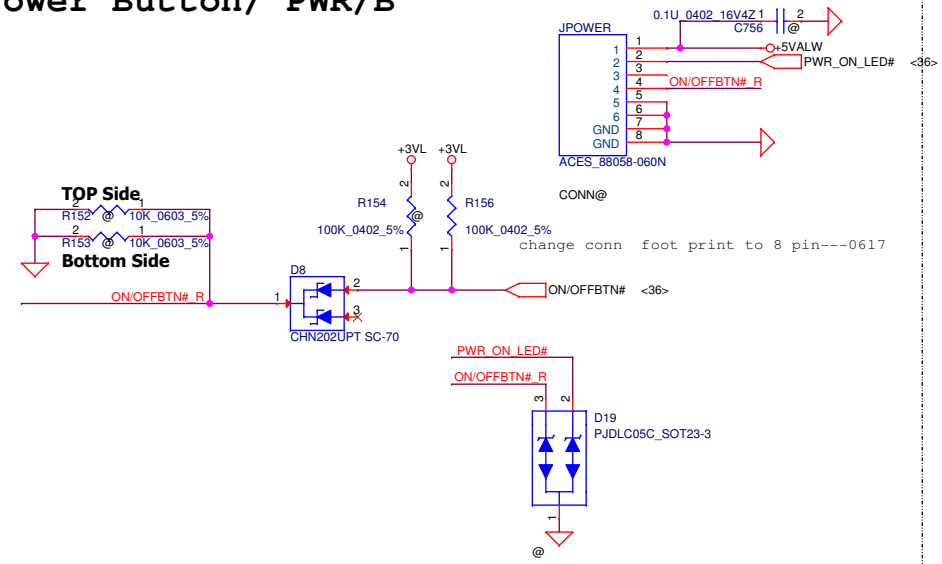
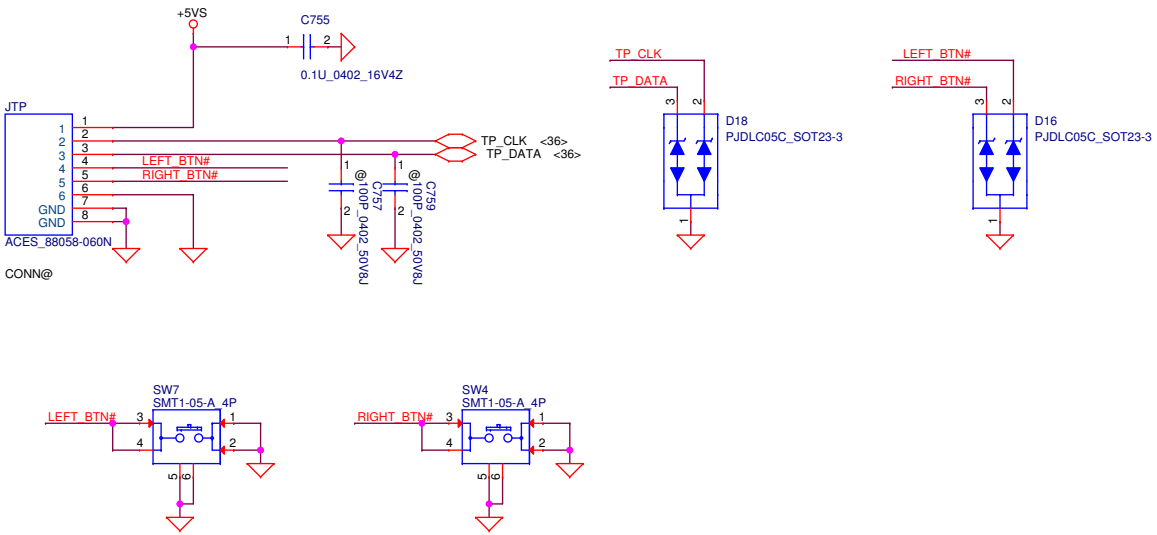
Power Button/ PWR/B

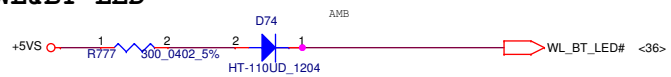


Touch/B Connector

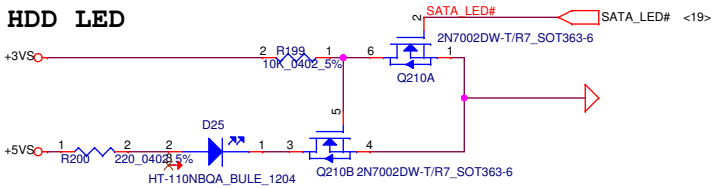


DC-IN LED

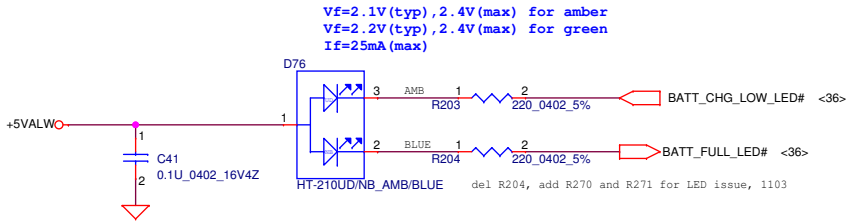
WL&BT LED



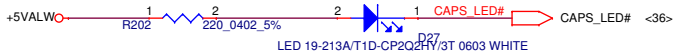
HDD LED



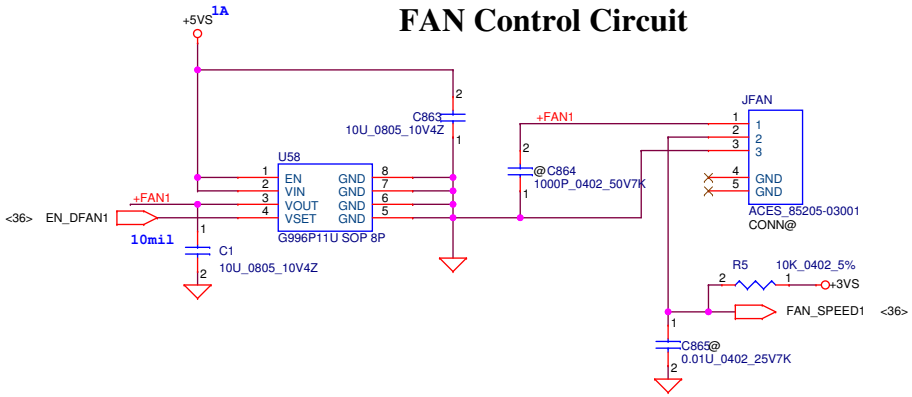
BATT CHARGE/FULL LED



CAP LOCK LED



FAN Control Circuit



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Issued Date	2012/06/01	Deciphered Date	2013/05/12

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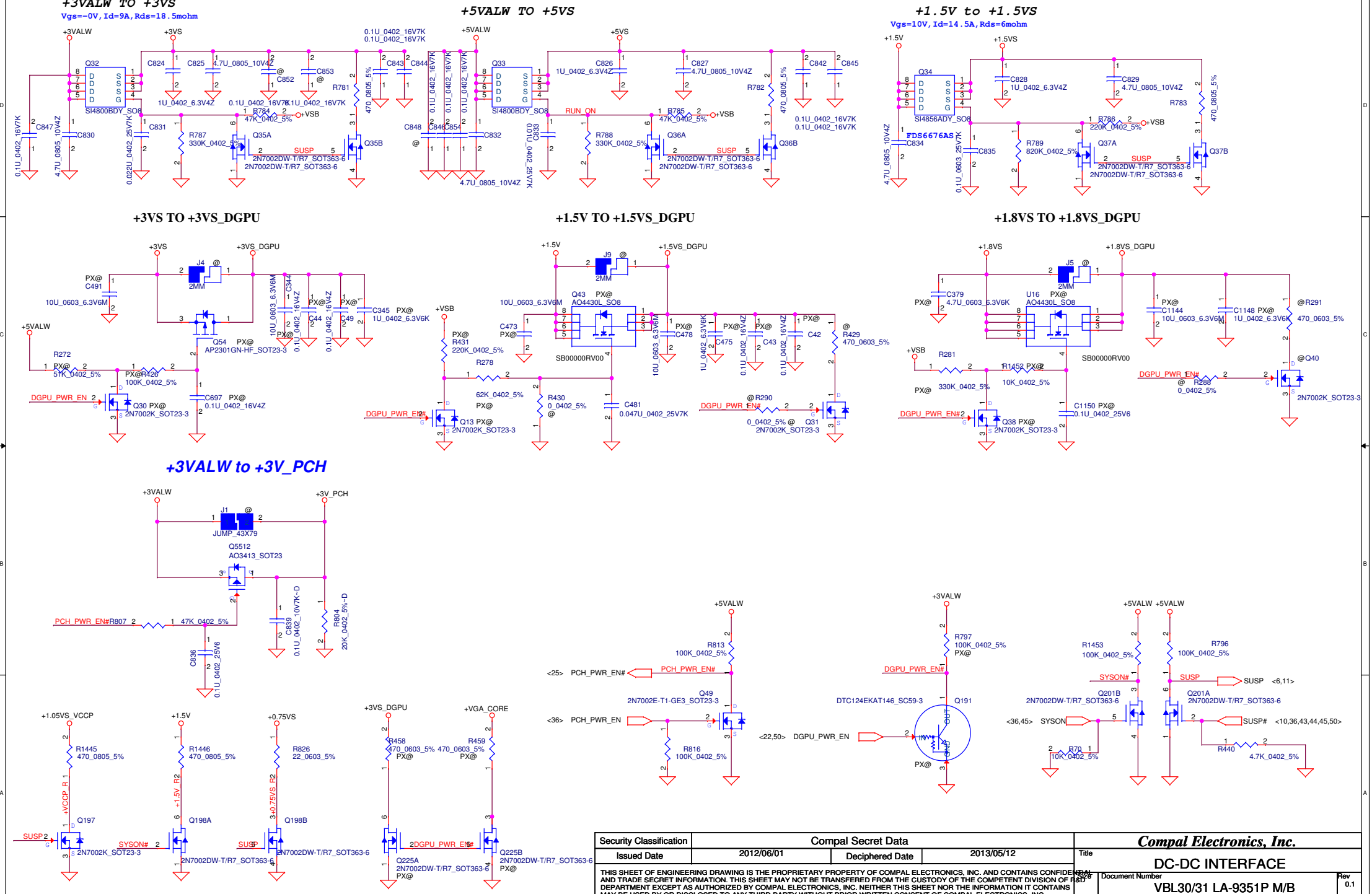
Compal Electronics, Inc.

Title: PWR/TP/LED/FAN

Size: B | Document Number: VBL30/31 LA-9351P M/B | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 38 of 50



Security Classification	Compal Secret Data		
Issued Date	2012/06/01	Deciphered Date	2013/05/12

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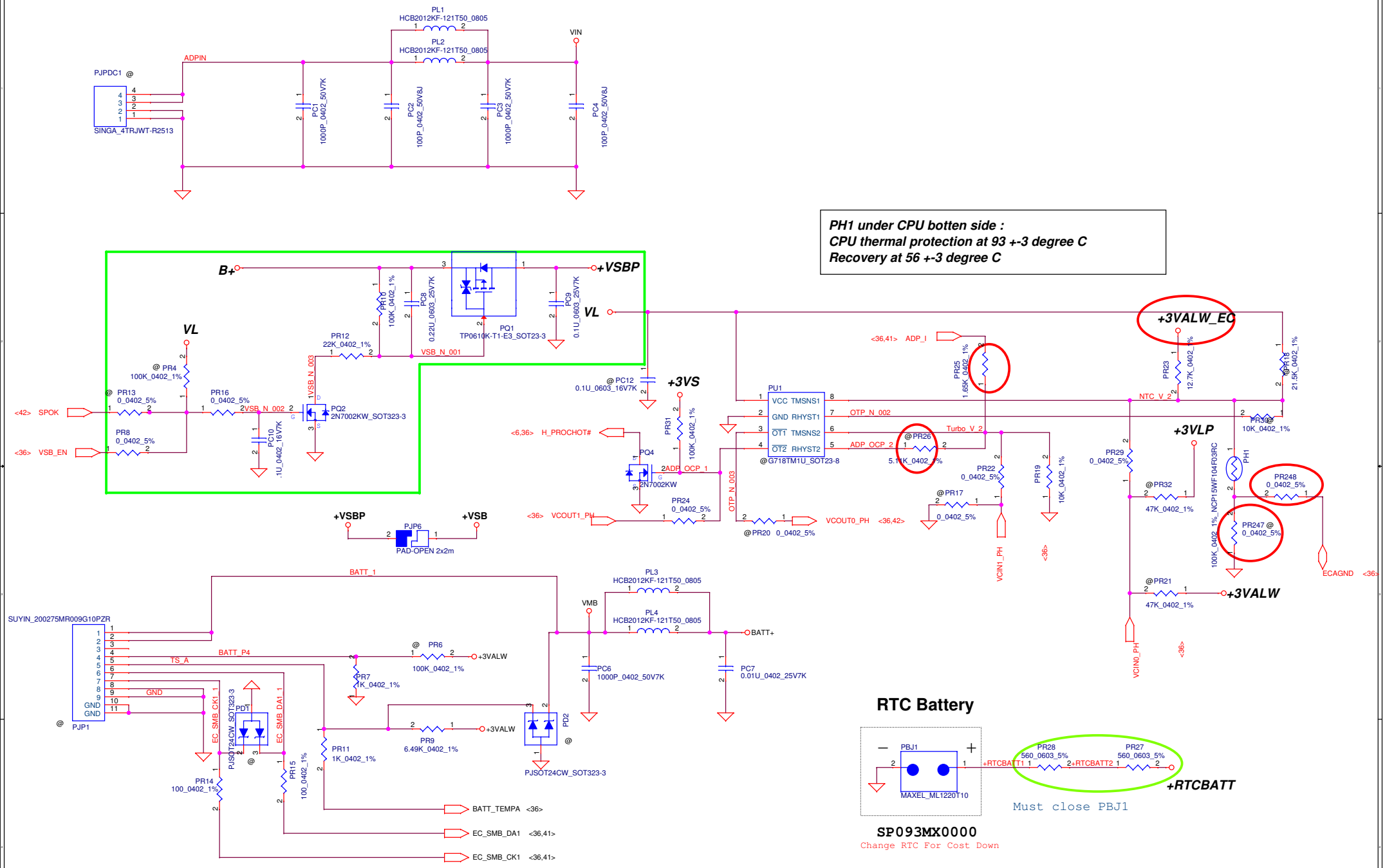
Compal Electronics, Inc.

Title: DC-DC INTERFACE

Size | Document Number: VBL30/31 LA-9351P M/B | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 39 of 50



Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2012/12/31

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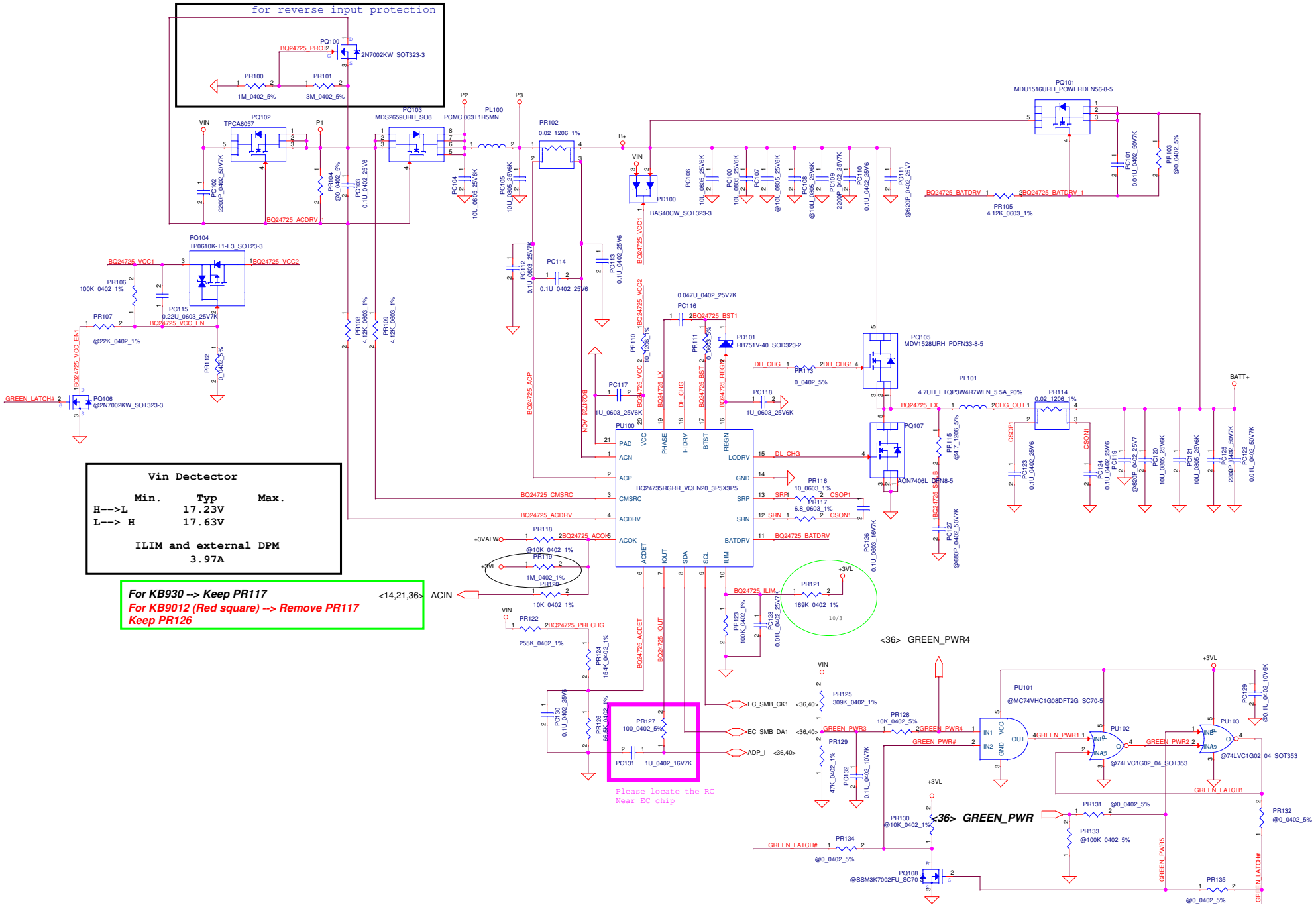
Compal Electronics, Inc.

Title: **PWR-DCIN / BATT CONN / OTP**

Size | Document Number: *VBL30/31* | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 40 of 50



Vin Dectector

	Min.	Typ	Max.
H-->L		17.23V	
L--> H		17.63V	

ILIM and external DPM
3.97A

For KB930 --> Keep PR117
For KB9012 (Red square) --> Remove PR117
Keep PR126

Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2012/12/31

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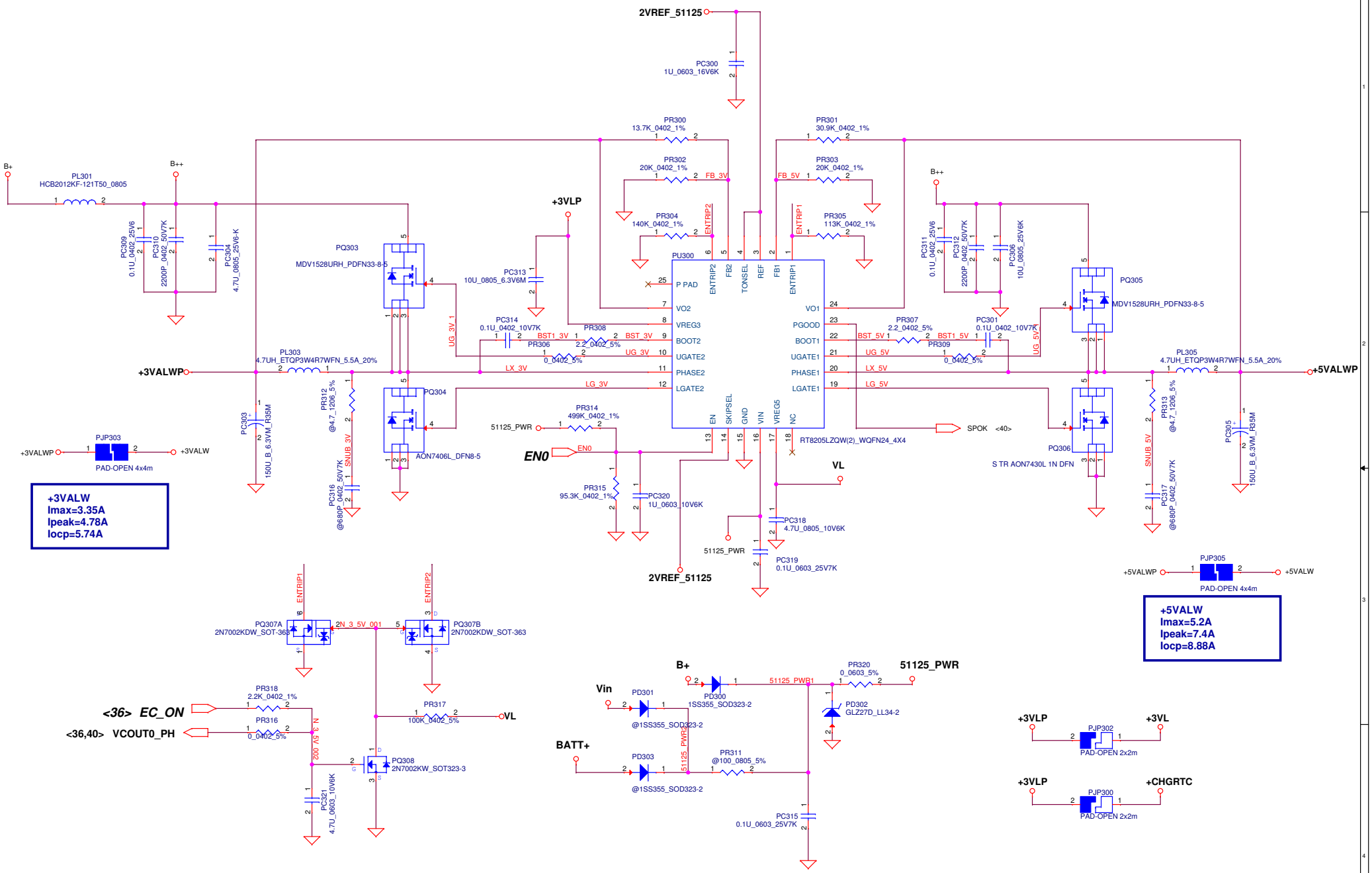
Compal Electronics, Inc.

Title: **PWR-CHARGER**

Document Number: *VBL30/31* | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 41 of 50



Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2012/12/31

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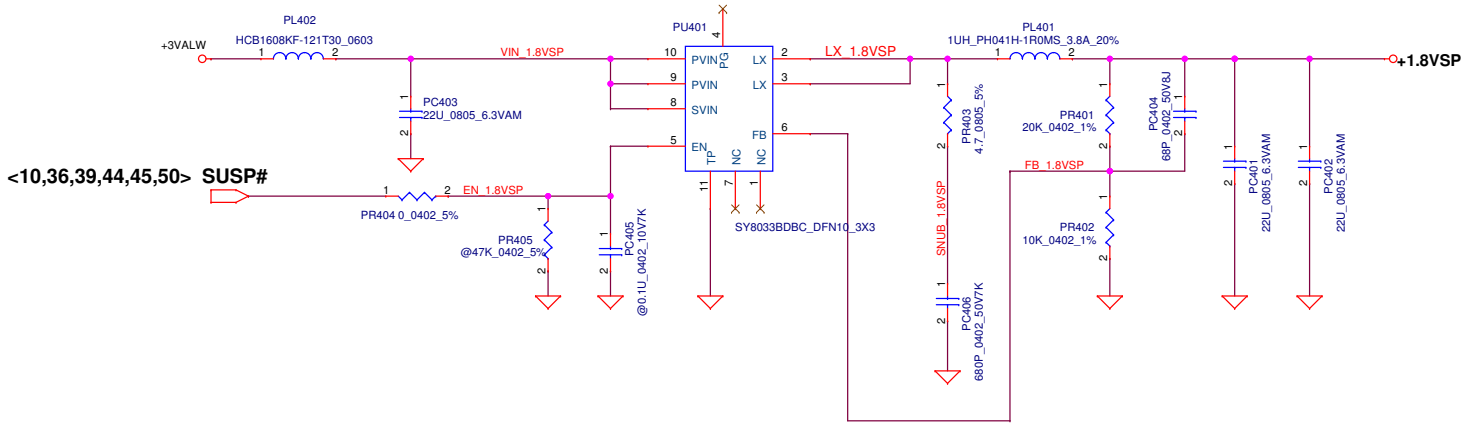
Compal Electronics, Inc.

Title: **PWR-3.3VALWP/5VALWP**

Size: Custom | Document Number: VBL30/31 | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 42 of 50



(3.5A,140mils ,Via NO.= 7)

+1.8V
Imax=2.25A
Ipeak=3.22A

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2009/01/23	Deciphered Date	2012/12/31	Title: PWR-1.8VSP
				Document Number: VBL30/31 — Rev: 0.1
				Date: Monday, July 16, 2012 — Sheet 43 of 50

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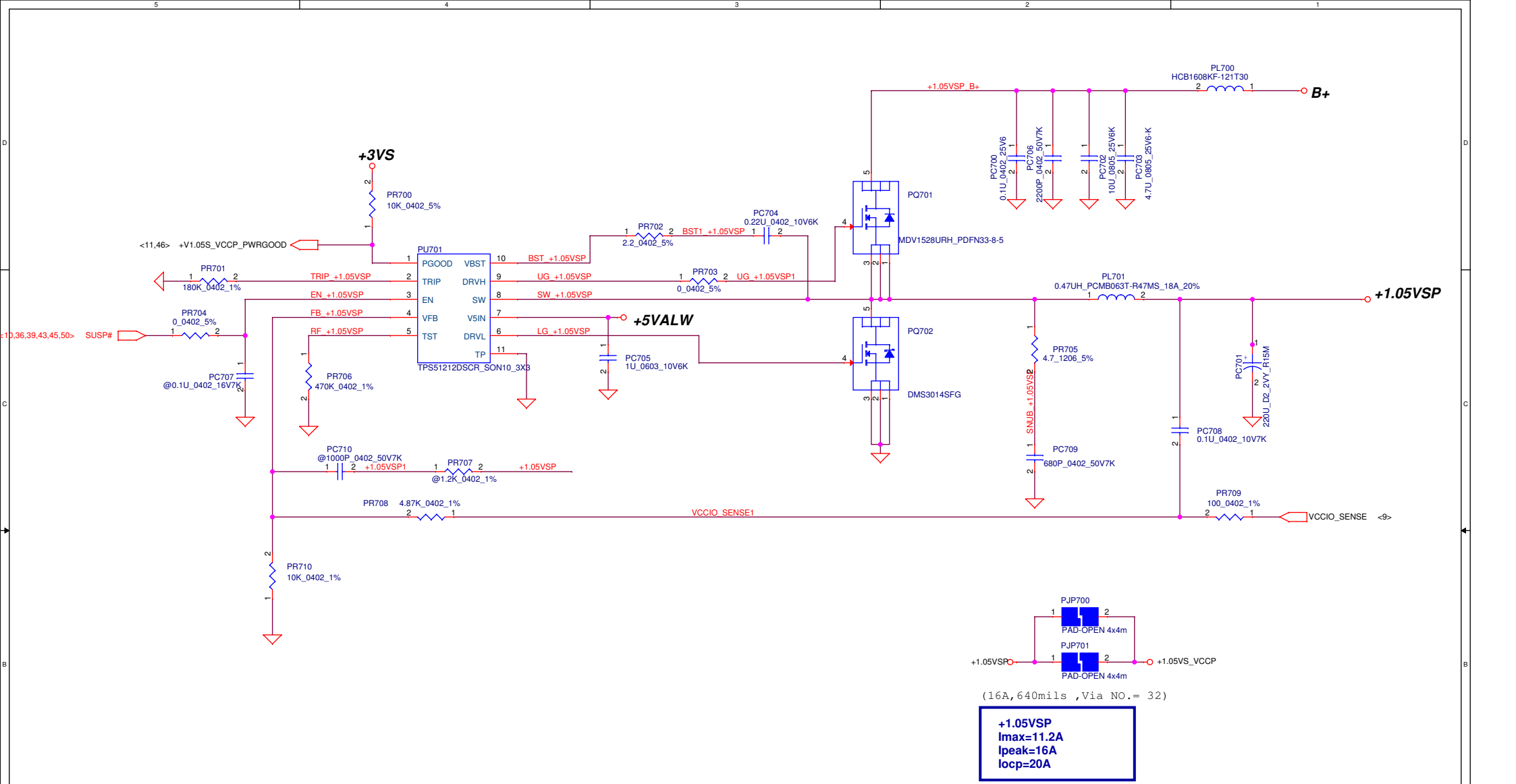

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2012/12/31

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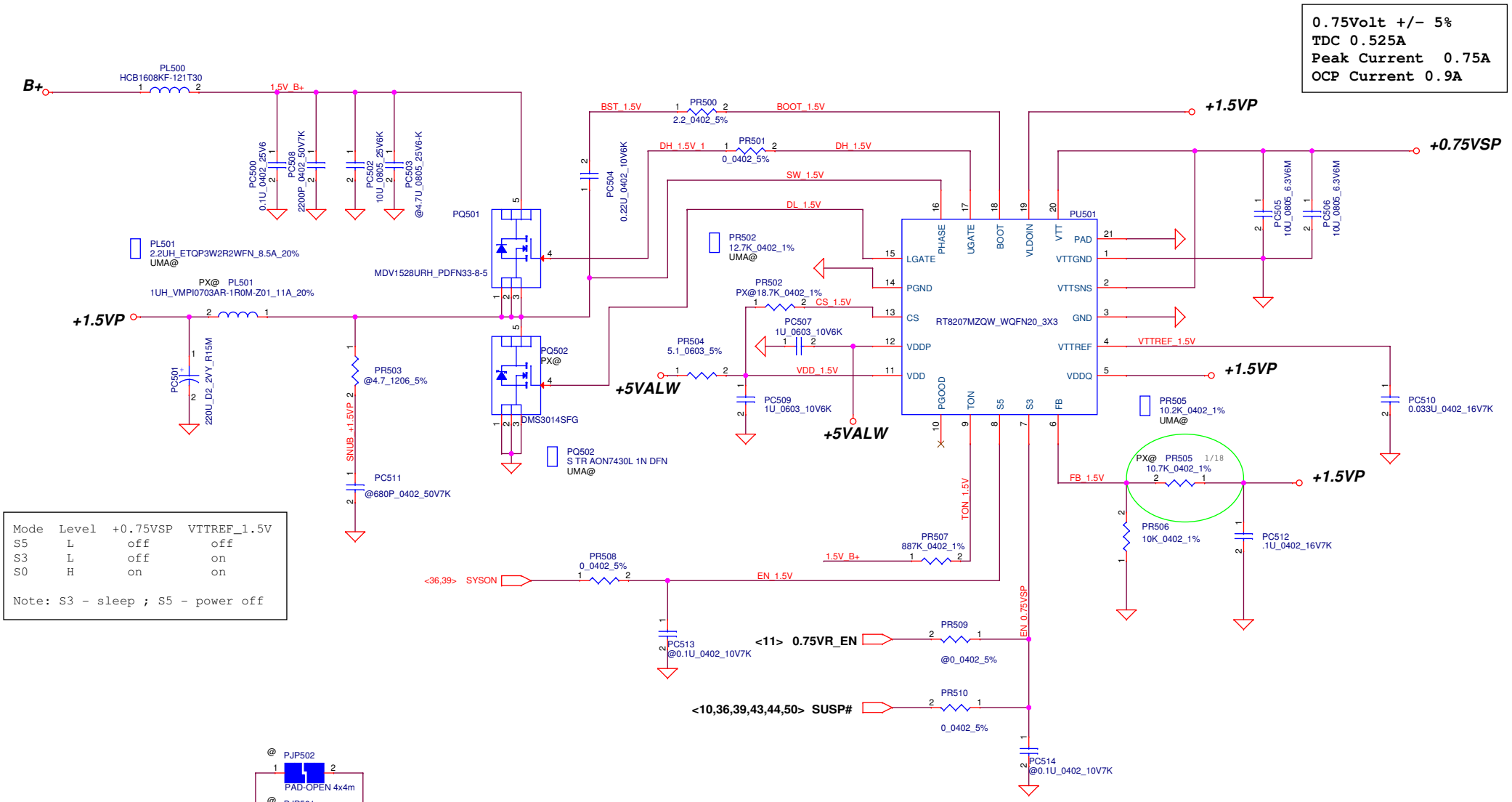
Compal Electronics, Inc.

Title: **PWR-+V1.05S_VCCP**

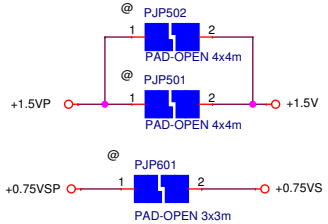
Size: Custom | Document Number: VBL30/31 | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 44 of 50



Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off



(13A,520mils ,Via NO.= 26)

(2A,80mils ,Via NO.= 4)

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Issued Date	2010/07/20	Deciphered Date	2012/12/31

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Compal Electronics, Inc.

Title: **PWR-1.5VP / +0.75VSP**

Size: Custom | Document Number: VBL30/31 | Rev: 0.1

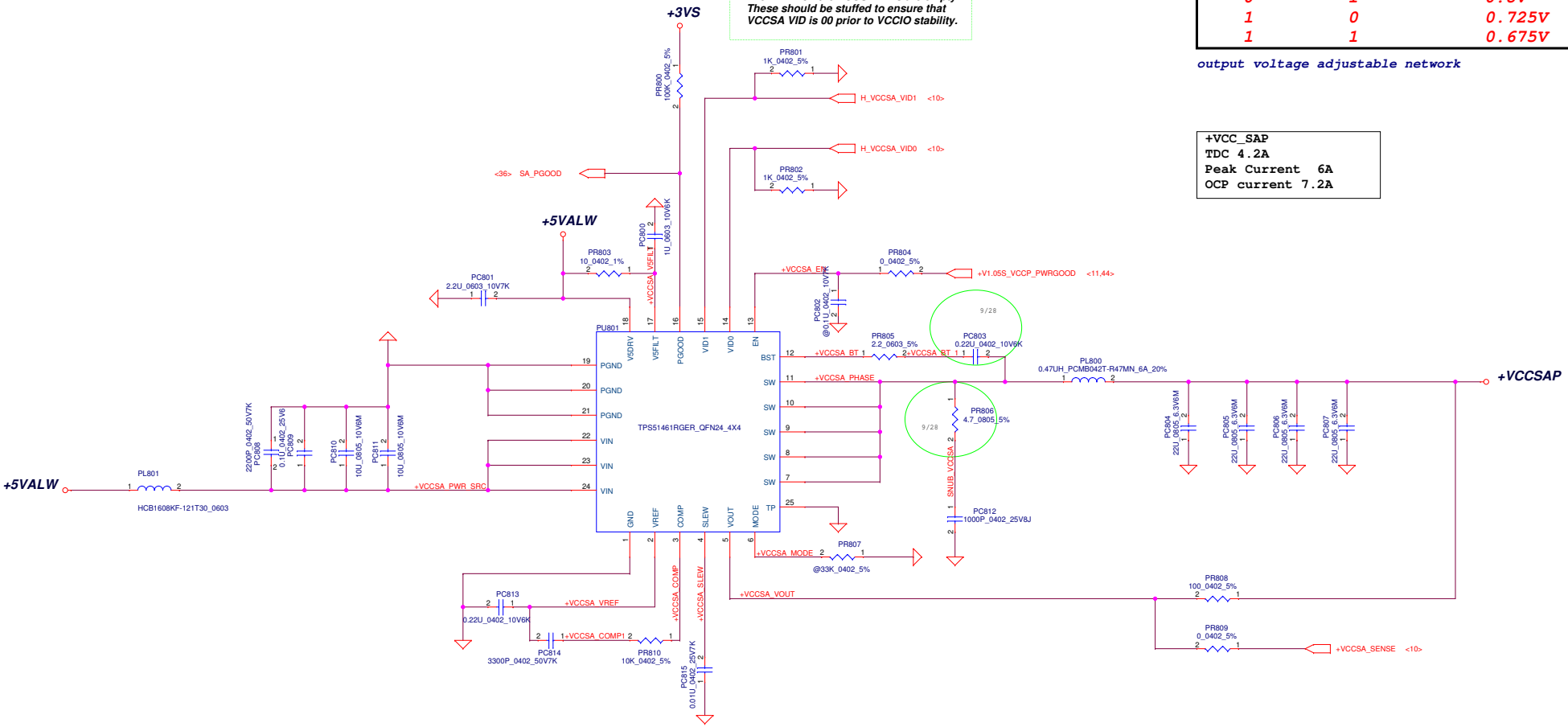
Date: Monday, July 16, 2012 | Sheet 45 of 50

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



(6A,240mils ,Via NO.= 12)

+VCCSA
Imax=4.2A
Ipeak=6A
Iocp=7.2

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Issued Date	2010/07/20	Deciphered Date	2012/12/31

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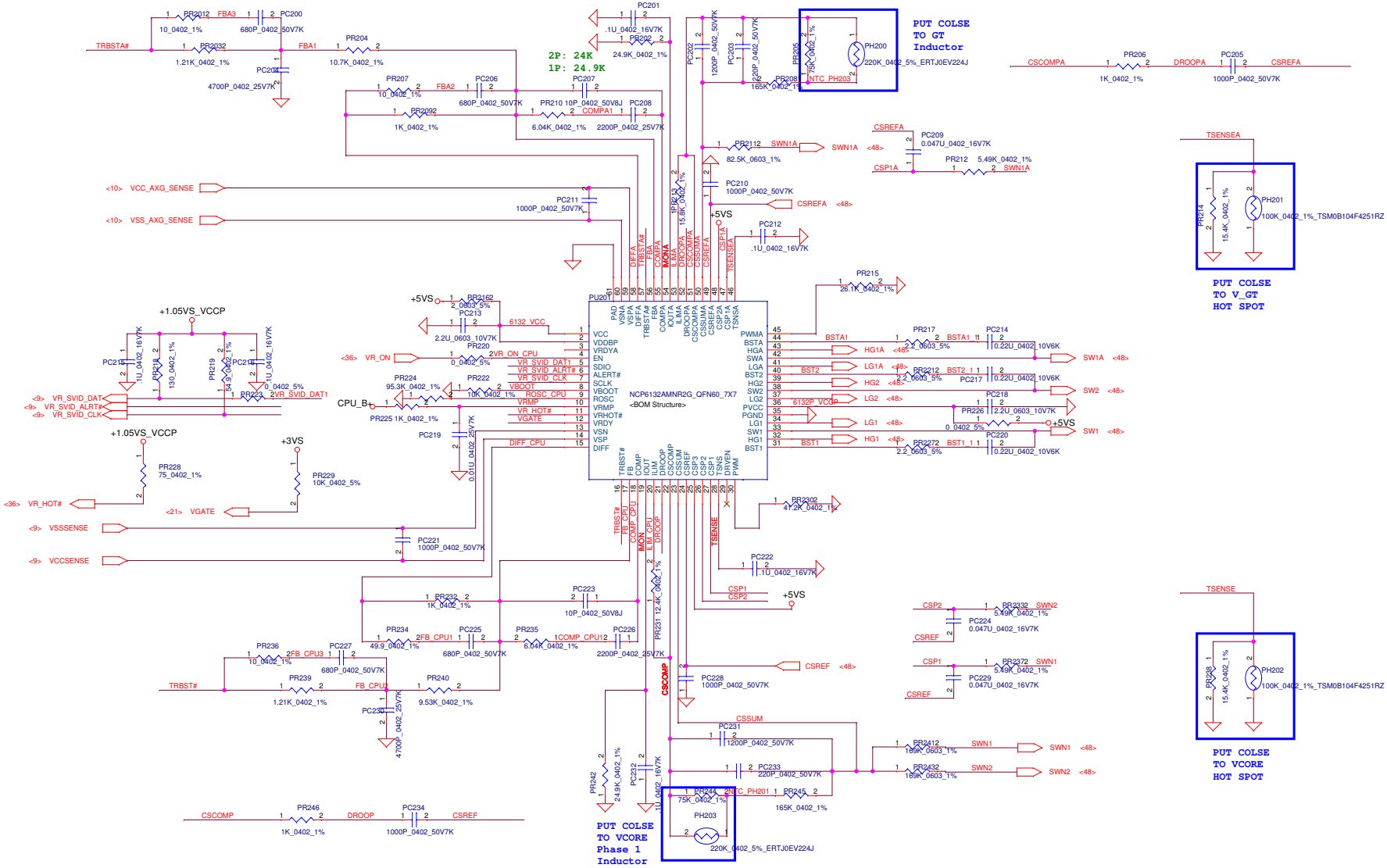
Compal Electronics, Inc.

Title: **PWR-VCC_SAP**

Size: C | Document Number: VBL30/31 | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 46 of 50



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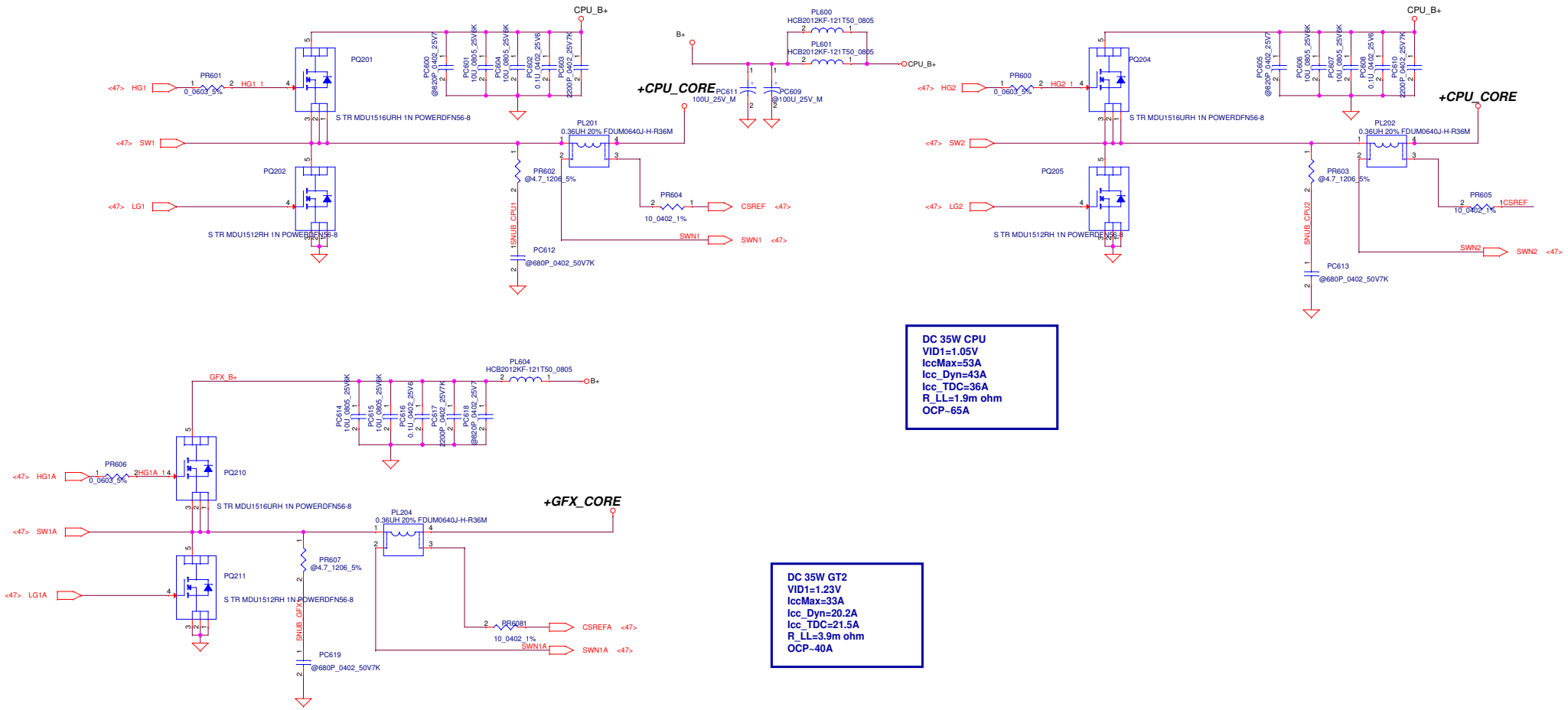
Compal Electronics, Inc.

Title: **PWR-CPU_CORE**

Size: C | Document Number: VBL30/31 | Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 47 of 50



DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP~65A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~40A

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Issued Date	2011/10/31	Deciphered Date	2012/12/31

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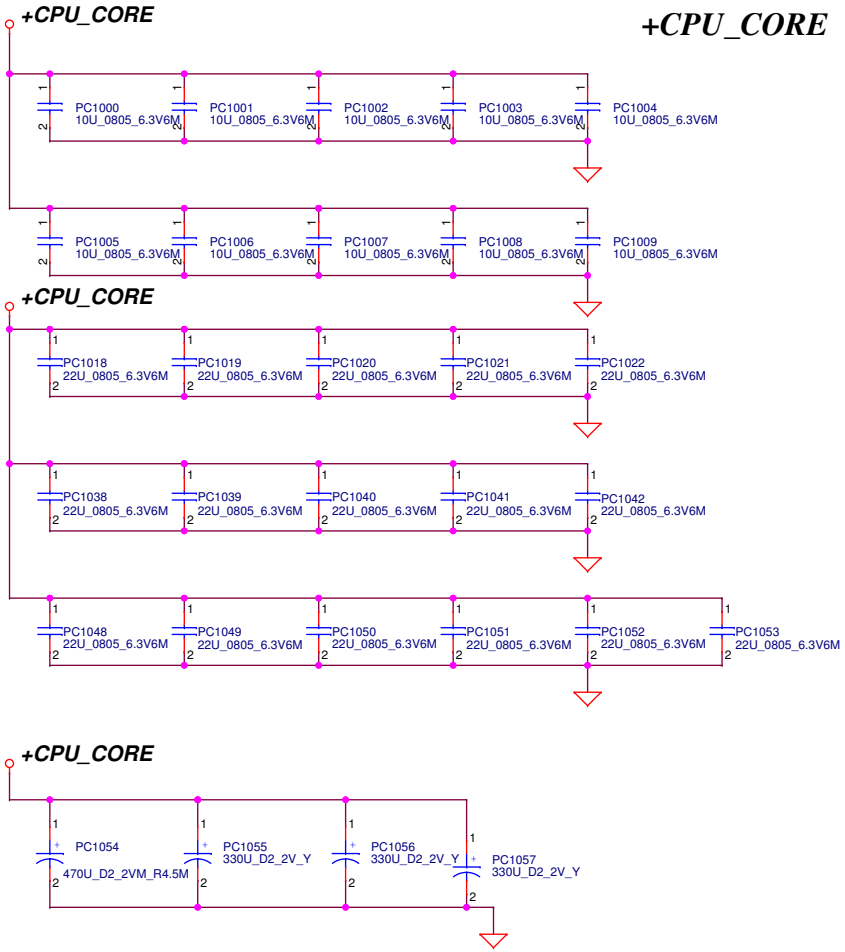
Title: ***PWR-VCC_CORE***

Document Number: VBL30/31

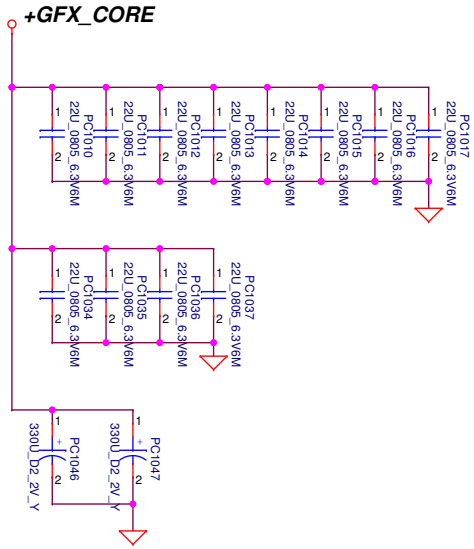
Rev: 0.1

Date: Monday, July 16, 2012 | Sheet 48 of 50



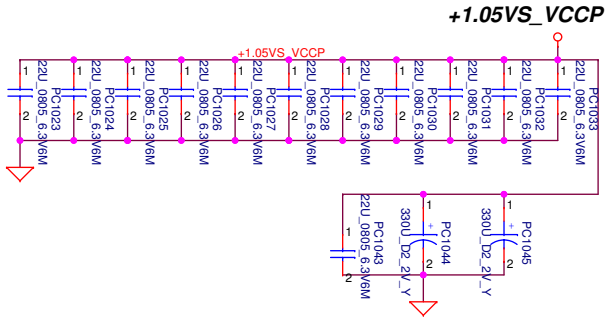
+CPU_CORE

+GFX_CORE



Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



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Compal Electronics, Inc.

Title: **PWR - PROCESSOR DECOUPLING**

Size: B | Document Number: VBL30/31 | Rev: 0.1

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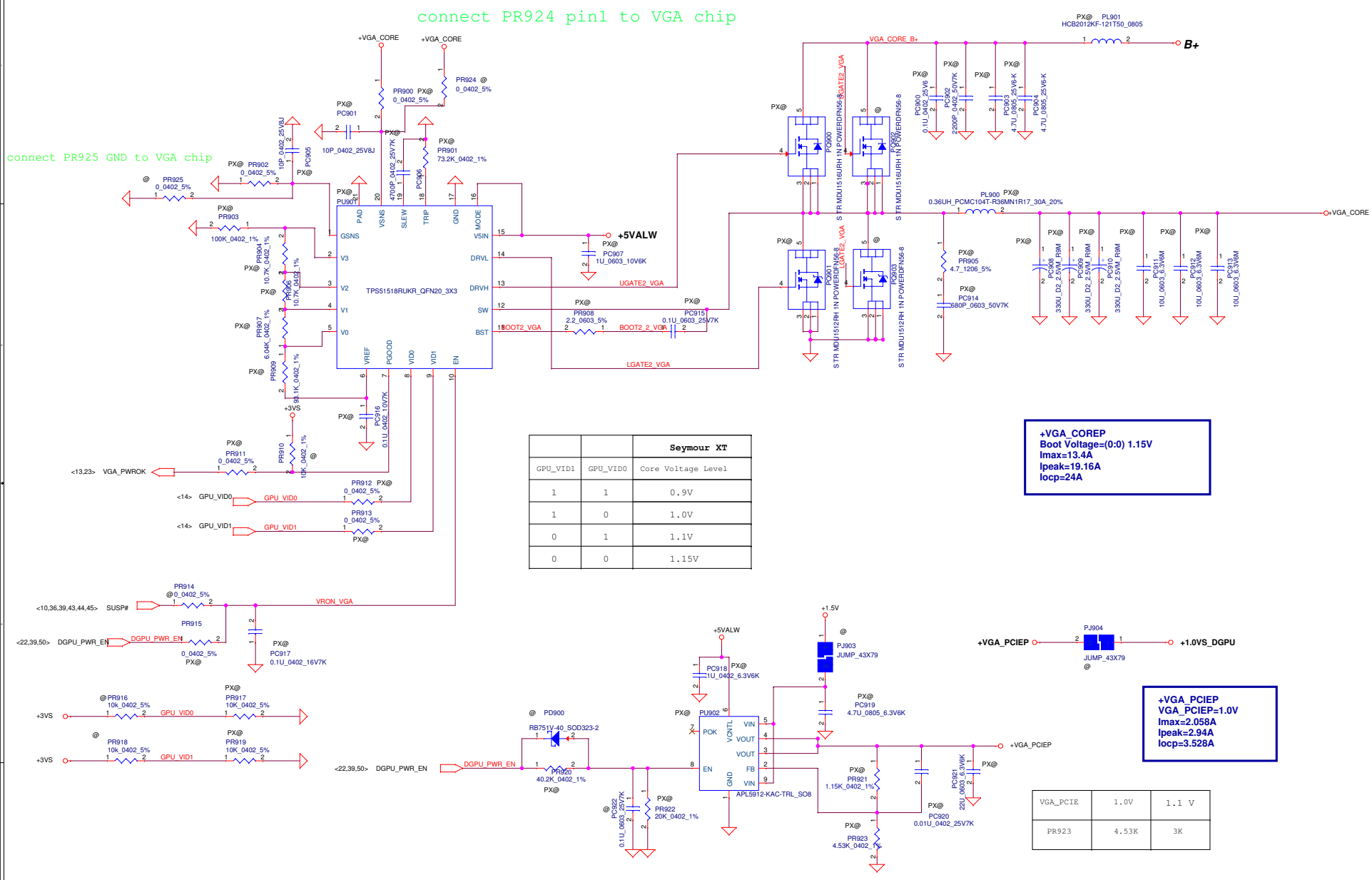

		Seymour XT
GPU_VID1	GPU_VID0	Core Voltage Level
1	1	0.9V
1	0	1.0V
0	1	1.1V
0	0	1.15V

VGA_PCIE	1.0V	1.1 V
PR923	4.53K	3K

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

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Title: **PWR-VGA_CORE/VGA_PCIE**

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