Compal Confidential

Model Name : VIUS3/S4
File Name : LA-8951PR01
BOM P/N:43

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VIUS3/S4 M/B Schematics Document

Intel Ivy Bridge ULV Processor + Panther Point PCH
AMD Seymour XT

2011-12-28

REV:0.1

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title: Cover Page
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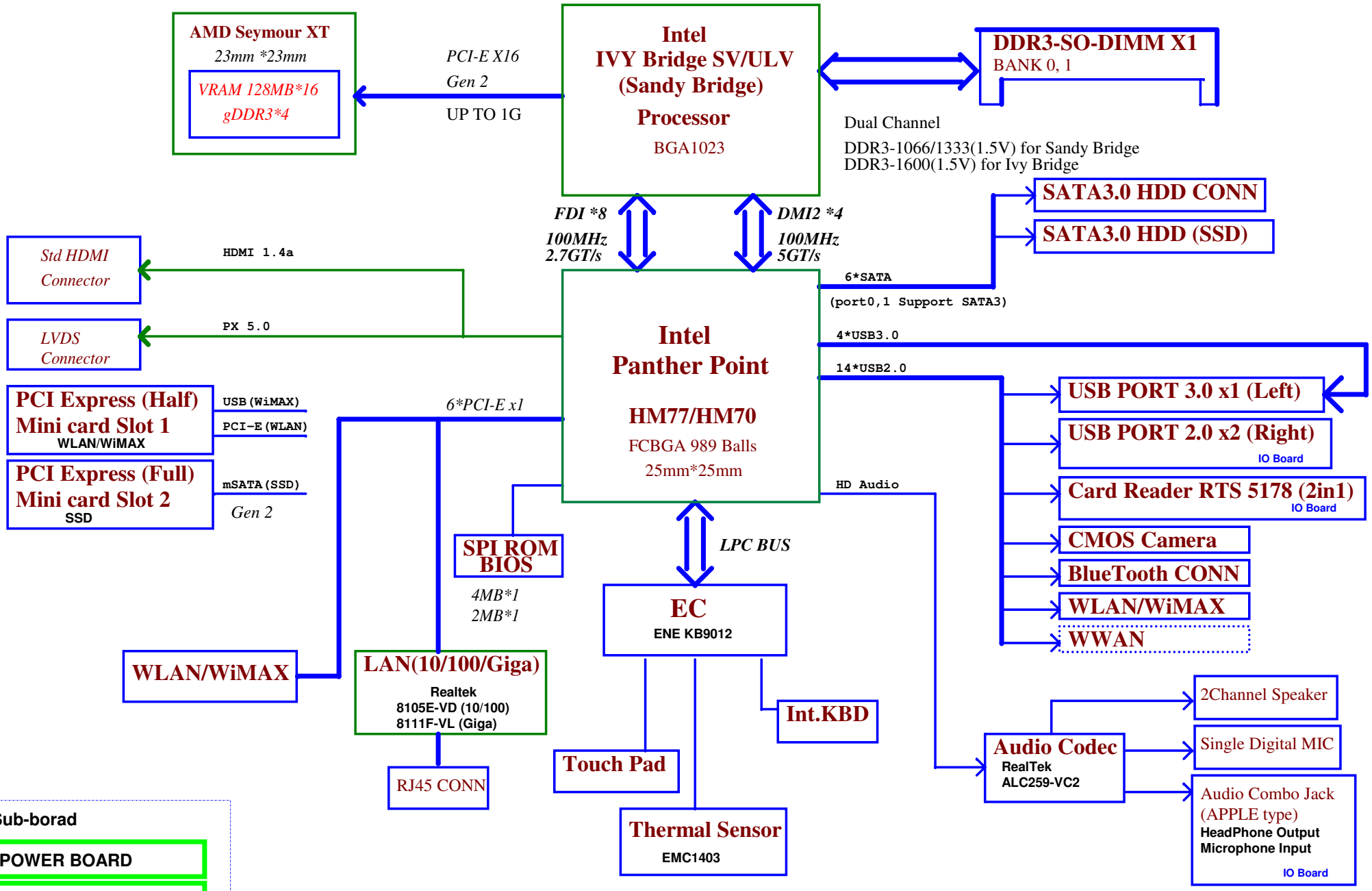
				Date: Thursday, February 02, 2012; Sheet 1 of 55

Compal confidential
File Name :VIUS3/VIUS4

Chief River



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/07/21	Deciphered Date 2012/12/31	Title: MB Block Diagram
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			Date: Thursday, February 02, 2012 / Sheet 2 of 55

Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V +1.5V_IO	+5VS +3VS +1.5VS +1.05VS_VTT +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Porject	Phase
0	0	0 V	0 V	0 V	G-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	G-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	G-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	G-series	EVT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	Y-series	EVT
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	Y-series	DVT
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	Y-series	PVT
7	NC	2.500 V	3.300 V	3.300 V	Y-series	MP

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor F75303M	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

AMD-GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

USB Port Table

USB 3.0	USB 2.0		Port	3 External USB Port
xHCI1	EHCI1	UHCI0	0	
xHCI2			1	USB 3.0 Port (Left Side)
xHCI3		UHCI1	2	Mini Card(WLAN)
xHCI4			3	
		UHCI2	4	X (USB PORT disabled on HM70)
			5	X (USB PORT disabled on HM70)
		UHCI3	6	X (USB PORT disabled on HM70)
			7	X (USB PORT disabled on HM70)
	EHCI2	UHCI4	8	USB/B (Right Side USB-BD)
			9	USB/B (Right Side USB-BD)
		UHCI5	10	USB Port (Right Side CR-BD)
			11	Camera (LVDS)
		UHCI6	12	X (USB PORT disabled on HM70)
			13	X (USB PORT disabled on HM70)

HM70 Disable xHCI3,xHCI4

BOM Structure Table

BTO Item	BOM Structure
INTEL UMA only	UMA@
GPU:Seymour XT	PX@ PX5@
HDMI	HDMI@
HDD1 (HM77 SATA 3.0)	HDD1@
HDD2 (HM70 SATA 2.0)	HDD2@
Interna-Intel-USB3.0	IU3@
Interna-Intel-USB2.0	IU2@
Blue Tooth	BT@
10/100 LAN	8105E@
GIGA LAN	8111F@
Connector	ME@
45 LEVEL	45@
Unpop	@

SATA Port Table

	HM77	HM70	
SATA P0	GEN3/2/1	GEN3/2/1	SSD
SATA P1	GEN3/2/1	Disable	HDD (HM77)
SATA P2	GEN2/1	GEN2/1	HDD (HM70)
SATA P3	GEN2/1	Disable	
SATA P4	GEN2/1	GEN2/1	
SATA P5	GEN2/1	GEN2/1	

HM70 Disable P1,P3

PCIe Port Table

	HM77	HM70	
PCIe P1	Enable	Enable	LAN
PCIe P2	Enable	Enable	WLAN
PCIe P3	Enable	Enable	
PCIe P4	Enable	Enable	
PCIe P5	Enable	Disable	
PCIe P6	Enable	Disable	
PCIe P7	Enable	Disable	
PCIe P8	Enable	Disable	

HM70 Disable P5,P6,P7,P8

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

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			Size B; Document Number LA-7981P; Rev 0.2
			Date: Friday, February 03, 2012; Sheet 3 of 55

Power-Up/Down Sequence

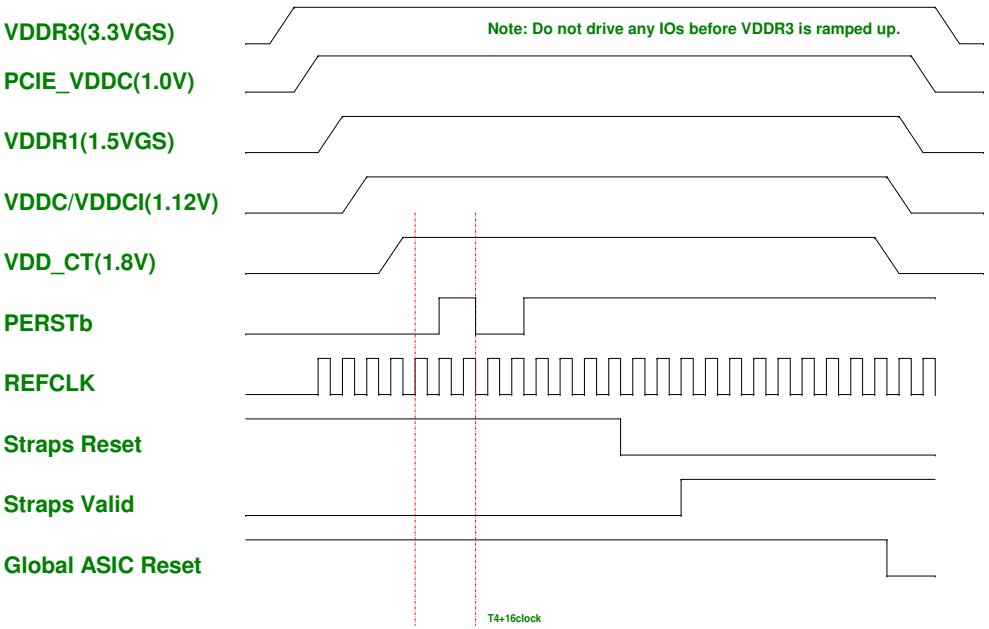
1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

2. VDDR3 should ramp-up before or simultaneously with VDDC.

3. For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

5.VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)



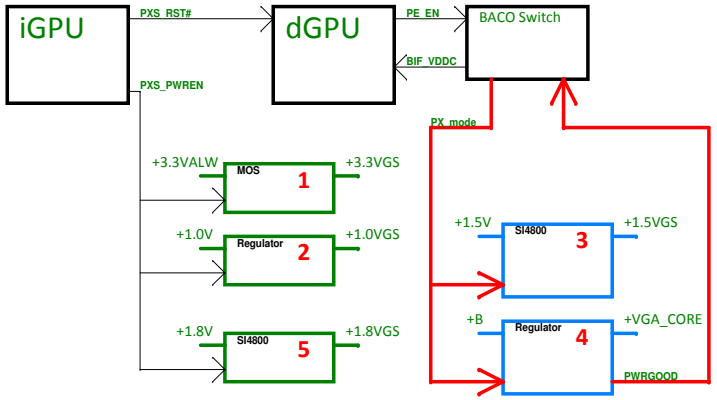
Without BACO option :

PXS_RST# : Low -> Reset dGPU ; High ->Normal operation
PXS_PWREN : Low -> dGPU Power OFF ; High -> dGPU Power ON

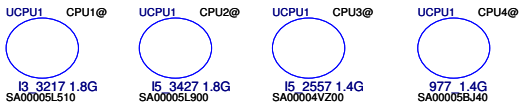
BACO option :

PXS_RST# : High ->Normal operation (dGPU is not reset on BACO mode)
PXS_PWREN : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

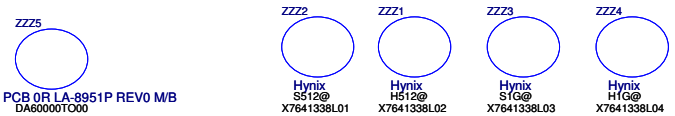
dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	~~1679mA~~
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode) BIF_VDDC=VGA_CORE When GPU enable BIF_VDDC=1.0V When BACO	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



CPU part



PCB part



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PEG_ICOMPI and RCOMPO signals should be shorted and routed
with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils
- typical impedance = 14.5 mohms

Layout placement: Place close to U8 (GPU)

+1.05VS_VTT

R249
24.9_0402_1%

W=12mil L=500mil S=15mil

PEG_COMP

UCPU1A

DMI

[15] DMI_CRX_PTX_N0	M2	DMI_RX#[0]	
[15] DMI_CRX_PTX_N1	P6	DMI_RX#[1]	
[15] DMI_CRX_PTX_N2	P1	DMI_RX#[2]	
[15] DMI_CRX_PTX_N3	P10	DMI_RX#[3]	
[15] DMI_CRX_PTX_P0	N3	DMI_RX[0]	
[15] DMI_CRX_PTX_P1	P7	DMI_RX[1]	
[15] DMI_CRX_PTX_P2	P3	DMI_RX[2]	
[15] DMI_CRX_PTX_P3	P11	DMI_RX[3]	
[15] DMI_CTX_PRX_N0	K1	DMI_TX#[0]	
[15] DMI_CTX_PRX_N1	M8	DMI_TX#[1]	
[15] DMI_CTX_PRX_N2	N4	DMI_TX#[2]	
[15] DMI_CTX_PRX_N3	R2	DMI_TX#[3]	
[15] DMI_CTX_PRX_P0	K3	DMI_TX[0]	
[15] DMI_CTX_PRX_P1	M7	DMI_TX[1]	
[15] DMI_CTX_PRX_P2	P4	DMI_TX[2]	
[15] DMI_CTX_PRX_P3	T3	DMI_TX[3]	

Intel(R) FDI

[15] FDI_CTX_PRX_N0	U7	FDI0_TX#[0]	
[15] FDI_CTX_PRX_N1	W11	FDI0_TX#[1]	
[15] FDI_CTX_PRX_N2	W1	FDI0_TX#[2]	
[15] FDI_CTX_PRX_N3	AA6	FDI0_TX#[3]	
[15] FDI_CTX_PRX_N4	W6	FDI1_TX#[0]	
[15] FDI_CTX_PRX_N5	V4	FDI1_TX#[1]	
[15] FDI_CTX_PRX_N6	Y2	FDI1_TX#[2]	
[15] FDI_CTX_PRX_N7	AC9	FDI1_TX#[3]	
[15] FDI_CTX_PRX_P0	U6	FDI0_TX[0]	
[15] FDI_CTX_PRX_P1	W10	FDI0_TX[1]	
[15] FDI_CTX_PRX_P2	W3	FDI0_TX[2]	
[15] FDI_CTX_PRX_P3	AA7	FDI0_TX[3]	
[15] FDI_CTX_PRX_P4	W7	FDI1_TX[0]	
[15] FDI_CTX_PRX_P5	T4	FDI1_TX[1]	
[15] FDI_CTX_PRX_P6	AA3	FDI1_TX[2]	
[15] FDI_CTX_PRX_P7	AC8	FDI1_TX[3]	
[15] FDI_FSYNC0	AA11	FDI0_FSYNC	
[15] FDI_FSYNC1	AC12	FDI1_FSYNC	
[15] FDI_INT	U11	FDI_INT	
[15] FDI_LSYNC0	AA10	FDI0_LSYNC	
[15] FDI_LSYNC1	AG8	FDI1_LSYNC	

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms
can't be left floating
,even if disable eDP function...

+1.05VS_VTT

R247
24.9_0402_1%

W=12mil L=500mil S=15mil

EDP_COMP

eDP

AF3	eDP_COMPIO	
AD2	eDP_ICOMPO	
AG11	eDP_HPD#	
AG4	eDP_AUX#	
AF4	eDP_AUX	
AC3	eDP_TX#[0]	
AC4	eDP_TX#[1]	
AE11	eDP_TX#[2]	
AE7	eDP_TX#[3]	
AC1	eDP_TX[0]	
AA4	eDP_TX[1]	
AE10	eDP_TX[2]	
AE6	eDP_TX[3]	

IVY-BRIDGE_BGA1023
@

PCI EXPRESS -- GRAPHICS

PEG_ICOMPI	G3	PEG_COMP	
PEG_ICOMPO	G1		
PEG_RCOMPO	G4		
PEG_RX#[0]	H22	PEG_GTX_C_HRX_N0	
PEG_RX#[1]	J21	PEG_GTX_C_HRX_N1	
PEG_RX#[2]	B22	PEG_GTX_C_HRX_N2	
PEG_RX#[3]	D21	PEG_GTX_C_HRX_N3	
PEG_RX#[4]	A19	PEG_GTX_C_HRX_N4	
PEG_RX#[5]	D17	PEG_GTX_C_HRX_N5	
PEG_RX#[6]	B14	PEG_GTX_C_HRX_N6	
PEG_RX#[7]	D13	PEG_GTX_C_HRX_N7	
PEG_RX#[8]	A11	PEG_GTX_C_HRX_N8	
PEG_RX#[9]	B10	PEG_GTX_C_HRX_N9	
PEG_RX#[10]	G8	PEG_GTX_C_HRX_N10	
PEG_RX#[11]	A8	PEG_GTX_C_HRX_N11	
PEG_RX#[12]	B6	PEG_GTX_C_HRX_N12	
PEG_RX#[13]	H8	PEG_GTX_C_HRX_N13	
PEG_RX#[14]	E5	PEG_GTX_C_HRX_N14	
PEG_RX#[15]	K7	PEG_GTX_C_HRX_N15	
PEG_RX[0]	K22	PEG_GTX_C_HRX_P0	
PEG_RX[1]	K19	PEG_GTX_C_HRX_P1	
PEG_RX[2]	C21	PEG_GTX_C_HRX_P2	
PEG_RX[3]	D19	PEG_GTX_C_HRX_P3	
PEG_RX[4]	C19	PEG_GTX_C_HRX_P4	
PEG_RX[5]	D16	PEG_GTX_C_HRX_P5	
PEG_RX[6]	C13	PEG_GTX_C_HRX_P6	
PEG_RX[7]	D12	PEG_GTX_C_HRX_P7	
PEG_RX[8]	C11	PEG_GTX_C_HRX_P8	
PEG_RX[9]	C9	PEG_GTX_C_HRX_P9	
PEG_RX[10]	F8	PEG_GTX_C_HRX_P10	
PEG_RX[11]	C8	PEG_GTX_C_HRX_P11	
PEG_RX[12]	C5	PEG_GTX_C_HRX_P12	
PEG_RX[13]	H6	PEG_GTX_C_HRX_P13	
PEG_RX[14]	F6	PEG_GTX_C_HRX_P14	
PEG_RX[15]	K6	PEG_GTX_C_HRX_P15	
PEG_TX#[0]	G22	PEG_HTX_GRX_N0	
PEG_TX#[1]	C23	PEG_HTX_GRX_N1	
PEG_TX#[2]	D23	PEG_HTX_GRX_N2	
PEG_TX#[3]	F21	PEG_HTX_GRX_N3	
PEG_TX#[4]	H19	PEG_HTX_GRX_N4	
PEG_TX#[5]	C17	PEG_HTX_GRX_N5	
PEG_TX#[6]	K15	PEG_HTX_GRX_N6	
PEG_TX#[7]	F17	PEG_HTX_GRX_N7	
PEG_TX#[8]	F14	PEG_HTX_GRX_N8	
PEG_TX#[9]	A15	PEG_HTX_GRX_N9	
PEG_TX#[10]	J14	PEG_HTX_GRX_N10	
PEG_TX#[11]	H13	PEG_HTX_GRX_N11	
PEG_TX#[12]	M10	PEG_HTX_GRX_N12	
PEG_TX#[13]	F10	PEG_HTX_GRX_N13	
PEG_TX#[14]	D9	PEG_HTX_GRX_N14	
PEG_TX#[15]	J4	PEG_HTX_GRX_N15	
PEG_TX[0]	F22	PEG_HTX_GRX_P0	
PEG_TX[1]	A23	PEG_HTX_GRX_P1	
PEG_TX[2]	D24	PEG_HTX_GRX_P2	
PEG_TX[3]	E21	PEG_HTX_GRX_P3	
PEG_TX[4]	G19	PEG_HTX_GRX_P4	
PEG_TX[5]	B18	PEG_HTX_GRX_P5	
PEG_TX[6]	K17	PEG_HTX_GRX_P6	
PEG_TX[7]	G17	PEG_HTX_GRX_P7	
PEG_TX[8]	E14	PEG_HTX_GRX_P8	
PEG_TX[9]	C15	PEG_HTX_GRX_P9	
PEG_TX[10]	K13	PEG_HTX_GRX_P10	
PEG_TX[11]	G13	PEG_HTX_GRX_P11	
PEG_TX[12]	K10	PEG_HTX_GRX_P12	
PEG_TX[13]	G10	PEG_HTX_GRX_P13	
PEG_TX[14]	D8	PEG_HTX_GRX_P14	
PEG_TX[15]	K4	PEG_HTX_GRX_P15	

C259	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_N0
C276	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_N1
C257	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_N2
C274	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_N3
C254	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_N4
C272	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_N5
C252	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_N6
C270	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_N7
C250	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_N8
C268	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_N9
C248	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_N10
C267	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_N11
C246	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_N12
C264	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_N13
C244	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_N14
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C277	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_P1
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C273	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_P5
C253	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_P6
C271	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_P7
C251	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_P8
C269	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_P9
C249	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_P10
C266	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_P11
C247	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_P12
C265	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_P13
C245	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_P14
C263	1	2	PX@	0.22U_0402_6.3V6K	PEG_GTX_HRX_P15
C562	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_N0
C582	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_N1
C564	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_N2
C584	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_N3
C566	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_N4
C587	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_N5
C568	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_N6
C589	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_N7
C570	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_N8
C591	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_N9
C572	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_N10
C593	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_N11
C574	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_N12
C594	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_N13
C576	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_N14
C597	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_N15
C561	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_P0
C583	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_P1
C563	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_P2
C585	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_P3
C565	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_P4
C586	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_P5
C567	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_P6
C588	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_P7
C569	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_P8
C590	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_P9
C571	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_P10
C592	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_P11
C573	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_P12
C595	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_P13
C575	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_P14
C596	1	2	PX@	0.22U_0402_6.3V6K	PEG_HTX_C_GRX_P15

PEG_GTX_HRX_N[0..15] [22]
PEG_GTX_HRX_P[0..15] [22]
PEG_HTX_C_GRX_N[0..15] [22]
PEG_HTX_C_GRX_P[0..15] [22]

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

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Issued Date	2011/06/24	Deciphered Date	2012/07/12

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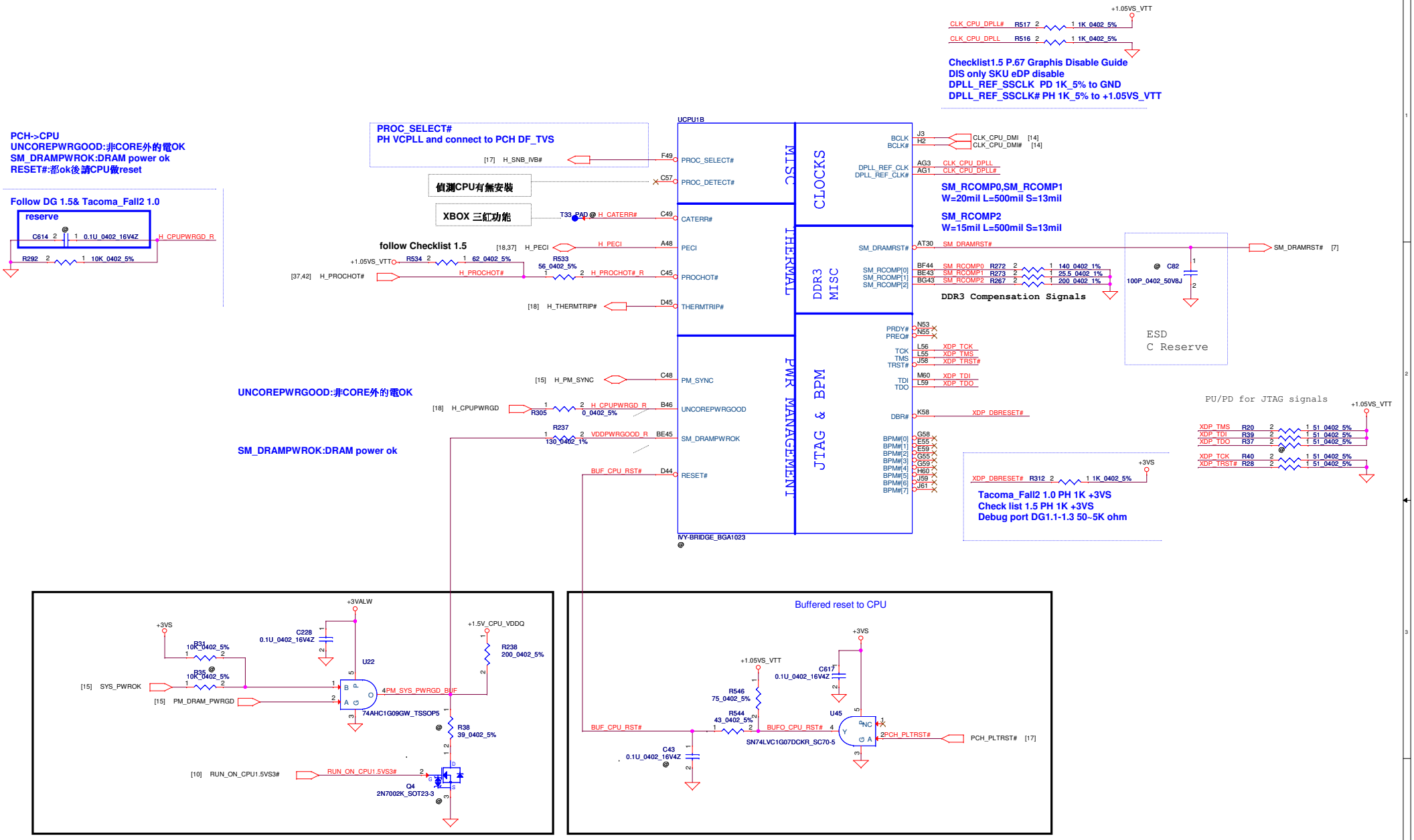
Compal Electronics, Inc.

Title: PROCESSOR(1/7) DMI,FDI,PEG

Size: Custom | Document Number: Sherry and Royal | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 5 of 55



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title: PROCESSOR(3/7) DDRIII
				Size: Custom; Document Number: Sherry and Royal; Rev: 0.1
				Date: Thursday, February 02, 2012; Sheet 6 of 55

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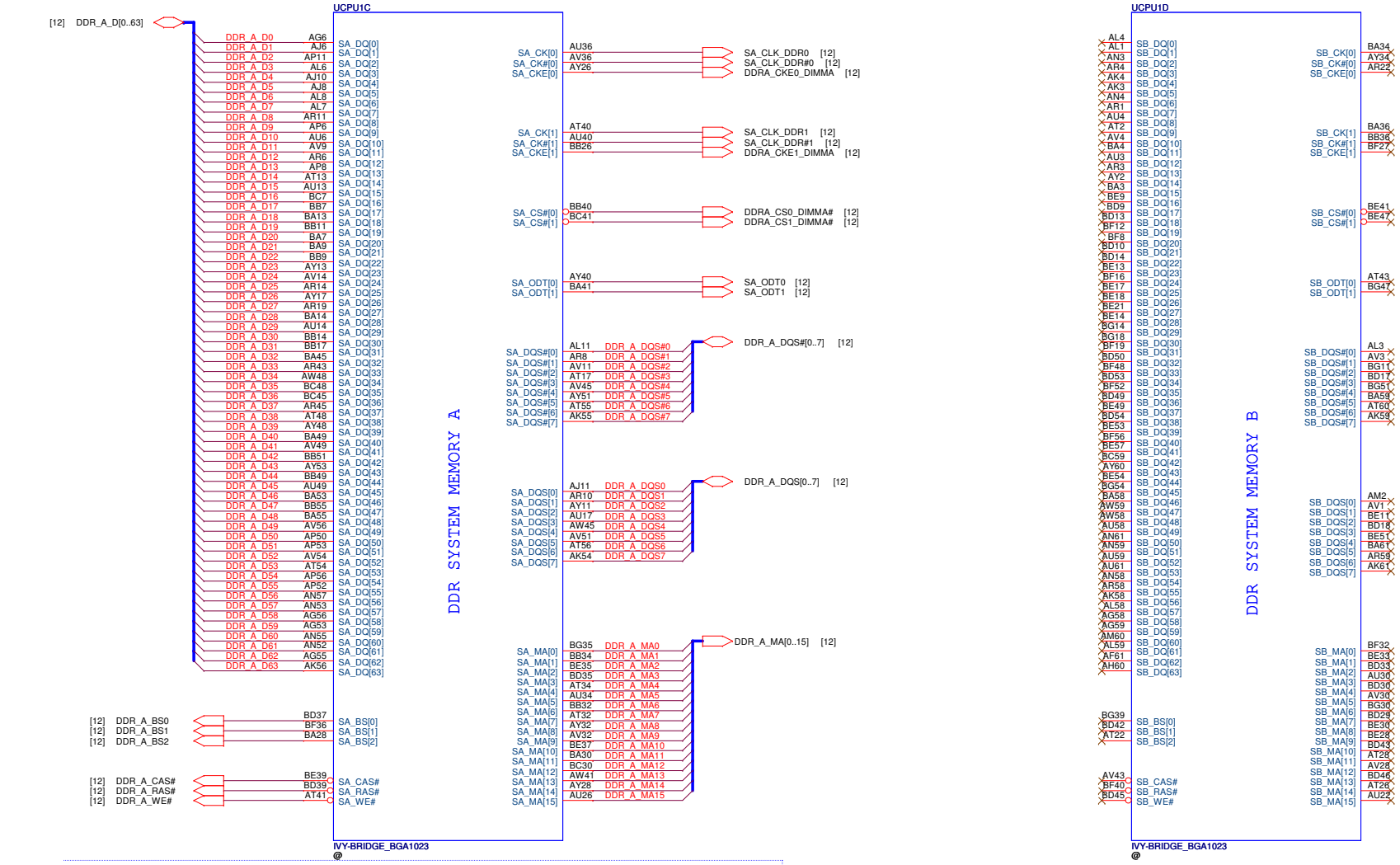

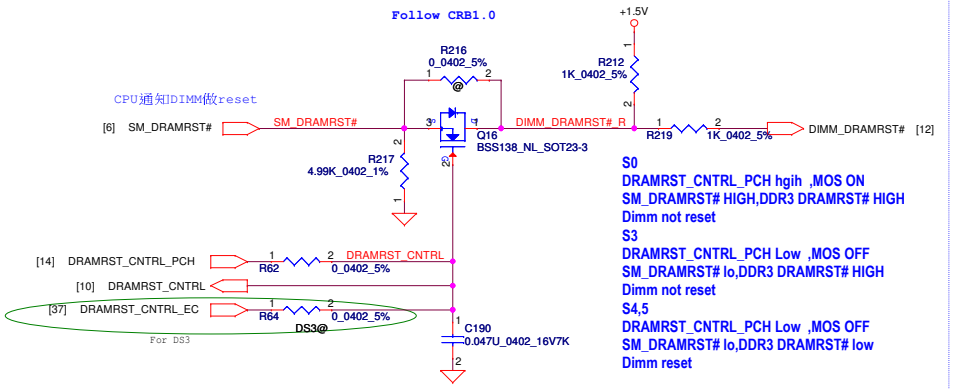

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title: PROCESSOR(3/7) DDRIII

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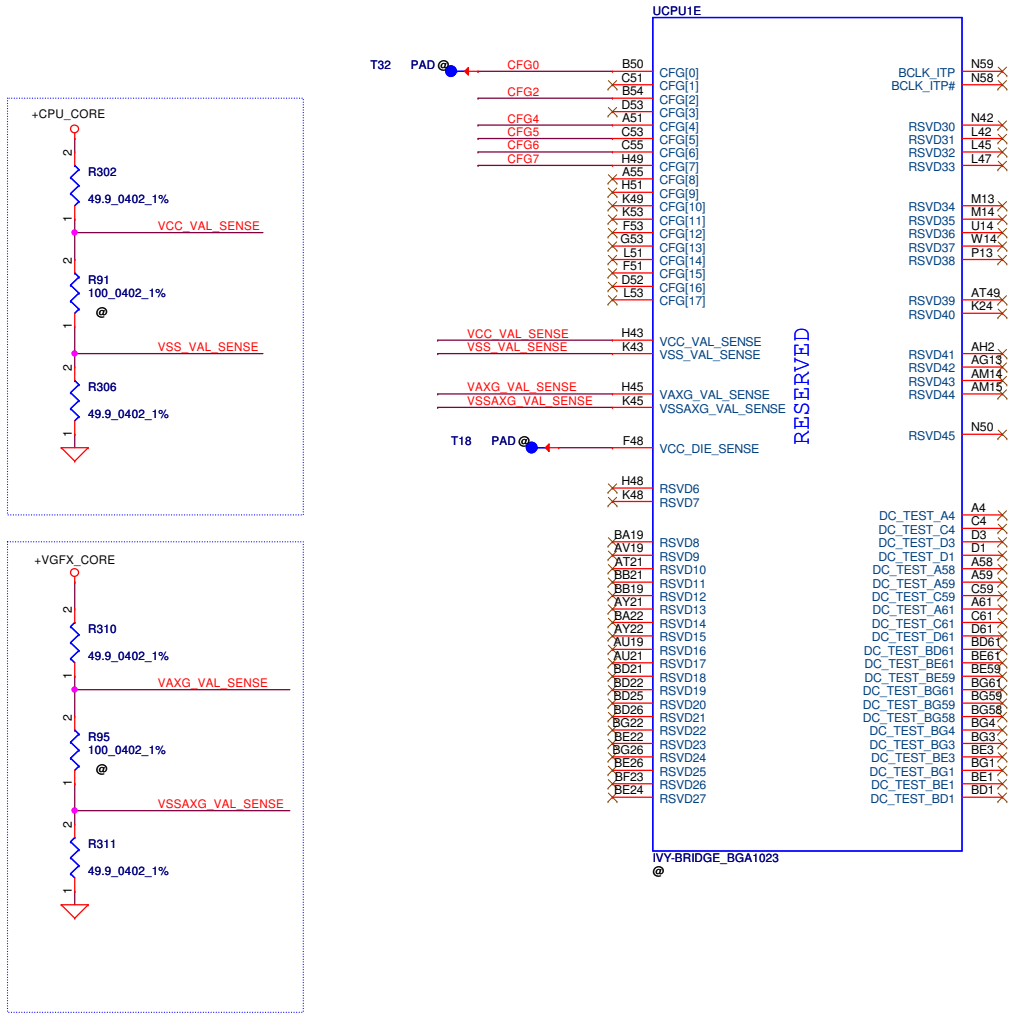
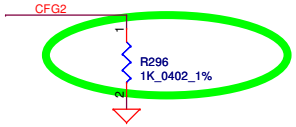
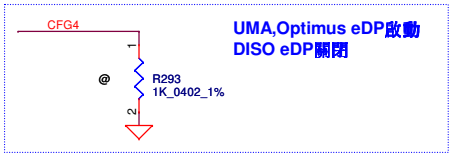


These pins are for solder joint reliability and non-critical to function. For BGA only.

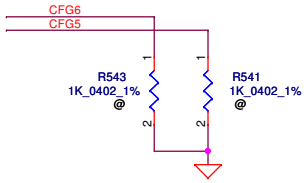
CFG Straps for Processor



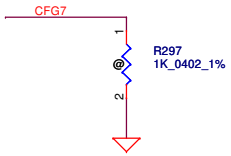
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0:Lane Reversed



eDP enable	
CFG4	★ 1:Disable 0:Enable



PCIE Port Bifurcation Straps	
CFG[6:5]	★11: (Default) 1x16 PCI Express 10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express



PEG DEFER TRAINING	Tacoma_Fall2 1.0 P.12
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Issued Date	2011/06/24	Deciphered Date	2012/07/12

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Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size: Custom | Document Number: Sherry and Royal | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 8 of 55

POWER

ULV type
DC 33A

8.5A

UCPU1F

+CPU_CORE

INTEL Recommend VCC
4*470UF,12*22uF(0805) and 35*2.2uF(0402)
PD0.8
CAP at Power side

CORE SUPPLY

A26	VCC[1]
A29	VCC[2]
A31	VCC[3]
A34	VCC[4]
A35	VCC[5]
A38	VCC[6]
A39	VCC[7]
A42	VCC[8]
C26	VCC[9]
C27	VCC[10]
C32	VCC[11]
C34	VCC[12]
C37	VCC[13]
C39	VCC[14]
C42	VCC[15]
D27	VCC[16]
D32	VCC[17]
D34	VCC[18]
D37	VCC[19]
D39	VCC[20]
D42	VCC[21]
E26	VCC[22]
E28	VCC[23]
E32	VCC[24]
E34	VCC[25]
E37	VCC[26]
E38	VCC[27]
F25	VCC[28]
F26	VCC[29]
F28	VCC[30]
F32	VCC[31]
F34	VCC[32]
F37	VCC[33]
F38	VCC[34]
F42	VCC[35]
G42	VCC[36]
H25	VCC[37]
H26	VCC[38]
H28	VCC[39]
H29	VCC[40]
H32	VCC[41]
H34	VCC[42]
H35	VCC[43]
H37	VCC[44]
H38	VCC[45]
H40	VCC[46]
J25	VCC[47]
J26	VCC[48]
J28	VCC[49]
J29	VCC[50]
J32	VCC[51]
J34	VCC[52]
J35	VCC[53]
J37	VCC[54]
J38	VCC[55]
J40	VCC[56]
J42	VCC[57]
K26	VCC[58]
K27	VCC[59]
K29	VCC[60]
K32	VCC[61]
K34	VCC[62]
K35	VCC[63]
K37	VCC[64]
K39	VCC[66]
K42	VCC[67]
L25	VCC[68]
L28	VCC[69]
L33	VCC[70]
L36	VCC[71]
L40	VCC[72]
N26	VCC[73]
N30	VCC[74]
N34	VCC[75]
N38	VCC[76]

PEG IO AND DDR IO

+1.05VS_VTT

For DDR

INTEL Recommend VCCIO
2*330UF,10*10uF(0603) and 26*1uF(0402)
PD0.8
CAP at Power side

VCCIO[1]	AF46
VCCIO[3]	AG48
VCCIO[4]	AG50
VCCIO[5]	AG51
VCCIO[6]	AJ17
VCCIO[7]	AJ21
VCCIO[8]	AJ25
VCCIO[9]	AJ43
VCCIO[10]	AJ47
VCCIO[11]	AK50
VCCIO[12]	AK51
VCCIO[13]	AL14
VCCIO[14]	AL15
VCCIO[15]	AL16
VCCIO[16]	AL20
VCCIO[17]	AL22
VCCIO[18]	AL26
VCCIO[19]	AL45
VCCIO[20]	AL48
VCCIO[21]	AM16
VCCIO[22]	AM17
VCCIO[23]	AM21
VCCIO[24]	AM43
VCCIO[25]	AM47
VCCIO[26]	AN20
VCCIO[27]	AN42
VCCIO[28]	AN45
VCCIO[29]	AN48

For PEG

VCCIO[30]	AA14
VCCIO[31]	AA15
VCCIO[32]	AB17
VCCIO[33]	AB20
VCCIO[34]	AC13
VCCIO[35]	AD16
VCCIO[36]	AD18
VCCIO[37]	AD21
VCCIO[38]	AE14
VCCIO[39]	AE15
VCCIO[40]	AF16
VCCIO[41]	AF18
VCCIO[42]	AF20
VCCIO[43]	AG15
VCCIO[44]	AG16
VCCIO[45]	AG17
VCCIO[46]	AG20
VCCIO[47]	AG21
VCCIO[48]	AJ14
VCCIO[49]	AJ15

+1.05VS_VTT

VCCIO50 W16
VCCIO51 W17

+3VS

R521 10K_0402_5%

VCCIO_SEL

R522 10K_0402_5% @

VCCIO_SEL after Ivy bridge ES2 Voltage support	
BC22 *	1/NC : (Default) +1.05VS_VTT 0: +1.0VS_VTT

VCCIO_SEL BC22 VCCIO_SEL

QUIET RAILS

+1.05VS_VTT

VCCPQE[1] AM25
VCCPQE[2] AN22

C553 1U_0402_6.3V6K

+1.05VS_VTT R531 130_0402_5%

+1.05VS_VTT R529 75_0402_5%

Place the PU
resistors close to CPU

SVID

VIDALERT#	A44	H_CPU_SVIDALRT#	R528	43_0402_1%	VR_SVID_ALRT# [50]
VIDSCLK	B43	H_CPU_SVIDCLK	R527	0_0402_5%	VR_SVID_CLK [50]
VIDSOUT	C44	H_CPU_SVIDDAT	R530	0_0402_5%	VR_SVID_DAT [50]

Place the PU
resistors close to VR

SENSE LINES

+CPU_CORE

R79 100_0402_1% @

R281 100_0402_1%

VCC_SENSE	F43	VCCSENSE_R	R282	0_0402_5%	VCCSENSE [50]
VSS_SENSE	G43	VSSSENSE_R	R289	0_0402_5%	VSSSENSE [50]

R288 100_0402_1%

R513 10_0402_5% +1.05VS_VTT

VCCIO_SENSE	AN16	VCCIO_SENSE	VCCIO_SENSE [47]
VSS_SENSE_VCCIO	AN17	VSSIO_SENSE_L	VSSIO_SENSE_L [47]

R512 10_0402_5%

Check list 1.5

Should change to connect form
power circuit & layout differential
with VCCIO_SENSE.

IVY-BRIDGE_BGA1023
@

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Issued Date	2011/06/24	Deciphered Date	2012/07/12

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Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

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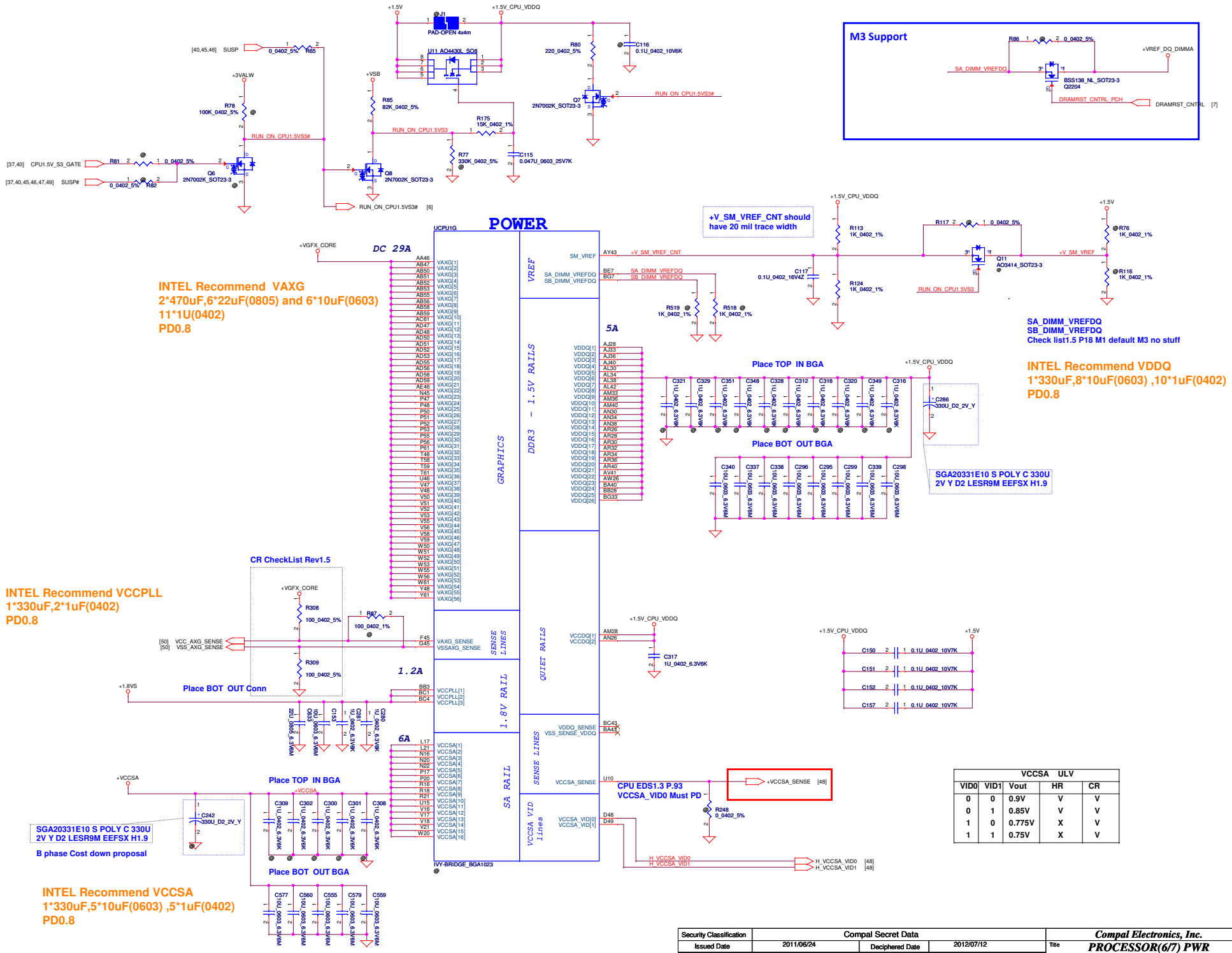
Date: Thursday, February 02, 2012 | Sheet 9 of 55



VCCSA ULV				
VID0	VID1	Vout	HR	CR
0	0	0.9V	V	V
0	1	0.85V	V	V
1	0	0.775V	X	V
1	1	0.75V	X	V

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Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title: PROCESSOR(6/7) PWR

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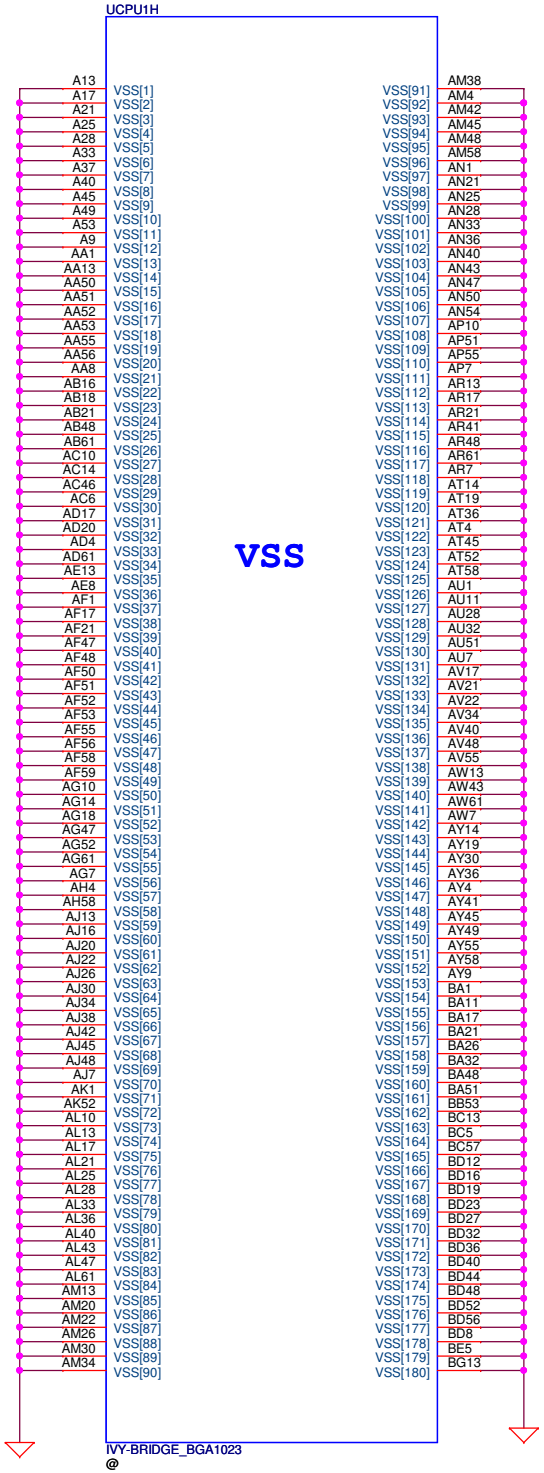

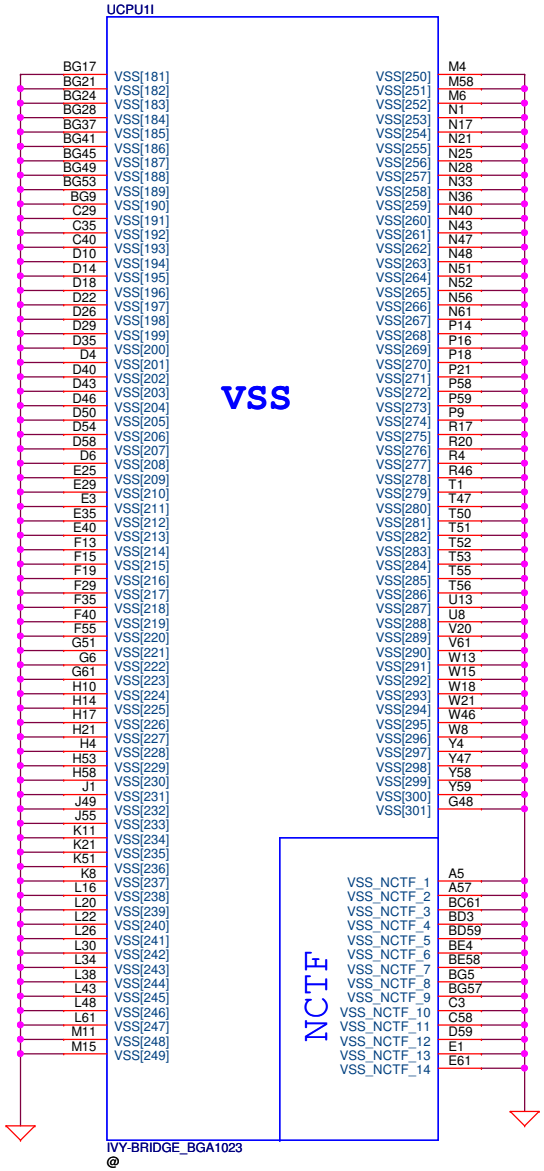

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

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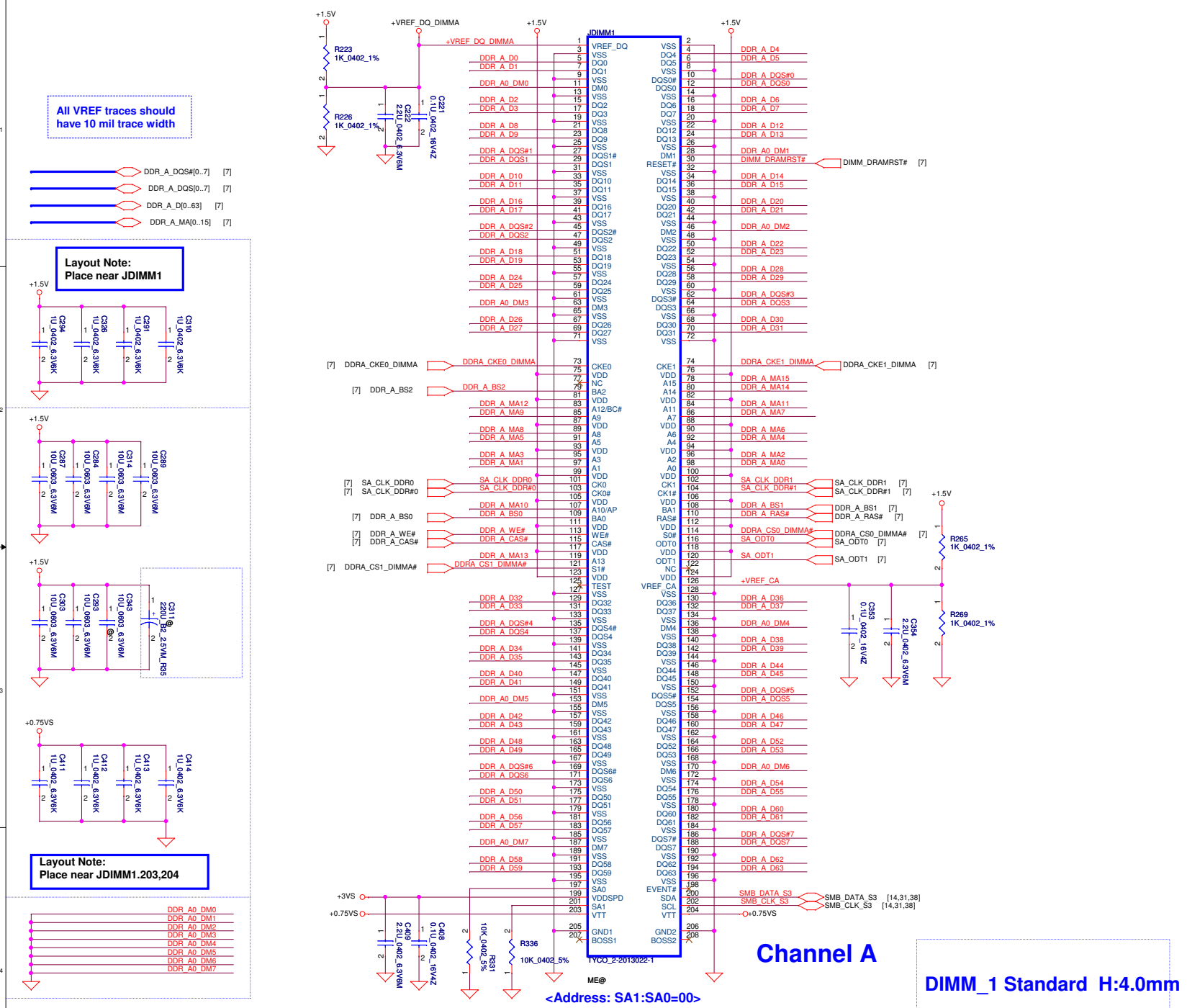
Compal Electronics, Inc.

Title: **PROCESSOR(7/7) VSS**

Size: Custom | Document Number: **Sherry and Royal** | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 11 of 55



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: DDRIII DIMMB

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RTCRST close to RAM door

+RTCBATT C439 1U_0402_6.3V6K R501 0_0603_5% PCH_RTCRST#
R356 20K_0402_5% PCH_SRTCRST#
R357 20K_0402_5%
C440 1U_0402_6.3V6K R372 0_0603_5%

+RTCBATT R358 1M_0402_5% SM_INTRUDER#
R355 330K_0402_5% PCH_INTVRMEN

INTVRMEN
★ H : Integrated VRM enable
L : Integrated VRM disable
(INTVRMEN should always be pull high.)

+3VS R109 1K_0402_5% HDA_SPKR
HIGH= Enable (No Reboot)Disable TCO timer system reboot feature
★ LOW= Disable (Default internal PD)

+3V_PCH R46 1K_0402_5% HDA_SDOUT_PCH
[37] ME_FLASH R73 0_0402_5%

HDA_SDO
ME debug mode,this signal has a weak internal PD
★ Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]

+3V_PCH R47 1K_0402_5% HDA_SYNC_PCH
This signal has a weak internal pull-down

On Die PLL VR Select is supplied by
★1.5V when sampled high
1.8V when sampled low
Needs to be pulled High for Huron River platfrom

[36] HDA_BITCLK_AUDIO R75 33_0402_5% R30 33_0402_5% HDA_BITCLK_PCH
[36] HDA_SYNC_AUDIO R74 33_0402_5% HDA_SYNC_PCH_R
[36] HDA_RST_AUDIO# R72 33_0402_5% HDA_RST_PCH#
[36] HDA_SDOUT_AUDIO HDA_SDOUT_PCH

+3V_PCH R134 200_0402_5% PCH_JTAG_TDO R141 100_0402_1%
+3V_PCH R143 200_0402_5% PCH_JTAG_TMS R140 100_0402_1%
+3V_PCH R137 200_0402_5% PCH_JTAG_TDI R142 100_0402_1%

PCH_RTCX1 R406 10M_0402_5% PCH_RTCX2
Y2 32.768KHZ_12.5PF_9H032000019
18P_0402_50V8J C452 C451 18P_0402_50V8J

Prevent back drive issue.

+5VS Q3 BSS138_NL_SOT23-3 R48 0_0402_5%
HDA_SYNC_PCH_R R29 1M_0402_5%
[36] HDA_SPKR
[36] HDA_SDIN0

R162 1K_0402_1% PCH_GPIO33
+3V_PCH R341 10K_0402_5% PCH_GPIO13
R100 51_0402_5%

U13A PANTHER_FCBGA989 <BOM Structure>

Signal	Pin	Block
PCH_RTCX1	A20	RTC
PCH_RTCX2	C20	RTC
PCH_RTCRST#	D20	RTC
PCH_SRTCRST#	G22	RTC
SM_INTRUDER#	K22	RTC
PCH_INTVRMEN	C17	RTC
HDA_BITCLK_PCH	N34	IHDA
HDA_SYNC_PCH	L34	IHDA
HDA_SPKR	T10	IHDA
HDA_RST_PCH#	K34	IHDA
HDA_SDIN0	E34	IHDA
HDA_SDIN1	G34	IHDA
HDA_SDIN2	C34	IHDA
HDA_SDIN3	A34	IHDA
HDA_SDOUT_PCH	A36	IHDA
PCH_GPIO33	C36	IHDA
PCH_GPIO13	N32	IHDA
PCH_JTAG_TCK	J3	JTAG
PCH_JTAG_TMS	H7	JTAG
PCH_JTAG_TDI	K5	JTAG
PCH_JTAG_TDO	H1	JTAG
SPI_CLK_PCH_R	T3	SPI
SPI_SB_CS0#	Y14	SPI
SPI_SB_CS1#	T1	SPI
SPI_SI	V4	SPI
SPI_SO_R	U3	SPI

LPC: FWH0 / LAD0 C38 LPC_AD0 → LPC_AD0 [31,37]; FWH1 / LAD1 A38 LPC_AD1 → LPC_AD1 [31,37]; FWH2 / LAD2 B37 LPC_AD2 → LPC_AD2 [31,37]; FWH3 / LAD3 C37 LPC_AD3 → LPC_AD3 [31,37]; FWH4 / LFRAME# D36 LPC_FRAME# → LPC_FRAME# [31,37]; LDRQ0# E36; LDRQ1# / GPIO23 K36; SERIRQ V5 SERIRQ → SERIRQ [37]

SATA 6G:
SATA0RXN AM3 / SATA0RXP AM1 → SATA_PRX_DTX_C_N0 [31], SATA_PRX_DTX_C_P0 [31]
SATA0TXN AP7 SATA_PTX_DRX_C_N0 2 — 1 C1185 0.01U_0402_16V7K → SATA_PTX_DRX_N0 [31]
SATA0TXP AP5 SATA_PTX_DRX_C_P0 2 — 1 C1208 0.01U_0402_16V7K → SATA_PTX_DRX_P0 [31]
SSD
SATA1RXN AM10 SATA_DTX_C_R_PRX_N1 R148 HDD1@ 2 — 1 0_0402_5% → SATA_DTX_C_PRX_N1 [35]
SATA1RXP AM8 SATA_DTX_C_R_PRX_P1 R149 HDD1@ 2 — 1 0_0402_5% → SATA_DTX_C_PRX_P1 [35]
SATA1TXN AP11 SATA_PTX_DRX_N1 R150 HDD1@ 2 — 1 0_0402_5% SATA_PTX_R_DRX_N1 HDD1@ 2 — 1 C1209 0.01U_0402_16V7K → SATA_PTX_R_DRX_N1 [35]
SATA1TXP AP10 SATA_PTX_DRX_P1 R151 HDD1@ 2 — 1 0_0402_5% SATA_PTX_R_DRX_P1 HDD1@ 2 — 1 C1223 0.01U_0402_16V7K → SATA_PTX_R_DRX_P1 [35]
HDD0 w/ HM77
Disable w/ HM70
SATA2RXN AD7 SATA_DTX_C_R_PRX_N2 R154 HDD2@ 2 — 1 0_0402_5% → SATA_DTX_C_PRX_N1
SATA2RXP AD5 SATA_DTX_C_R_PRX_P2 R157 HDD2@ 2 — 1 0_0402_5% → SATA_DTX_C_PRX_P1
SATA2TXN AH5 SATA_PTX_DRX_N2 R160 HDD2@ 2 — 1 0_0402_5% → SATA_PTX_R_DRX_N1_CO
SATA2TXP AH4 SATA_PTX_DRX_P2 R161 HDD2@ 2 — 1 0_0402_5% → SATA_PTX_R_DRX_P1_CO
HDD1 w/ HM70
SATA3RXN AB8 / SATA3RXP AB10 / SATA3TXN AF3 / SATA3TXP AF1 — Disable w/ HM70
SATA4RXN Y7 / SATA4RXP Y5 / SATA4TXN AD3 / SATA4TXP AD1
SATA5RXN Y3 / SATA5RXP Y1 / SATA5TXN AB3 / SATA5TXP AB1
SATAICOMPO Y11 — L=500mil S=15mil
SATAICOMPI Y10 SATA_COMP R121 37.4_0402_1% +1.05VS_VTT
SATA3RCOMPO AB12 — L=500mil S=15mil
SATA3COMPI AB13 SATA3_COMP R126 49.9_0402_1% +1.05VS_VTT
SATA3RBIAS AH1 RBIAS_SATA3 R440 750_0402_1%
SATALED# P3 PCH_SATALED#
SATA0GP / GPIO21 V14 PCH_GPIO21 — No use PH 10K +3VS
SATA1GP / GPIO19 P1 BBS_BIT0_R

SERIRQ R118 10K_0402_5% +3VS

GPIO19 has internal Pull up
GPIO21 Debug Port DG 1.2 PH 4.7K +3VS
+3VS
BBS_BIT0_R R466 10K_0402_5%
PCH_SATALED# R429 10K_0402_5%
PCH_GPIO21 R136 10K_0402_5%

Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
–	1	0
★ SPI	1	1

8MB SPI ROM FOR ME
& Non-share ROM.

+3VS R266 3.3K_0402_5% SPI_WP#1
R221 3.3K_0402_5% SPI_HOLD#1
R127 3.3K_0402_5% SPI_WP#
R171 3.3K_0402_5% SPI_HOLD#

SPI_SB_CS1# R172 0_0402_5% CS1# — SPI_SB_CS1#
SPI_SO_R R188 33_0402_5% SPI_SO1 — SPI_SO_R
SPI_WP#1
U46 16M W25Q16BVSSIG SOIC 8P: CS# 1, SO 2, WP# 3, GND 4, VCC 8, HOLD# 7, SCLK 6, SI 5
+3VS
SPI_HOLD#1 — SPI_HOLD#
SPI_CLK1 — SPI_CLK
SPI_SI1 — SPI_SI
R199 0_0402_5% SPI_CLK_PCH_R
R196 33_0402_5% SPI_SI

Reserve for EMI
C459 10P_0402_50V8J R434 33_0402_5% SPI_CLK_PCH_R

U6 Rersver 4M+2M Solution

+3VS C191 0.1U_0402_16V4Z
SPI_SB_CS0#2 R173 0_0402_5% CS# — SPI_SB_CS0#
SPI_SO_R R169 33_0402_5% SPI_SO_L — SPI_SO_R
SPI_WP#
U44 32M W25Q32BVSSIG SOIC 8P: CS# 1, SO 2, WP# 3, GND 4, VCC 8, HOLD# 7, SCLK 6, SI 5
SPI_HOLD# — SPI_HOLD#
SPI_CLK_PCH — SPI_CLK_PCH
SPI_SI_R — SPI_SI_R
R168 0_0402_5% SPI_CLK_PCH_R
R170 33_0402_5% SPI_SI

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Issued Date	2011/06/24	Deciphered Date	2012/07/12

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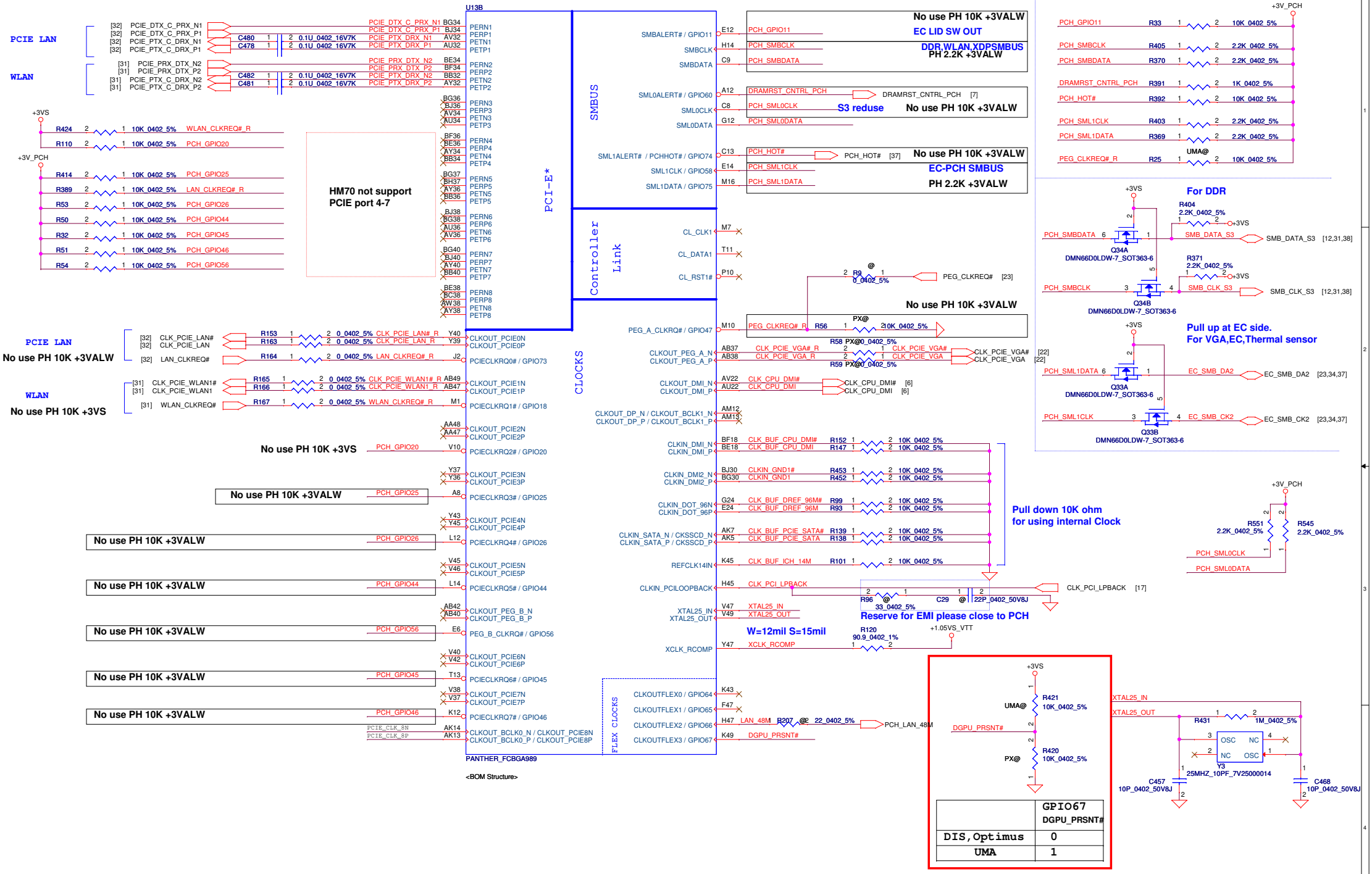
Compal Electronics, Inc.
Title: PCH (1/9) SATA,HDA,SPI, LPC, XDP
Size: Custom | Document Number: Sherry and Royal | Rev: 0.1
Date: Thursday, February 02, 2012 | Sheet 13 of 55



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Issued Date	2011/06/24	Deciphered Date	2012/07/12

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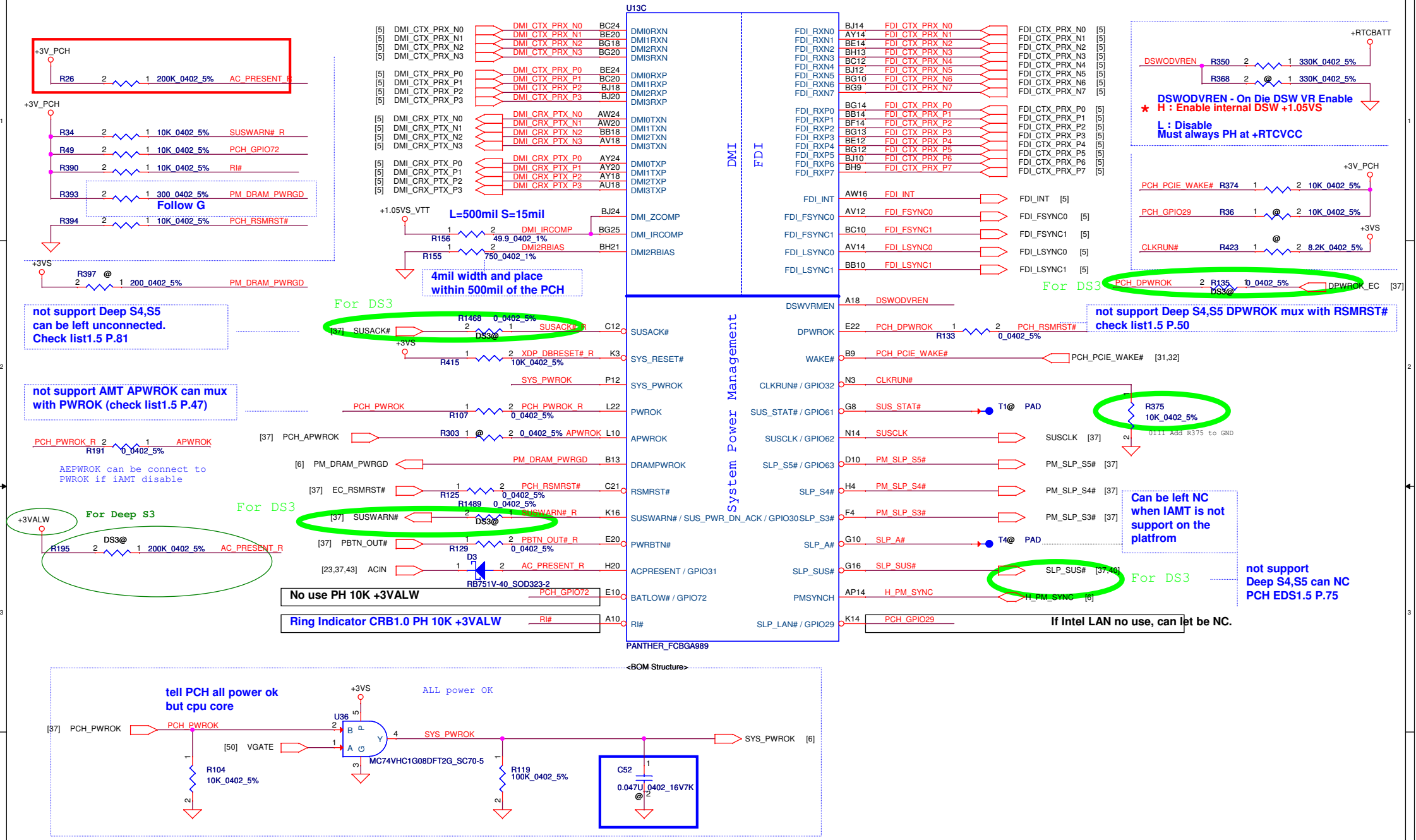
Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

Size: Custom | Document Number: Sherry and Royal | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 14 of 55



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

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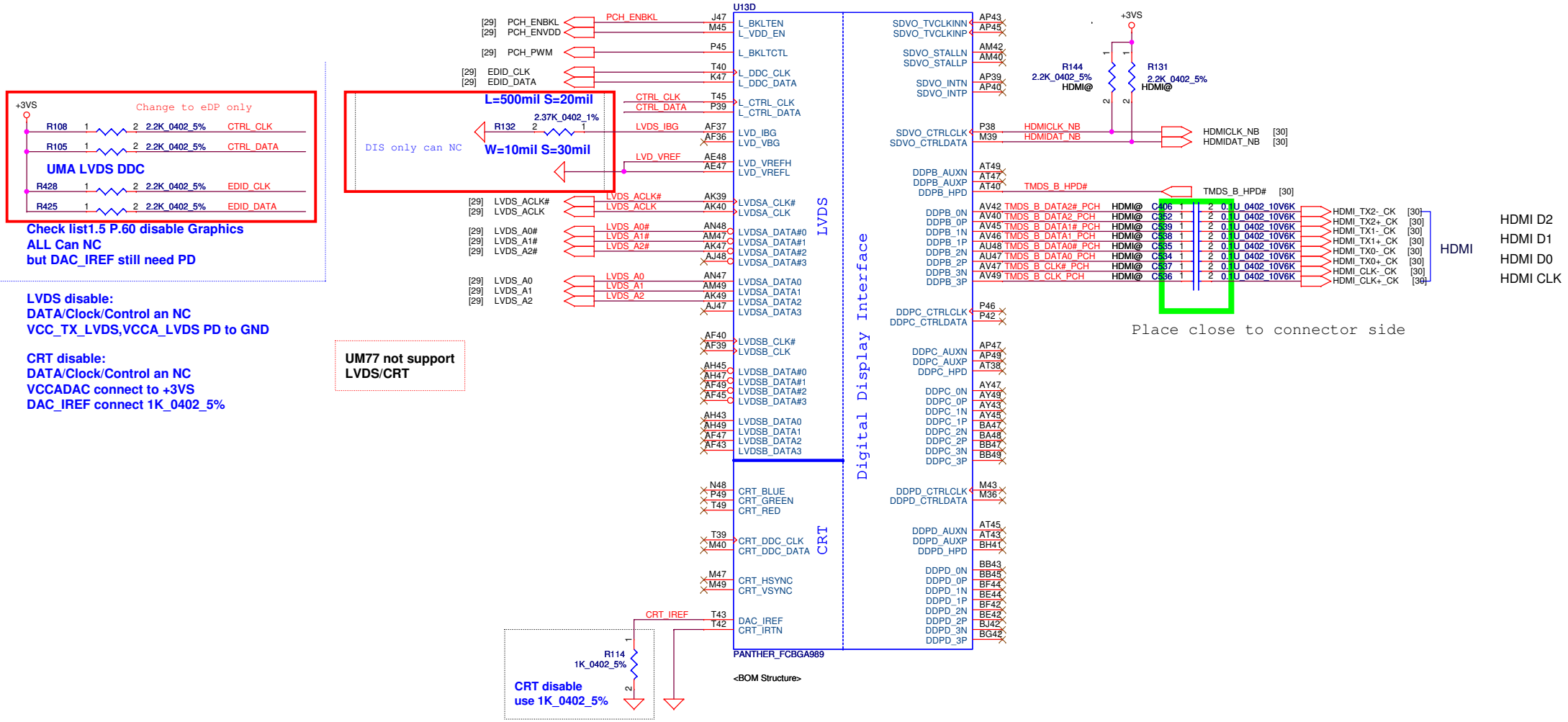
Compal Electronics, Inc.

Title: PCH (3/9) DMI,FDI,PM

Size: Custom | Document Number: Sherry and Royal | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 15 of 55



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title: PCH (4/9) LVDS,CRT,DP,HDMI
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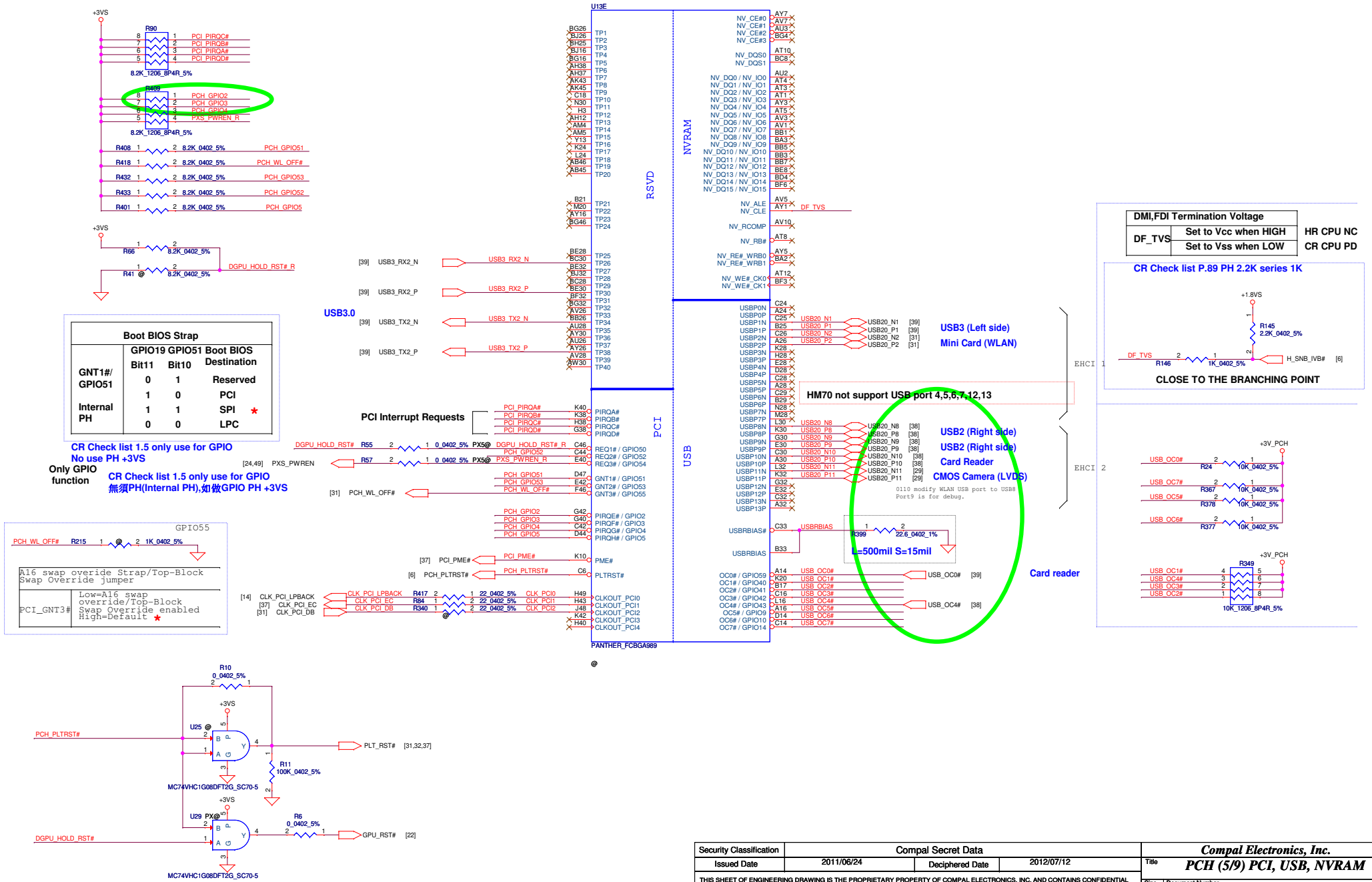
				Date: Thursday, February 02, 2012; Sheet 16 of 55



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

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Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, NVRAM

Size: Custom | Document Number: Sherry and Royal | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 17 of 55

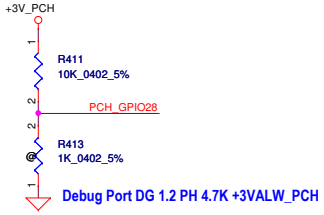
HDA_SYNC PH(PLL =+1.5VS)

GPIO28

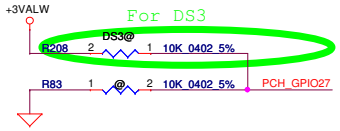
On-Die PLL Voltage Regulator

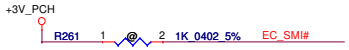
This signal has a weak internal pull up

★ H : On-Die PLL voltage regulator enable
L : On-Die PLL Voltage Regulator disable

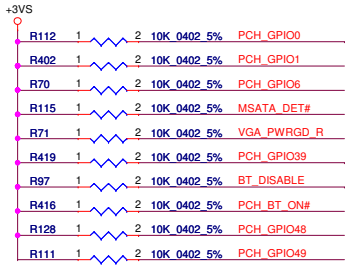


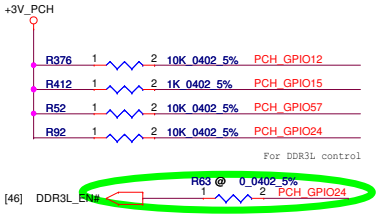
Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal





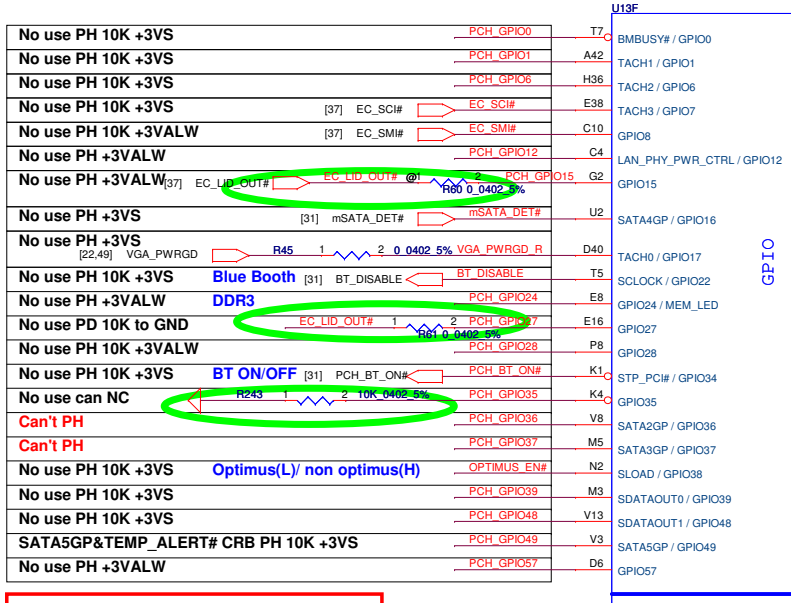
SATA2GP/GPIO36 & SATA3GP/GPIO37
Sampled at Rising edge of PWROK.
Weak internal pull-down.
(weak internal pull-down is disabled after PLTRST# de-asserts)
NOTE: This signal should NOT be pulled high when strap is sampled

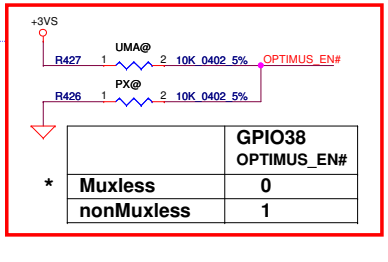




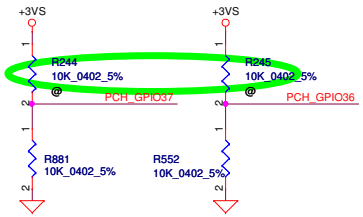
GPIO24 Unmultiplexed
NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.
CRB1.0 PH10K to +3VALW

Fan Tachometer Inputs TACH1~7 only on server can insted to GPIO

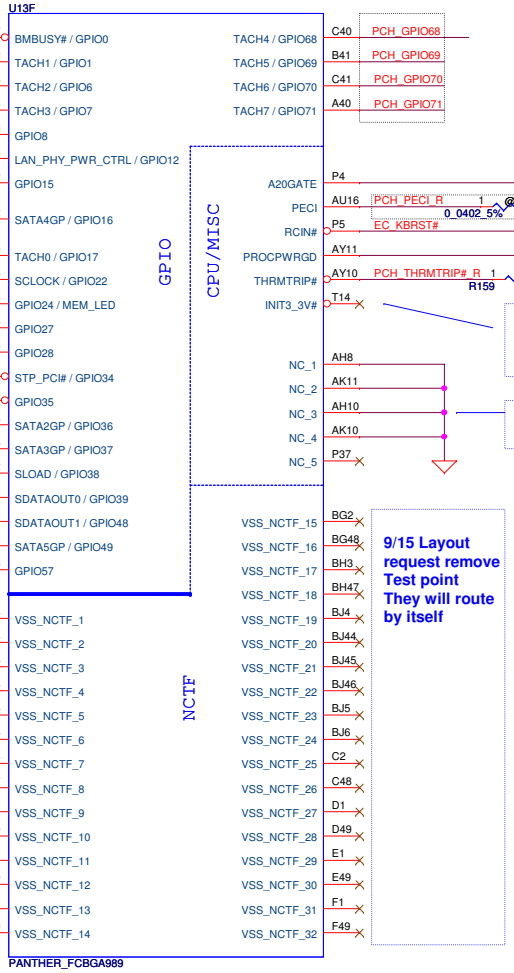




	GPIO38 OPTIMUS_EN#
* Muxless	0
nonMuxless	1

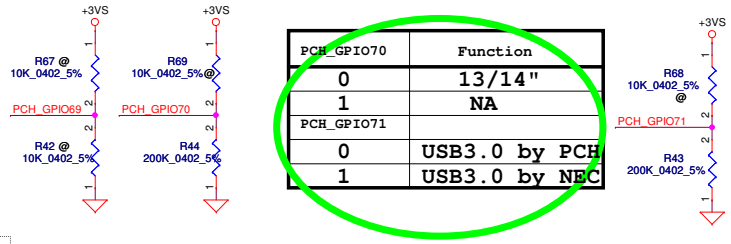


GPIO36/GPIO37 is Strap functionality
that requires internal pull down to be sampled at rising PWROK.
When uses as SATA2GP/SATA3GP for mechanical presence detect
-use a external pull up 150K-200K ohm to Vcc3_3
When used as GP input
-ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA*GP
-use 8.2K-10K pull-down
check list page 47



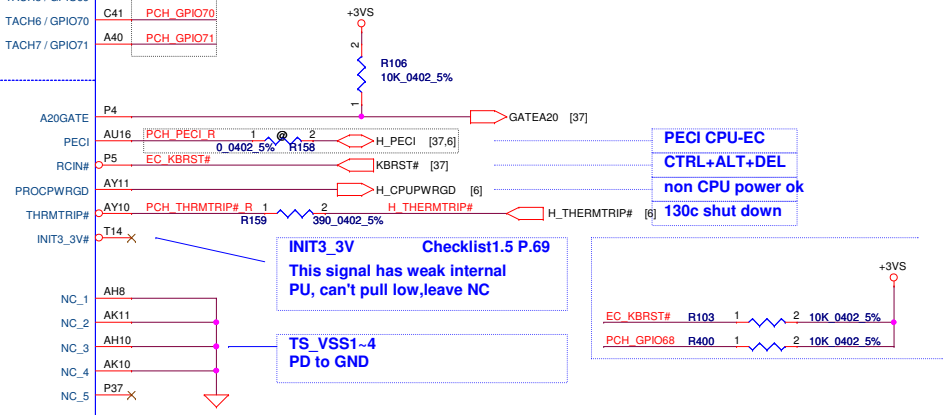
9/15 Layout request remove Test point They will route by itself

9/15 Layout request remove Test point They will route by itself



PCH_GPIO70	Function
0	13/14"
1	NA
PCH_GPIO71	
0	USB3.0 by PCH
1	USB3.0 by NEC

Need?



INIT3_3V Checklist1.5 P.69
This signal has weak internal PU, can't pull low,leave NC

TS_VSS1~4
PD to GND

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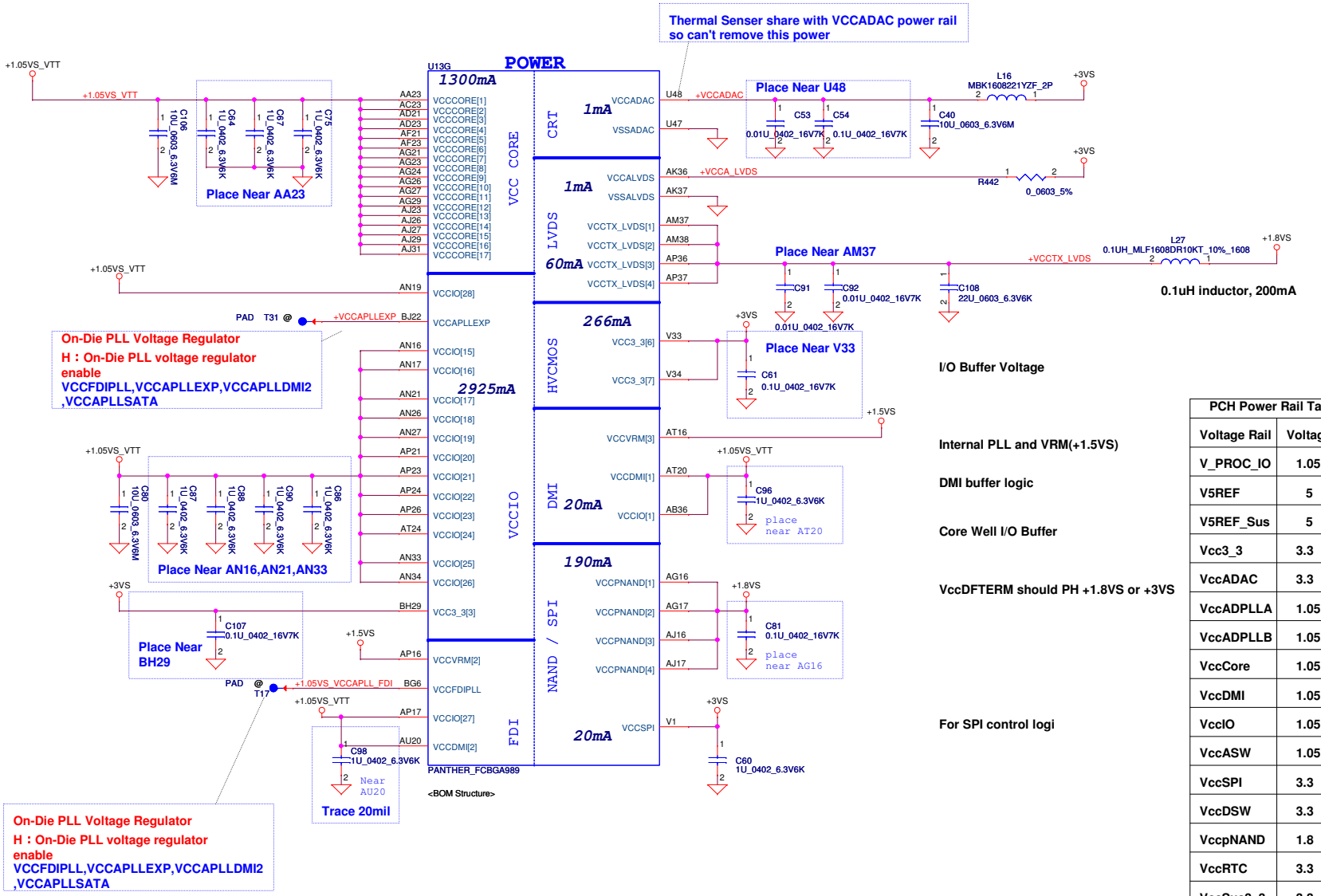
Compal Electronics, Inc.

Title: *PCH (6/9) GPIO, CPU, MISC*

Size: Custom | Document Number: *Sherry and Royal* | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 18 of 55



PCH Power Rail Table			
Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

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Issued Date	2011/06/24	Deciphered Date	2012/07/12

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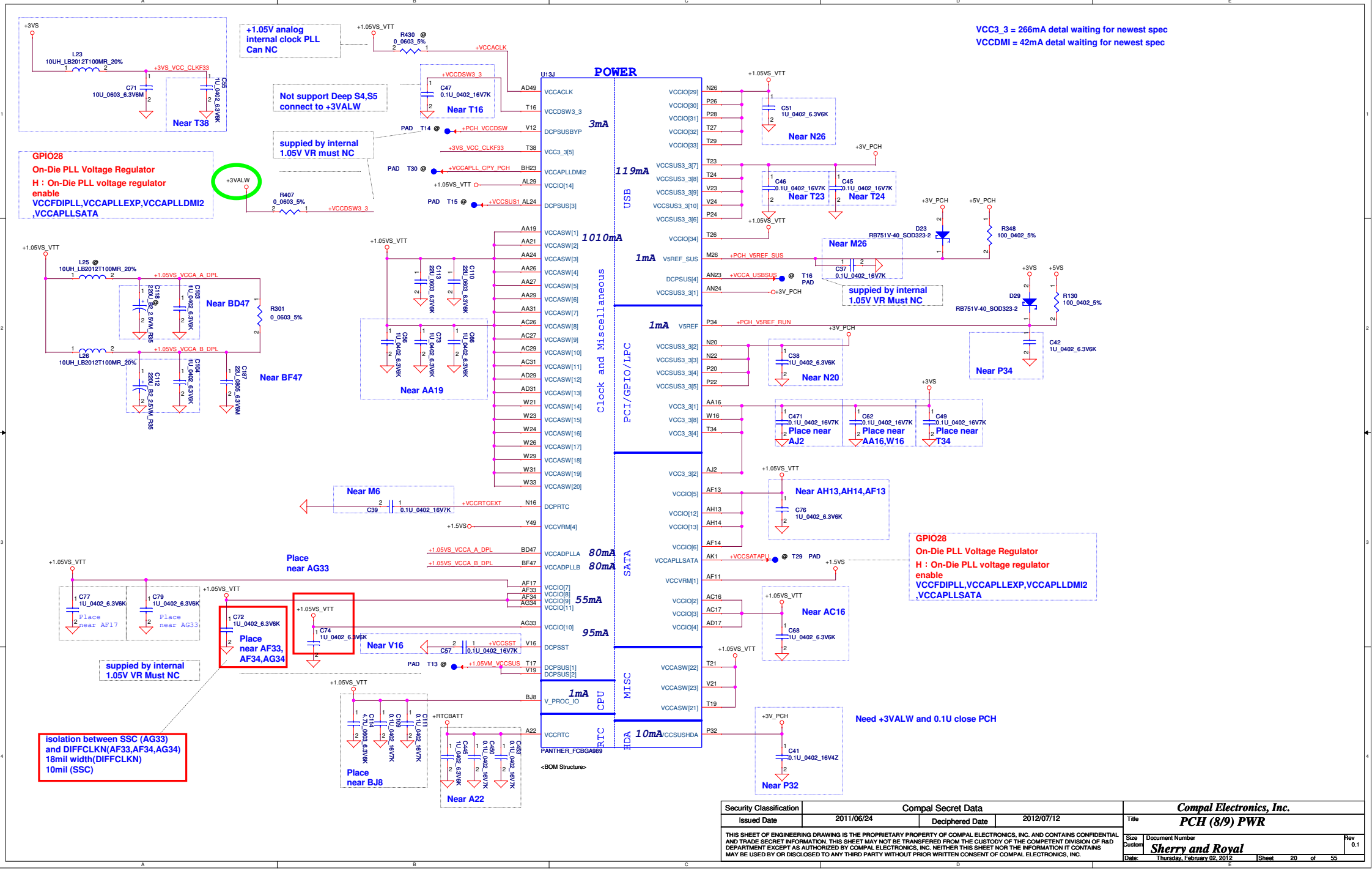
Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: Sherry and Royal | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 19 of 55



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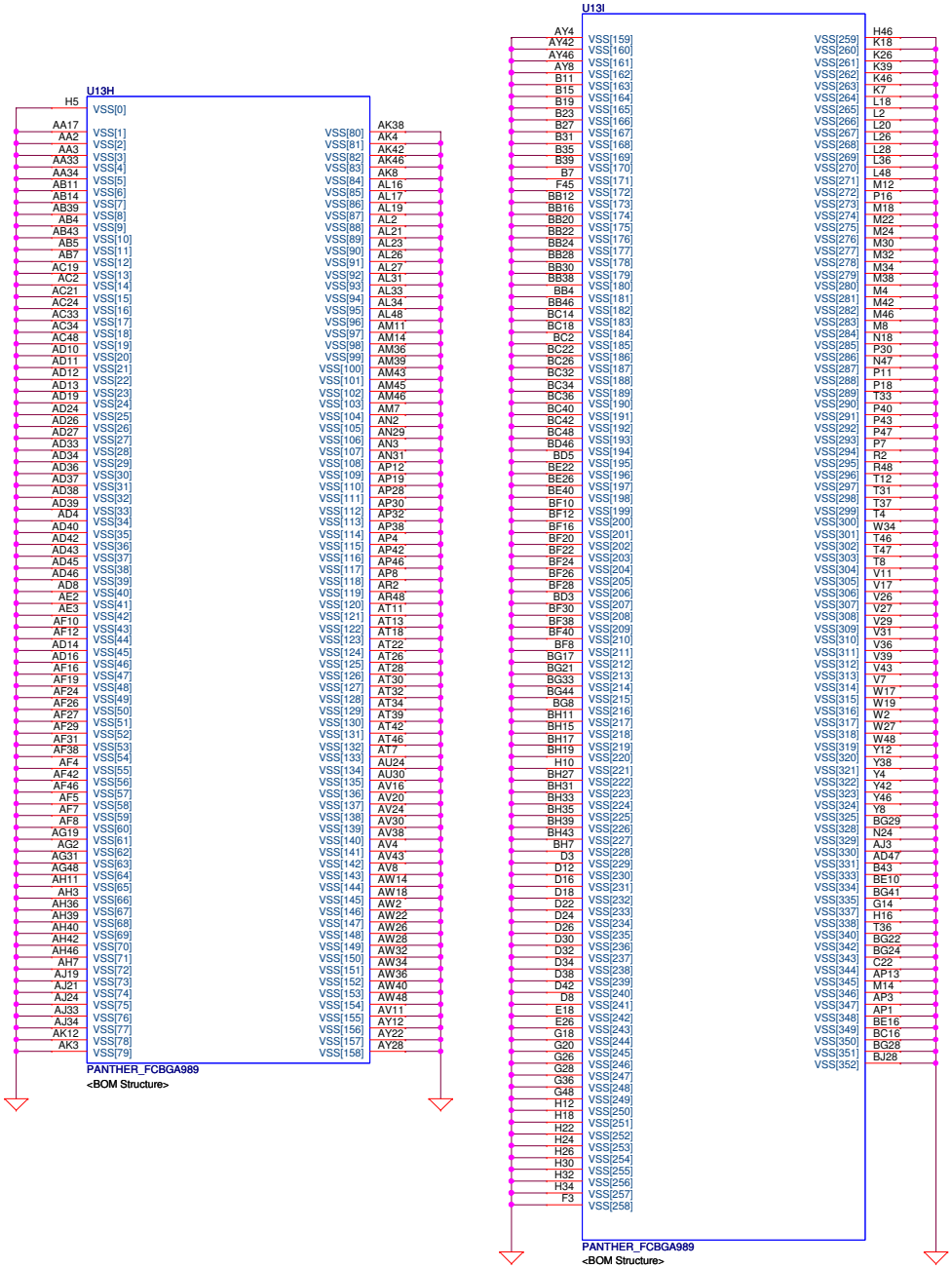
Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size: Custom | Document Number: Sherry and Royal | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 20 of 55



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

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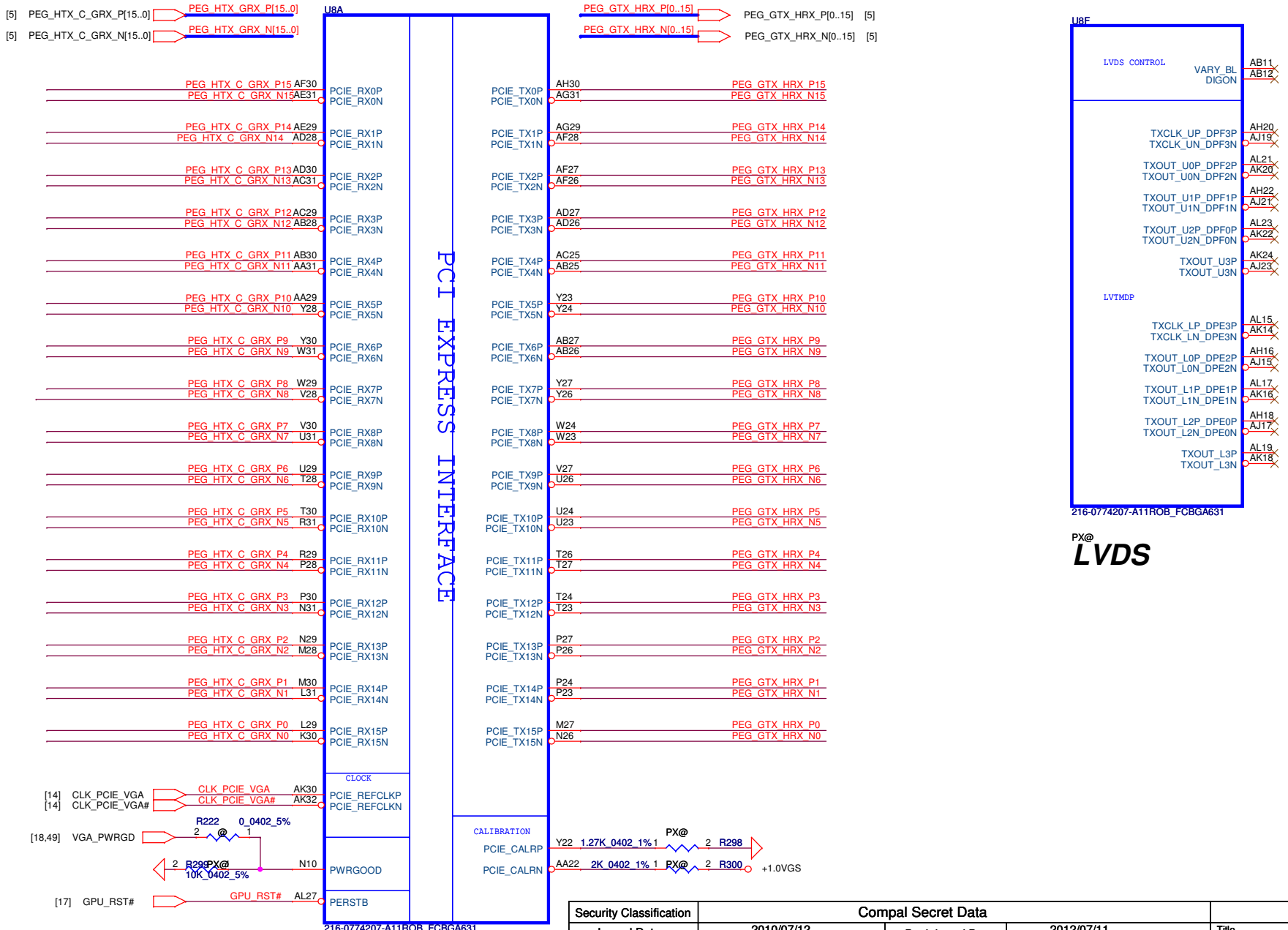
Compal Electronics, Inc.

Title: **PCH (9/9) VSS**

Size: Custom | Document Number: **Sherry and Royal** | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 21 of 55



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title: SeymourXT-S3 PCIE/LVDS
				Size: B; Document Number; Rev: 0.1
				Date: Thursday, February 02, 2012; Sheet 22 of 55

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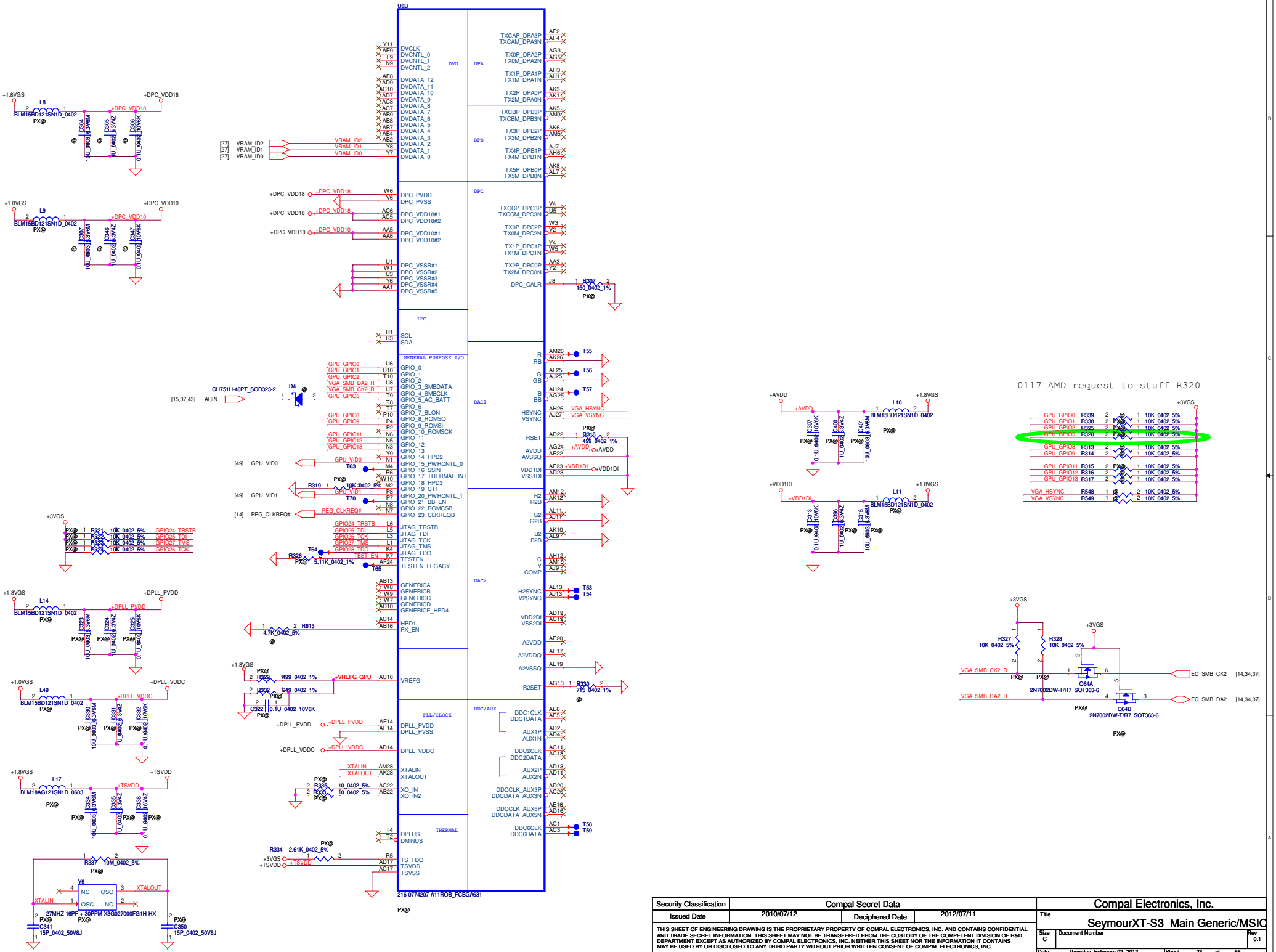

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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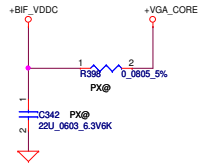
Compal Electronics, Inc.

Title: SeymourXT-S3 Main Generic/MSIC

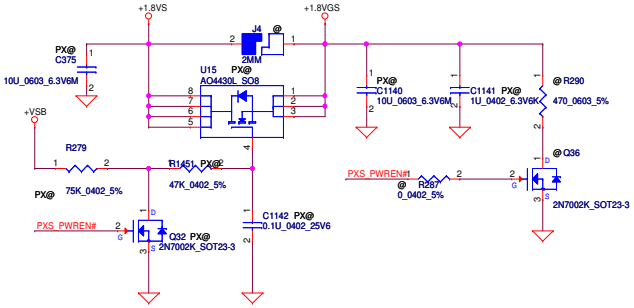
Size: C | Document Number | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 23 of 55

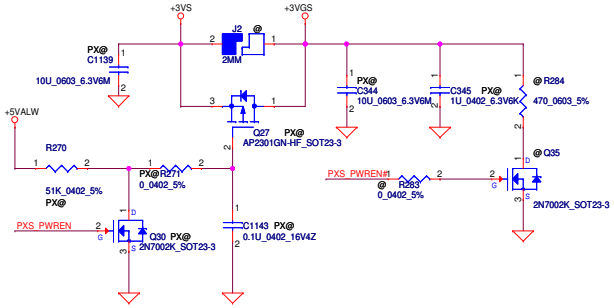
55mA@1.0V, in BACO mode

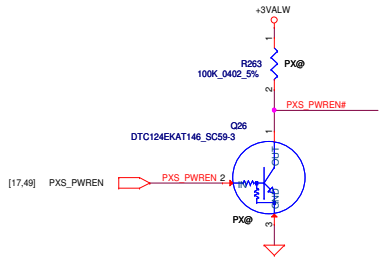


+1.8VS TO +1.8VGS

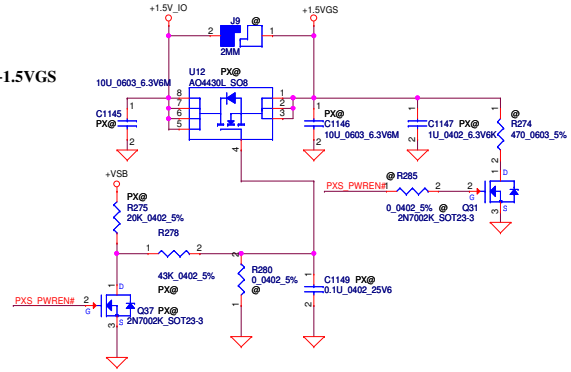


+3.3VS TO +3.3VGS





+1.5V TO +1.5VGS



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/10/12	Deciphered Date	2013/10/12	Title: SeymourXT_S3_BACO POWER
				Size: C; Document Number: Sherry and Royal; Rev: 0.1
				Date: Thursday, February 02, 2012; Sheet 24 of 55

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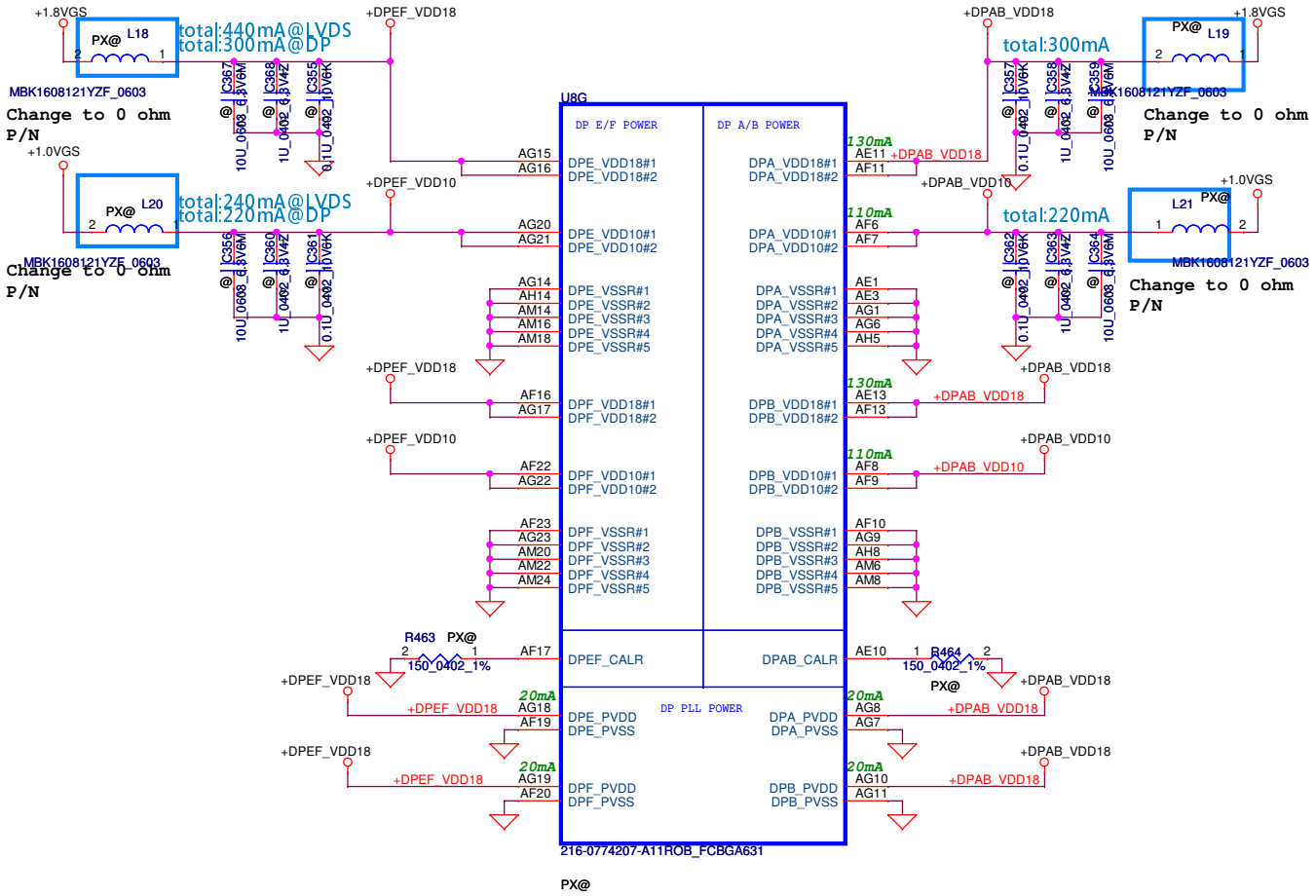

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title: SeymourXT-S3 DP PWR
				Size: B; Document Number; Rev: 0.1
				Date: Thursday, February 02, 2012; Sheet 25 of 55

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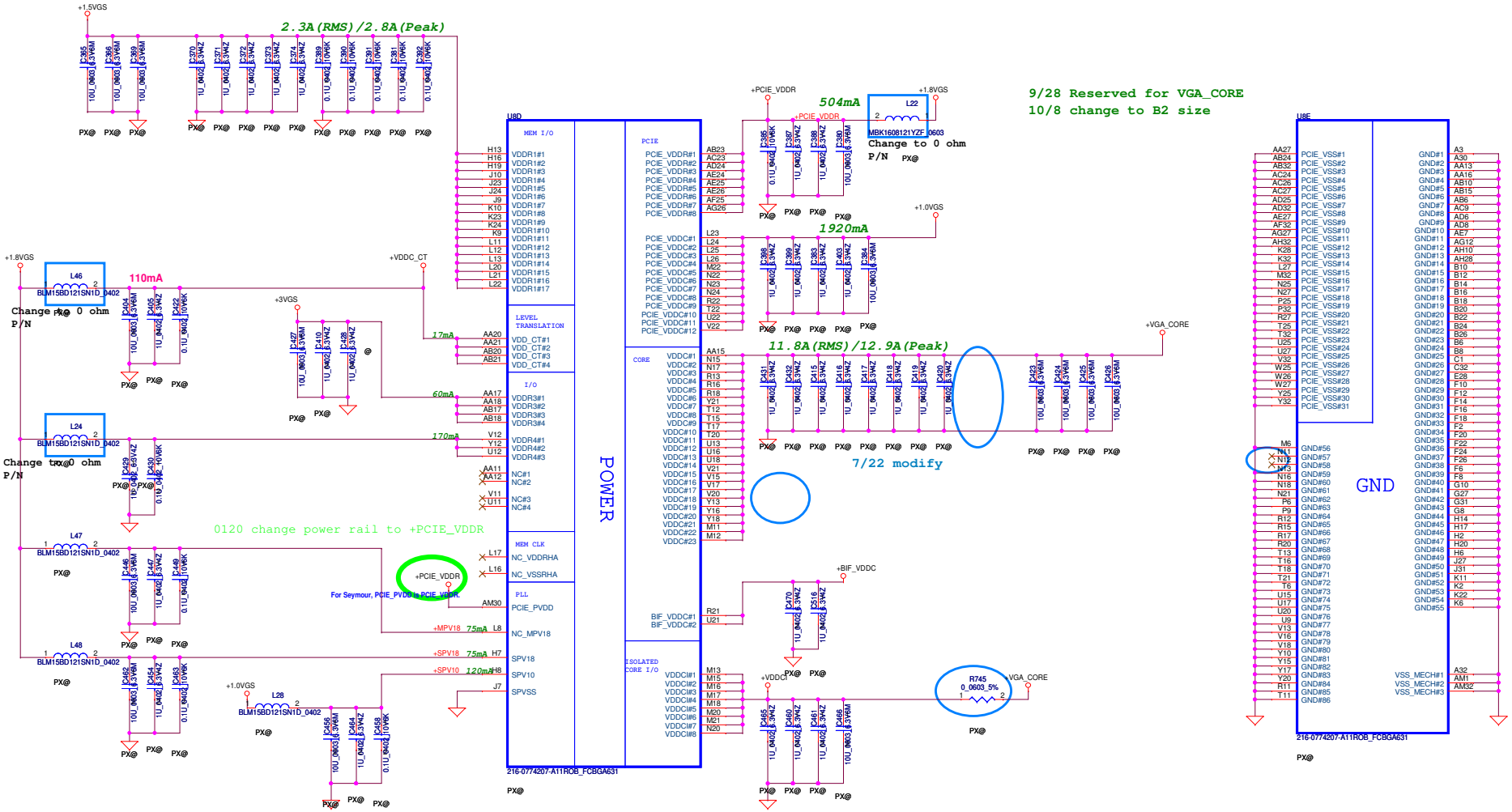

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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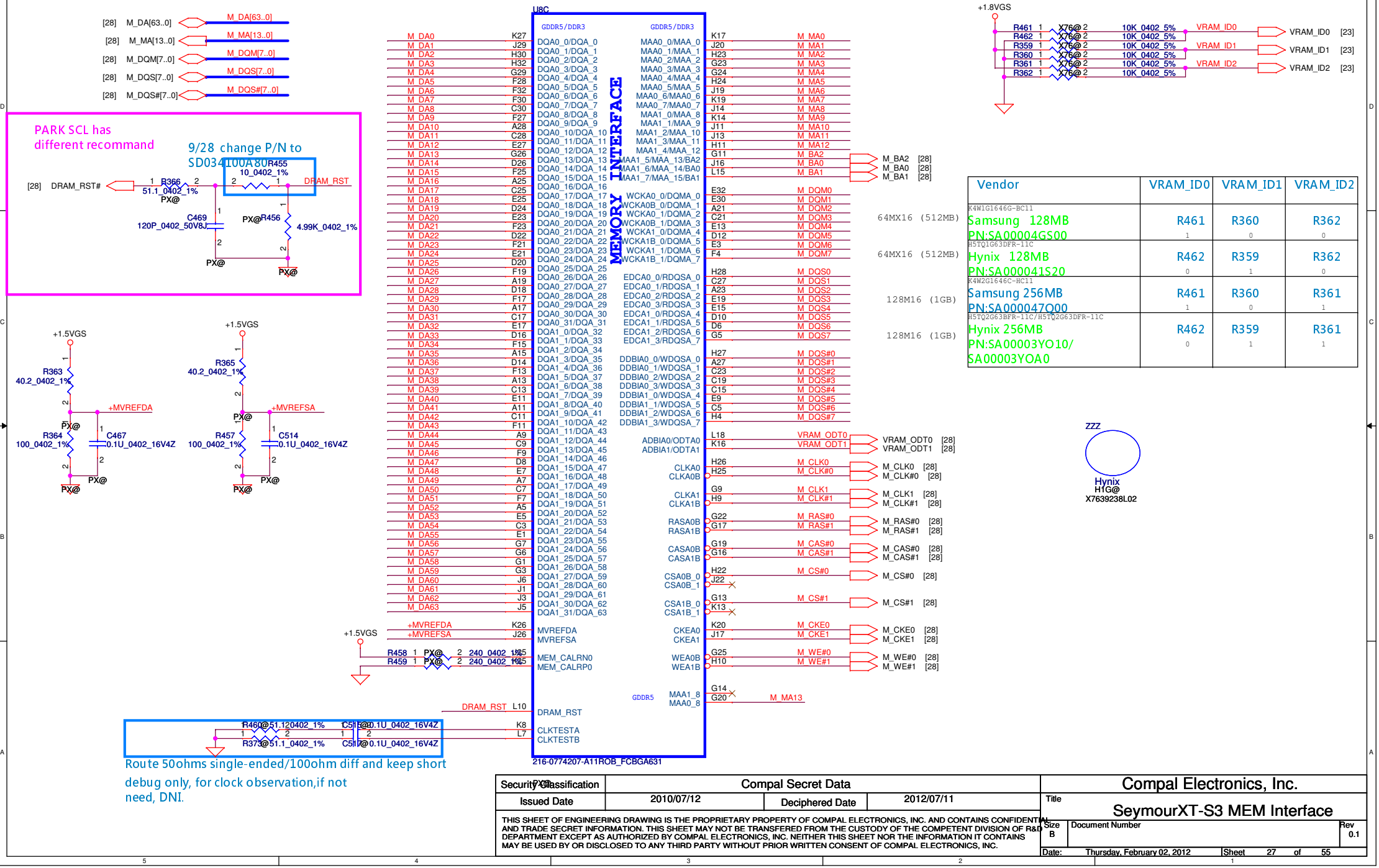
Compal Electronics, Inc.

Title: SeymourXT-S3 PWR/GND

Size: C | Document Number | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 26 of 55



Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
K4W1G1646G-BC11 Samsung 128MB PN:SA00004GS00	R461 1	R360 0	R362 0
H5TQ1G63DFR-11C Hynix 128MB PN:SA000041S20	R462 0	R359 1	R362 0
K4W2G1646C-HC11 Samsung 256MB PN:SA000047Q00	R461 1	R360 0	R361 1
H5TQ2G63BFR-11C/H5TQ2G63DFR-11C Hynix 256MB PN:SA00003YO10/ SA00003YOA0	R462 0	R359 1	R361 1

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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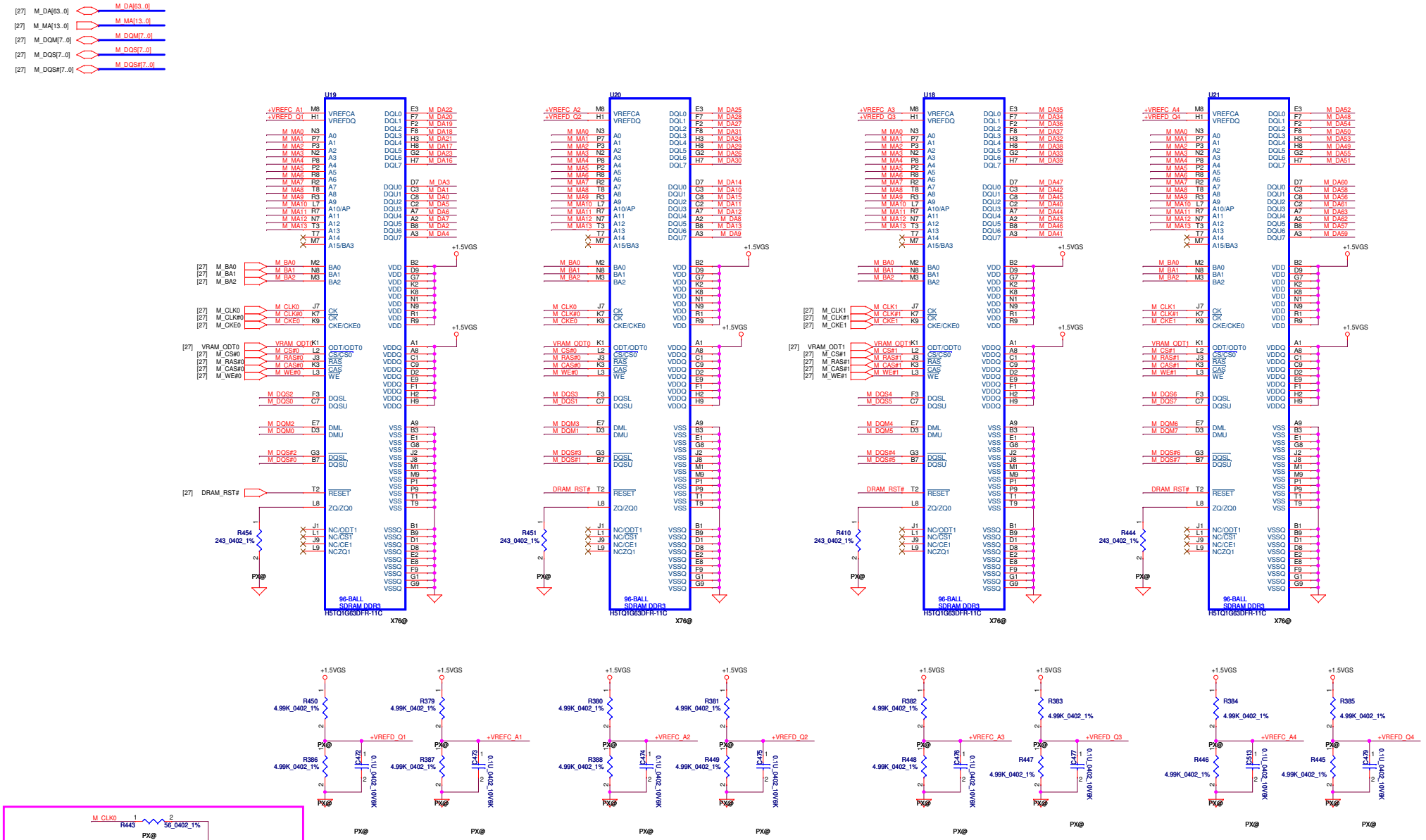
Compal Electronics, Inc.

Title: SeymourXT-S3 MEM Interface

Size: B | Document Number | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 27 of 55



ref 139-02 recommand
add off page
Park SCL recommand pu 60.4 ohm
to +1.5VGS
0619 update

VRAM P/N :
Hynix : SA000041S10 (S IC D3 64MX16 H5TQ1G63BFR-11C FBGA C38!)
Samsung : SA000041T10 (S IC D3 64MX16 K4W1G1646E-HC11 FBGA C38!)
update VRAM PN 0619 update

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/07/12	Deciphered Date	2012/07/11	Title: SeymourXT-S3 VRAM
				Size: C; Document Number: ; Rev: 0.1
				Date: Thursday, February 02, 2012; Sheet 28 of 55

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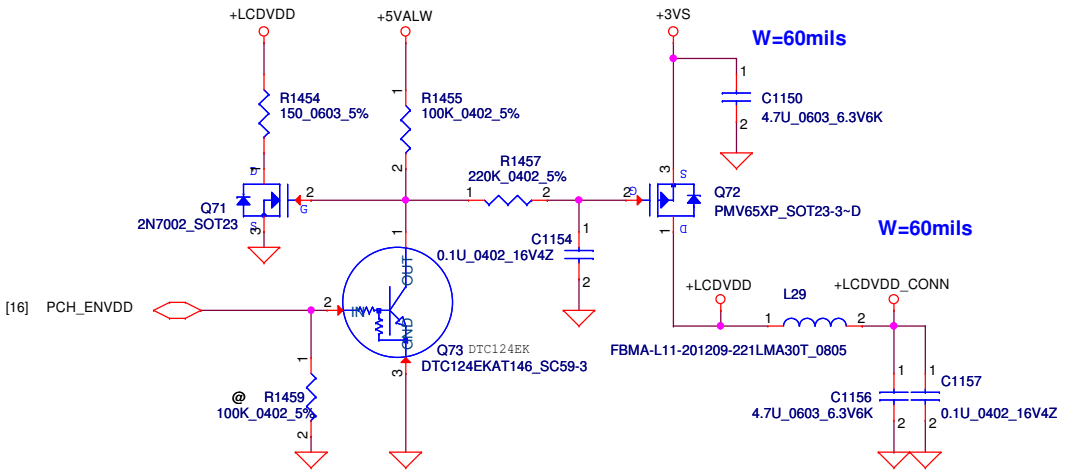
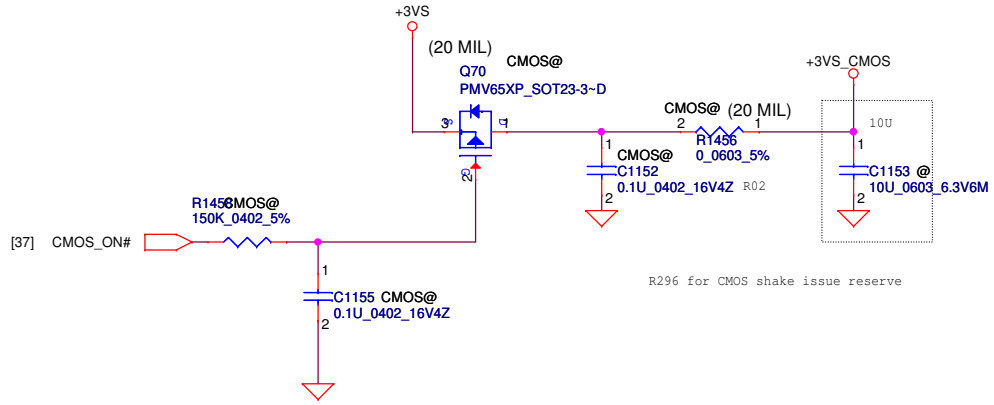
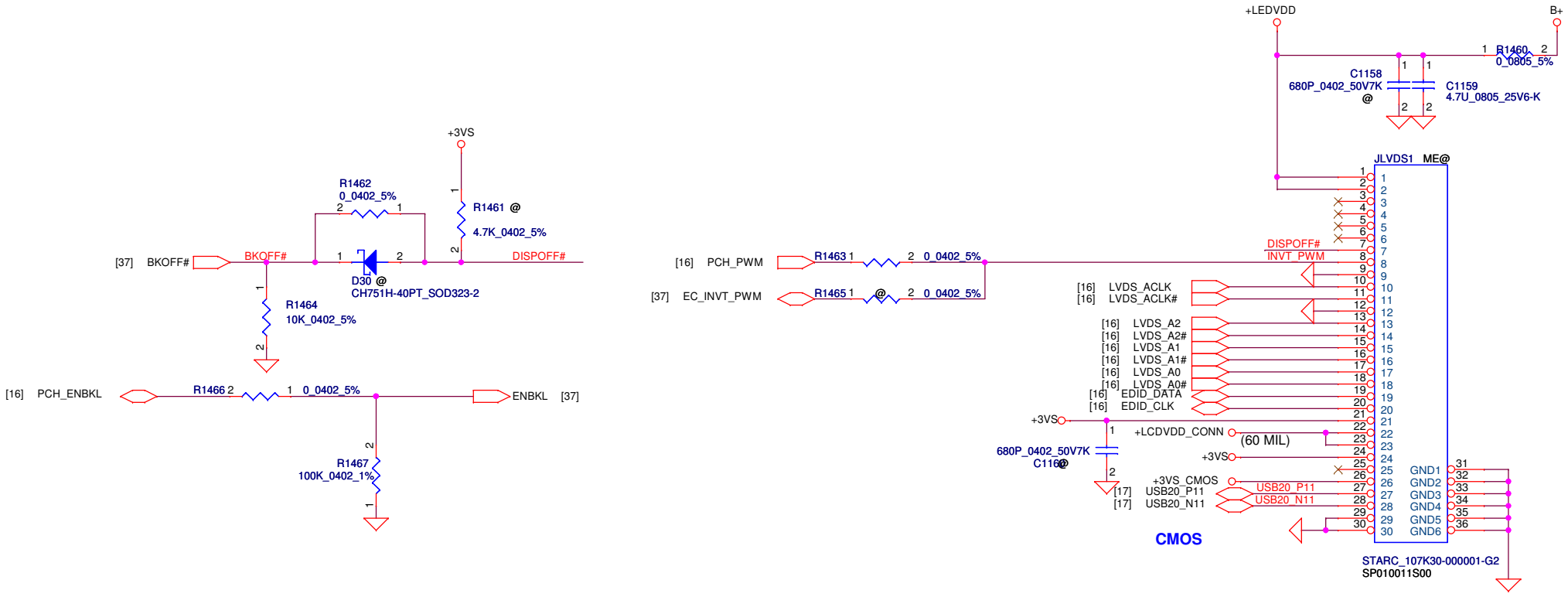
LCD POWER CIRCUIT



CMOS Camera



VGA LCD/PANEL BD. Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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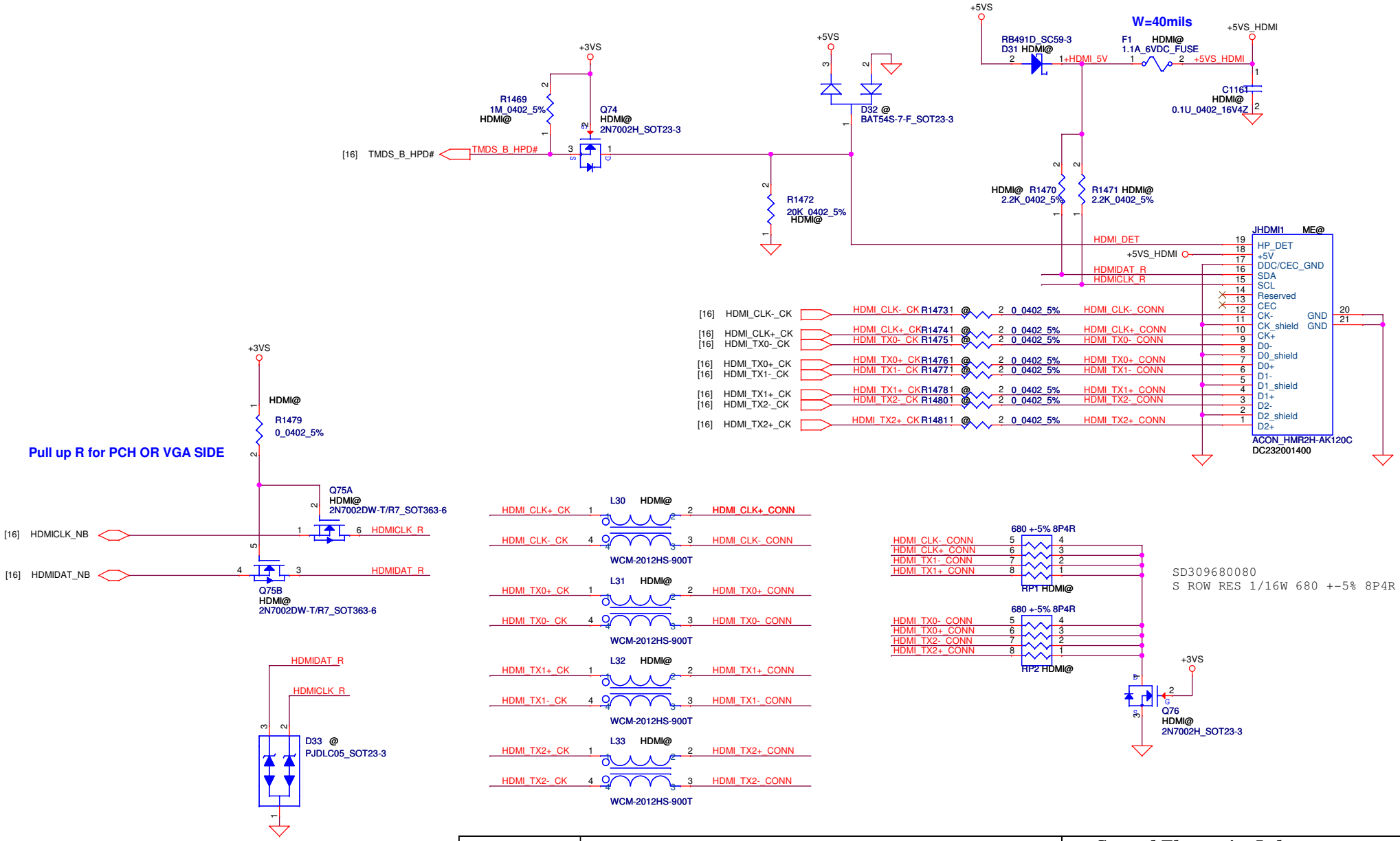
Compal Electronics, Inc.

Title: **LVDS/CAMERA**

Size: Custom | Document Number: **Sherry and Royal** | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 29 of 55



SD309680080
S ROW RES 1/16W 680 +-5% 8P4R

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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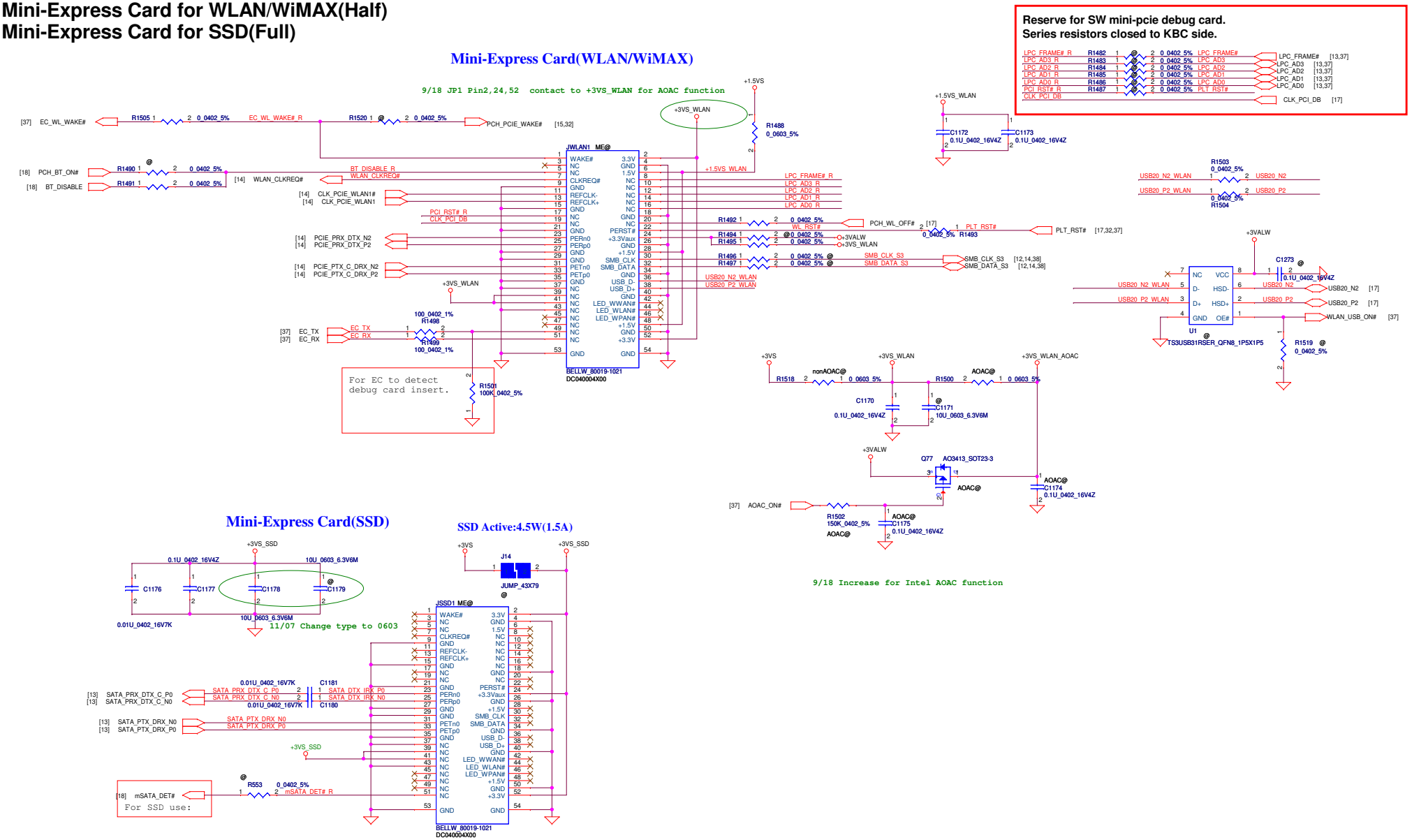
Compal Electronics,Ltd.

Title: **HDMI CONN**

Size: B | Document Number: **Sherry and Royal** | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 30 of 55

Mini-Express Card for WLAN/WiMAX(Half)
Mini-Express Card for SSD(Full)



Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

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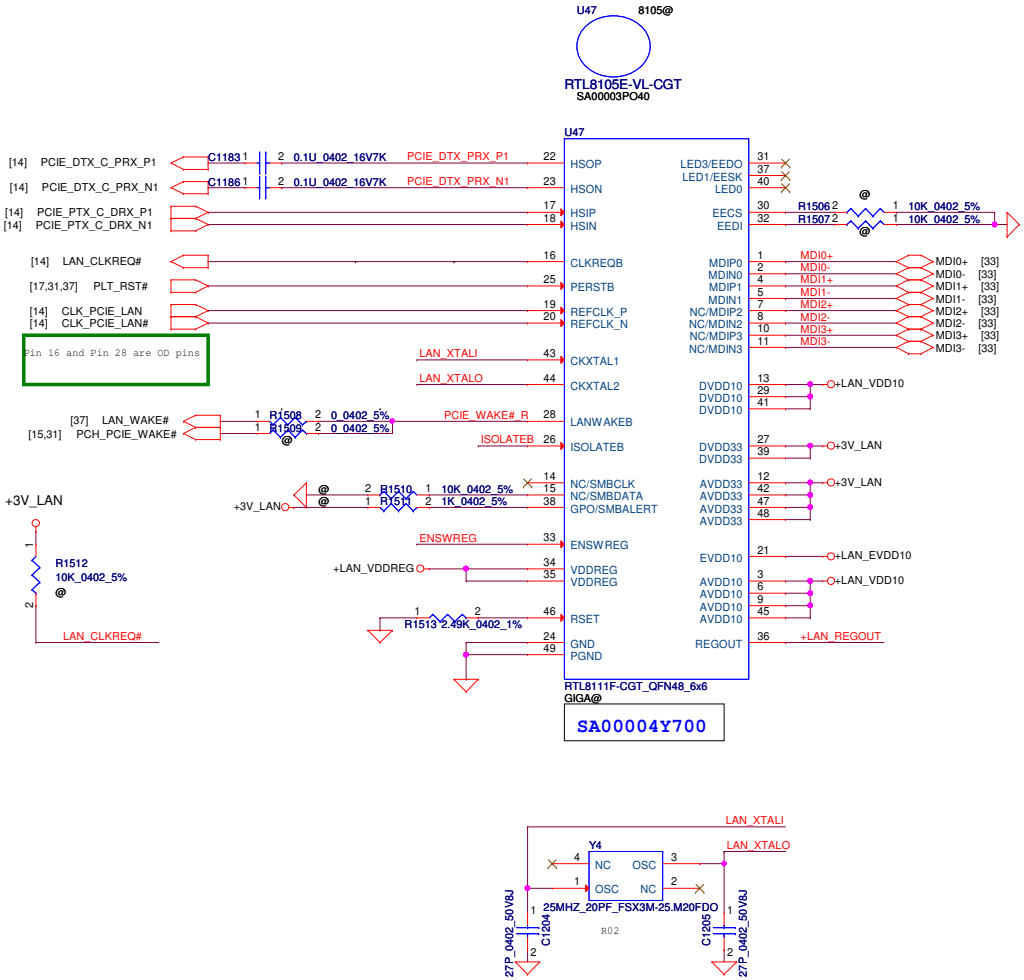
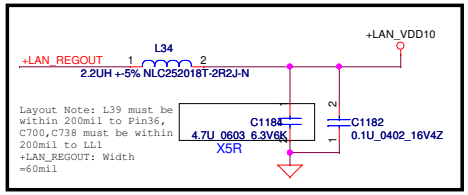
Compal Electronics, Inc.

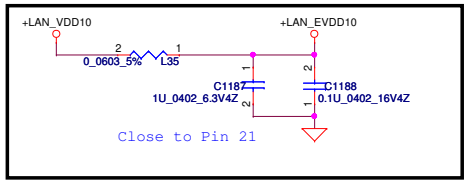
Title: **Mini-Card**

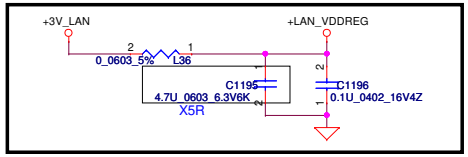
Size | Document Number: **Sherry and Royal** | Rev: 0.1

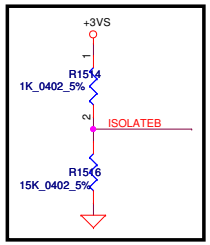
Date: Thursday, February 02, 2012 | Sheet 31 of 55

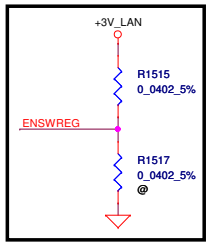






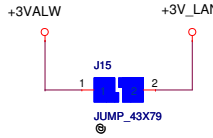






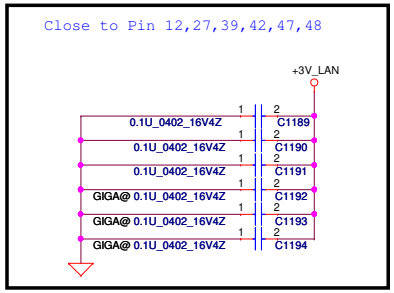
H: Enable internal Regular
L: Disable

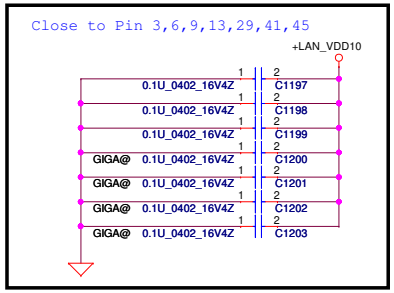
Layout Notice : Place as close chip as possible.



Layout Notice : Place as close chip as possible.

Rising time (10%~90%)1mS <Rising time <100mS





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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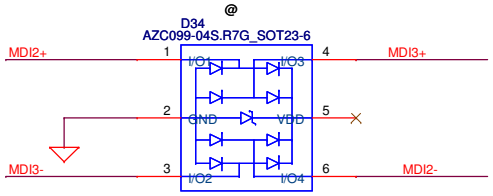
Compal Electronics, Inc.

Title: LAN-RTL8111F/8105E

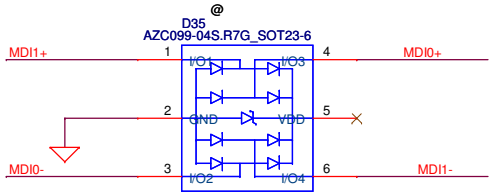
Size: Custom | Document Number: Sherry and Royal | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 32 of 55

Reserve gas tube for EMI go rural solution

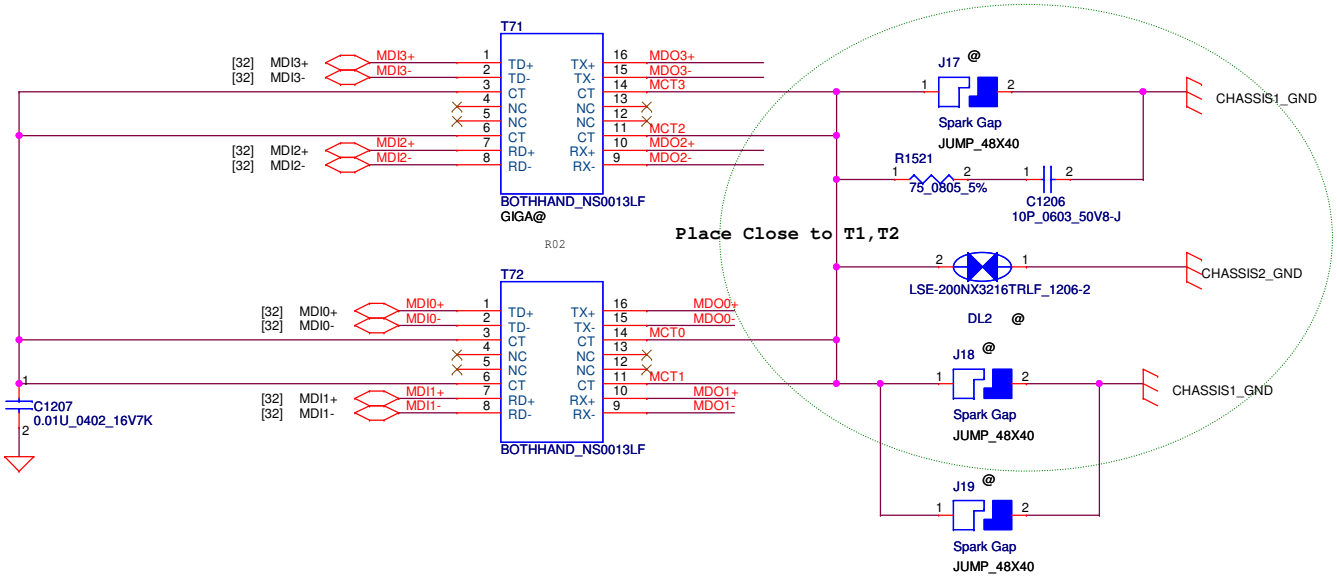


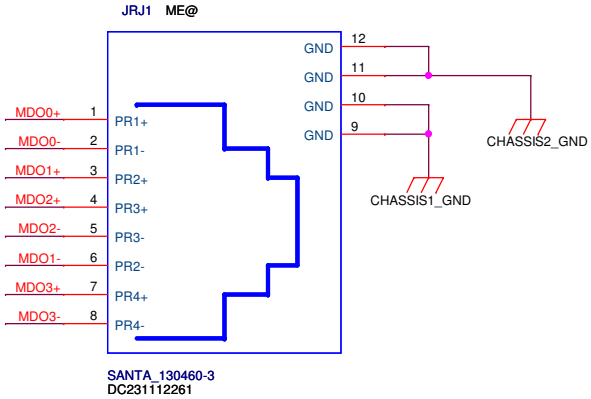
Place Close to T71



Place Close to T72

D34/D35
1'S PN:SC300001G00
2'S PN:SC300002E00





Reserve for EMI go rural solution

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title: LAN_Transformer
				Size: B; Document Number: Sherry and Royal; Rev: 0.1
				Date: Thursday, February 02, 2012; Sheet 33 of 55

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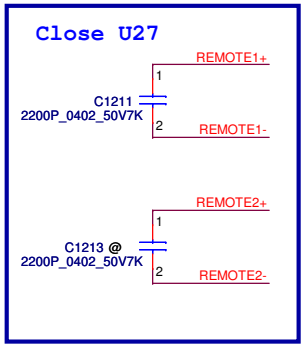
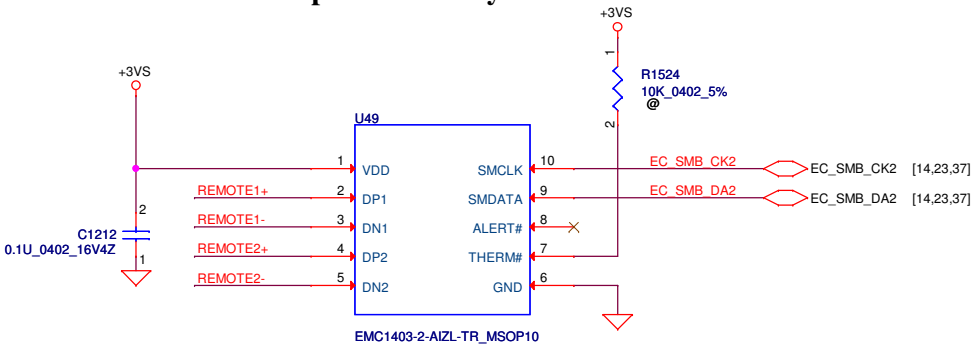
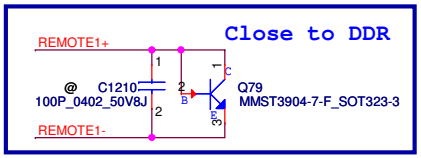
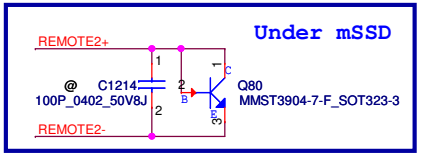
SMSC thermal sensor placed near by VRAM





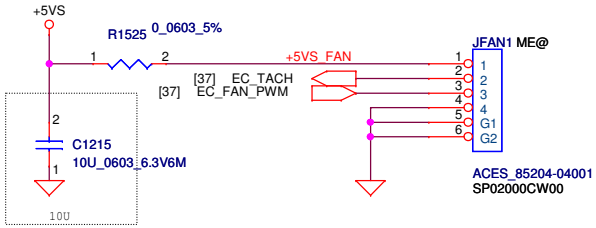
Address 1001_101xb



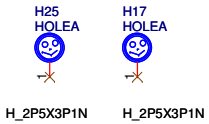


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn

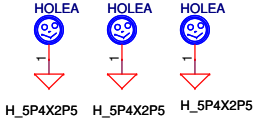


R



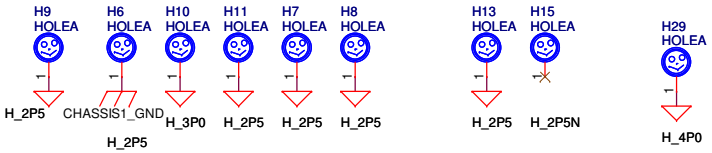
E

R



M/B 橢圓孔

M/B KB 橢圓孔

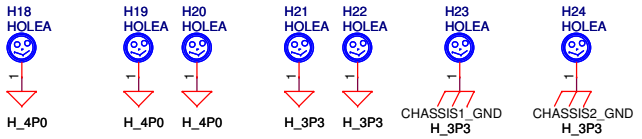


A

2P5 * 9 pcd

F

G



B CPU

C GPU

D LAN

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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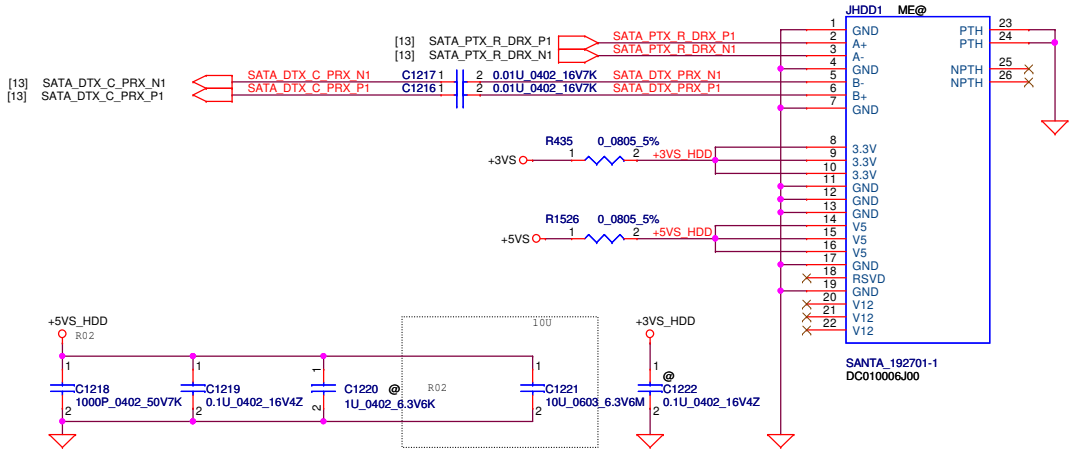
Compal Electronics,Ltd.

Title: **Fintek-Thermal IC/FAN/screw**

Size: B | Document Number: **Sherry and Royal** | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 34 of 55

SATA HDD Conn.



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title: HDD/ODD/BT Connector
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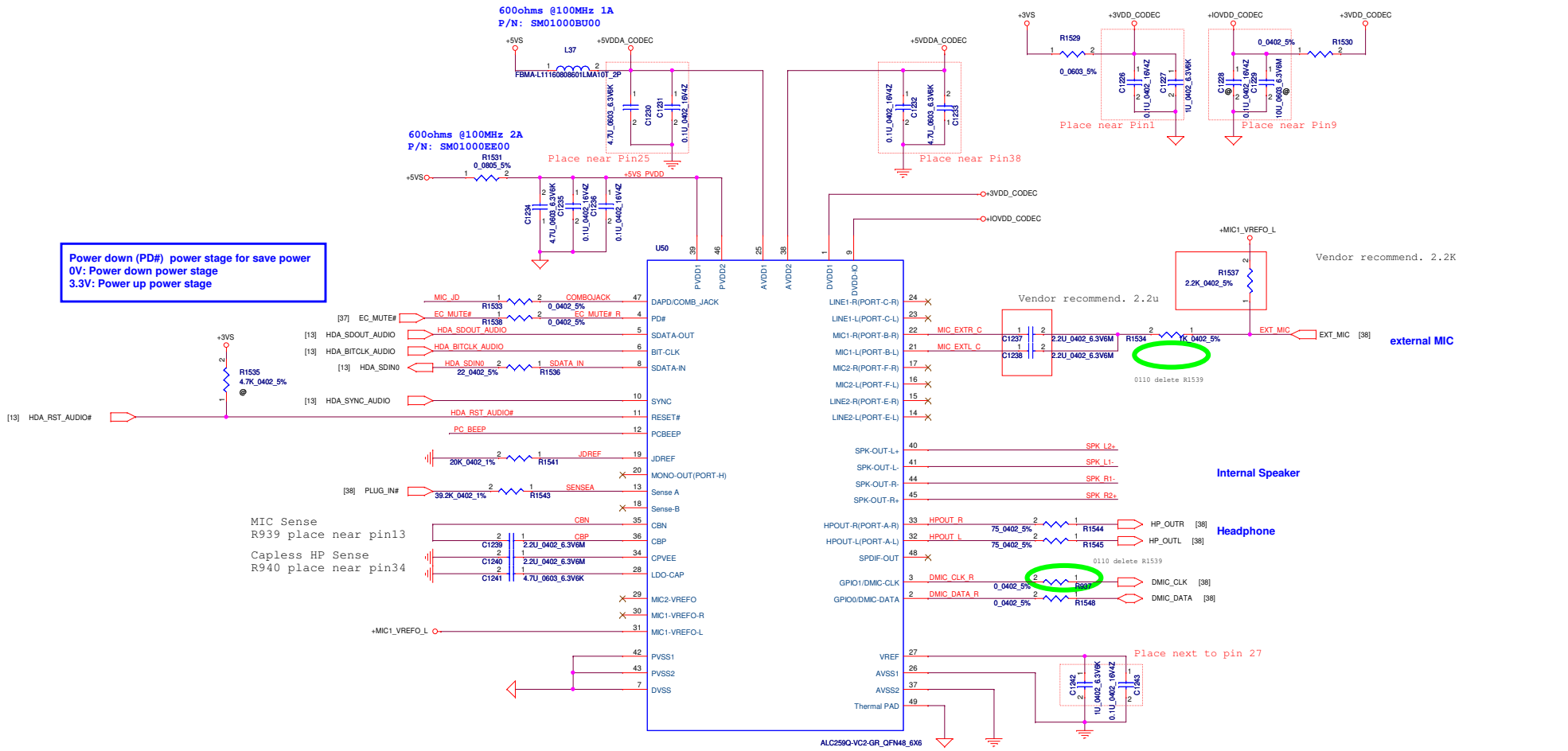
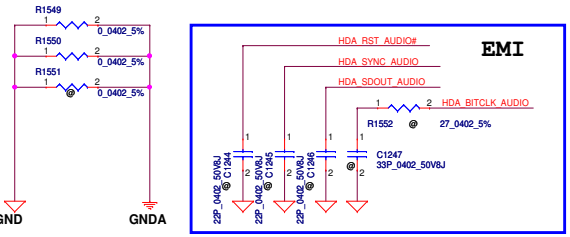
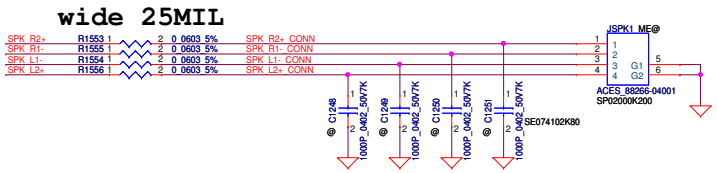
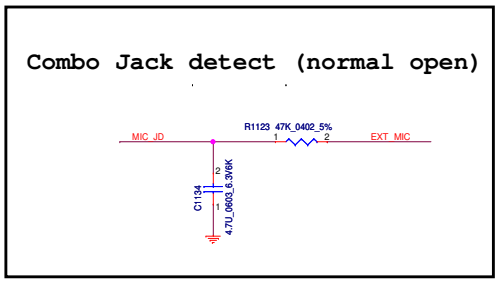
				Date: Thursday, February 02, 2012; Sheet 35 of 55

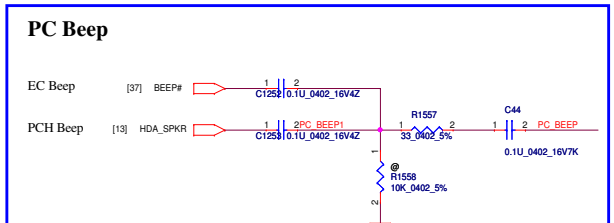


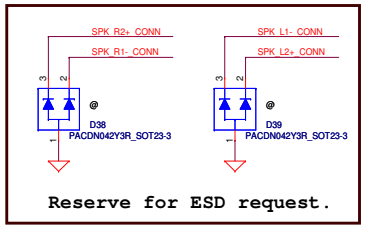
Pin Assignment	Location	Function
SPK-OUT (Pin40/41/44/45)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
MIC1(Pin21/22)	External	Mic in











Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

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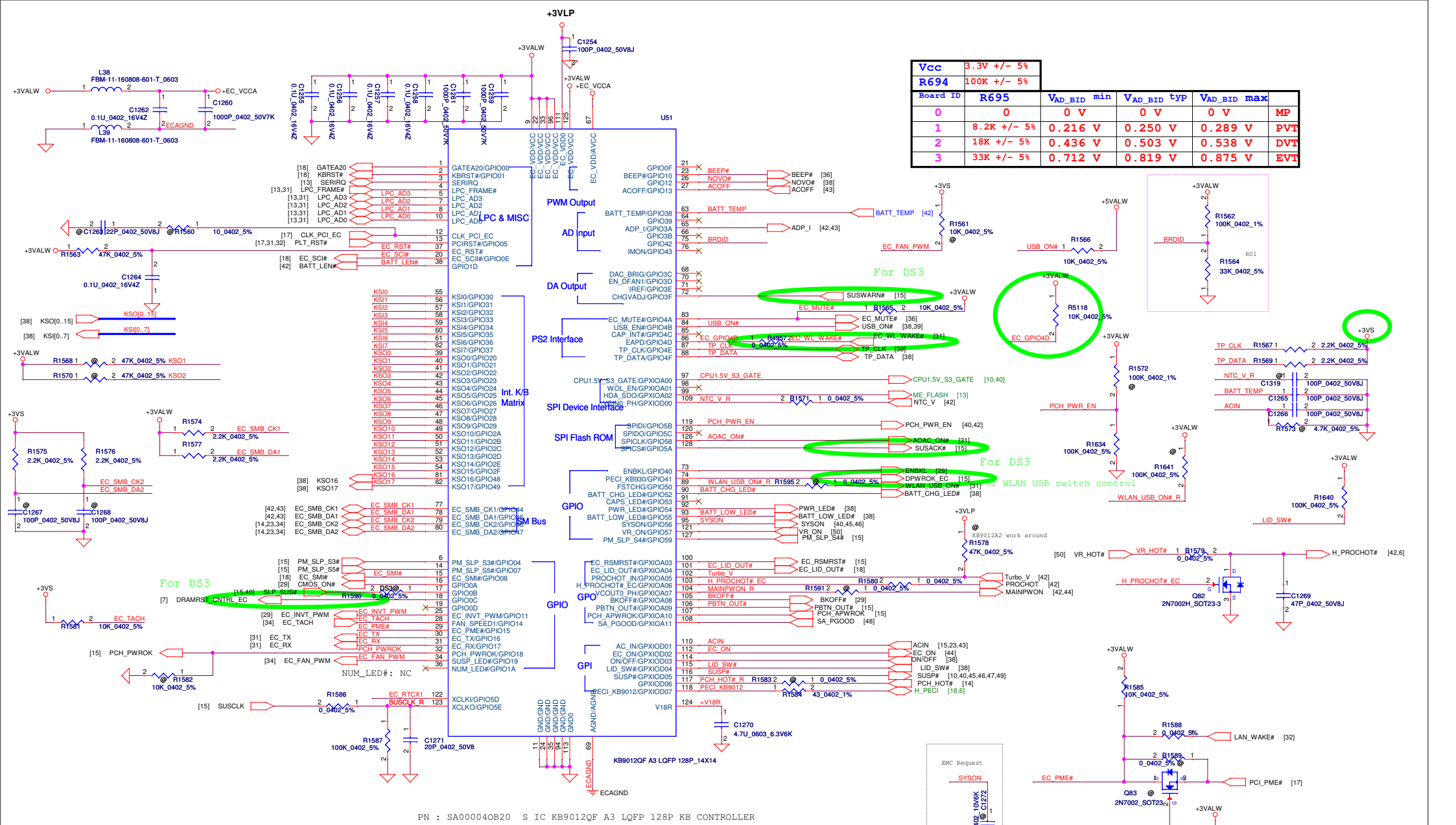
Compal Electronics,Ltd.

Title: HD Audio Codec_ALC259Q-VC

Size: C | Document Number: Sherry and Royal | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 36 of 55



Vcc	3.3V +/- 5%
R694	100K +/- 5%

Board ID	R695	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	
0	0	0 V	0 V	0 V	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	EVT

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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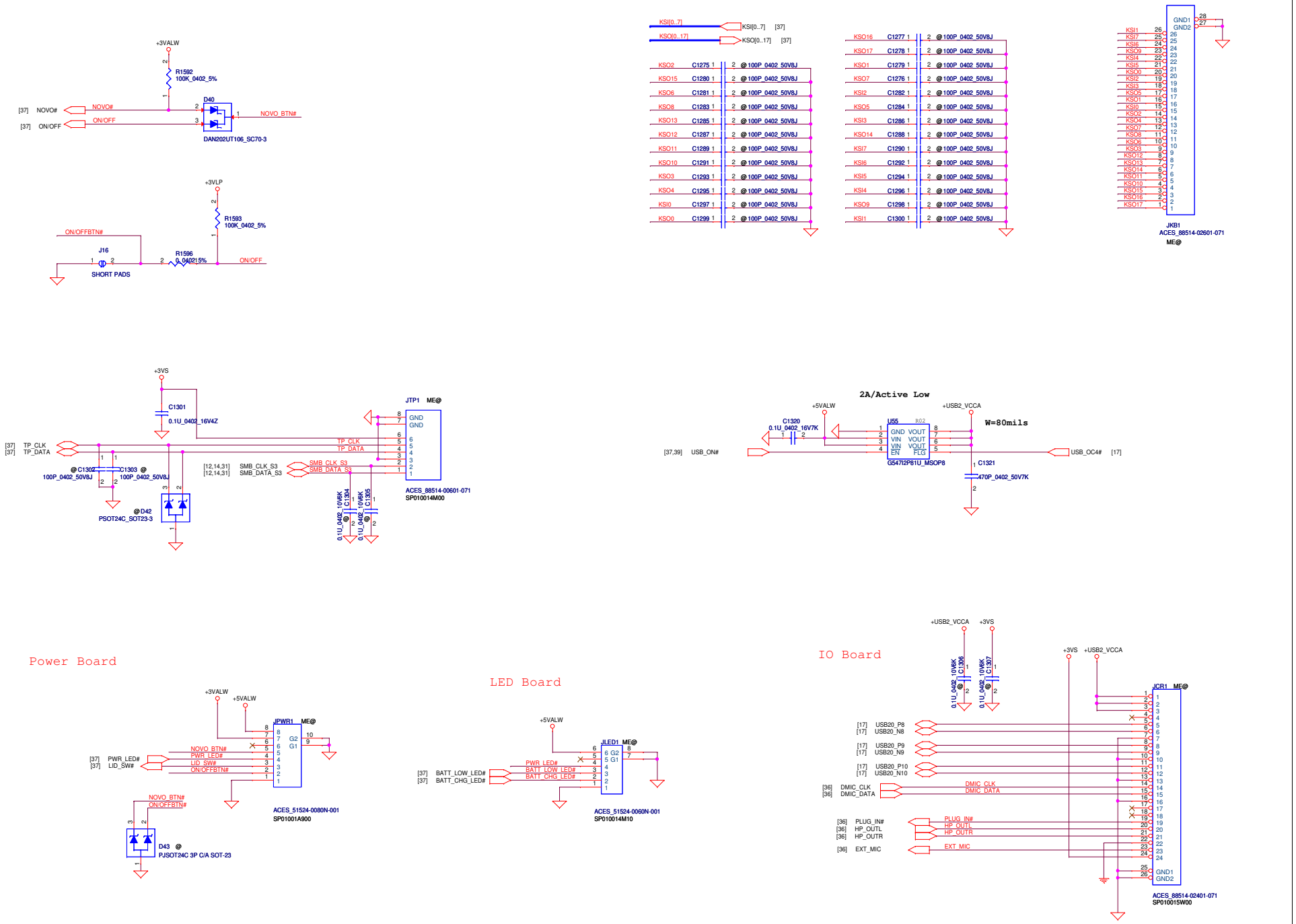
Compal Electronics, Inc.

Title: **BIOS & EC I/O Port**

Size: Custom | Document Number: **Sherry and Royal** | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 37 of 55



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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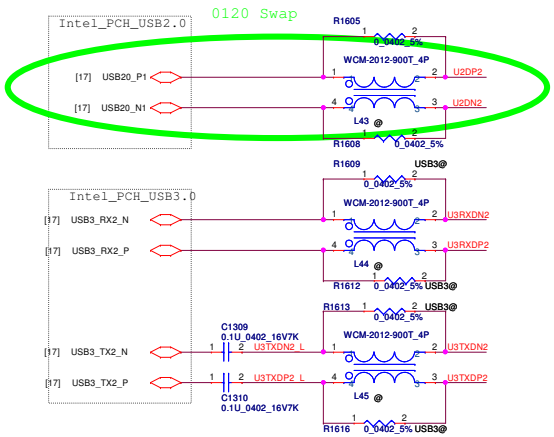
Compal Electronics, Inc.

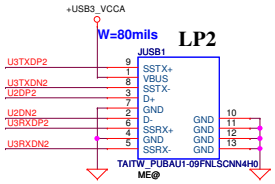
Title: **ROM/KBD/PWR/CR/LED/TP Conn.**

Size: C | Document Number: **Sherry and Royal** | Rev: 0.1

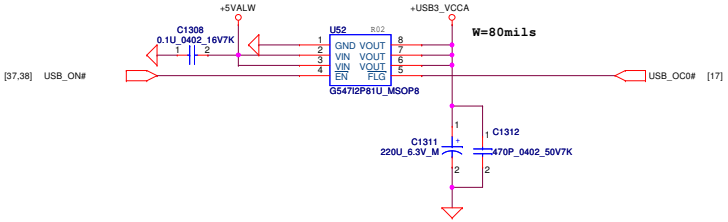
Date: Thursday, February 02, 2012 | Sheet 38 of 55

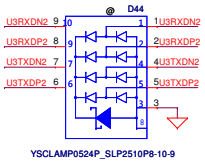


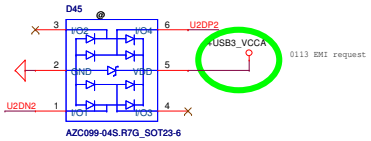
Place TX AC coupling Cap (C843~C850). Close to connector



2A/Active Low







For EMI request

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title: USB3.0/Left USB Ports

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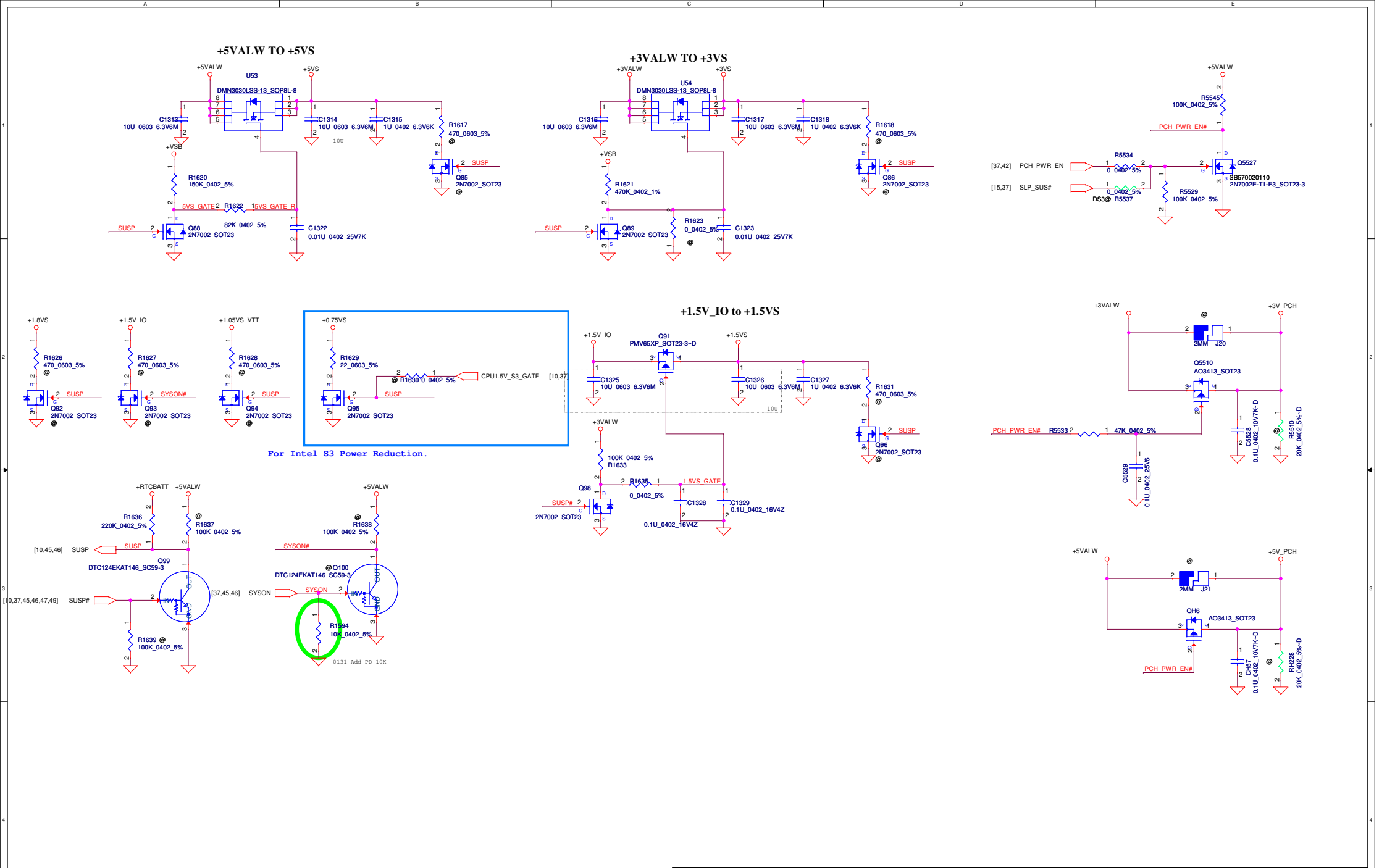
Size	Document Number	Rev
Custom		0.1

Date: Thursday, February 02, 2012 Sheet 39 of 55



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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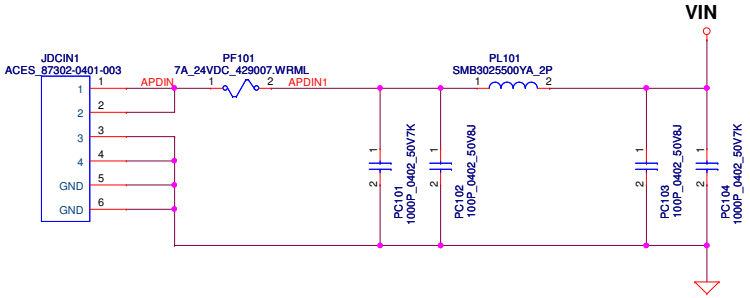
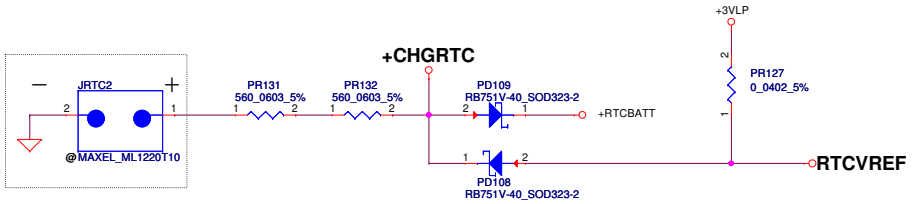
Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: Sherry and Royal | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 40 of 55





RTC Battery

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

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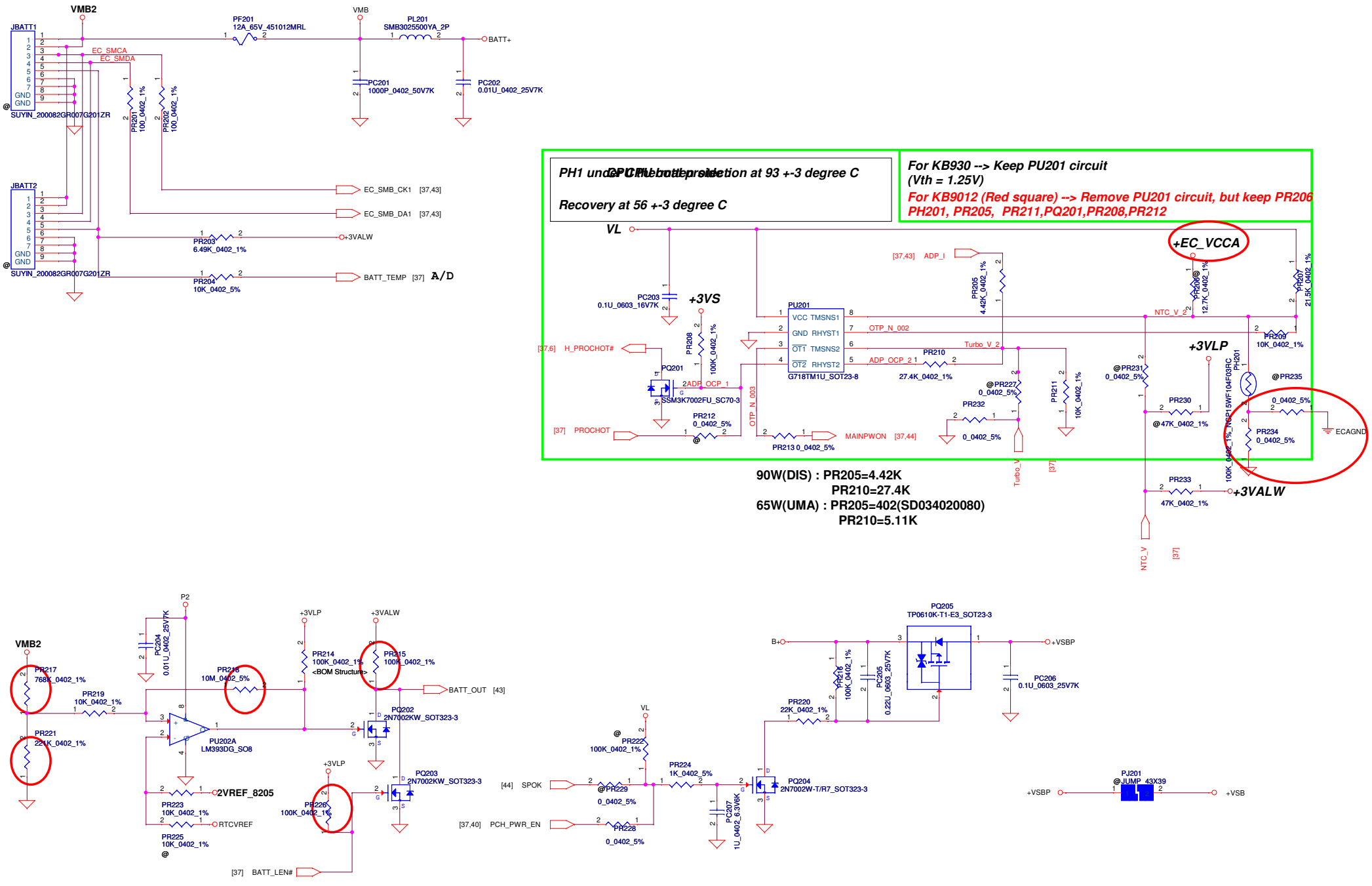
Compal Electronics, Inc.

Title: ***PWR DCIN***

Size: Custom | Document Number: **C38-G series Chief River Schematic** | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 41 of 55



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

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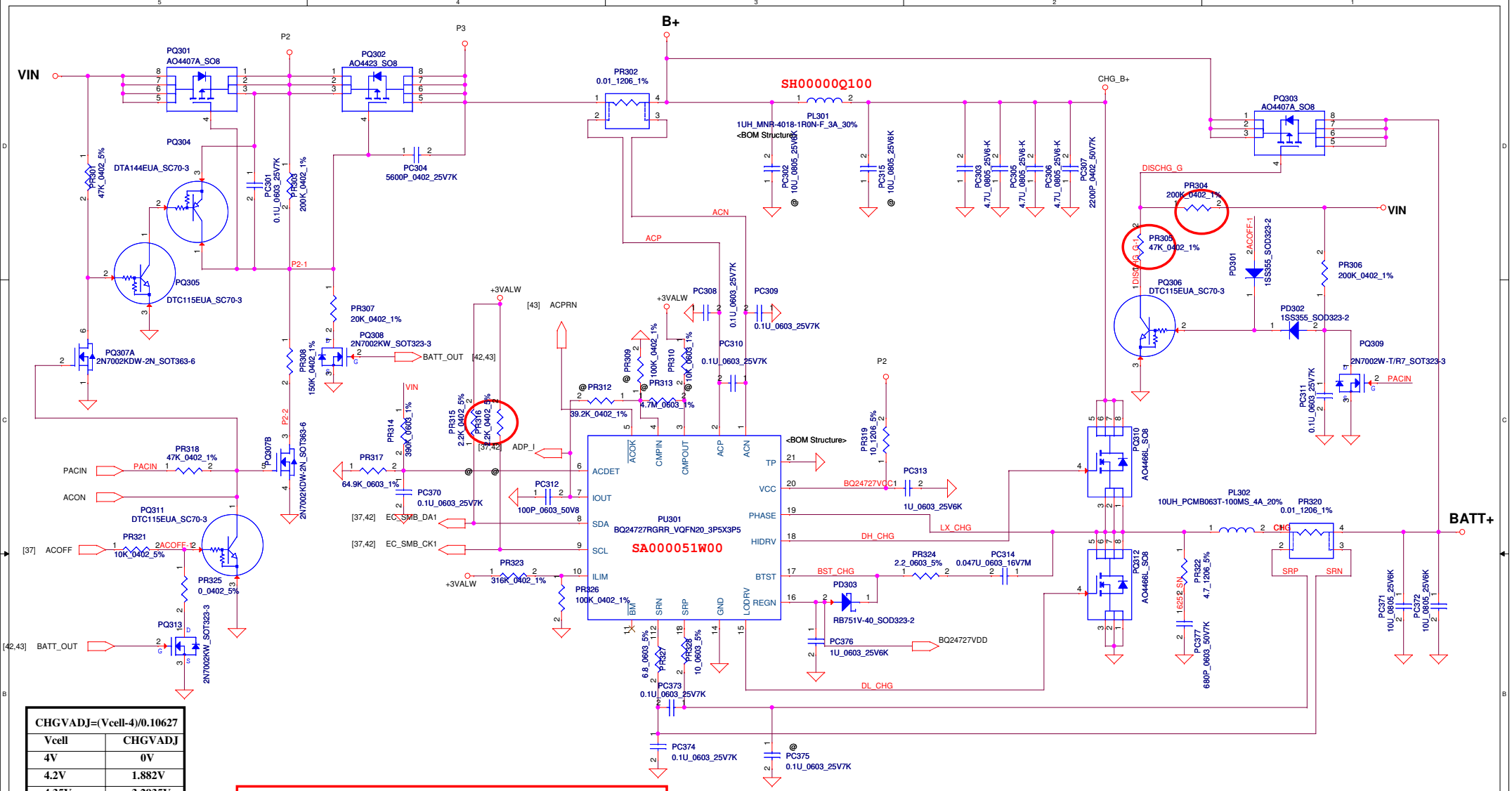
Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 42 of 55



CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2012/07/11

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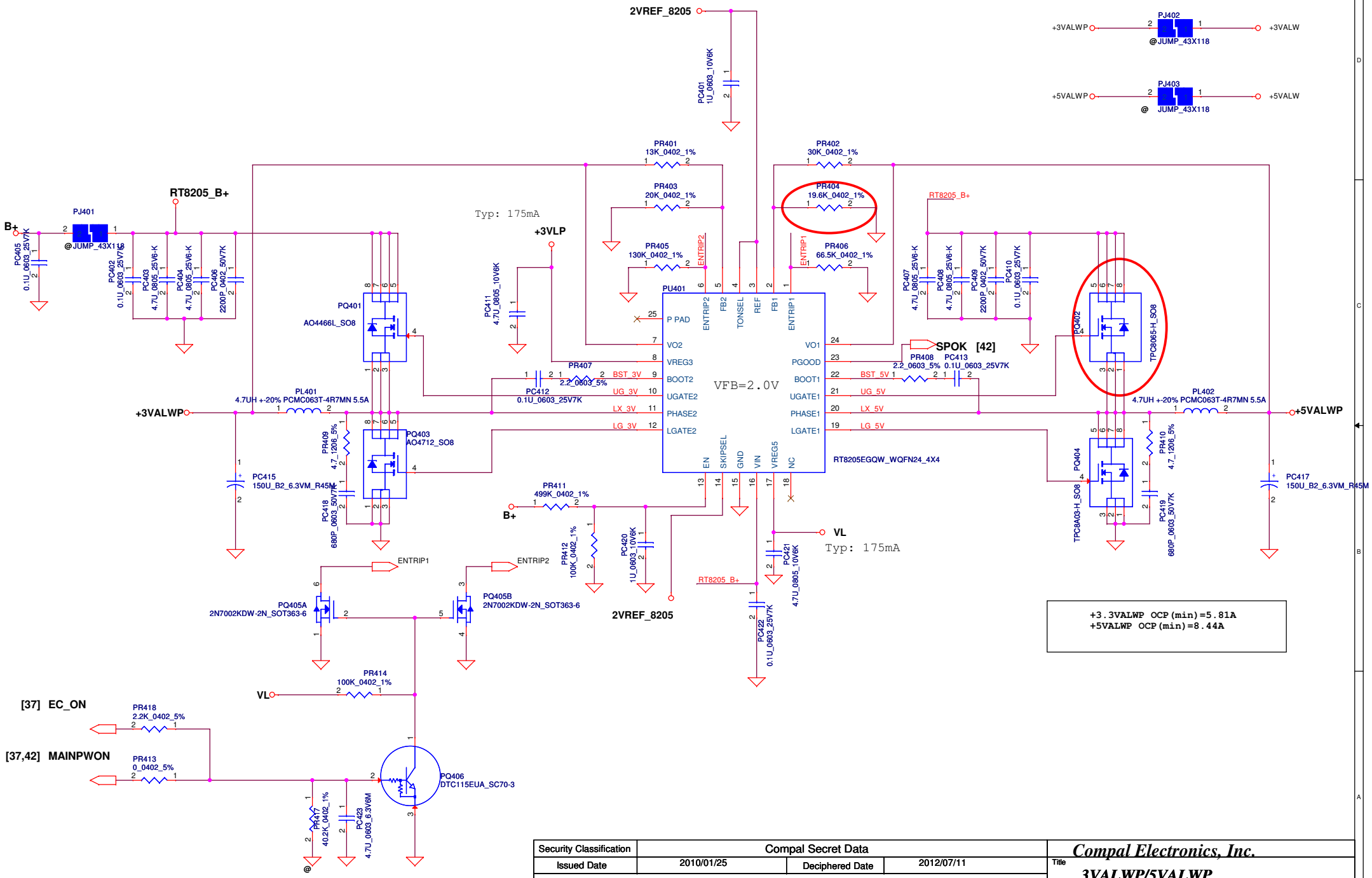
Compal Electronics, Inc.

Title: CHARGER

Size: | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 43 of 55

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

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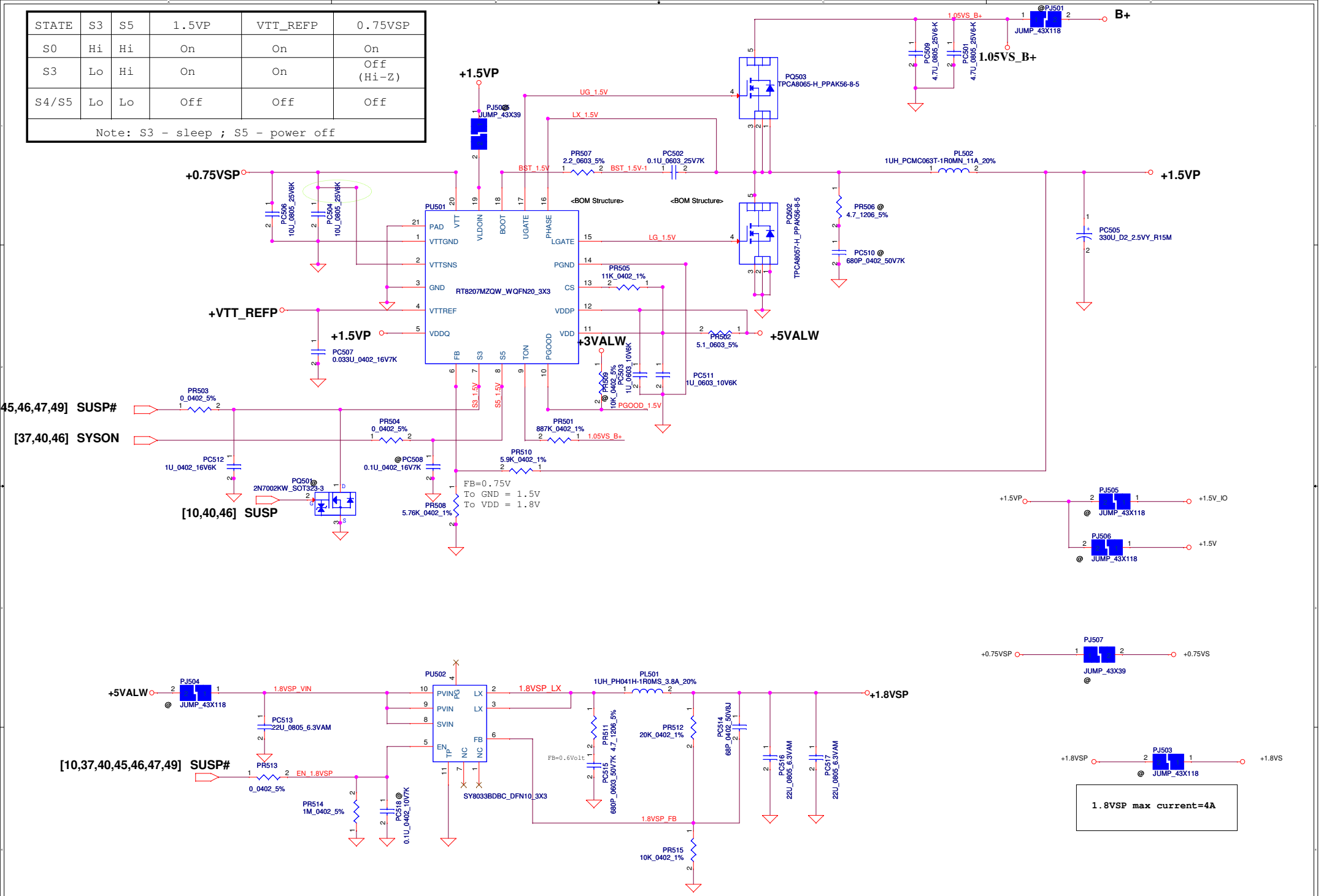
Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 44 of 55

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

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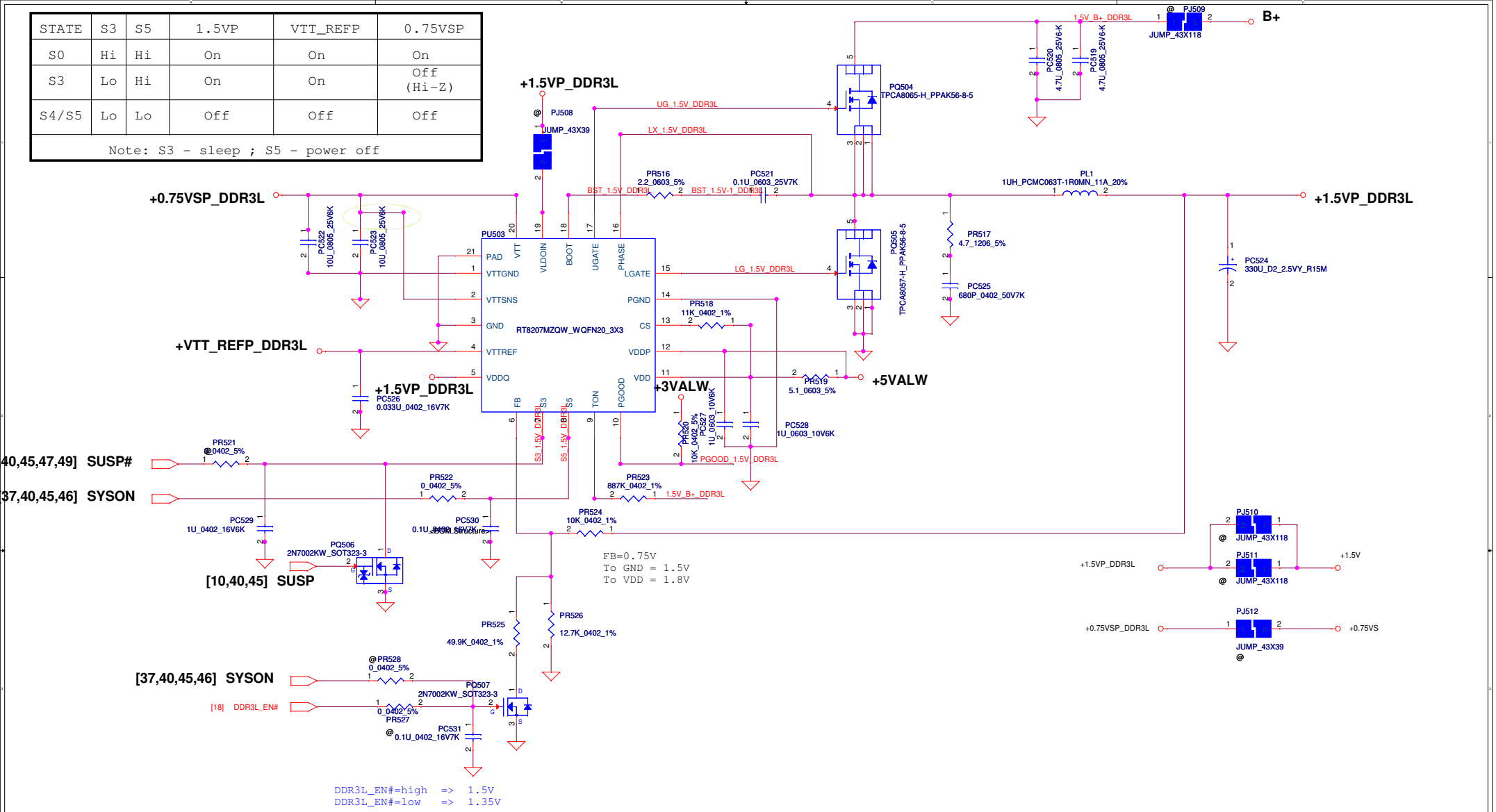
Compal Electronics, Inc.

Title: PWR-+1.5VP/+1.8VSP

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 45 of 55

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

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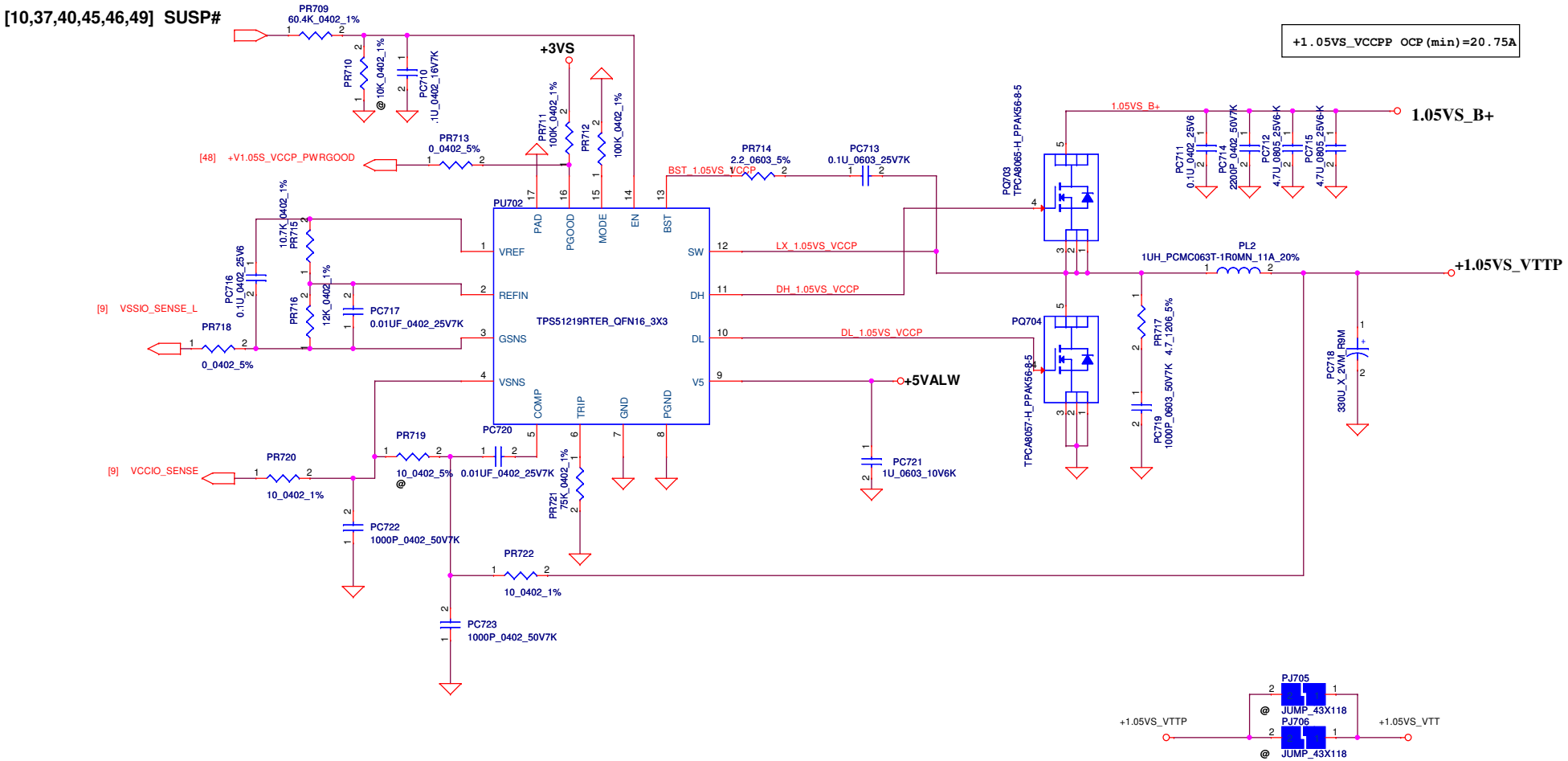
Compal Electronics, Inc.

Title: PWR-+1.5VP/+1.8VSP

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 46 of 55



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: ***PWR +1.05VS_VCCPP/***

Size: Custom | Document Number: **C38-G series Chief River Schematic** | Rev: 0.1

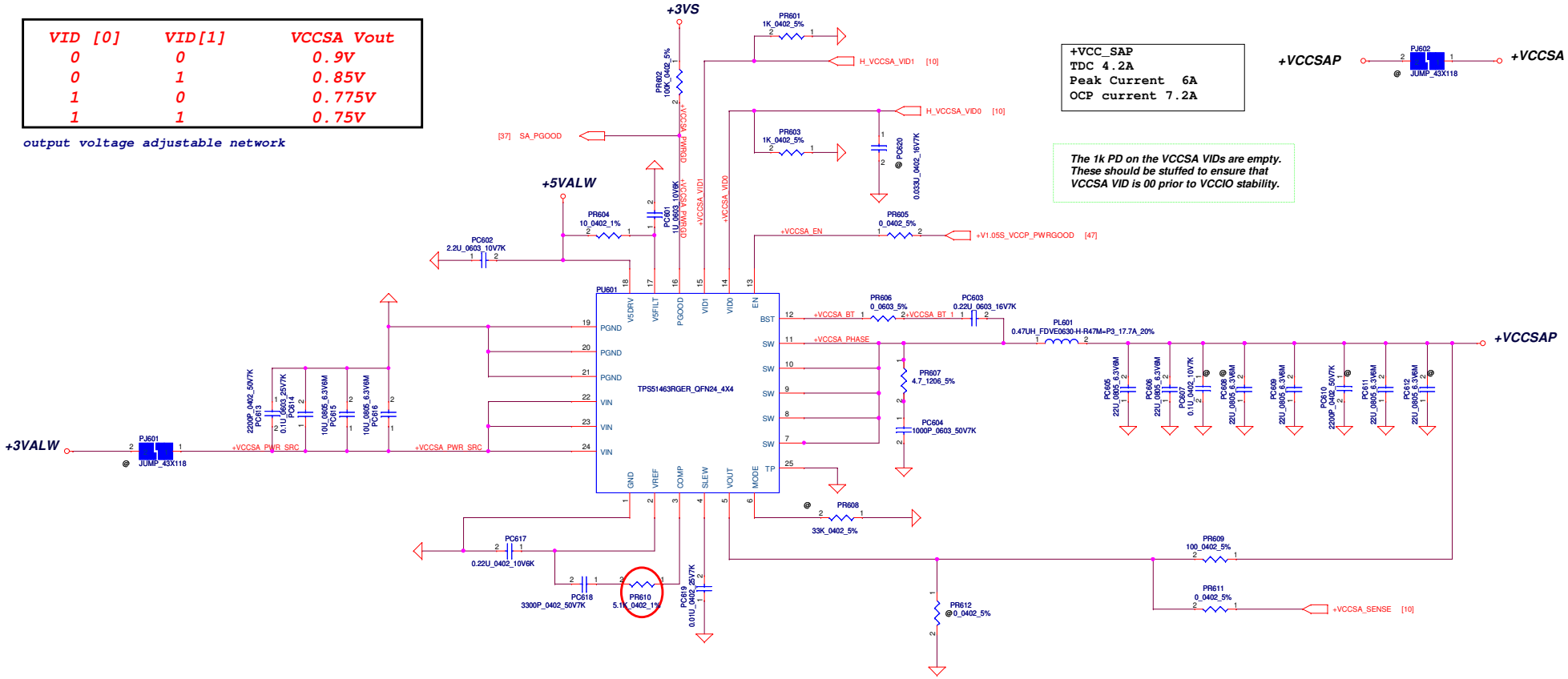
Date: Thursday, February 02, 2012 | Sheet 47 of 55

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



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Issued Date	2010/01/25	Deciphered Date	2012/07/11

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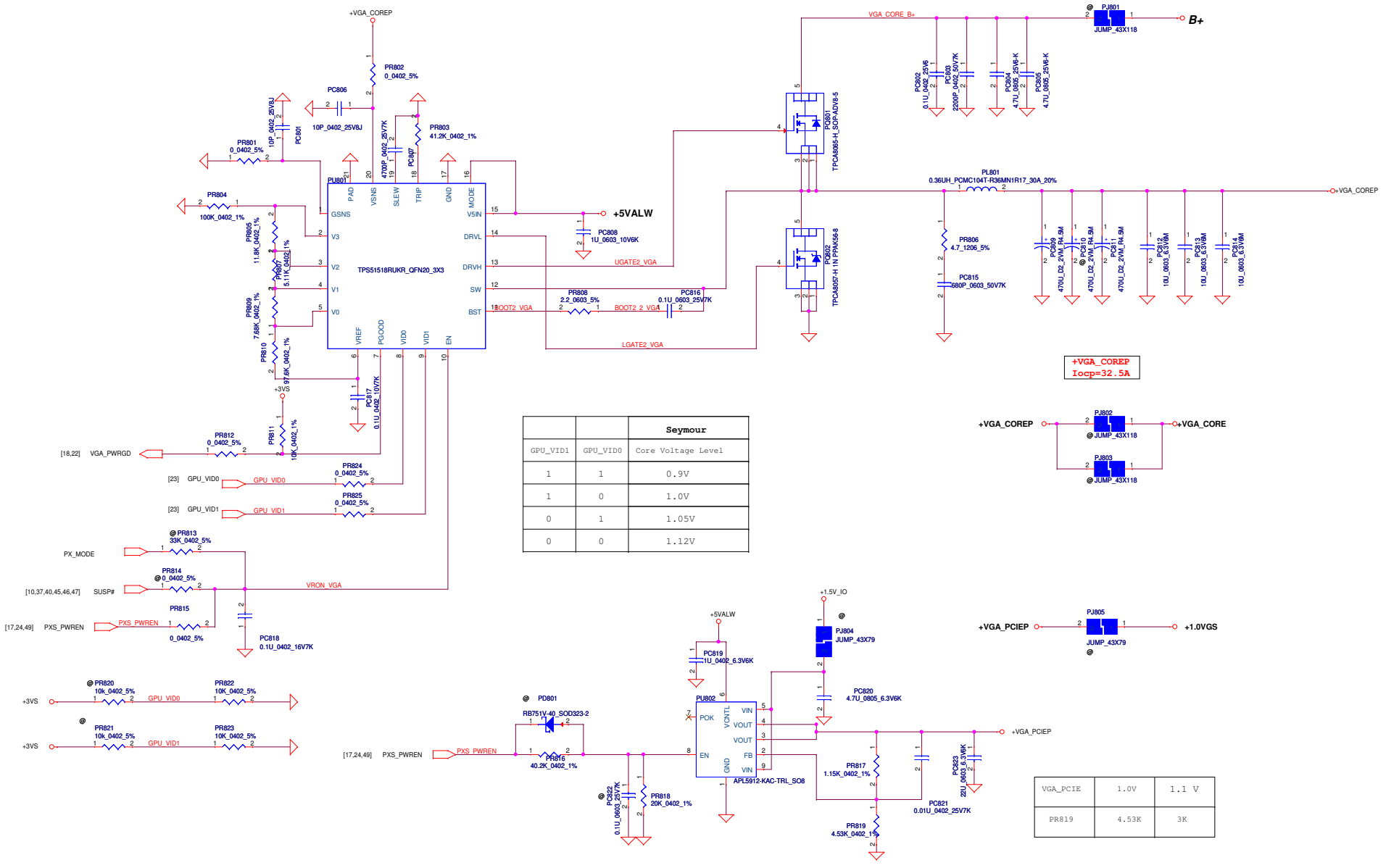
Compal Electronics, Inc.

Title: PWR +VCCSAP

Size: C | Document Number: C38-G series Chief River Schematic | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 48 of 55



		Seymour
GPU_VID1	GPU_VID0	Core Voltage Level
1	1	0.9V
1	0	1.0V
0	1	1.05V
0	0	1.12V

VGA_PCIE	1.0V	1.1 V
PR819	4.53K	3K

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

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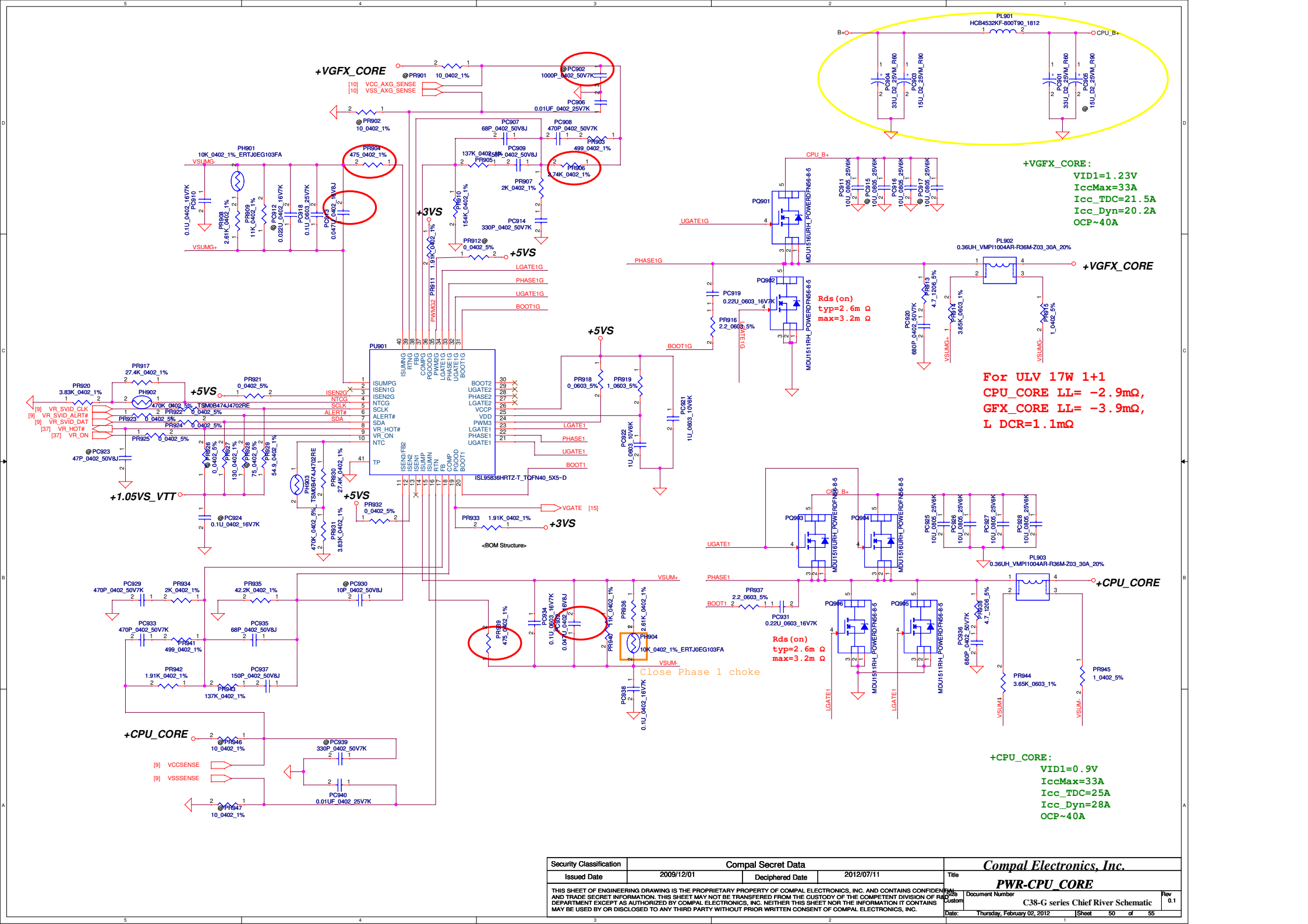
Compal Electronics, Inc.

Title: **PWR-VGA_CORE/VGA_PCIE**

Size | Document Number | Rev 0.1

Date: Thursday, February 02, 2012 | Sheet 49 of 55



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2009/12/01	Deciphered Date	2012/07/11	Title: PWR-CPU_CORE
				Size: Custom; Document Number: C38-G series Chief River Schematic; Rev: 0.1
				Date: Thursday, February 02, 2012; Sheet 50 of 55

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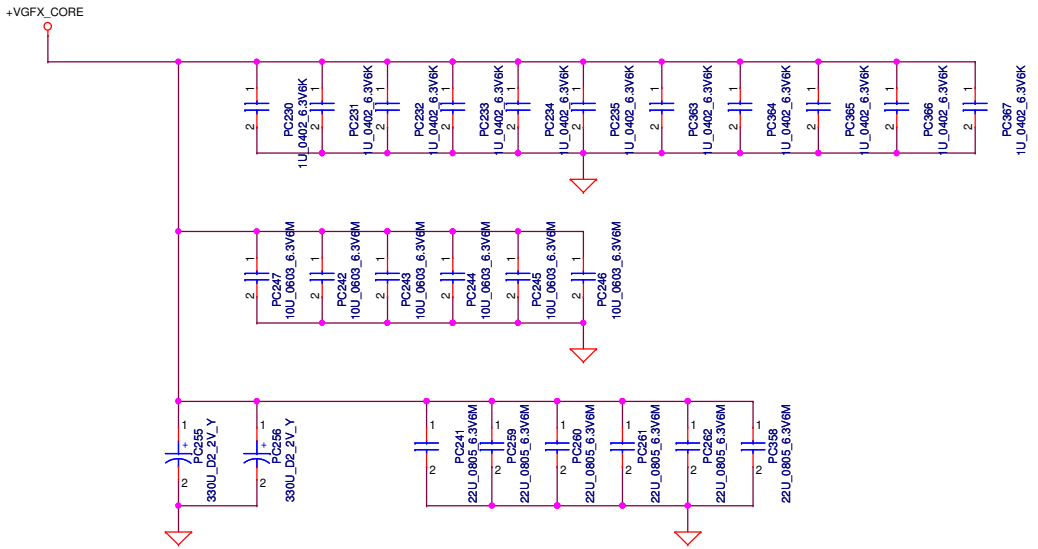

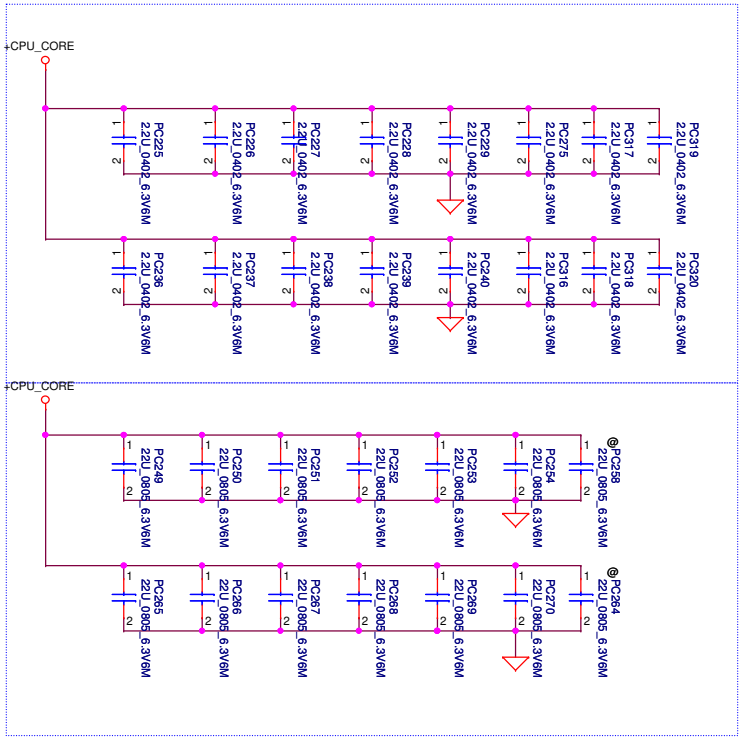

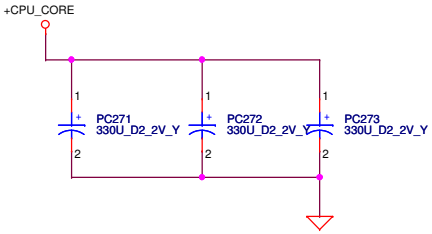

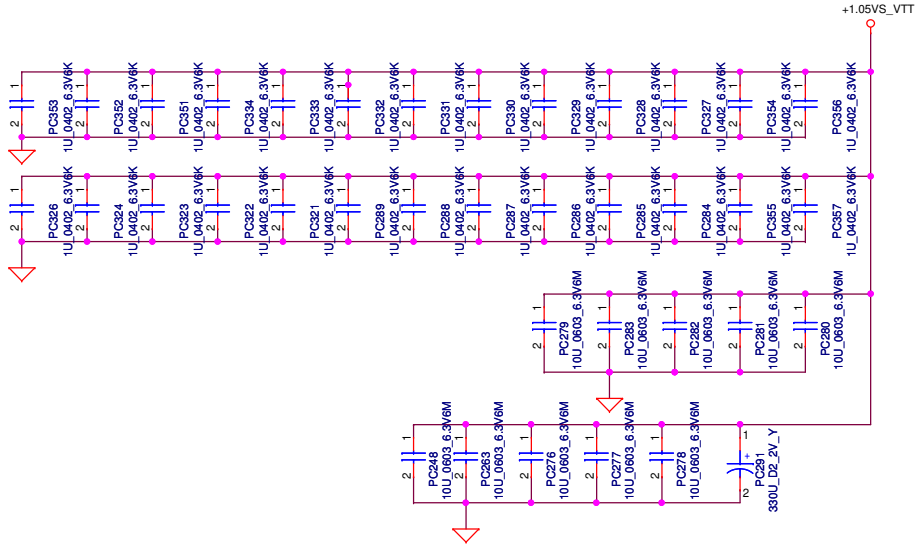

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Compal Electronics, Inc.

Title: CPU_CORE_CAP

Size: Custom | Document Number | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 51 of 55

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
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8					
9					
10					
11					
12					
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15					
16					
17					

Security Classification: Compal Secret Data
Issued Date: 2009/01/06 Deciphered Date: 2012/07/11

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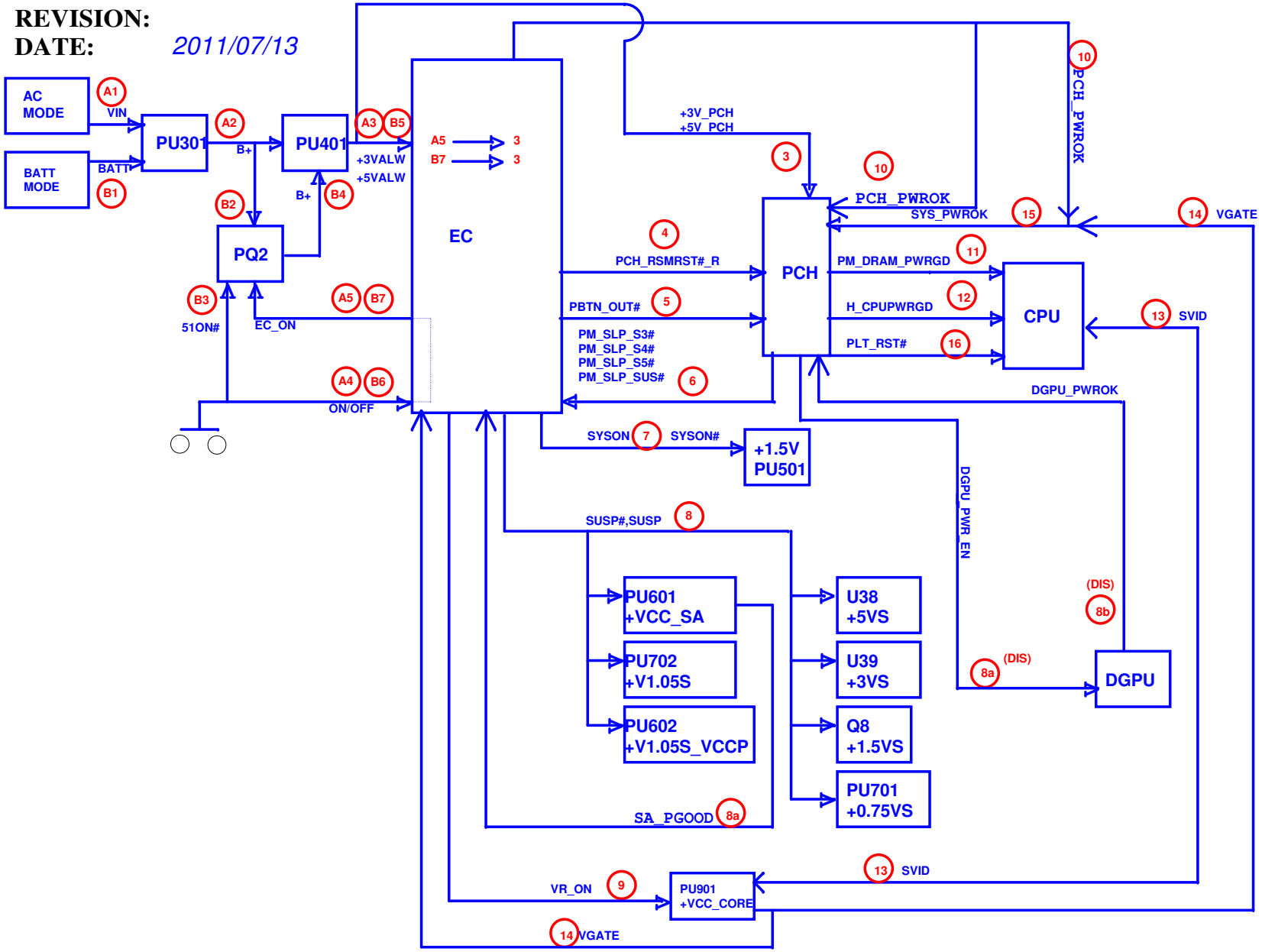
COMPAL CONFIDENTIAL

MODEL NAME: *Power Sequence Block Diagram*
PCB NAME: *LA-7981P*
REVISION:
DATE: *2011/07/13*



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Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Compal Electronics, Inc.

Title: *Power sequence*

Size: Custom | Document Number: *Sherry and Royal* | Rev: 0.1

Date: Thursday, February 02, 2012 | Sheet 53 of 55

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Initial				DVT
2					
3					
4					
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6					
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Issued Date	2011/06/15	Deciphered Date	2012/07/11
Title	HW-PIR1		
Size	Document Number		Rev
Custom	Sherry and Royal		0.1
Date:	Thursday, February 02, 2012	Sheet 54 of 55	