Compal Confidential

Model Name : Q1VZC
File Name :LA-8943P
BOM P/N:43

ZZZ5	ZZZ1	ZZZ2	ZZZ3	ZZZ4
PCB	LA-8943P	LS-8941P	LS-8942P	LS-8943P
DAZ@	DA2@	DA2@	DA2@	DA2@

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CHROME M/B Schematics Document

Intel Sandy Bridge ULV Processor + Panther Point PCH

2012-08-10

REV:1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/03/21	Deciphered Date	2013/03/21	Title: Cover Page
				Size: Custom; Document Number: CHROME M/B LA-8943P Schematic; Rev: 0.1
				Date: Friday, August 10, 2012; Sheet 1 of 45

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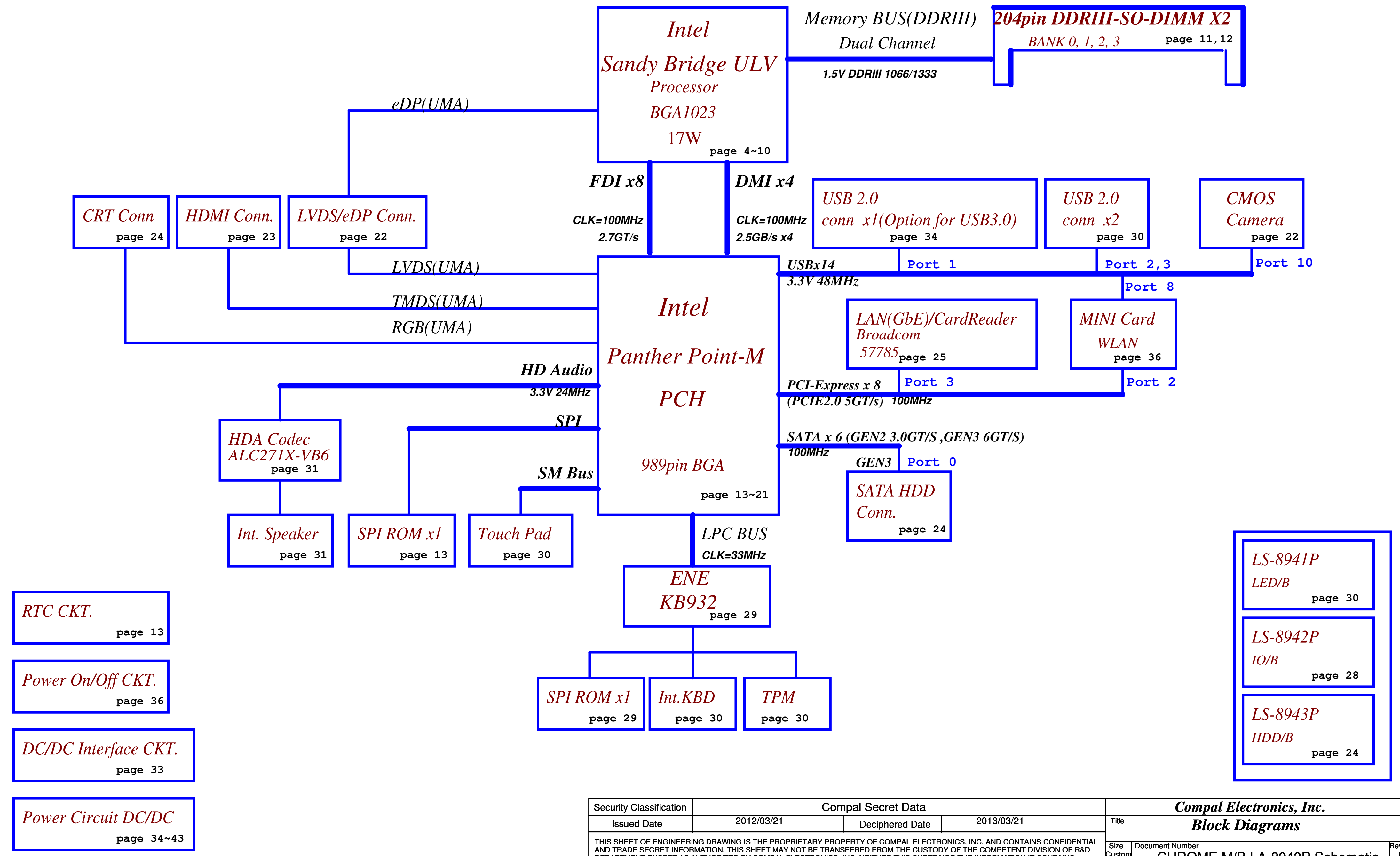
Model Name : Q1VZC
File Name :LA-8943P



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				Date: Friday, August 10, 2012	Sheet 2 of 45

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON
+VCCSUS3_3	+3VALW to +VCCSUS3_3 power rail for PCH (Short Jump)	ON	ON	OFF
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON
+5VREF_SUS	+5VALW to +5VREF_SUS power rail for PCH (Short resister)	ON	ON	OFF
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

PCH SM Bus address

Device			Address	
ChannelA	DIMM0	A0	1010 000X	JDIMM1(STD)
ChannelB	DIMM0	B0	1010 010X	JDIMM2(REV)

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

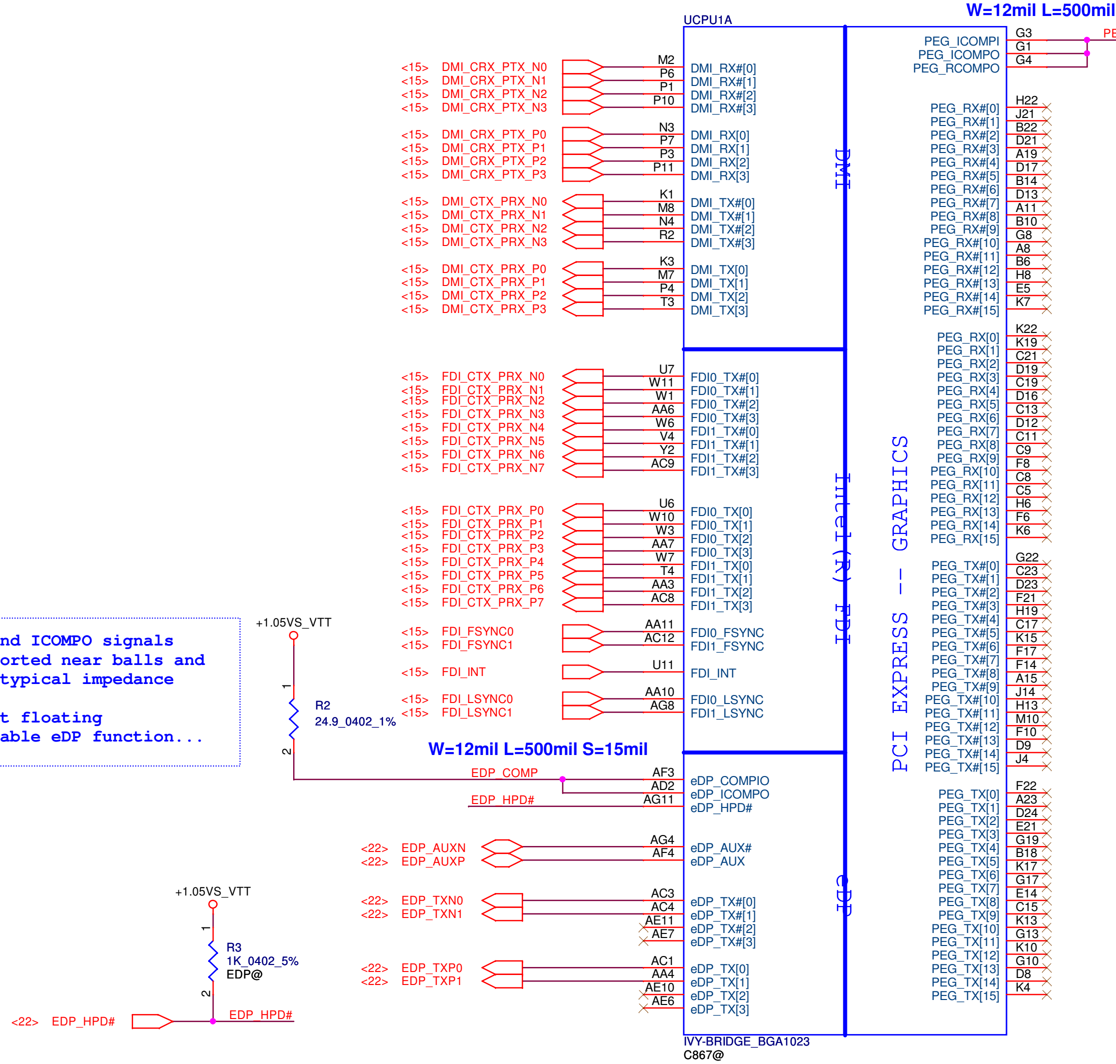
BTO Item	BOM Structure
Celeron 867	C867@
Celeron 877	C877@
Unpop	@
eDP Panel	EDP@
LVDS Panel	LVDS@
Connector	CONN@
USB3 Only	USB3@
Deep S3	DS3@
Normal S3	S3@
Intel i5/i7 CPU only	I57@
Celeron/Pentium/i3 CPU only	CP3@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	
		1	USB 2.0(Options for USB3.0)
	UHCI1	2	USB port(Left 2.0)
		3	USB Port(Left 2.0)
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini Card(WLAN)
		9	
	UHCI5	10	Camera
		11	
	UHCI6	12	
		13	

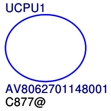
USB 3.0	Port	
XHCI	1	
	2	USB Port(Right 3.0)
	3	
	4	

PEG_ICOMPI and RCOMPO signals should be shorted and routed
with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils
- typical impedance = 14.5 mohms

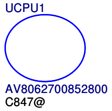


eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms can't be left floating ,even if disable eDP function...

C867@	Celeron 867	HR	1.3G	SA00005BH40(S IC AV8062701148901 SR0FK J1 1.3G ABO!)
C877@	Celeron 877	HR	1.4G	SA00005QI10(S IC AV8062701148001 QB35 J1 1.4G ABO!)



SA00005QI10



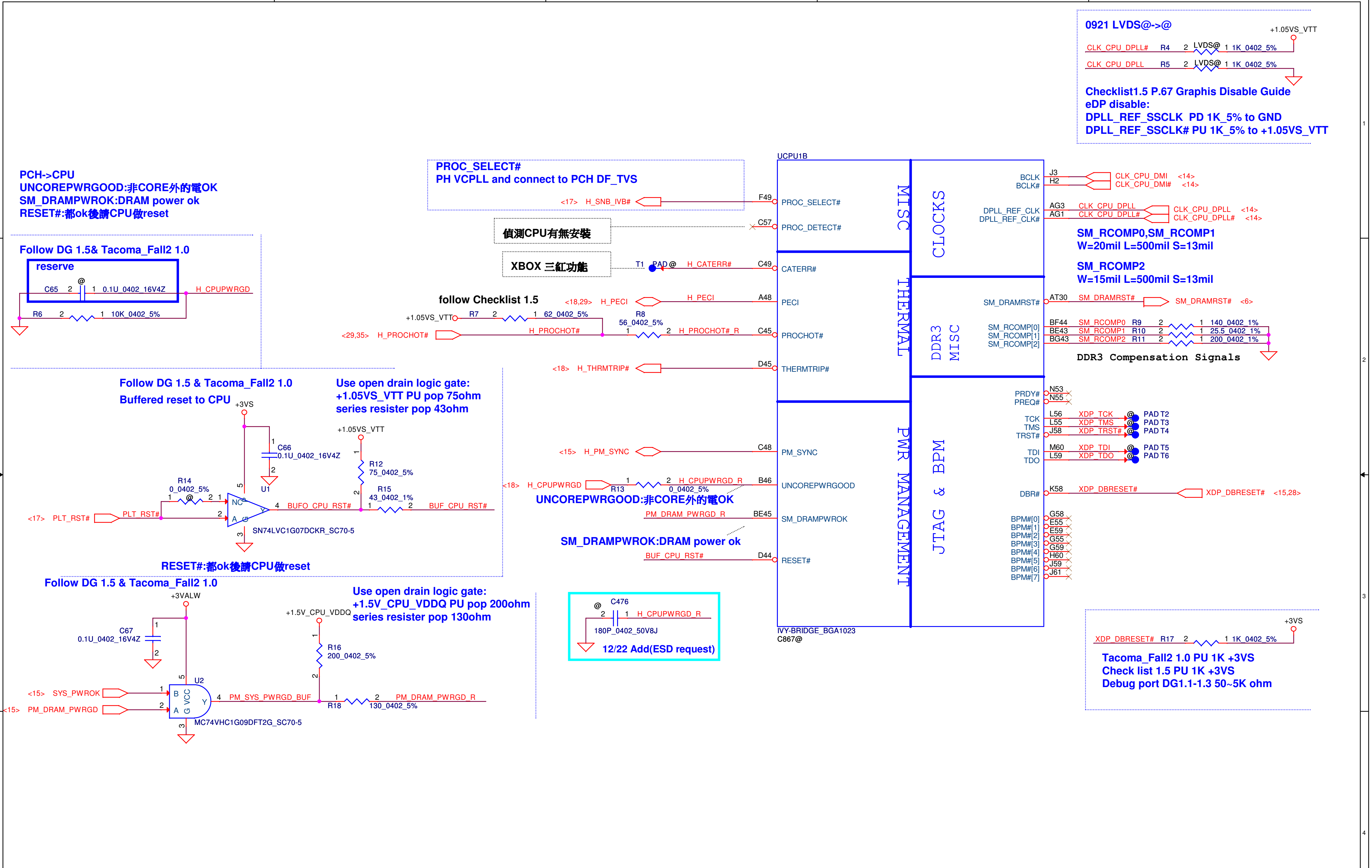
SA00005VK20

Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

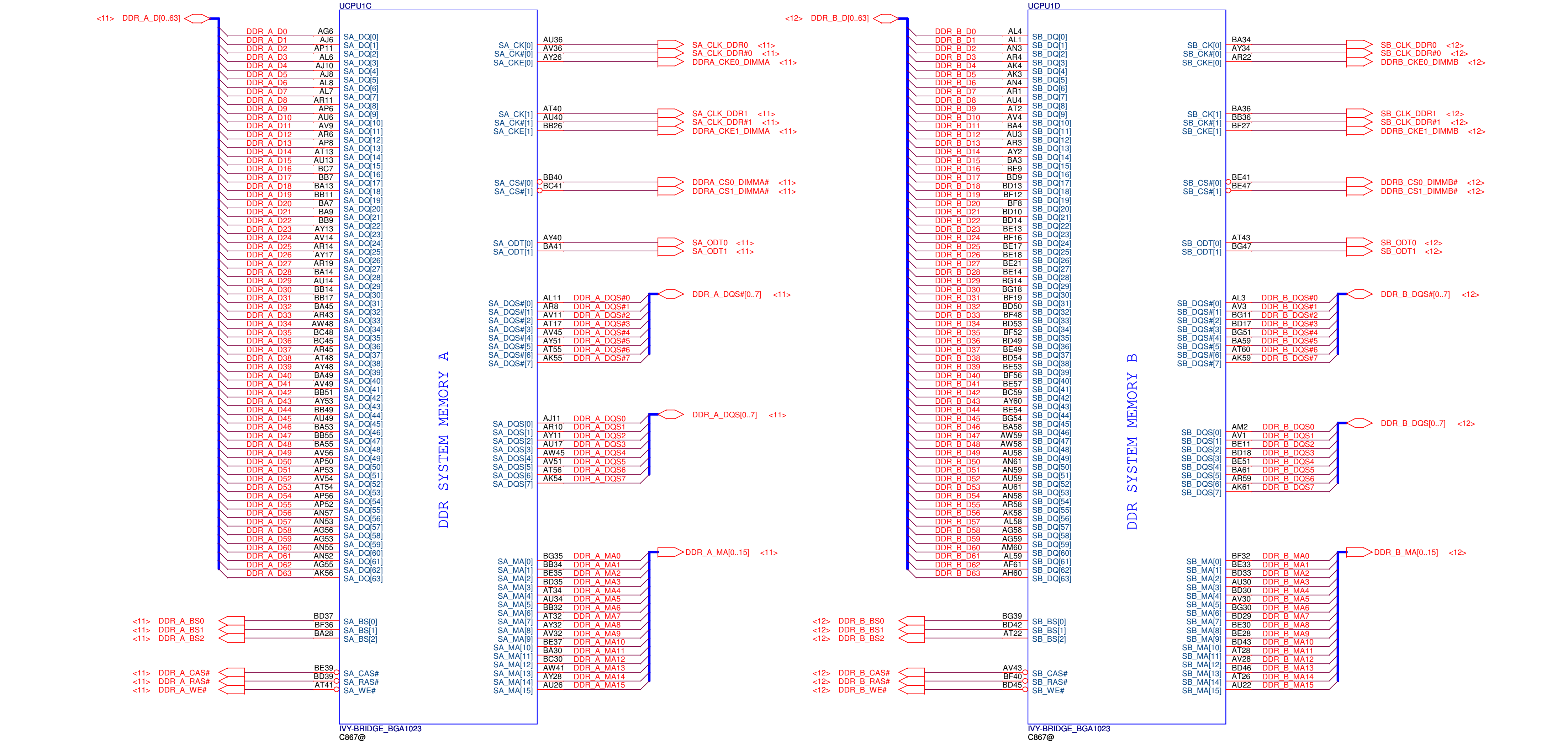
Compal Electronics, Inc.

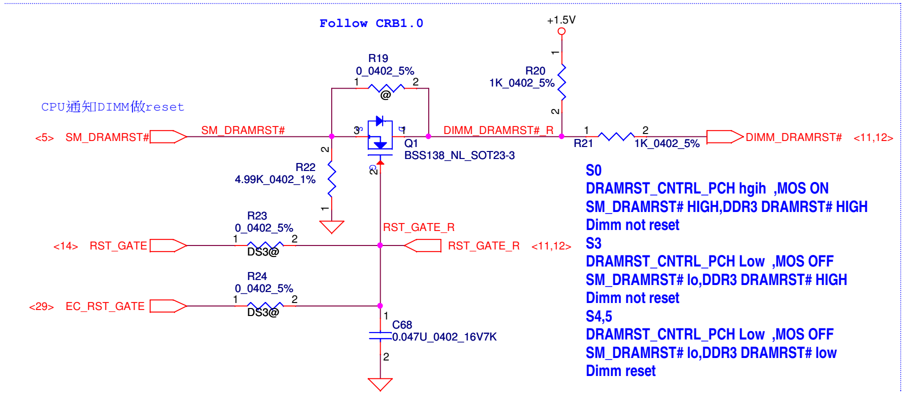
Title: ***PROCESSOR(1/7) DMI,FDI,PEG***

Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev: 0.1



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/03/21	Deciphered Date	2013/03/21	Title: PROCESSOR(3/7) DDRIII
				Size: Custom; Document Number: CHROME M/B LA-8943P Schematic; Rev 0.1
				Date: Friday, August 10, 2012; Sheet 5 of 45





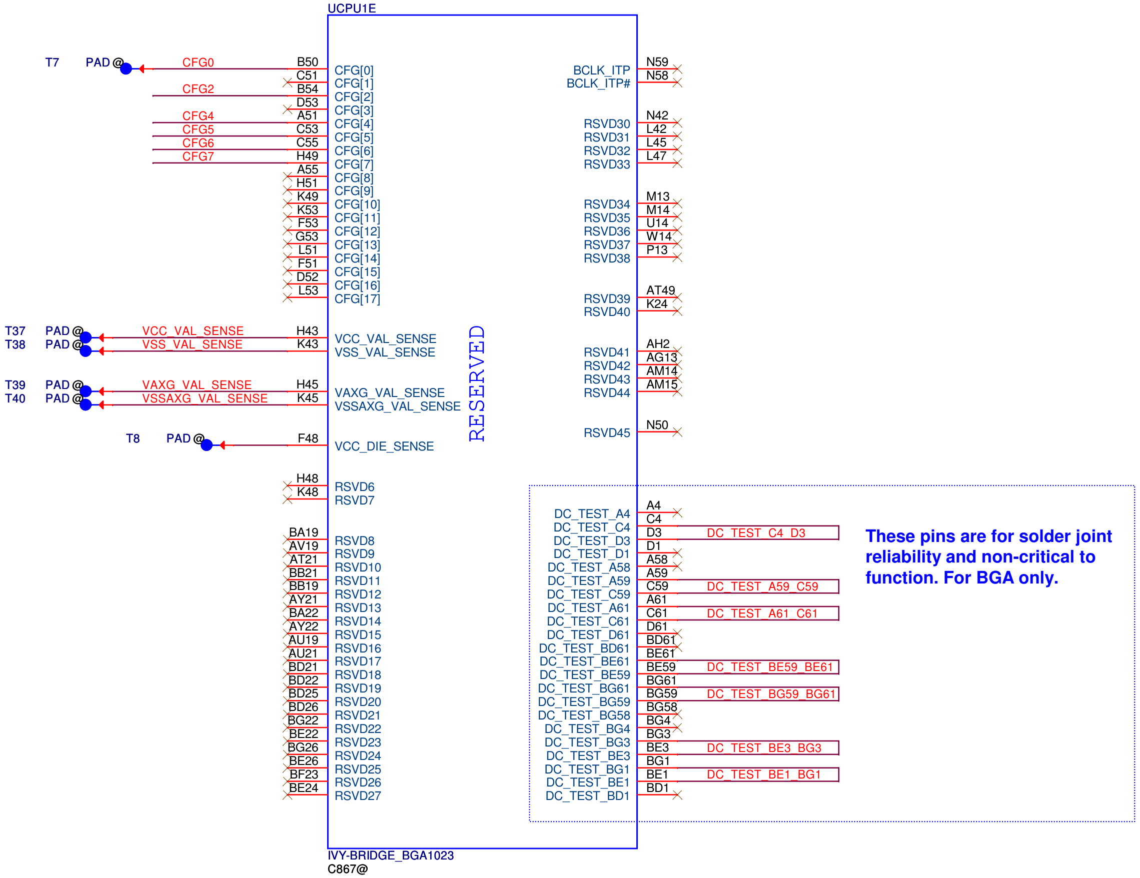
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

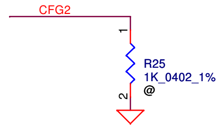
Title: **PROCESSOR(3/7) DDRIII**

Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev 0.1

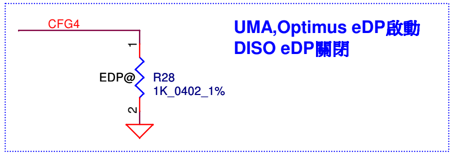
Date: Friday, August 10, 2012 | Sheet 6 of 45



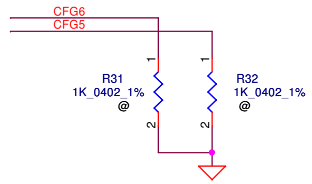
CFG Straps for Processor



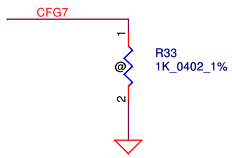
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0:Lane Reversed



eDP enable	
CFG4	★ 1:Disable 0:Enable



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) 1x16 PCI Express ★10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express



PEG DEFER TRAINING	Tacoma_Fall2 1.0 P.12
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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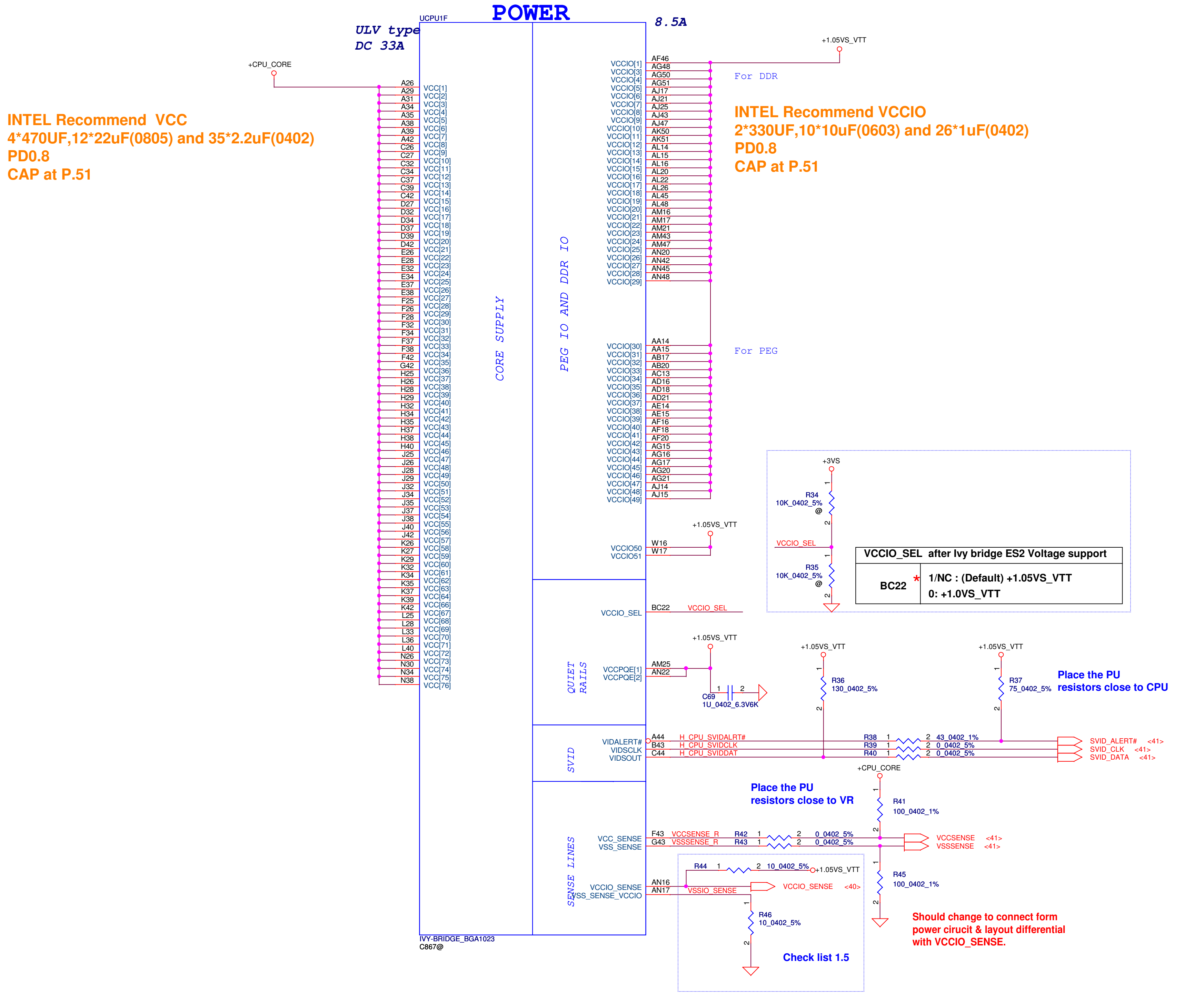
Issued Date	2012/03/21	Deciphered Date	2013/03/21	Title: PROCESSOR(4/7) RSVD,CFG
				Size: Custom; Document Number: CHROME M/B LA-8943P Schematic; Rev 0.1
				Date: Friday, August 10, 2012; Sheet 7 of 45



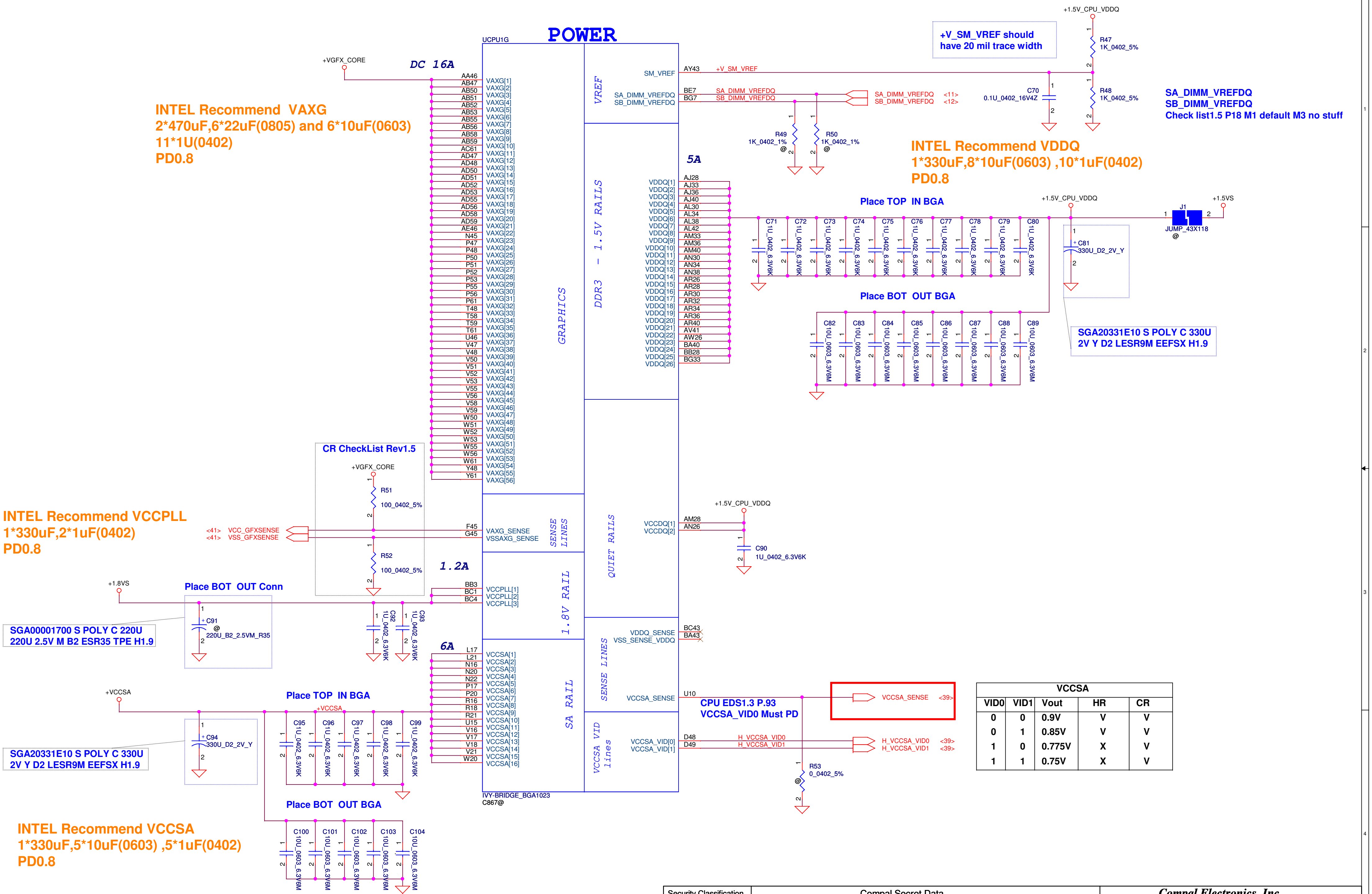
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: **PROCESSOR(5/7) PWR,BYPASS**

Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev: 0.1

Date: Friday, August 10, 2012 | Sheet 8 of 45



VCCSA				
VID0	VID1	Vout	HR	CR
0	0	0.9V	V	V
0	1	0.85V	V	V
1	0	0.775V	X	V
1	1	0.75V	X	V

Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: PROCESSOR(6/7) PWR

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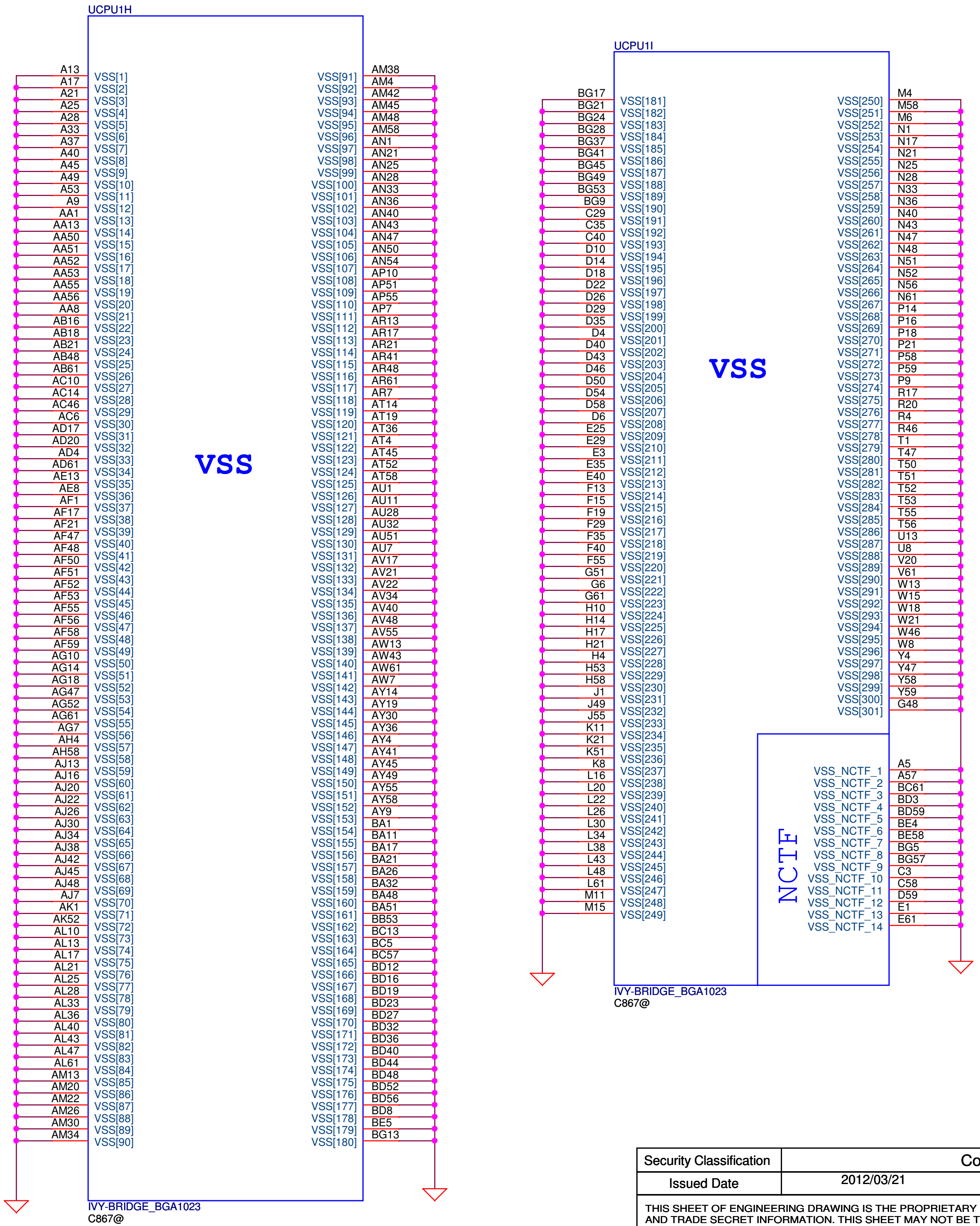
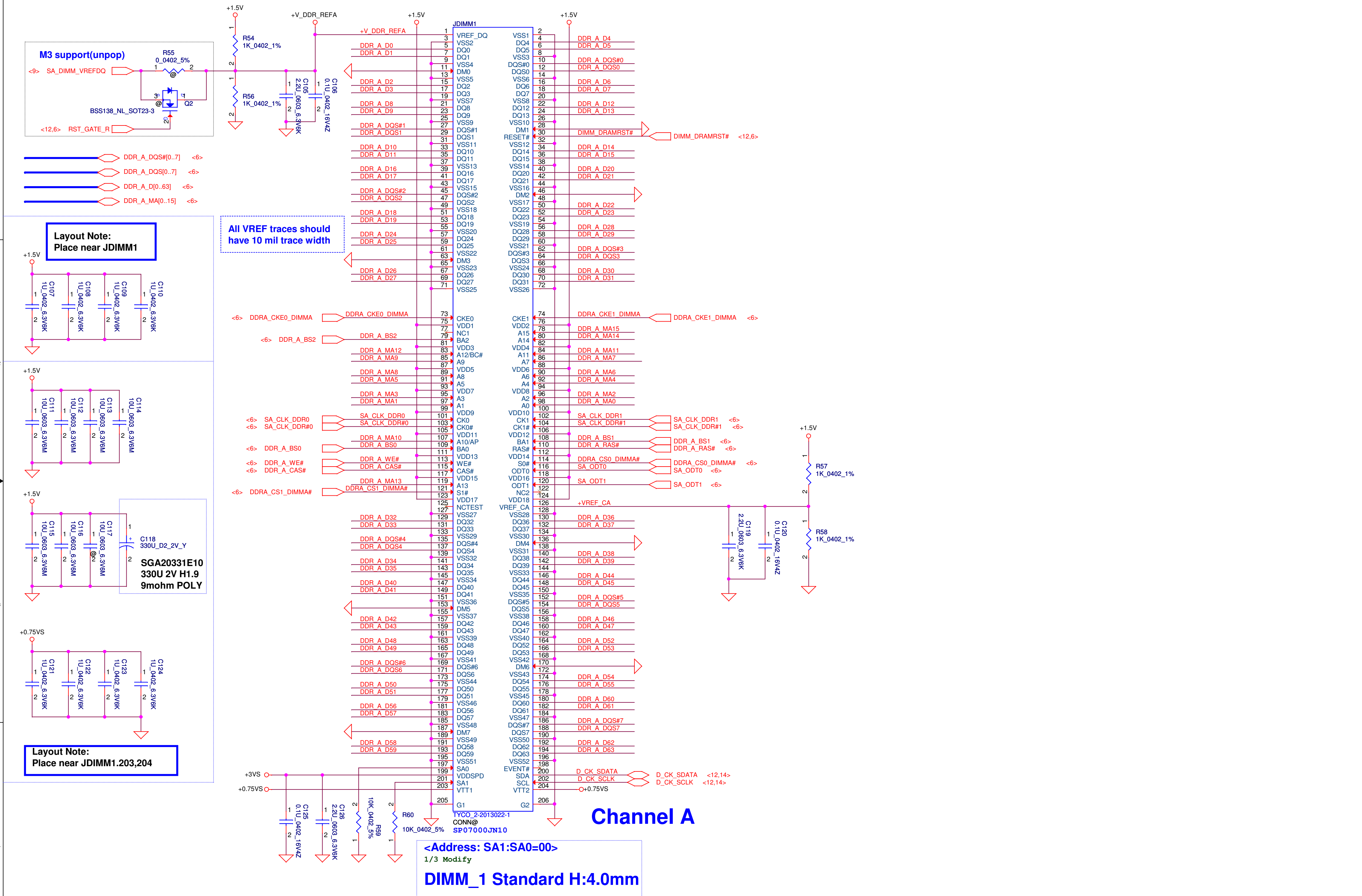


Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: ***PROCESSOR(7/7) VSS***

Size	Document Number	Rev
Custom	CHROME M/B LA-8943P Schematic	0.1



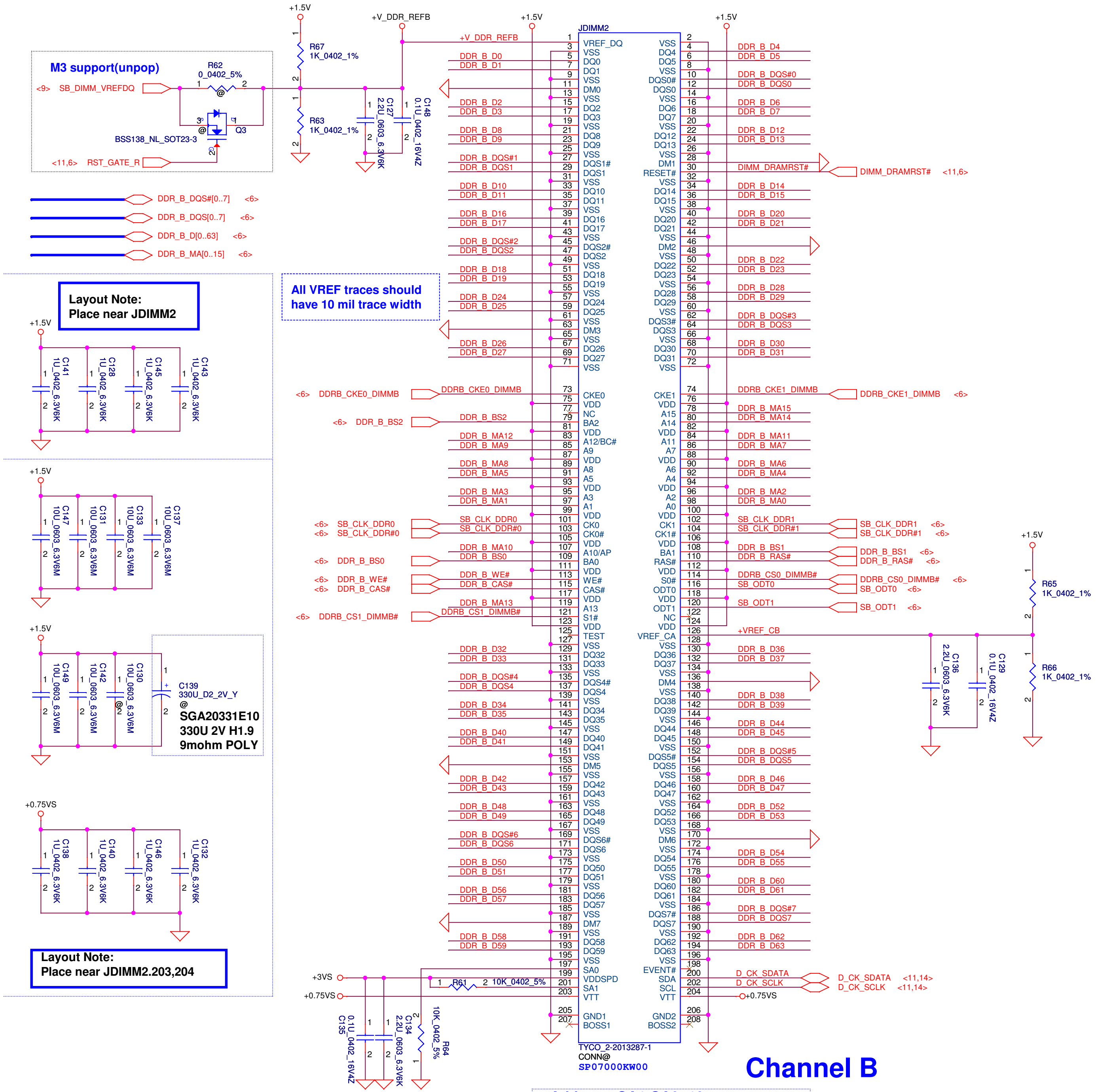
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: DDRIII DIMMA

Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev: 0.1

Date: Friday, August 10, 2012 | Sheet 11 of 45



Channel B

<Address: SA1:SA0=10>

12/21 Modify

DIMM_2 Reverse H:4.0mm

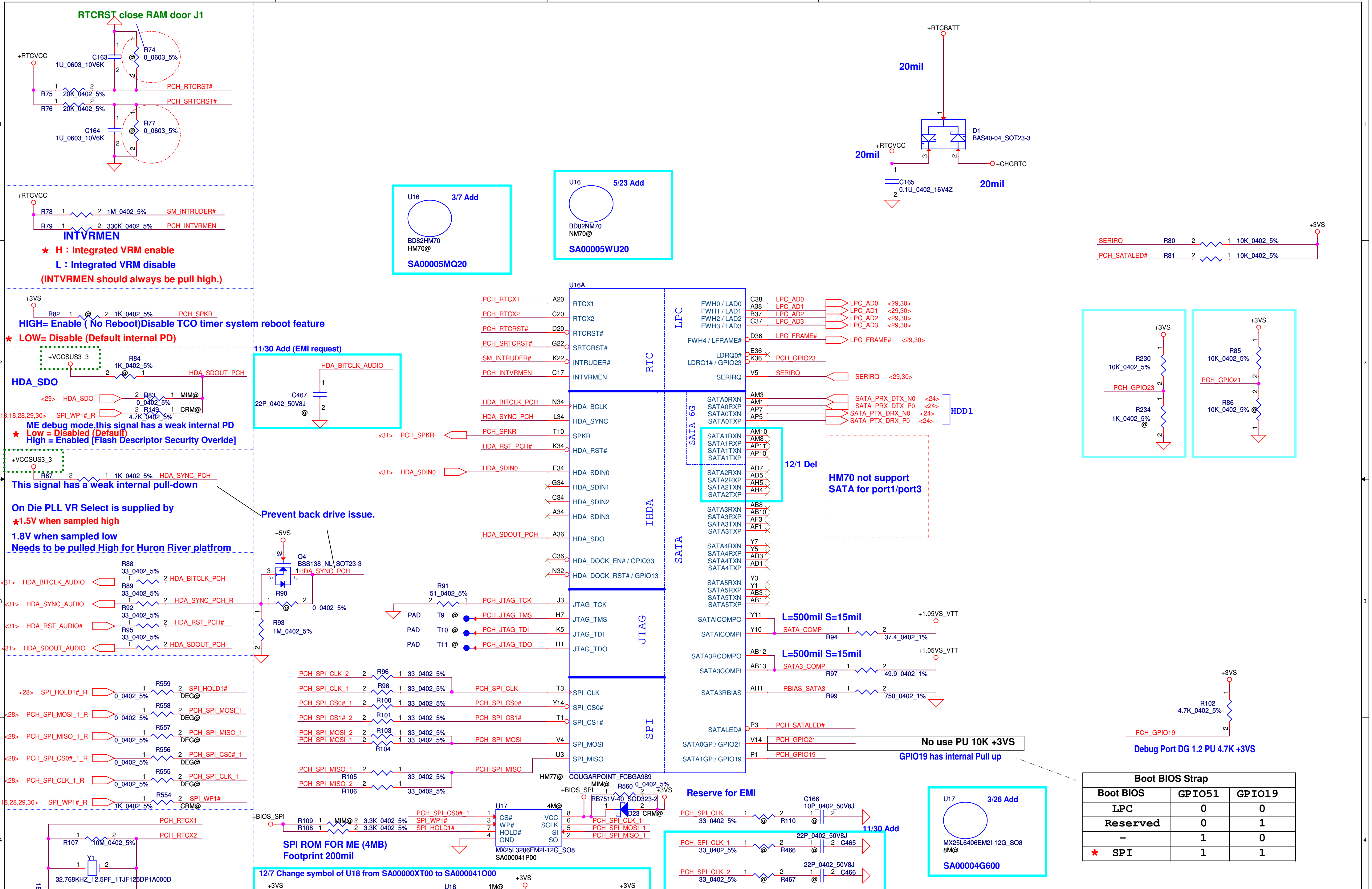
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: **DDRIII DIMMB**

Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev: 0.1

Date: Friday, August 10, 2012 |



Boot BIOS Strap

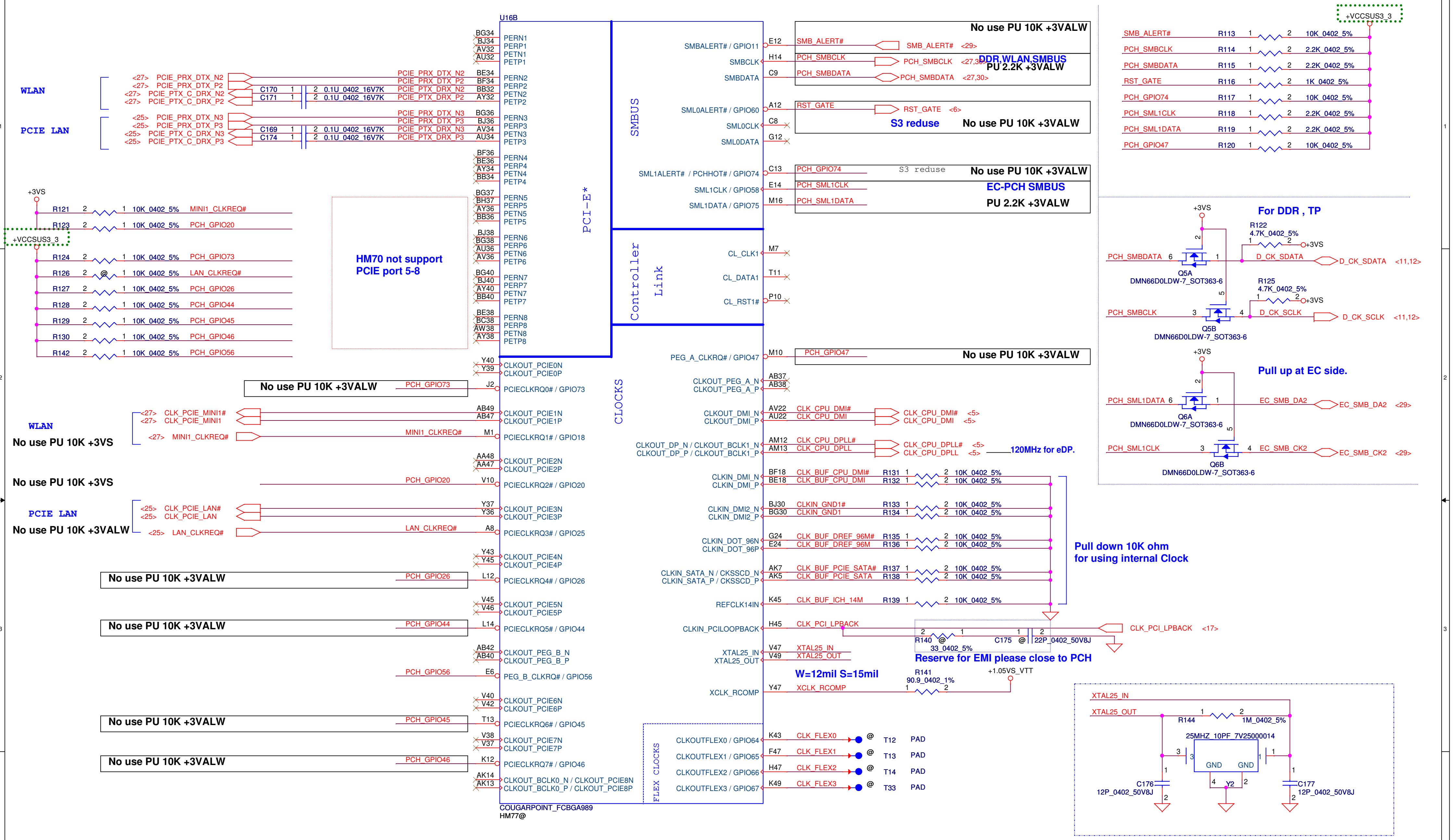
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
–	1	0
★ SPI	1	1

Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: *PCH (1/9) SATA,HDA,SPI, LPC, XDP*

Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev 0.1



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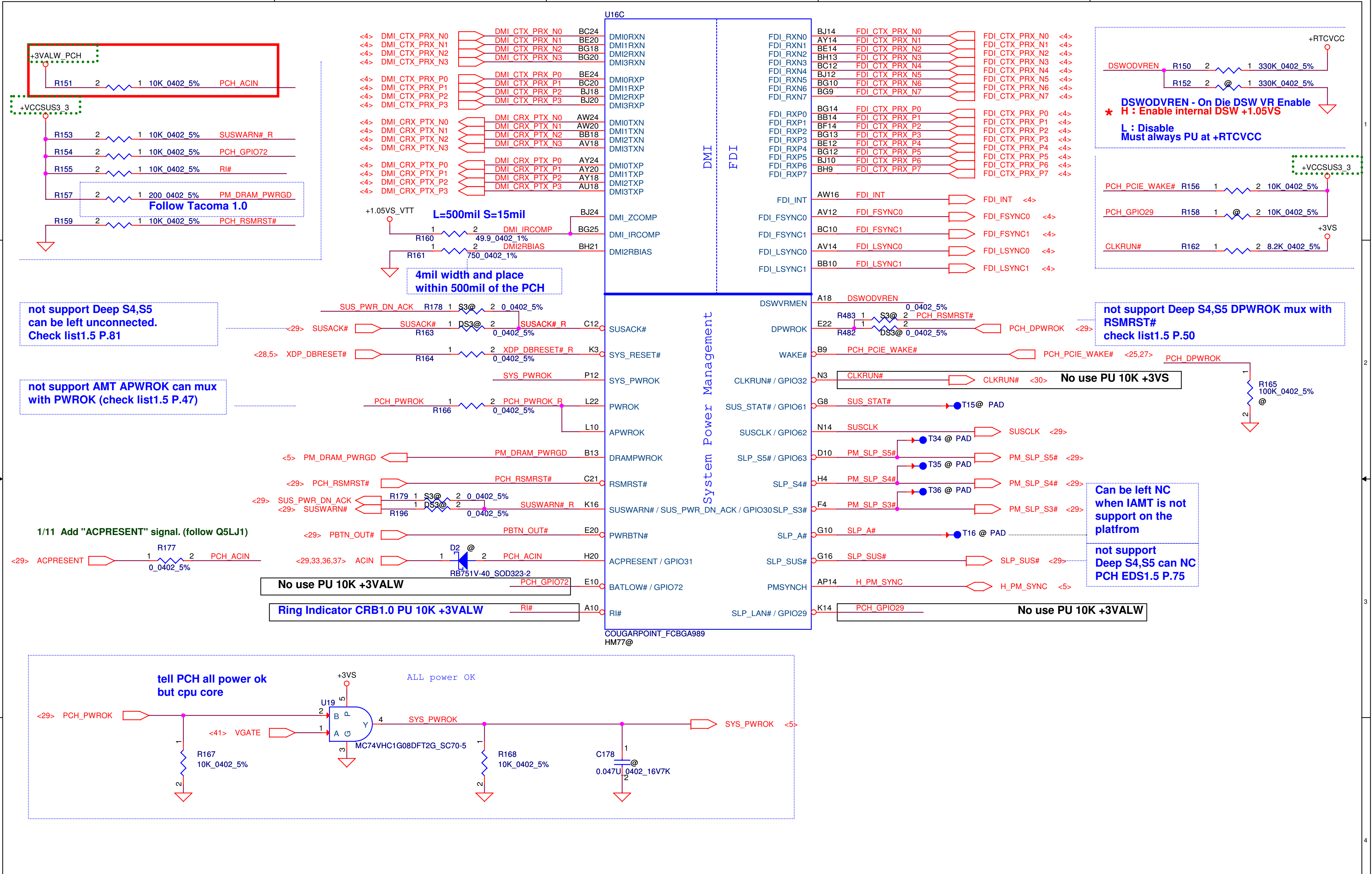
Compal Electronics, Inc.

Title: **PCH (2/9) PCIE, SMBUS, CLK**

Size	Document Number	Rev
Custom	CHROME M/B LA-8943P Schematic	0.1

Date: Friday, August 10, 2012 | Sheet 14 of 45



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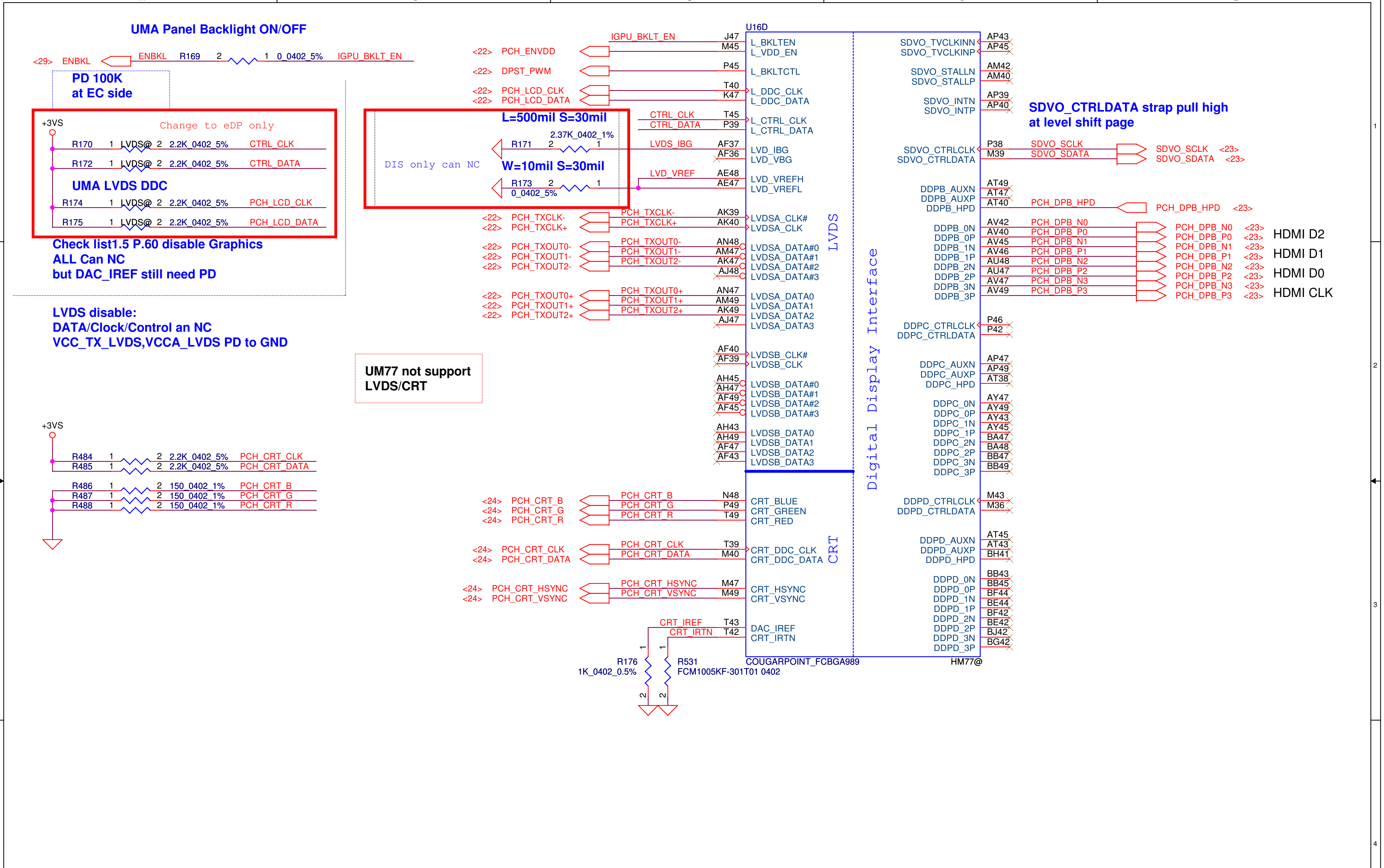
Compal Electronics, Inc.

Title: ***PCH (3/9) DMI,FDI,PM***

Size	Document Number	Rev
Custom	CHROME M/B LA-8943P Schematic	0.1

Date: Friday, August 10, 2012 | Sheet 15 of 45



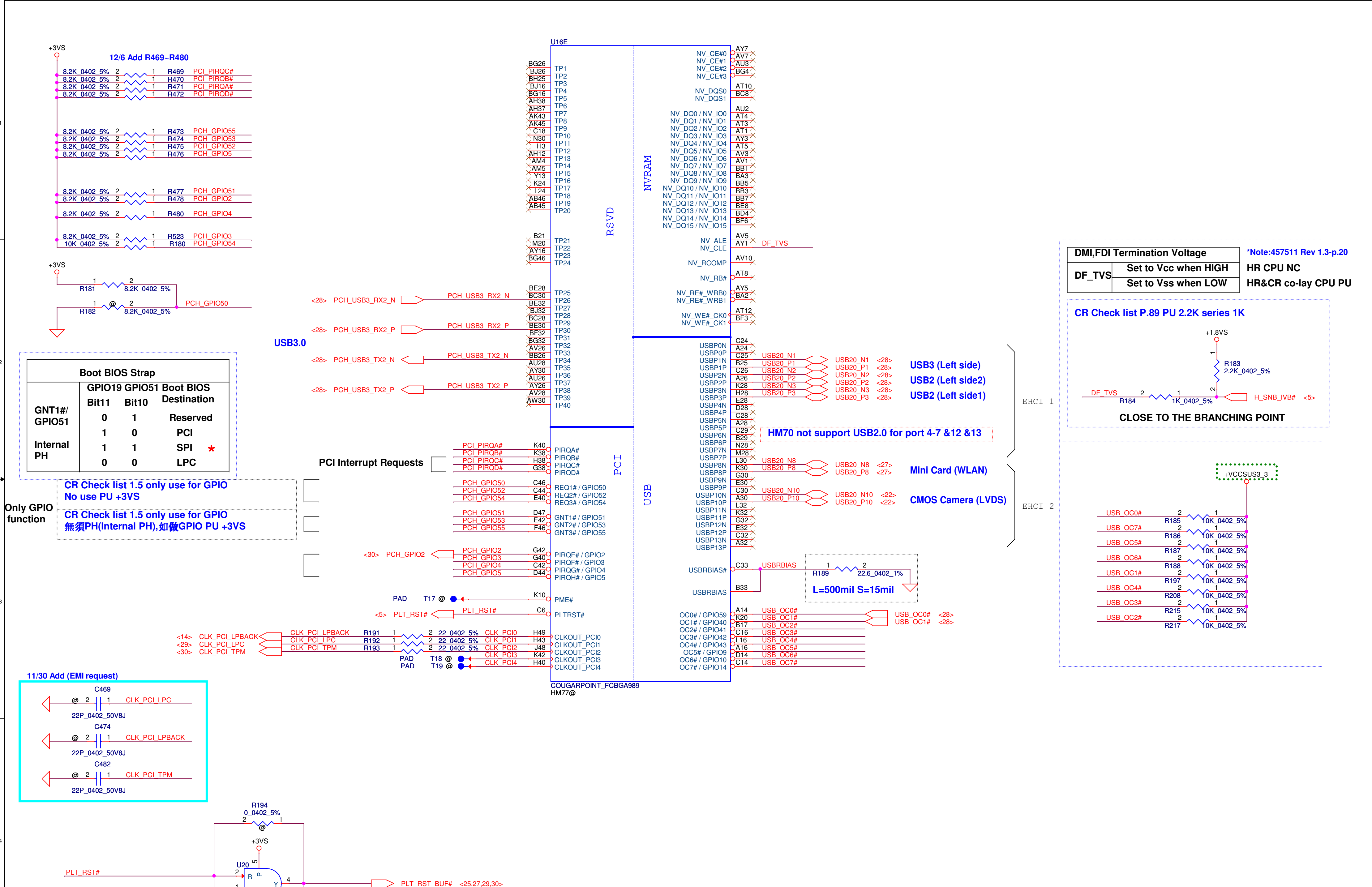
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: ***PCH (4/9) LVDS,CRT,DP,HDMI***

Size	Document Number	Rev
Custom	CHROME M/B LA-8943P Schematic	0.1

Date: Friday, August 10, 2012

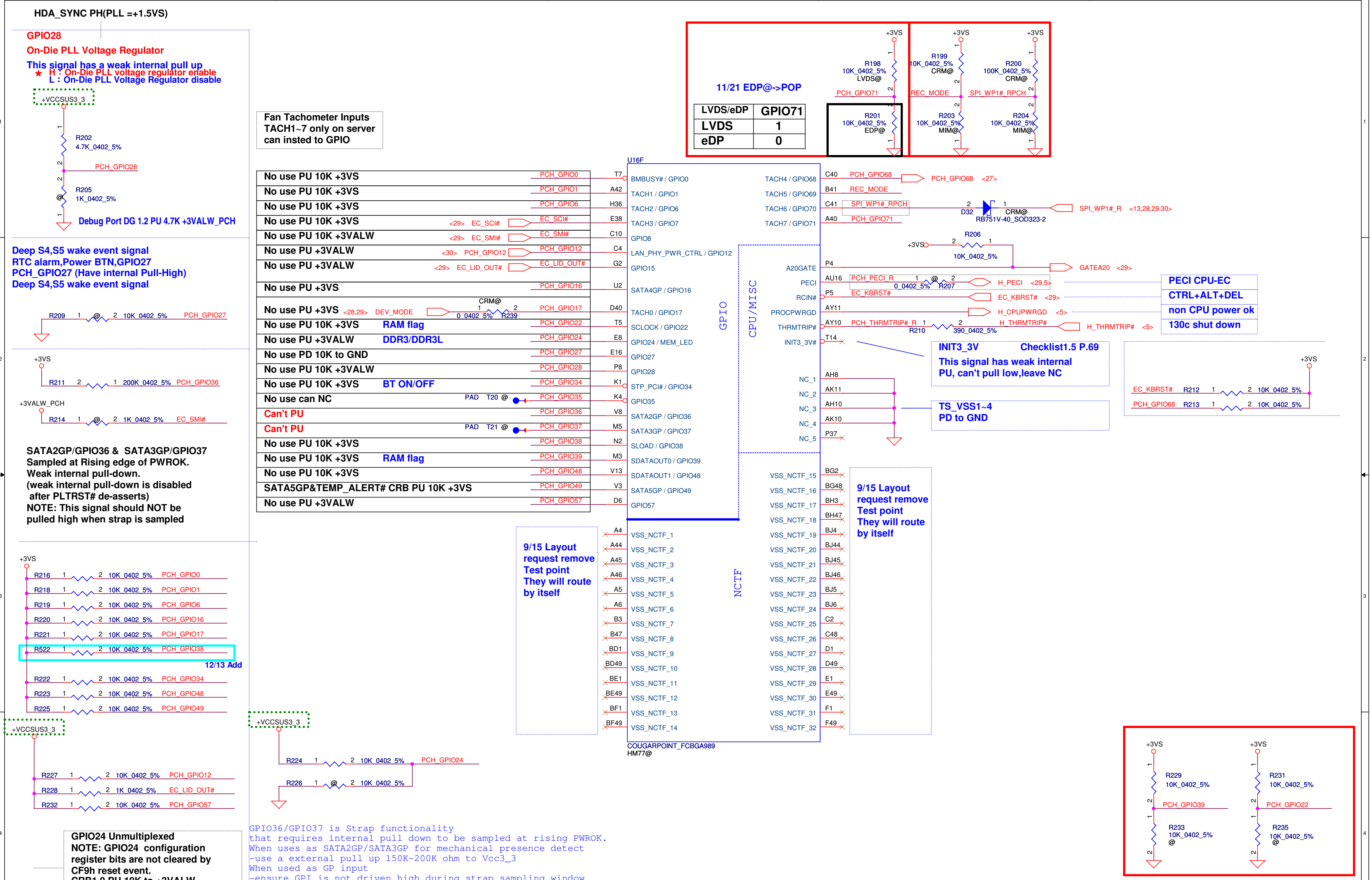


Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: **PCH (5/9) PCI, USB, NVRAM**

Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev 0.1

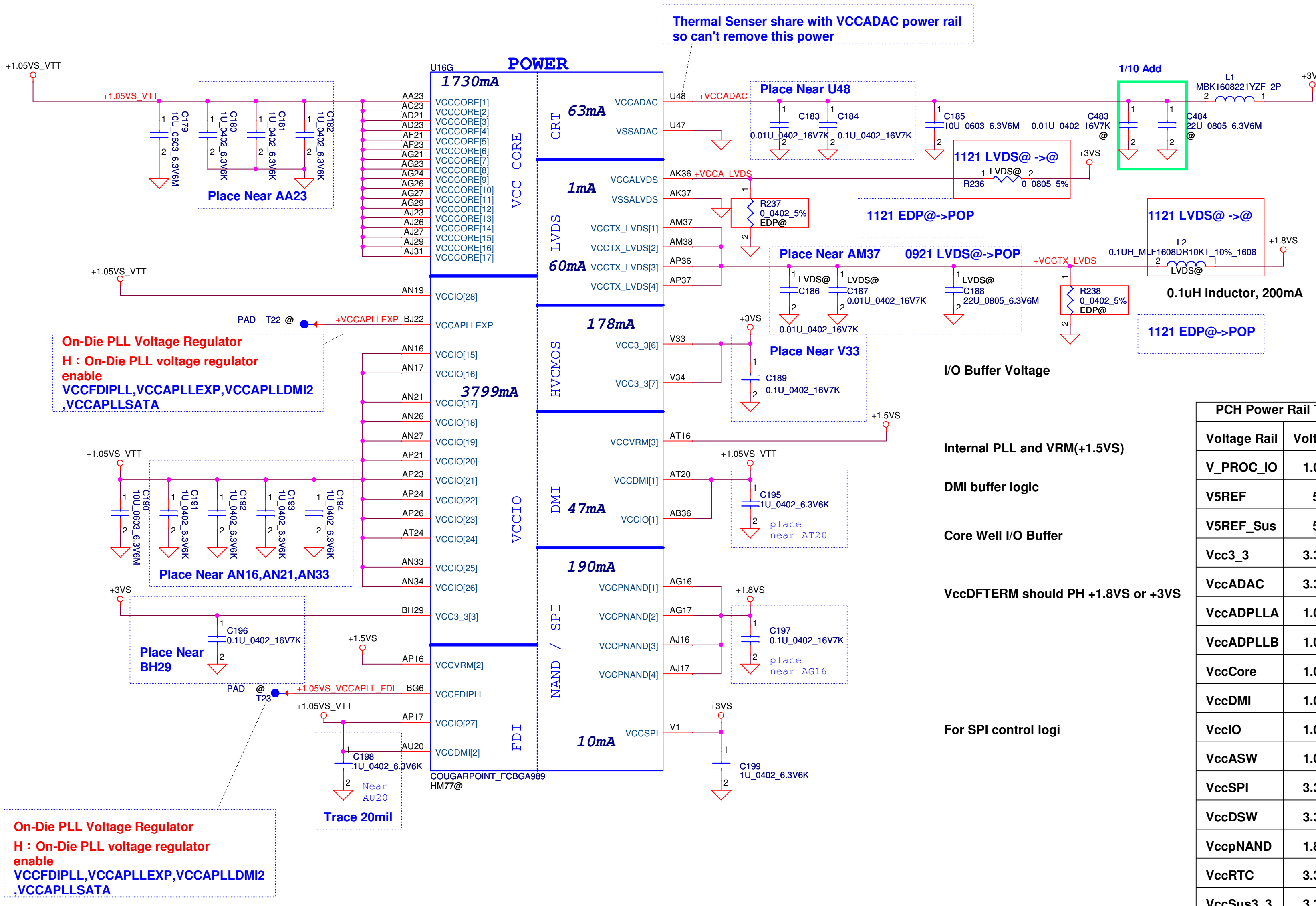


Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: **PCH (6/9) GPIO, CPU, MISC**

Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev: 0.1



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.002	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.178	I/O Buffer Voltage
VccADAC	3.3	0.063	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.075	Display PLL A power
VccADPLLB	1.05	0.075	Display PLL B power
VccCore	1.05	1.73	Internal Logic Voltage
VccDMI	1.05	0.047	DMI Buffer Voltage
VccIO	1.05	3.799	Core Well I/O buffers
VccASW	1.05	0.803	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.01	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.065	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

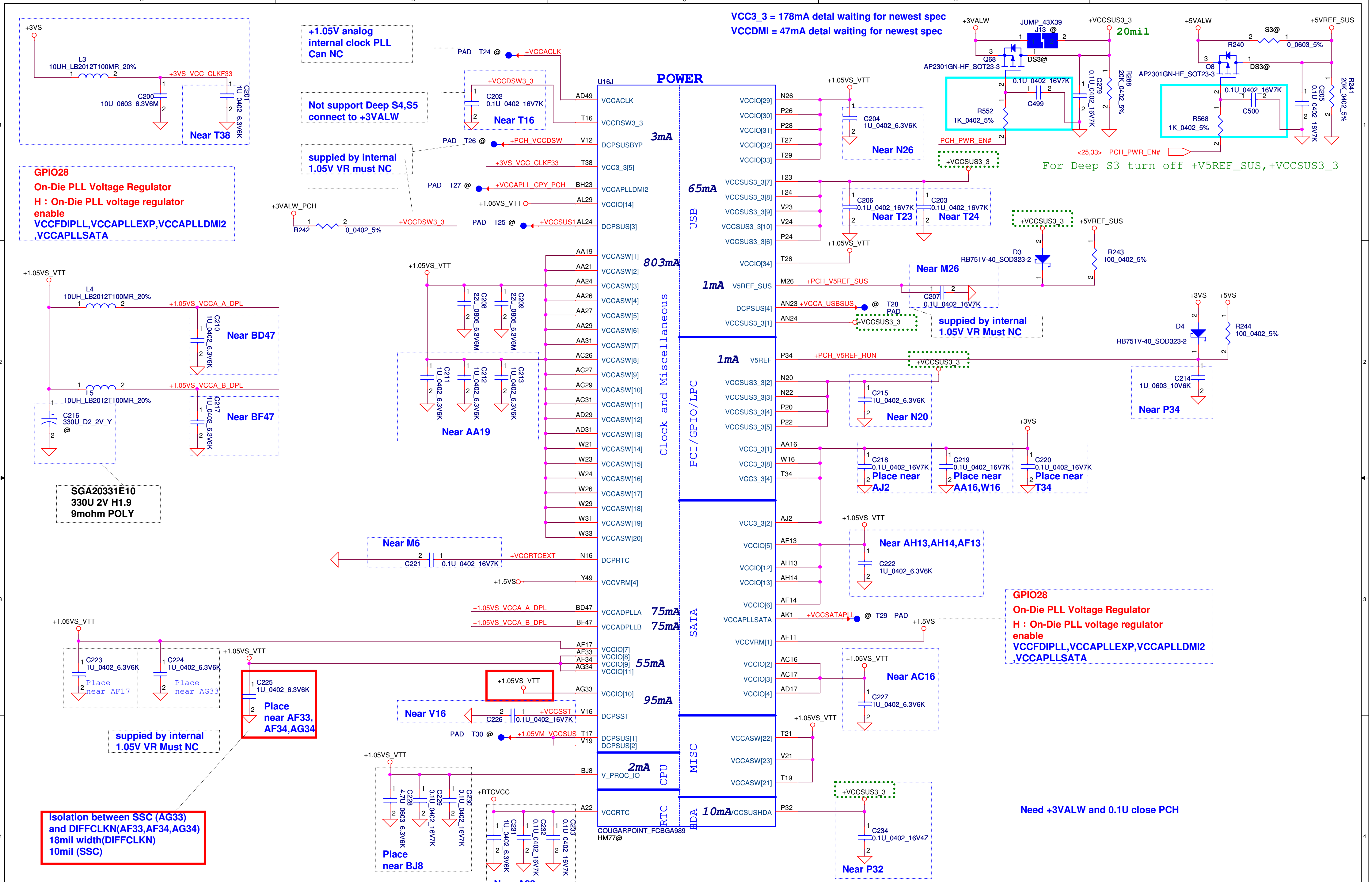
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: *PCH (7/9) PWR*

Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev 0.1

Date: Friday, August 10, 2012 | Sheet 19 of 45



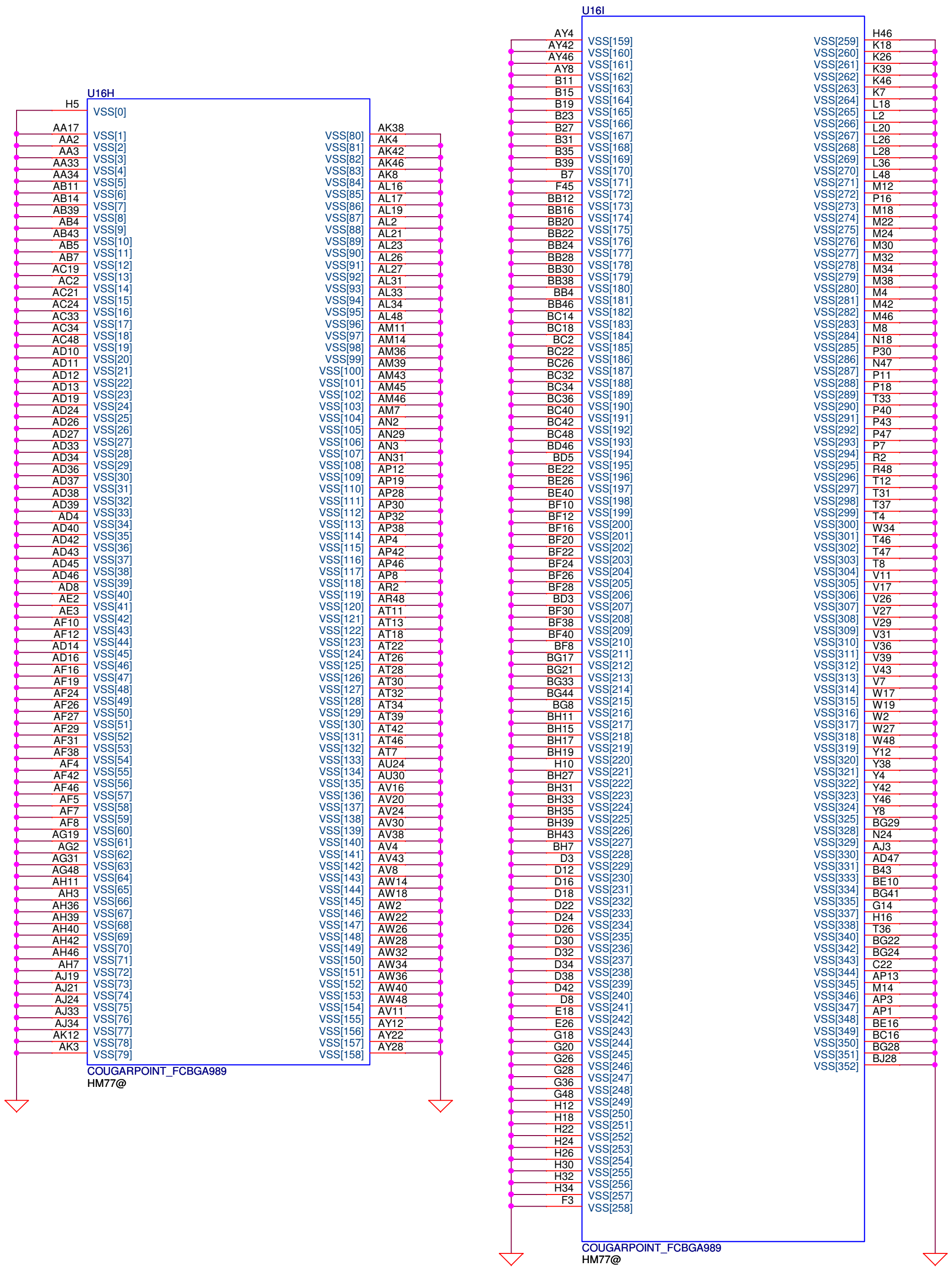
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: **PCH (8/9) PWR**

Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev 0.1

Date: Friday, August 10, 2012 |



Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title **PCH (9/9) VSS**

Size Custom | Document Number CHROME M/B LA-8943P Schematic | Rev 0.1

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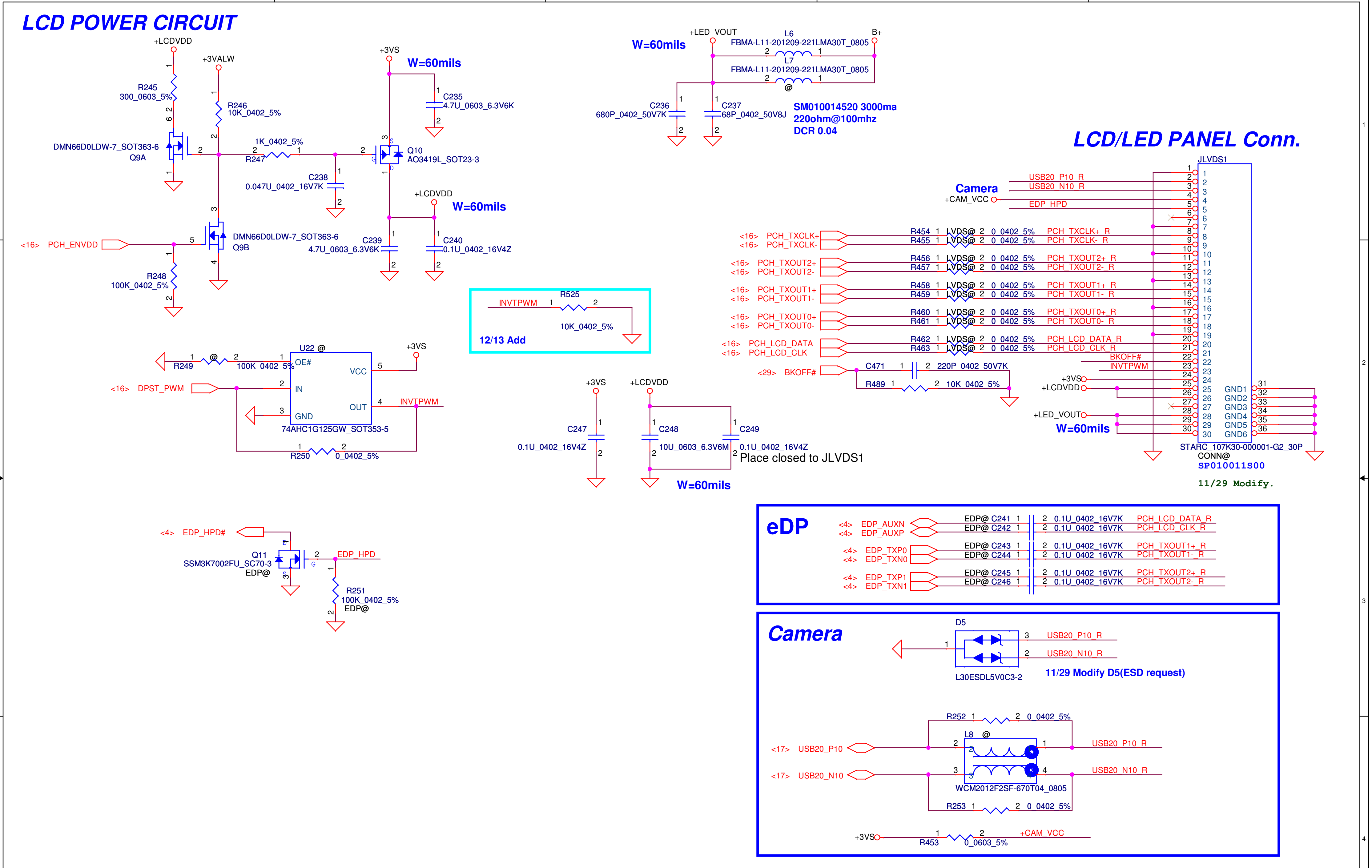

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Issued Date	2012/03/21	Deciphered Date	2013/03/21	Title: LVDS&eDP
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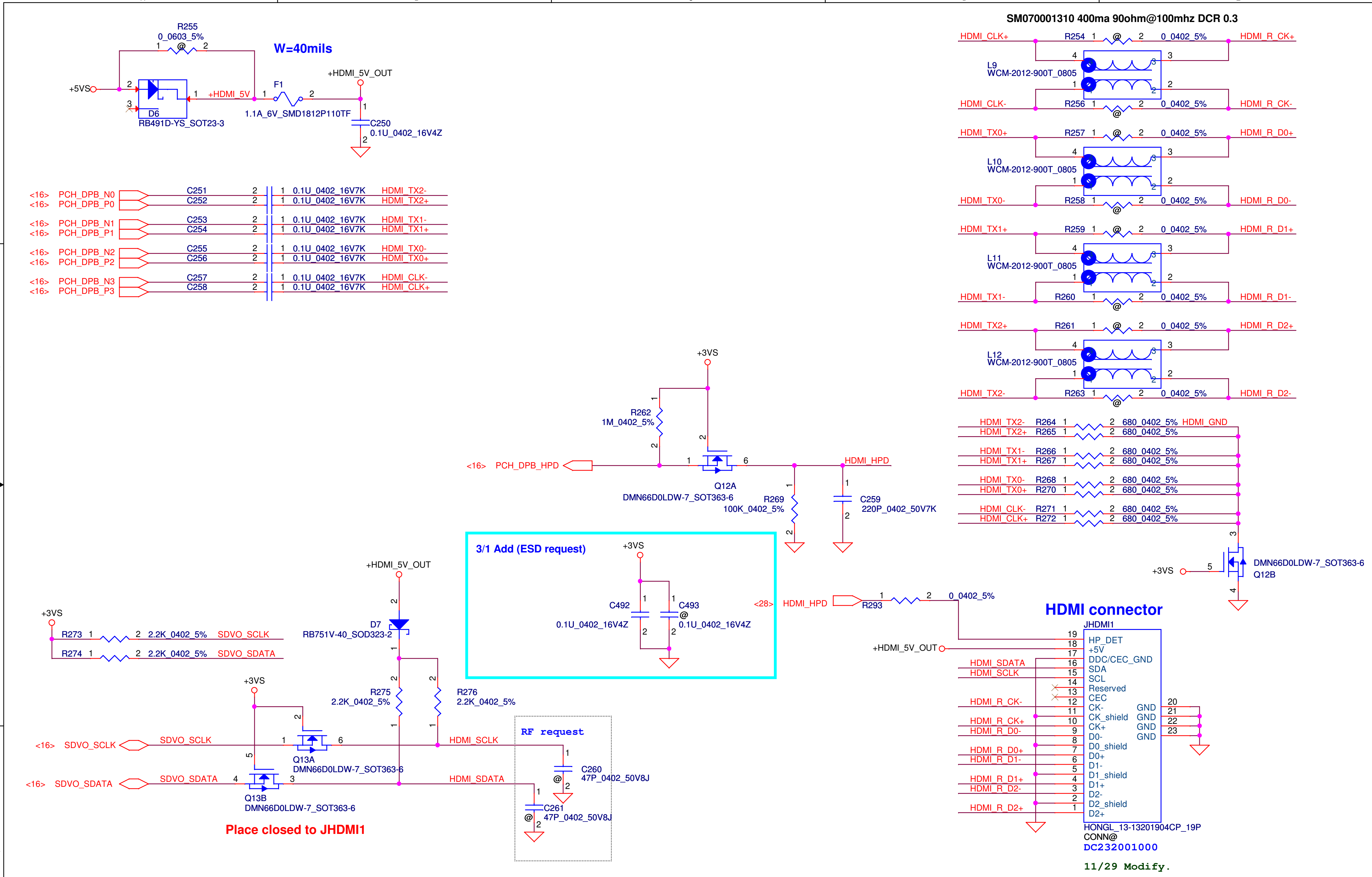
				Date: Friday, August 10, 2012; Sheet 22 of 45



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/03/21	Deciphered Date 2013/03/21	Title: HDMI Conn
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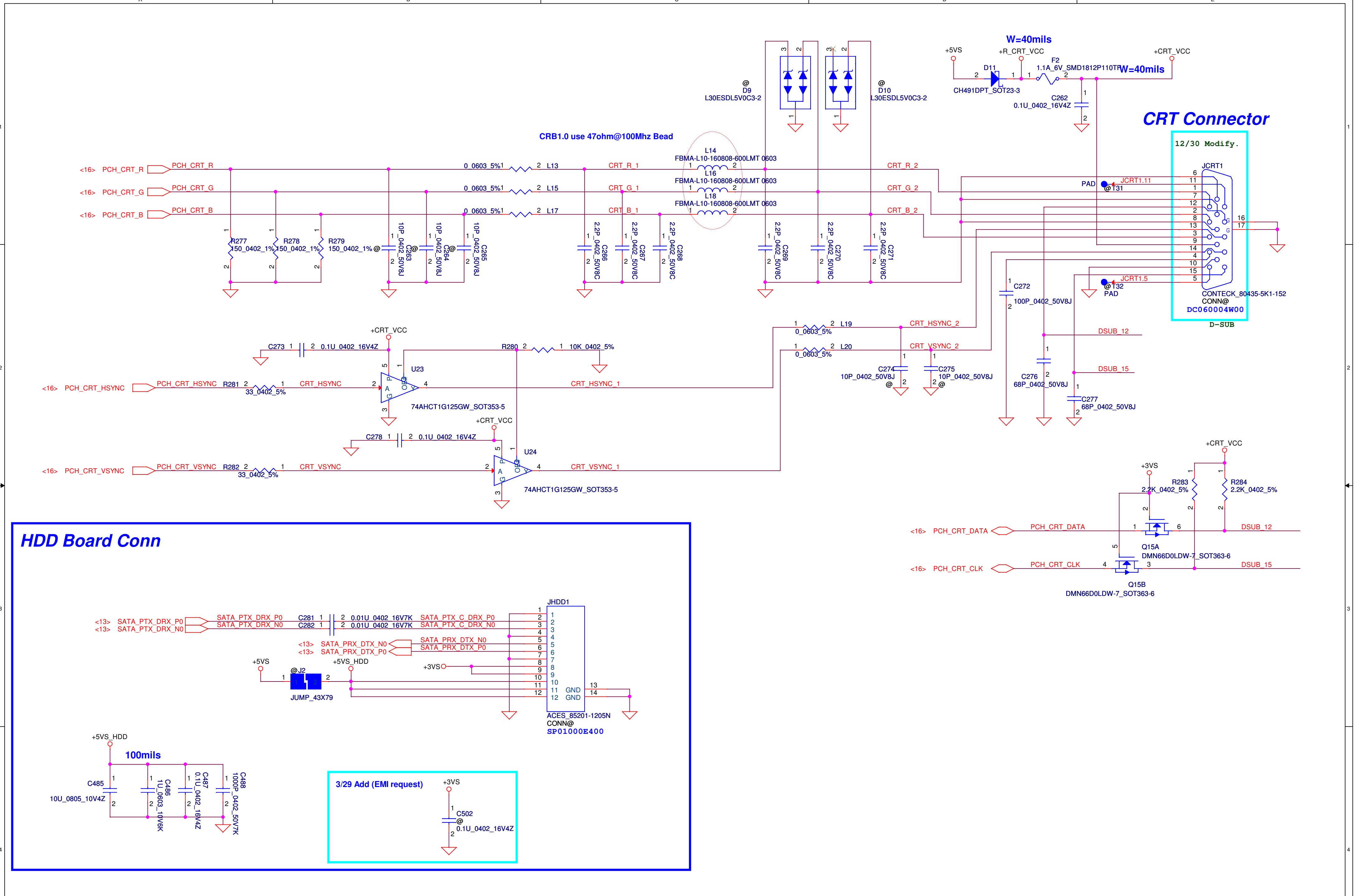
			Date: Friday, August 10, 2012; Sheet 23 of 45



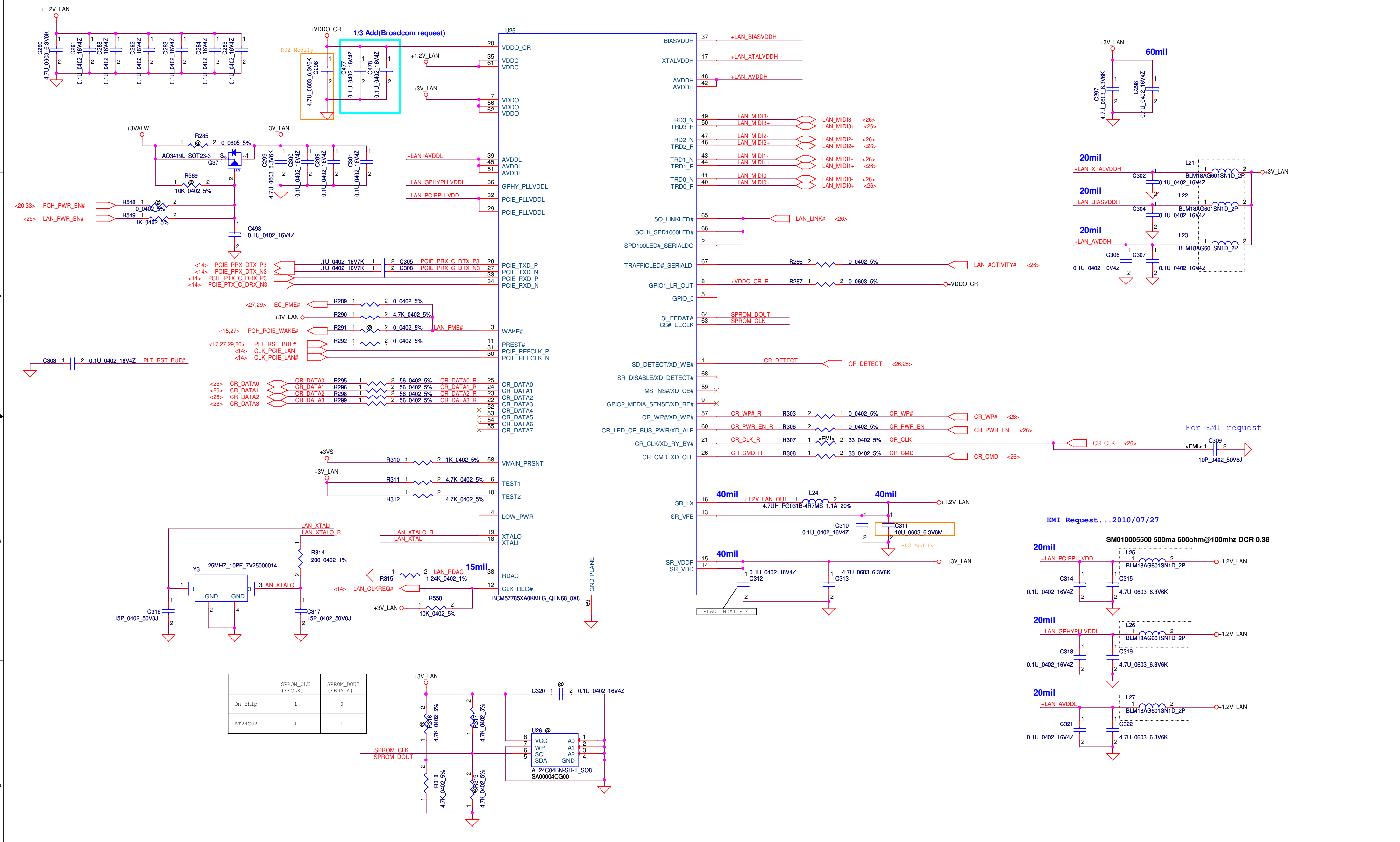
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: CRT&HDD Connector

Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev: 0.1

Date: Friday, August 10, 2012 |

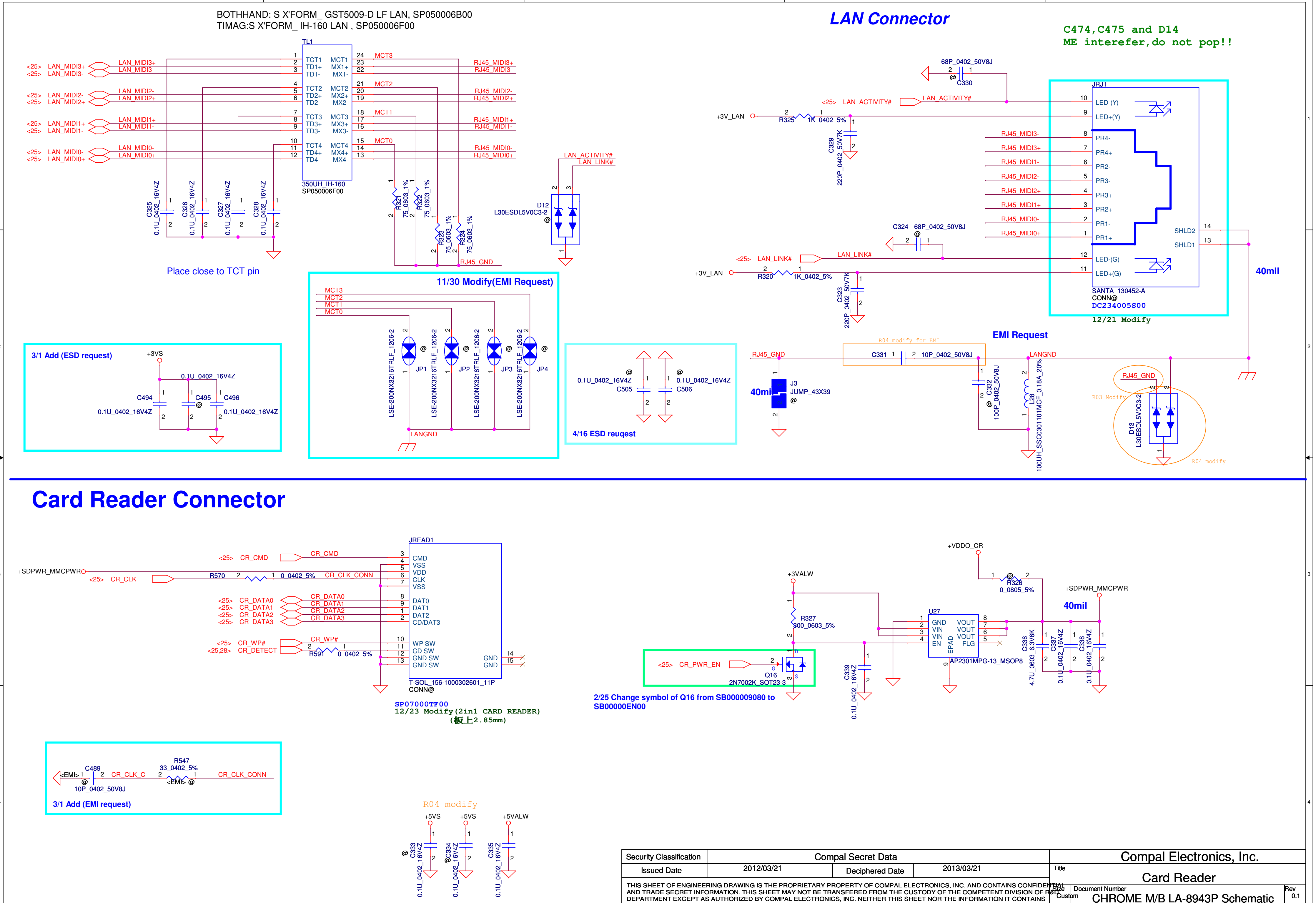


	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/03/21	Deciphered Date	2013/03/21	Title: LAN Boardcom 57785

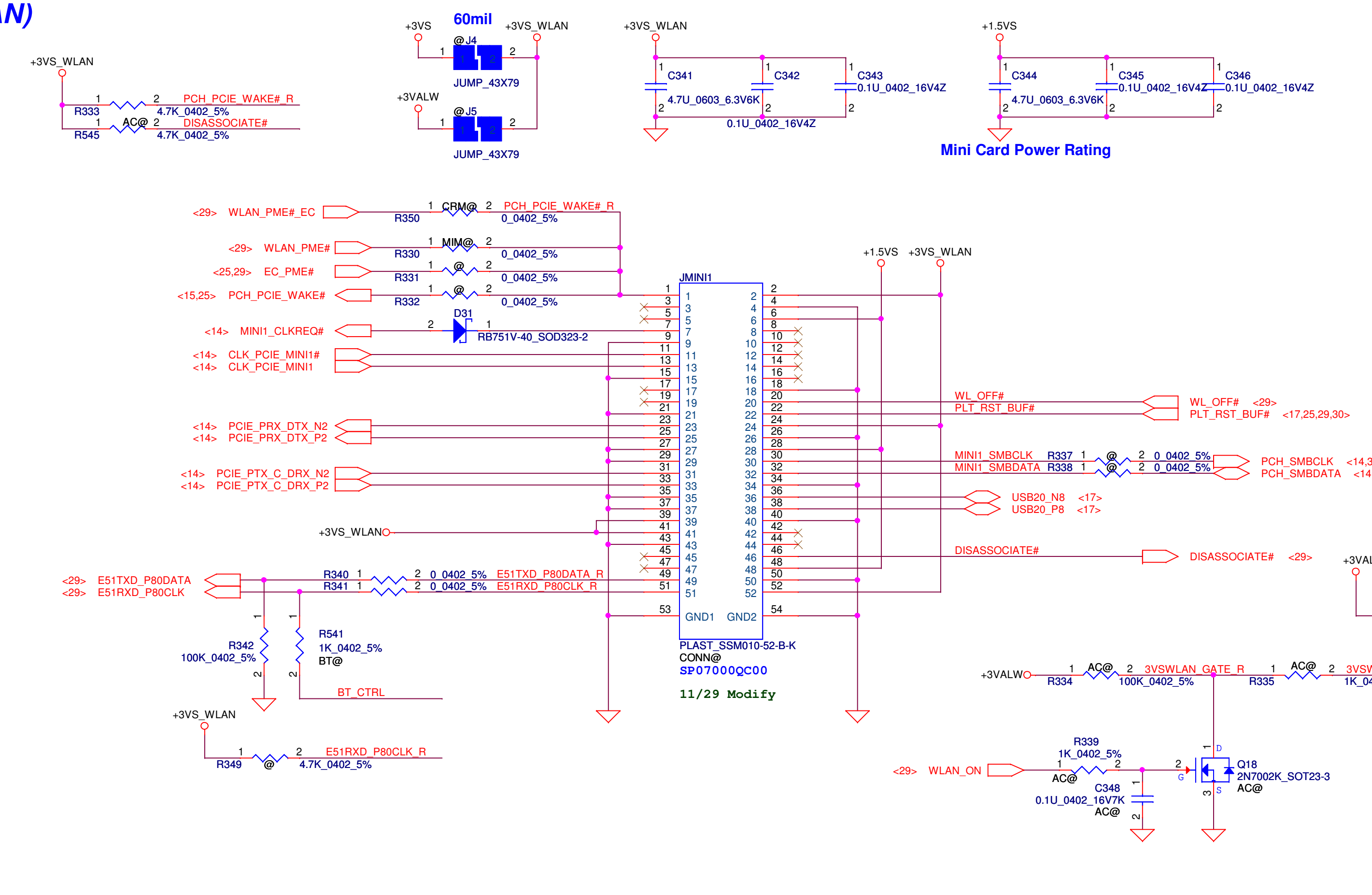
Size	Document Number	Rev
Custom	CHROME M/B LA-8943P Schematic	0.1

Date: Friday, August 10, 2012 | Sheet 25 of 45



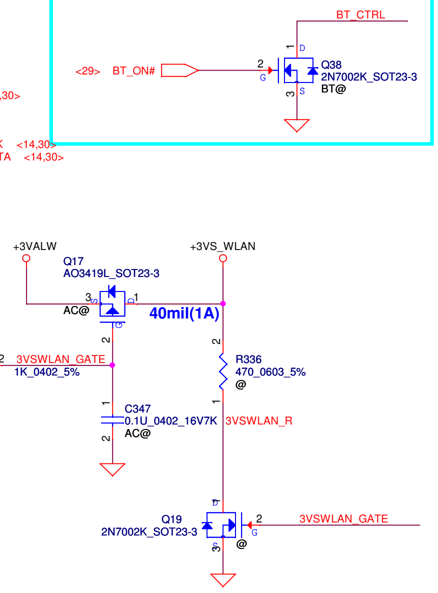
Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/03/21	Deciphered Date	2013/03/21	Title: Card Reader
				Size: Custom; Document Number: CHROME M/B LA-8943P Schematic; Rev: 0.1
				Date: Friday, August 10, 2012; Sheet 26 of 45

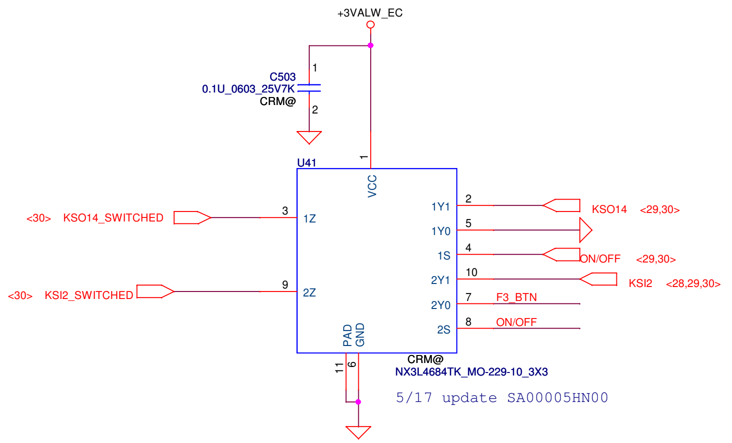
MINI CARD(Wireless LAN)

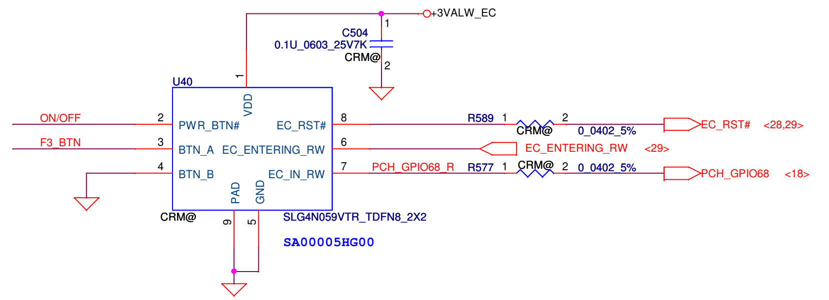


WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H



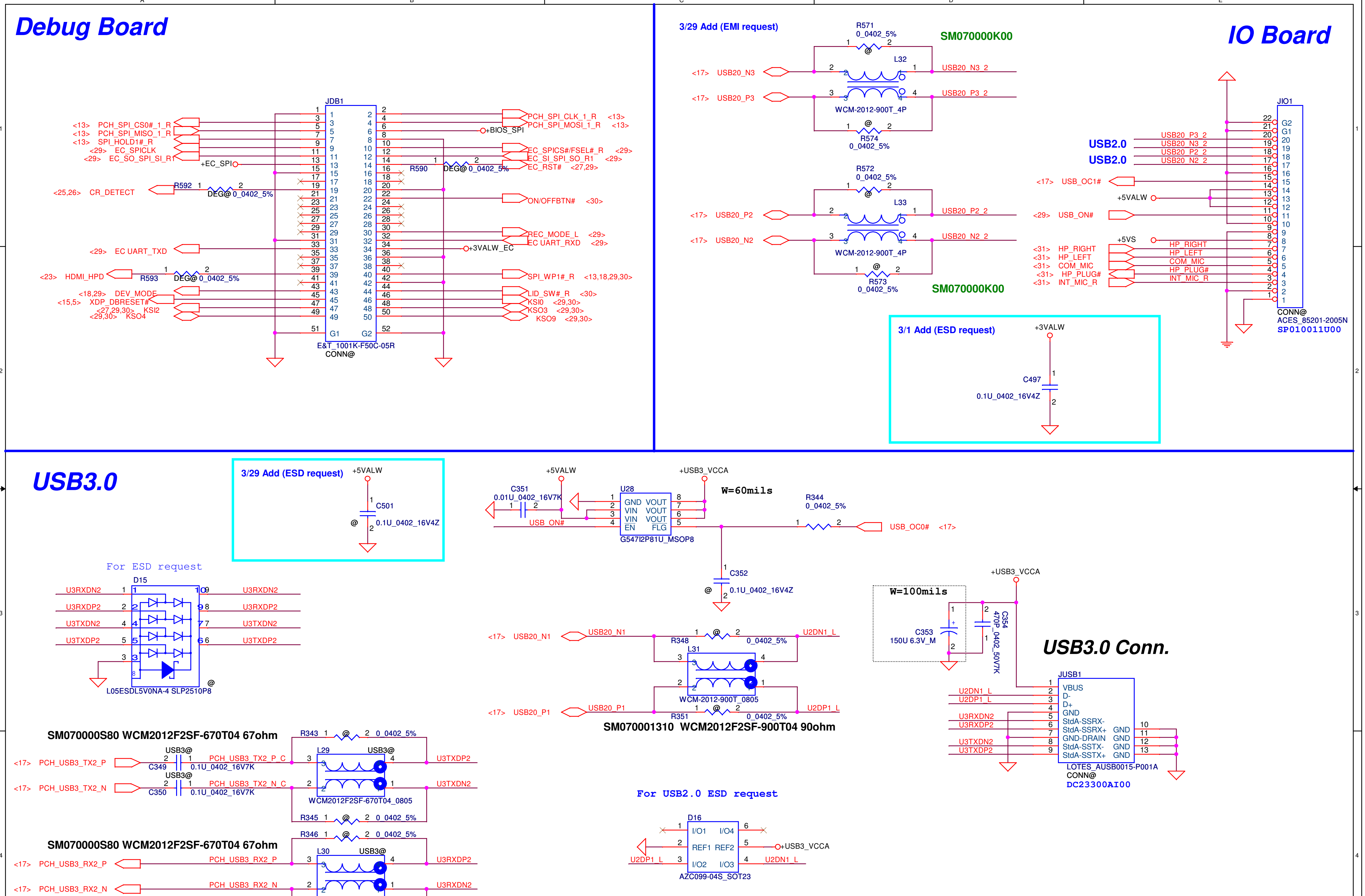




Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

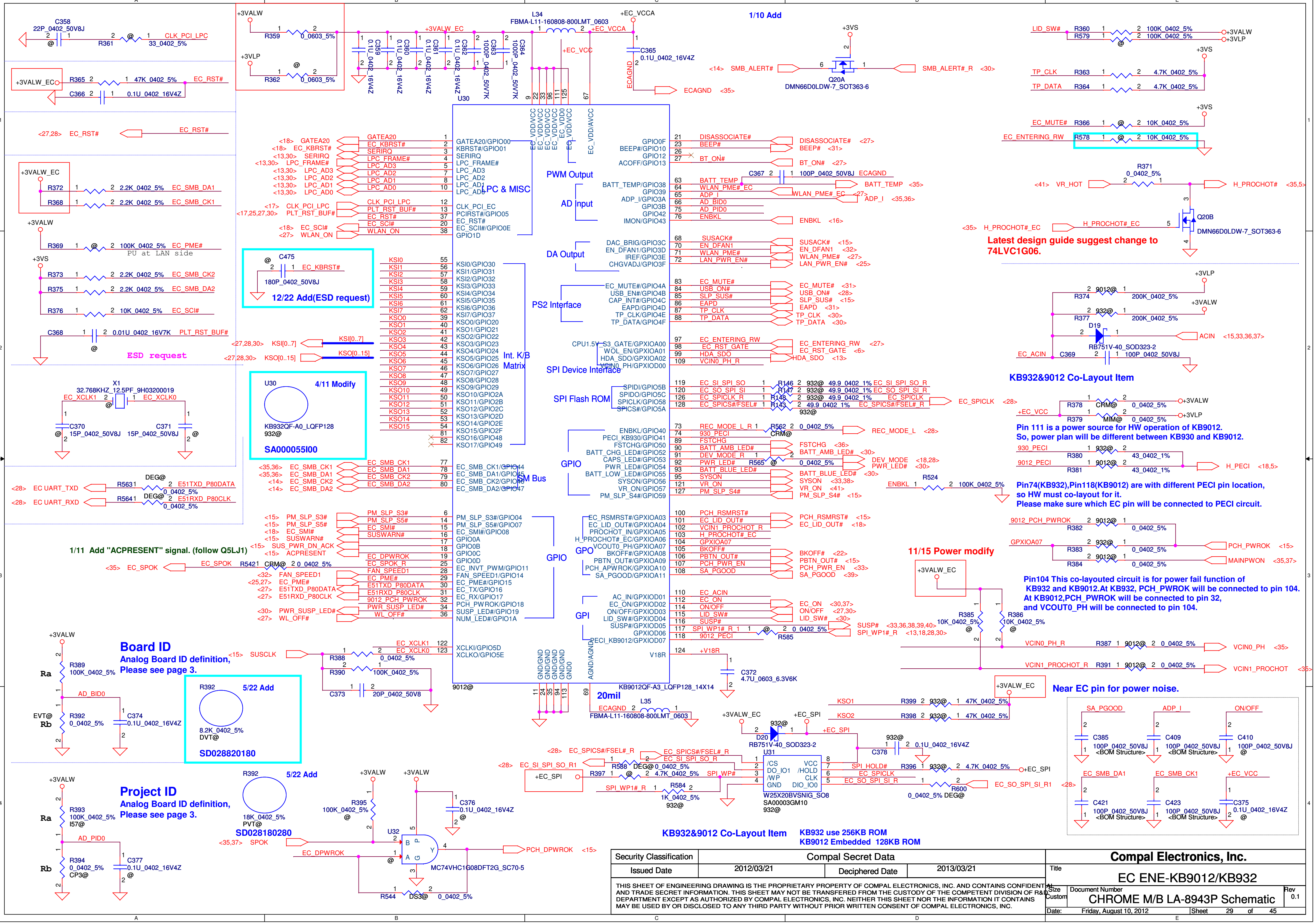
Title	MINI CARD (WLAN)/Holeless RST	
Size: Custom	Document Number: CHROME M/B LA-8943P Schematic	Rev: 0.1
Date: Friday, August 10, 2012	Sheet 27 of 45	



Security Classification	Compal Secret Data			Title
Issued Date	2012/03/21	Deciphered Date	2013/03/21	IO Board & USB3.0

Size	Document Number	Rev
Custom	CHROME M/B LA-8943P Schematic	0.1

Date: Friday, August 10, 2012


1/10 Add
Latest design guide suggest change to 74LVC1G06.
KB932&9012 Co-Layout Item
Pin 111 is a power source for HW operation of KB9012.
So, power plan will be different between KB930 and KB9012.
Pin74(KB932),Pin118(KB9012) are with different PECI pin location,
so HW must co-layout for it.
Please make sure which EC pin will be connected to PECI circuit.
11/15 Power modify
Pin104 This co-layouted circuit is for power fail function of KB932 and KB9012.At KB932, PCH_PWROK will be connected to pin 104.
At KB9012,PCH_PWROK will be connected to pin 32,
and VCOUT0_PH will be connected to pin 104.
Near EC pin for power noise.
12/22 Add(ESD request)
ESD request
4/11 Modify
KB932QF-A0_LQFP128
SA000055I00
1/11 Add "ACPRESENT" signal. (follow Q5LJ1)
Board ID
Analog Board ID definition,
Please see page 3.
5/22 Add
SD028820180
Project ID
Analog Board ID definition,
Please see page 3.
SD028180280
KB9012FQ-A3_LQFP128_14X14
U30
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
20mil
KB932&9012 Co-Layout Item
KB932 use 256KB ROM
KB9012 Embedded 128KB ROM
W25X20BVSNIG_SO8
MC74VHC1G08DFT2G_SC70-5
Security Classification
Compal Secret Data
Issued Date
2012/03/21
Deciphered Date
2013/03/21
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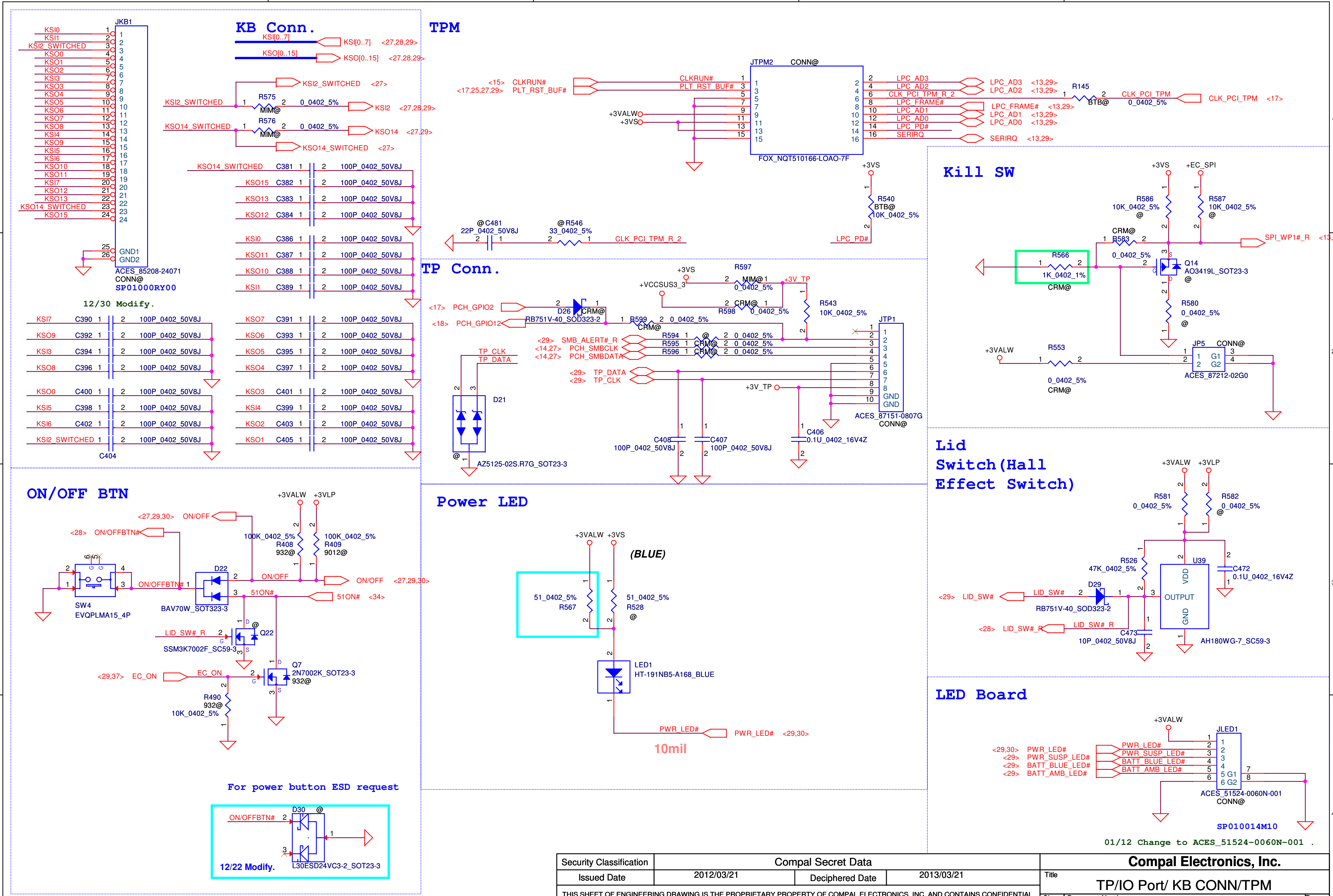
Compal Electronics, Inc.
Title
EC ENE-KB9012/KB932
Size Custom
Document Number
CHROME M/B LA-8943P Schematic
Rev 0.1
Date: Friday, August 10, 2012
Sheet 29 of 45



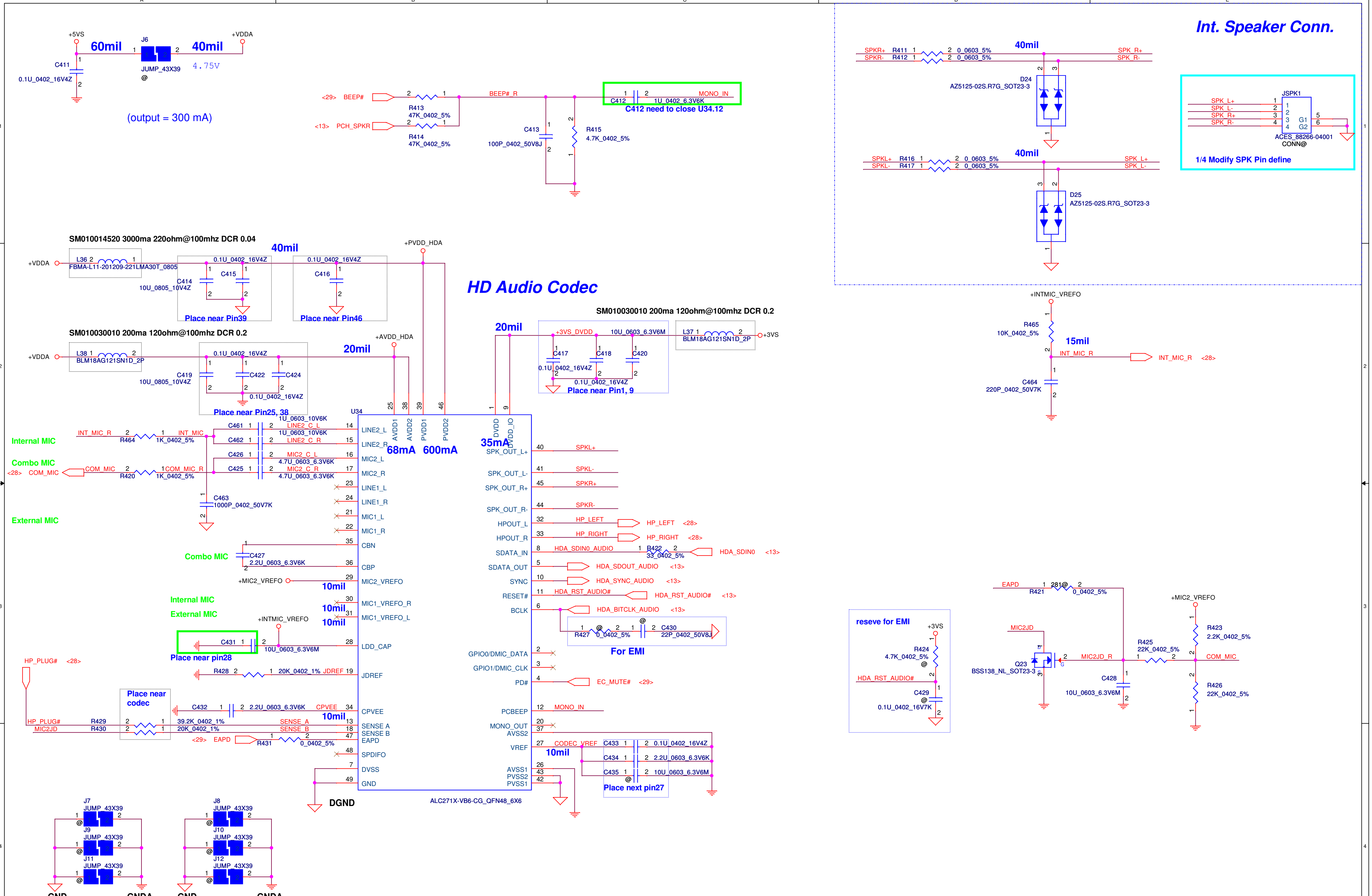
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: TP/IO Port/ KB CONN/TPM

Size: Custom | Document Number: CHROME M/B LA-8943P Schematic | Rev 0.1

Date: Friday, August 10, 2012 | Sheet 30 of 45



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/03/21	Deciphered Date	2013/03/21	Title: HD Audio Codec ALC271X
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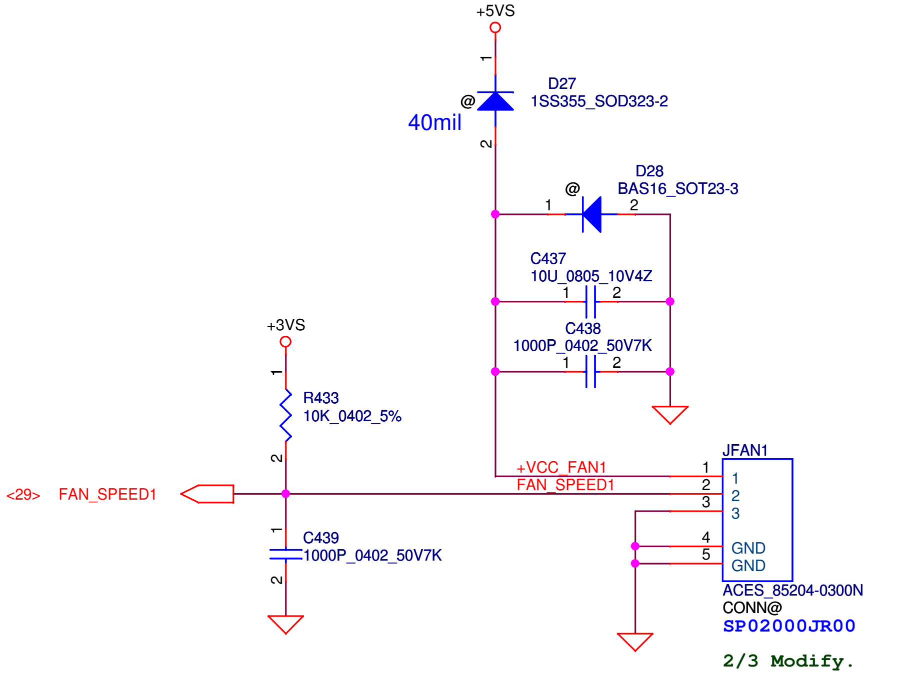
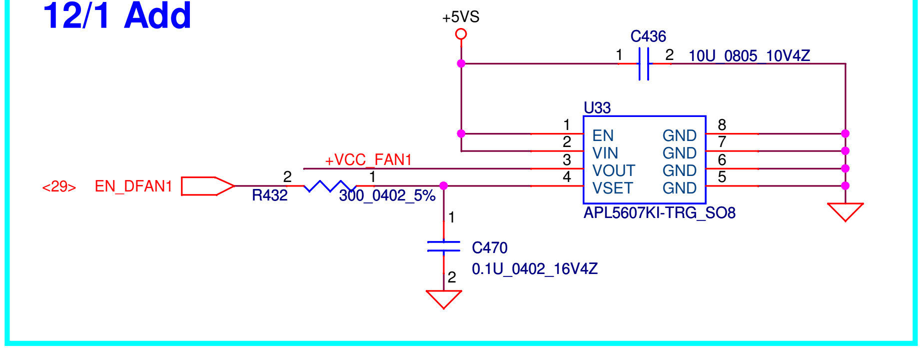
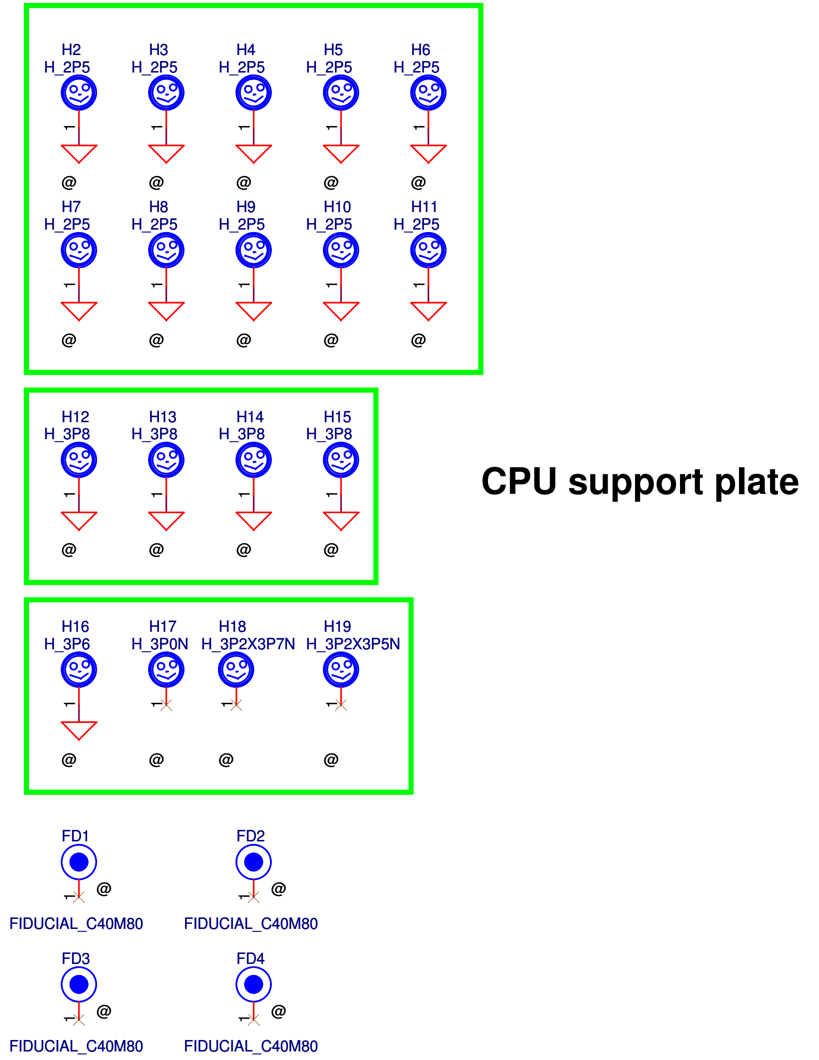
				Date: Friday, August 10, 2012; Sheet 31 of 45

FAN1 Conn



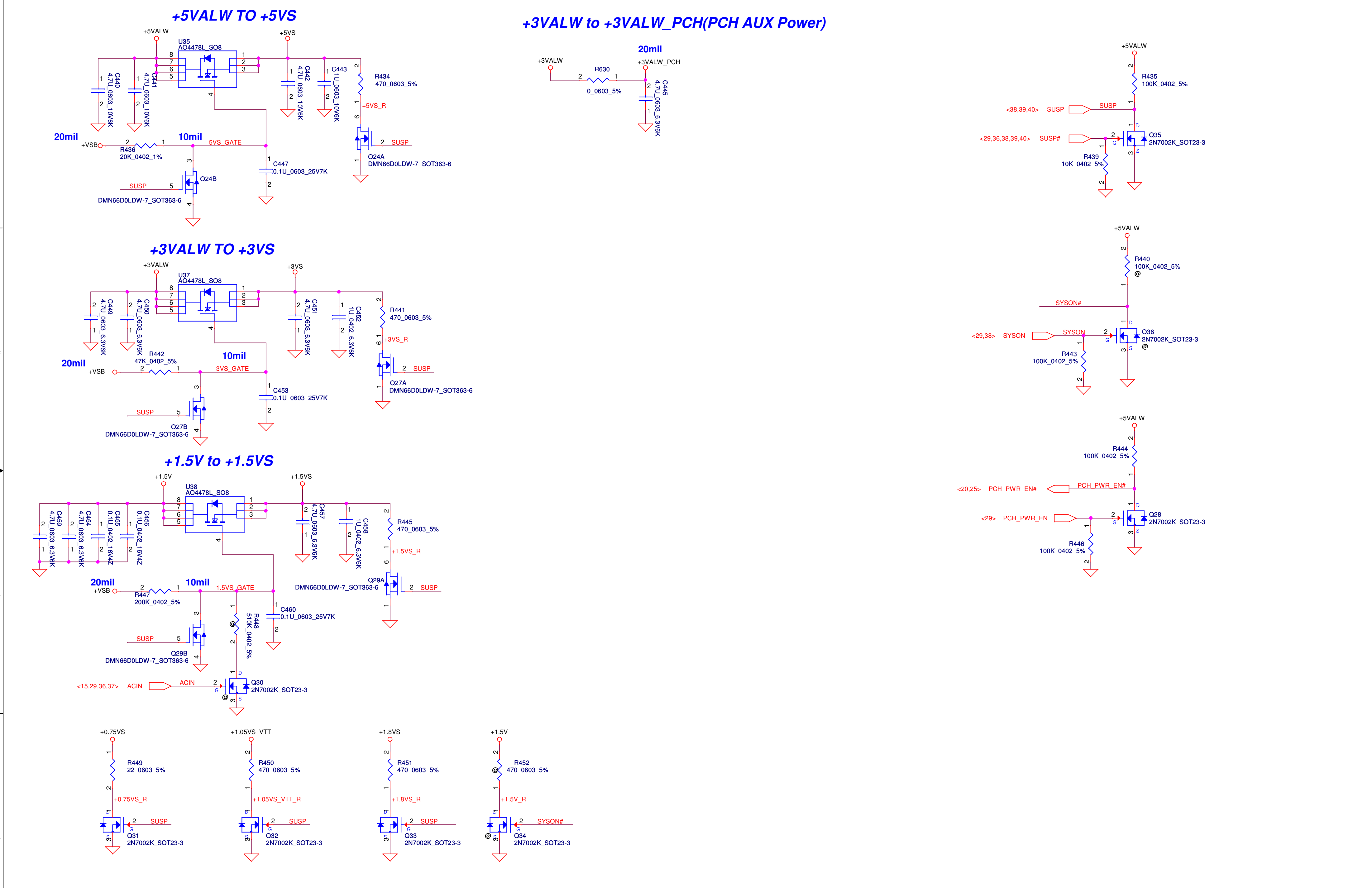
12/1 Add





Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.		
Title: FAN & Screw Hole		
Size: Custom	Document Number: CHROME M/B LA-8943P Schematic	Rev: 0.1
Date: Friday, August 10, 2012	Sheet 32 of 45	



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/03/21	Deciphered Date	2013/03/21	Title: DC Interface
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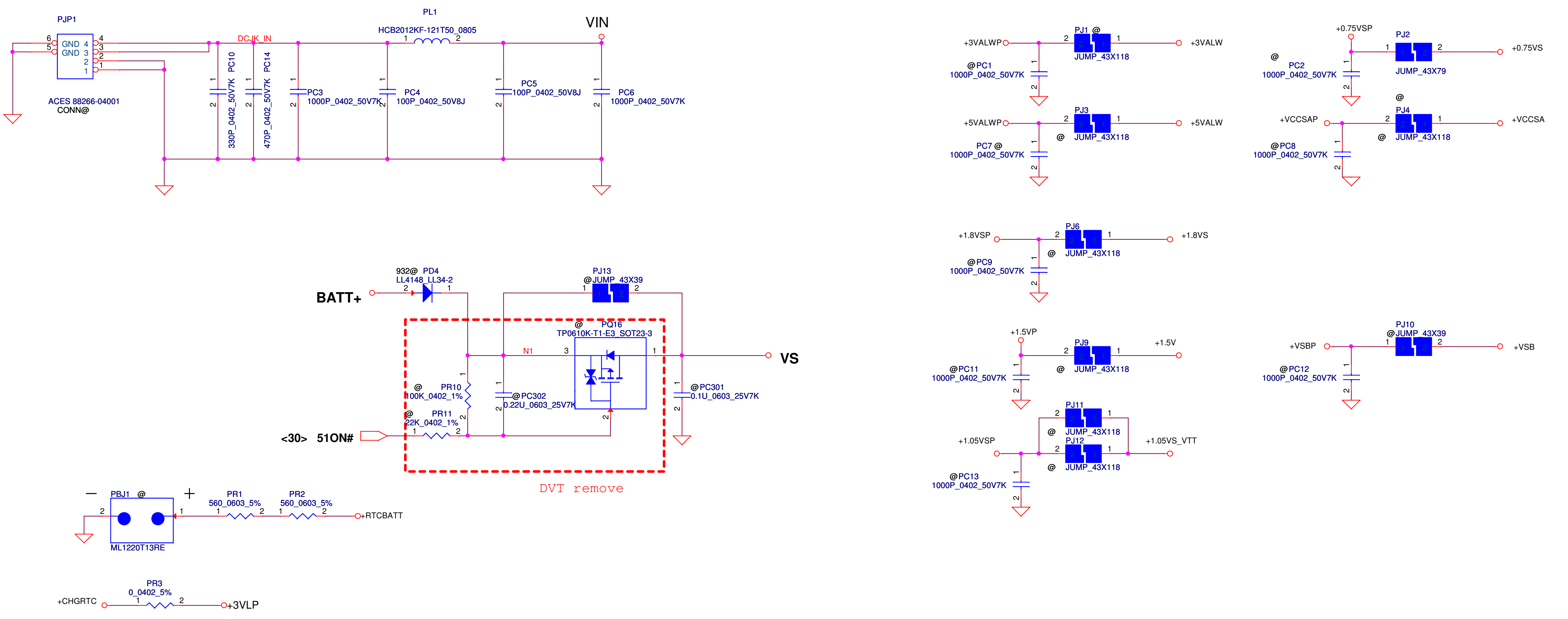
				Date: Friday, August 10, 2012; Sheet 33 of 45



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/03/21	Deciphered Date	2013/03/21	Title: PWR DCIN / Pre-charge
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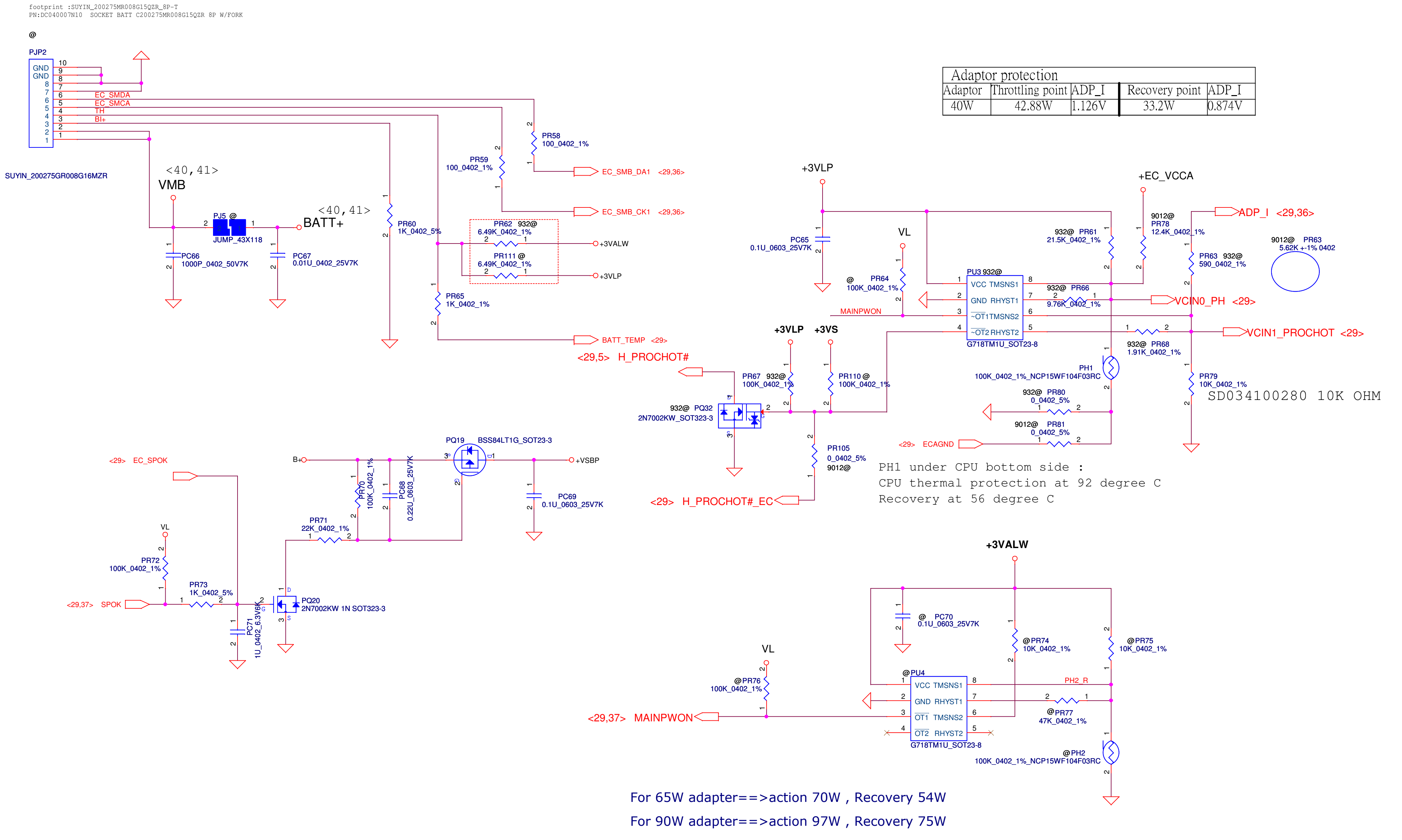
				Date: Friday, August 10, 2012; Sheet 34 of 46



Adaptor protection

Adaptor	Throttling point	ADP_I	Recovery point	ADP_I
40W	42.88W	1.126V	33.2W	0.874V

PH1 under CPU bottom side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C

For 65W adapter==>action 70W , Recovery 54W

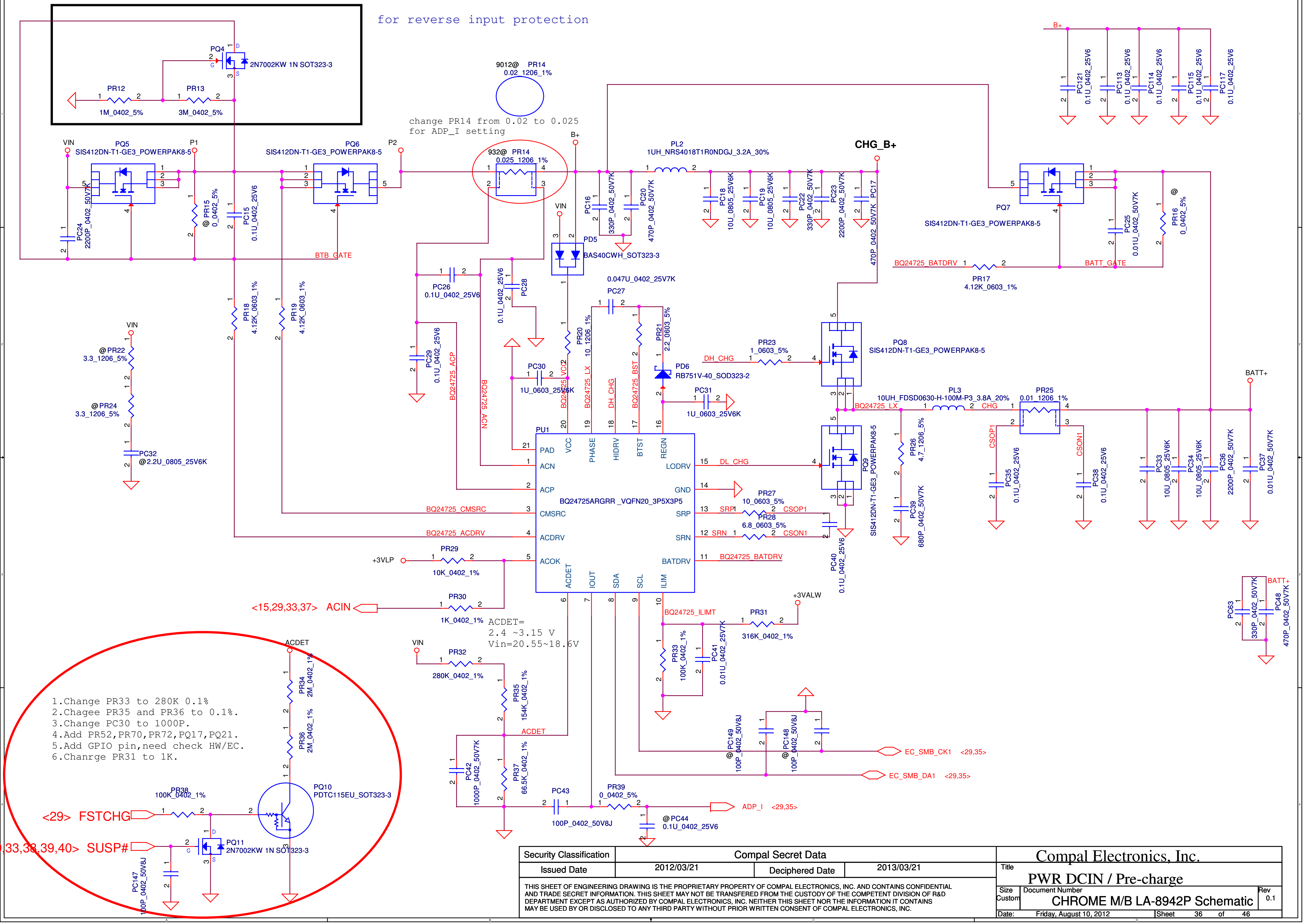
For 90W adapter==>action 97W , Recovery 75W

Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

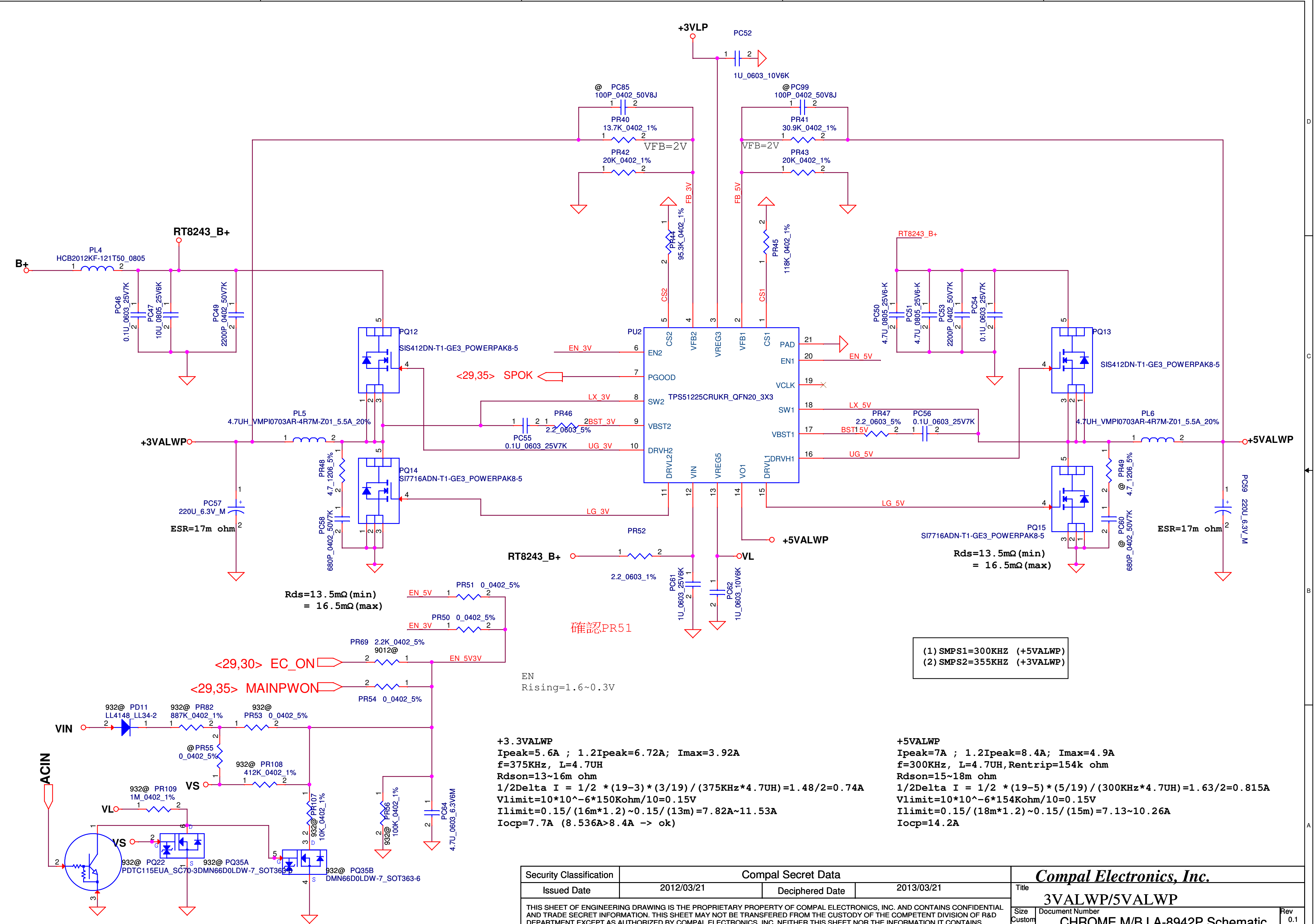
Size: Custom | Document Number: CHROME M/B LA-8942P Schematic | Rev 0.1



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/03/21	Deciphered Date	2013/03/21	Title: PWR DCIN / Pre-charge

Size	Document Number	Rev
Custom	CHROME M/B LA-8942P Schematic	0.1

Date: Friday, August 10, 2012



+3.3VALWP
Ipeak=5.6A ; 1.2Ipeak=6.72A; Imax=3.92A
f=375KHz, L=4.7UH
Rdson=13~16m ohm
1/2Delta I = 1/2 *(19-3)*(3/19)/(375KHz*4.7UH)=1.48/2=0.74A
Vlimit=10*10^-6*150Kohm/10=0.15V
Ilimit=0.15/(16m*1.2)~0.15/(13m)=7.82A~11.53A
Iocp=7.7A (8.536A>8.4A -> ok)

+5VALWP
Ipeak=7A ; 1.2Ipeak=8.4A; Imax=4.9A
f=300KHz, L=4.7UH,Rentrip=154k ohm
Rdson=15~18m ohm
1/2Delta I = 1/2 *(19-5)*(5/19)/(300KHz*4.7UH)=1.63/2=0.815A
Vlimit=10*10^-6*154Kohm/10=0.15V
Ilimit=0.15/(18m*1.2)~0.15/(15m)=7.13~10.26A
Iocp=14.2A

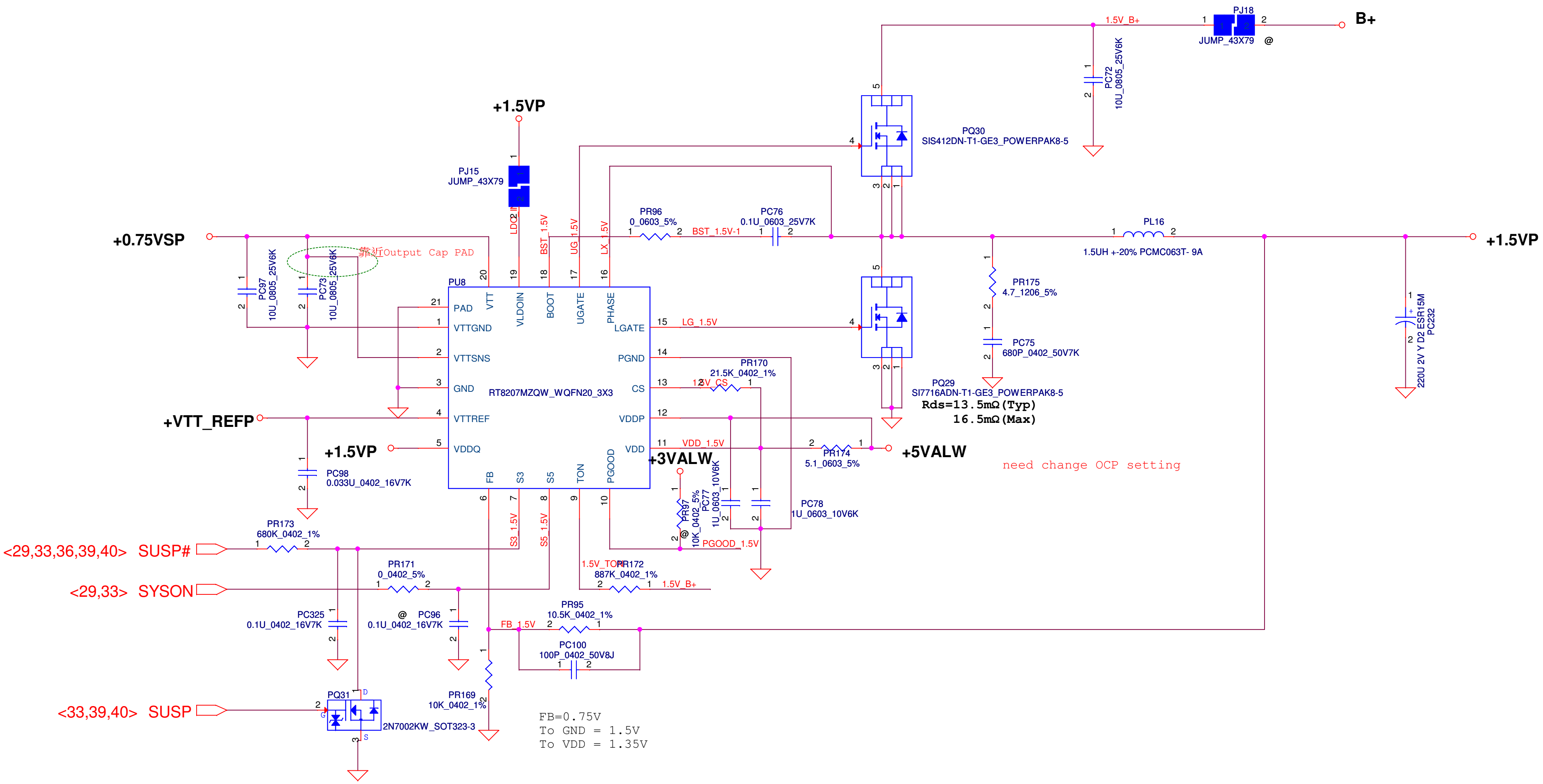
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size: Custom | Document Number: CHROME M/B LA-8942P Schematic | Rev 0.1

Date: Friday, August 10, 2012 |



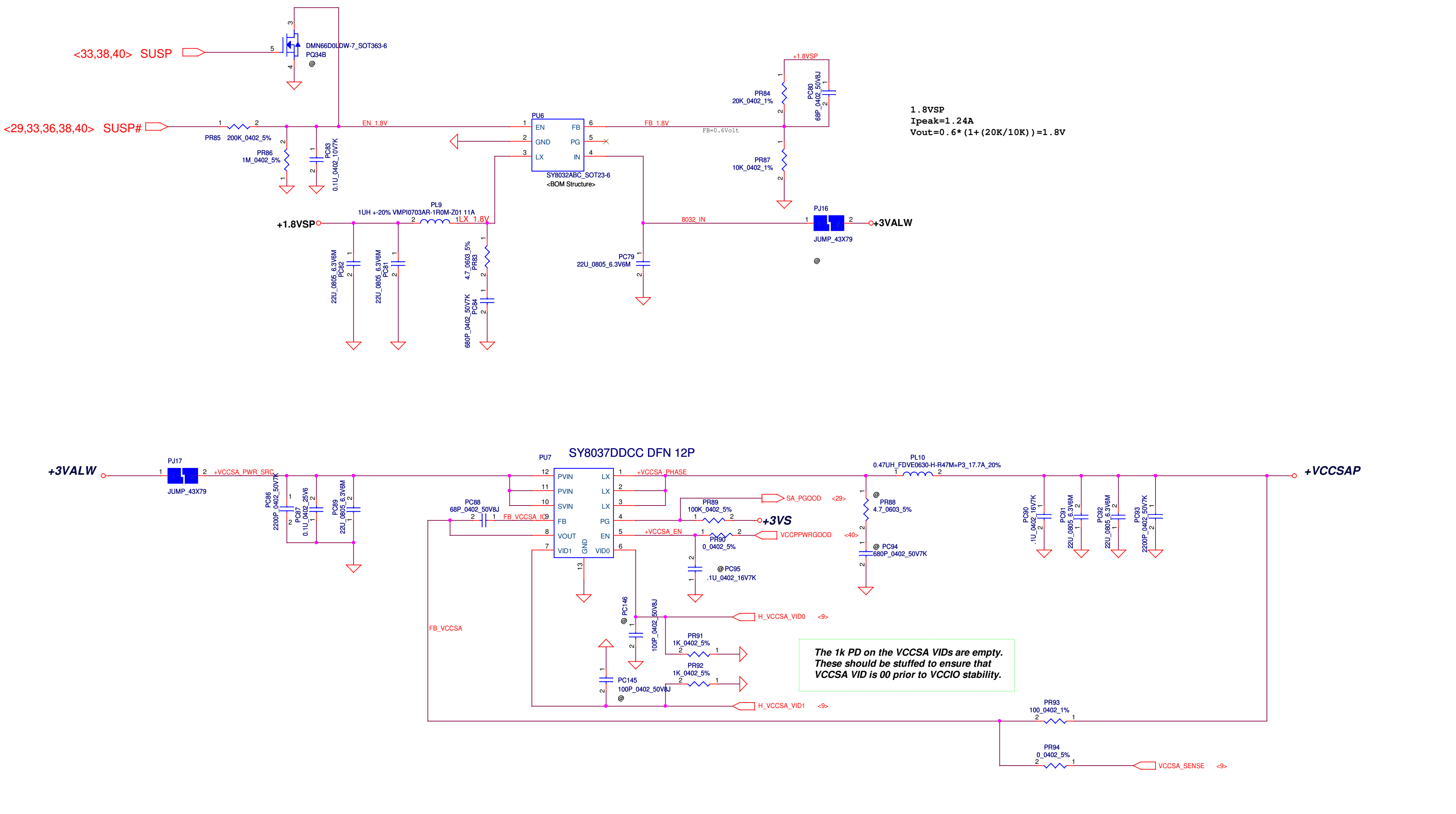
STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)
Note: S3 - sleep ; S5 - power off					

<Vo=1.5V> VFB=0.75V
V=0.75*(1+10K/10.5K)=1.52V
Fsw=286K to 200KHz

Cout ESR=17m ohm Rdson(max)=16.5 mohm Rdson(typ)=13.5 mohm.
Ipeak=12 A, Imax=8.4A, Iocp=14.4A

Delta I=((Vin-Vo)*(Vo/Vin))/(L*Fsw)=2.195A
=>1/2Delta I=1.099A

Iocpmax=((21.5K*11uA)/0.0135)+0.5 delta I= A
Iocpmin=((21.5K*9uA)/(0.0165))+0.5 delta I=15.6A




```
1.8VSP
Ipeak=1.24A
Vout=0.6*(1+(20K/10K))=1.8V
```

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

```
+VCC_SAP
TDC 4.2A
Peak Current  6A
OCP current 7.2A
```

VID [0]	VID[1]	VCCSA Vout(ULV only)
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

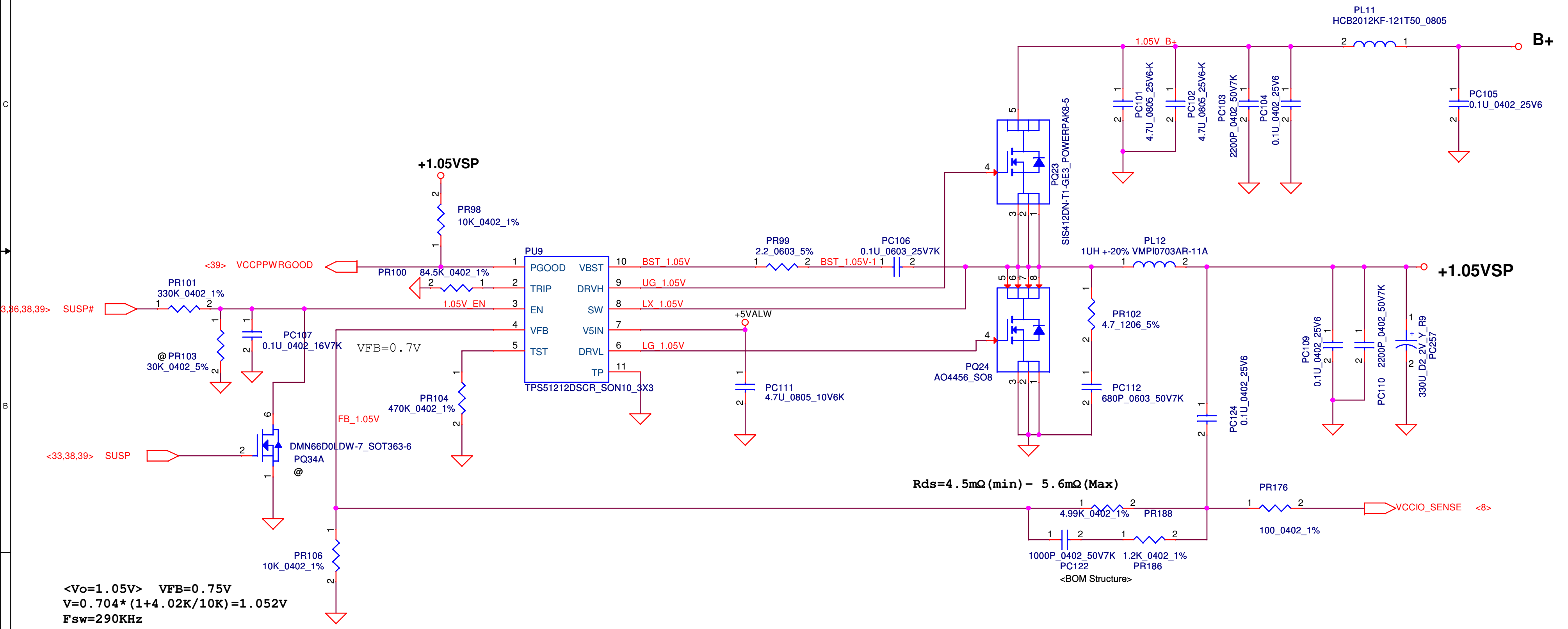
output voltage adjustable network

Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: PWR +VCCSAP

Size: C | Document Number: CHROME M/B LA-8942P Schematic | Rev: 0.1



<Vo=1.05V> VFB=0.75V
V=0.704*(1+4.02K/10K)=1.052V
Fsw=290KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=15.6A, Imax=10.92A, Iocp=18.72A

Delta I=((19-1.05)*(1.05/19))/(L*Fsw)=2.06A

Iocpmax=((15K*11uA)/0.0045)+1.665A=23.54A
Iocpmin=((15K*9uA)/(0.0056*1.3))+1.665A=19A
Iocp=A

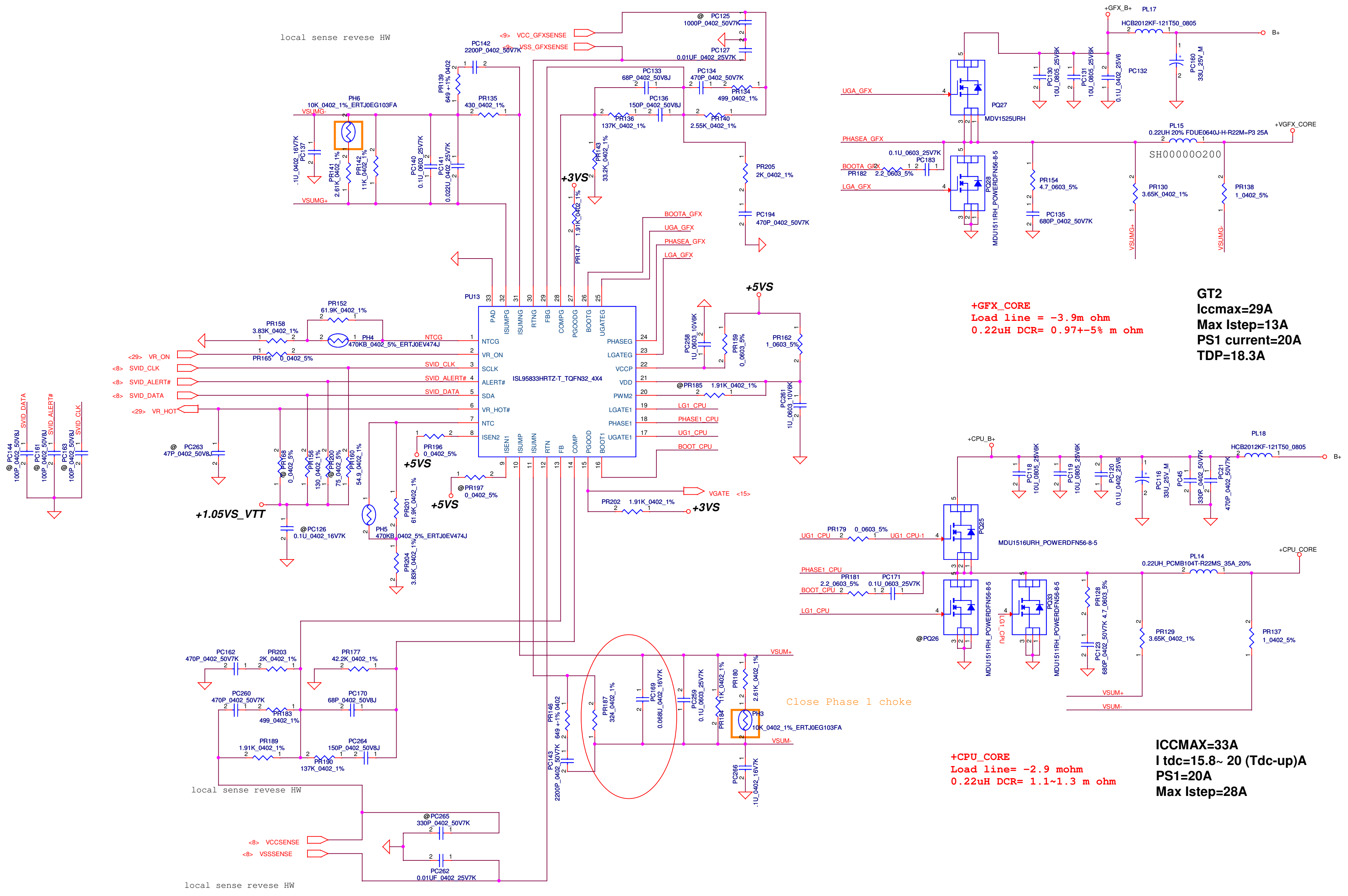
Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: PWR +1.05VS_VCCPP/+0.75VSP

Size: Custom | Document Number: CHROME M/B LA-8942P Schematic | Rev 0.1

Date: Friday, August 10, 2012



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/03/21	Deciphered Date	2013/03/21	Title: CPU/GFX_CORE
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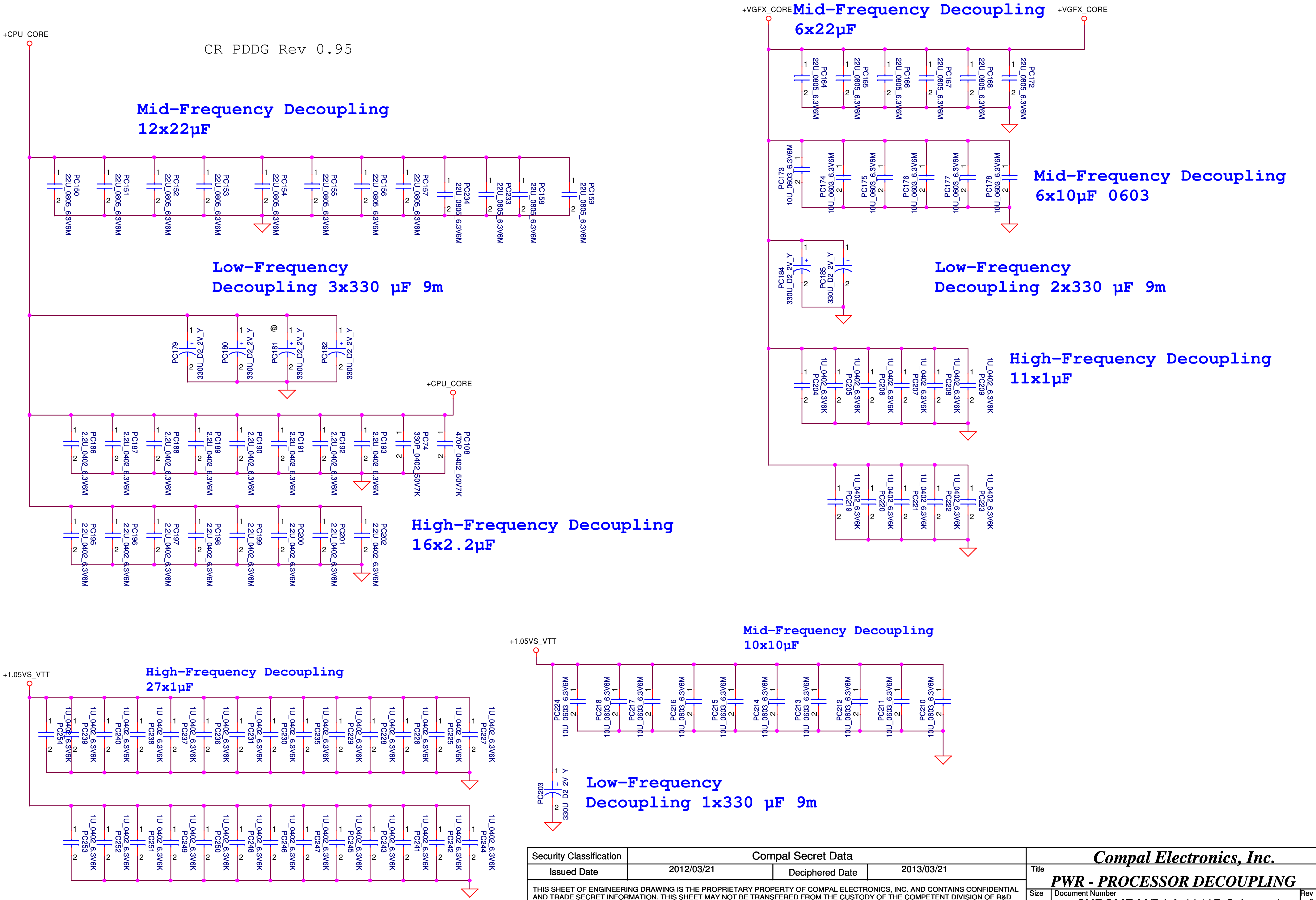
				Date: Friday, August 10, 2012; Sheet 41 of 46



Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: **PWR - PROCESSOR DECOUPLING**

Size | Document Number: CHROME M/B LA-8942P Schematic | Rev 0.1

Date: Friday, August 10, 2012 | Sheet 42 of 46

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Modify DCIN/Pre-change power circuit	0.1	34	Add PC301 330P_0402_50V7K, PC302 470P_0402_50V7K for EMI solution	2012/4/5	EVT
2		Modify Battery CONN/OTP power circuit	0.1	35	Add PR80 0ohm to GND for BOM control (9012 AGND)	2012/4/5	EVT
3		Modify CHARGER	0.1	36	Add PC16,PC63 330P_0402_50V7K, PC20, PC48 470P_0402_50V7K, PC113, PC114, PC115, PC117, PC121 0.1U_0402_25V6 PR26 4.7_1206_5%, PC39 680P_0402_50V7K for EMI solution	2012/4/5	EVT
4		Modify 3VALWP/5VALWP power circuit	0.1	37	Add Snubber PR48 4.7_1206_5%, PC58 680P_0402_50V7K for EMI solution	2012/4/5	EVT
5		Modify 1.5VP/0.75VSP power circuit	0.1	38	Add Snubber PR175 4.7_1206_5%, PC75 680P_0402_50V7K for EMI solution	2012/4/5	EVT
6		Modify 1.05VS power circuit	0.1	40	Delete PR105 5.1K_0402_1%; PR178 0_0402_5%, Add PR188 4.99K_0402_1%; PR186 1.2K_0402_1%, PC122 1000P_0402_50V7K; PC124 0.1U_0402_25V6 for improve load response	2012/4/5	EVT
7		Modify CPU/GFX_CORE power circuit	0.1	41	Add PC45 330P_0402_50V7K, PC21 470P_0402_50V7K for EMI solution Add PC169 0.047I_0402_25V7K, change PR187 from 523 to 348_0402_1% change PR135 from 412 to 430_0402_1%	2012/4/5	EVT
8		Modify CPU/GFX_CORE power circuit	0.1	41	change PL14 from 0.22U_PCMB104T-R22MS_35A_20% to 0.22UH MMD-10RCZ-R22M-28A (from H=3 to H=4) change PR201, PR152 from 27.4K to 61.9K_0402_1%, change PH4,PH5 470K_0402_5%(from Thinking to Panasonic) thermal issue	2012/4/5	EVT
9		Modify PROCESSOR DECOUPLING power circuit	0.1	42	Add PC74 330P_0402_50V7K, PC108 470P_0402_50V7K for EMI solution	2012/4/5	EVT
10		Modify DCIN/Pre-change power circuit	0.1	34	Sawp PC10 and PC301; Sawp PC14 and PC302	2012/4/5	EVT
11		Modify Battery CONN/OTP power circuit	0.1	35	Add PR105 0ohm to GND for BOM control (9012 H_PROCHOT#_EC) change PR61 from 21K to 21.5K and PR66 from 9.53K to 9.76K for 92 throttling and 56C recovery	2012/4/18	EVT
12		Modify Battery CONN/OTP power circuit	0.1	35	Delete PR78 and add PR61, PR63 for EC932, change PR66 from 9.53kohm to 9.76k ohm, OTP setting 92C thermal protection, 56C recovery	2012/4/26	EVT
13		Modify 3VALWP/5VALWP power circuit	0.1	37	Change PR56 from 402K to 100K for 3V/5V enable setting, Add PR53 for 3V/5V enable setting.	2012/4/26	EVT
14		Modify CPU/GFX_CORE power circuit	0.1	41	change PR187 from 348 to 324 for OCP 40A fine tune, change PC169 from 0.047U to 0.068U (RC match)	2012/4/26	EVT
15		Modify CHARGER	0.1	36	change PC22 from 0.1U_0402_25V6 to 330P_0402_50V7K	2012/5/2	EVT

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Modify Prochot# setting from KB9012 to G718(EVT MEMO introction)	0.2	35	change PR63 from 2.26K to 590 ohm, PR68 from 9.1 to 1.91K From 46.2W~38W to 42.8W~33.2W	2012/5/7	EVT
2		Modify Battery CONN/OTP power circuit Modify 3VALWP/5VALWP power circuit	0.2	35 37	Sawp PR81 and PR82 location leverage Mimic winsows	2012/5/17	DVT
3		Modify Battery CONN/OTP power circuit	0.2	35	Add PR111 between 3VLP and battery connect TH for EC932	2012/5/23	DVT
4		Remove PQ16 PC302 PR10 PR11	0.2	34	Remove 51ON# RC, BATT+ to VS switch	2012/5/23	
5		MAINPWON double pull high.	0.2	35	Remove PR64	2012/5/23	
6		Modify 3v5v EN pin voltage (from 4.9V to 4.524V) for EN pin rating.	0.2	35	Change PR108 from 316K to 412K.	2012/5/23	
7		Modify 3v5v EN pin voltage for EN pin rating.	0.3	35	Change PR82 from 1000K to 887K.	2012/7/9	PVT
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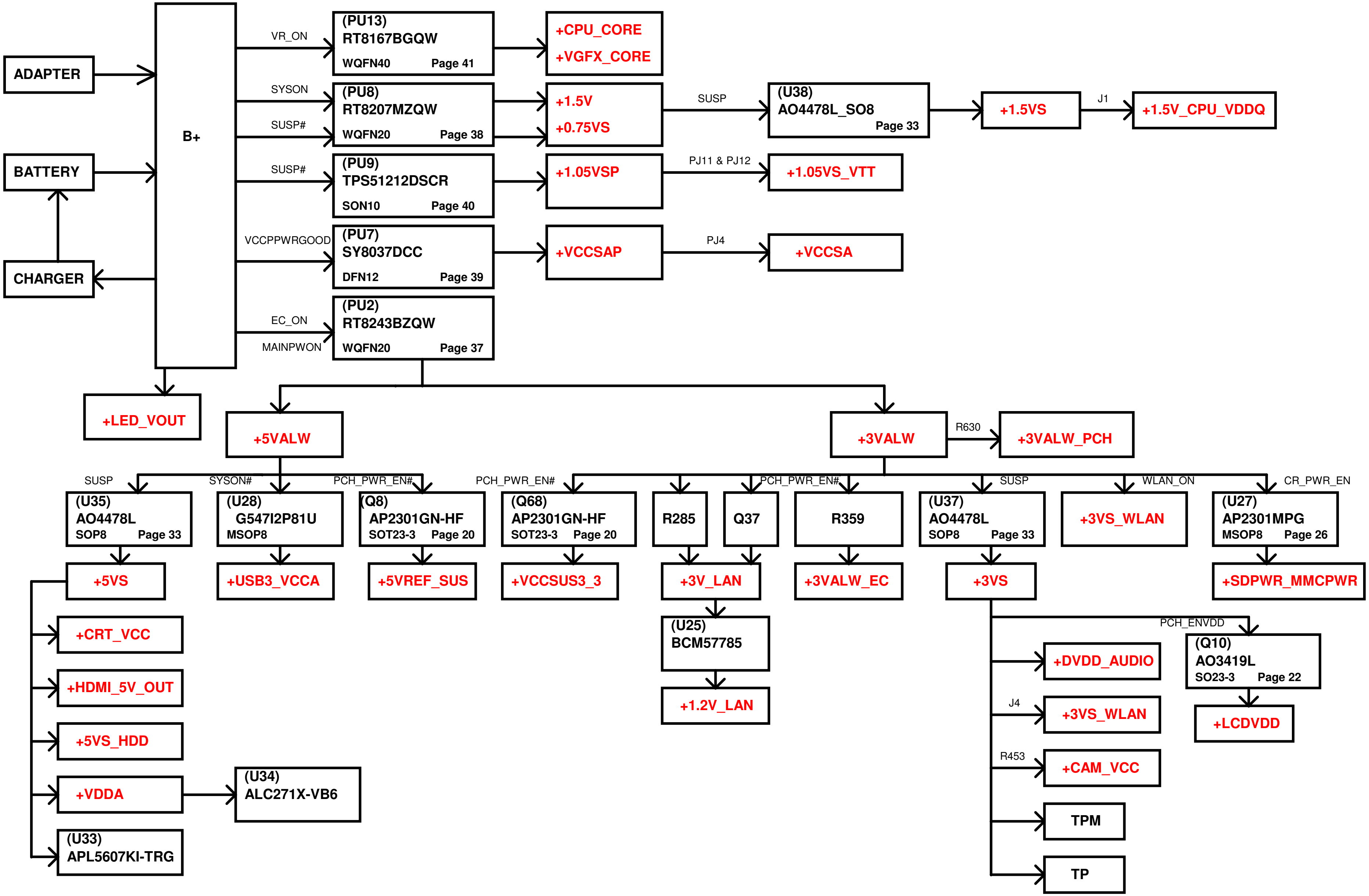
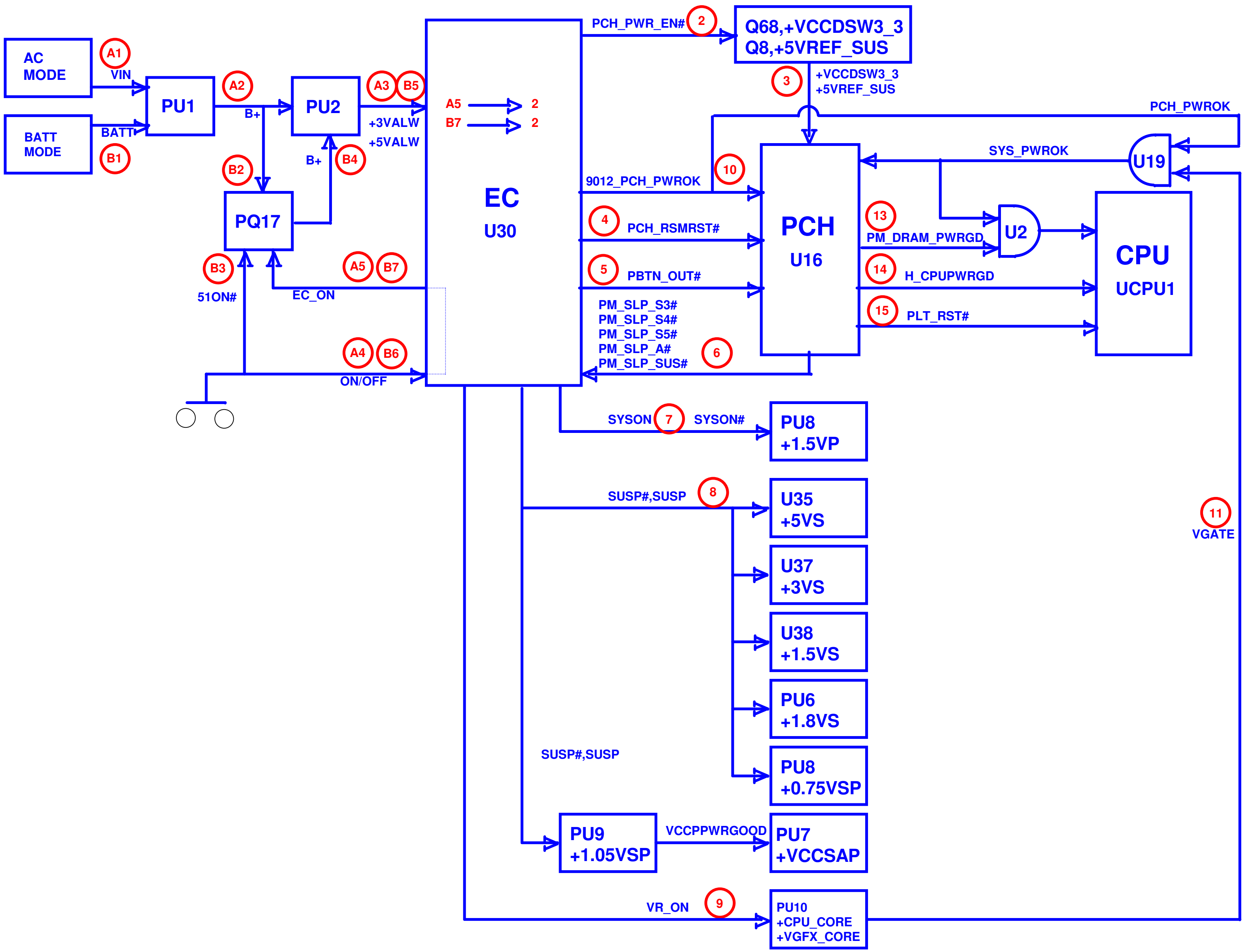


Security Classification	Compal Secret Data		
Issued Date	2012/03/21	Deciphered Date	2013/03/21

Compal Electronics, Inc.

Title: **Power Rail**

Size: Custom | Document Number: **CHROME M/B LA-8942P Schematic** | Rev 0.1



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Date: Friday, August 10, 2012 |