

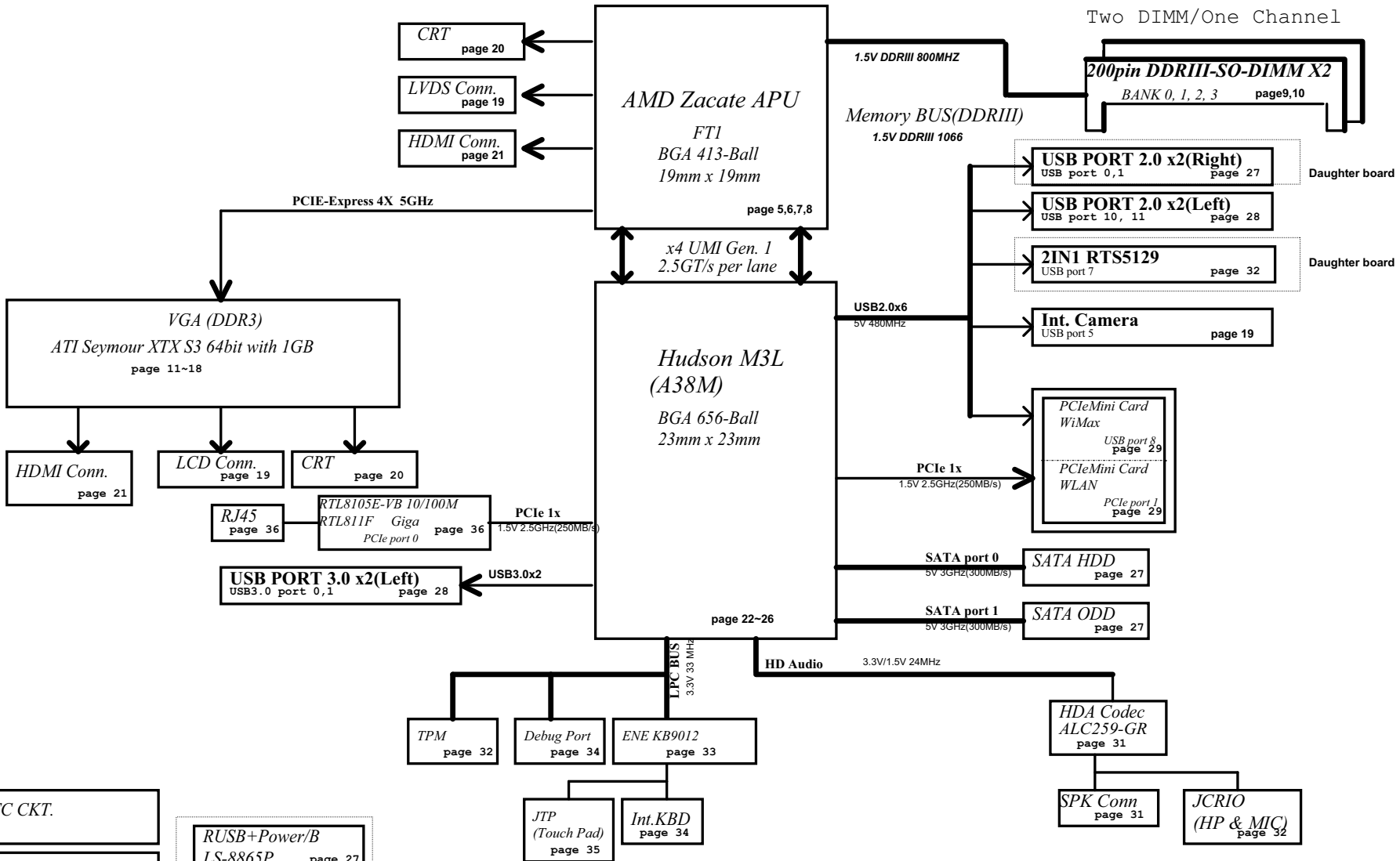
VBLE4 / VBLE5

Eureka

LA-8868P REV 1.0 Schematic

**AMD Brazos 2.0 / Zacate APU / Hudson-M3L FCH
2012-07-12 Rev 1.0**

Security Classification	Compal Secret Data		Title	
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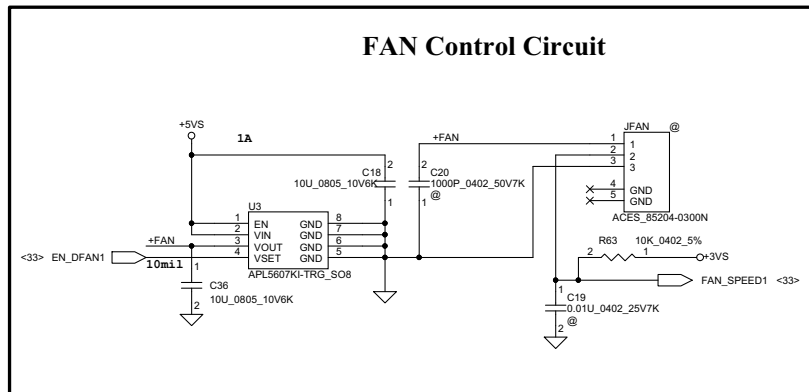
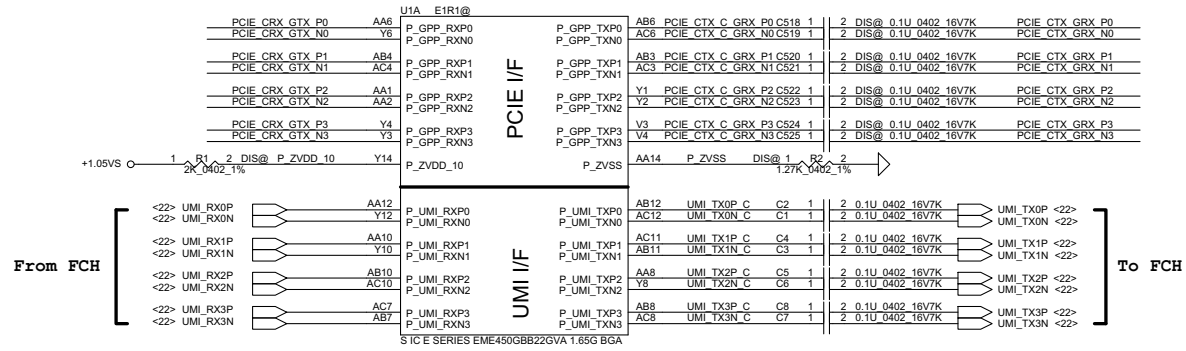
- RTC CKT.
- Power On/Off CKT.
- DC/DC Interface CKT.
- Power Circuit DC/DC

- RUSB+Power/B LS-8865P page 27
- Audio+CR/B LS-8864P page 32
- ODD/B LS-8862P page 27
- TP/B LS-8863P page 35

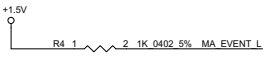
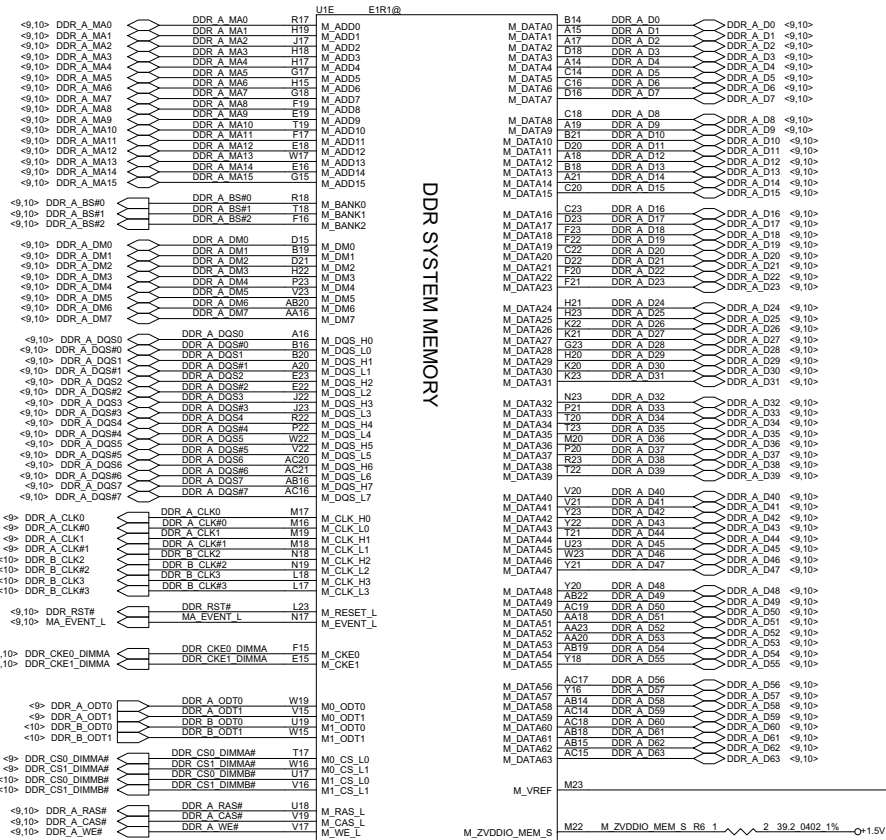
Daughter board

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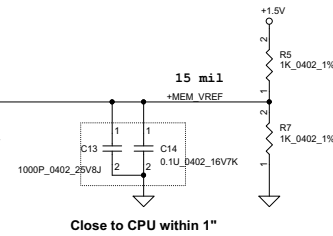
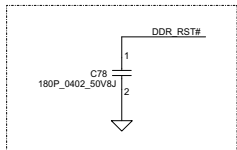
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 <11> PCIE_CTX_GRX_N[3..0] ← PCIE_CTX_GRX_N[3..0]
 <11> PCIE_CRX_GTX_P[3..0] → PCIE_CRX_GTX_P[3..0]
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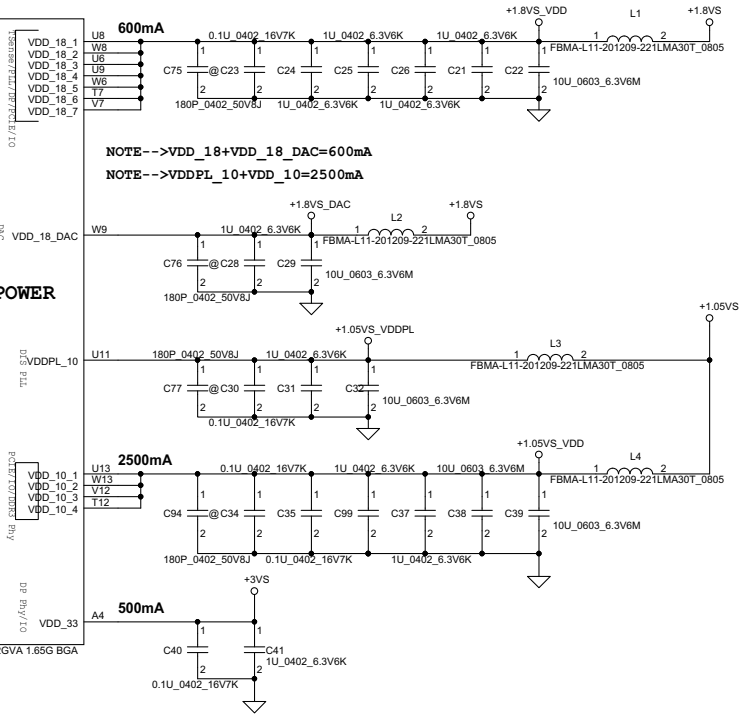
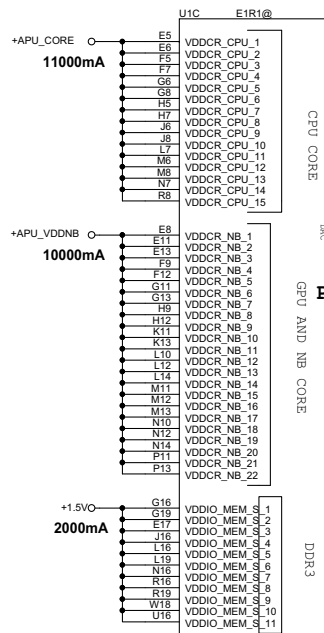
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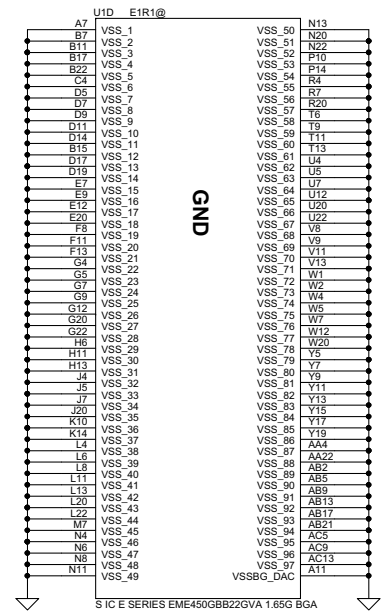
8/6 Add C78 for ESD request



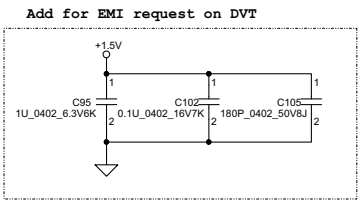
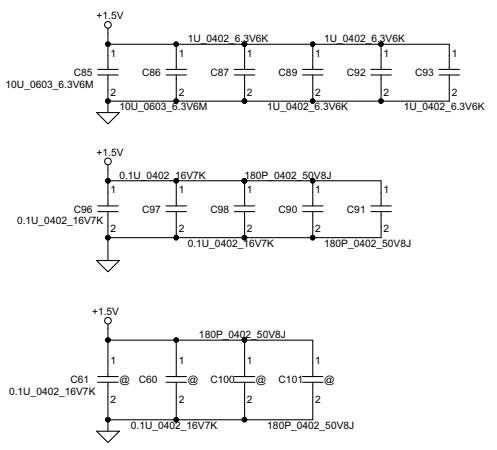
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NOTE-->VDD_18+VDD_18_DAC=600mA
 NOTE-->VDDPL_10+VDD_10=2500mA

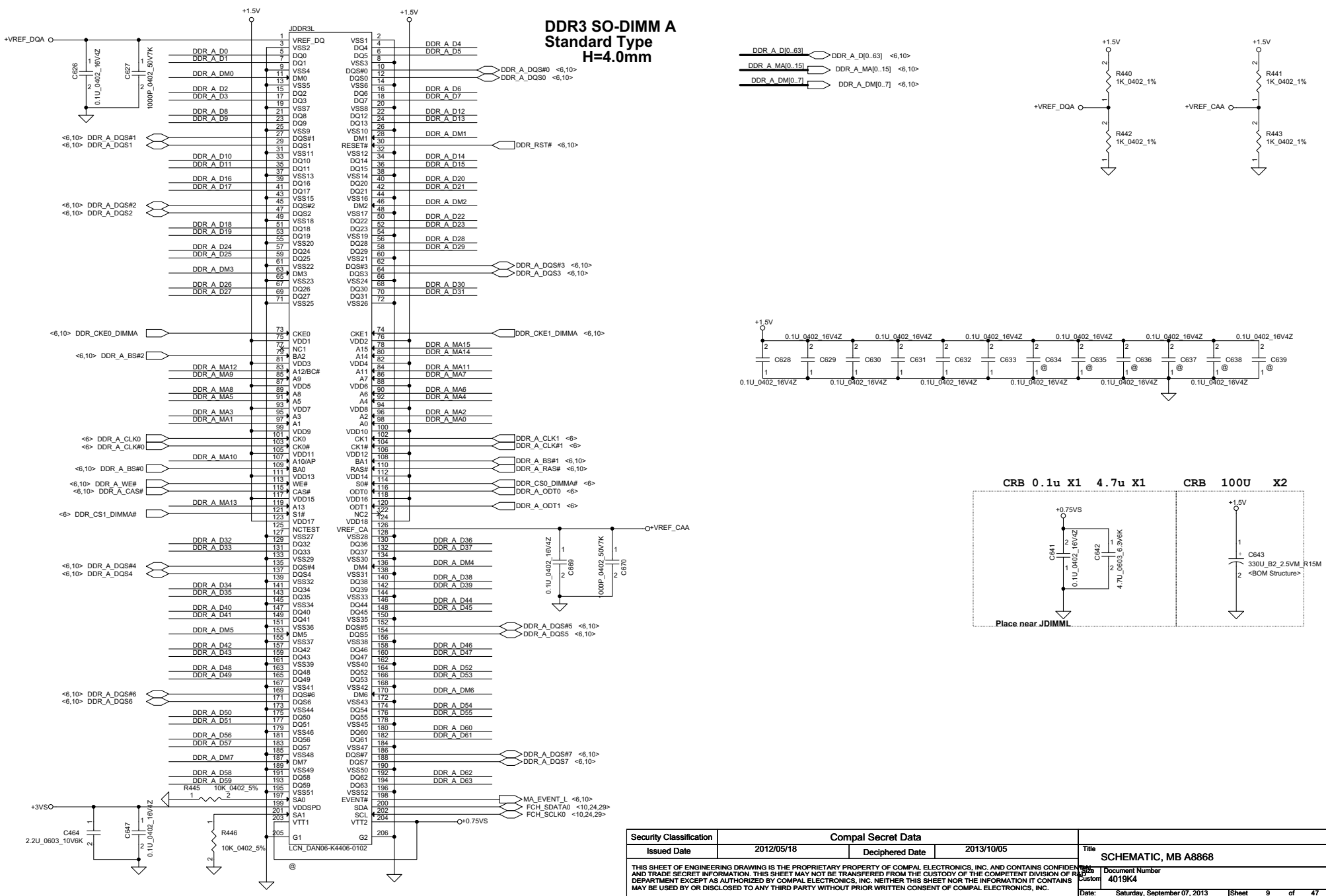


GND



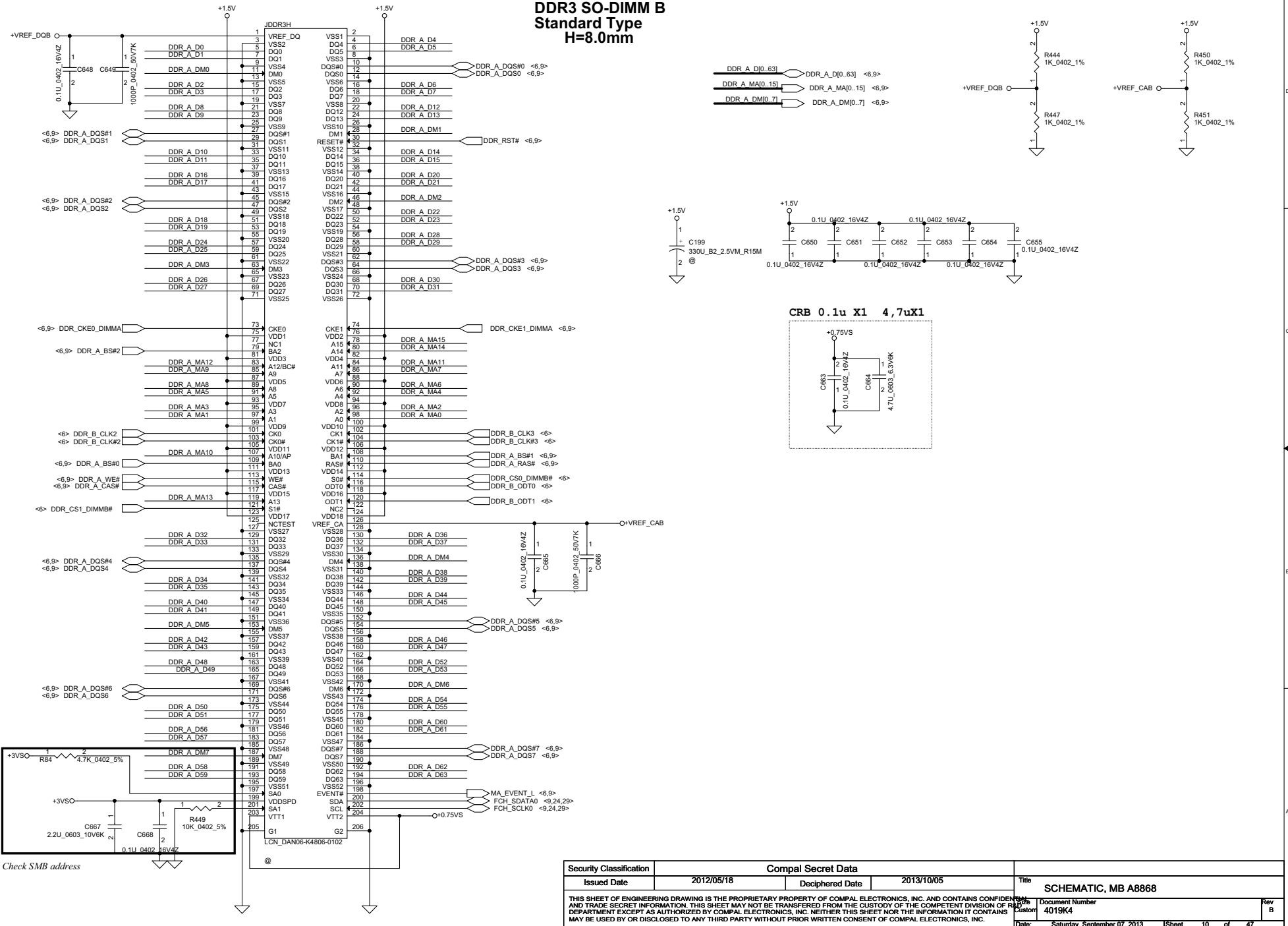
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DDR3 SO-DIMM A Standard Type H=4.0mm

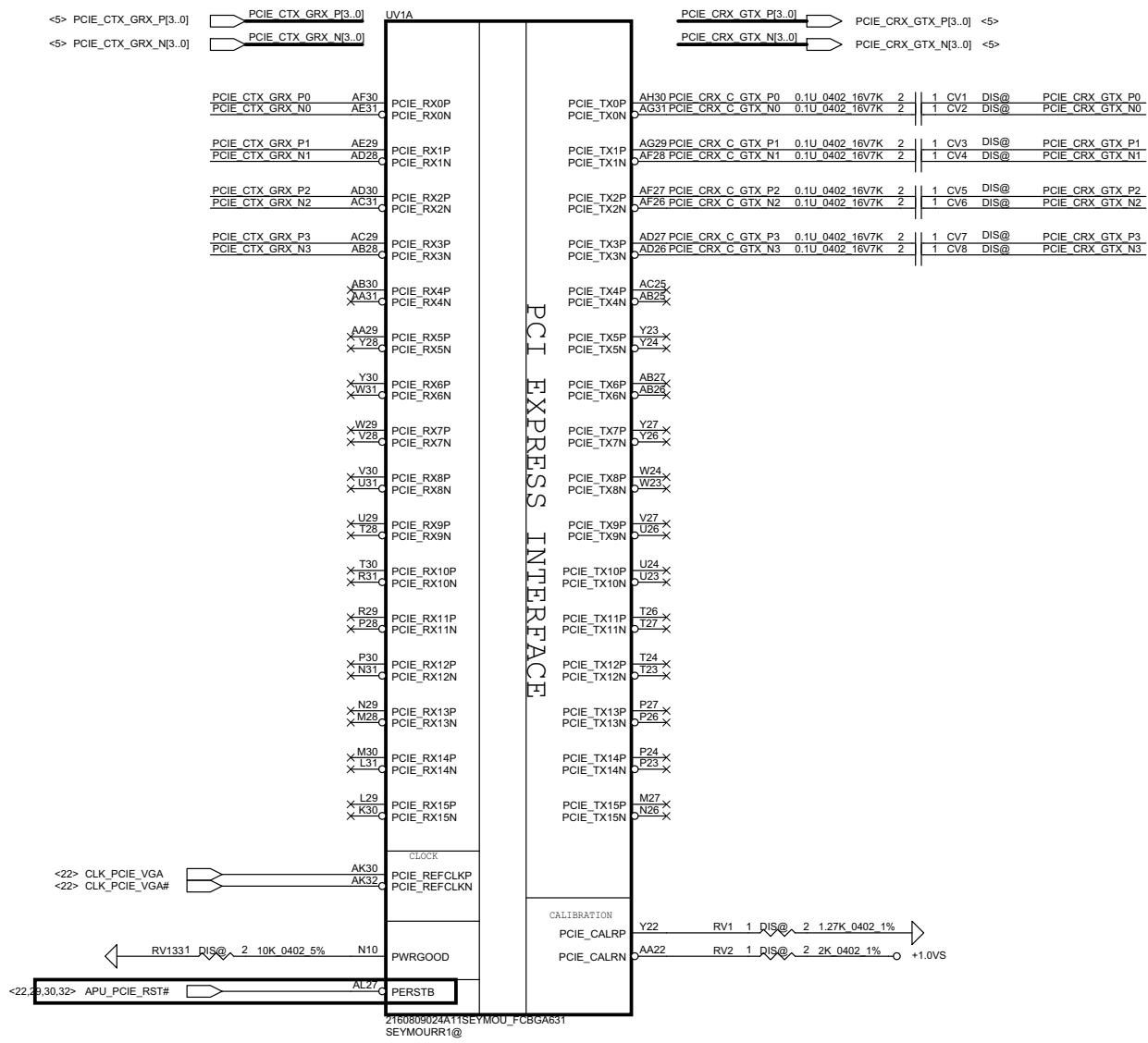


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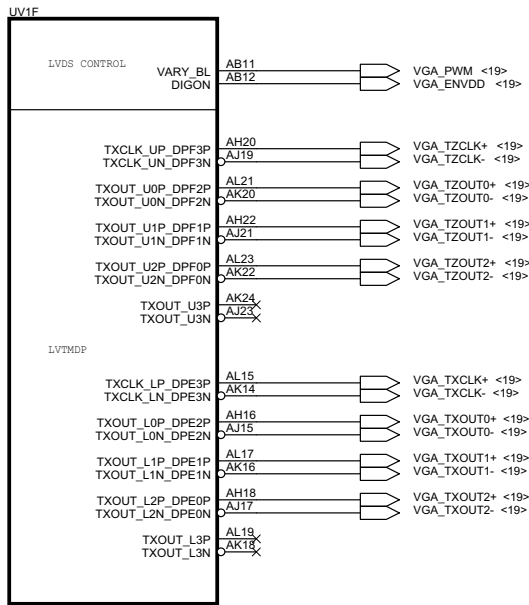
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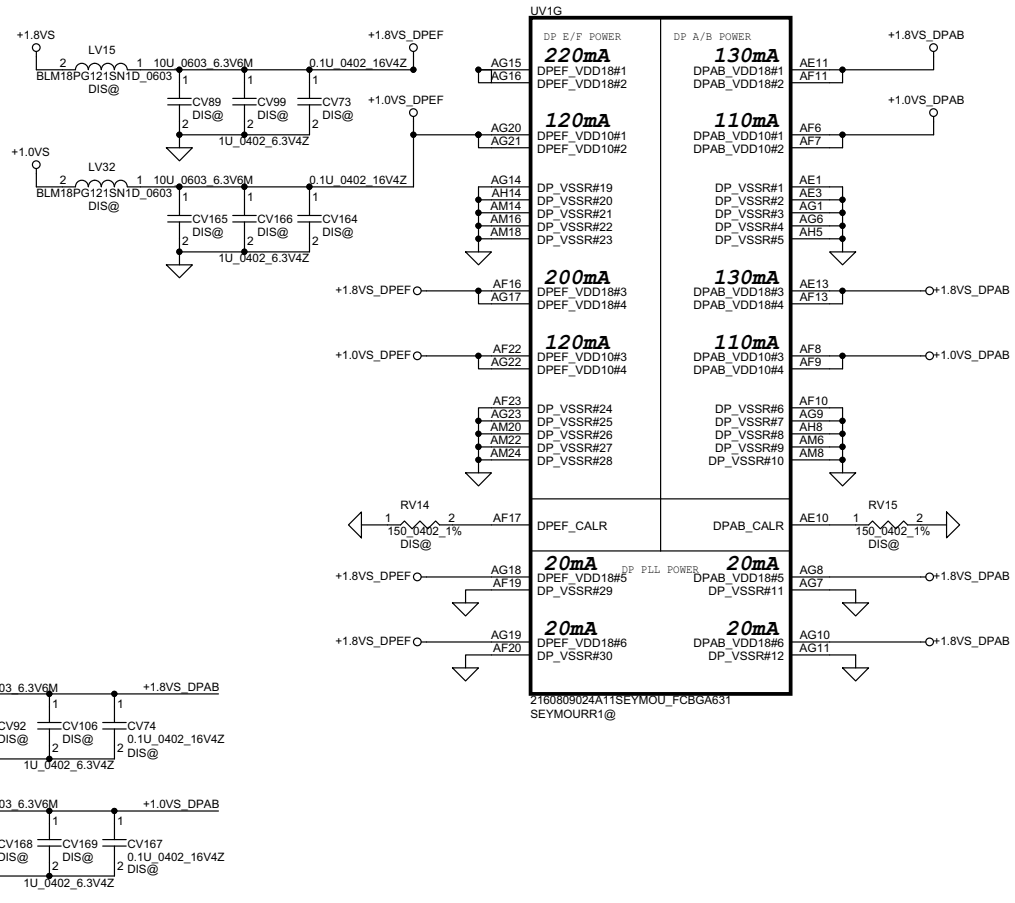
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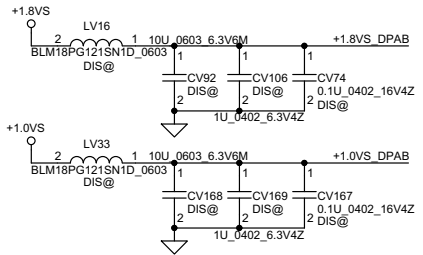
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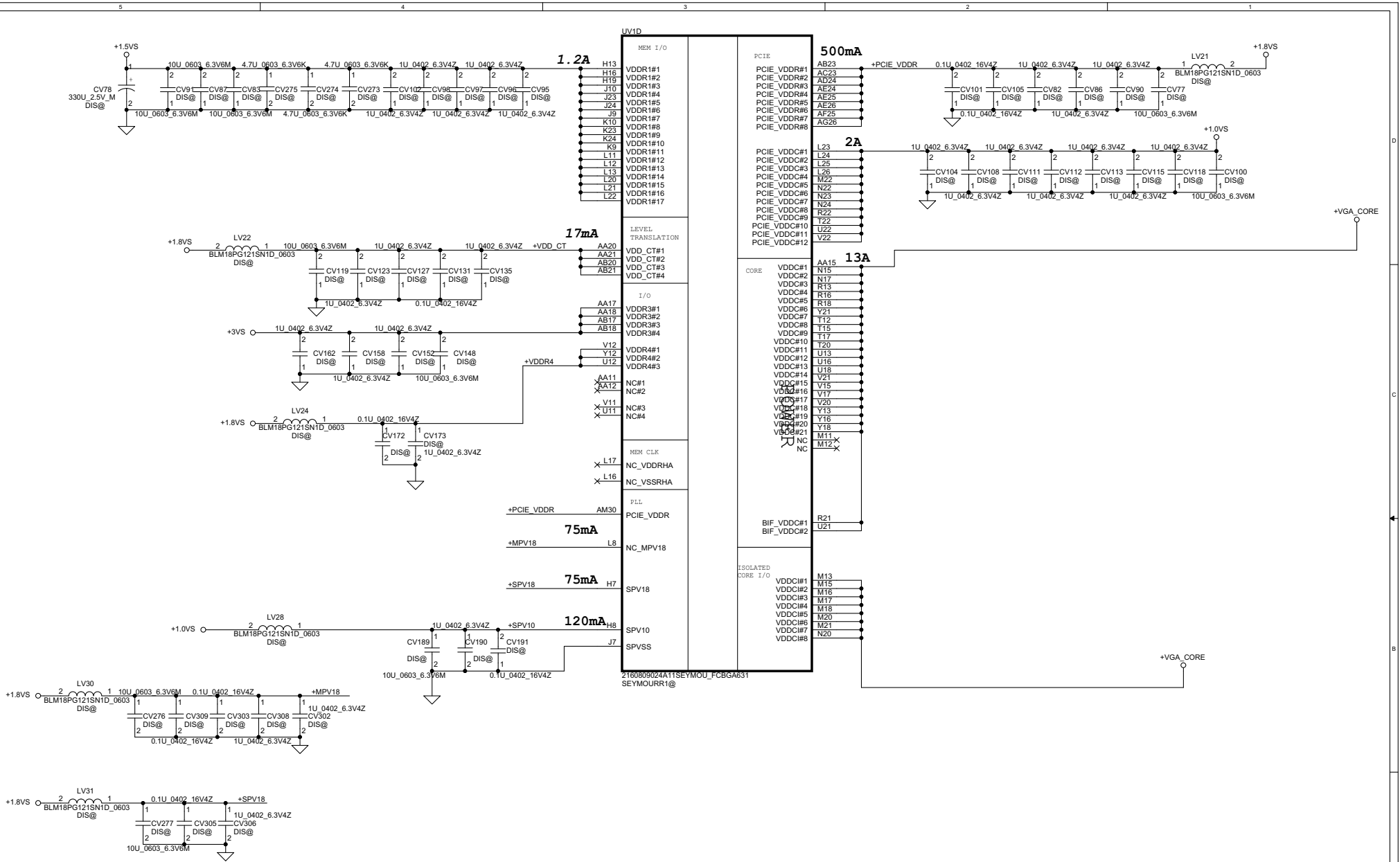
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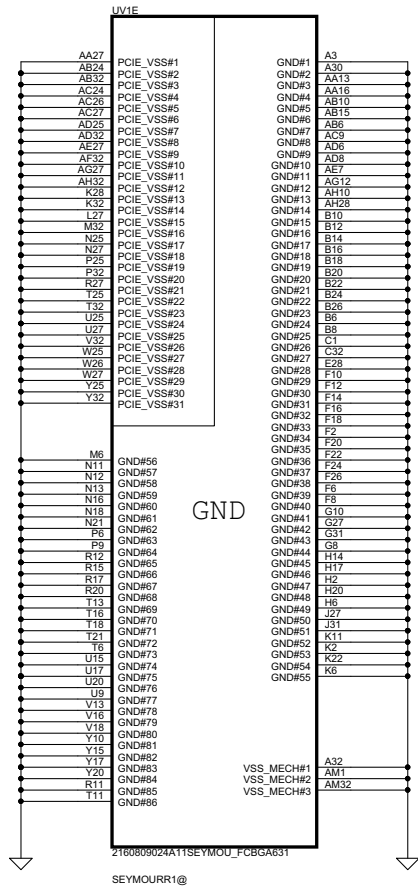
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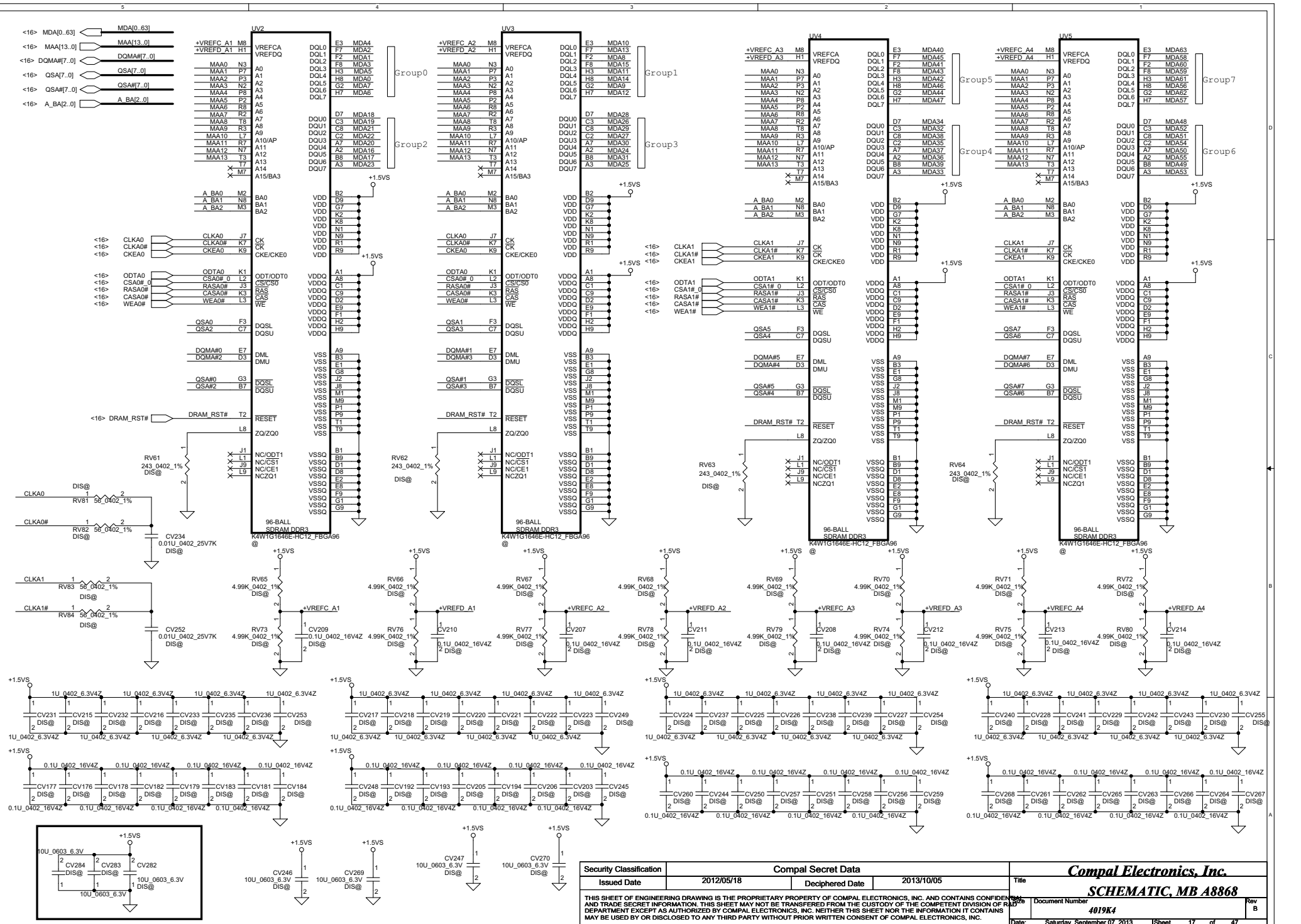
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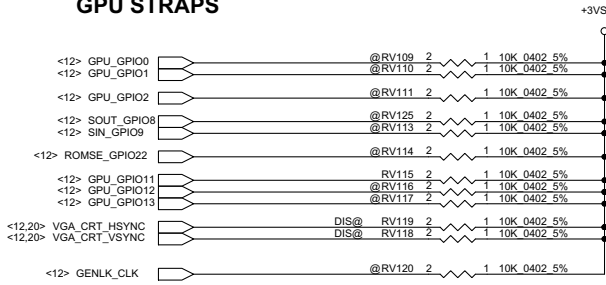


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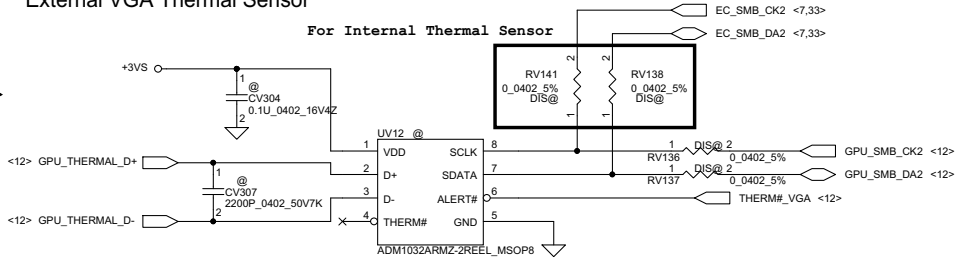
GPU STRAPS



GPU by the system BIOS		GPU by VBIOS	
GPIO22 = 0 (BIOS_ROM_EN = 0)		GPIO22 = 1 (BIOS_ROM_EN = 1)	
GPIO[13:11]	MEMORY SIZE	GPIO[13:11]	
0 0 0	128MB	1 0 0	
0 0 1	256MB	(M25P05A)	
0 1 0	64MB		

External VGA Thermal Sensor

For Internal Thermal Sensor



Need to check the VBIOS setting

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

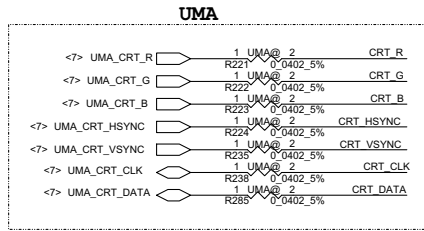
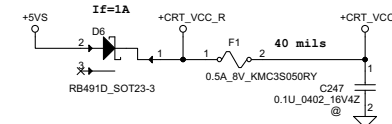
Straps Name	Pin Name	Net Name	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	GPU_GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	0
TX_DEEMPH_EN	GPIO1	GPU_GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	0
BIF_GEN2_EN_A	GPIO2	GPU_GPIO2	PCIe GNE2 ENABLED 0 = Advertises the PCIe device as 2.5 GT/s capable at power-on 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0 5.0 GT/s capability will be controlled by software
RESERVED	GPIO_8_ROMSO	SOUT_GPIO8	RESERVED	0
RESERVED	GPIO_21_BB_EN	N.C	RESERVED	0 (internal pulldown)
VGA_DIS	GPIO_9_ROMSI	SIN_GPIO9	VGA Controller 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0 (Enable)
BIOS_ROM_EN	GPIO_22_ROMCSB	ROMSE_GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
CONFIG(2:0)	GPIO[13:11]	GPU_GPIO11 GPU_GPIO12 GPU_GPIO13	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.	0 0 1 (256M)
RESERVED	GENLK_CLK	GENLK_CLK		0
AUD[1] AUD[0]	HSYNC VSYNC	VGA_CRT_HSYNC VGA_CRT_VSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	0 0

STRAPS	PIN	GPU	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 1,0
VRAM_ID[1:0]	DVDDATA (1,0)	Seymour-S3	512M 64Mx16 (x4)	SAM K4W1G1646G-BC11	SA00004GS00	1 0
			1G 128Mx16 (x4)	SAM K4W2G1646C-HC11	SA000047Q00	1 1

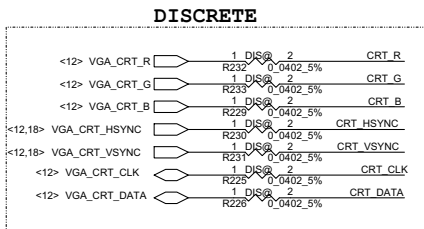
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CRT CONNECTOR

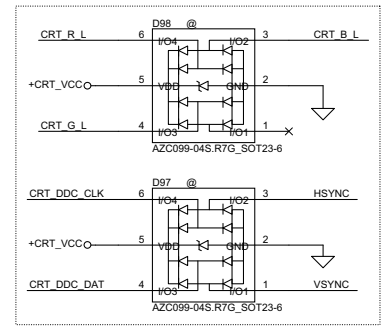
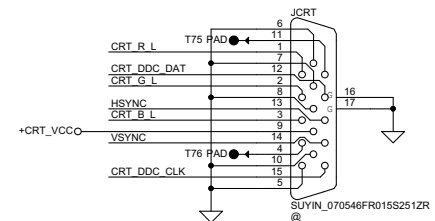
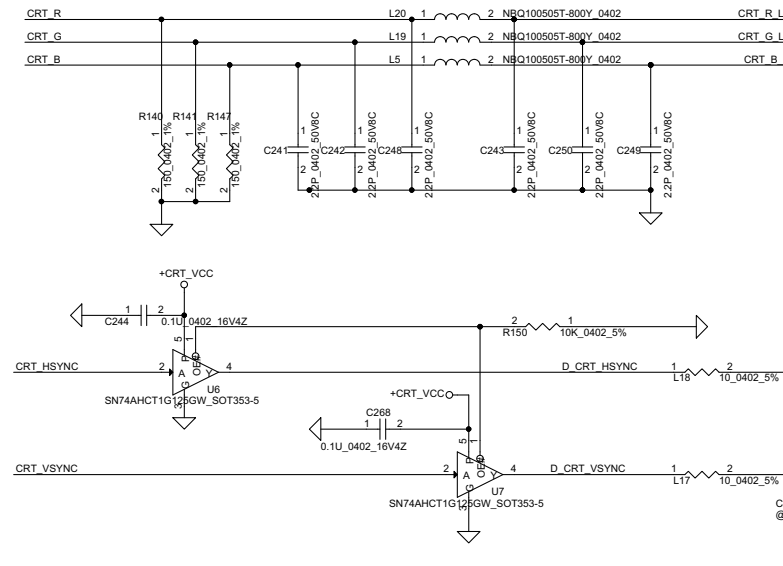
Remove D3~D5 on DVT



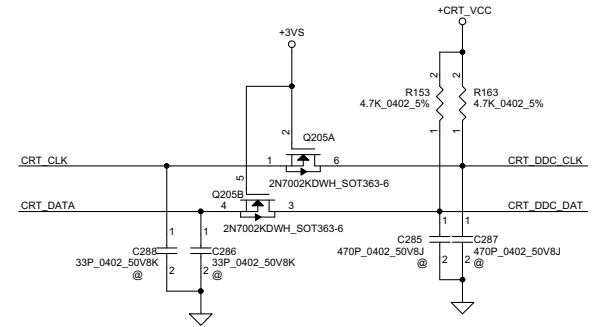
Close to CRT Connector



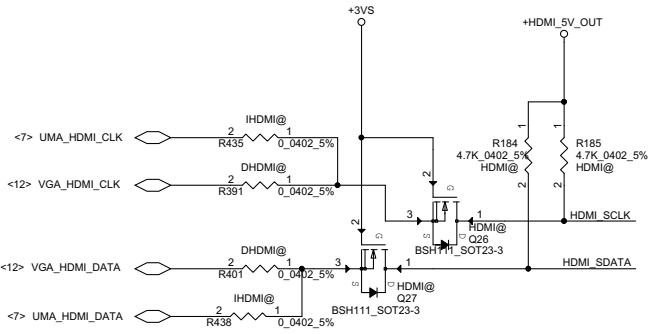
Close to CRT Connector



Reserve ESD for CRT connector on DVT



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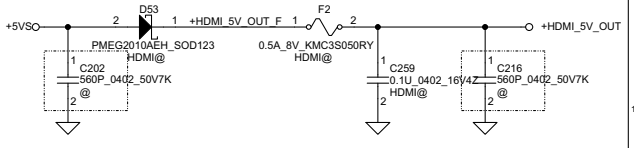
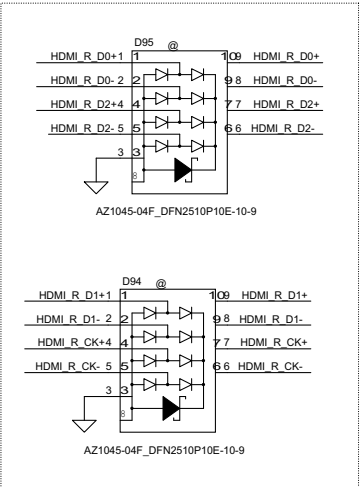
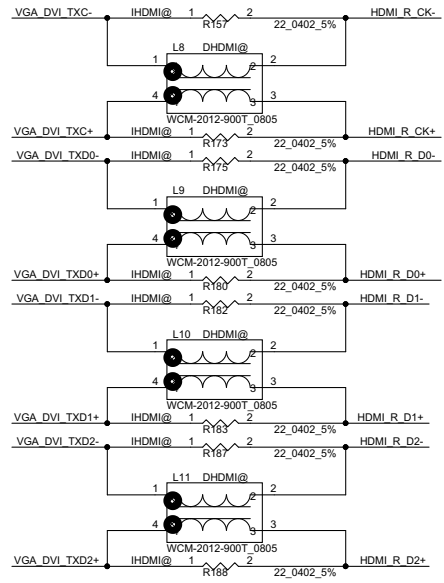
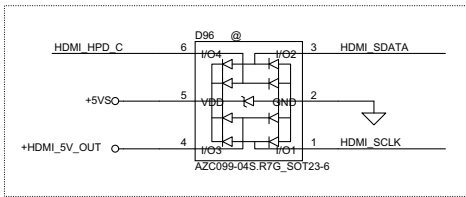


DISCRETE

<12> VGA_HDMI_CLK+	CV296	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXC+
<12> VGA_HDMI_CLK-	CV293	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXC-
<12> VGA_HDMI_TX0+	CV294	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD0+
<12> VGA_HDMI_TX0-	CV297	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD0-
<12> VGA_HDMI_TX1+	CV299	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD1+
<12> VGA_HDMI_TX1-	CV298	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD1-
<12> VGA_HDMI_TX2+	CV295	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD2+
<12> VGA_HDMI_TX2-	CV300	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD2-

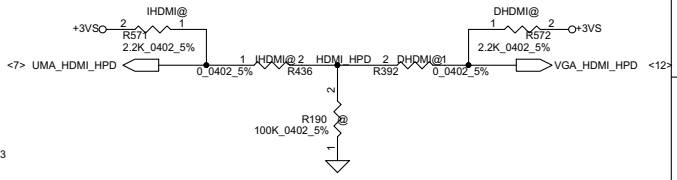
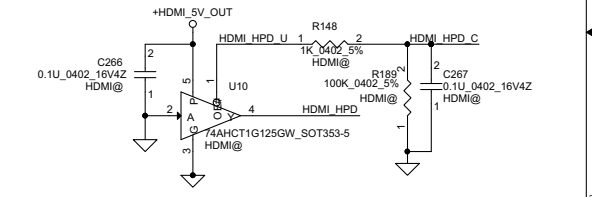
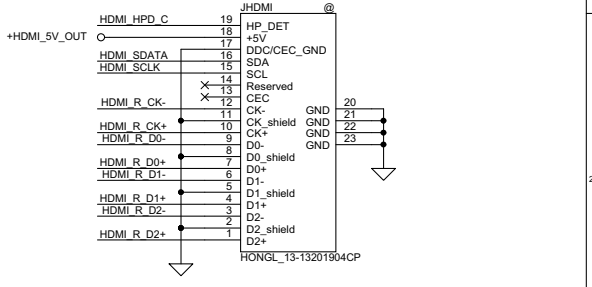
UMA

<7> UMA_HDMI_TXC+	C838	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXC+
<7> UMA_HDMI_TXC-	C837	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXC-
<7> UMA_HDMI_TX0+	C843	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXD0+
<7> UMA_HDMI_TX0-	C844	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXD0-
<7> UMA_HDMI_TX1+	C841	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXD1+
<7> UMA_HDMI_TX1-	C842	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXD1-
<7> UMA_HDMI_TX2+	C839	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXD2+
<7> UMA_HDMI_TX2-	C840	1	2	0.1U_0402_16V7K	IHDMI@	VGA_DVI_TXD2-



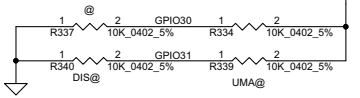
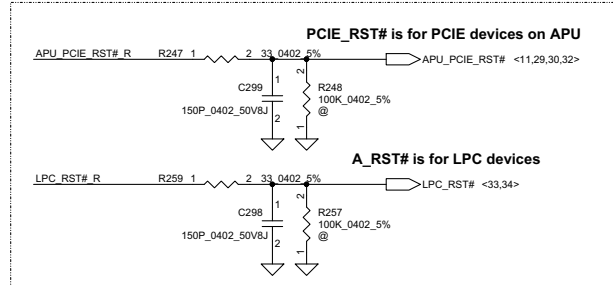
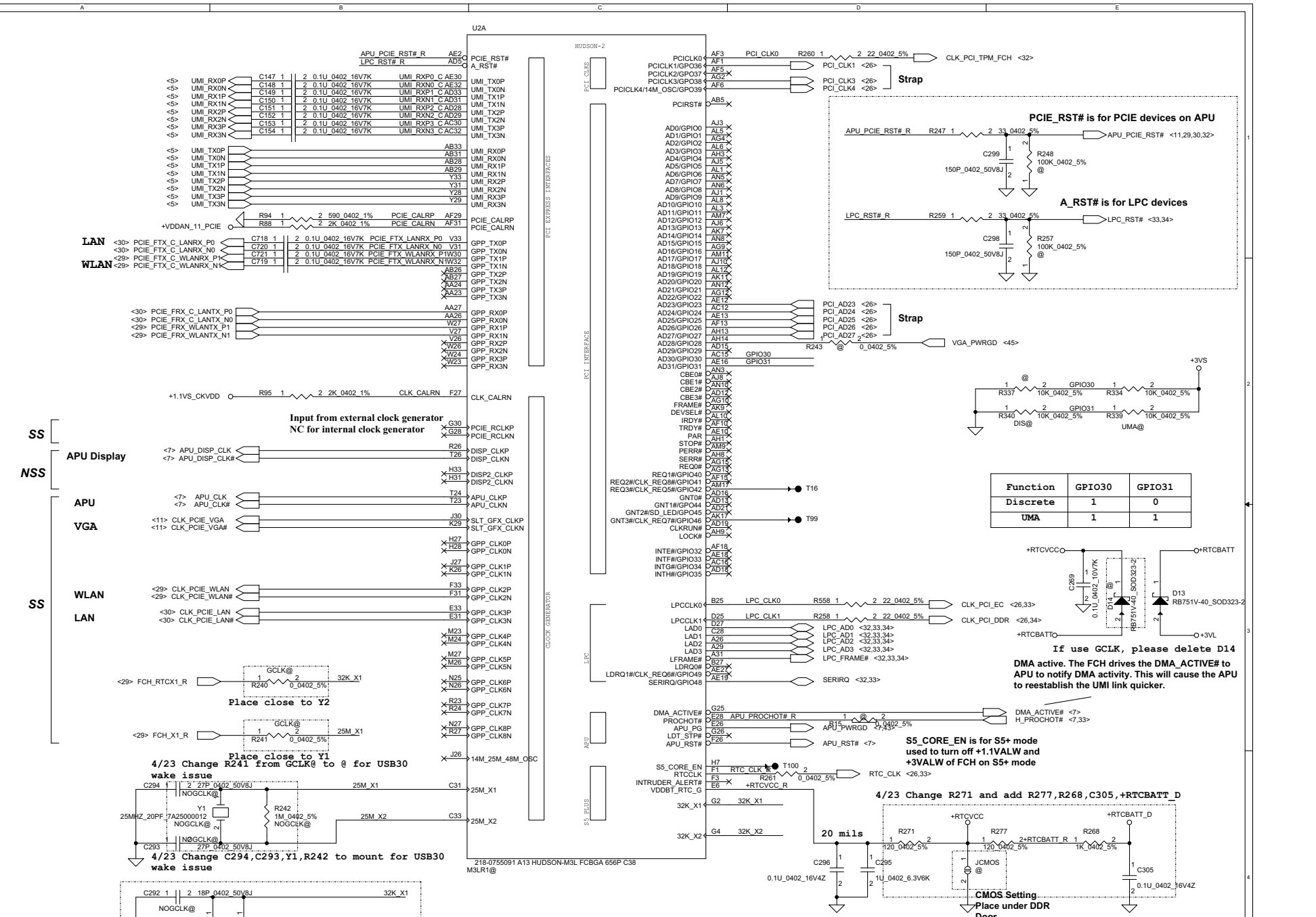
4/23 Add C202 and C216 for EMI request

HDMI Connector

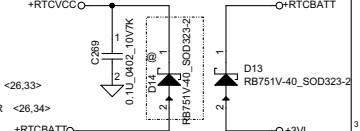


Reserve ESD for HDMI conn. on DVT

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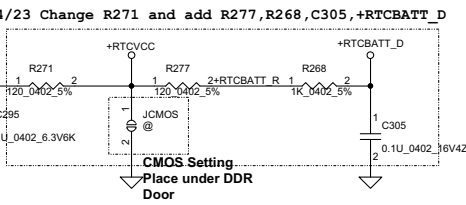


Function	GPIO30	GPIO31
Discrete	1	0
UMA	1	1



If use GCLK, please delete D14 DMA active. The FCH drives the DMA_ACTIVE# to APU to notify DMA activity. This will cause the APU to reestablish the UMI link quicker.

S5_CORE_EN is for S5+ mode used to turn off +1.1VALW and +3VALW of FCH on S5+ mode

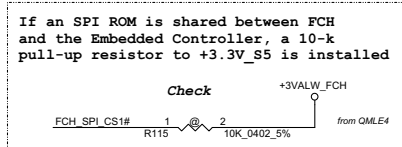


CMOS Setting Place under DDR Door

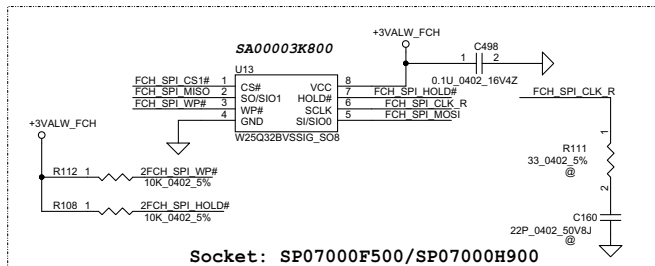
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		SCHMATIC, MB A8868
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HDMI_EN# (Internal 8.2K PU)

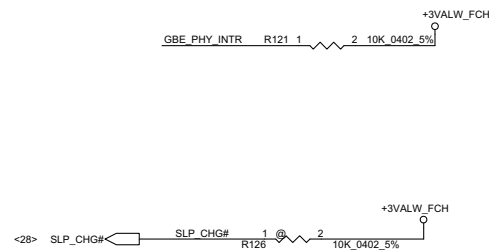
HDMI_EN#	H	L
SKU	Non-HDMI SKU	HDMI SKU



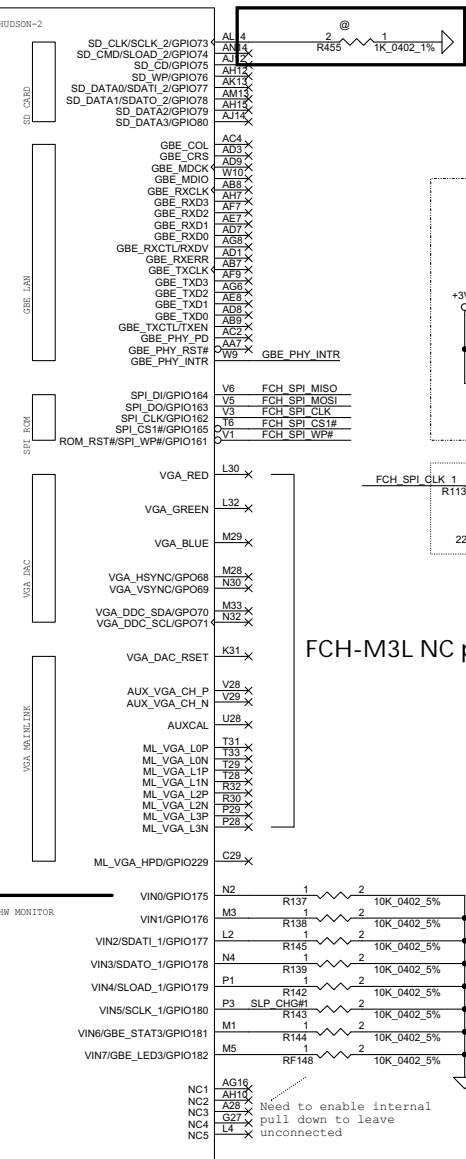
4MB SPI ROM & Non-shared ROM



5/17 Add R113 and reserve C161 for EMI request



FCH-M3L NC pin



218-0755091 A13 HUDSON-M3L FC8GA 656P C38

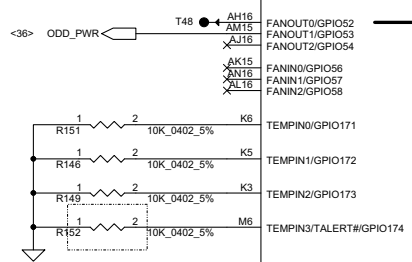
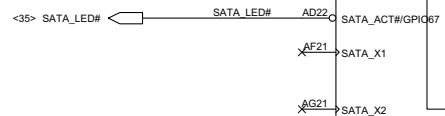
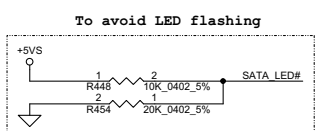
M3LR1@

12/22 Follow the last Compal CRB board

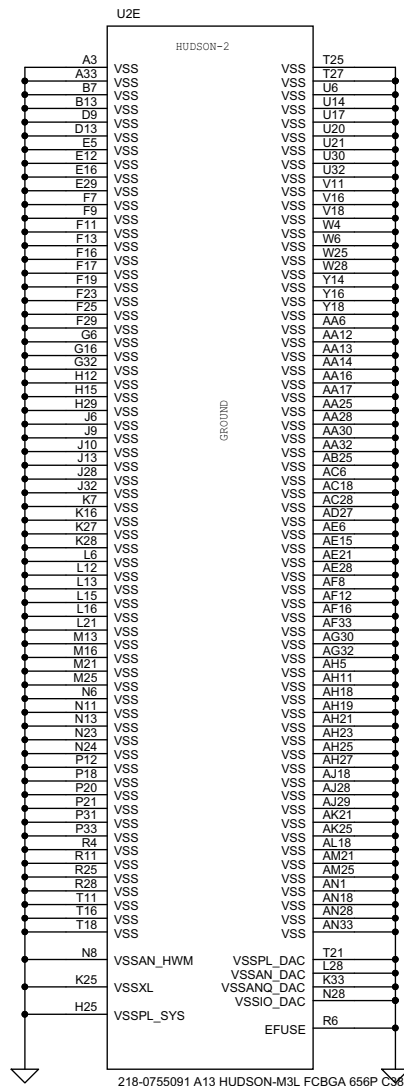
HDD
 <27> SATA_FRX_C_DTX_N0
 <27> SATA_FRX_C_DTX_P0
 <27> SATA_FRX_C_DTX_N1
 <27> SATA_FRX_C_DTX_P1

ODD
 <27> SATA_FRX_C_DTX_N1
 <27> SATA_FRX_C_DTX_P1

FCH-M3L NC pin

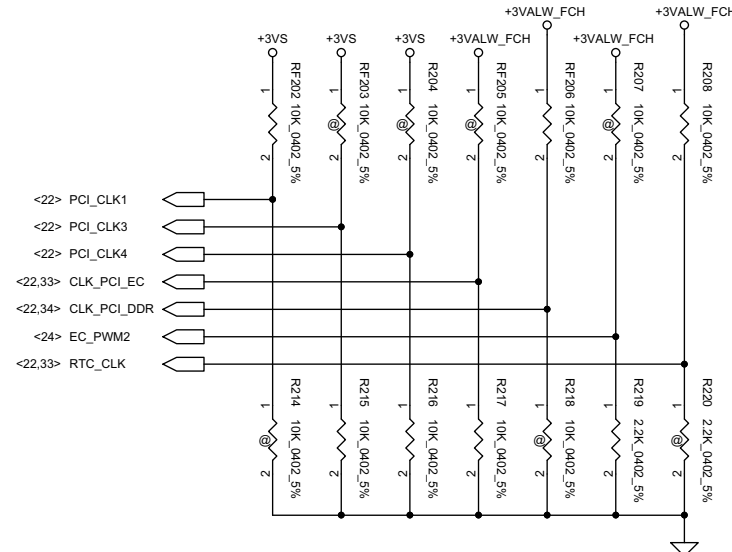


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STRAP PINS

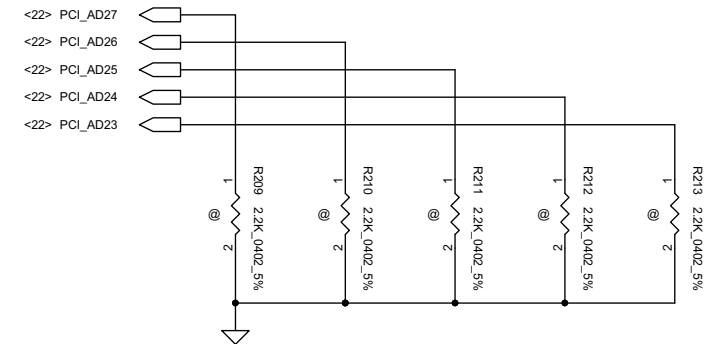
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCI E GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCI E GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



DEBUG STRAPS

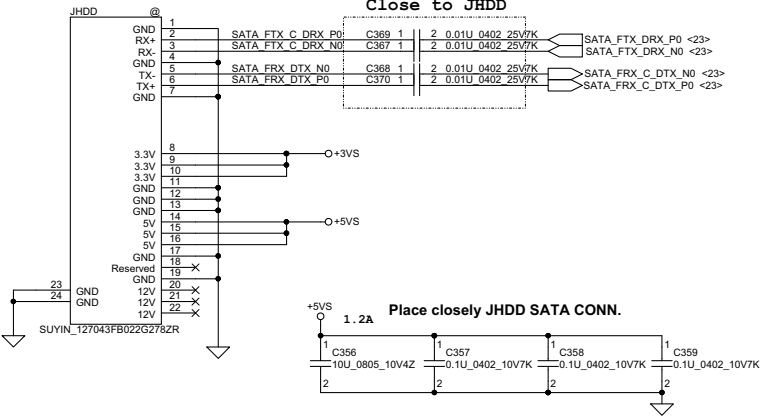
FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCI E STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCI E STRAPS	ENABLE PCI MEM BOOT

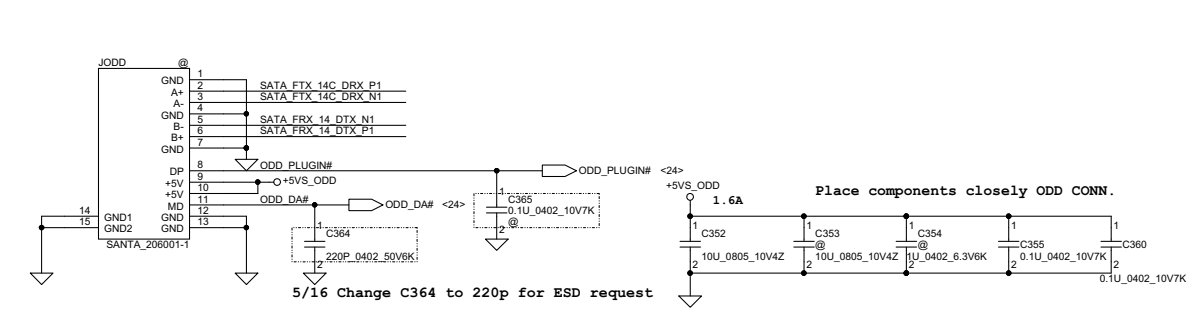


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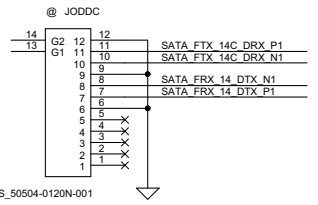
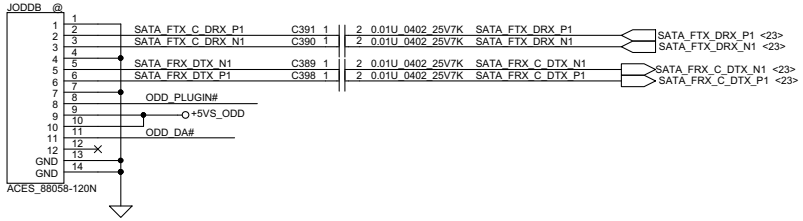
SATA HDD Conn.



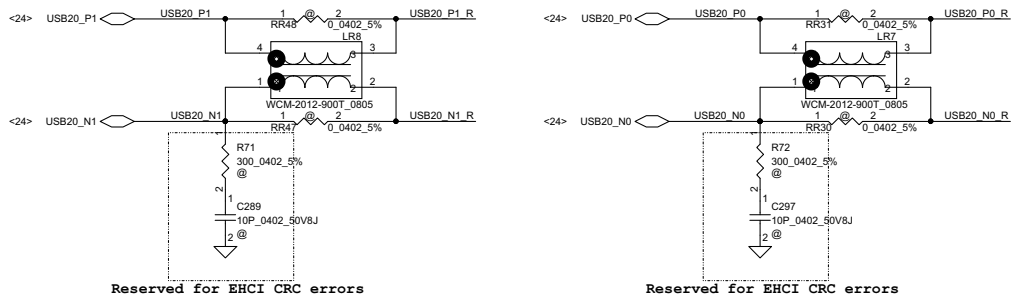
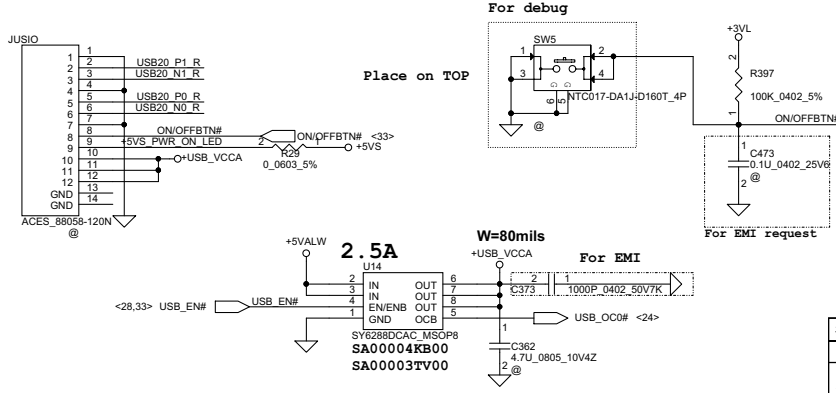
SATA ODD Conn (for 14")



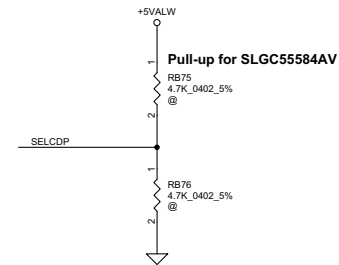
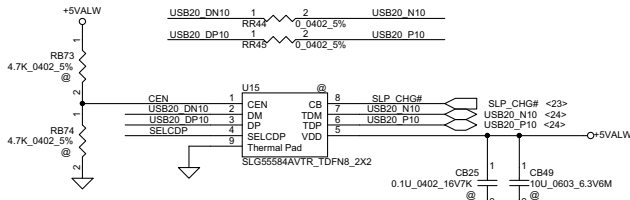
SATA ODD Conn (for 15")



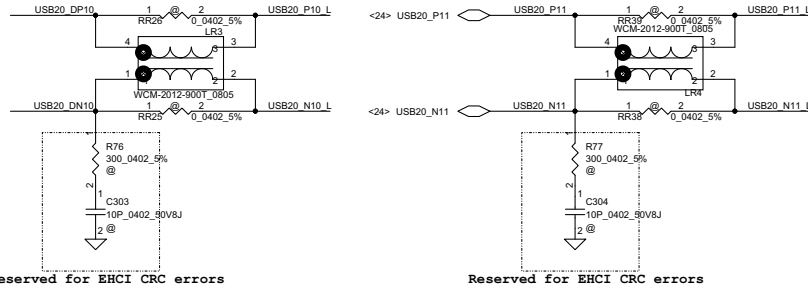
Power Button & RUSB connector



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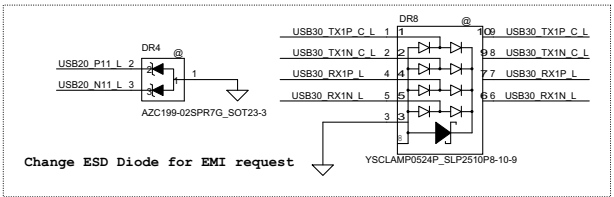
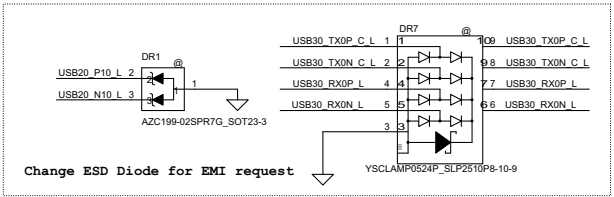
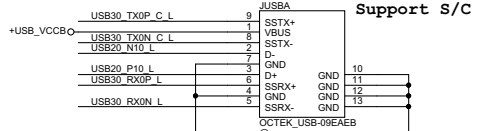
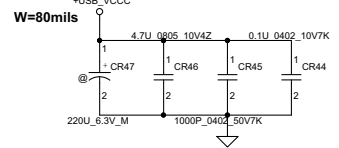
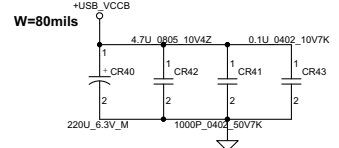
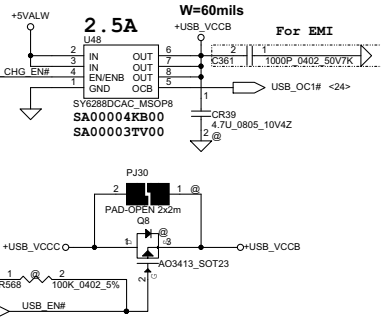
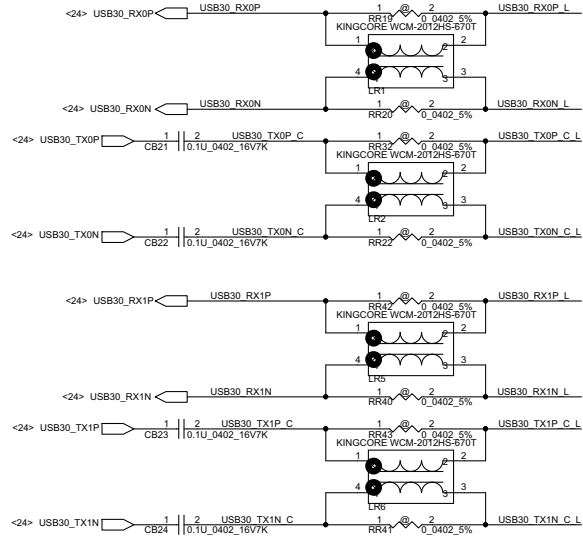


SLP_CHG#	SELCDP	Function
0	X	DCP autotdetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only



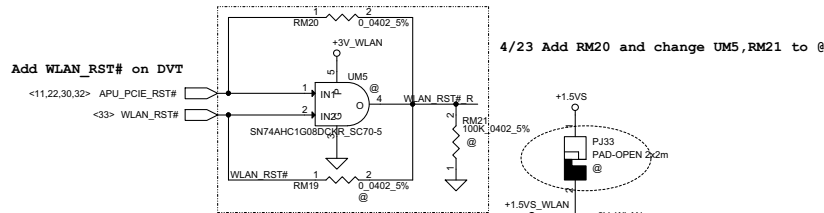
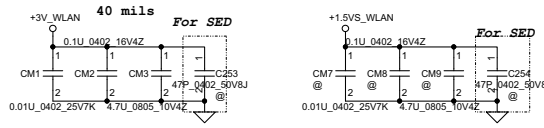
Reserved for EHCI CRC errors

Reserved for EHCI CRC errors



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Slot 1 Half PCIe Mini Card-WLAN

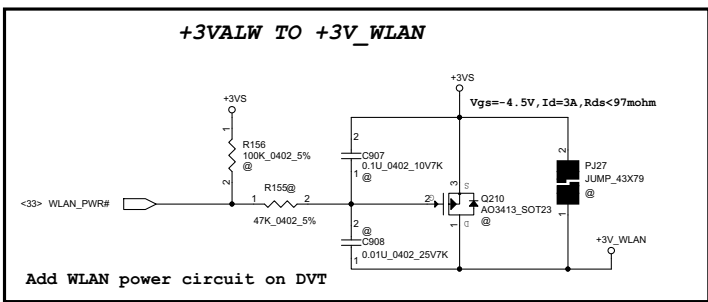
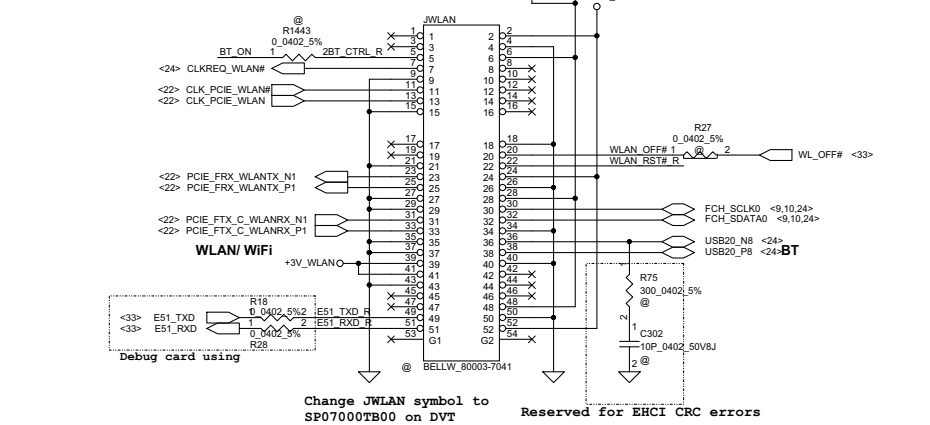


WLAN&BT Combo module circuits

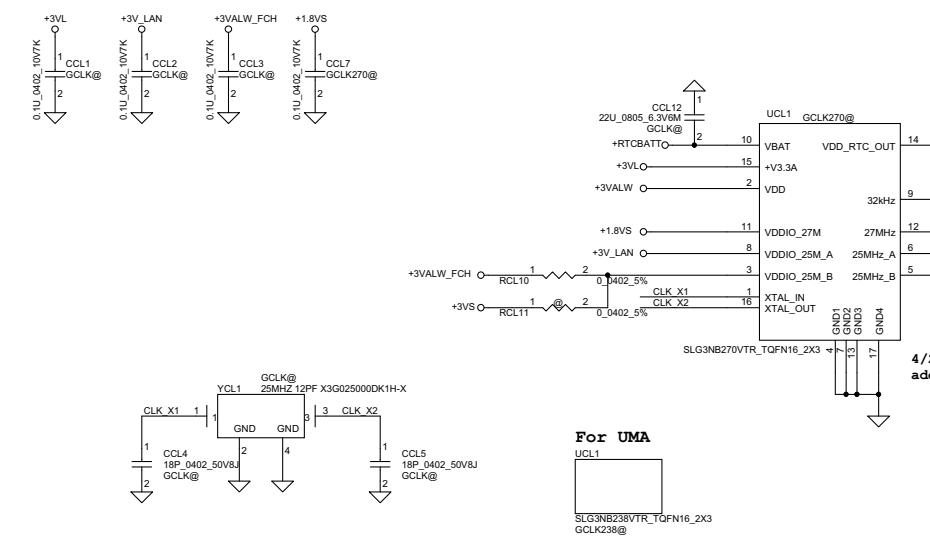
	BT on module Enable	BT on module Disable
BT_ON	H	L

<33> BT_ON 1 R328 2 E51_RXD_R
TK_0402_5%

For isolate BT_CTRL and Compal Debug Card.



Green Clock Generator

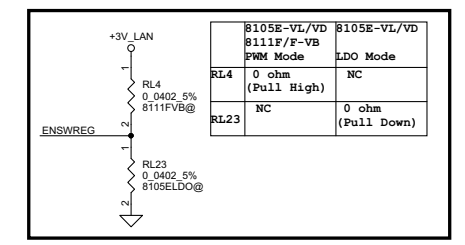
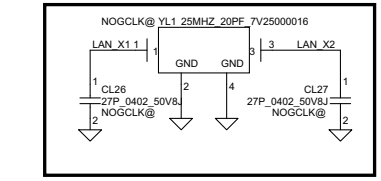
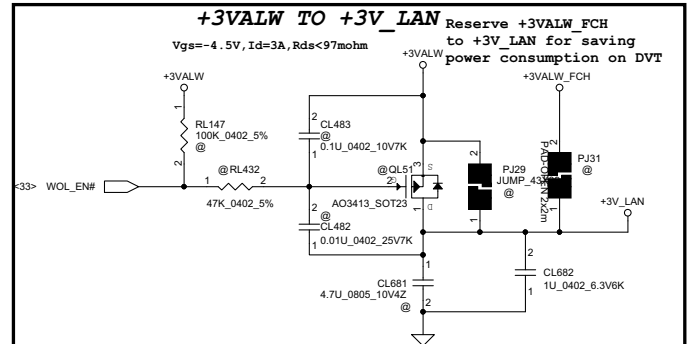
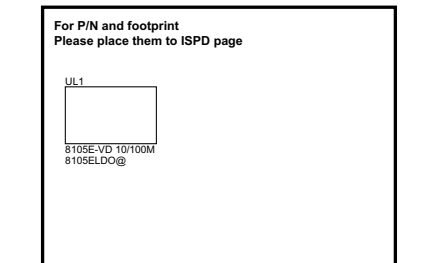
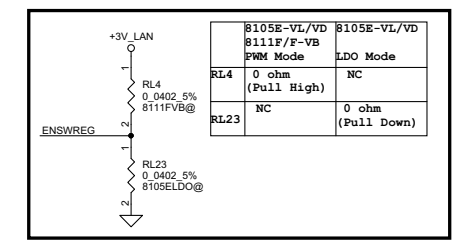
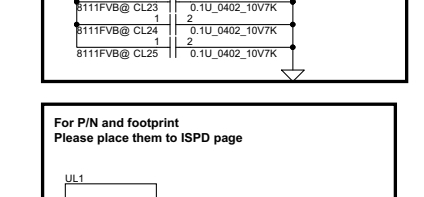
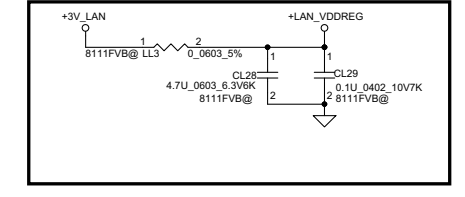
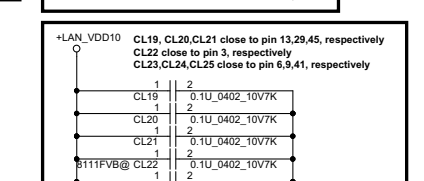
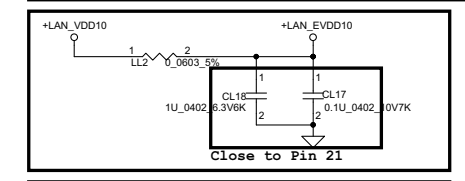
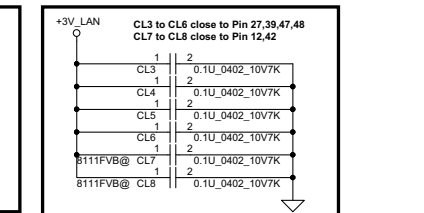
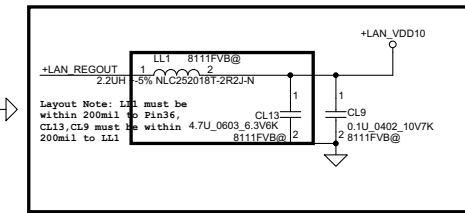
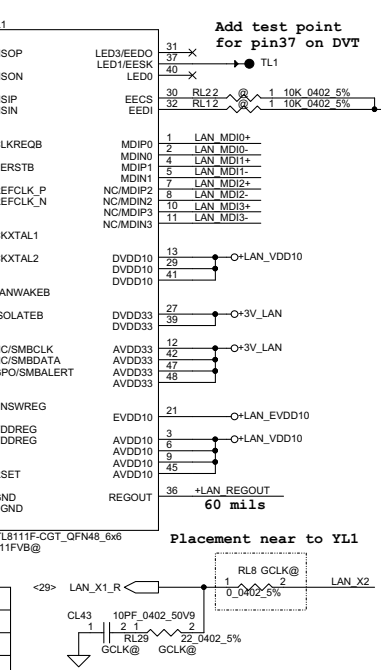
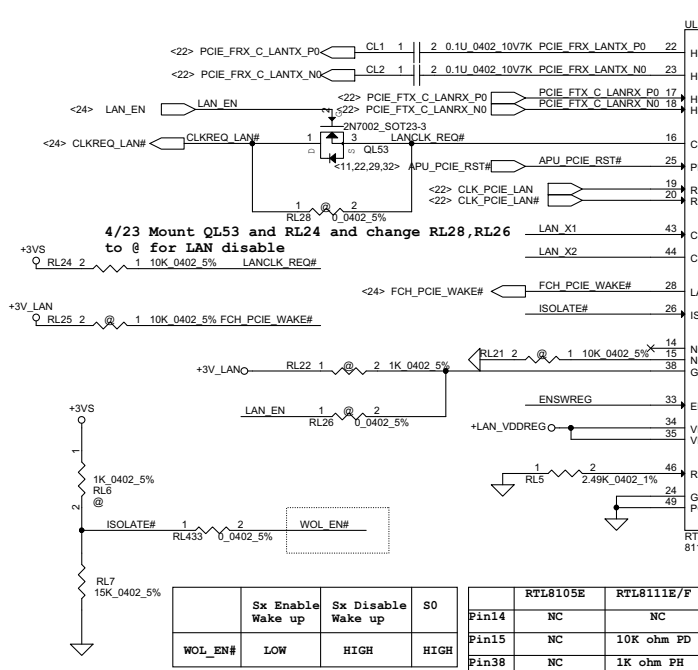


4/23 Change UCL1.2 to +3VALW, UCL1.14 to +RTVCVCC_D and add RCL10, RCL11 for USB30 wake issue

LAN X1 R R 1 @ 2 0.0402_5%
RCL5

Reserved for Swing Level adjustment (Close GCLK side)

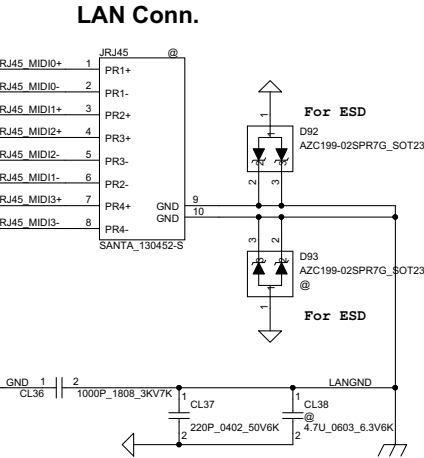
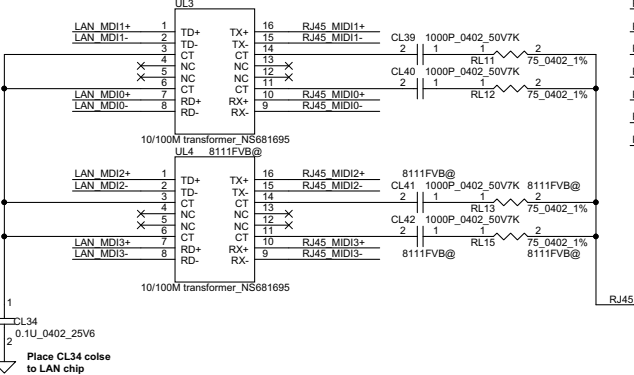
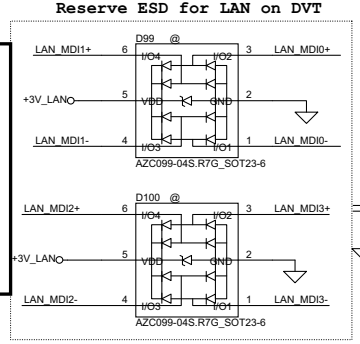
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+3V_LAN rising time (10%~90%) need > 1ms and < 100ms.

LAN	WOL	LAN_EN		ISOLATEB	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

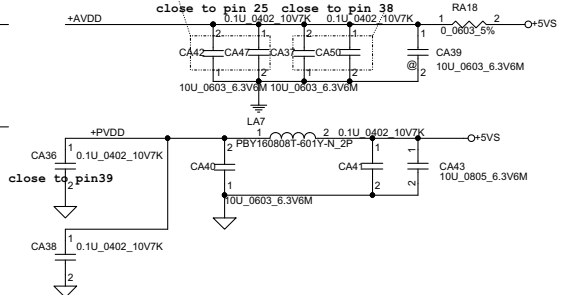
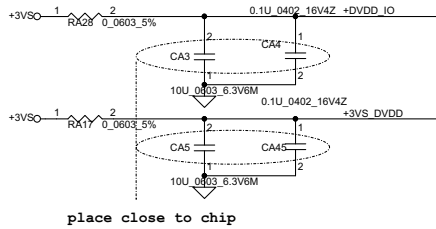
* S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms



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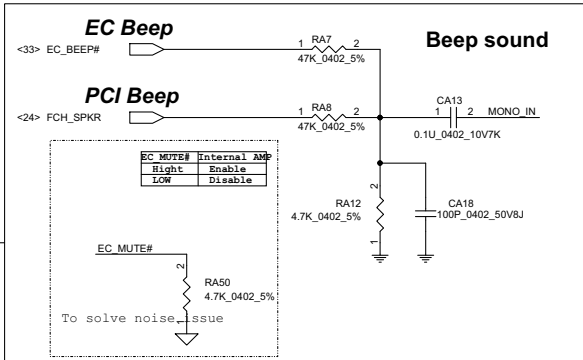
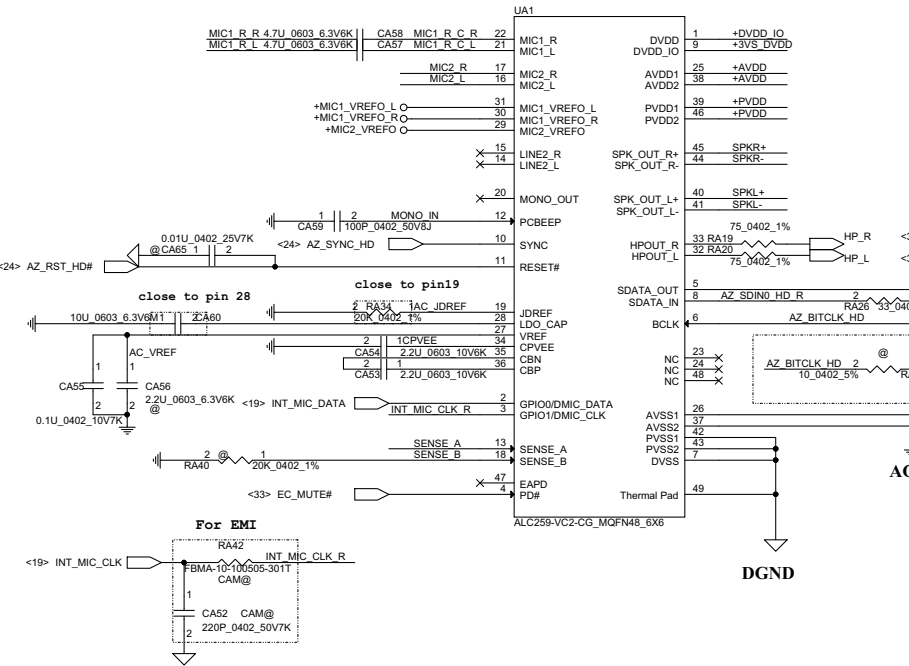
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35mA for 3.3V level

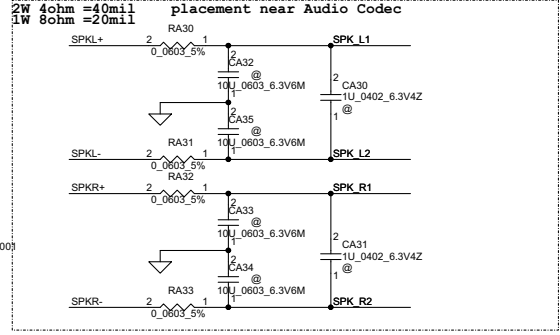
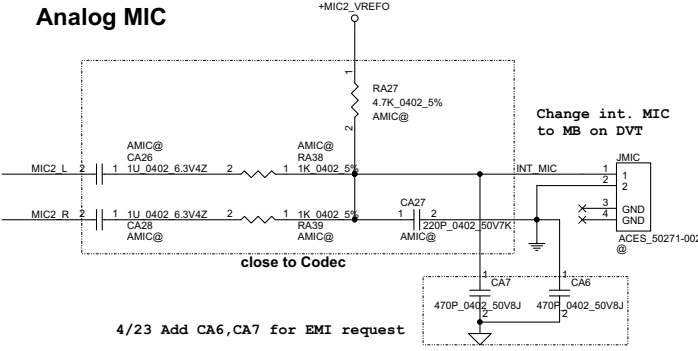


place close to chip

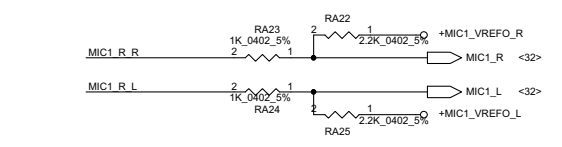
For EMI please place near codec



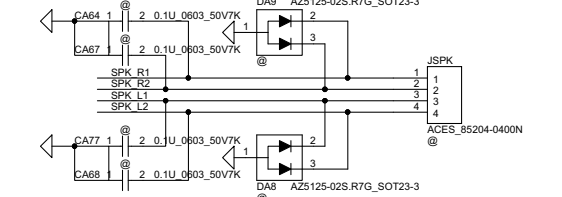
Analog MIC



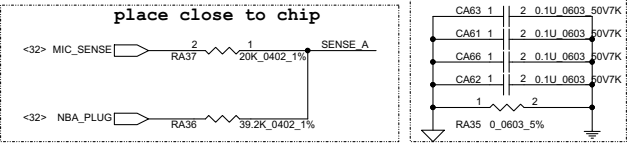
Ext. MIC/LINE IN JACK



SPK Conn. 4/23 Add CA64, CA67, CA68, CA77 for EMI request

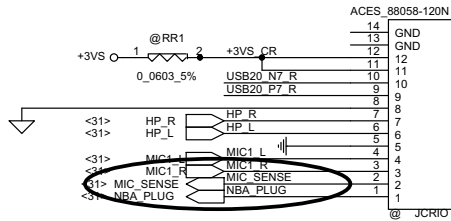


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Analog MIC
	10K	PORT-H (PIN 20)	

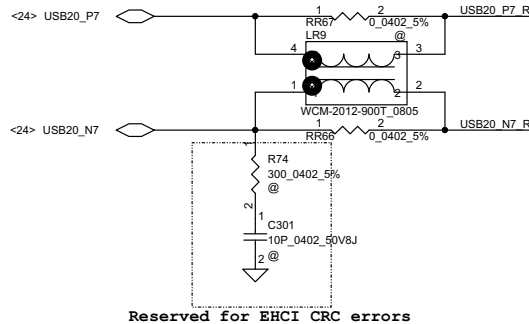


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CardReader Conn.

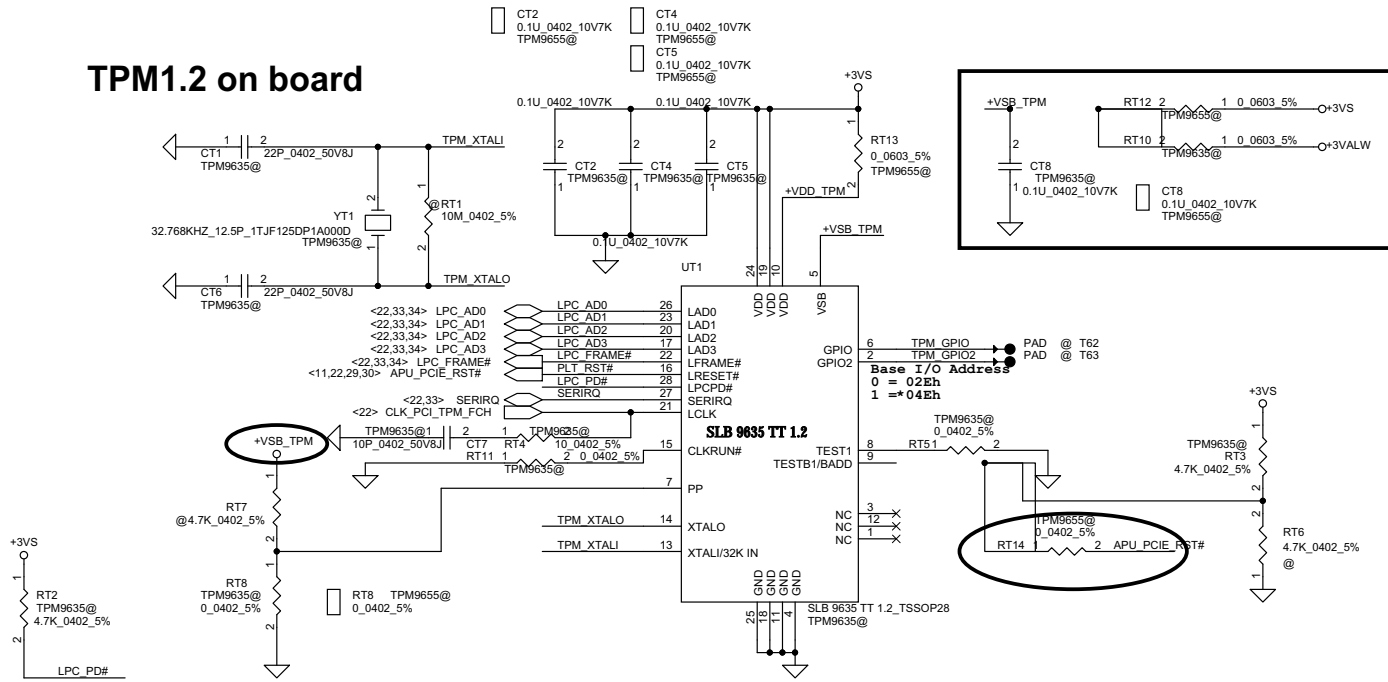


Update JCRI0 pin definition on DVT

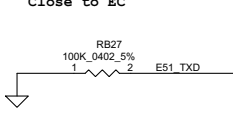
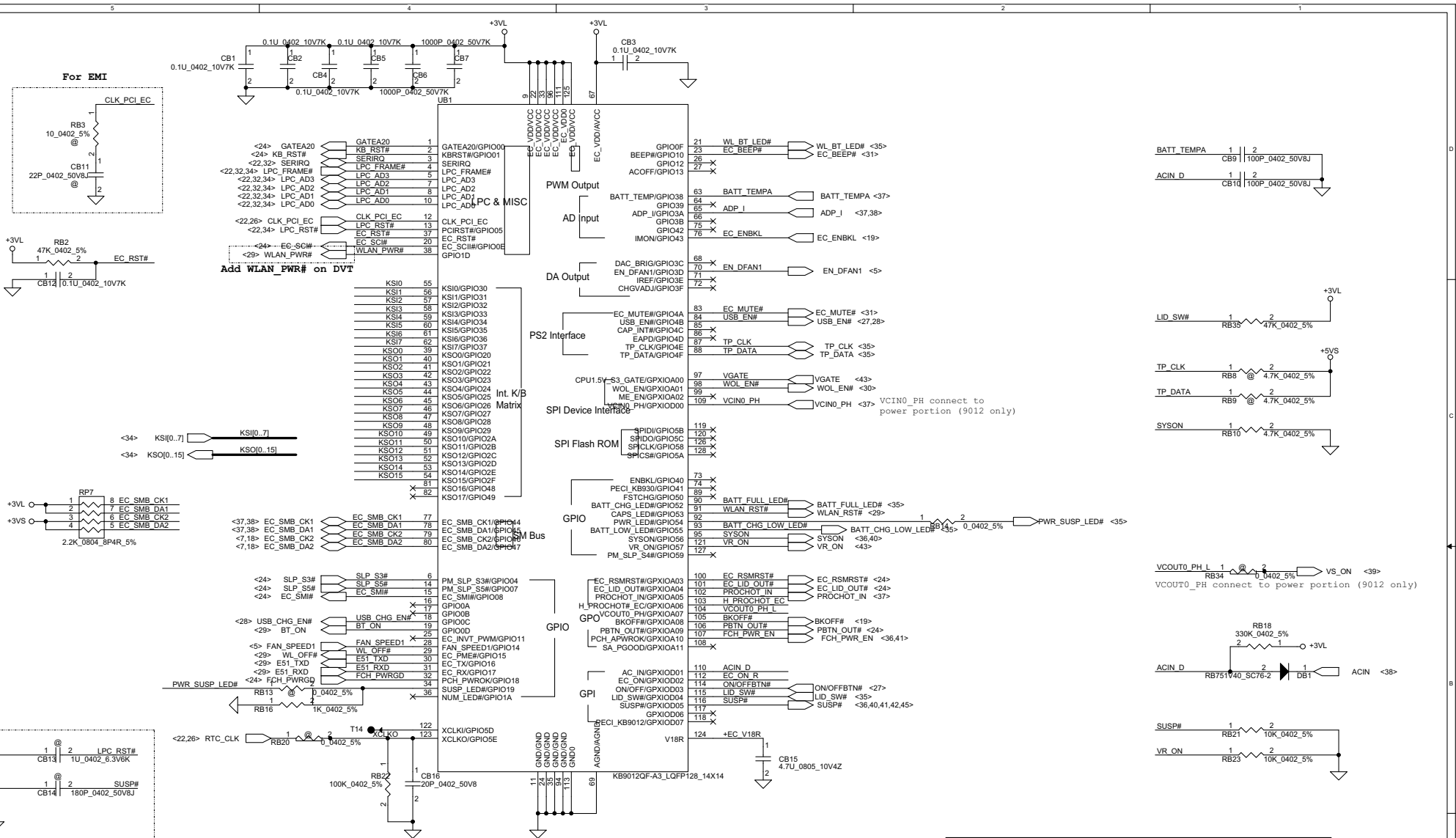


Reserved for EHCI CRC errors

TPM1.2 on board

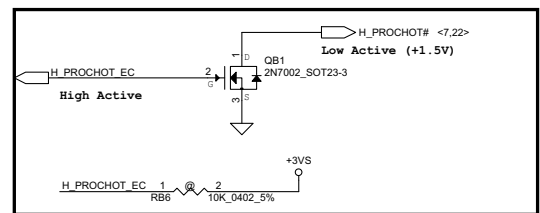
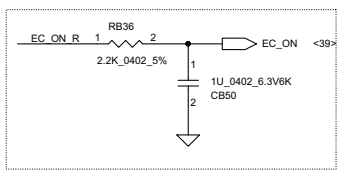


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Voltage Comparator Pins FOR 9012 A3

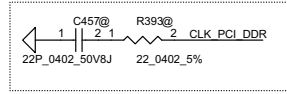
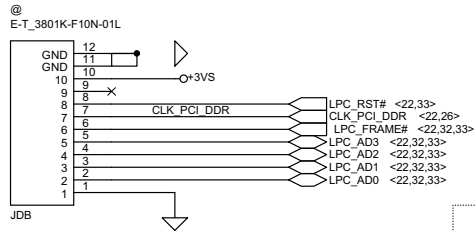
VCIN0 pin109	>1.2V	<1.2V
VCIN1 pin102		
VCOUT0 pin104	HIGH	LOW
VCOUT1 pin103	LOW	HIGH



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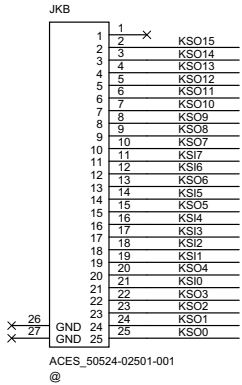
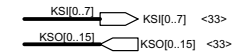
LPC Debug Port

Place the PAD under DDR DIMM.



For EMI

KEYBOARD CONN.



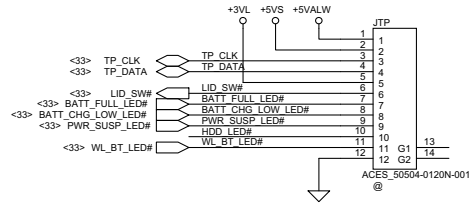
For EMI

Close to JKB

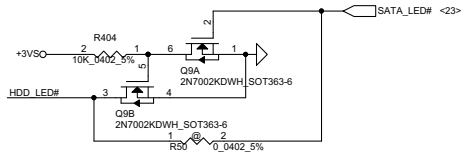
Signal	Pin 1	Pin 2	Component
KSO2	1	2	100P_0402_50V8J
KSO1	1	2	100P_0402_50V8J
KSO0	1	2	100P_0402_50V8J
KSO4	1	2	100P_0402_50V8J
KSO3	1	2	100P_0402_50V8J
KSO5	1	2	100P_0402_50V8J
KSO14	1	2	100P_0402_50V8J
KSO6	1	2	100P_0402_50V8J
KSO7	1	2	100P_0402_50V8J
KSO13	1	2	100P_0402_50V8J
KSO8	1	2	100P_0402_50V8J
KSO9	1	2	100P_0402_50V8J
KSO10	1	2	100P_0402_50V8J
KSO11	1	2	100P_0402_50V8J
KSO12	1	2	100P_0402_50V8J
KSO15	1	2	100P_0402_50V8J
KSI7	1	2	100P_0402_50V8J
KSI2	1	2	100P_0402_50V8J
KSI3	1	2	100P_0402_50V8J
KSI4	1	2	100P_0402_50V8J
KSI0	1	2	100P_0402_50V8J
KSI5	1	2	100P_0402_50V8J
KSI6	1	2	100P_0402_50V8J
KSI1	1	2	100P_0402_50V8J
KSI11	1	2	100P_0402_50V8J
	1	2	100P_0402_50V8J

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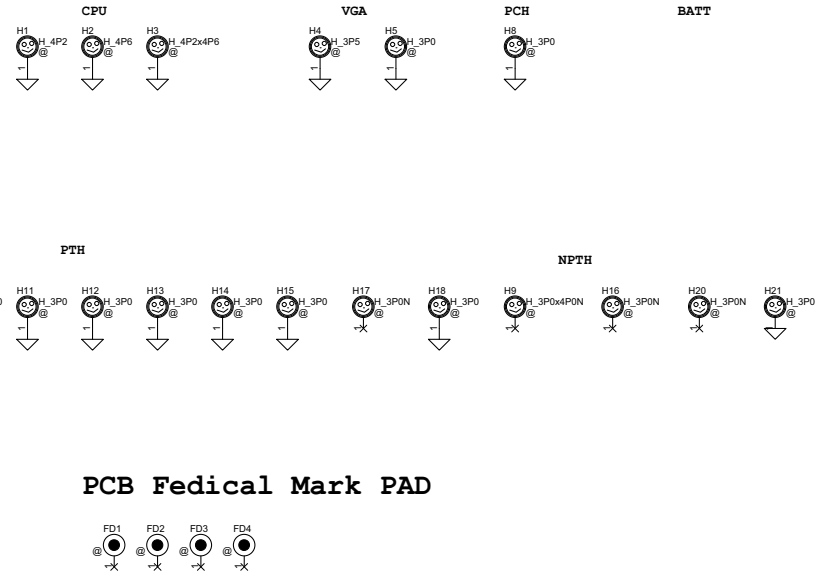
Touchpad Connector (Reserve 7 pins for LED & Win8 TP)



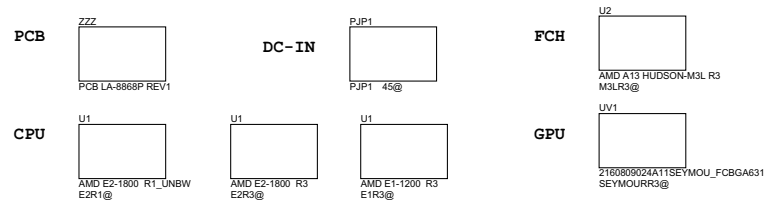
HDD LED



Screw Hole

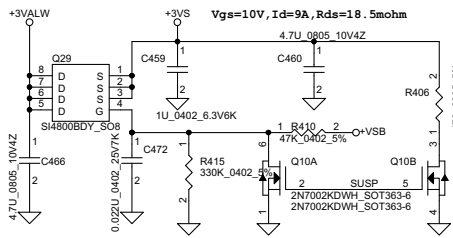


ISPD

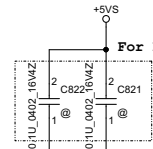
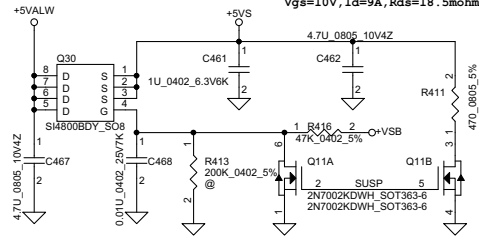


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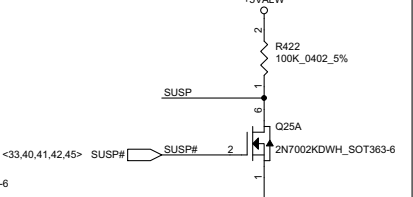
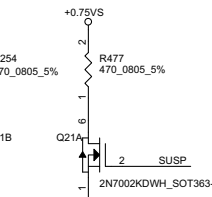
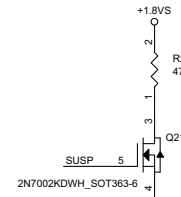
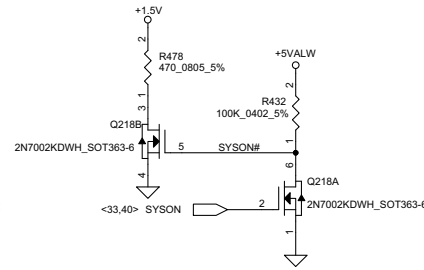
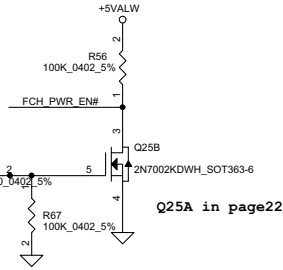
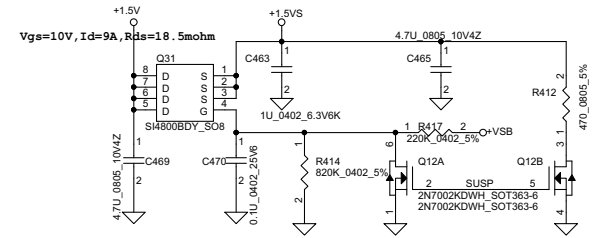
+3VALW TO +3VS



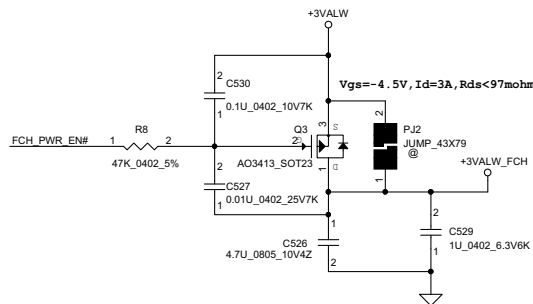
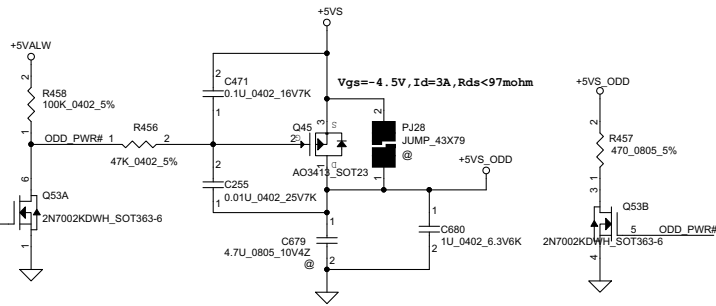
+5VALW TO +5VS



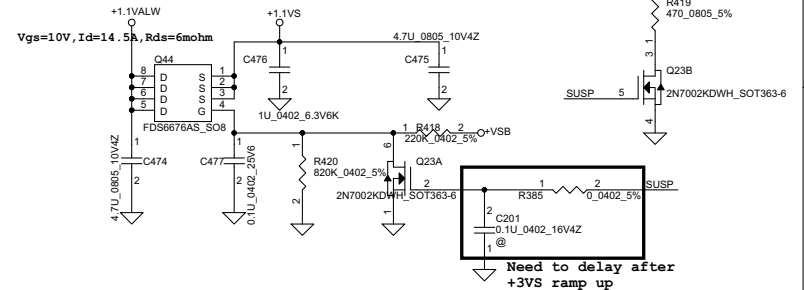
+1.5V to +1.5VS



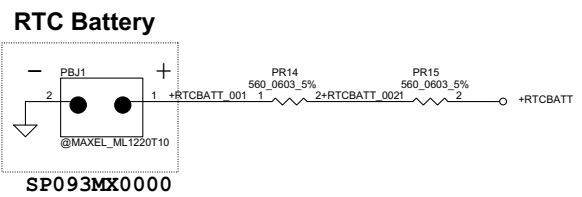
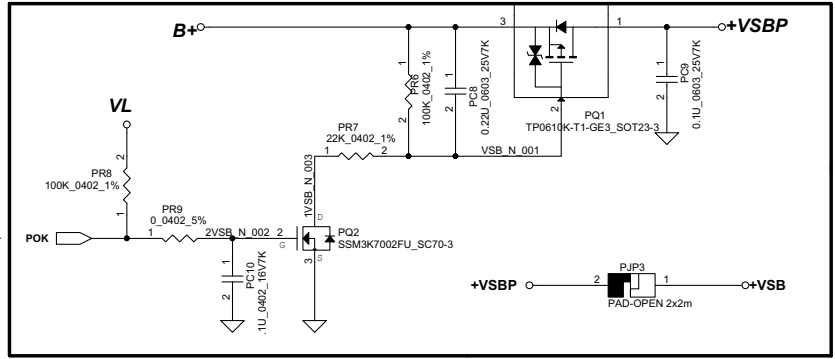
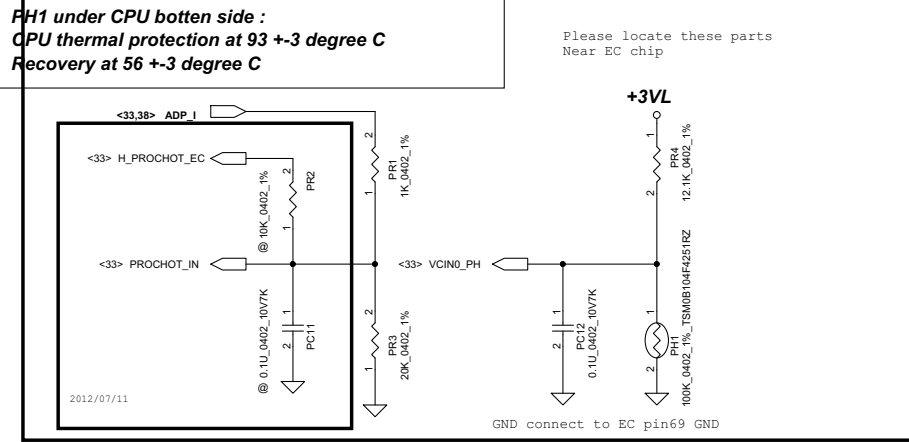
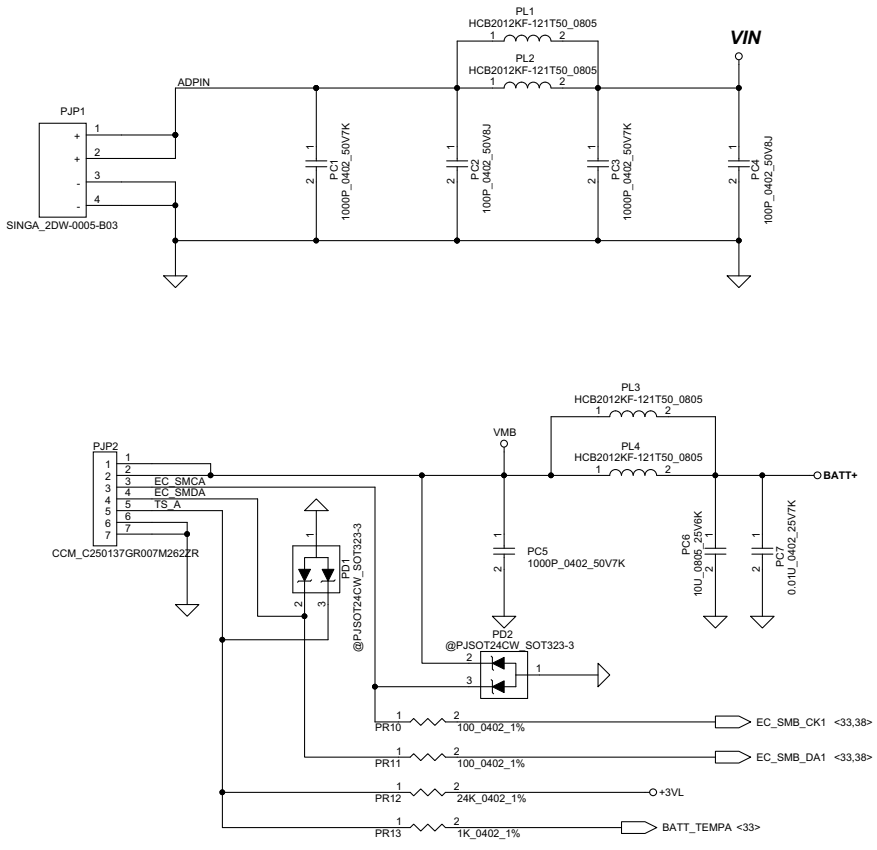
+5VS TO +5VS_ODD



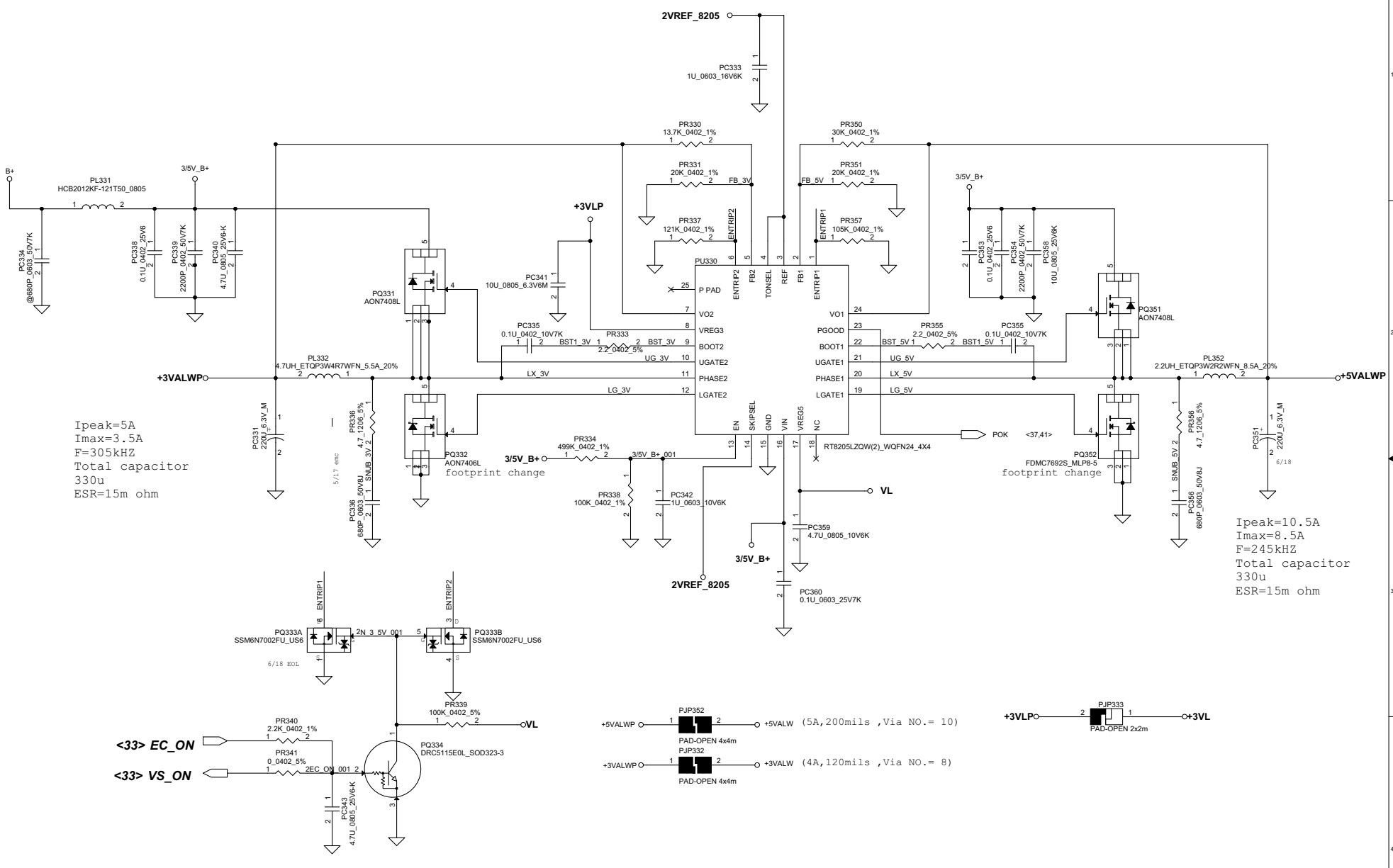
+1.1VALW to +1.1VS



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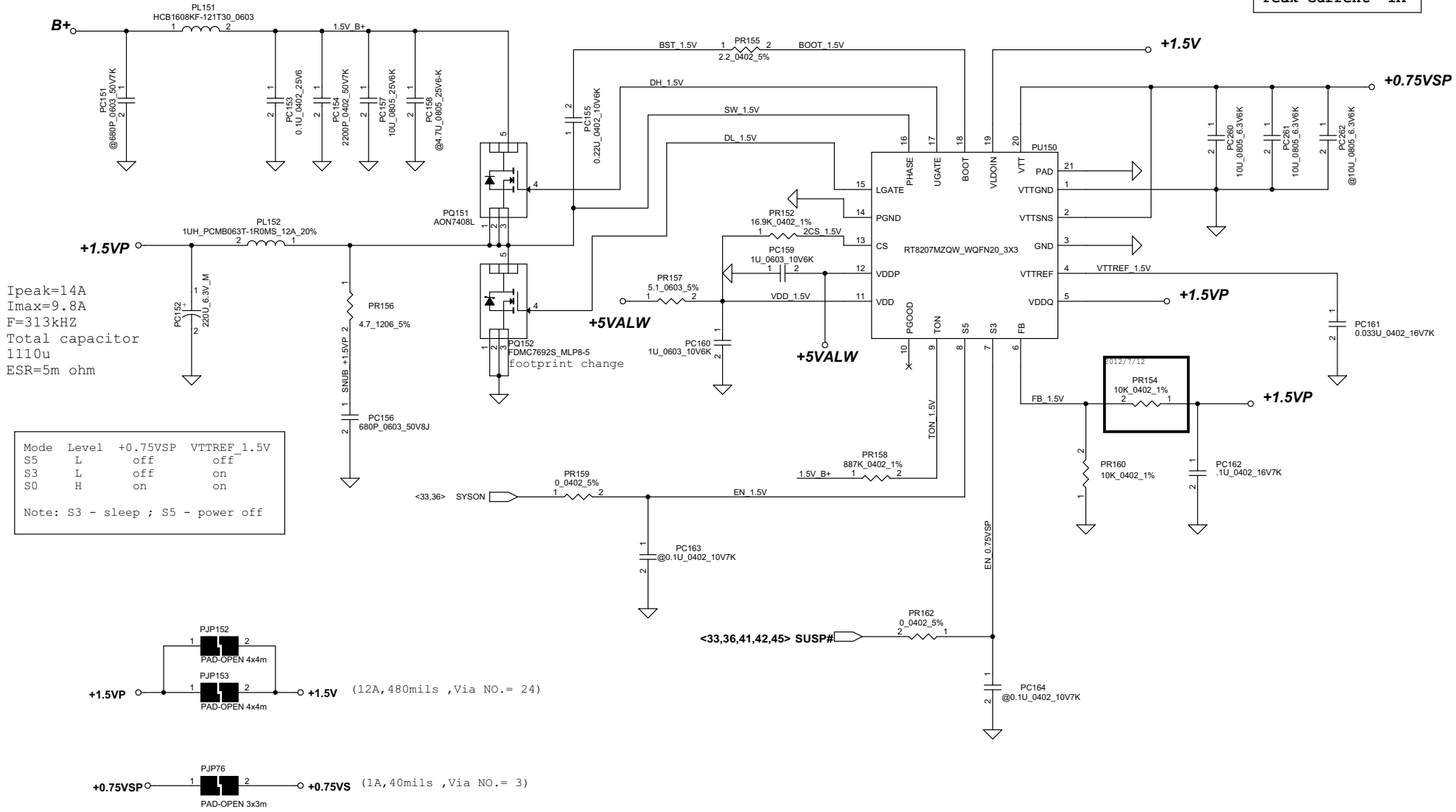


Ipeak=5A
 Imax=3.5A
 F=305kHz
 Total capacitor
 330u
 ESR=15m ohm

Ipeak=10.5A
 Imax=8.5A
 F=245kHz
 Total capacitor
 330u
 ESR=15m ohm

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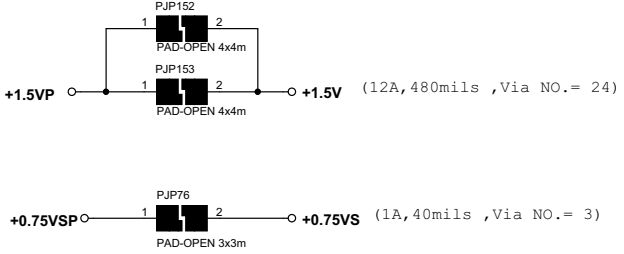
0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A



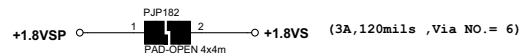
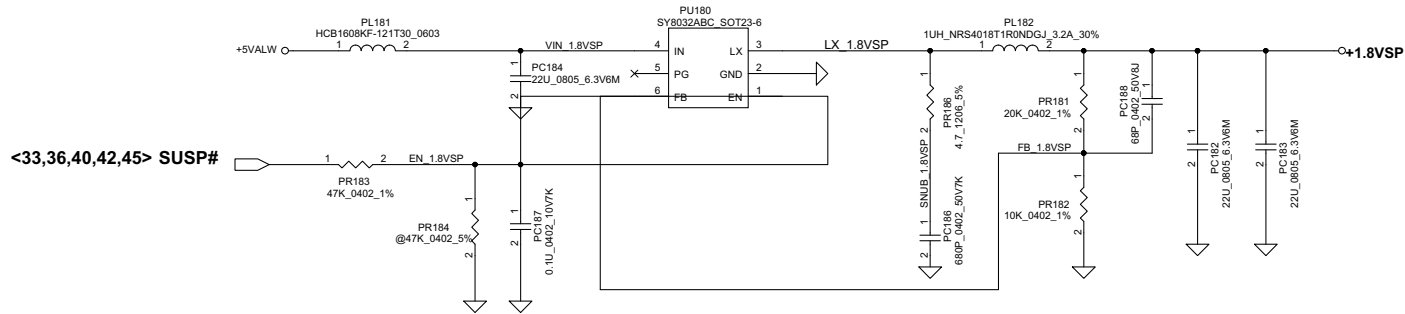
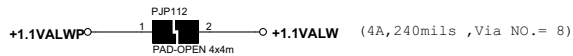
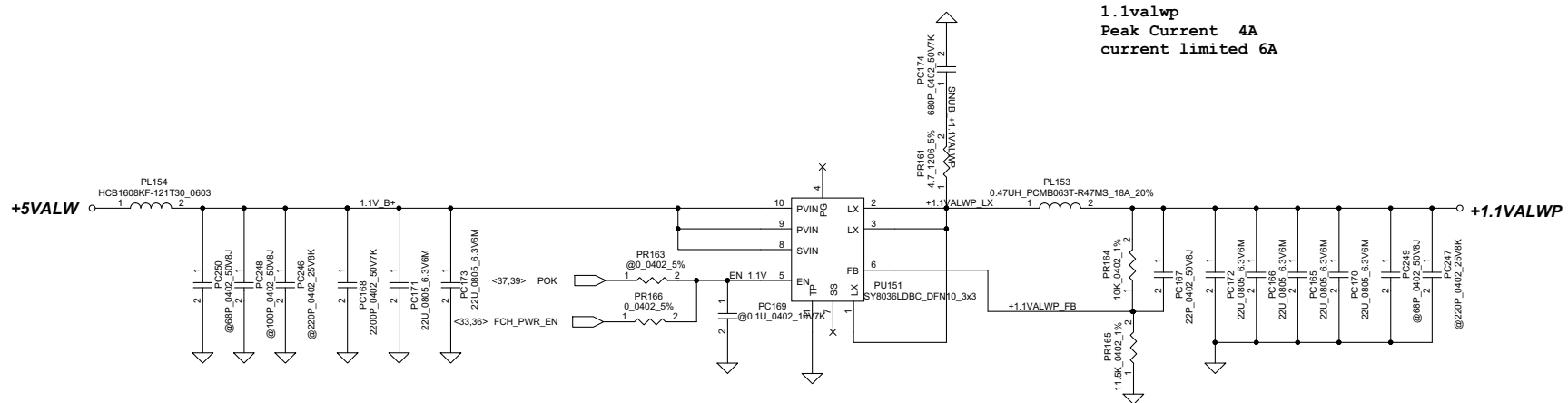
Ipeak=14A
Imax=9.8A
F=313kHz
Total capacitor
1110u
ESR=5m ohm

Mode	Level	+0.75VSP	VTTREF 1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

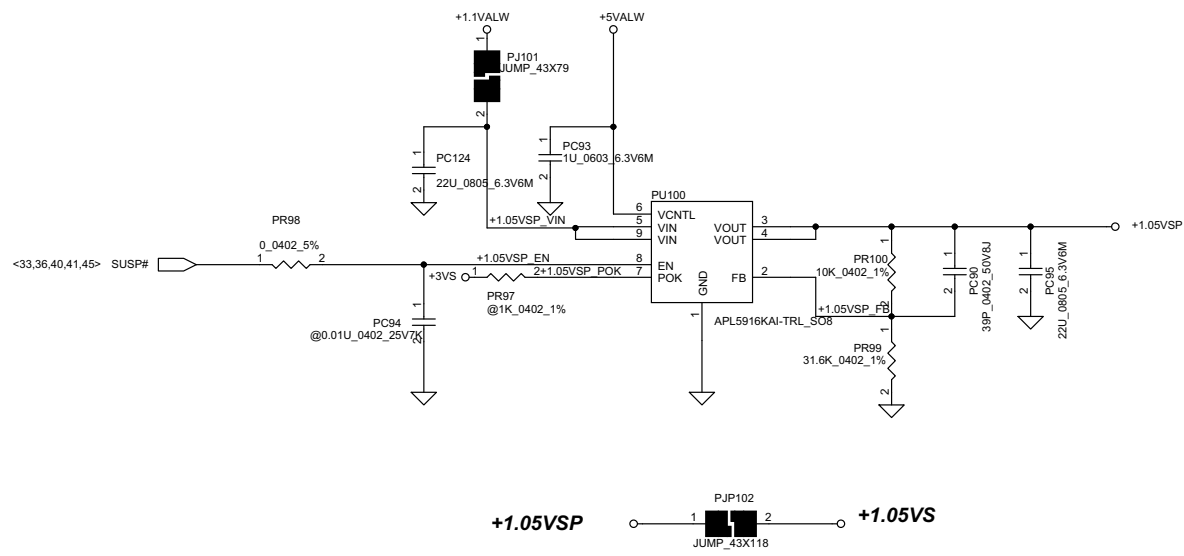
Note: S3 - sleep ; S5 - power off



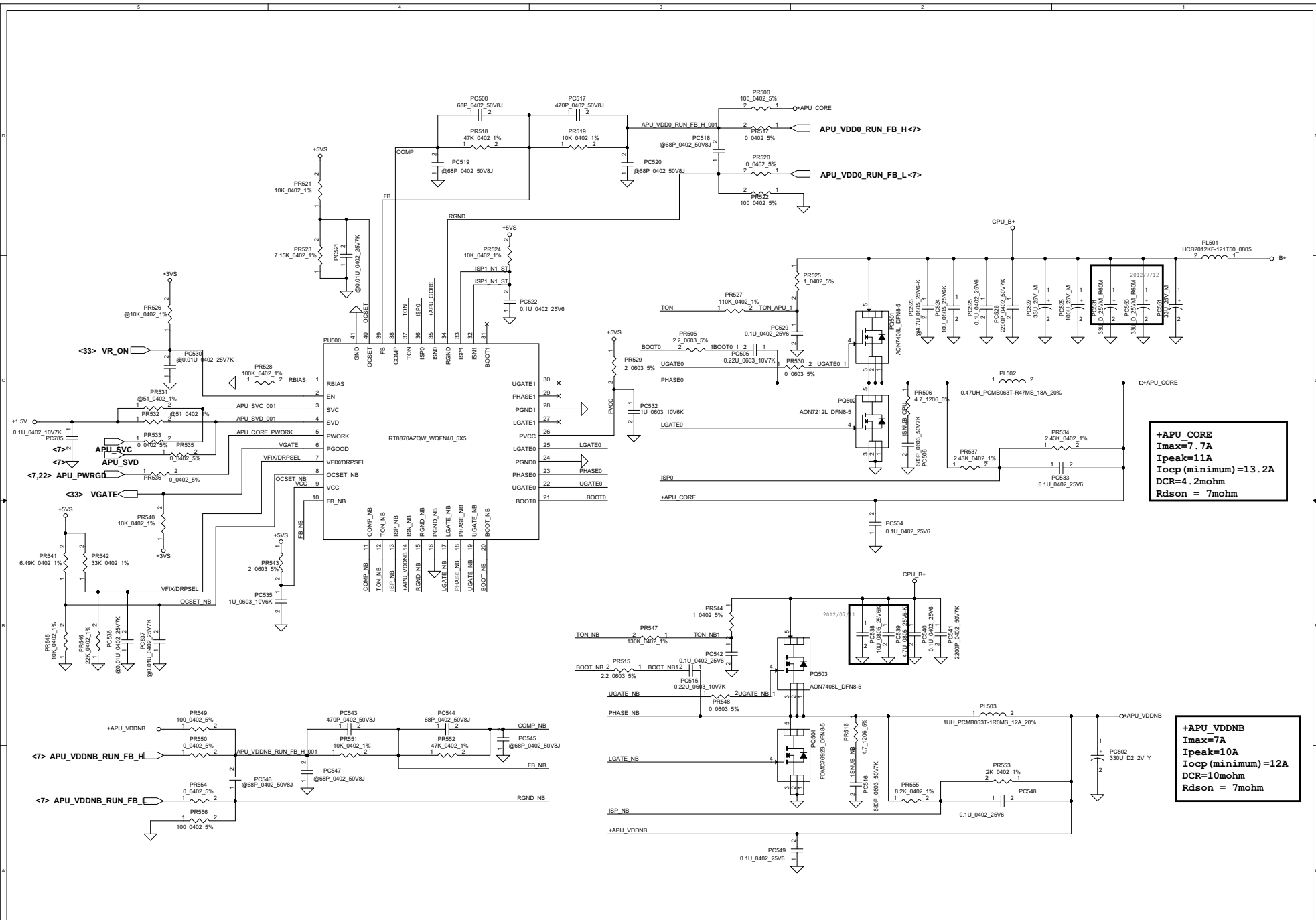
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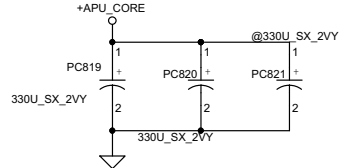
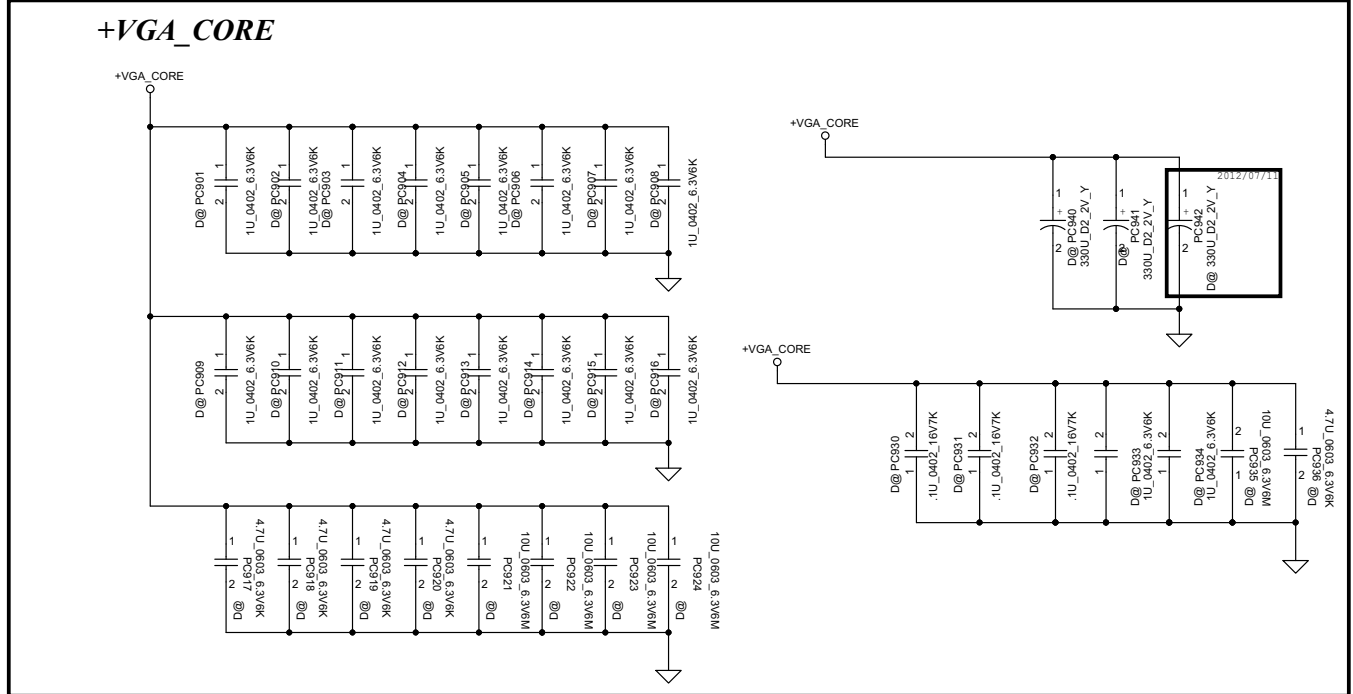
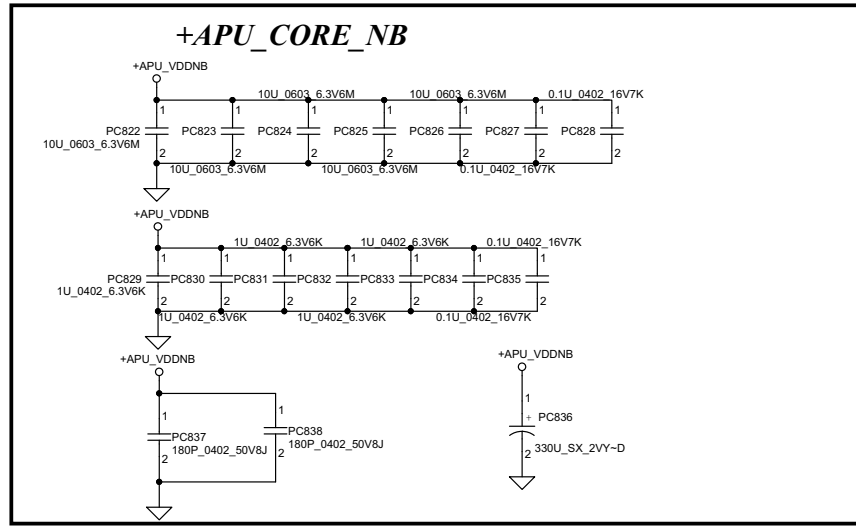
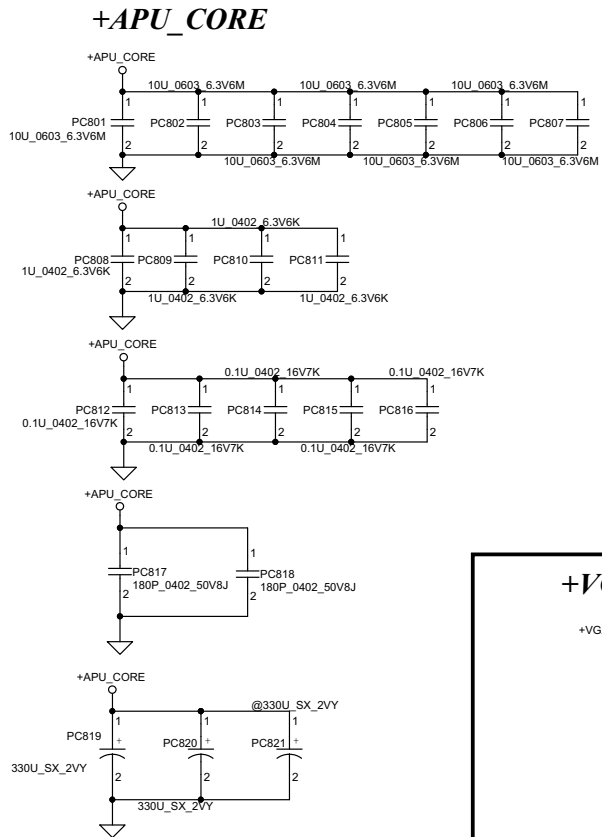
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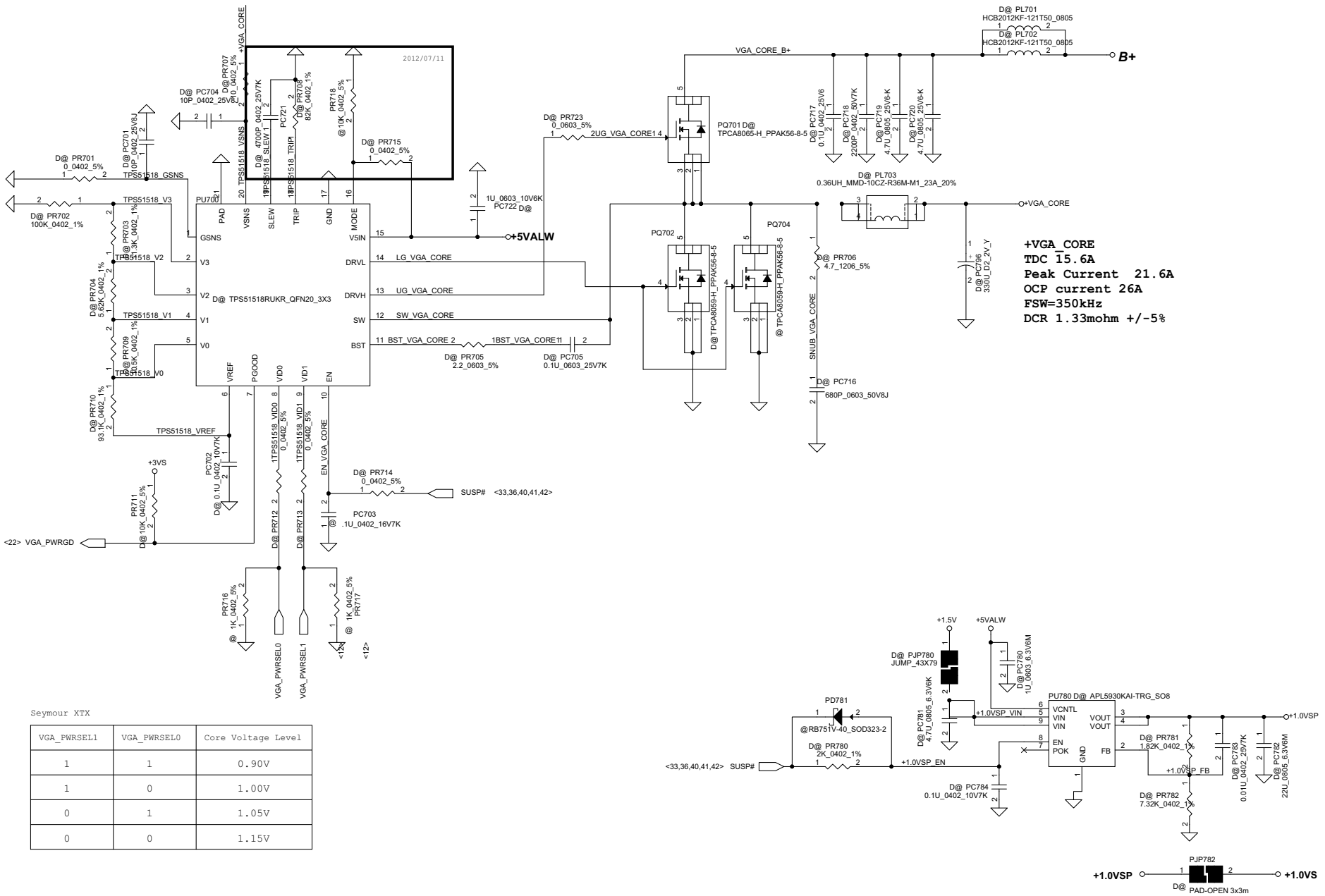
+APU CORE
 $I_{max} = 7.7A$
 $I_{peak} = 11A$
 $I_{ocp}(\text{minimum}) = 13.2A$
 $DCR = 4.2m\Omega$
 $R_{dson} = 7m\Omega$

+APU_VDDNB
 $I_{max} = 7A$
 $I_{peak} = 10A$
 $I_{ocp}(\text{minimum}) = 12A$
 $DCR = 10m\Omega$
 $R_{dson} = 7m\Omega$

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+VGA_CORE
TDC 15.6A
Peak Current 21.6A
OCP current 26A
FSW=350kHz
DCR 1.33mohm +/-5%

Seymour XTx

VGA_PWRSEL1	VGA_PWRSEL0	Core Voltage Level
1	1	0.90V
1	0	1.00V
0	1	1.05V
0	0	1.15V

Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.
Issued Date	2011/12/30	Deciphered Date	2013/10/05	SCHEMATIC, MB A8868
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