Compal Confidential

PAWGE Schematics Document

AMD APU Zacate-FT1 + FCH Hudson-M3L + GPU RobsonXT

2011-11-21

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

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Title	Cover Page	
Size B	Document Number LA8681P	Rev 1.0
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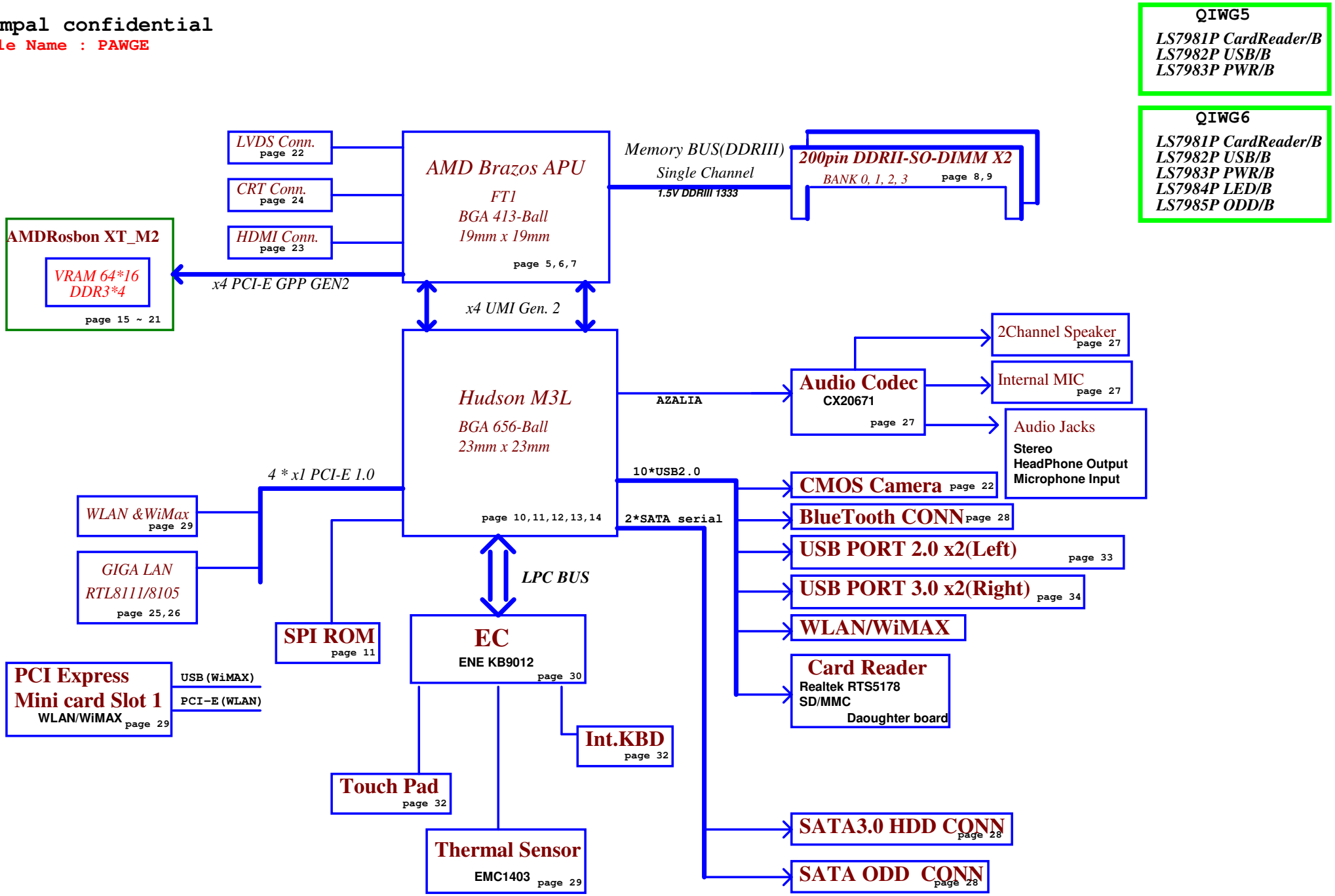
File Name : PAWGE



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Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VS	1.0V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON(WOL)	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+1.1VALW	1.1V always on power rail	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001-011xb	15H

EC SM Bus2 address

Device	Address	HEX
EMC1412-2 (dGPU)	1111-100xb	F8H
EMC1403-2(DDR,WLAN)	1001-101xb	9AH
SB-TSI	1001-100xb	98H

SM Bus Controller 0

(FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		
H_THERMTRIP# (FCH_ALERT#)		

SM Bus Controller 1

(FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		

FCH Hudson-M3L USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	Right USB
Port1	Right USB
Port2	Mini-PCIE
Port3	USB Camera
Port4	NC
Port5	CardReader
Port6	BT
Port7	NC
Port8	NC
Port9	NC
Port10	Left USB1
Port11	Left USB2
Port12	NC
Port13	NC

Brazos PCIE Port List

APU	PCIE0	GPU PCIE x4
	PCIE1	
	PCIE2	
	PCIE3	
FCH	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M3L SATA Port List

SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

BOM Structure

UMA@ : UMA only
PX@ : DIS muxluss PX 4.0
Robson@ : Robson GPU
GIGA@ : RTL8111 1000
8105@ : RTL8105 10/100
DIMM@ : DIMM select
CMOS@ : USB camera
BT@ : BT function
ME@ : ME components
X76@, H1G@, H512@, S1G@, S512@ : VRAM
45@ : 45 Level
HDMI@ : HDMI function
non HDMI@ : HDMI function

AN@ : Apple + Nokia ear phone combo
A@ : Apple ear phone
PCB@ : PCB PN
14@ : 14"
15@ : 15"
BBH@ : BBH
nonBBH@@ : nonBBH@

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Title: Notes List

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Power-Up/Down Sequence

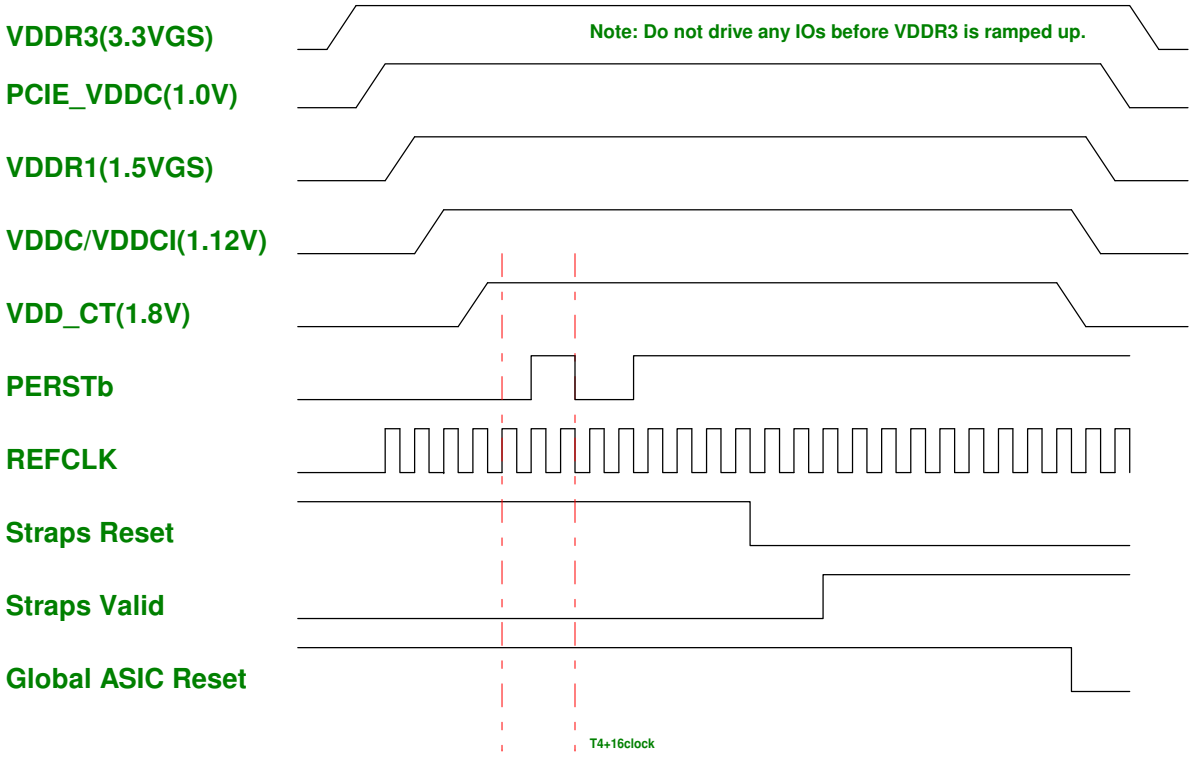
1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

2. VDDR3 should ramp-up before or simultaneously with VDDC.

3. For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

5.VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)



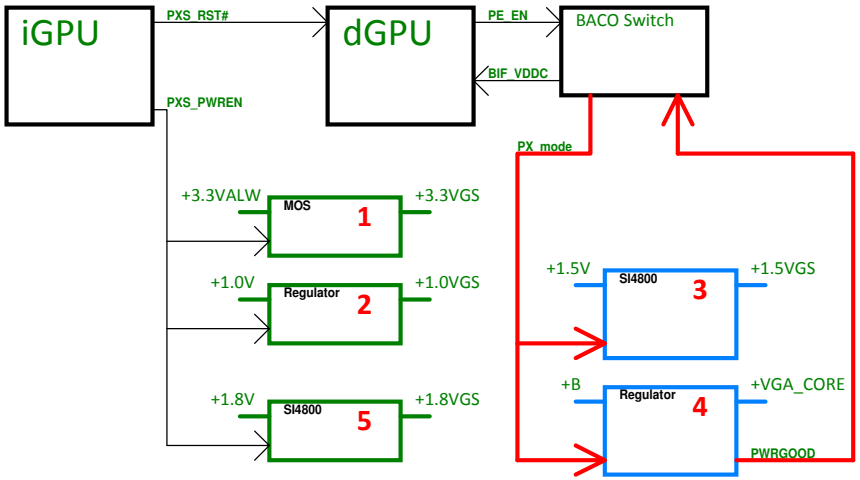
Without BACO option :

PXS_RST# : Low -> Reset dGPU ; High ->Normal operation
PXS_PWREN : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

PXS_RST# : High ->Normal operation (dGPU is not reset on BACO mode)
PXS_PWREN : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	~~1679mA~~
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode) BIF_VDDC=VGA_CORE When GPU enable BIF_VDDC=1.0V When BACO	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



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Title: dGPU Block Diagram

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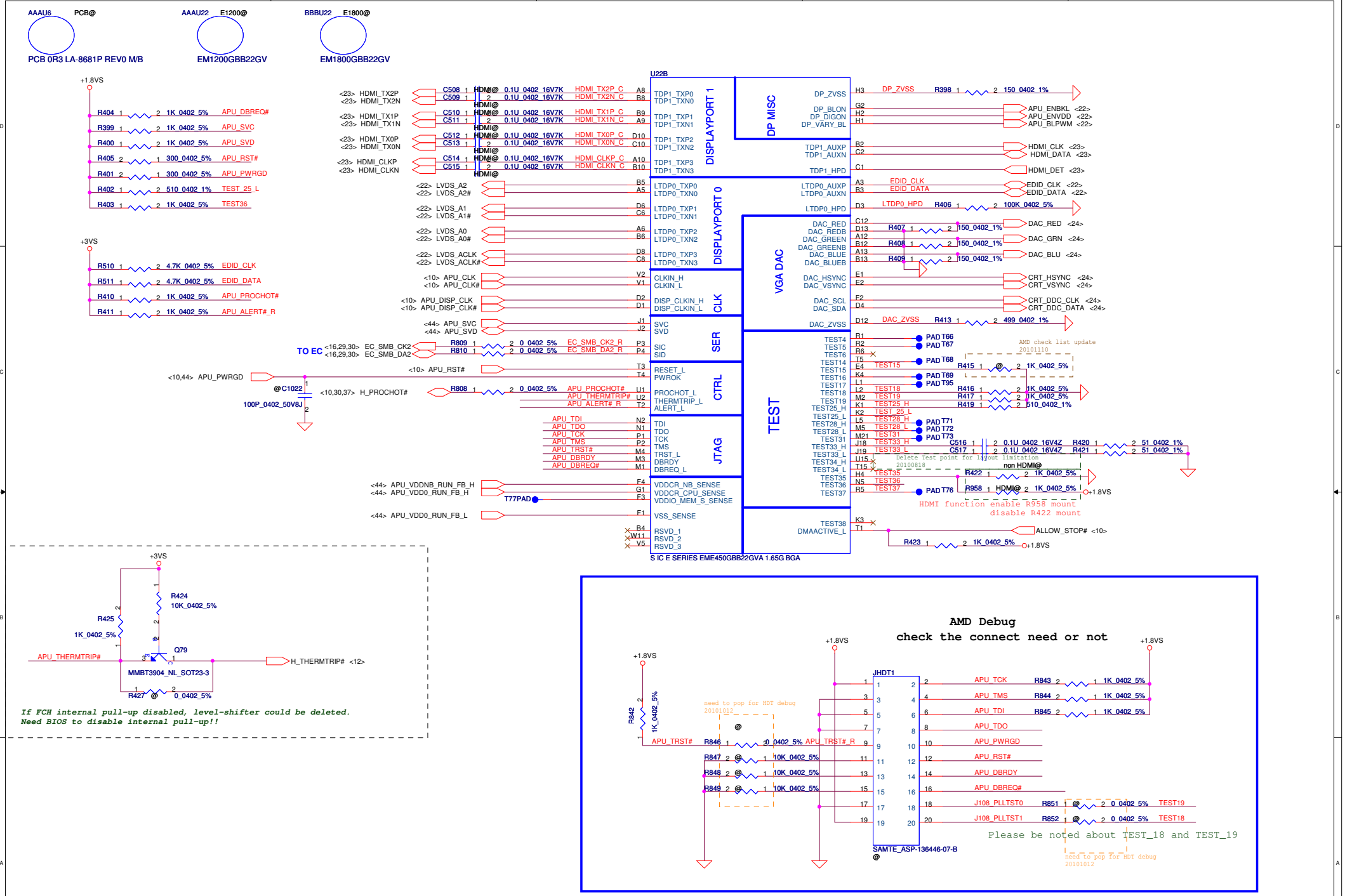

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Title: FT1 CTRL/DP/CRT

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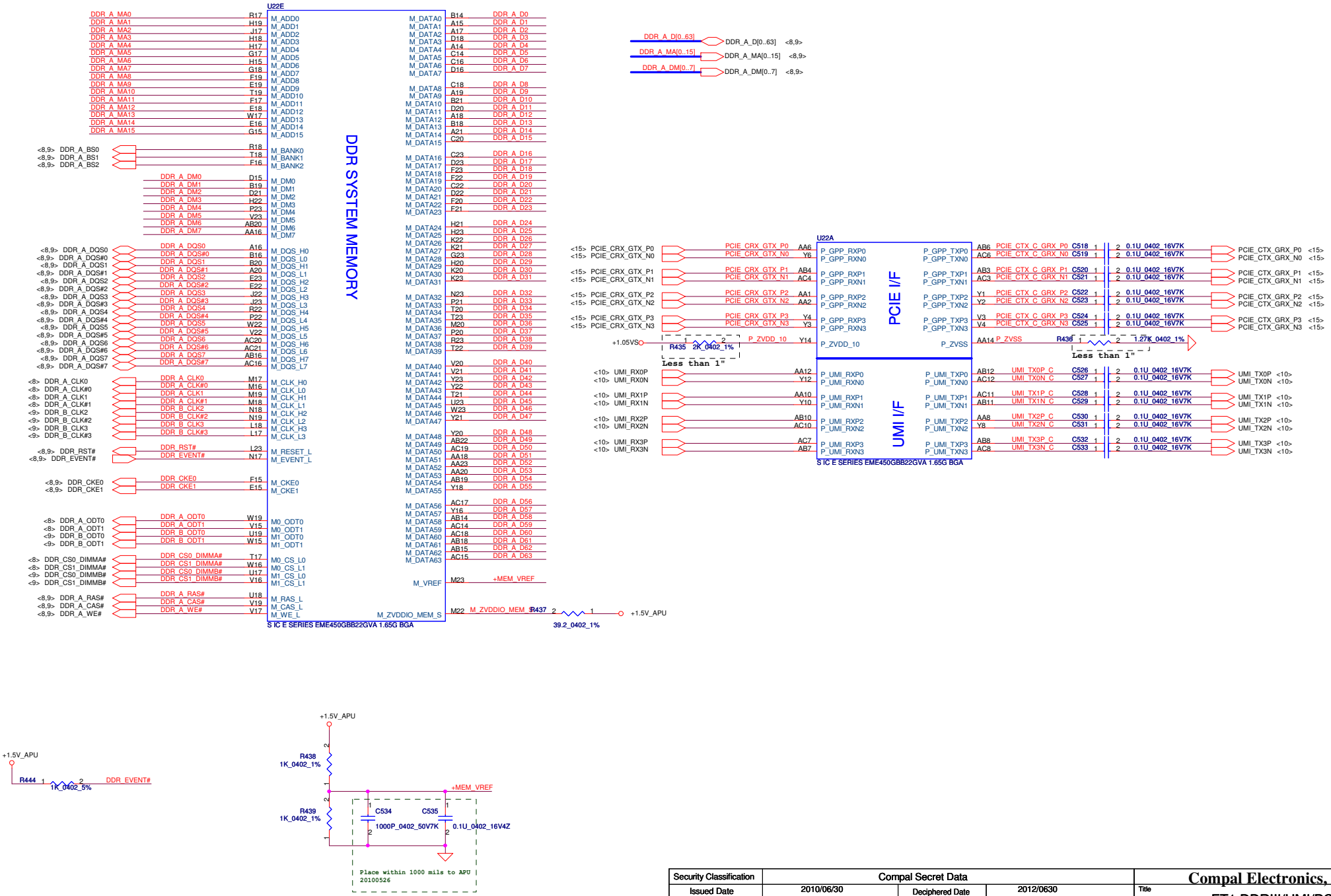
Date: Wednesday, November 30, 2011 | Sheet 5 of 48



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Compal Electronics, Inc.

Title: FT1 DDRIII/UMI/PCIE

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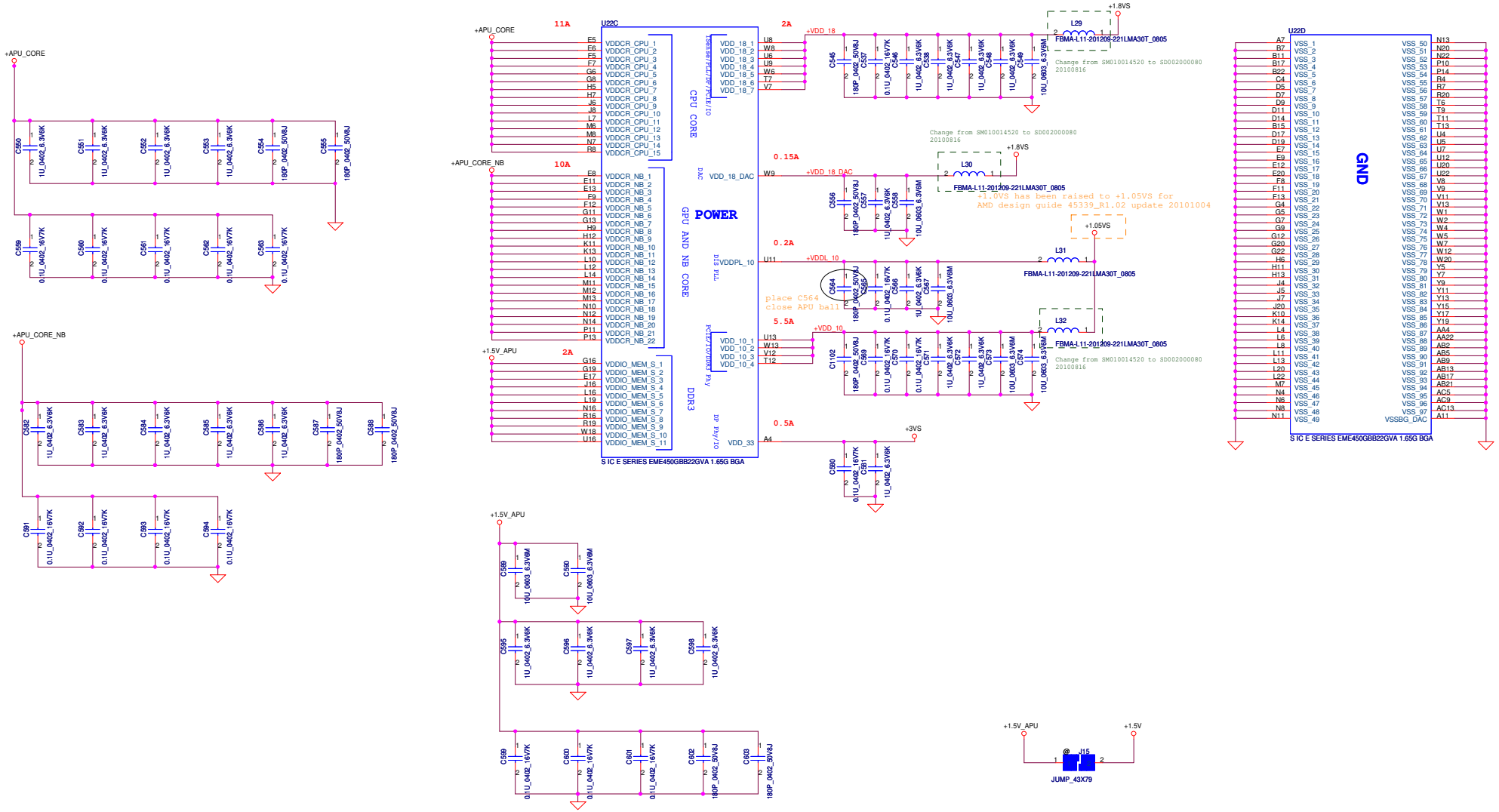
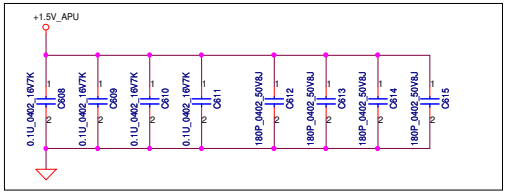
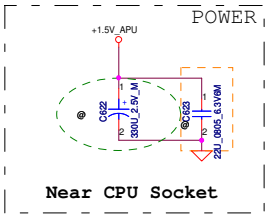


By case (Along split)





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Title: P07-FT1 PWR/VSS

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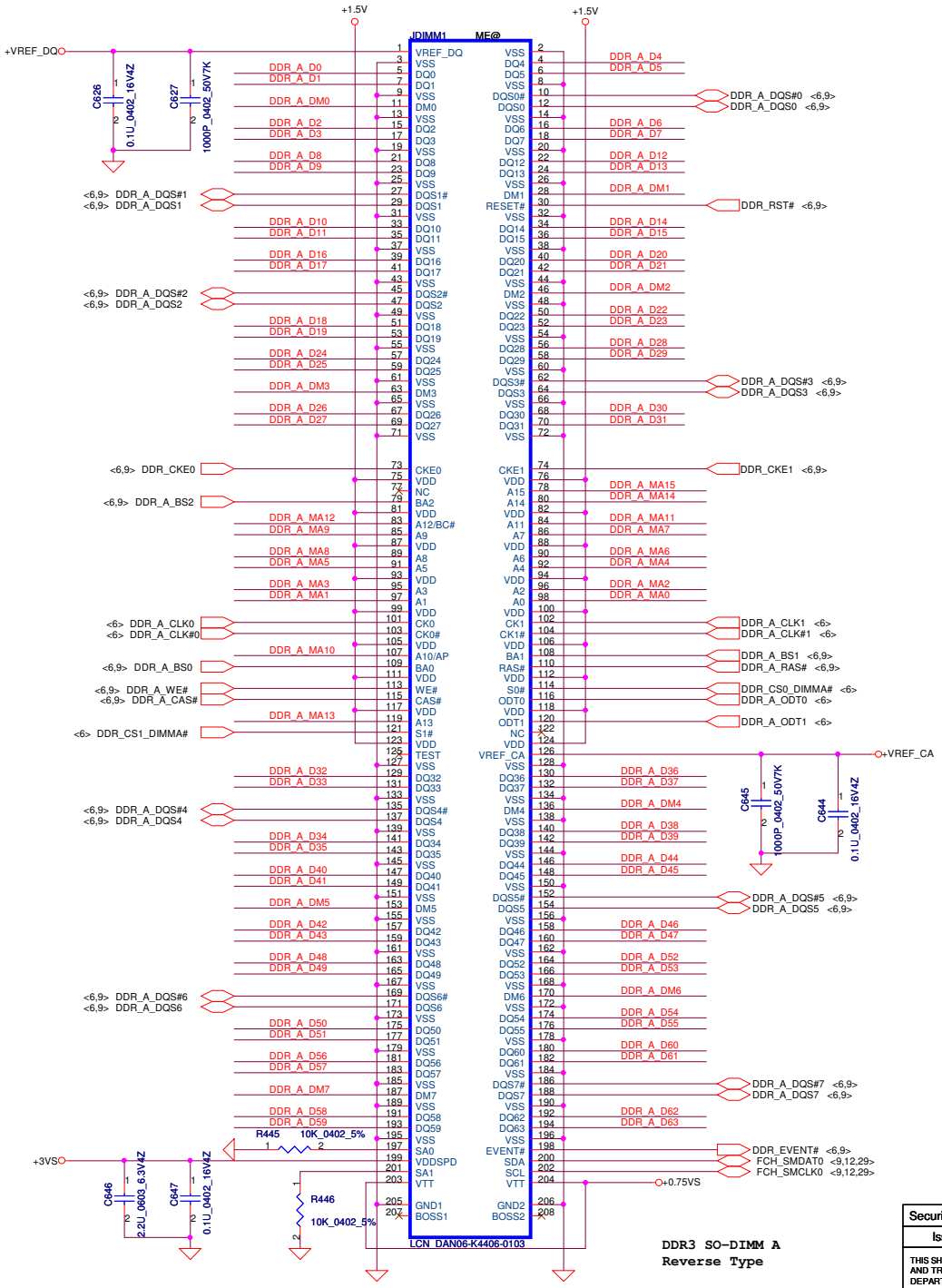

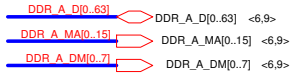

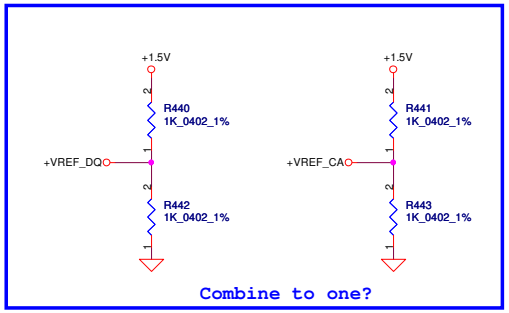

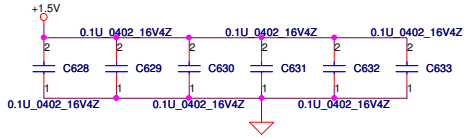

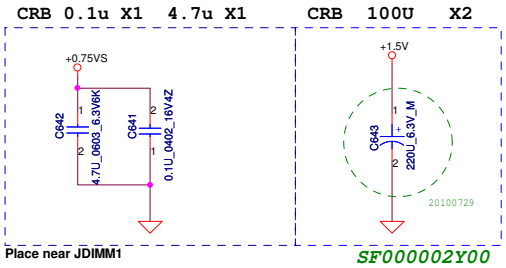

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Title: DDR3 SODIMM-I Socket

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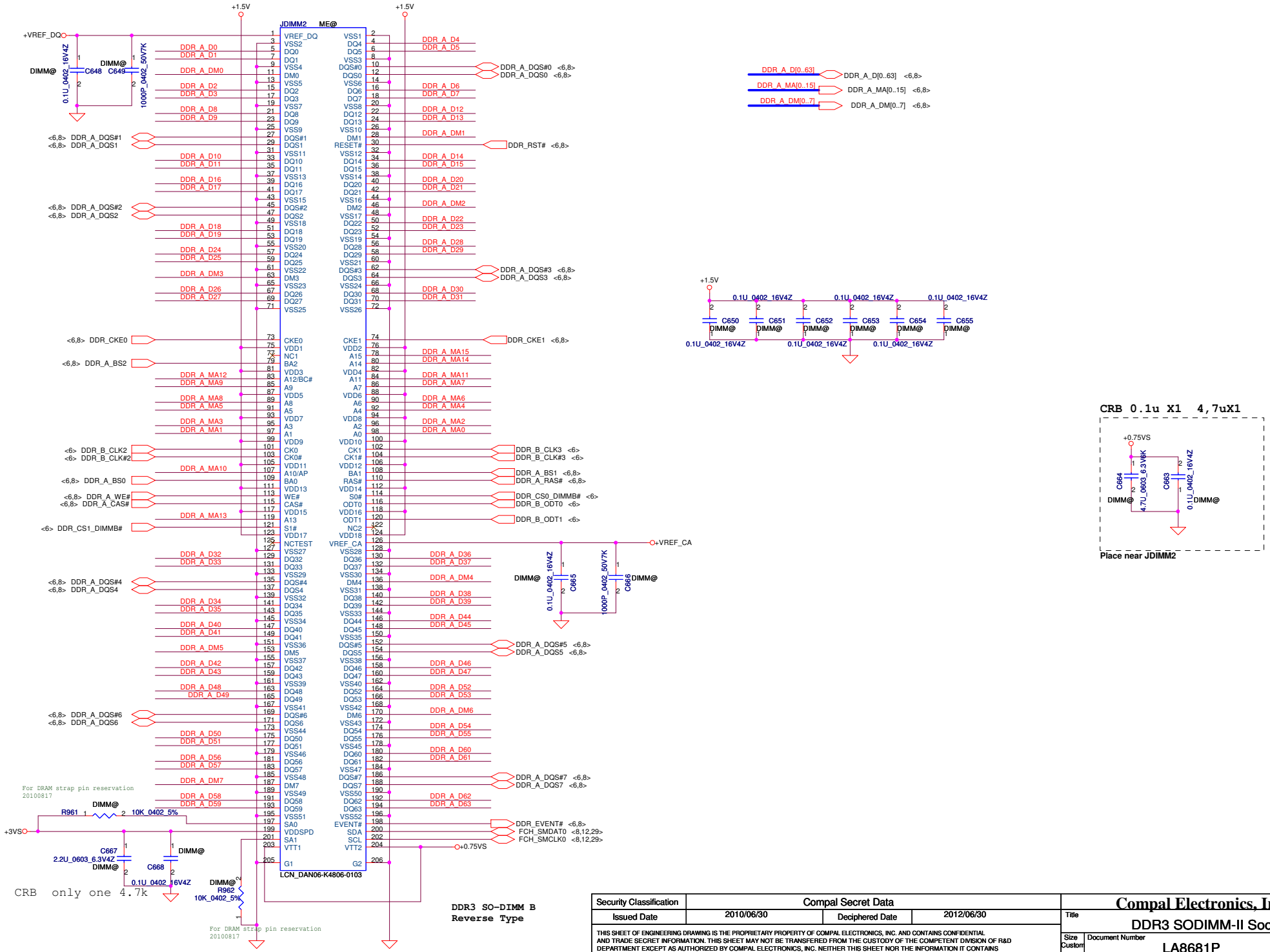

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Compal Electronics, Inc.

Title: DDR3 SODIMM-II Socket

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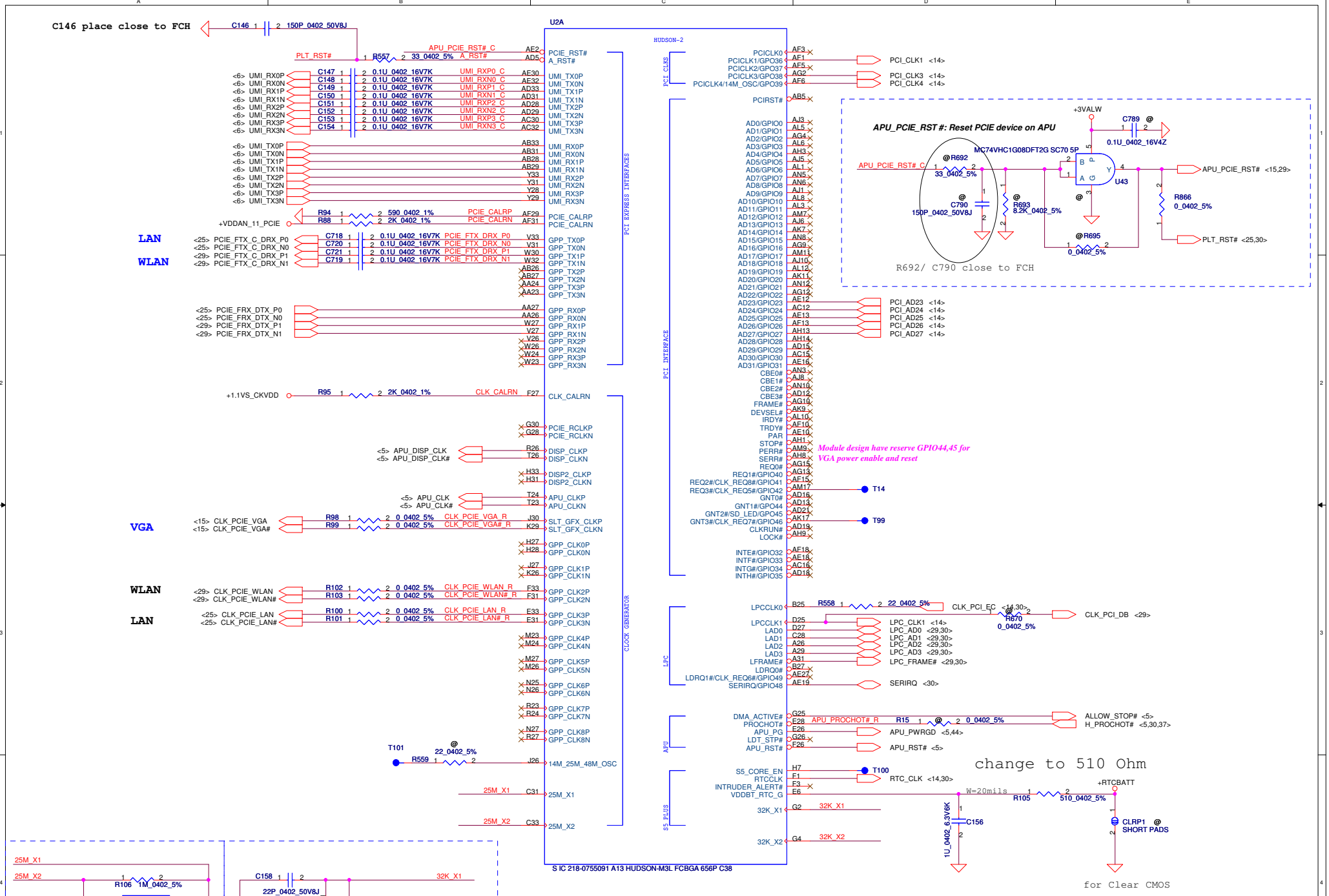

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Title: FCH PCIE/CLK/PCI/LPC/RTC

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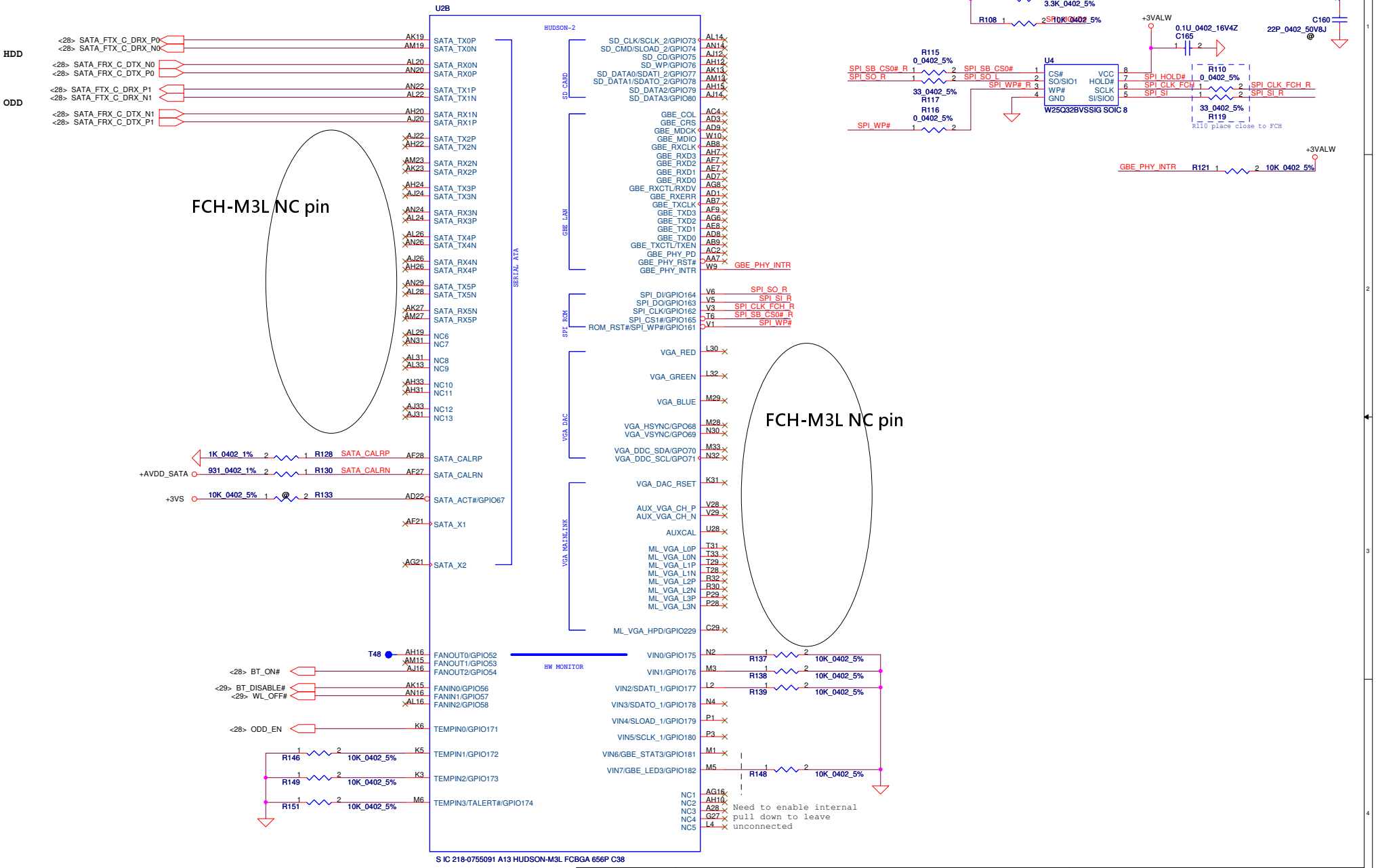
4MB SPI ROM
& Non-share ROM.



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Title: FCH SATA/SPI/VGA/HWM/SD

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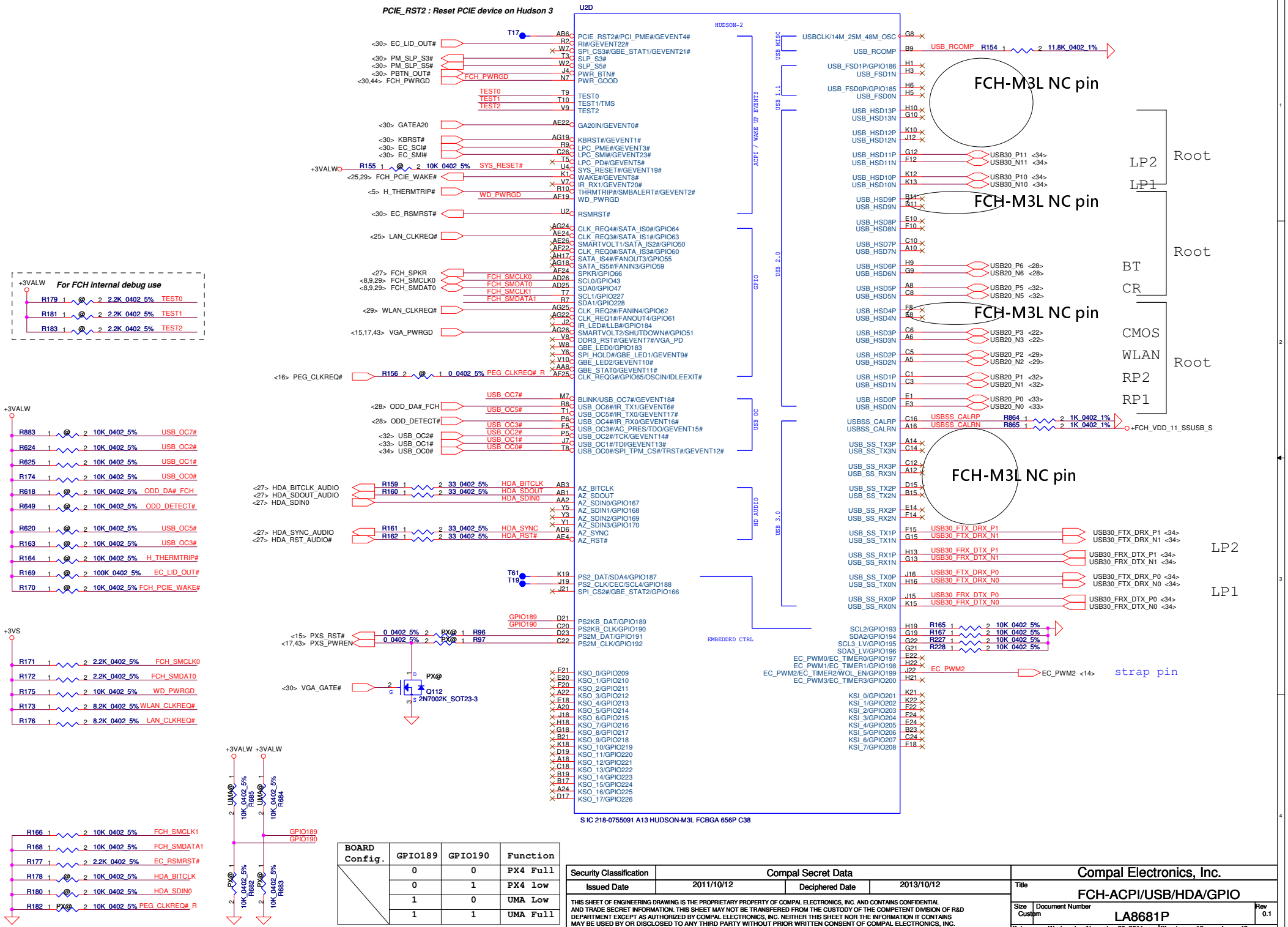

BOARD Config.	GPIO189	GPIO190	Function
	0	0	PX4 Full
	0	1	PX4 low
	1	0	UMA Low
	1	1	UMA Full

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Title: FCH-ACPI/USB/HDA/GPIO

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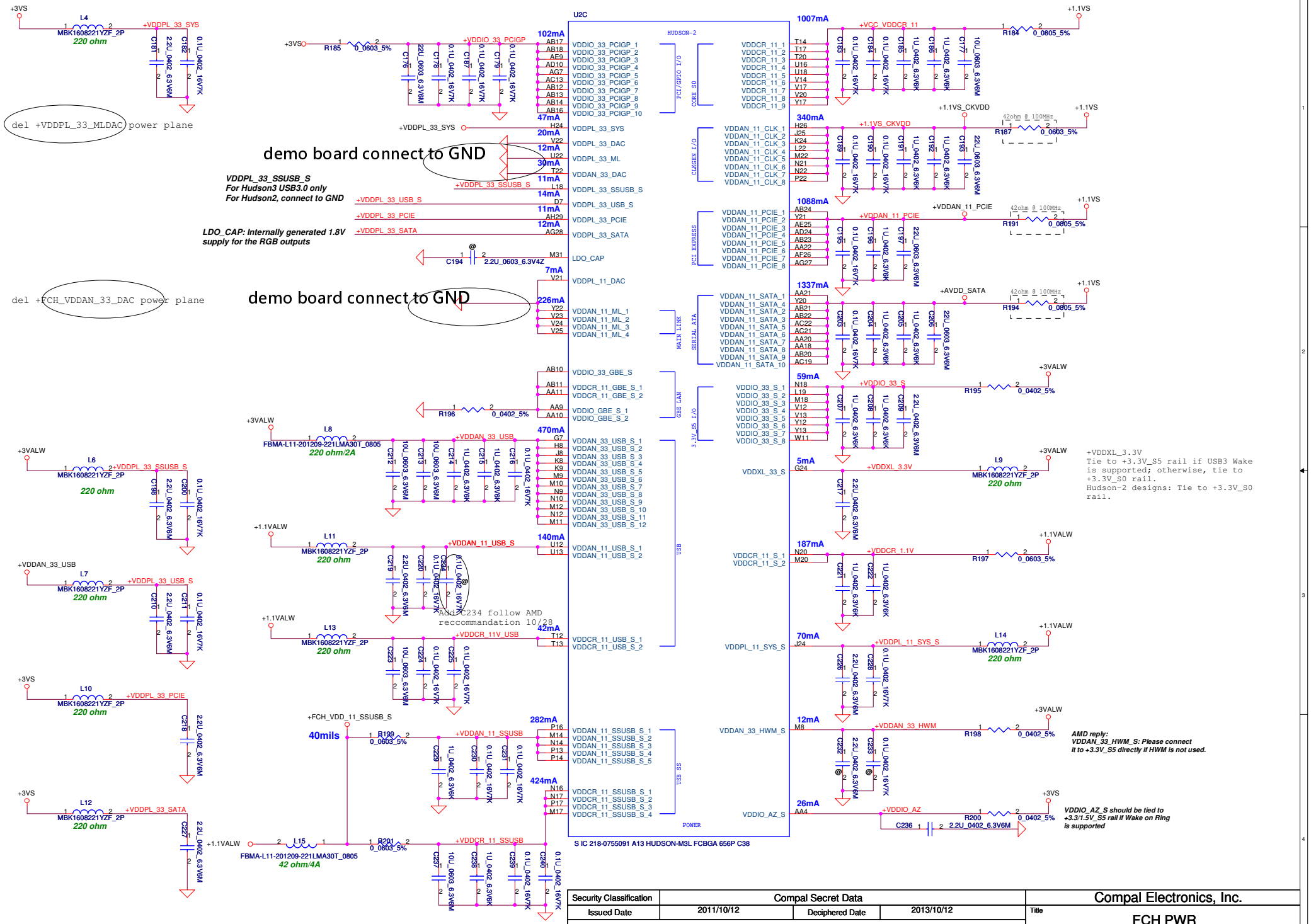

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Title: FCH PWR

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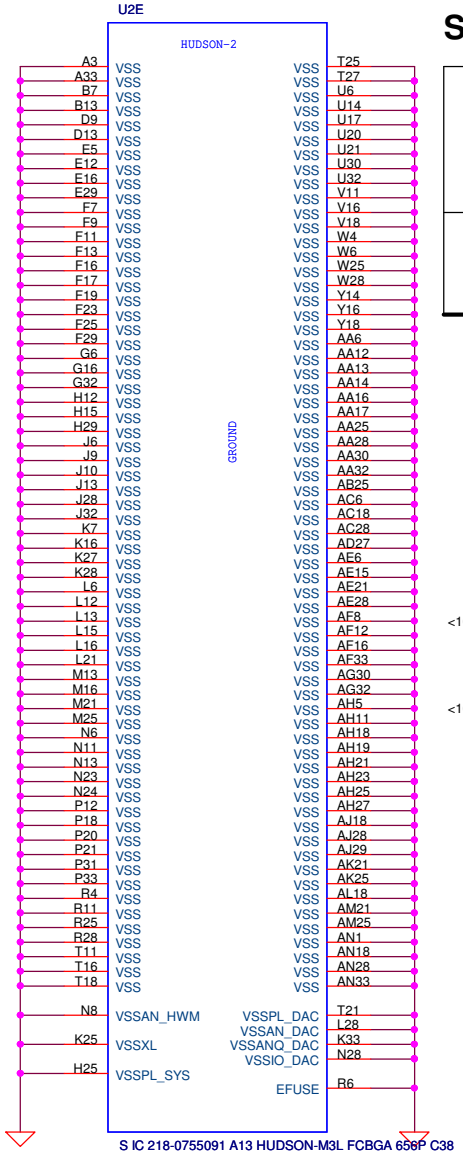


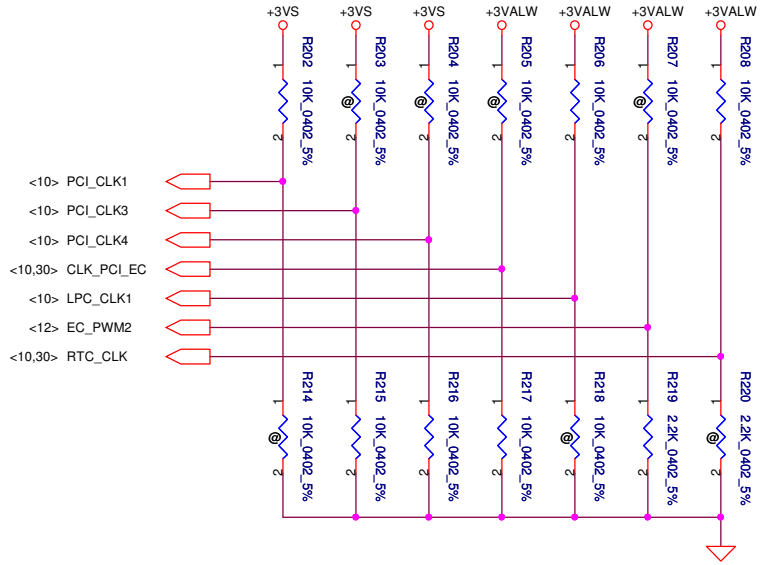
STRAP PINS

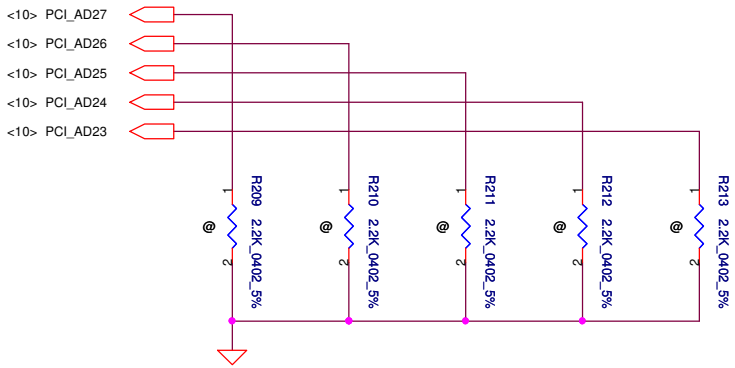
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT





Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

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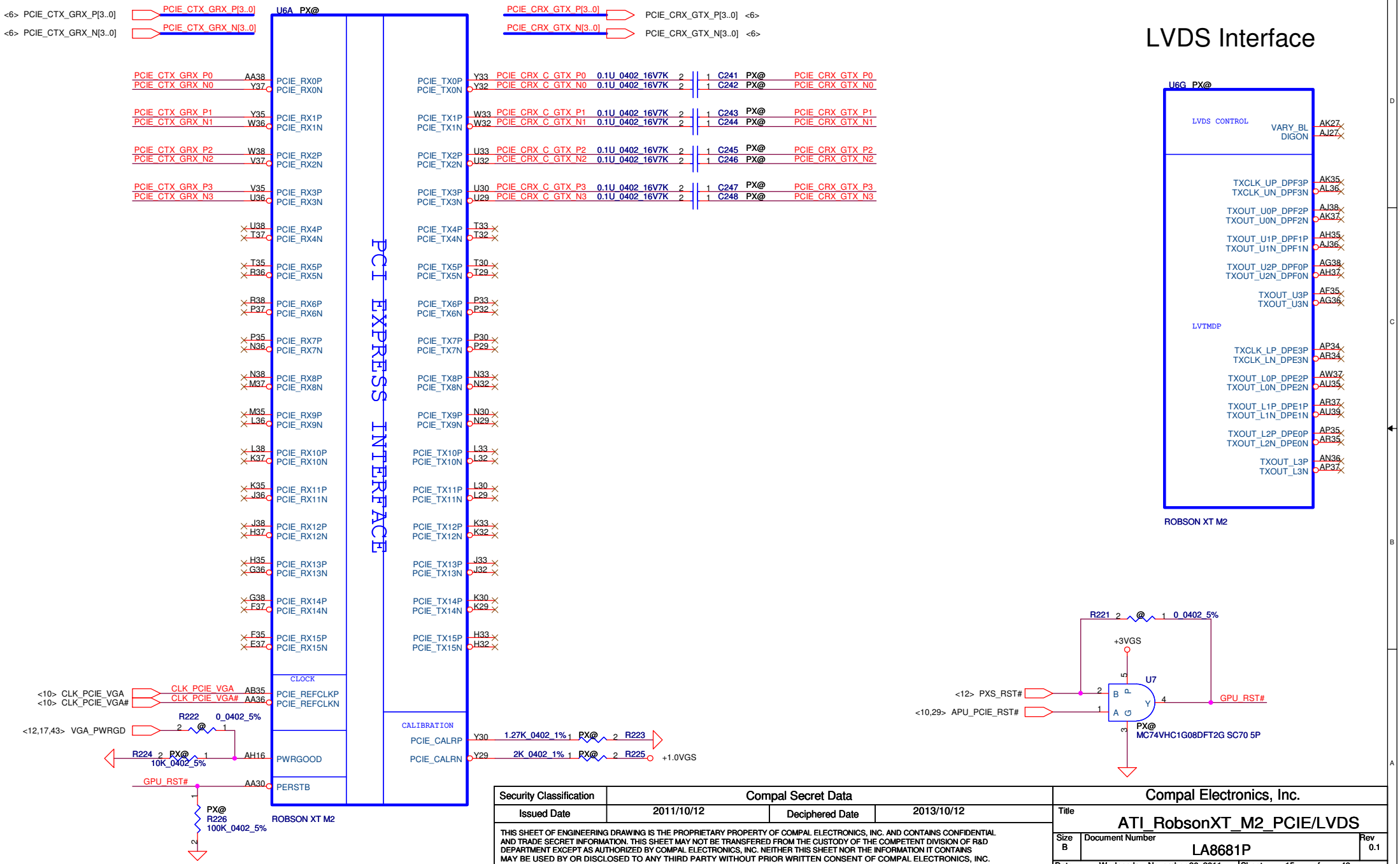
Compal Electronics, Inc.

Title: FCH-VSS/Strap

Size: B | Document Number: LA8681P | Rev: 0.1

Date: Wednesday, November 30, 2011 | Sheet 14 of 48

LVDS Interface



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Compal Electronics, Inc.

Title: ATI_RobsonXT_M2_PCIE/LVDS

Size: B | Document Number: LA8681P | Rev: 0.1

Date: Wednesday, November 30, 2011 | Sheet 15 of 48

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

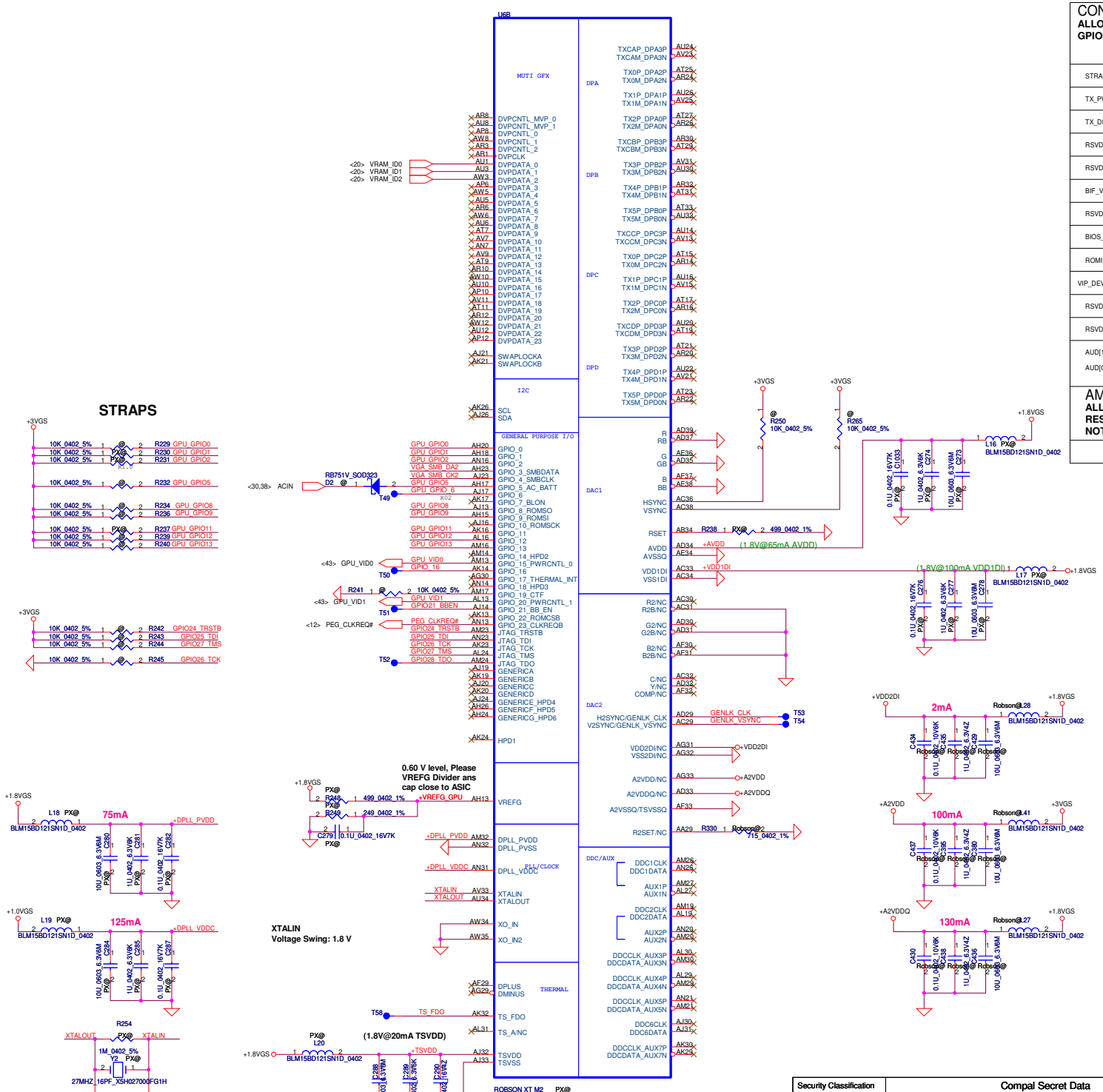
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS 0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIE speed when compliance test 0: 2.5GT/s 1: 5GT/s	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0: disable 1: enable	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

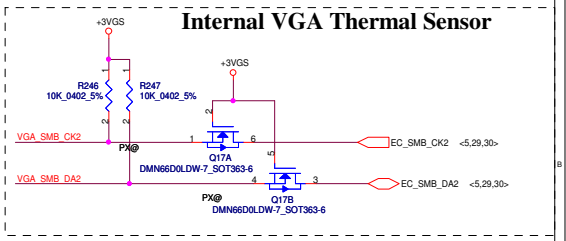
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21 H2SYNC GENERICC GPIO2 GPIO8

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)



Internal VGA Thermal Sensor



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Issued Date	2011/10/12	Deciphered Date	2013/10/12

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Compal Electronics, Inc.

Title: ATI_RobsonXT_M2_Main_MSIC

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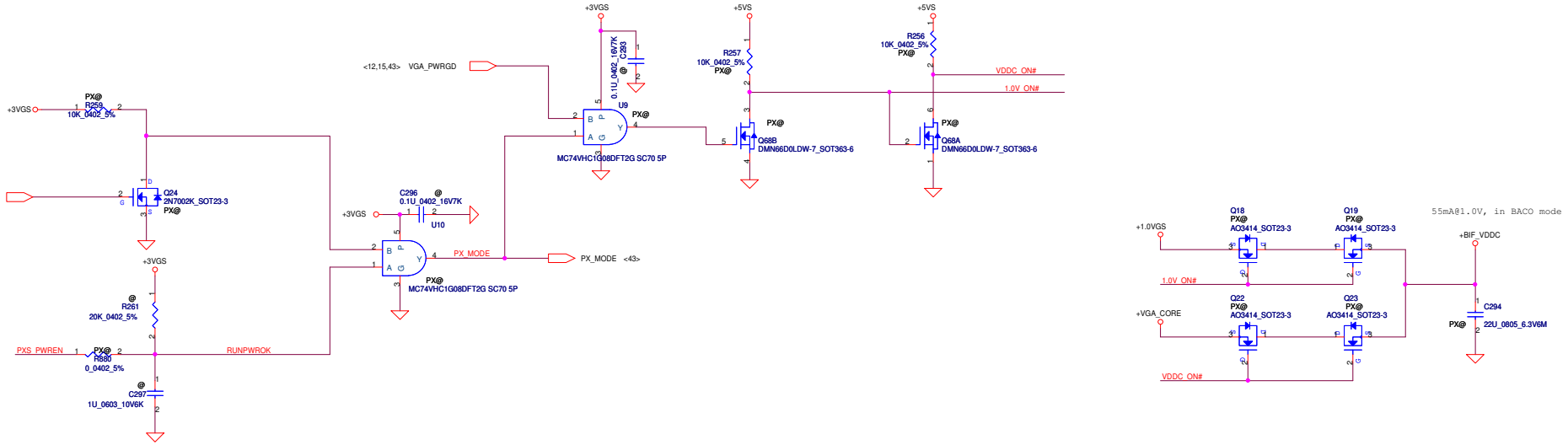
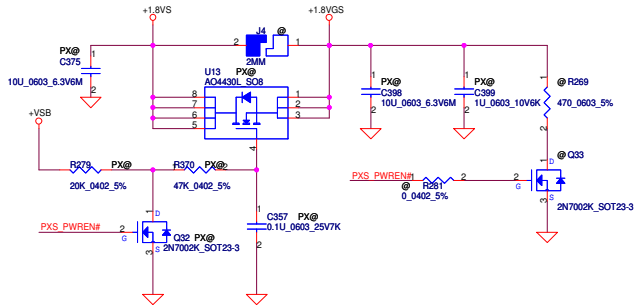
Date: Wednesday, November 30, 2011 | Sheet 16 of 48



+1.8VS TO +1.8VGS



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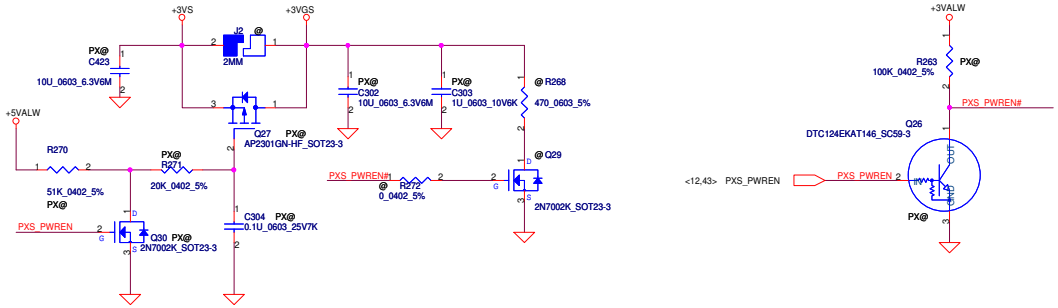
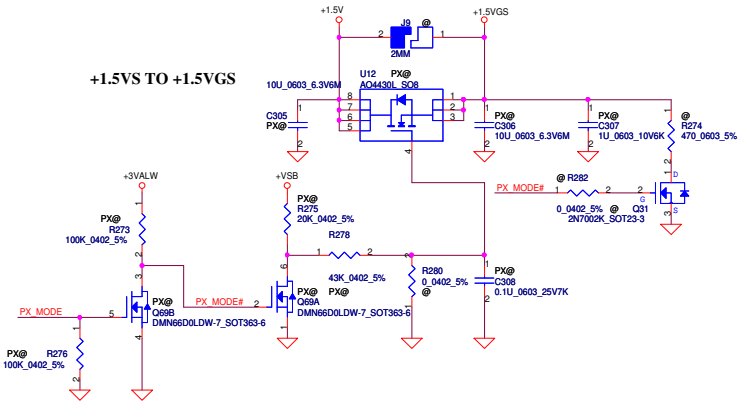
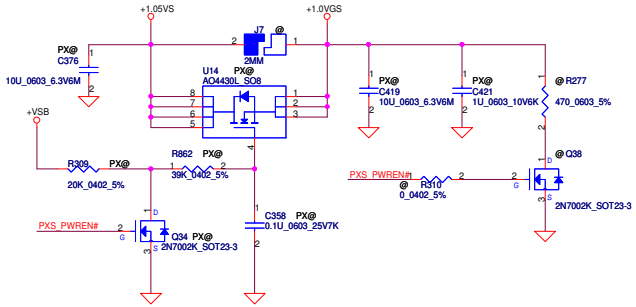


+1.5VS TO +1.5VGS



+1.05VS TO +1.0VGS



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Issued Date	2011/10/12	Deciphered Date	2013/10/12	Title: ATI_RobsonXT_M2_BACO POWER
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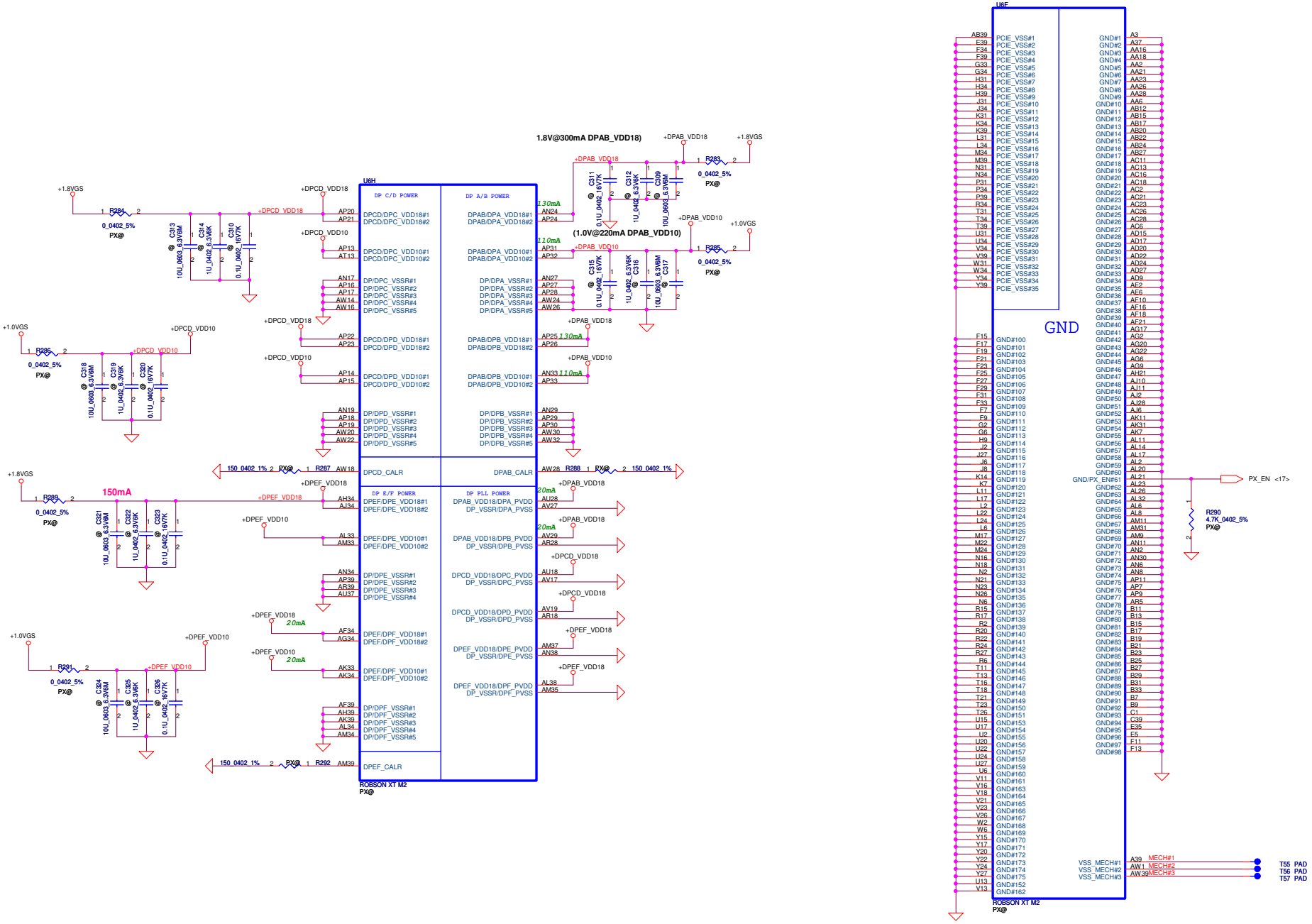
				Date: Wednesday, November 30, 2011; Sheet 17 of 48



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Issued Date	2011/10/12	Deciphered Date	2013/10/12

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Compal Electronics, Inc.

Title: ATI_RobsonXT_M2_PWR_GND

Size	Document Number	Rev
C	LA8681P	0.1

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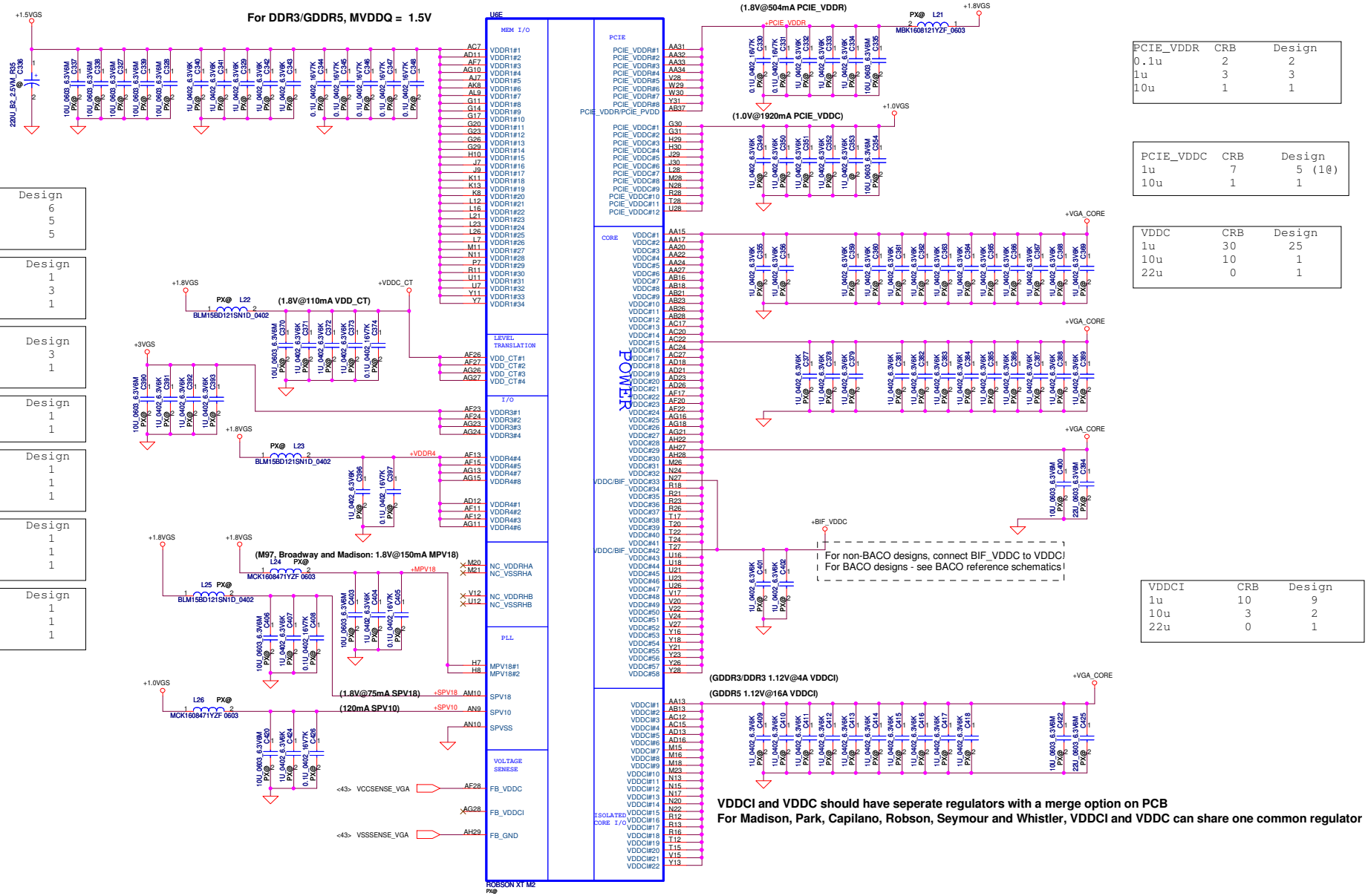

VDDR1	CRB	Design
0.1u	6	6
1u	10	5
10u	6	5

VDD_CT	CRB	Design
0.1u	1	1
1u	3	3
10u	1	1

VDDR3	CRB	Design
1u	3	3
10u	1	1

VDDR4	CRB	Design
0.1u	1	1
1u	1	1

MPV18	CRB	Design
0.1u	2	1
1u	2	1
10u	1	1

SPV18	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

SPV10	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

PCIE_VDDR	CRB	Design
0.1u	2	2
1u	3	3
10u	1	1

PCIE_VDDC	CRB	Design
1u	7	5 (1@)
10u	1	1

VDDC	CRB	Design
1u	30	25
10u	10	1
22u	0	1

VDDCI	CRB	Design
1u	10	9
10u	3	2
22u	0	1

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Issued Date	2011/10/12	Deciphered Date	2013/10/12

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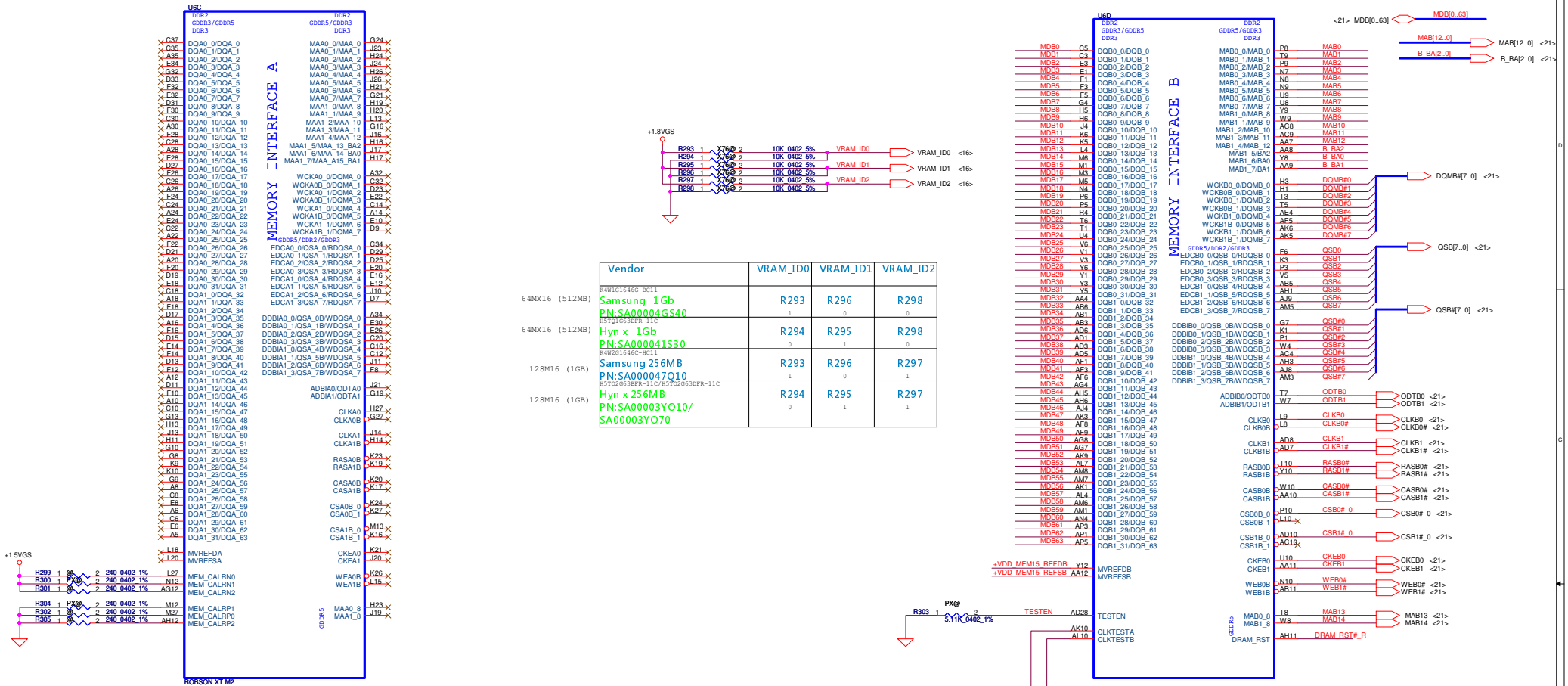
Compal Electronics, Inc.

Title: ATI_RobsonXT_M2_Power

Size: C | Document Number: LA8681P | Rev: 0.1

Date: Wednesday, November 30, 2011 | Sheet 19 of 48



Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
64MX16 (512MB) K4W1G1646G-BC11 Samsung 1Gb PN:SA00004GS40	R293 1	R296 0	R298 0
64MX16 (512MB) H5TQ1G63DFR-11C Hynix 1Gb PN:SA000041S30	R294 0	R295 1	R298 0
128M16 (1GB) K4W2G1646C-HC11 Samsung 256MB PN:SA000047Q10	R293 1	R296 0	R297 1
128M16 (1GB) H5TQ2G63DFR-11C/H5TQ2G63DFR-11C Hynix 256MB PN:SA00003YO10/ SA00003YO70	R294 0	R295 1	R297 1

PX@

	Rosbon M2
R299	@
R300	POP
R301	@
R302	@
R304	POP
R305	@

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

route 50ohms single-ended/100ohms diff and keep short
Debug only, for clock observation, if not needed, DNI
5mil 5mil

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Compal Electronics, Inc.

Title: ATI_RobsonXT_M2_MEM IF

Size	Document Number	Rev
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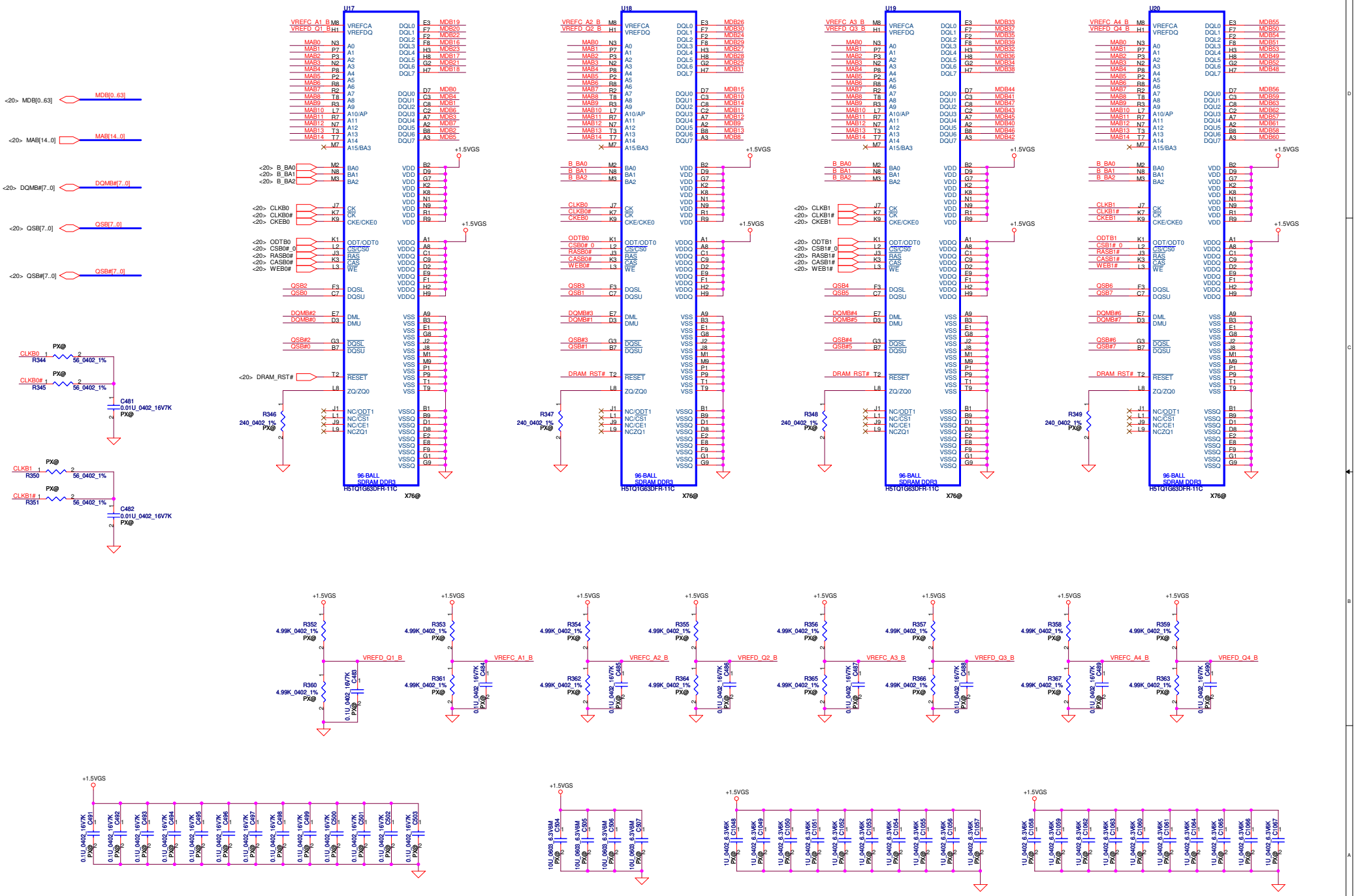

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Compal Electronics, Inc.

Title: ATI_RobsonXT_M2_VRAM_B

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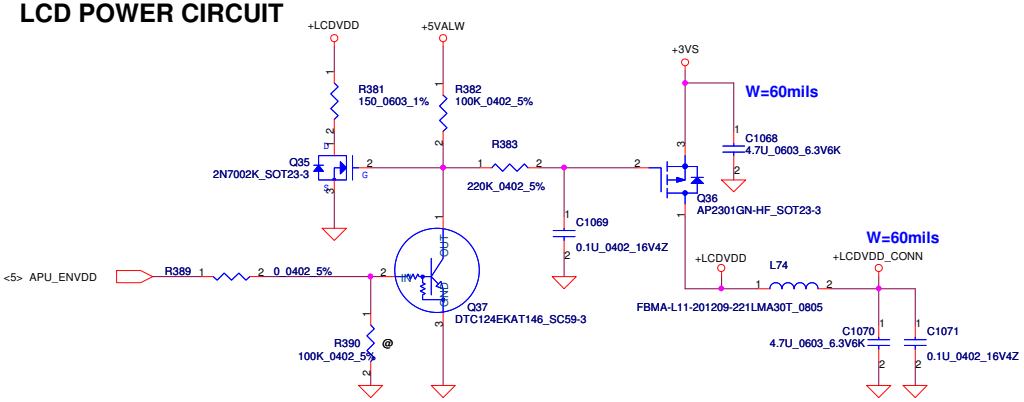
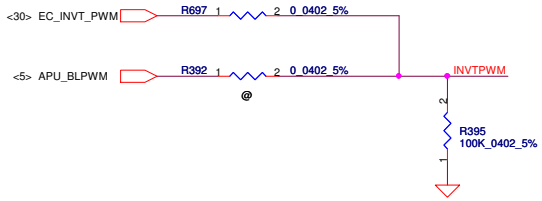
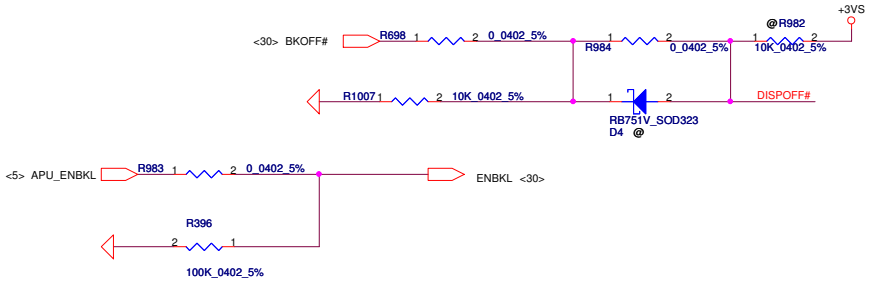
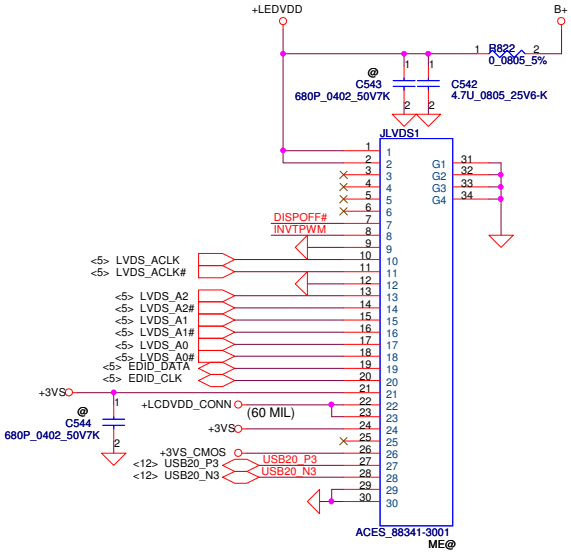
LCD POWER CIRCUIT

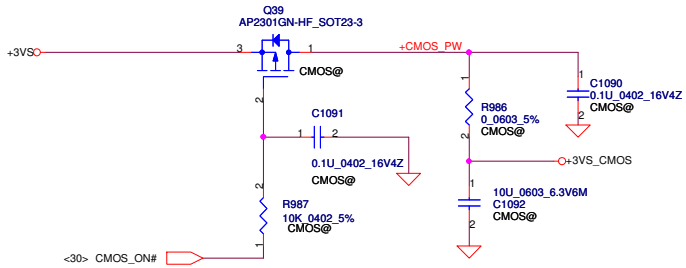








CMOS Camera



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Compal Electronics, Inc.

Title: LVDS/CAMERA

Size: B | Document Number: LA8681P | Rev: 0.1

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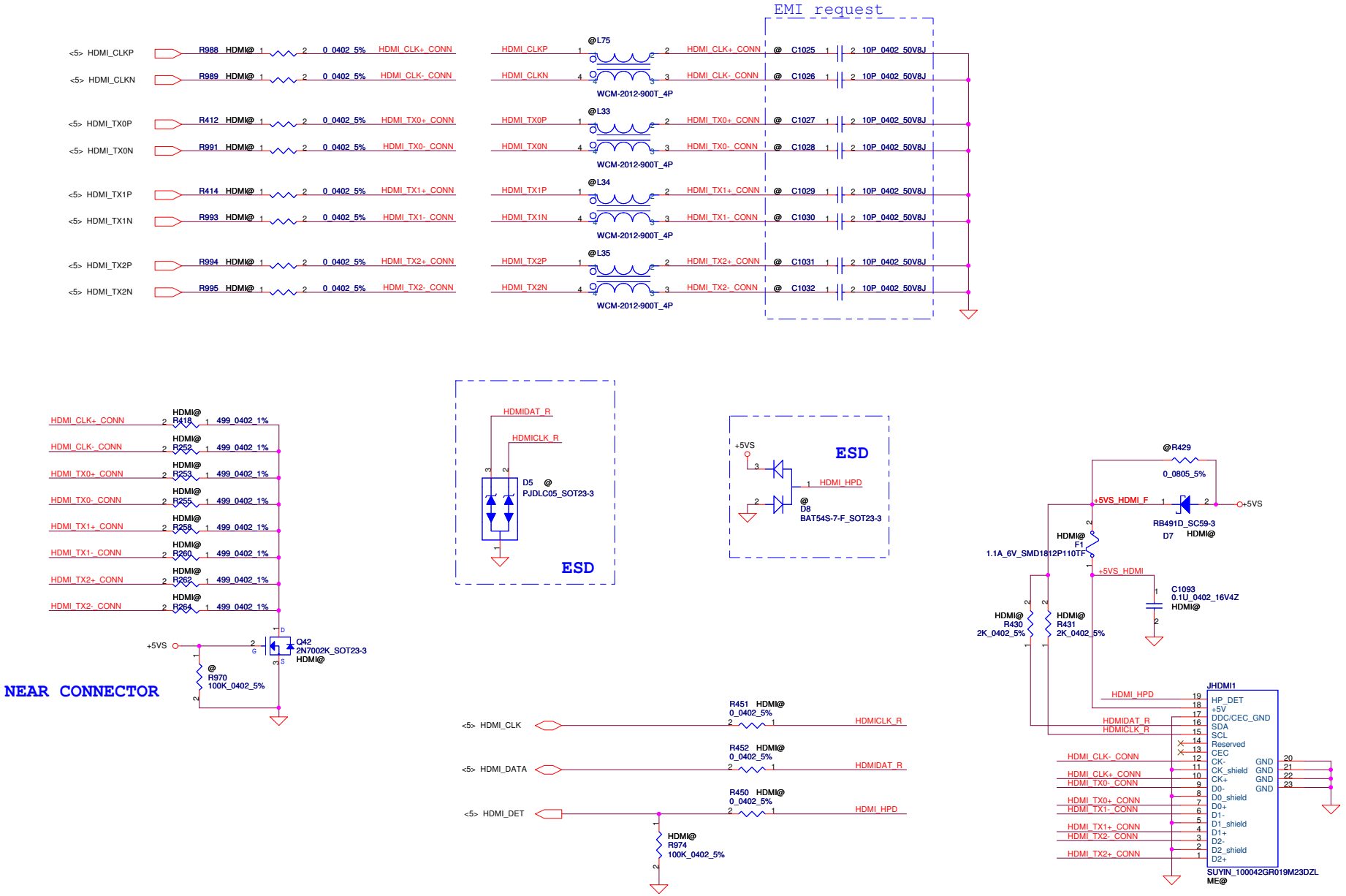

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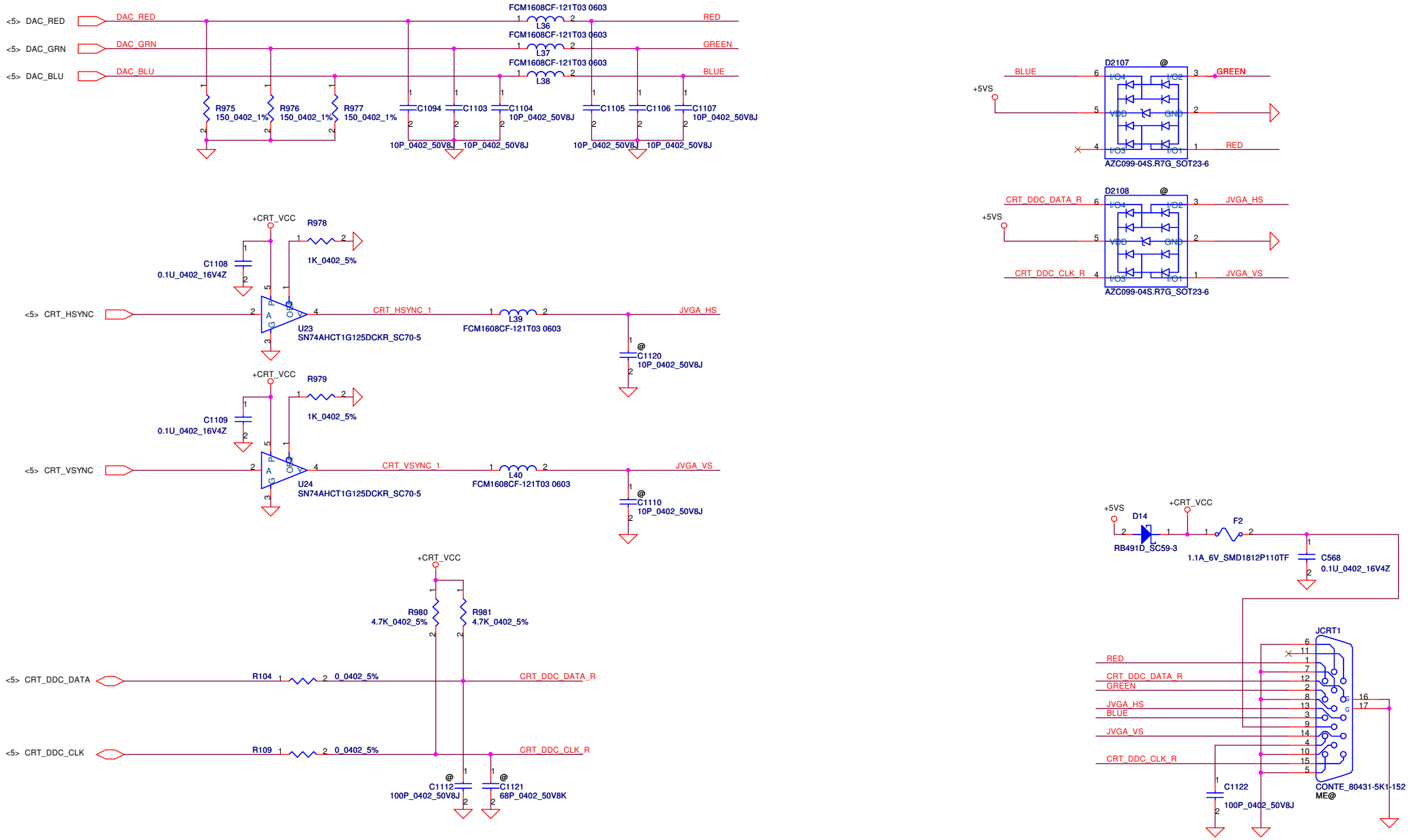
Compal Electronics, Inc.

Title: HDMI Connector

Size: Custom | Document Number: LA8681P | Rev: 0.1

Date: Wednesday, November 30, 2011 | Sheet 23 of 48



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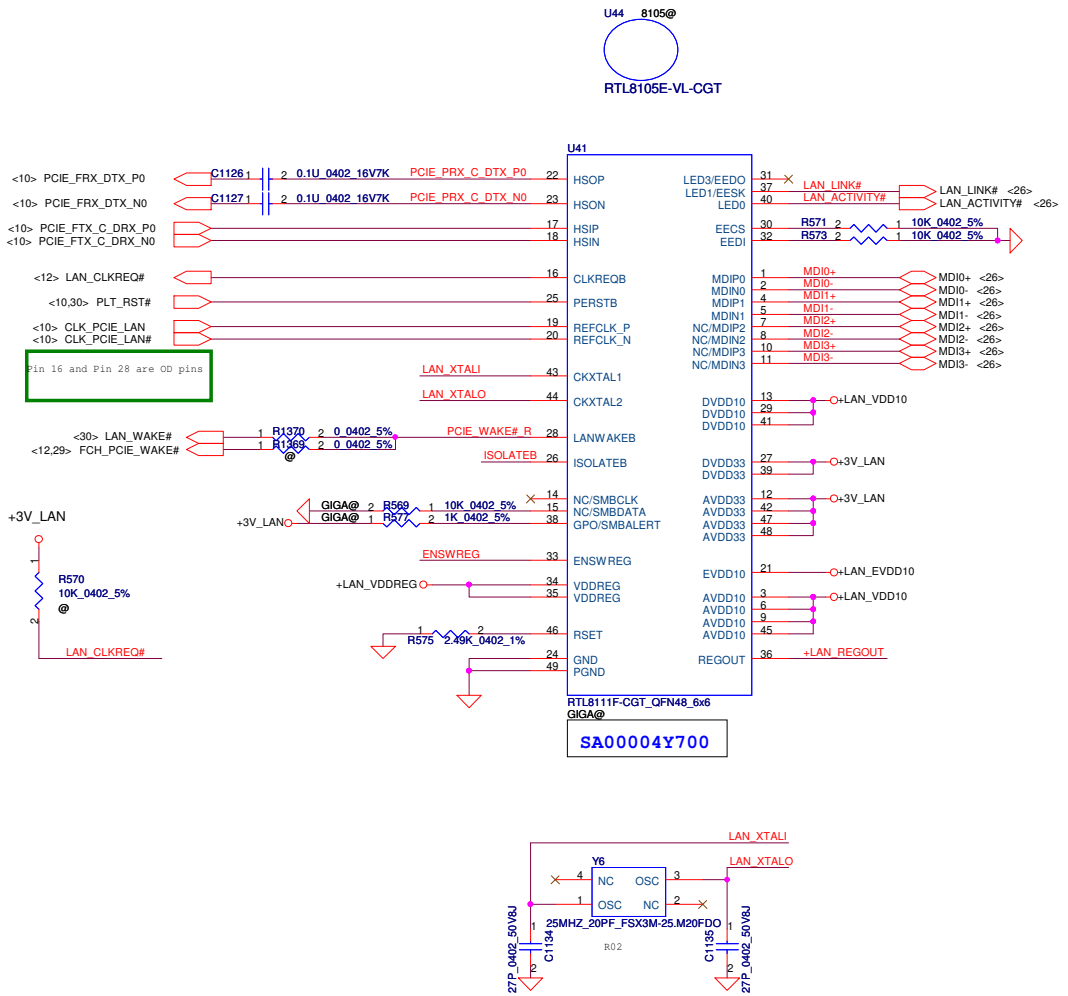
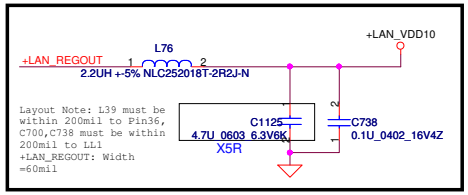
Compal Electronics, Inc.

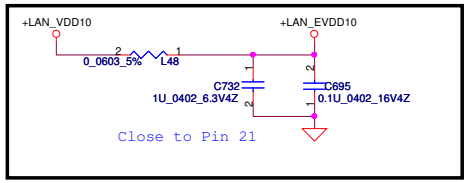
Title: CRT Connector

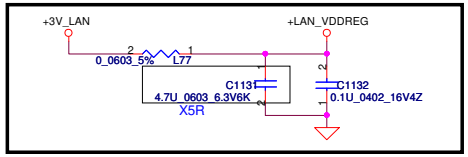
Size: Custom | Document Number: LA8681P | Rev: 0.1

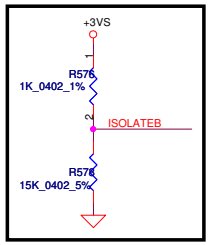
Date: Wednesday, November 30, 2011 | Sheet 24 of 48

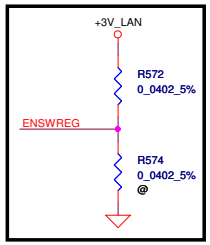




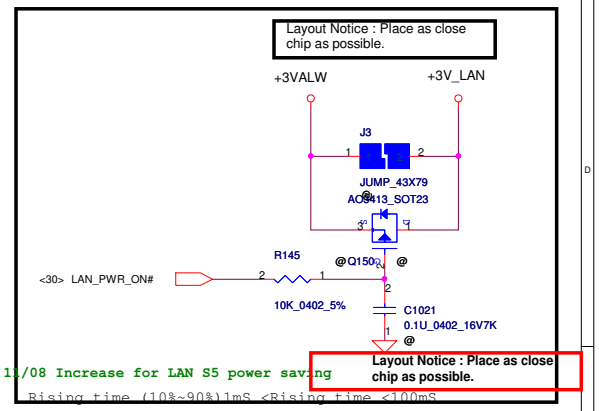






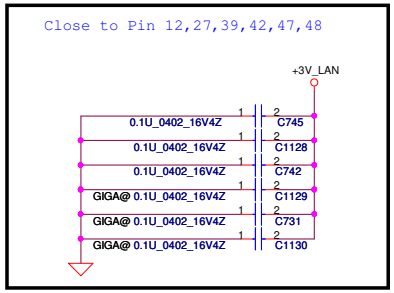


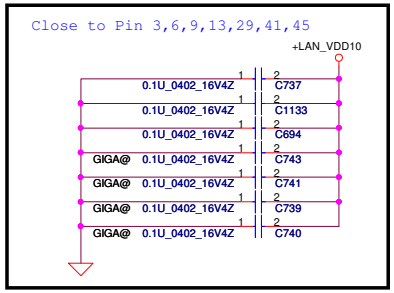
H: Enable internal Regular
L: Disable



11/08 Increase for LAN S5 power saving

Rising time (10%~90%)1mS <Rising time <100mS





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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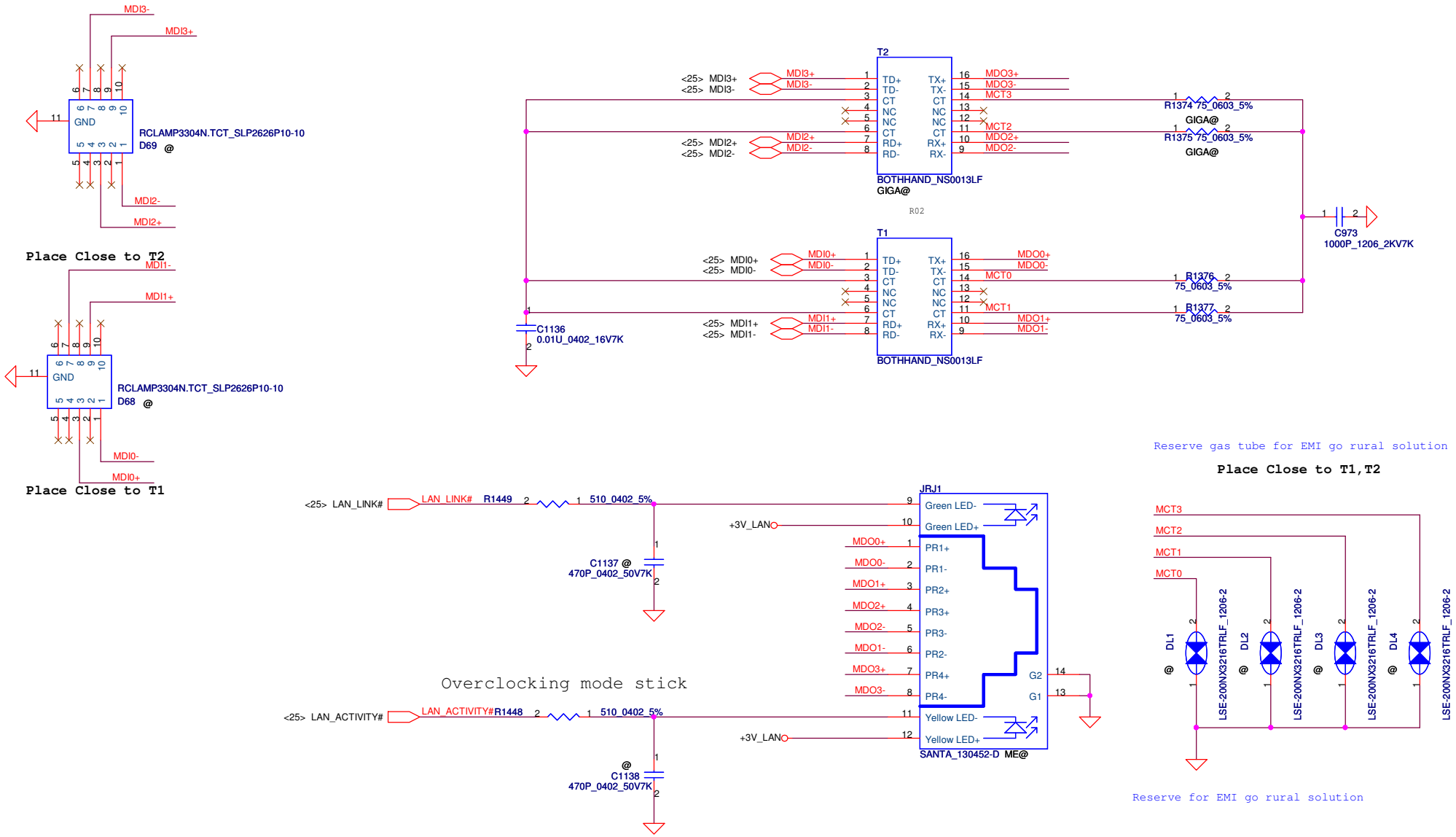
Compal Electronics, Inc.

Title: LAN-RTL8111F/8105E

Size: Custom | Document Number: LA-7984P | Rev: 0.1

Date: Wednesday, November 30, 2011 | Sheet 25 of 48



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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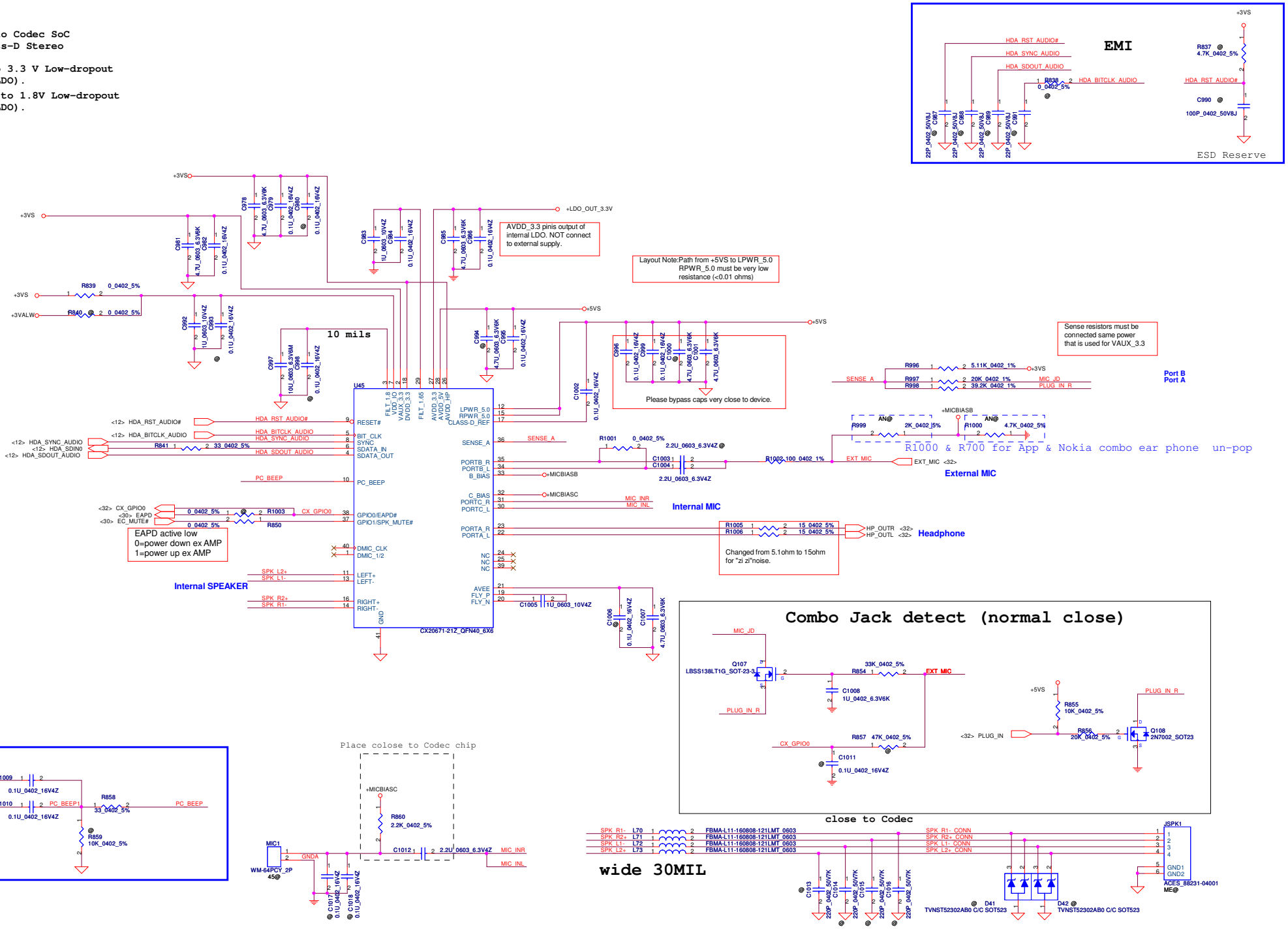
Compal Electronics, Inc.

Title: LAN_Transformer

Size: B | Document Number: LA-7984P | Rev: 0.1

Date: Wednesday, November 30, 2011 | Sheet 26 of 48

CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

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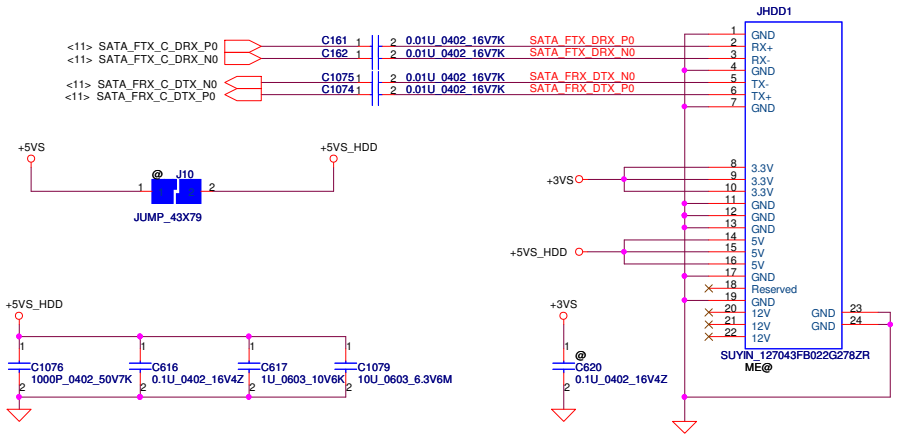
Compal Electronics, Inc.

Title: CX20671 Codec

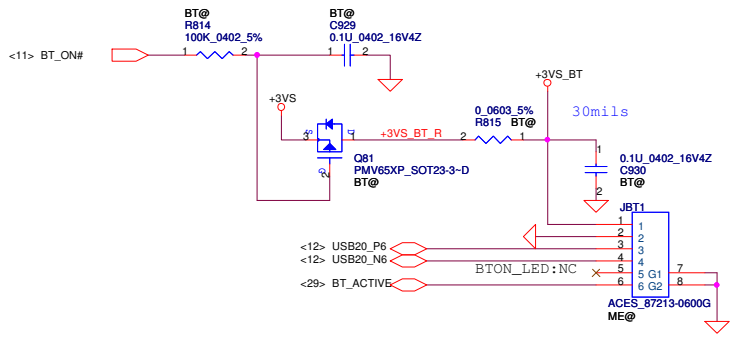
Size: Custom | Document Number: LA8681P | Rev: 0.1

Date: Wednesday, November 30, 2011 | Sheet 27 of 48

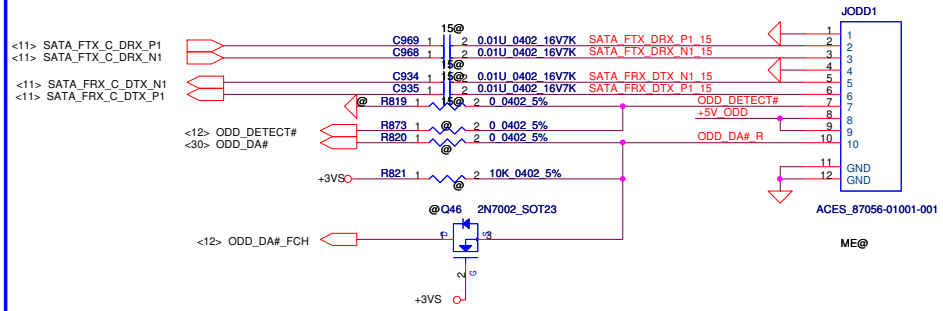
HDD CONN

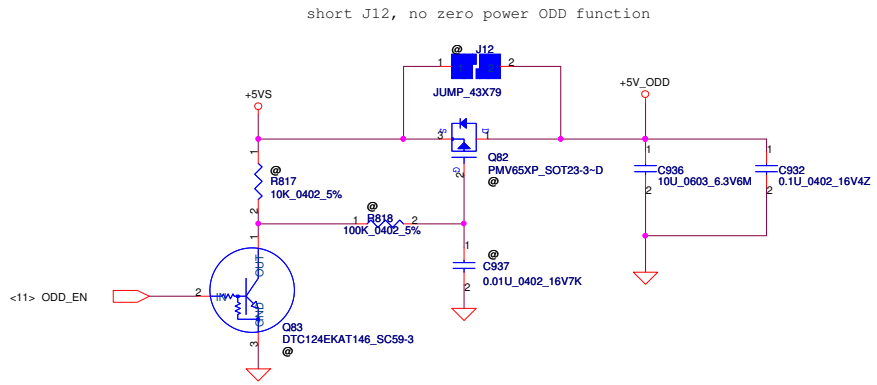


BT MODULE CONN

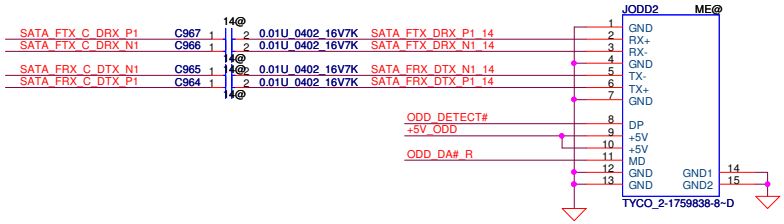


ODD CONN 15"





ODD CONN 14"



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

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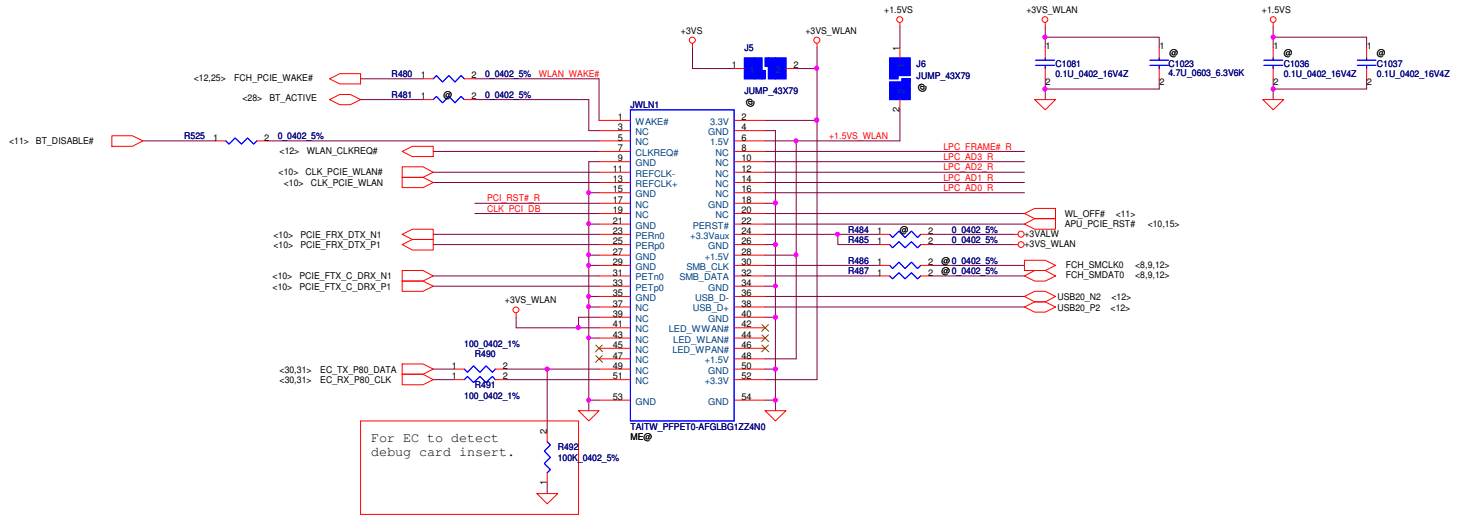
Compal Electronics, Inc.

Title: HDD/ODD/BT

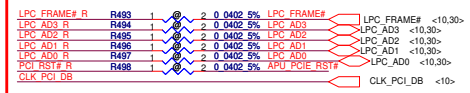
Size: B | Document Number: LA8681P | Rev: 0.1

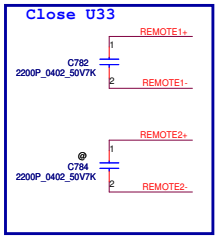
Date: Wednesday, November 30, 2011 | Sheet 28 of 48

Mini-Express Card for WLAN/WiMAX(Half)

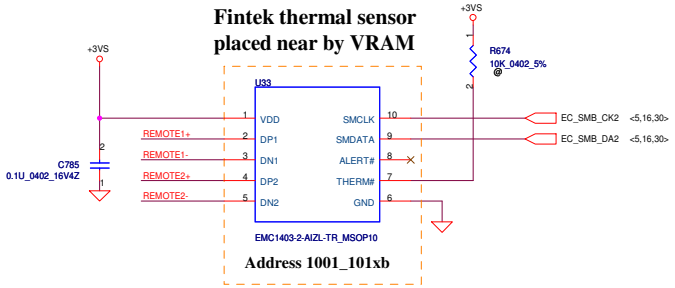


Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

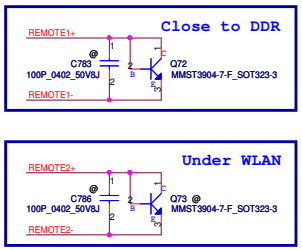




Fintek thermal sensor placed near by VRAM



Change from SA000029210 to SA000046C00 for main source



REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/10/12	Deciphered Date	2013/10/12	Title: Mini PCIE/Thermal IC
				Size: Document Number: LA8681P Rev: 0.1
				Date: Wednesday, November 30, 2011 Sheet 29 of 48

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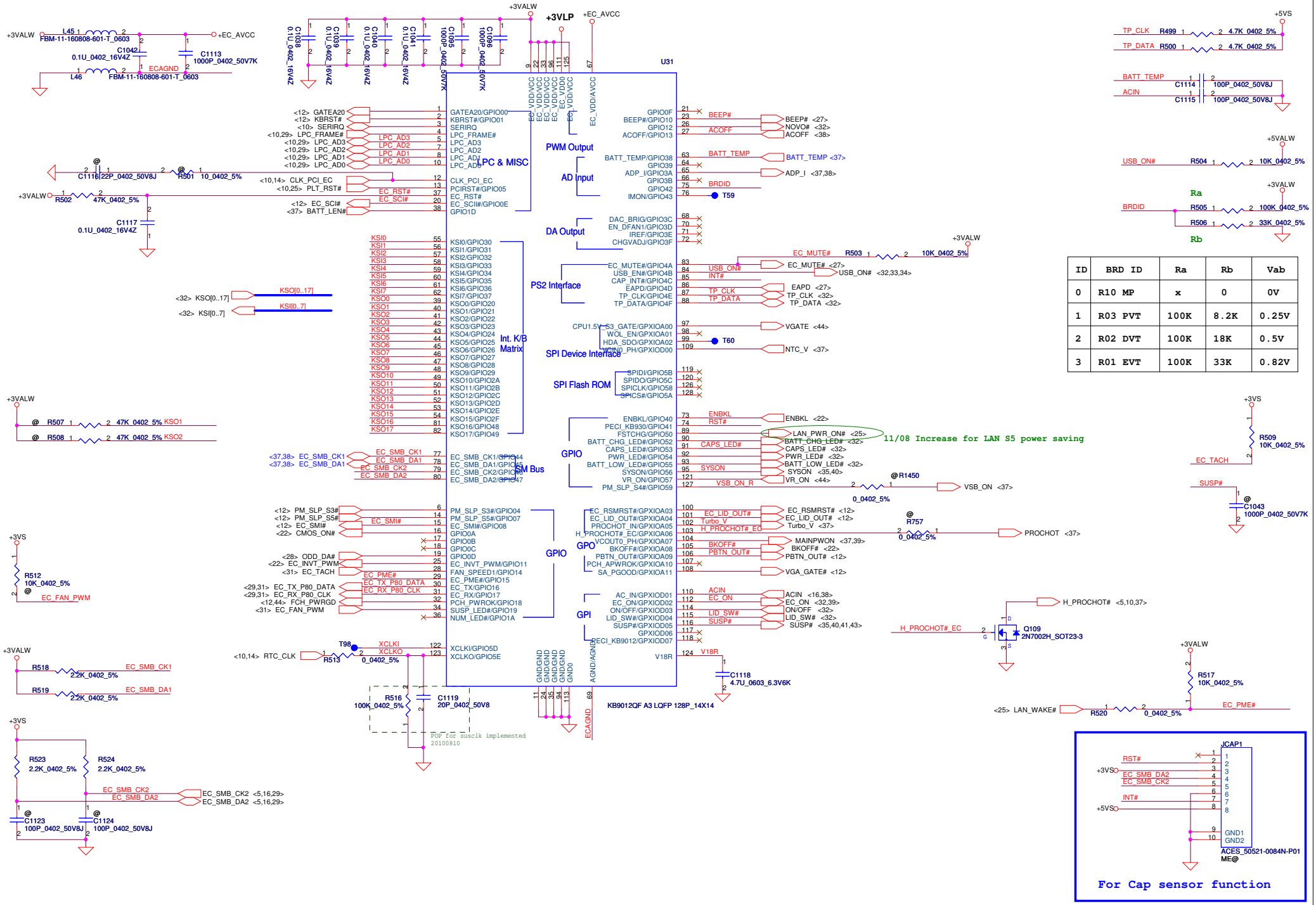

ID	BRD ID	Ra	Rb	Vab
0	R10 MP	x	0	0V
1	R03 PVT	100K	8.2K	0.25V
2	R02 DVT	100K	18K	0.5V
3	R01 EVT	100K	33K	0.82V

Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

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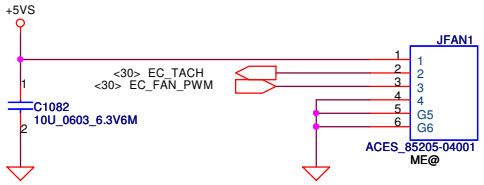
Compal Electronics, Inc.

Title: KB9012/Cap sensor

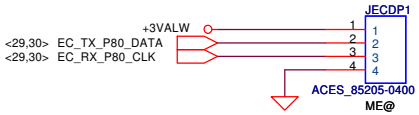
Size: Custom | Document Number: LA8681P | Rev: 0.1

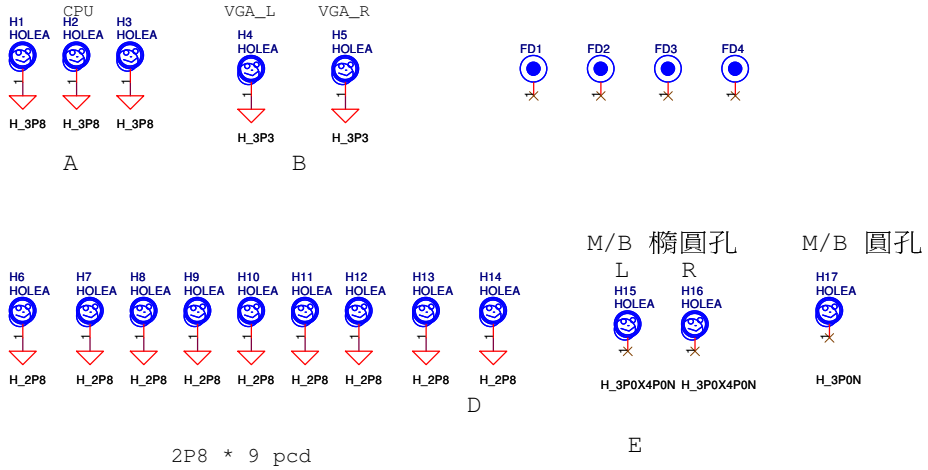
Date: Wednesday, November 30, 2011 | Sheet 30 of 48

FAN CONN



EC DEBUG PORT





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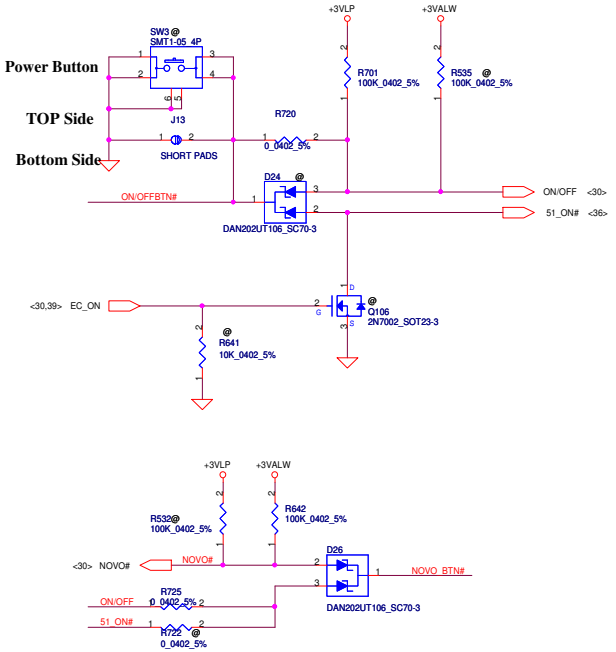
Compal Electronics, Inc.

Title: FAN/SCREW/EC Debug

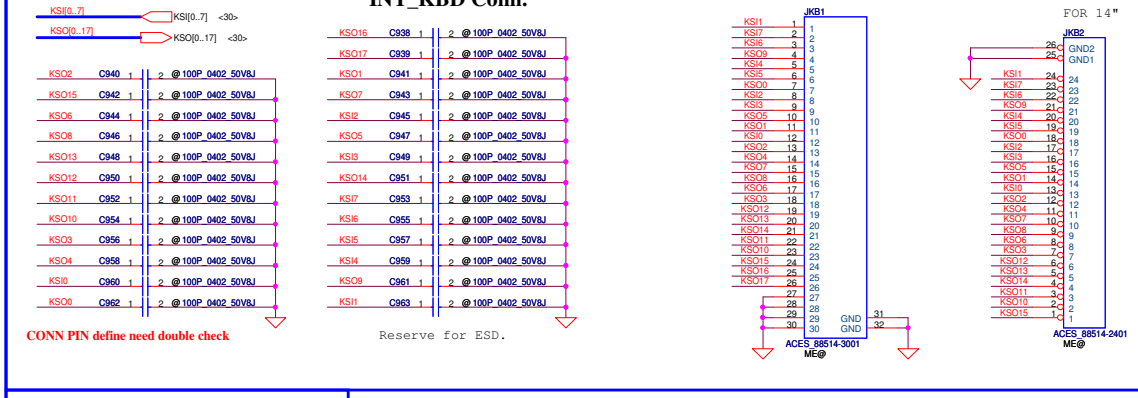
Size: B | Document Number: LA8681P | Rev: 0.1

Date: Wednesday, November 30, 2011 | Sheet 31 of 48

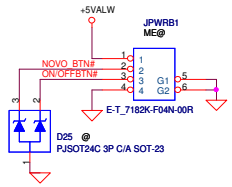
ON/OFF switch



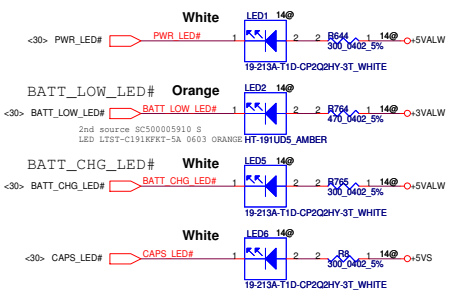
INT_KBD Conn.



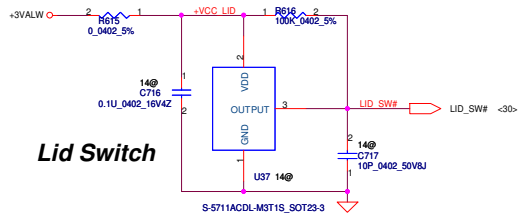
Power Button Board Conn. 8pin



FOR 14"



Lid Switch



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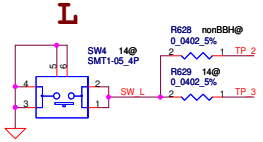
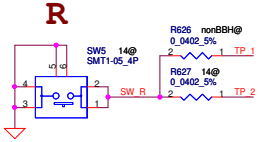
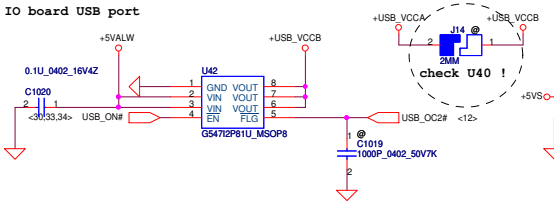


R

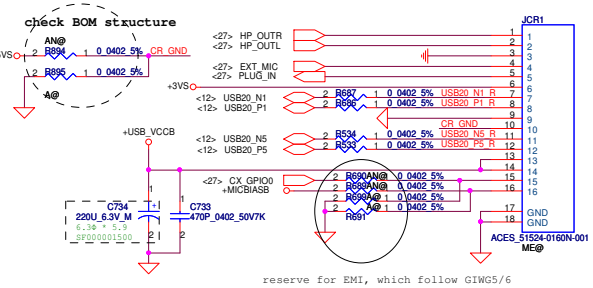


IO board USB port



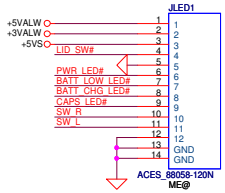
EMI request

Card Reader/Audio Jack SB CONN



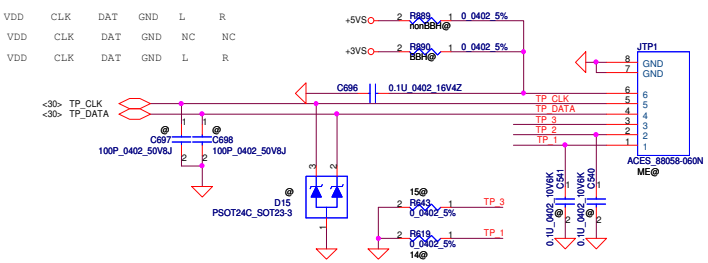
FOR 15"

LED B/D Conn



To TP/B Conn.

pin	6	5	4	3	2	1
14	VDD	CLK	DAT	L	R	GND
15	VDD	CLK	DAT	GND	L	R
BB-H	VDD	CLK	DAT	GND	NC	NC
BB-L	VDD	CLK	DAT	GND	L	R



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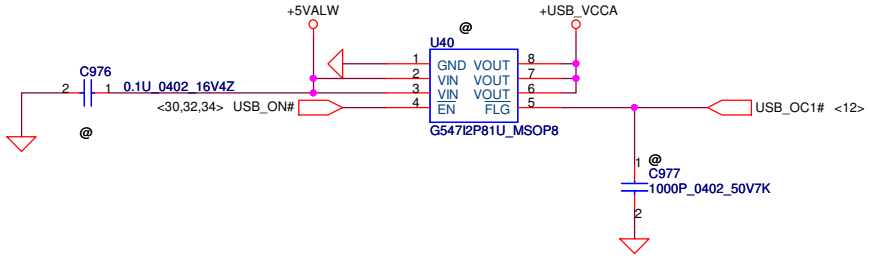
Compal Electronics, Inc.

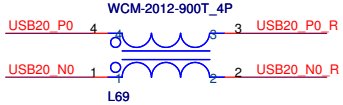
Title: KBD/PWR/CR/LED/TP Conn.

Size: C | Document Number: LA8681P | Rev: 0.1

Date: Wednesday, November 30, 2011 | Sheet 32 of 48

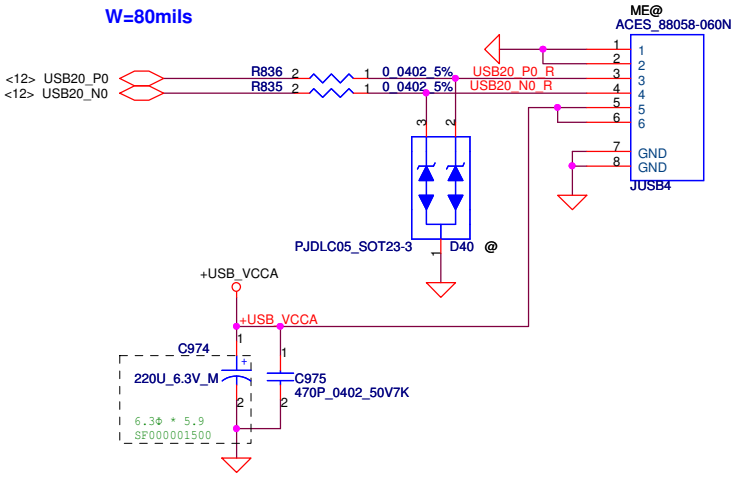


Right Ext.USB FFC Conn.



Update to SM070001S00 for EMI request

W=80mils



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Issued Date	2011/10/12	Deciphered Date	2013/10/12

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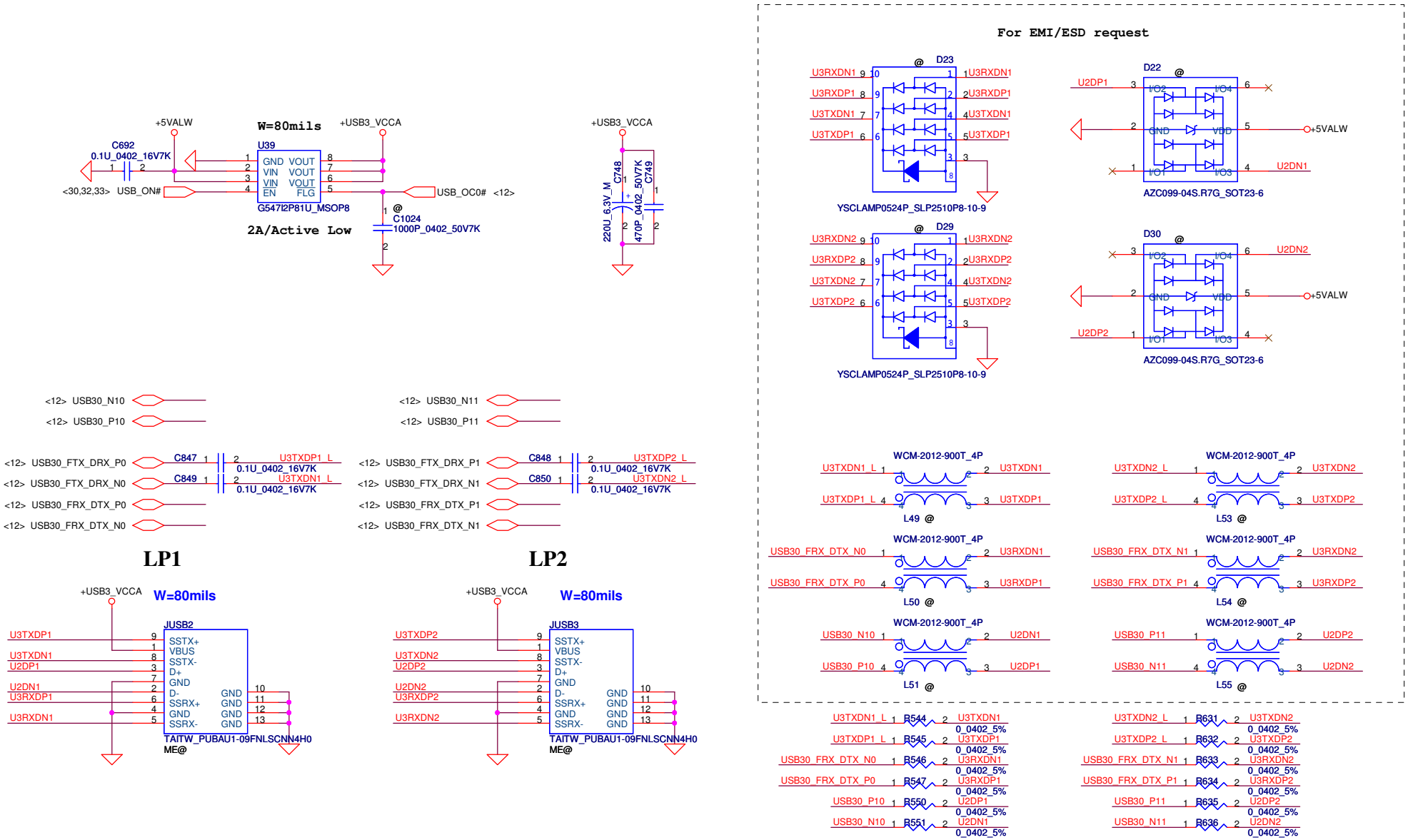
Compal Electronics, Inc.

Title: USB cable port

Size: B | Document Number: LA8681P | Rev: 0.1

Date: Wednesday, November 30, 2011 | Sheet 33 of 48



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

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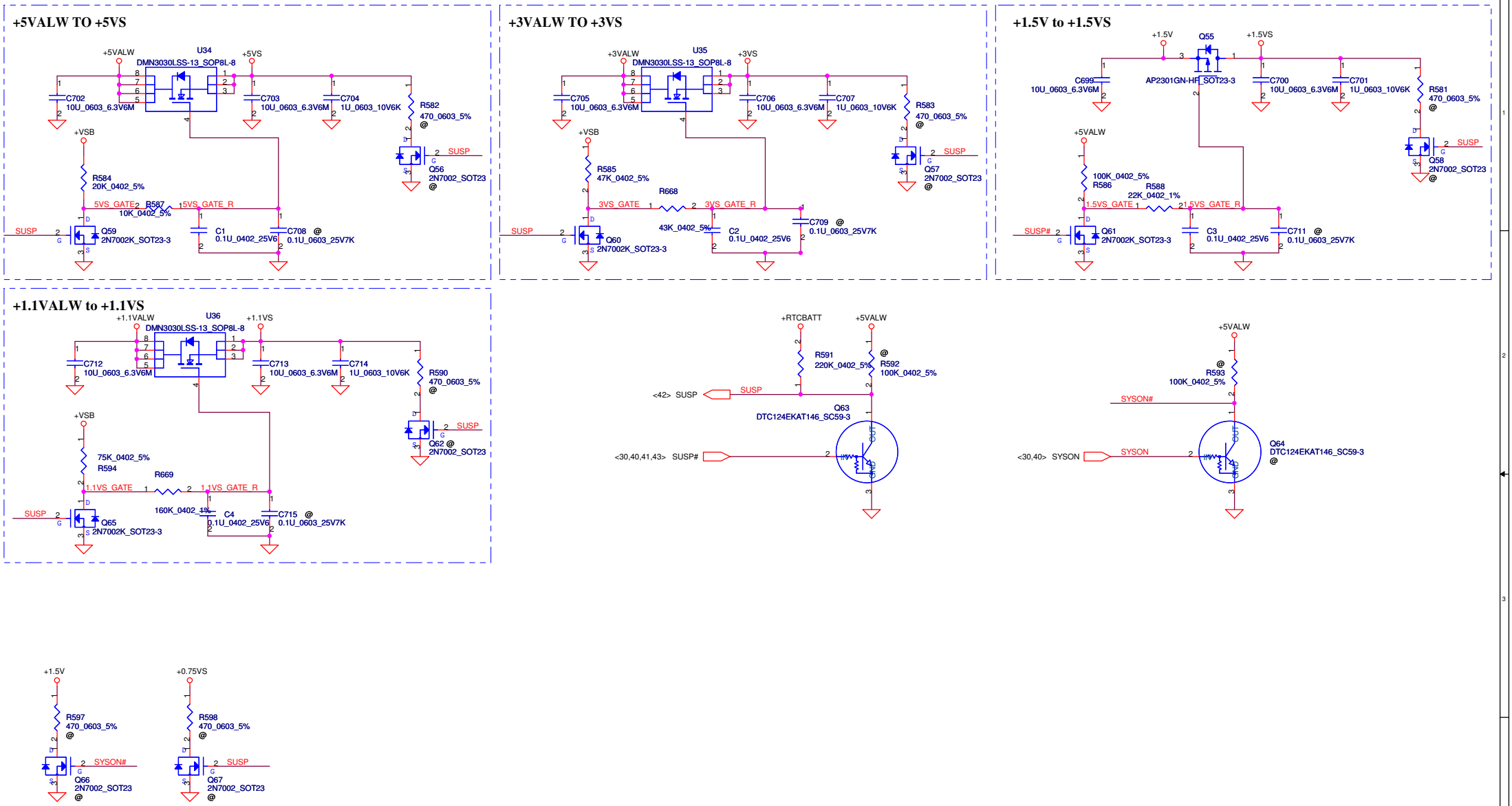
Compal Electronics, Inc.

Title: Left USB3.0

Size: B | Document Number: LA8681P | Rev: 0.1

Date: Wednesday, November 30, 2011 | Sheet 34 of 48



Security Classification	Compal Secret Data		
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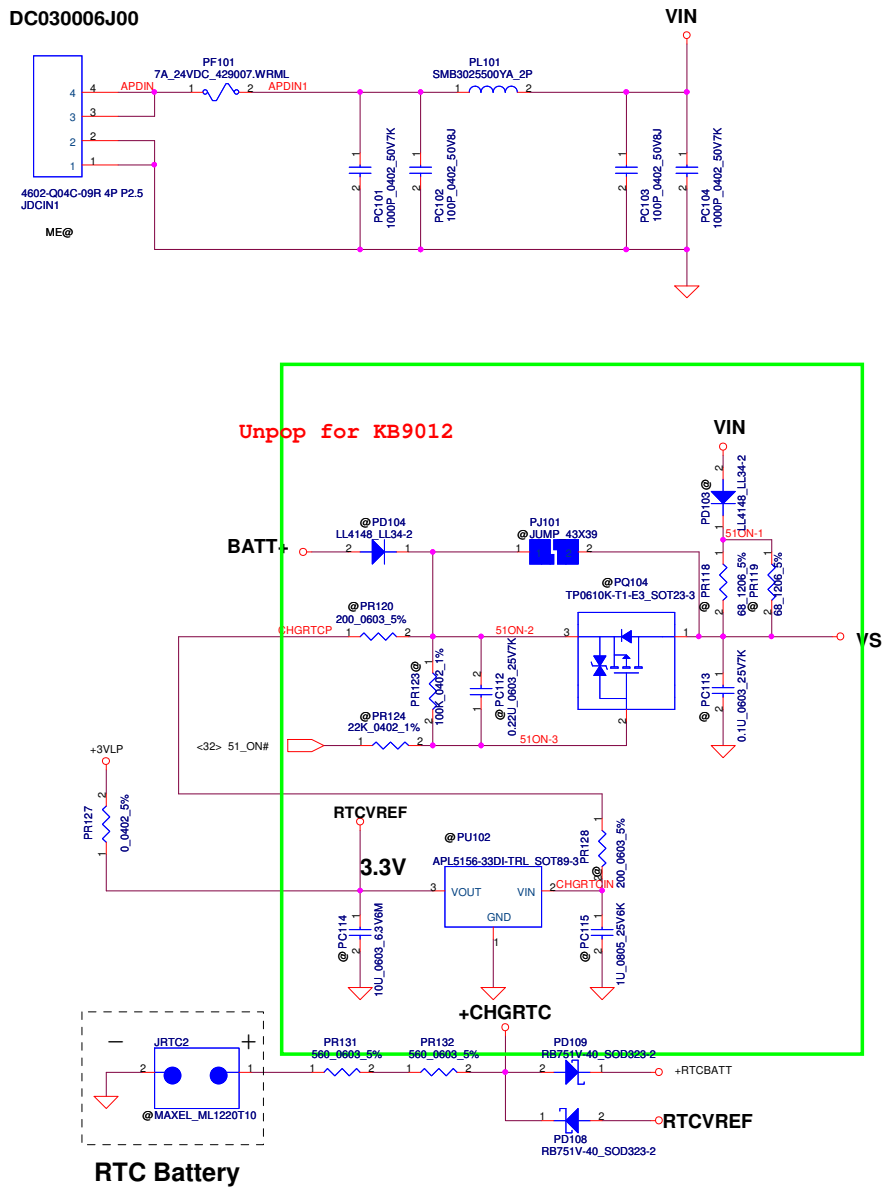
Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: LA8681P | Rev: 0.1

Date: Wednesday, November 30, 2011 | Sheet 35 of 48



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/10/12	Deciphered Date	2013/10/12	Title: PWR DCIN
				Size: Custom; Document Number; Rev 0.1
				Date: Wednesday, November 30, 2011; Sheet 36 of 48

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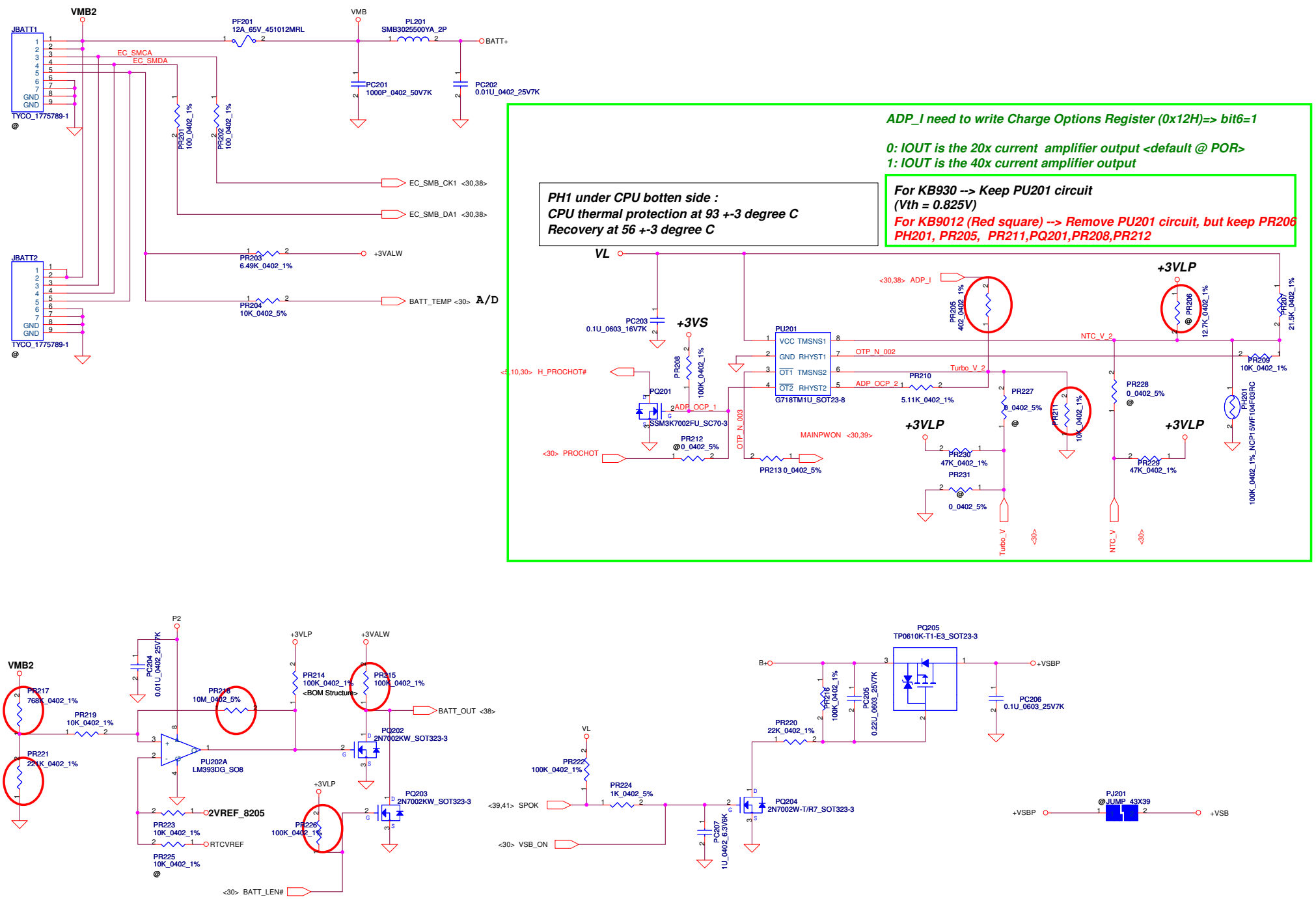

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Issued Date	2011/10/12	Deciphered Date	2013/10/12

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Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

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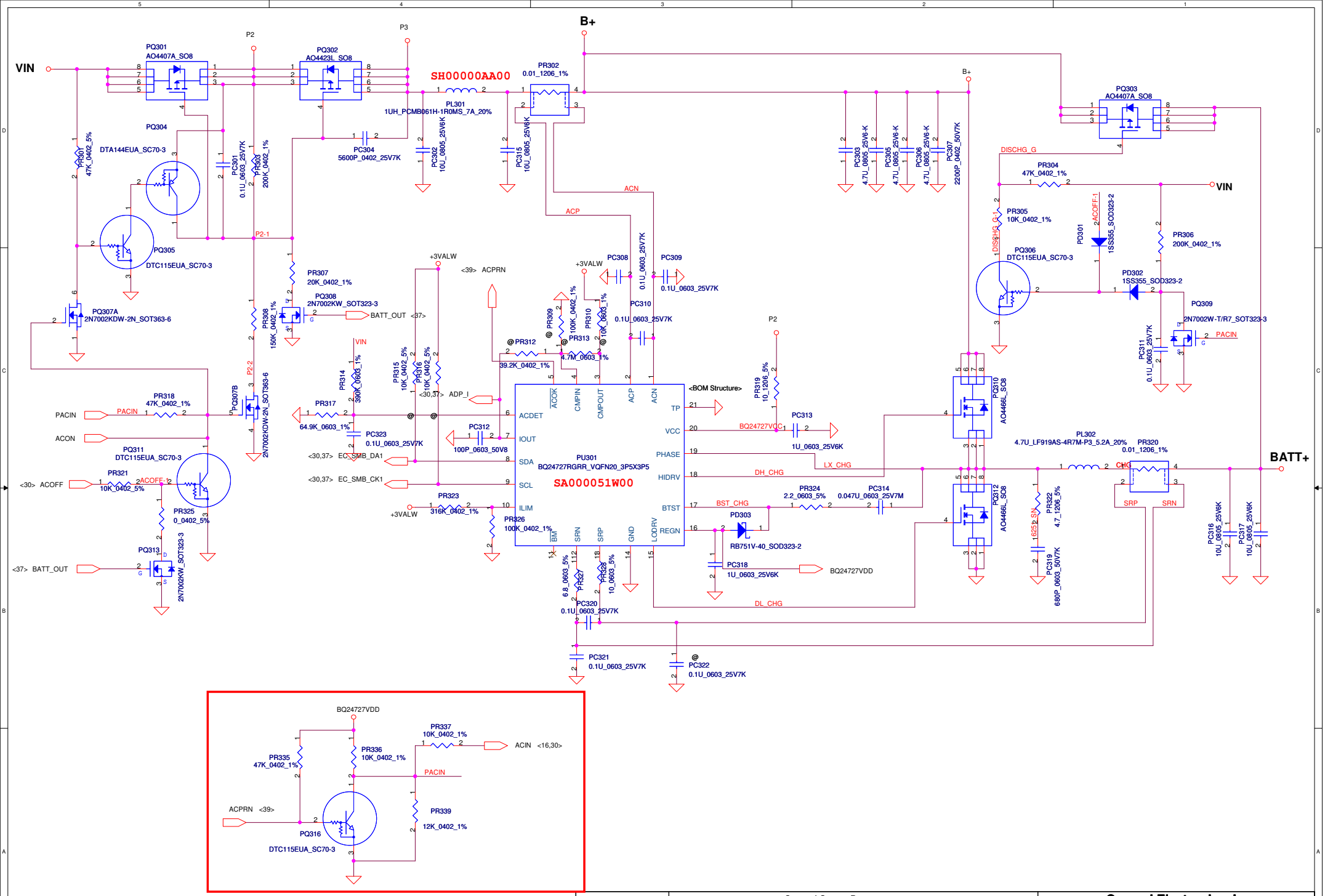

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Issued Date	2011/10/12	Deciphered Date	2013/10/12

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Compal Electronics, Inc.

Title: **CHARGER**

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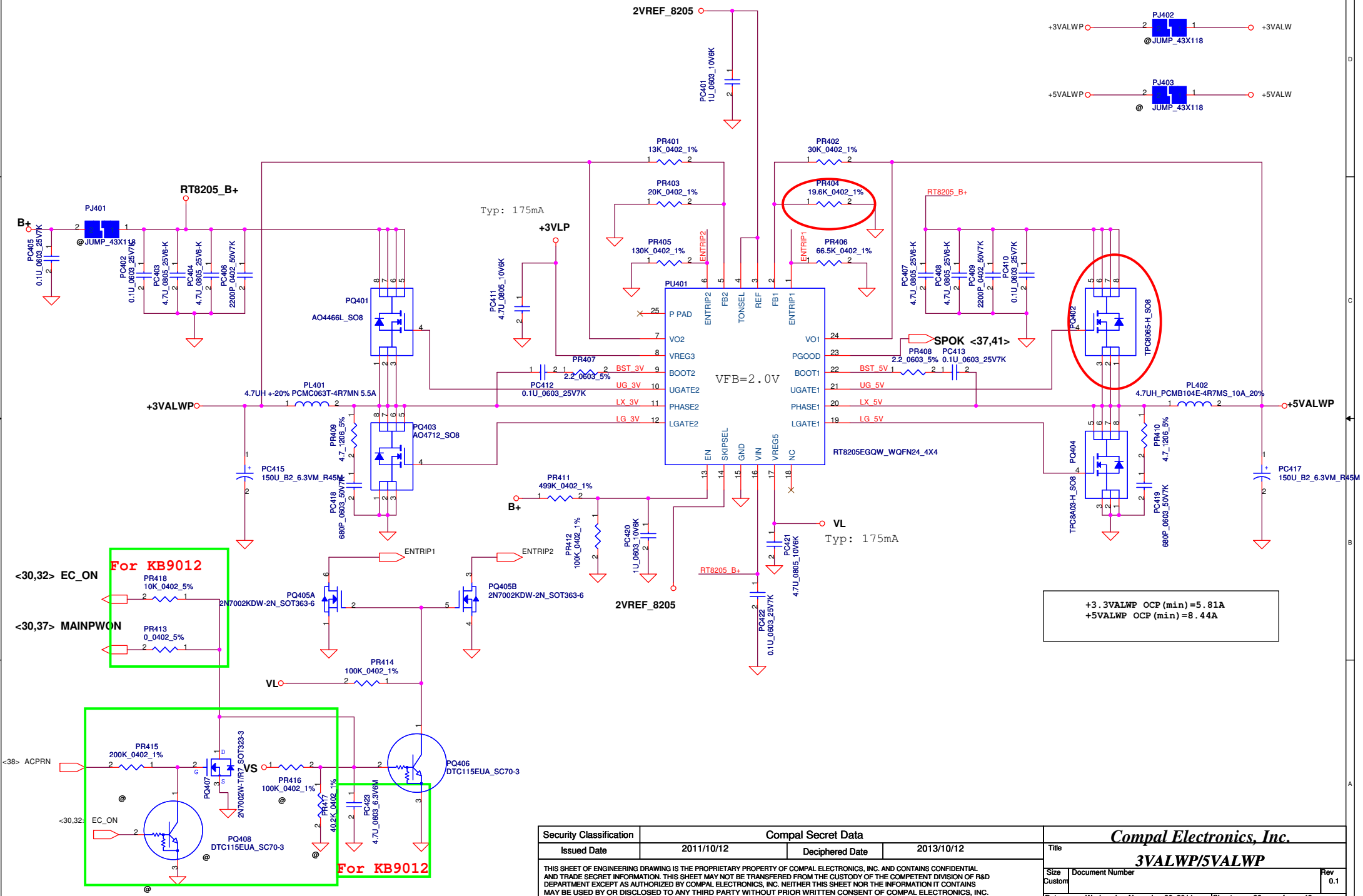
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



Security Classification	Compal Secret Data		
Issued Date	2011/10/12	Deciphered Date	2013/10/12

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Compal Electronics, Inc.

Title: **3VALWP/5VALWP**

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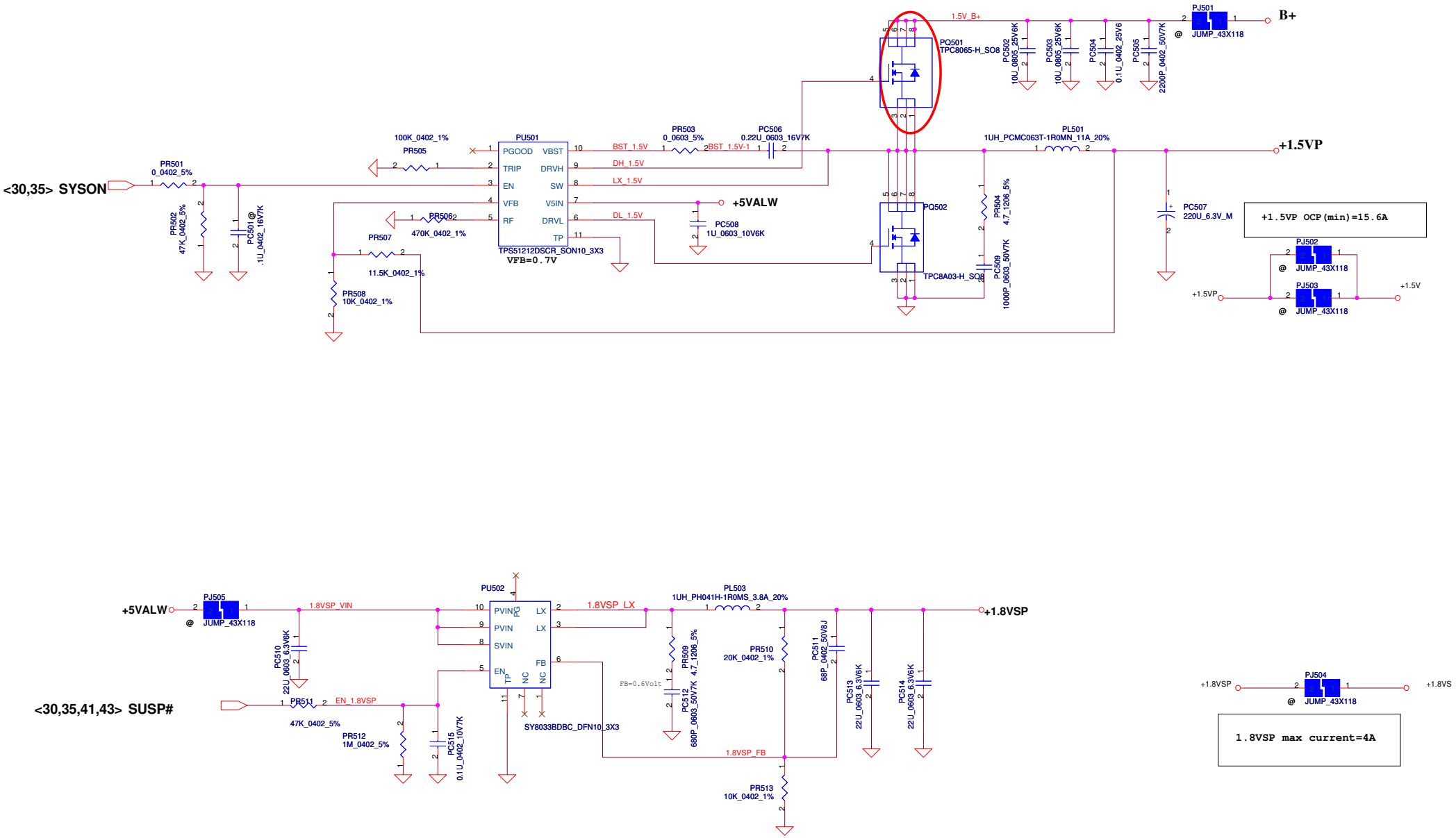

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Issued Date	2011/10/12	Deciphered Date	2013/10/12

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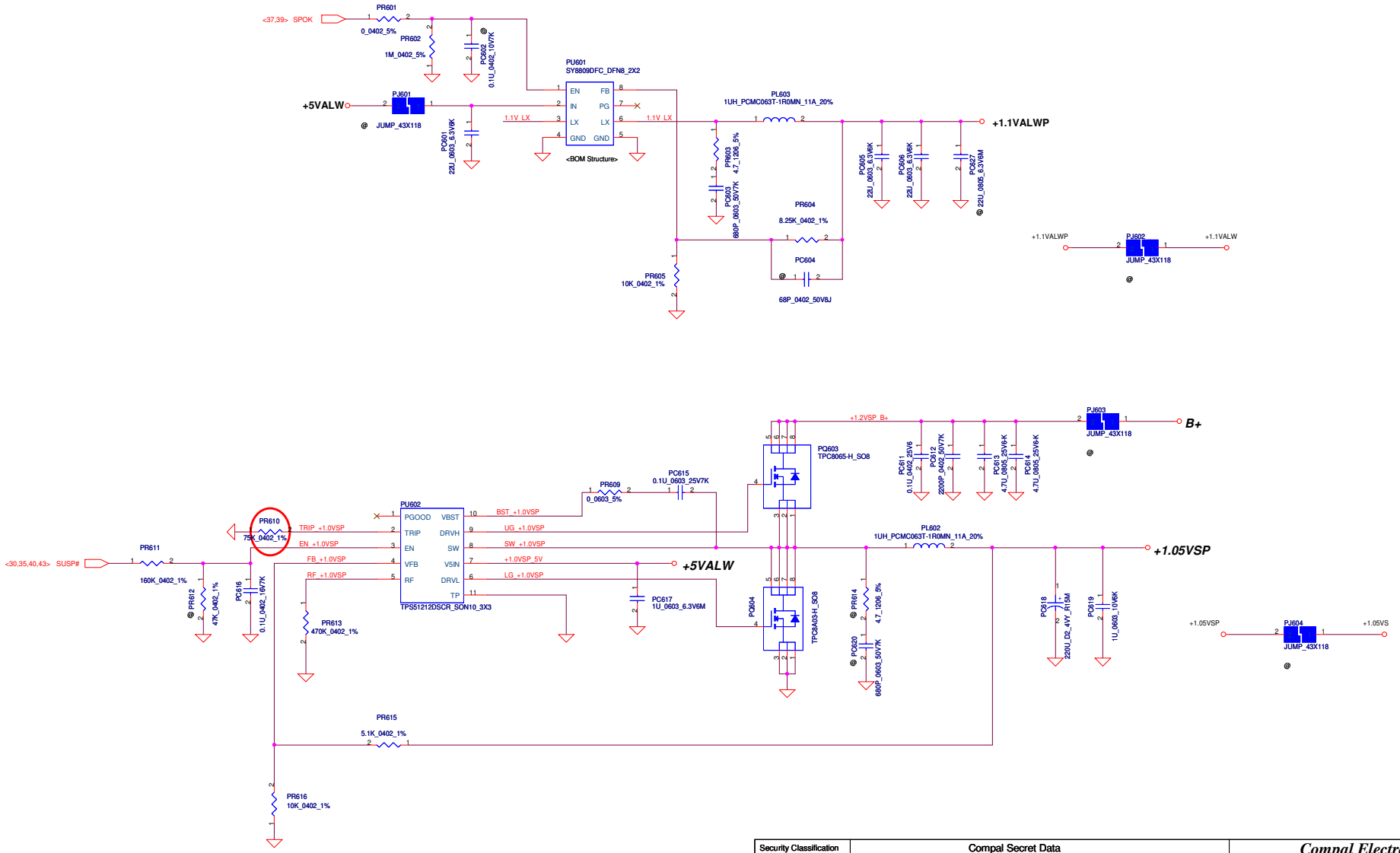
Compal Electronics, Inc.

Title: **PWR-+1.5VP/+1.8VSP**

Size: Custom | Document Number | Rev: 0.1

Date: Wednesday, November 30, 2011 | Sheet 40 of 48



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Issued Date	2011/10/12	Deciphered Date	2013/10/12

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Compal Electronics, Inc.

Title: PWR +1.1VALWP/+1.0VSP

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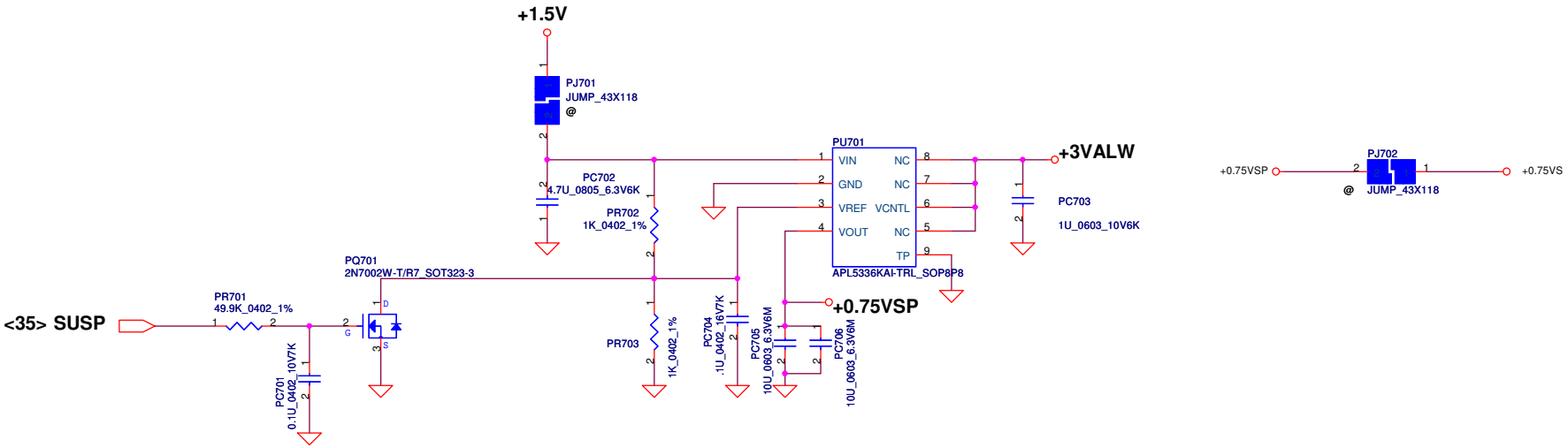

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Issued Date	2011/10/12	Deciphered Date	2013/10/12

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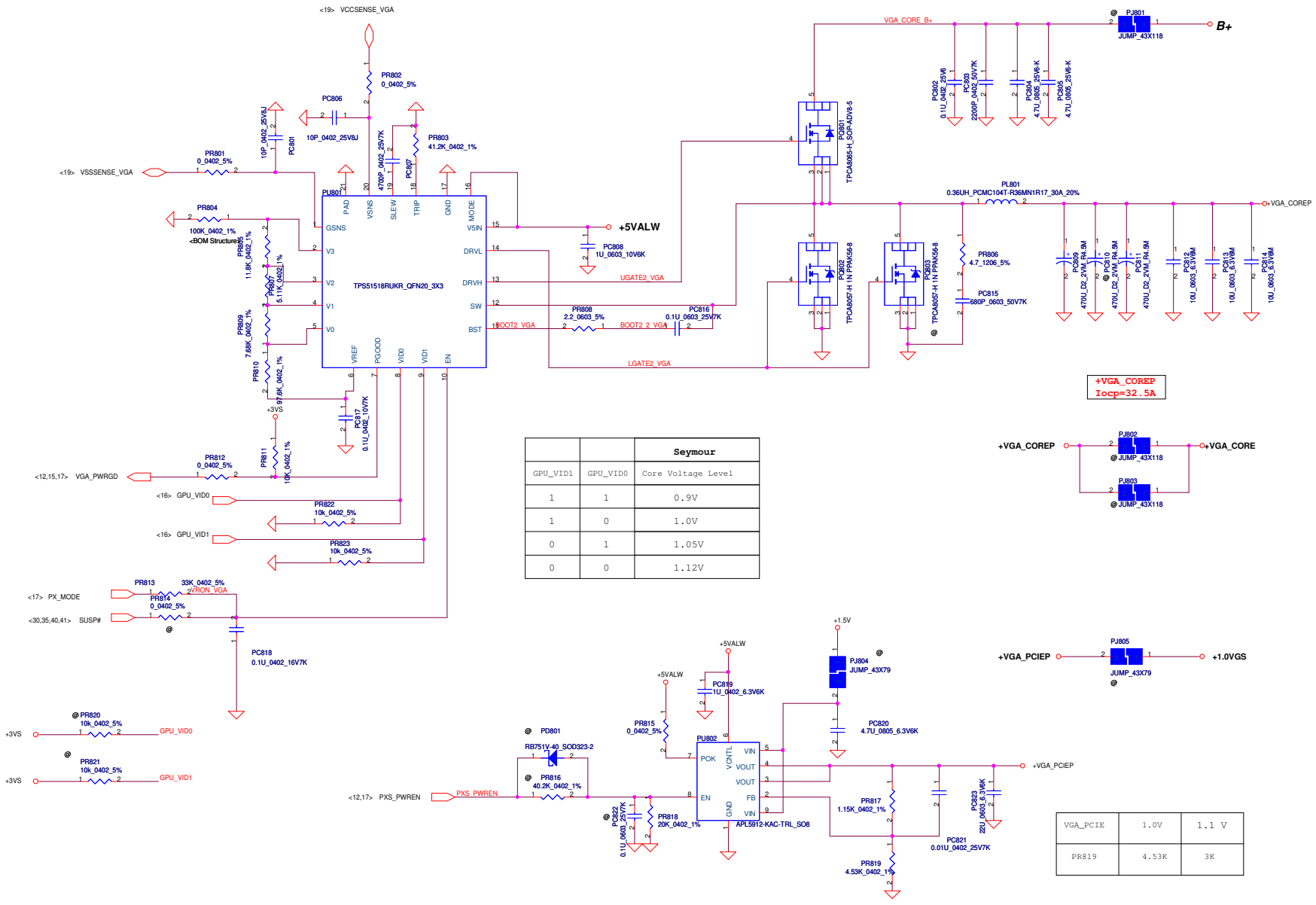
Compal Electronics, Inc.

Title: **PWR +0.75VSP**

Size: Custom | Document Number | Rev: 0.1

Date: Wednesday, November 30, 2011 | Sheet 42 of 48



		Seymour
GPU_VID1	GPU_VID0	Core Voltage Level
1	1	0.9V
1	0	1.0V
0	1	1.05V
0	0	1.12V

VGA_PCIE	1.0V	1.1 V
PR819	4.53K	3K

Security Classification: Compal Secret Data
Issued Date: 2011/10/12 Deciphered Date: 2013/10/12

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Compal Electronics, Inc.

Title: PWR-VGA_CORE/VGA_PCIE

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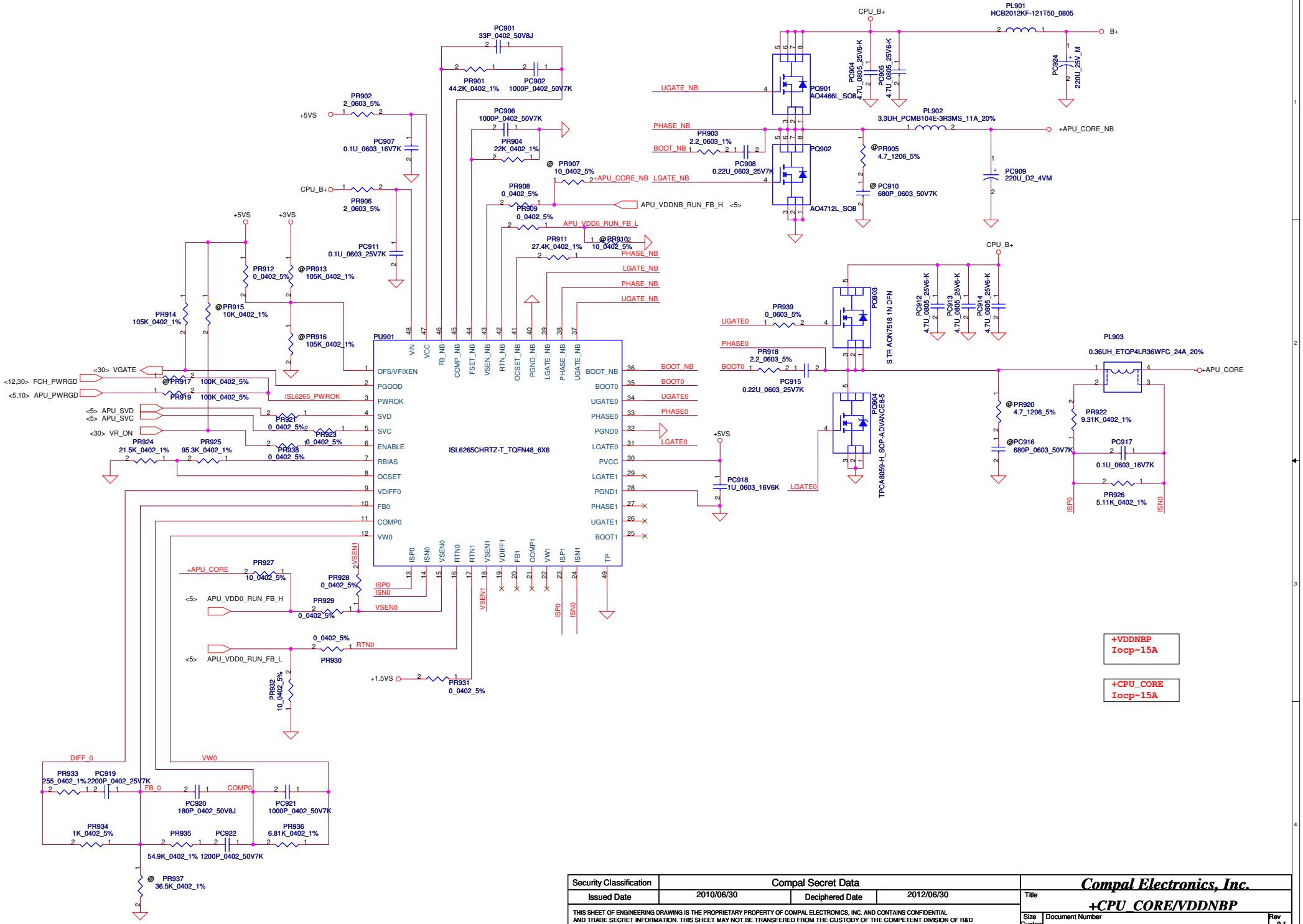

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **+CPU_CORE/VDDNBP**

Size: Custom | Document Number | Rev 0.1

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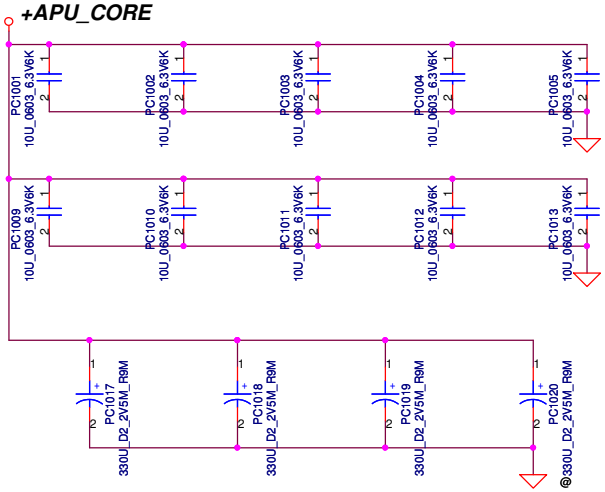
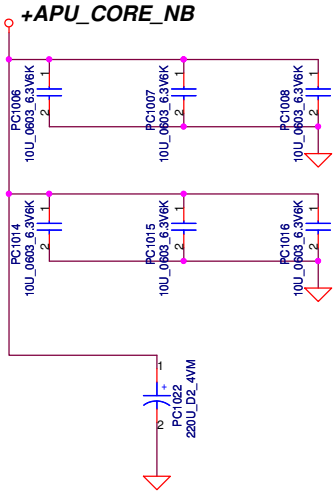
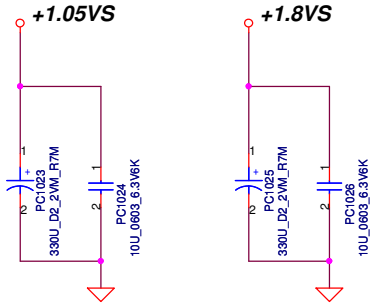
+CPU_CORE



+CPU_CORE_NB





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Issued Date	2011/10/12	Deciphered Date	2013/10/12

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Compal Electronics, Inc.

Title: **PWR - PROCESSOR DECOUPLING**

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	(CPU CORE/VDDNBP)...VR_ON增加PR938				
2	0402 0 歐姆				
3	APU_CORE_NB....PC1021拿掉				
4					
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16					
17					

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Issued Date	2011/10/12	Deciphered Date	2013/10/12

Compal Electronics, Inc.

Title: **PIR (PWR)**

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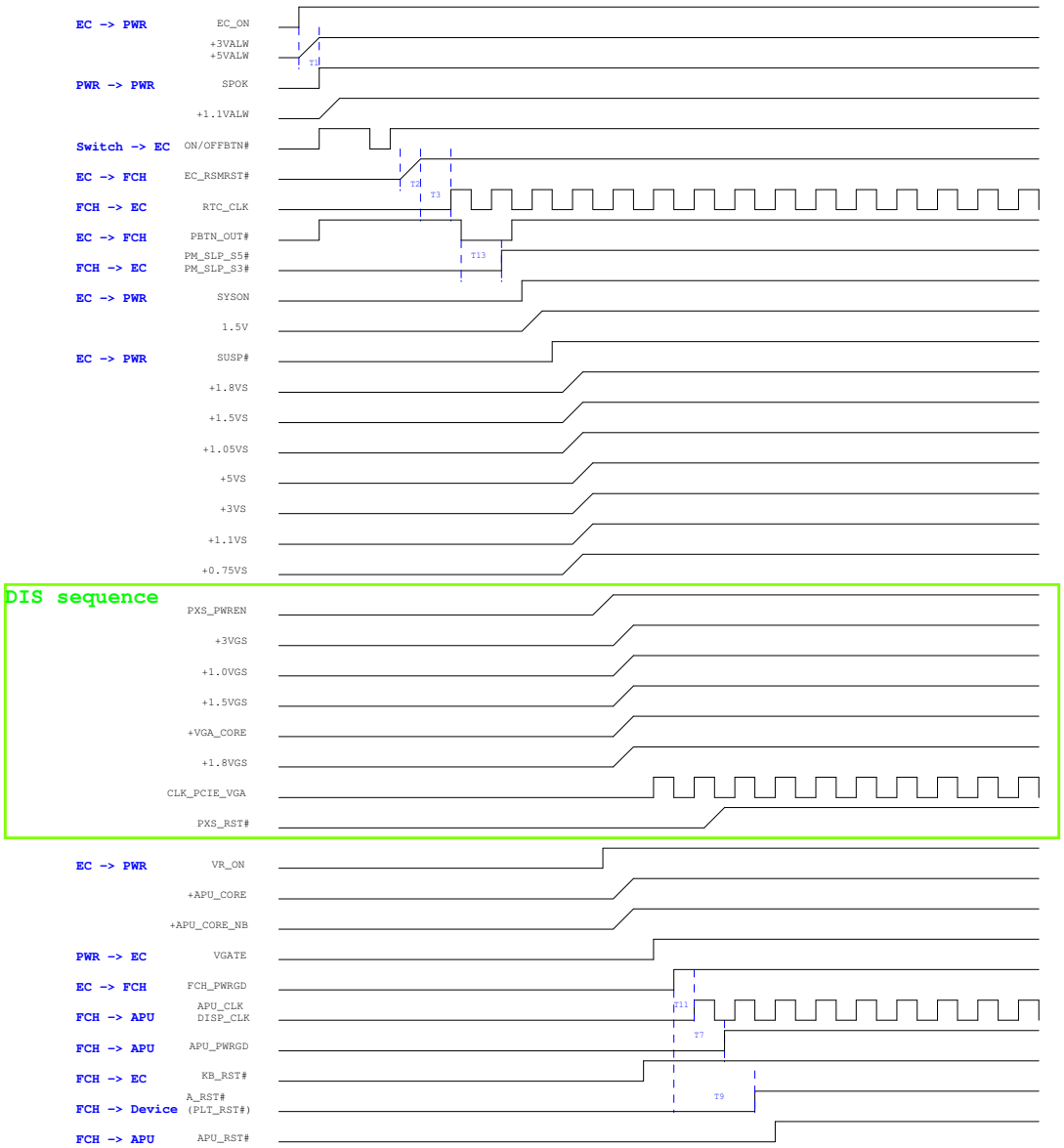
QAWGE Power Sequence (AC mode)



1ms< T1 < 100ms : +3VALW rising time, for LAN chip request
+3VALW need rampe up before +1.1VALW or at the same time.

T2 < 50ms : EC_RSMRST# rising time
+3VALW need rampe up before EC_RSMRST# de-assertion at least 10ms
+1.1VALW need rampe up before EC_RSMRST# de-assertion
T3 > 16ms : EC_RSMRST# de-assert to start RTCCLK

T13 > 200ns : PBTN_OUT# to SLP_S3#/S5# de-assertion

+3VS need rampe up before +1.1VS or at the same time.

The time delay between PXS_PWREN assertion
and PXS_RST# de-assertion must be more than 100ms.

CLK_PCIE_VGA should be 100us earlier than PXS_RST# de-assert.

T11< 32ms : FCH_POK assertion to clock out

98ms< T7< 150ms : FCH_POK assertion to APU_PWRGD

KB_RST# should be de-asserted before FCH_POK

101ms< T9< 113ms :
FCH_POK assertion to A_RST# de-assertion

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Issued Date	2011/10/12	Deciphered Date	2013/10/12

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Compal Electronics, Inc.

Title: PWR - PROCESSOR DECOUPLING

Size | Document Number | Rev 0.1

Date: Tuesday, November 29, 2011 | Sheet 47 of 47