| ZZZ1 | ZZZ2 | ZZZ3 | ZZZ4 | ZZZ5 | ZZZ6 |
|---|---|---|---|---|---|
| PCB<br>DAZ@ | LA-8501P<br>MB@ | LS-8501P<br>DA2@ | LS-8502P<br>DA2@ | LS-8503P<br>DA2@ | LS-8504P<br>DA2@ |

# Compal Confidential

## QLA13/15 LA8501P Schematics Document

### AMD Trinity APU with DDRIII + FCH Hudson D3

### AIO M/B

**Friday, May 18, 2012**

**REV:1.0**



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|---|---|---|---|---|
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| | | | | Date: Friday, May 18, 2012; Sheet 1 of 59 |

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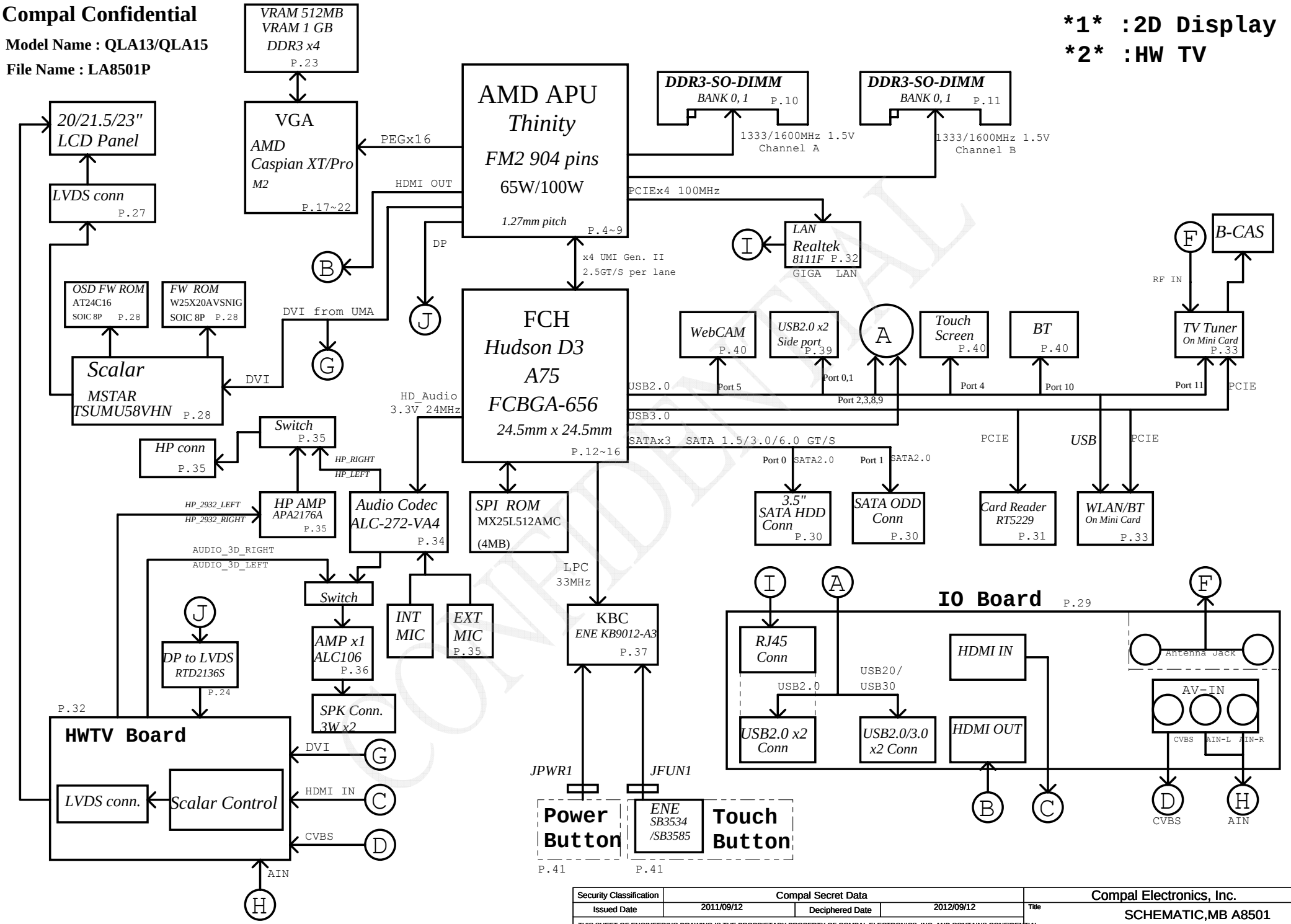
**Model Name : QLA13/QLA15**

**File Name : LA8501P**

***1* :2D Display**
***2* :HW TV**



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| Issued Date | 2011/09/12 | Deciphered Date | 2012/09/12 |



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|---|---|---|---|
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| Title | SCHEMATIC,MB A8501 | | |
| Size: Custom | Document Number: 4019HO | | Rev: B |
| Date: Friday, May 18, 2012 | Sheet 2 of 59 | | |

## Voltage Rails

| Power Plane | Description | S1 | S3 | S5 |
|---|---|---|---|---|
| +12V1 | Adapter power supply (12V)(For V_5V;V_3.3V;1.5V;12VS) | ON | ON | OFF |
| +12V2 | Adapter power supply (12V)(For VGA_CORE;1.05VS;VRAM_1.5VS;CPU_CORE;VGFX_COREP) | ON | ON | OFF |
| +CPU_CORE | Core voltage for CPU | ON | OFF | OFF |
| +VGFX_CORE | Graphics voltage for CPU | ON | OFF | OFF |
| +0.75VS | 0.75V switched power rail for DDR terminator | ON | OFF | OFF |
| +1.05VS | 1.05V switched power rail for CPU | ON | OFF | OFF |
| +1.05VS_PCH | 1.05V switched power rail for PCH | ON | OFF | OFF |
| +1.5V | 1.5V power rail for DDRIII | ON | ON | OFF |
| +1.5VS | 1.5V switched power rail | ON | OFF | OFF |
| +1.8VS | 1.8V switched power rail | ON | OFF | OFF |
| +3VALW | 3.3V always on power rail once PS_ON# low | ON | ON | OFF |
| +3VSB | 3.3V power rail befor PS_ON# low | ON | ON | ON |
| +3.3V_LAN | 3.3V power rail for LAN | ON | ON | ON |
| +3VS | 3.3V switched power rail | ON | OFF | OFF |
| +V_3.3V | 3.3V power rail once Adapter plug-in | ON | ON | OFF |
| +V_5V | 5V power rail once Adapter plug-in | ON | ON | OFF |
| +5VSB | 5V power rail befor PS_ON# low | ON | ON | ON |
| +5VALW | 5V always on power rail once PS_ON# low | ON | ON | ON |
| +5VS | 5V switched power rail | ON | OFF | OFF |
| +RTCVCC | RTC power | ON | ON | ON |
| +3VS_DGPU | 3.3V power rail for GPU | ON | OFF | OFF |
| +VGA_CORE | Graphics power rail for GPU | ON | OFF | OFF |
| +1.05VS_DGPU | 1.05VS switched power rail for GPU | ON | OFF | OFF |
| +VRAM_1.5VS | 1.5VS power rail for VRAM | ON | OFF | OFF |

| STATE \ SIGNAL | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +VSB | +VS |
|---|---|---|---|---|---|---|
| Full ON | HIGH | HIGH | HIGH | ON | ON | ON |
| S1(Power On Suspend) | HIGH | HIGH | HIGH | ON | ON | ON |
| S3 (Suspend to RAM) | LOW | HIGH | HIGH | ON | ON | OFF |
| S4 (Suspend to Disk) | LOW | LOW | HIGH | ON | ON | OFF |
| S5 (Soft OFF) | LOW | LOW | LOW | OFF | ON | OFF |

## BOARD ID Table

| Board ID | Ra/Rb | Vad-bid |
|---|---|---|
| AV SKU | R442 100K | 3.3V |
| NON AV SKU | R445 0 ohm | 0 V |

## USB Port Table

| USB 2.0 | USB 1.1 | Port | Device (D3 Only) |
|---|---|---|---|
| | OHCI | 0 | NC |
| | | 1 | NC |
| EHCI1 DEV18 Fn2 | OHCI | 0 | USB Conn B |
| | | 1 | USB Conn B |
| | | 2 | Touch Screen |
| | | 3 | Camera |
| | | 4 | USB Conn R |
| EHCI2 DEV19 FN2 | OHCI | 5 | MINI(WALN+BT) |
| | | 6 | BT |
| | | 7 | Mini Card(TV Tuner) |
| | | 8 | HWTV |
| | | 9 | USB Conn R |
| EHCI3 DEV22 Fn2 | OHCI | 10 | |
| | | 11 | |
| | | 12 | USB30 Conn3 |
| | | 13 | USB30 Conn4 |
| xHCI DEV16 Fn0 (D3 Only) | | 0 | |
| | | 1 | |
| xHCI DEV16 Fn1 | | 2 | USB 3.0 Port2 |
| | | 3 | USB 3.0 Port3 |

## BTO Option Table

| BTO Item | BOM Structure |
|---|---|
| MBSC@ | VGA@ |
| HWTV@ | UMA@ |
| USB3@ | DIS@ |
| 9012@ | EC 9012@ |
| DIS@ | W/ DIS |
| 930@ | EC 930@ |
| | |
| | |
| Hynix VRAM(512M) | HYN512@ |
| Samsung VRAM(512M) | SAM512@ |
| Hynix VRAM(1G) | HYN1G@ |
| Samsung VRAM(1G) | SAM1G@ |
| | |
| | |

## EC SM Bus1 address

| Device | Address | HEX |
|---|---|---|
| ALC106 | 0100_100xb | 48H |

## EC SM Bus2 address

| Device | Address | HEX |
|---|---|---|
| EMC1412-A (dGPU) | 1111_100xb | F8H |
| SB-TSI | 1001-100xb | 98H |
| LVDS TR( RTD-2136S) | 1001-010xb | 0x94 |
| CPU CORE(IR3565MCP02TRP) | | 0x08 |

## PCH SM Bus address

| Device | Address | |
|---|---|---|
| DDR DIMM1 (FCH_SMB0) | 1001-000xb | 90 |
| DDR DIMM2 (FCH_SMB0) | 1001-001xb | 92 |
| DDR DIMM3 (FCH_SMB0) | 1001-010xb | 94 |
| DDR DIMM4 (FCH_SMB0) | 1001-011xb | 96 |

## SKU ID(Project) Table

| Project_ID2 (GPIO191) | Project_ID1 (GPIO190) | Project_ID0 (GPIO189) | SKU | BOM CONTROL @ |
|---|---|---|---|---|
| 0 | 0 | 0 | UMA_w/o ATV | GPIO189L@ GPIO190L@ GPIO191L@ MBSC@ DAZ@ |
| 0 | 0 | 1 | UMA_w/ ATV | GPIO189H@ GPIO190L@ GPIO191L@ HWTV@ DAZ@ |
| 0 | 1 | 0 | DIS_512M_w/o ATV | GPIO189L@ GPIO190H@ GPIO191L@ MBSC@ DIS@ DAZ@ X7636838L04 |
| 0 | 1 | 1 | DIS_512M_w/ ATV | GPIO189H@ GPIO190H@ GPIO191L@ HWTV@ DIS@ DAZ@ X7636838L04 |
| 1 | 0 | 0 | DIS_1G_w/o ATV | GPIO189L@ GPIO190L@ GPIO191H@ MBSC@ DIS@ DAZ@ X7636838L02 |
| 1 | 0 | 1 | DIS_1G_w/ ATV | GPIO189H@ GPIO190L@ GPIO191H@ HWTV@ DIS@ DAZ@ X7636838L02 |
| 1 | 1 | 0 | X | |
| 1 | 1 | 1 | X | |

| | Vendor | VRAM_ID0 | VRAM_ID1 | VRAM_ID2 | | | |
|---|---|---|---|---|---|---|---|
| X7636838L04 | Hynix 512 | L | L | L | VRAM_ID0L@ | VRAM_ID1L@ | HYN512@ |
| X7636838L02 | Hynix 1G | H | L | L | VRAM_ID0H@ | VRAM_ID1L@ | HYN1G@ |
| X7636838L03 | Samsung 512 | L | H | L | VRAM_ID0L@ | VRAM_ID1H@ | SAM512@ |
| X7636838L01 | Samsung 1G | H | H | L | VRAM_ID0H@ | VRAM_ID1H@ | SAM1G@ |

| | | | |
|---|---|---|---|
| R1 | SA000041S20 | HYN512@ | S IC D3 64MX16 H5TQ1G63DFR-11C |
| R3 | SA000041S70 | | S IC D3 64M16 H5TQ1G63DFR-11C FBGA C38A! |
| R1 | SA00004GS00 | SAM512@ | S IC D3 64M16 K4W1G1646G-BC11 FBGA 96P |
| R3 | SA00004GS50 | | S IC D3 64M16 K4W1G1646G-BC11 FBGA C38A! |
| R1 | SA00003YO00 | HYN1G@ | S IC D3 128MX16 H5TQ2G63BFR-11C FBGA 96P |
| R3 | SA00003YO40 | | S IC D3 128M16 H5TQ2G63BFR-11C 96P C38A! |
| R1 | SA000047Q00 | SAM1G@ | S IC D3 128M16 K4W2G1646C-HC11 FBGA 96P |
| R3 | SA000047Q30 | | S IC D3 128M16 K4W2G1646C-HC11 96P C38A! |

| | | |
|---|---|---|
| VRAM_ID0L@ | R1233 | SD028100280 |
| VRAM_ID1L@ | R1234 | SD028100280 |
| VRAM_ID0H@ | R1230 | SD028100280 |
| VRAM_ID1H@ | R1231 | SD028100280 |



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|---|---|---|---|
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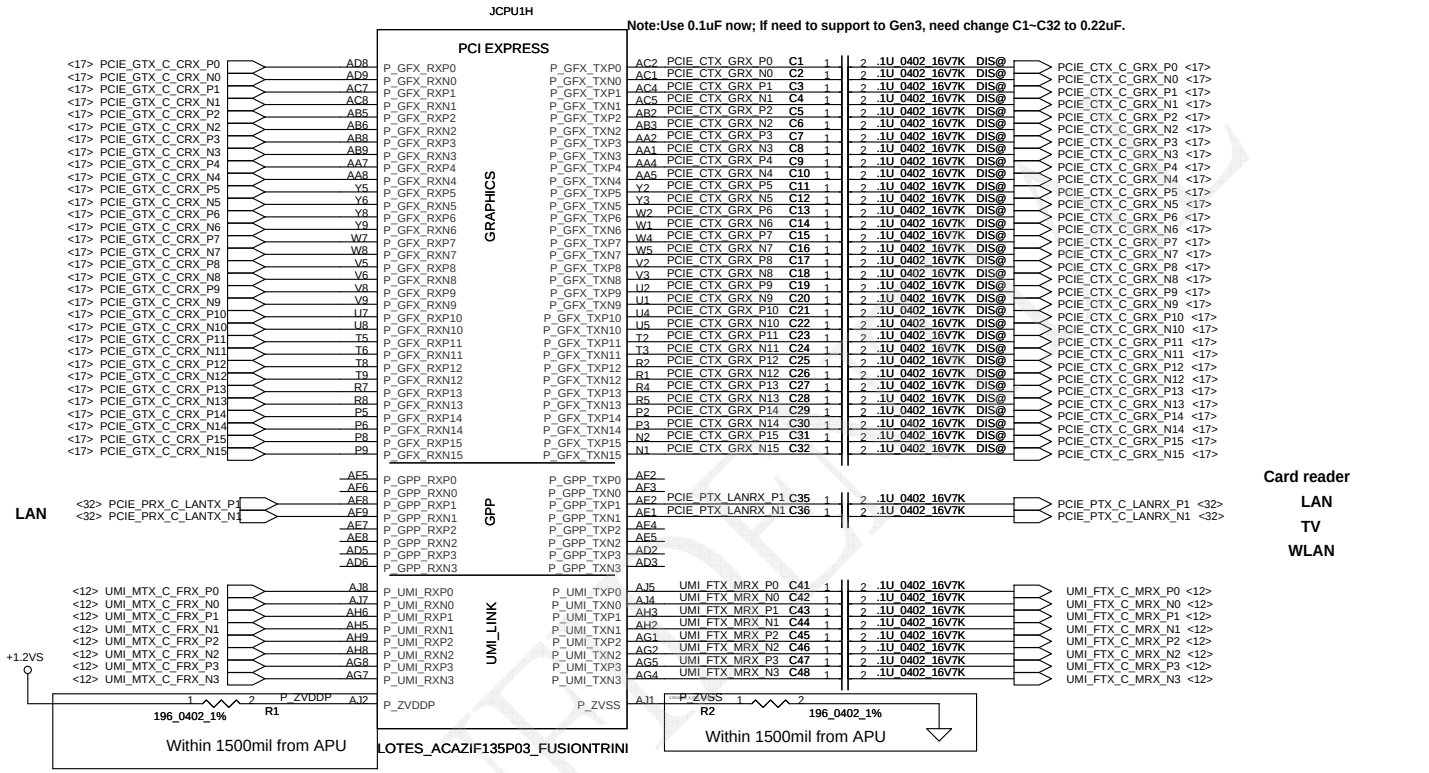
| Date: Friday, May 18, 2012 | Sheet 3 | of 59 | |



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|---|---|---|---|
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| Issued Date | 2011/09/12 | Deciphered Date | 2012/09/12 |



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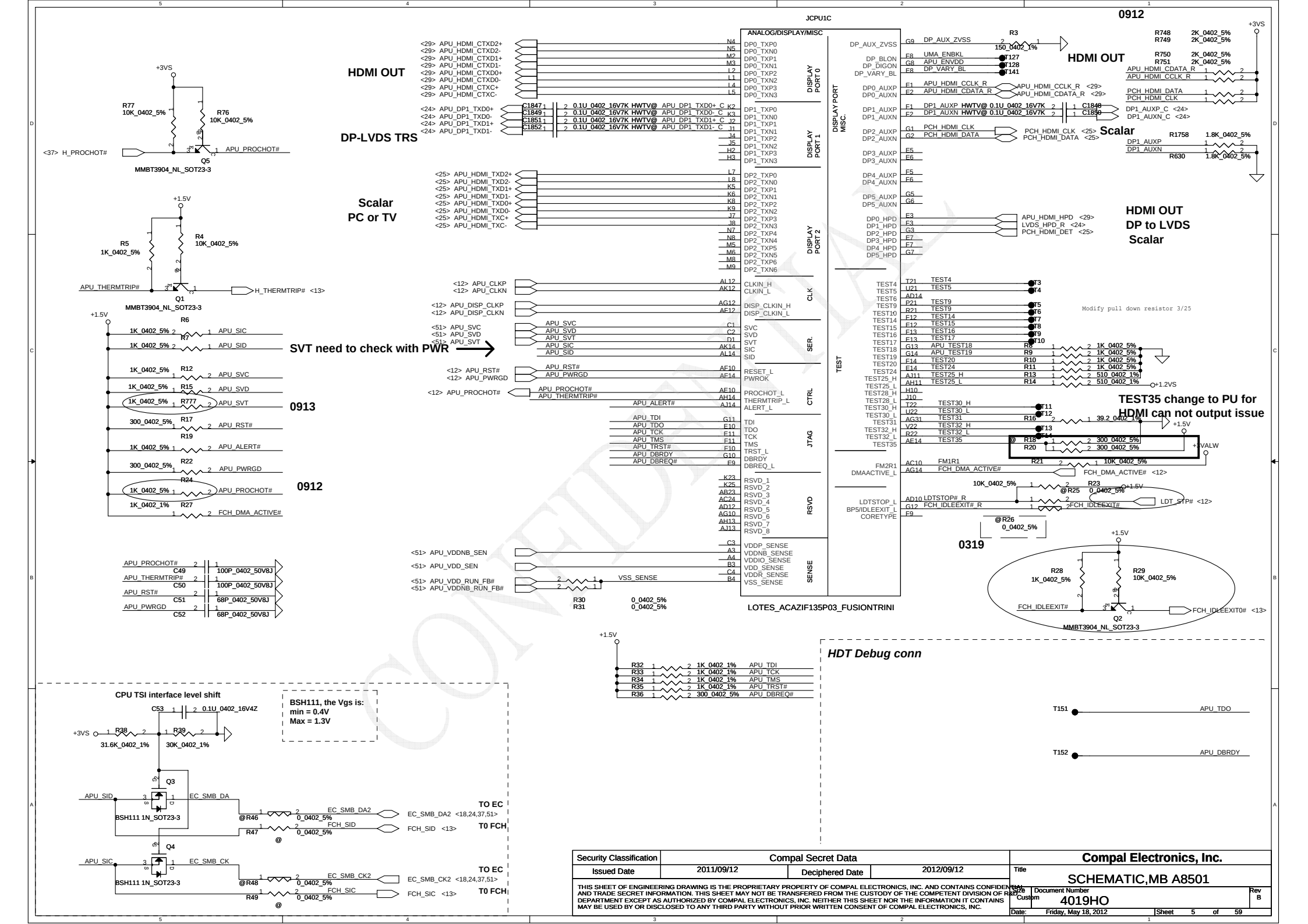


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|---|---|---|
| Custom | 4019HO | B |

Date: Friday, May 18, 2012 | Sheet 5 of 59

<10> DDR_A_MA[0..15]
<10> DDR_A_DM[0..7]
<10> DDR_A_DQS[0..7]
<10> DDR_A_DQS#[0..7]
<10> DDR_A_D[0..63]
<11> DDR_B_MA[0..15]
<11> DDR_B_DM[0..7]
<11> DDR_B_DQS[0..7]
<11> DDR_B_DQS#[0..7]
<11> DDR_B_D[0..63]

JCPU1A

MEMORY CHANNEL A

| | | | | | |
|---|---|---|---|---|---|
| DDR_A_MA0 | V27 | MA_ADD0 | MA_DATA0 | F16 | DDR_A_D0 |
| DDR_A_MA1 | P27 | MA_ADD1 | MA_DATA1 | G16 | DDR_A_D1 |
| DDR_A_MA2 | R25 | MA_ADD2 | MA_DATA2 | H18 | DDR_A_D2 |
| DDR_A_MA3 | P26 | MA_ADD3 | MA_DATA3 | F19 | DDR_A_D3 |
| DDR_A_MA4 | R24 | MA_ADD4 | MA_DATA4 | F15 | DDR_A_D4 |
| DDR_A_MA5 | P24 | MA_ADD5 | MA_DATA5 | H15 | DDR_A_D5 |
| DDR_A_MA6 | P23 | MA_ADD6 | MA_DATA6 | E18 | DDR_A_D6 |
| DDR_A_MA7 | N26 | MA_ADD7 | MA_DATA7 | F18 | DDR_A_D7 |
| DDR_A_MA8 | N23 | MA_ADD8 | | | |
| DDR_A_MA9 | M25 | MA_ADD9 | MA_DATA8 | G20 | DDR_A_D8 |
| DDR_A_MA10 | V24 | MA_ADD10 | MA_DATA9 | H20 | DDR_A_D9 |
| DDR_A_MA11 | N25 | MA_ADD11 | MA_DATA10 | E23 | DDR_A_D10 |
| DDR_A_MA12 | M24 | MA_ADD12 | MA_DATA11 | G23 | DDR_A_D11 |
| DDR_A_MA13 | Y23 | MA_ADD13 | MA_DATA12 | G19 | DDR_A_D12 |
| DDR_A_MA14 | L27 | MA_ADD14 | MA_DATA13 | E20 | DDR_A_D13 |
| DDR_A_MA15 | L24 | MA_ADD15 | MA_DATA14 | F22 | DDR_A_D14 |
| | | | MA_DATA15 | G22 | DDR_A_D15 |
| DDR_A_BS0 | W26 | MA_BANK0 | MA_DATA16 | F24 | DDR_A_D16 |
| DDR_A_BS1 | V25 | MA_BANK1 | MA_DATA17 | H24 | DDR_A_D17 |
| DDR_A_BS2 | L26 | MA_BANK2 | MA_DATA18 | E27 | DDR_A_D18 |
| DDR_A_DM0 | F17 | MA_DM0 | MA_DATA19 | F27 | DDR_A_D19 |
| DDR_A_DM1 | H21 | MA_DM1 | MA_DATA20 | H23 | DDR_A_D20 |
| DDR_A_DM2 | F25 | MA_DM2 | MA_DATA21 | F24 | DDR_A_D21 |
| DDR_A_DM3 | G29 | MA_DM3 | MA_DATA22 | E26 | DDR_A_D22 |
| DDR_A_DM4 | AF29 | MA_DM4 | MA_DATA23 | H26 | DDR_A_D23 |
| DDR_A_DM5 | AF25 | MA_DM5 | | | |
| DDR_A_DM6 | AG21 | MA_DM6 | MA_DATA24 | G28 | DDR_A_D24 |
| DDR_A_DM7 | AF17 | MA_DM7 | MA_DATA25 | E29 | DDR_A_D25 |
| | | | MA_DATA26 | H29 | DDR_A_D26 |
| DDR_A_DQS0 | H17 | MA_DQS_H0 | MA_DATA27 | H30 | DDR_A_D27 |
| DDR_A_DQS#0 | G17 | MA_DQS_L0 | MA_DATA28 | H27 | DDR_A_D28 |
| DDR_A_DQS1 | F21 | MA_DQS_H1 | MA_DATA29 | F28 | DDR_A_D29 |
| DDR_A_DQS#1 | F21 | MA_DQS_L1 | MA_DATA30 | F31 | DDR_A_D30 |
| DDR_A_DQS2 | G26 | MA_DQS_H2 | MA_DATA31 | G31 | DDR_A_D31 |
| DDR_A_DQS#2 | G25 | MA_DQS_L2 | MA_DATA32 | AD30 | DDR_A_D32 |
| DDR_A_DQS3 | F30 | MA_DQS_H3 | MA_DATA33 | AE30 | DDR_A_D33 |
| DDR_A_DQS#3 | E30 | MA_DQS_L3 | MA_DATA34 | AG27 | DDR_A_D34 |
| DDR_A_DQS4 | AE28 | MA_DQS_H4 | MA_DATA35 | AF27 | DDR_A_D35 |
| DDR_A_DQS#4 | AE29 | MA_DQS_L4 | MA_DATA36 | AD31 | DDR_A_D36 |
| DDR_A_DQS5 | AG24 | MA_DQS_H5 | MA_DATA37 | AE31 | DDR_A_D37 |
| DDR_A_DQS#5 | AG25 | MA_DQS_L5 | MA_DATA38 | AG28 | DDR_A_D38 |
| DDR_A_DQS6 | AF20 | MA_DQS_H6 | MA_DATA39 | AD28 | DDR_A_D39 |
| DDR_A_DQS#6 | AF21 | MA_DQS_L6 | | | |
| DDR_A_DQS7 | AE16 | MA_DQS_H7 | MA_DATA40 | AF26 | DDR_A_D40 |
| DDR_A_DQS#7 | AD16 | MA_DQS_L7 | MA_DATA41 | AD25 | DDR_A_D41 |
| | | | MA_DATA42 | AF23 | DDR_A_D42 |
| DDR_A_CLK0 | U27 | MA_CLK_H0 | MA_DATA43 | AE23 | DDR_A_D43 |
| DDR_A_CLK0# | U26 | MA_CLK_L0 | MA_DATA44 | AD27 | DDR_A_D44 |
| DDR_A_CLK1 | T23 | MA_CLK_H1 | MA_DATA45 | AE26 | DDR_A_D45 |
| DDR_A_CLK1# | U23 | MA_CLK_L1 | MA_DATA46 | AE24 | DDR_A_D46 |
| DDR_A_CLK2 | T25 | MA_CLK_H2 | MA_DATA47 | AD24 | DDR_A_D47 |
| DDR_A_CLK2# | T26 | MA_CLK_L2 | MA_DATA48 | AG22 | DDR_A_D48 |
| DDR_A_CLK3 | R27 | MA_CLK_H3 | MA_DATA49 | AD21 | DDR_A_D49 |
| DDR_A_CLK3# | R28 | MA_CLK_L3 | MA_DATA50 | AE19 | DDR_A_D50 |
| | | | MA_DATA51 | AG19 | DDR_A_D51 |
| DDR_A_CKE0 | L23 | MA_CKE0 | MA_DATA52 | AD22 | DDR_A_D52 |
| DDR_A_CKE1 | K26 | MA_CKE1 | MA_DATA53 | AE22 | DDR_A_D53 |
| | | | MA_DATA54 | AF20 | DDR_A_D54 |
| DDR_A_ODT0 | AA24 | MA0_ODT0 | MA_DATA55 | AD19 | DDR_A_D55 |
| DDR_A_ODT1 | AC27 | MA0_ODT1 | | | |
| DDR_A_ODT2 | AA25 | MA1_ODT0 | MA_DATA56 | AG18 | DDR_A_D56 |
| DDR_A_ODT3 | AC26 | MA1_ODT1 | MA_DATA57 | AE17 | DDR_A_D57 |
| | | | MA_DATA58 | AF15 | DDR_A_D58 |
| DDR_A_CS0# | Y27 | MA0_CS_L0 | MA_DATA59 | AG15 | DDR_A_D59 |
| DDR_A_CS1# | AB26 | MA0_CS_L1 | MA_DATA60 | AD18 | DDR_A_D60 |
| DDR_A_CS2# | W23 | MA1_CS_L0 | MA_DATA61 | AF18 | DDR_A_D61 |
| DDR_A_CS3# | AB25 | MA1_CS_L1 | MA_DATA62 | AG16 | DDR_A_D62 |
| | | | MA_DATA63 | AD15 | DDR_A_D63 |
| DDR_A_RAS# | W25 | MA_RAS_L | | | |
| DDR_A_CAS# | Y24 | MA_CAS_L | | | |
| DDR_A_WE# | Y26 | MA_WE_L | | | |
| MA_RESET# | J25 | MA_RESET_L | | | |
| MA_EVENT# | U24 | MA_EVENT_L | | | |
| +M_VREF | K22 | M_VREF | | | |
| M_ZVDDIO | J24 | M_ZVDDIO | | | |

<10> DDR_A_BS0
<10> DDR_A_BS1
<10> DDR_A_BS2
<10> DDR_A_CLK0
<10> DDR_A_CLK0#
<10> DDR_A_CLK1
<10> DDR_A_CLK1#
<10> DDR_A_CLK2
<10> DDR_A_CLK2#
<10> DDR_A_CLK3
<10> DDR_A_CLK3#
<10> DDR_A_CKE0
<10> DDR_A_CKE1
<10> DDR_A_ODT0
<10> DDR_A_ODT1
<10> DDR_A_ODT2
<10> DDR_A_ODT3
<10> DDR_A_CS0#
<10> DDR_A_CS1#
<10> DDR_A_CS2#
<10> DDR_A_CS3#
<10> DDR_A_RAS#
<10> DDR_A_CAS#
<10> DDR_A_WE#
<10> MA_RESET#

DDR_A_CLK2
DDR_A_CLK2#
DDR_A_CLK3
DDR_A_CLK3#
DDR_A_ODT2
DDR_A_ODT3
DDR_A_CS2#
DDR_A_CS3#
DDR_A_RAS#
DDR_A_CAS#
DDR_A_WE#
MA_RESET#
MA_EVENT#

+1.5V
R50 1K_0402_5%
+M_VREF
+1.5V
R52 39.2_0402_1%
M_ZVDDIO

LOTES_ACAZIF135P03_FUSIONTRINI

JCPU1B

MEMORY CHANNEL B

| | | | | | |
|---|---|---|---|---|---|
| DDR_B_MA0 | V31 | MB_ADD0 | MB_DATA0 | A16 | DDR_B_D0 |
| DDR_B_MA1 | N28 | MB_ADD1 | MB_DATA1 | C16 | DDR_B_D1 |
| DDR_B_MA2 | P29 | MB_ADD2 | MB_DATA2 | B18 | DDR_B_D2 |
| DDR_B_MA3 | N29 | MB_ADD3 | MB_DATA3 | A19 | DDR_B_D3 |
| DDR_B_MA4 | N31 | MB_ADD4 | MB_DATA4 | C15 | DDR_B_D4 |
| DDR_B_MA5 | M30 | MB_ADD5 | MB_DATA5 | B15 | DDR_B_D5 |
| DDR_B_MA6 | M31 | MB_ADD6 | MB_DATA6 | D17 | DDR_B_D6 |
| DDR_B_MA7 | M28 | MB_ADD7 | MB_DATA7 | C18 | DDR_B_D7 |
| DDR_B_MA8 | M27 | MB_ADD8 | | | |
| DDR_B_MA9 | L30 | MB_ADD9 | MB_DATA8 | D20 | DDR_B_D8 |
| DDR_B_MA10 | W31 | MB_ADD10 | MB_DATA9 | A20 | DDR_B_D9 |
| DDR_B_MA11 | L29 | MB_ADD11 | MB_DATA10 | D22 | DDR_B_D10 |
| DDR_B_MA12 | K28 | MB_ADD12 | MB_DATA11 | D23 | DDR_B_D11 |
| DDR_B_MA13 | AB28 | MB_ADD13 | MB_DATA12 | C19 | DDR_B_D12 |
| DDR_B_MA14 | K31 | MB_ADD14 | MB_DATA13 | D19 | DDR_B_D13 |
| DDR_B_MA15 | J31 | MB_ADD15 | MB_DATA14 | A22 | DDR_B_D14 |
| | | | MB_DATA15 | C22 | DDR_B_D15 |
| DDR_B_BS0 | W29 | MB_BANK0 | MB_DATA16 | C24 | DDR_B_D16 |
| DDR_B_BS1 | V30 | MB_BANK1 | MB_DATA17 | B24 | DDR_B_D17 |
| DDR_B_BS2 | K29 | MB_BANK2 | MB_DATA18 | B26 | DDR_B_D18 |
| DDR_B_DM0 | D16 | MB_DM0 | MB_DATA19 | C27 | DDR_B_D19 |
| DDR_B_DM1 | B20 | MB_DM1 | MB_DATA20 | A23 | DDR_B_D20 |
| DDR_B_DM2 | A25 | MB_DM2 | MB_DATA21 | B23 | DDR_B_D21 |
| DDR_B_DM3 | D29 | MB_DM3 | MB_DATA22 | D26 | DDR_B_D22 |
| DDR_B_DM4 | AL29 | MB_DM4 | MB_DATA23 | A26 | DDR_B_D23 |
| DDR_B_DM5 | AH25 | MB_DM5 | | | |
| DDR_B_DM6 | AK21 | MB_DM6 | MB_DATA24 | C28 | DDR_B_D24 |
| DDR_B_DM7 | AJ17 | MB_DM7 | MB_DATA25 | D28 | DDR_B_D25 |
| | | | MB_DATA26 | C31 | DDR_B_D26 |
| DDR_B_DQS0 | A17 | MB_DQS_H0 | MB_DATA27 | D31 | DDR_B_D27 |
| DDR_B_DQS#0 | B17 | MB_DQS_L0 | MB_DATA28 | B27 | DDR_B_D28 |
| DDR_B_DQS1 | B21 | MB_DQS_H1 | MB_DATA29 | A28 | DDR_B_D29 |
| DDR_B_DQS#1 | C21 | MB_DQS_L1 | MB_DATA30 | B30 | DDR_B_D30 |
| DDR_B_DQS2 | D25 | MB_DQS_H2 | MB_DATA31 | C30 | DDR_B_D31 |
| DDR_B_DQS#2 | C25 | MB_DQS_L2 | MB_DATA32 | AJ30 | DDR_B_D32 |
| DDR_B_DQS3 | B29 | MB_DQS_H3 | MB_DATA33 | AK30 | DDR_B_D33 |
| DDR_B_DQS#3 | A29 | MB_DQS_L3 | MB_DATA34 | AH28 | DDR_B_D34 |
| DDR_B_DQS4 | AJ29 | MB_DQS_H4 | MB_DATA35 | AJ27 | DDR_B_D35 |
| DDR_B_DQS#4 | AH29 | MB_DQS_L4 | MB_DATA36 | AG30 | DDR_B_D36 |
| DDR_B_DQS5 | AK25 | MB_DQS_H5 | MB_DATA37 | AH31 | DDR_B_D37 |
| DDR_B_DQS#5 | AL25 | MB_DQS_L5 | MB_DATA38 | AK28 | DDR_B_D38 |
| DDR_B_DQS6 | AJ20 | MB_DQS_H6 | MB_DATA39 | AL28 | DDR_B_D39 |
| DDR_B_DQS#6 | AJ21 | MB_DQS_L6 | | | |
| DDR_B_DQS7 | AL16 | MB_DQS_H7 | MB_DATA40 | AJ26 | DDR_B_D40 |
| DDR_B_DQS#7 | AL17 | MB_DQS_L7 | MB_DATA41 | AH26 | DDR_B_D41 |
| | | | MB_DATA42 | AH23 | DDR_B_D42 |
| DDR_B_CLK0 | U30 | MB_CLK_H0 | MB_DATA43 | AJ23 | DDR_B_D43 |
| DDR_B_CLK0# | U29 | MB_CLK_L0 | MB_DATA44 | AK27 | DDR_B_D44 |
| DDR_B_CLK1 | T29 | MB_CLK_H1 | MB_DATA45 | AL26 | DDR_B_D45 |
| DDR_B_CLK1# | T28 | MB_CLK_L1 | MB_DATA46 | AJ24 | DDR_B_D46 |
| DDR_B_CLK2 | R31 | MB_CLK_H2 | MB_DATA47 | AK24 | DDR_B_D47 |
| DDR_B_CLK2# | T31 | MB_CLK_L2 | MB_DATA48 | AK22 | DDR_B_D48 |
| DDR_B_CLK3 | P30 | MB_CLK_H3 | MB_DATA49 | AH22 | DDR_B_D49 |
| DDR_B_CLK3# | R30 | MB_CLK_L3 | MB_DATA50 | AL19 | DDR_B_D50 |
| | | | MB_DATA51 | AK19 | DDR_B_D51 |
| DDR_B_CKE0 | J30 | MA_CKE0 | MB_DATA52 | AL23 | DDR_B_D52 |
| DDR_B_CKE1 | J28 | MA_CKE1 | MB_DATA53 | AL22 | DDR_B_D53 |
| | | | MB_DATA54 | AH20 | DDR_B_D54 |
| DDR_B_ODT0 | AA30 | MB0_ODT0 | MB_DATA55 | AL20 | DDR_B_D55 |
| DDR_B_ODT1 | AC30 | MB0_ODT1 | | | |
| DDR_B_ODT2 | AA31 | MB1_ODT0 | MB_DATA56 | AJ18 | DDR_B_D56 |
| DDR_B_ODT3 | AC29 | MB1_ODT1 | MB_DATA57 | AH17 | DDR_B_D57 |
| | | | MB_DATA58 | AJ15 | DDR_B_D58 |
| DDR_B_CS0# | Y29 | MB0_CS_L0 | MB_DATA59 | AK15 | DDR_B_D59 |
| DDR_B_CS1# | AB29 | MB0_CS_L1 | MB_DATA60 | AH19 | DDR_B_D60 |
| DDR_B_CS2# | Y30 | MB1_CS_L0 | MB_DATA61 | AK18 | DDR_B_D61 |
| DDR_B_CS3# | AB31 | MB1_CS_L1 | MB_DATA62 | AK16 | DDR_B_D62 |
| | | | MB_DATA63 | AH16 | DDR_B_D63 |
| DDR_B_RAS# | W28 | MB_RAS_L | | | |
| DDR_B_CAS# | AA27 | MB_CAS_L | | | |
| DDR_B_WE# | AA28 | MB_WE_L | | | |
| MB_RESET# | J27 | MB_RESET_L | | | |
| MB_EVENT# | V28 | MB_EVENT_L | | | |

<11> DDR_B_BS0
<11> DDR_B_BS1
<11> DDR_B_BS2
<11> DDR_B_CLK0
<11> DDR_B_CLK0#
<11> DDR_B_CLK1
<11> DDR_B_CLK1#
<11> DDR_B_CLK2
<11> DDR_B_CLK2#
<11> DDR_B_CLK3
<11> DDR_B_CLK3#
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<11> DDR_B_CKE1
<11> DDR_B_ODT0
<11> DDR_B_ODT1
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<11> DDR_B_ODT3
<11> DDR_B_CS0#
<11> DDR_B_CS1#
<11> DDR_B_CS2#
<11> DDR_B_CS3#
<11> DDR_B_RAS#
<11> DDR_B_CAS#
<11> DDR_B_WE#
<11> MB_RESET#

DDR_B_CLK2
DDR_B_CLK2#
DDR_B_CLK3
DDR_B_CLK3#
DDR_B_ODT2
DDR_B_ODT3
DDR_B_CS2#
DDR_B_CS3#
DDR_B_RAS#
DDR_B_CAS#
DDR_B_WE#
MB_RESET#
MB_EVENT#

+1.5V
R51 1K_0402_5%

LOTES_ACAZIF135P03_FUSIONTRINI

1116 modify

PLACE WITHIN 1.5" OF APU

+1.5V
R53 1K_0402_1%
+M_VREF
R54 1K_0402_1%
C54 1000P_0402_50V7K
C55 0.1U_0402_16V4Z

MA_EVENT#
MB_EVENT#
MA_EVENT# <10>
MB_EVENT# <11>



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| Size: Custom | Document Number: 4019HO | | Rev: B |
| Date: Friday, May 18, 2012 | Sheet 6 of 59 | | |

VDD = Variable per VID

VDDIO = 1.25V/1.35V/1.5V (DDR3)

+CPU_CORE

JCPU1D

VDD

H8 H12 H14 J6 J9 J11 J13 J15 J17 J19 J21 K4 K7 K10 K12 K14 K16 K18 K20 L3 L11 L15 L17 L21 M10 M12 M16 M18 M20 N3 N6 N11 N19 N21 P1 P4 P7 P10 P12 P20 R11 R13 R19 T1 T10 T12 T20 U3 U6 U11 U13

VDD_1 VDD_2 VDD_3 VDD_4 VDD_5 VDD_6 VDD_7 VDD_8 VDD_9 VDD_10 VDD_11 VDD_12 VDD_13 VDD_14 VDD_15 VDD_16 VDD_17 VDD_18 VDD_19 VDD_20 VDD_21 VDD_22 VDD_23 VDD_24 VDD_25 VDD_26 VDD_27 VDD_28 VDD_29 VDD_30 VDD_31 VDD_32 VDD_33 VDD_34 VDD_35 VDD_36 VDD_37 VDD_38 VDD_39 VDD_40 VDD_41 VDD_42 VDD_43 VDD_44 VDD_45 VDD_46 VDD_47 VDD_48 VDD_49 VDD_50 VDD_51

VDD_52 VDD_53 VDD_54 VDD_55 VDD_56 VDD_57 VDD_58 VDD_59 VDD_60 VDD_61 VDD_62 VDD_63 VDD_64 VDD_65 VDD_66 VDD_67 VDD_68 VDD_69 VDD_70 VDD_71 VDD_72 VDD_73 VDD_74 VDD_75 VDD_76 VDD_77 VDD_78 VDD_79 VDD_80 VDD_81 VDD_82 VDD_83 VDD_84 VDD_85 VDD_86 VDD_87 VDD_88 VDD_89 VDD_90 VDD_91 VDD_92 VDD_93 VDD_94 VDD_95 VDD_96 VDD_97 VDD_98 VDD_99

U19 V1 V4 V7 V10 V12 V20 W11 W13 W19 W21 Y1 Y10 Y12 Y14 Y16 Y18 Y20 AA3 AA6 AA11 AA13 AA15 AA17 AA19 AA21 AB1 AB4 AB7 AB10 AB14 AB16 AB18 AC11 AC13 AC15 AC17 AC19 AC21 AD1 AE3 AF6 AF1 AF4 AF7 AG6 AH1 AH7

+CPU_CORE

LOTES_ACAZIF135P03_FUSIONTRINI

+1.5V

JCPU1E

POWER

J26 J29 K24 K27 K30 L25 L28 L31 M22 M23 M26 M29 N24 N27 N30 P22 P25 P28 P31 R23 R26 R29 T24 T27 T30 U25 U28 U31 V23 V26 V29 W24 W27 W30 Y22 Y25 Y28 Y31 AA23 AA26 AA29 AB22 AB24 AB27 AB30 AC23 AC25 AC28 AC31

VDDIO_1 VDDIO_2 VDDIO_3 VDDIO_4 VDDIO_5 VDDIO_6 VDDIO_7 VDDIO_8 VDDIO_9 VDDIO_10 VDDIO_11 VDDIO_12 VDDIO_13 VDDIO_14 VDDIO_15 VDDIO_16 VDDIO_17 VDDIO_18 VDDIO_19 VDDIO_20 VDDIO_21 VDDIO_22 VDDIO_23 VDDIO_24 VDDIO_25 VDDIO_26 VDDIO_27 VDDIO_28 VDDIO_29 VDDIO_30 VDDIO_31 VDDIO_32 VDDIO_33 VDDIO_34 VDDIO_35 VDDIO_36 VDDIO_37 VDDIO_38 VDDIO_39 VDDIO_40 VDDIO_41 VDDIO_42 VDDIO_43 VDDIO_44 VDDIO_45 VDDIO_46 VDDIO_47 VDDIO_48 VDDIO_49

AD13 AE13

VDDA_1 VDDA_2

A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 M14 N13

VDDNB_1 VDDNB_2 VDDNB_3 VDDNB_4 VDDNB_5 VDDNB_6 VDDNB_7 VDDNB_8 VDDNB_9 VDDNB_10 VDDNB_11 VDDNB_12 VDDNB_13 VDDNB_14 VDDNB_15 VDDNB_16 VDDNB_17 VDDNB_18 VDDNB_19 VDDNB_20 VDDNB_21 VDDNB_22 VDDNB_23 VDDNB_24 VDDNB_25 VDDNB_26 VDDNB_27 VDDNB_28 VDDNB_29 VDDNB_30 VDDNB_CAP_1 VDDNB_CAP_2

+CPU_CORE_NB

VDDNB = 0.8V (Variable)

+VDDNBCAP C59 1 2 22U_0805_6.3V6M C60 1 2 22U_0805_6.3V6M

Place close pin M14 and N13 inside the backplate cavity opening

AK2 AK3 AK4 AK5 AL6

VDDP_A_1 VDDP_A_2 VDDP_A_3 VDDP_A_4 VDDP_A_5

AK8 AK9 AK10 AL8

VDDR_1 VDDR_2 VDDR_3 VDDR_4

AK6 AL3 AL4 AL5

VDDP_B_1 VDDP_B_2 VDDP_B_3 VDDP_B_4

AL9 AL10

VDDR_5 VDDR_6

LOTES_ACAZIF135P03_FUSIONTRINI

+2.5VS

C56 4.7U_0603_6.3V6K C57 0.22U_0603_16V4Z C58 3300P_0402_50V7K

VDDA
1x 4.7uF 0805/X5R
1x 0.22uF 0603/X7R
1x 3300P

(VDDP_A) +1.2VS

C61 10U_0603_6.3V6M C62 10U_0603_6.3V6M C63 22U_0805_6.3V6M C64 4.7U_0603_6.3V6K C65 1000P_0402_50V7K C66 180P_0402_50V8J C67 180P_0402_50V8J

VDDP(A_B) EMI
2x 22uF 0805/X5R BOT side
2x 10uF 0805/X5R
1x 0.22uF 0603/X7R
1x 1000P
4x180P

(VDDR_A) +1.2VS

C67 22U_0805_6.3V6M C68 10U_0603_6.3V6M C69 0.22U_0603_16V4Z C70 180P_0402_50V8J

EMI
BOT side

(VDDP_B) +1.2VS

C71 10U_0603_6.3V6M C72 0.22U_0603_16V4Z C73 22U_0805_6.3V6M C74 180P_0402_50V8J C75 180P_0402_50V8J

EMI
BOT side

(VDDR_B) +1.2VS

C76 10U_0603_6.3V6M C77 4.7U_0603_6.3V6K C78 0.22U_0603_16V4Z C79 0.22U_0603_16V4Z C80 180P_0402_50V8J

EMI
BOT side

+1.2VS

C81 220U_6.3V_M

VDDR(A_B)
1x 22uF 0805/X5R
2x 10uF 0805/X5R
3x 0.22uF 0603/X7R
2x180P

VDDR = 1.2V
VDDPCIE = 1.2V
ONLY ONE SIDE OF VDDPCIE & VDDR MUST CONNECTED ON THE PCB.CONNECTING BOTH SIDES IS ACCEPTABLE BUT NOT REQUIRED. BOTH SIDES MUST BE DECOUPLED.

VDDP and VDDR support two separate power planes with single regulator



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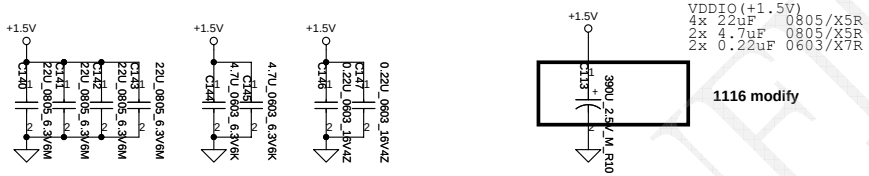
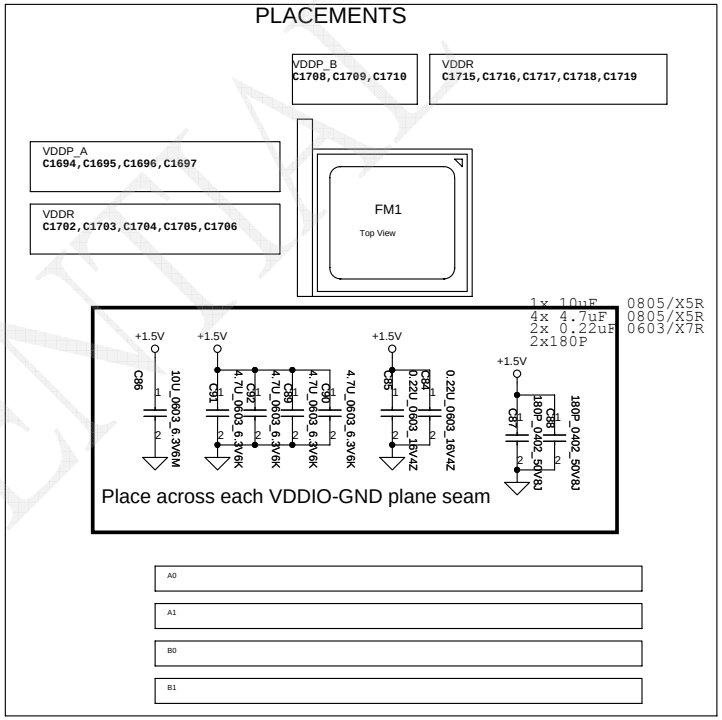
| Size | Document Number | Rev |
|---|---|---|
| Custom | 4019HO | B |

Date: Friday, May 18, 2012 Sheet 7 of 59

**+CPU_CORE At PWR Page53**

**+CPU_CORE_NB At PWR Page53**



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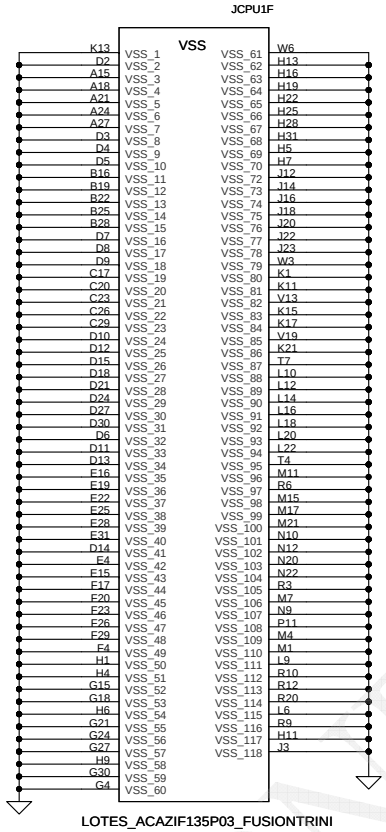
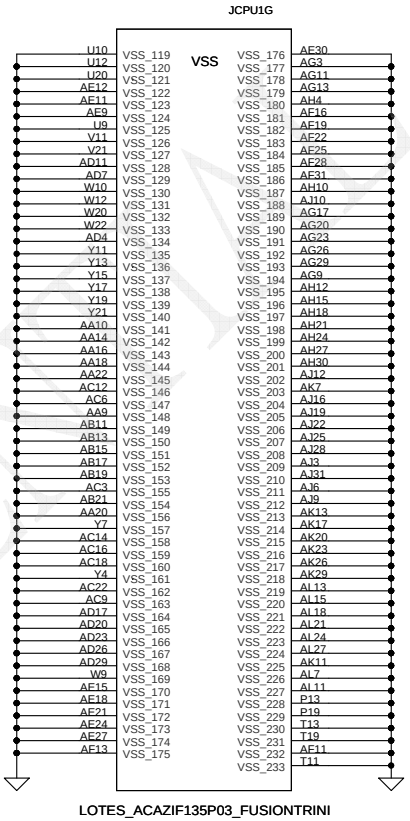
Date: Friday, May 18, 2012 | Sheet 8 of 59



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|---|---|---|
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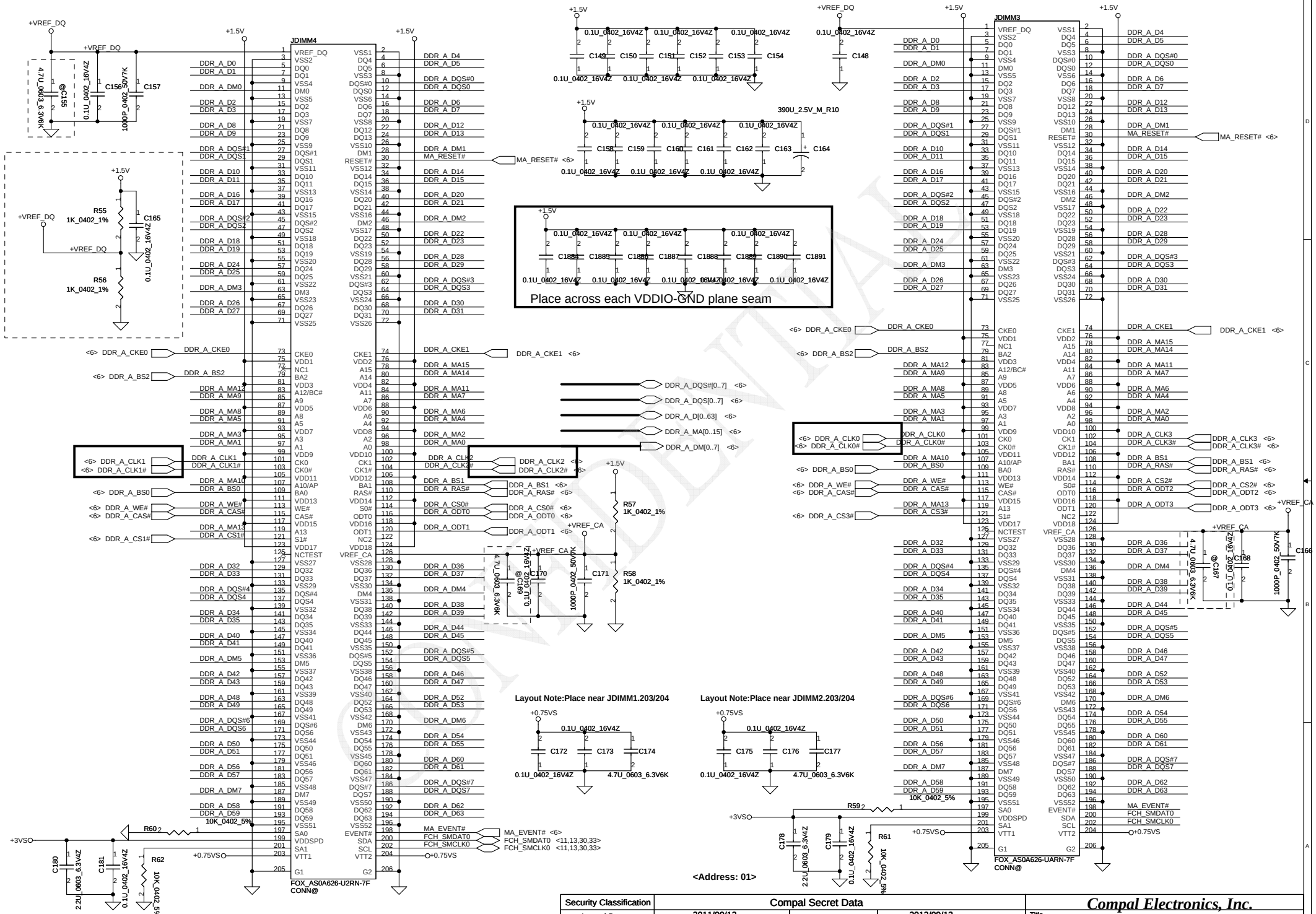
Date: Friday, May 18, 2012 | Sheet 9 of 59

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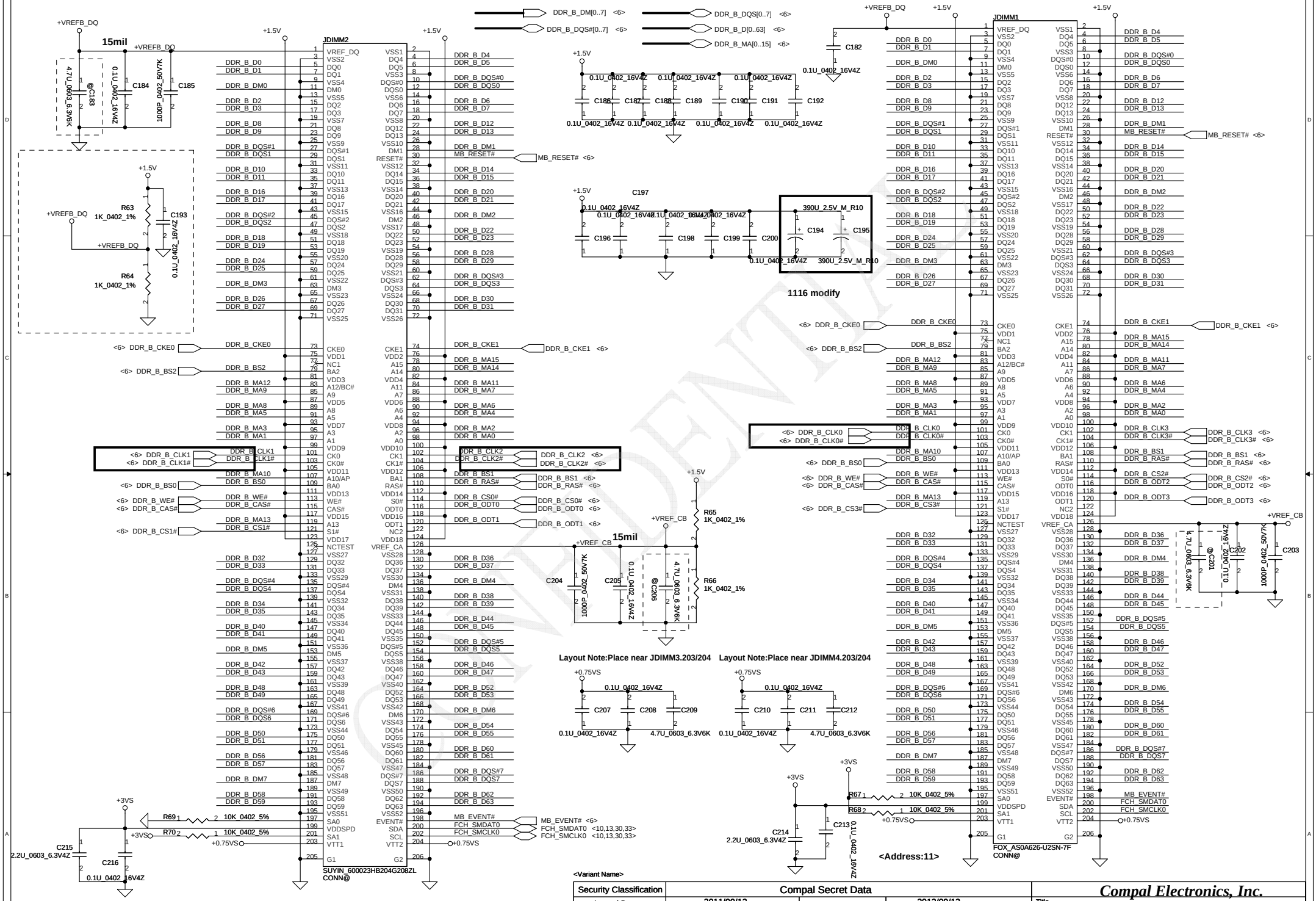
| Date: Friday, May 18, 2012 | Sheet 10 of 59 | |


JDIMM2
JDIMM1
SUYIN_600023HB204G208ZL CONN@
FOX_AS0A626-U2SN-7F CONN@
15mil
Layout Note:Place near JDIMM3.203/204
Layout Note:Place near JDIMM4.203/204
1116 modify
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<Address:11>
2011 0426
DDR3 SO-DIMM B
change to Normal Type L
<Variant Name>
Security Classification
Compal Secret Data
Issued Date
2011/09/12
Deciphered Date
2012/09/12
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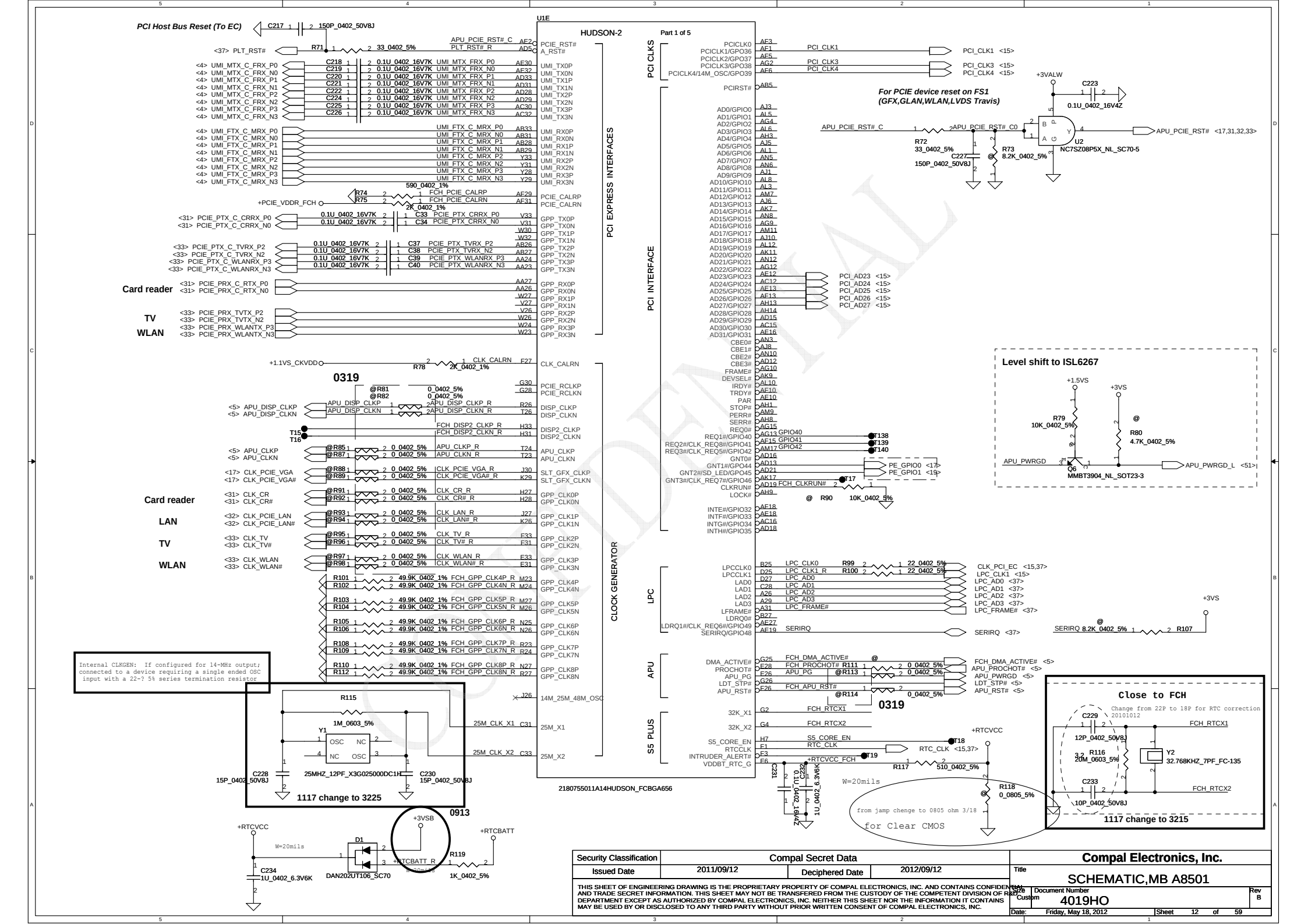
SCHEMATIC,MB A8501
Document Number
4019HO
Rev
B
Date: Friday, May 18, 2012
Sheet 11 of 59

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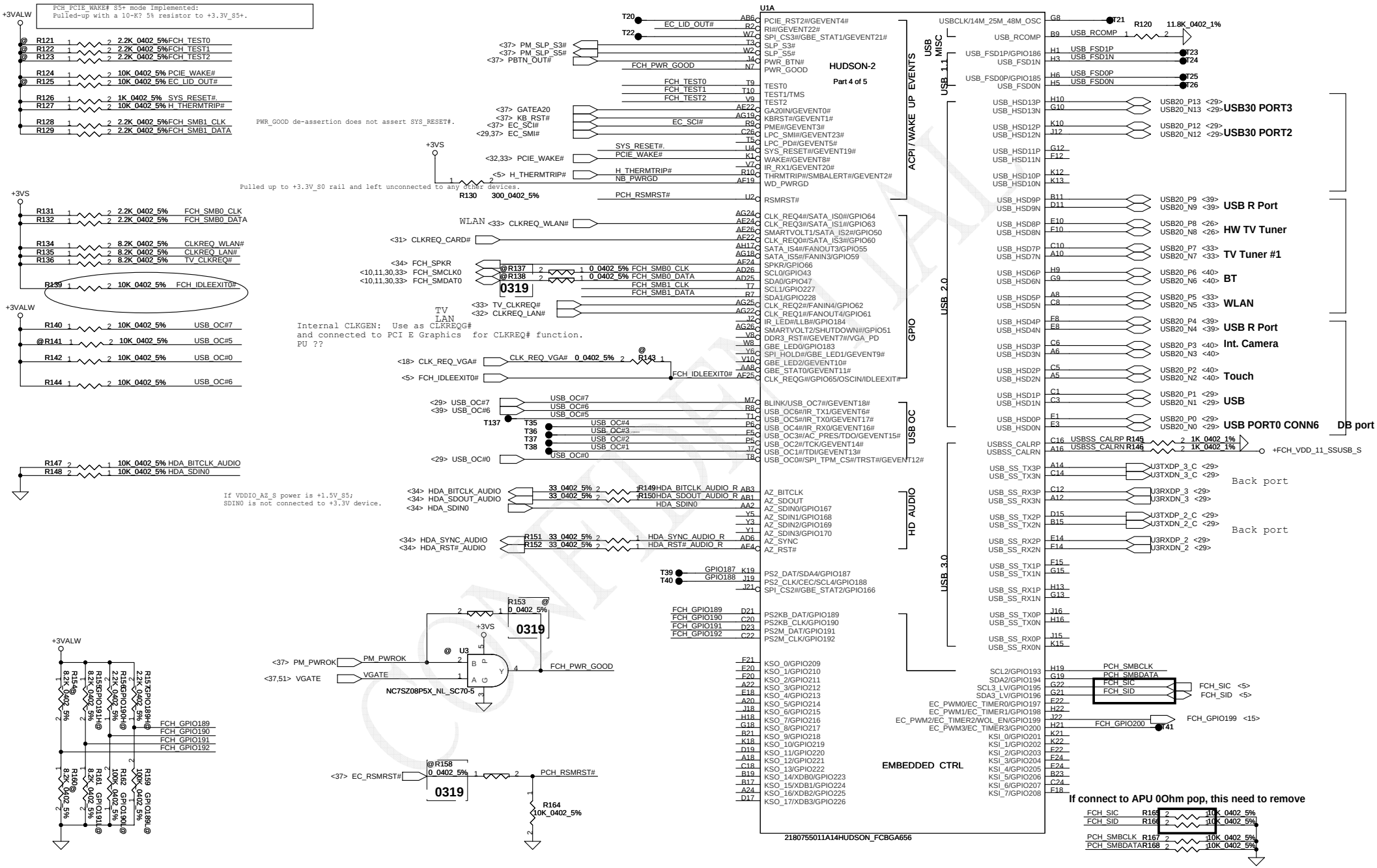
| Size | Document Number | Rev |
|---|---|---|
| Custom | 4019HO | B |

Date: Friday, May 18, 2012 | Sheet 12 of 59



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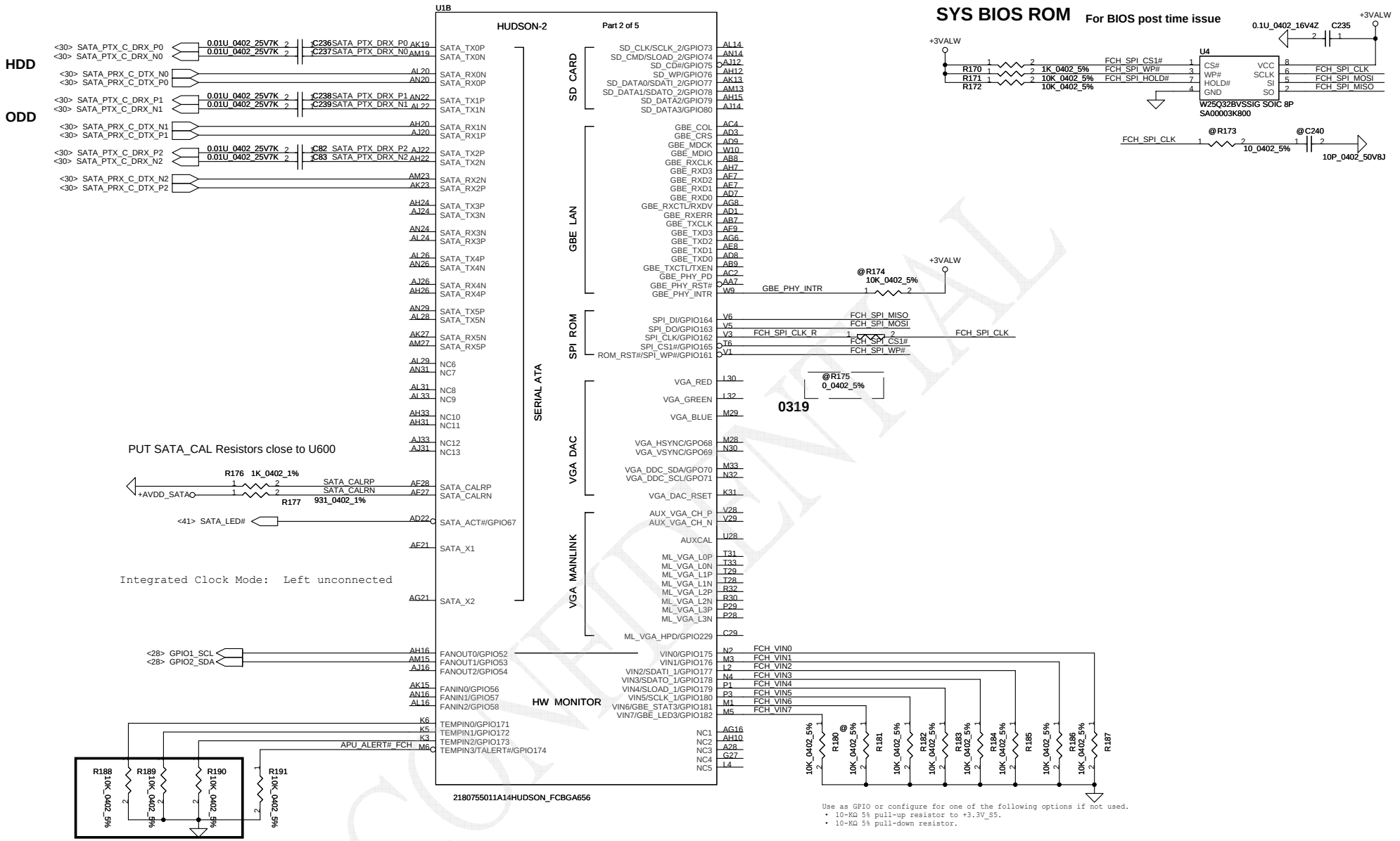




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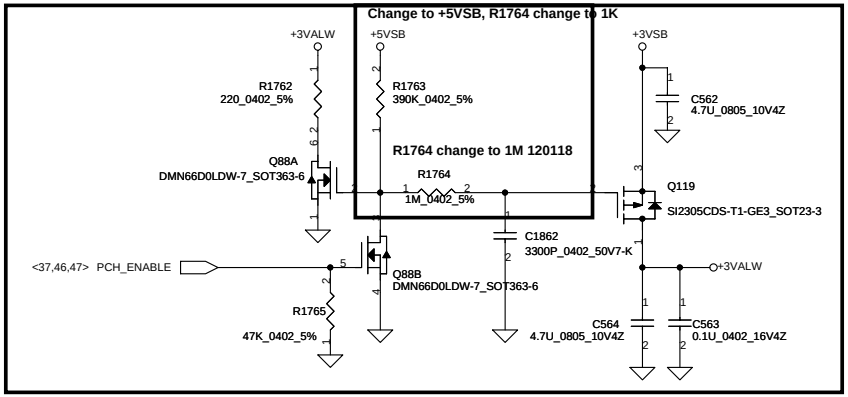
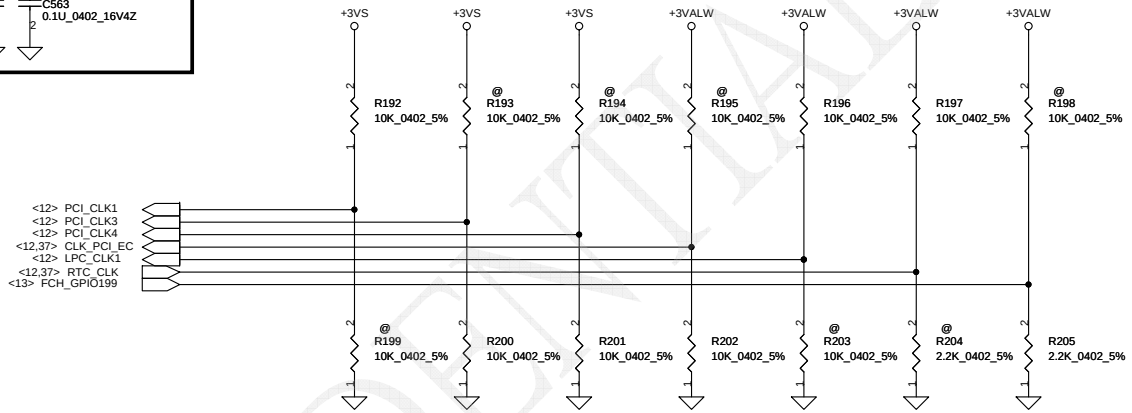



## STRAP PINS

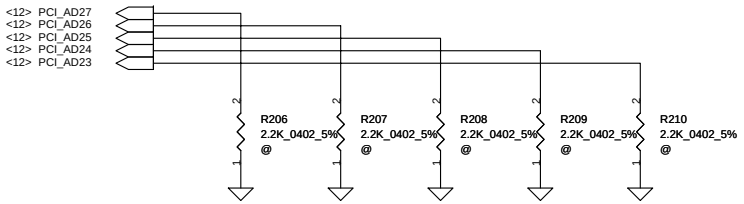
| | PCI_CLK1 | PCI_CLK3 | PCI_CLK4 | CLK_PCI_EC | LPC_CLK1 | FCH_GPIO199 | RTC_CLK |
|---|---|---|---|---|---|---|---|
| PULL HIGH | ALLOW PCIE GEN2 DEFAULT | USE DEBUG STRAPS | NON_FUSION CLOCK MODE | EC ENABLED | CLKGEN ENABLED DEFAULT | LPC ROM | S5 PLUS MODE DISABLED DEFAULT |
| PULL LOW | FORCE PCIE GEN1 | IGNORE DEBUG STRAP DEFAULT | FUSION CLOCK MODE DEFAULT | EC DISABLED DEFAULT | CLKGEN DISABLE | SPI ROM DEFAULT | S5 PLUS MODE ENABLED |




## DEBUG STRAPS

**FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]**

| | PCI_AD27 | PCI_AD26 | PCI_AD25 | PCI_AD24 | PCI_AD23 |
|---|---|---|---|---|---|
| PULL HIGH | USE PCI PLL DEFAULT | RESERVED | Normal REFCLK termination DEFAULT | USE DEFAULT PCIE STRAPS DEFAULT | DISABLE PCI MEM BOOT DEFAULT |
| PULL LOW | BYPASS PCI PLL | RESERVED | Inverted REFCLK termination | USE EEPROM PCIE STRAPS | ENABLE PCI MEM BOOT |



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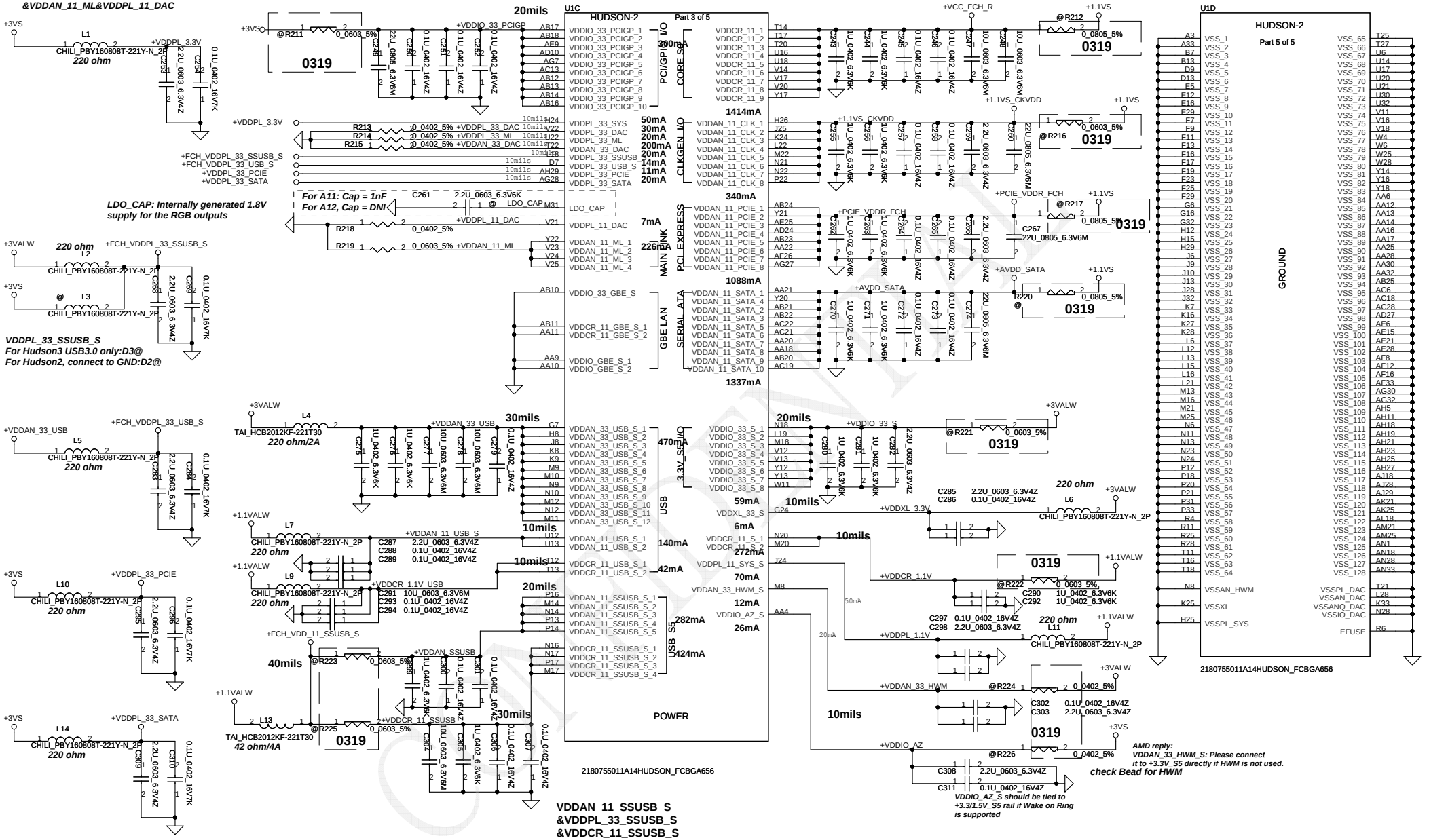
Size: Custom | Document Number: 4019HO | Rev: B

Date: Friday, May 18, 2012 | Sheet 15 of 59

*VGA(CRT) Translator Not Implemented: Connected to VSS.*
*VDDAN_33_DAC&VDDPL_33_ML&VDDPL_33DAC*
*&VDDAN_11_ML&VDDPL_11_DAC*

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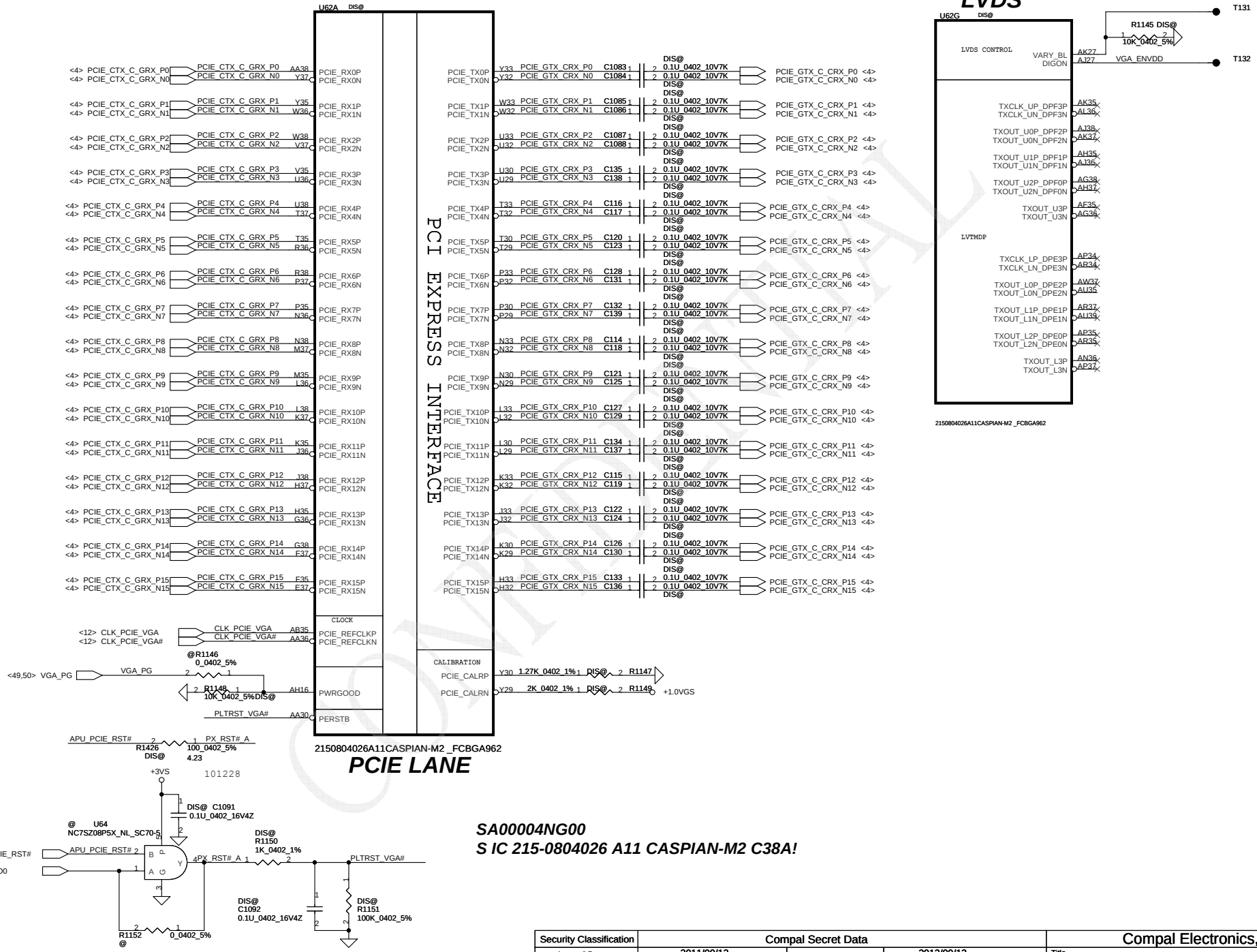


***SA00004NG00***
***S IC 215-0804026 A11 CASPIAN-M2 C38A!***



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| Date: Friday, May 18, 2012 | Sheet 17 of 59 | | |

## CONFIGURATION STRAPS

**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET**

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

| STRAPS | PIN | DESCRIPTION OF DEFAULT SETTINGS | RECOMMENDED SETTINGS |
|---|---|---|---|
| TX_PWRS_ENB | GPIO0 | PCIE FULL TX OUTPUT SWING | X |
| TX_DEEMPH_EN | GPIO1 | PCIE TRANSMITTER DE-EMPHASIS ENABLED | X |
| RSVD | GPIO2 | RESERVED | 0 |
| RSVD | GPIO8 | RESERVED | 0 |
| BIF_VGA DIS | GPIO9 | VGA ENABLED | 0 |
| RSVD | GPIO21 | RESERVED | 0 |
| BIOS_ROM_EN | GPIO_22_ROMCSB | ENABLE EXTERNAL BIOS ROM | X |
| ROMIDCFG(2:0) | GPIO[13:11] | SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT | XXX |
| VIP_DEVICE_STRAP_ENA | V2SYNC | IGNORE VIP DEVICE STRAPS | 0 |
| RSVD | H2SYNC | | 0 |
| RSVD | GENERICC | | 0 |
| AUD[1]<br>AUD[0] | HSYNC<br>VSYNC | AUD[1] AUD[0]<br>0 0 No audio function<br>0 1 Audio for DisplayPort and HDMI if dongle is detected<br>1 0 Audio for DisplayPort only<br>1 1 Audio for both DisplayPort and HDMI | 11 |
| | GPIO21, H2SYNC, GENERICC, GPIO2, GPIO8 | AMD RESERVED CONFIGURATION STRAPS<br>**ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET** | |

## STRAPS

## VGA Thermal Sensor EMC1412-A

Closed to GPU

U65 — EMC1412-A-ACZL-TR MSOP 8P

EMC1412-A (SA00003YA00)
Address 1111_100xb
S.IC EMC1412-A-ACZL-TR MSOP 8P SENSOR

## XTALIN

Voltage Swing: 1.8 V

1117 change to 3225

## Internal HDMI

0.60 V level, Please VREFG Divider ans cap close to ASIC

## External HDMI

Not need HDMI
AUDIO from Dgpu 120118

## Global Swap Lock on Multiple GPUs

NC on Park, Robson and Seymour
NC on Park, Robson

NC on Park, Robson and Seymour

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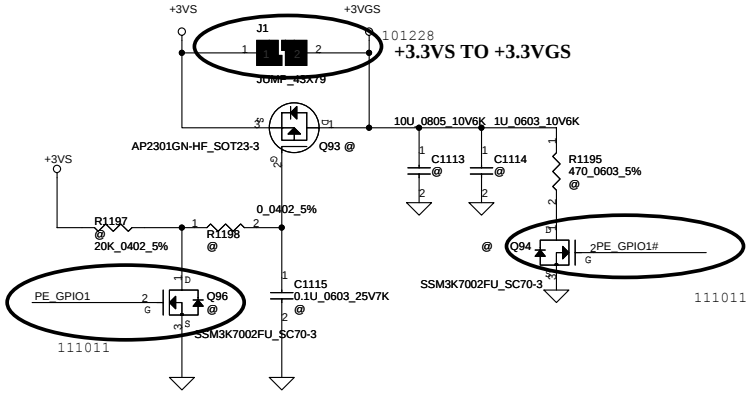
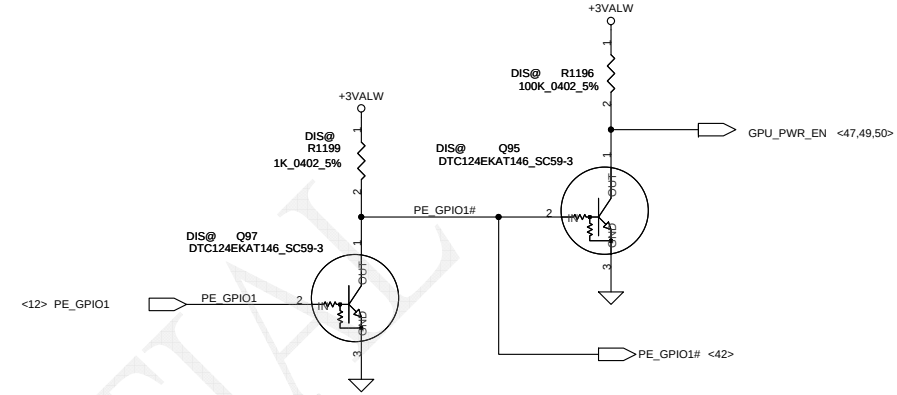
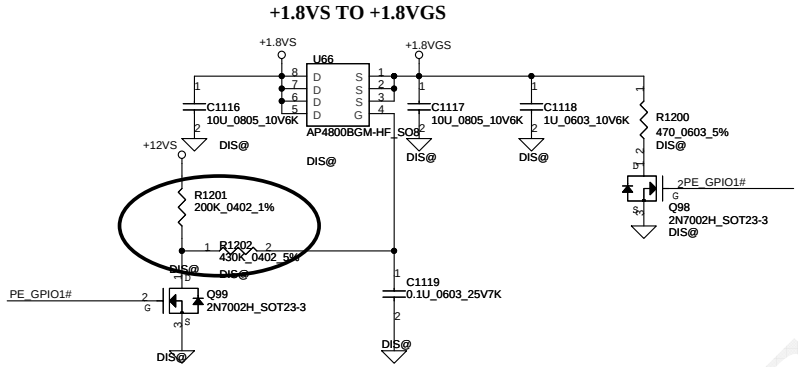
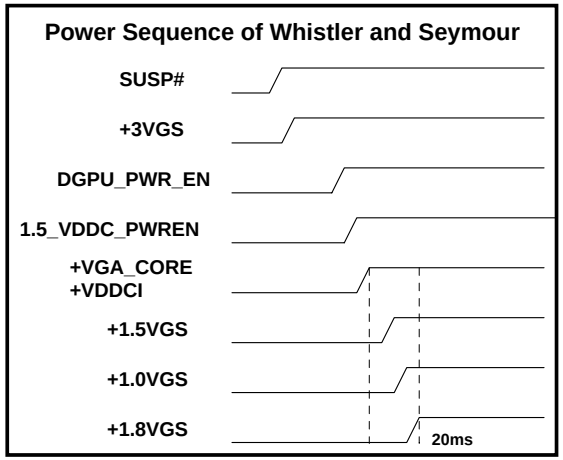
Size: Custom | Document Number: 4019HO | Rev: B

Date: Friday, May 18, 2012 | Sheet 18 of 59



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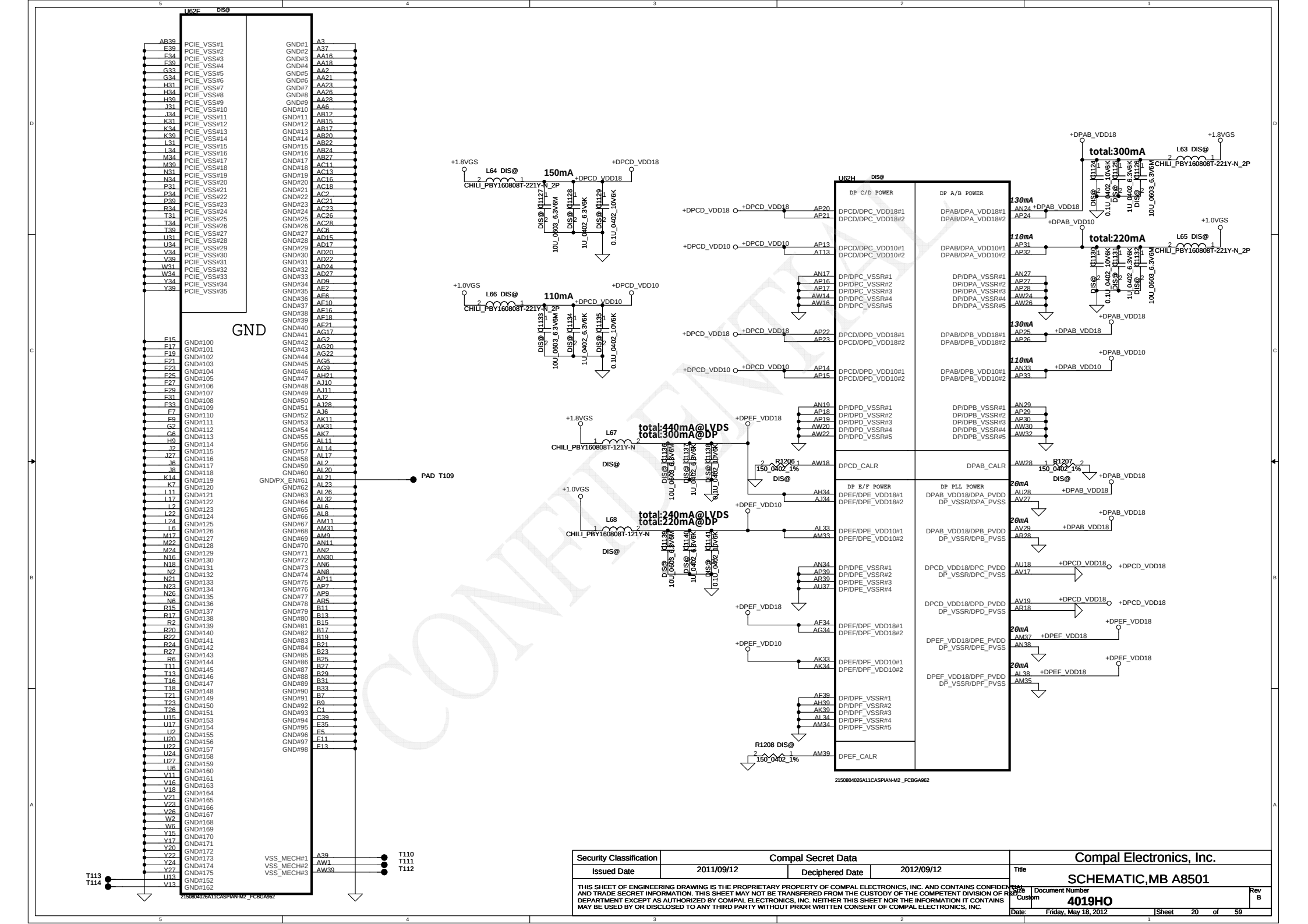
Date: Friday, May 18, 2012 Sheet 19 of 59

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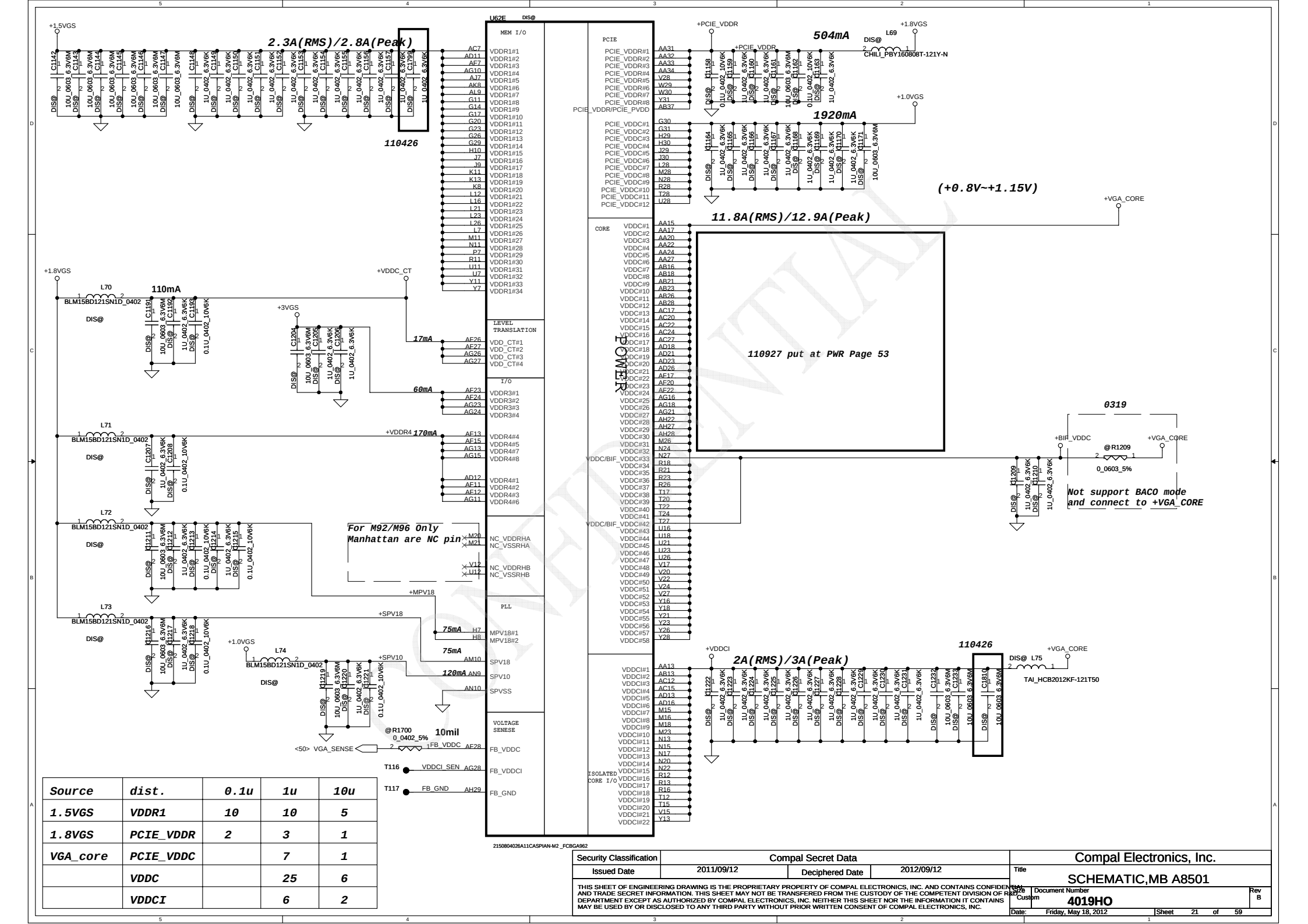
Date: Friday, May 18, 2012 Sheet 20 of 59




| Source | dist. | 0.1u | 1u | 10u |
|---|---|---|---|---|
| 1.5VGS | VDDR1 | 10 | 10 | 5 |
| 1.8VGS | PCIE_VDDR | 2 | 3 | 1 |
| VGA_core | PCIE_VDDC | | 7 | 1 |
| | VDDC | | 25 | 6 |
| | VDDCI | | 6 | 2 |



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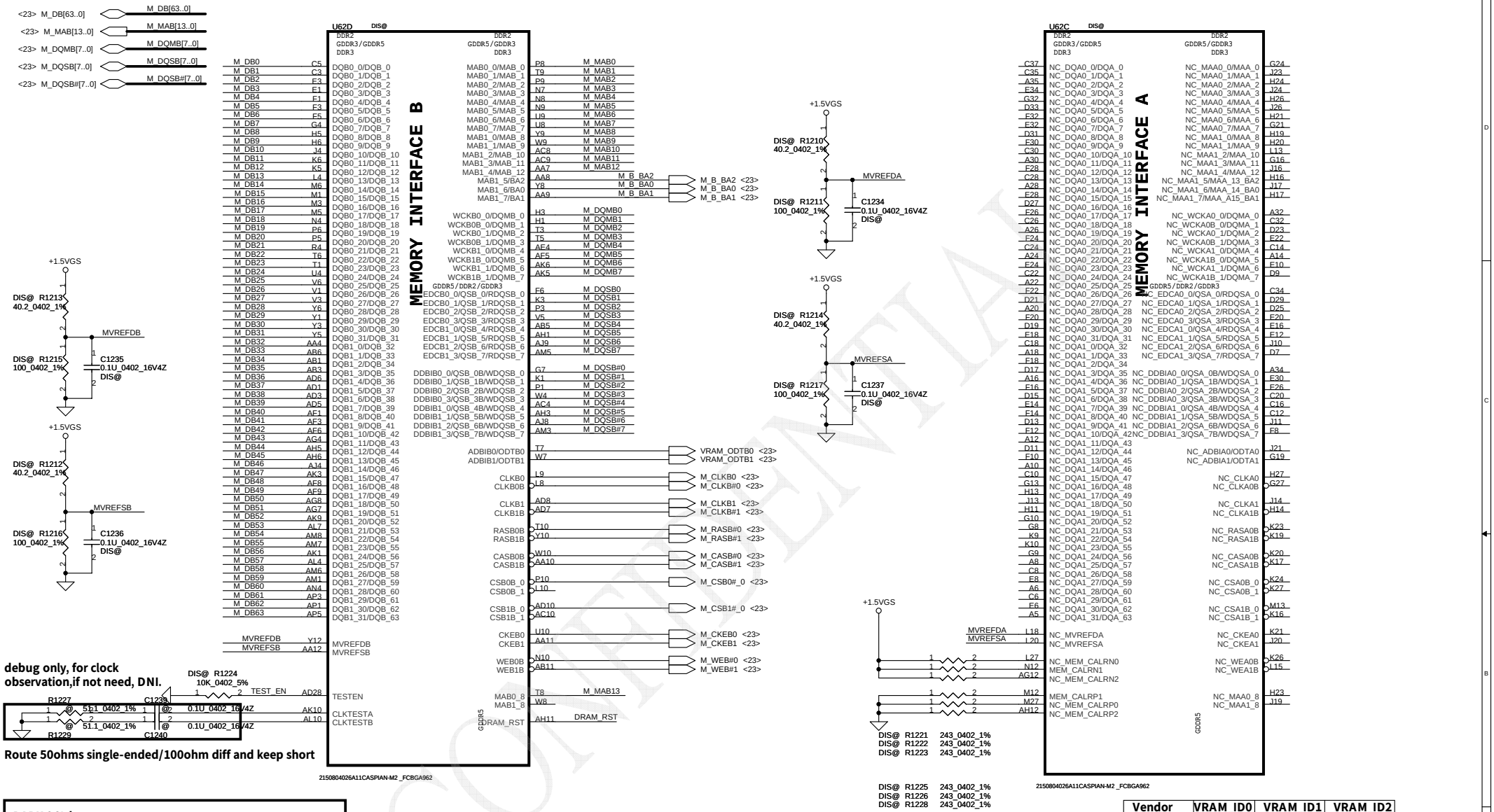


| Vendor | VRAM_ID0 | VRAM_ID1 | VRAM_ID2 |
|---|---|---|---|
| Hynix 512 | L | L | L |
| Hynix 1G | H | L | L |
| Samsung 512 | L | H | L |
| Samsung 1G | H | H | L |

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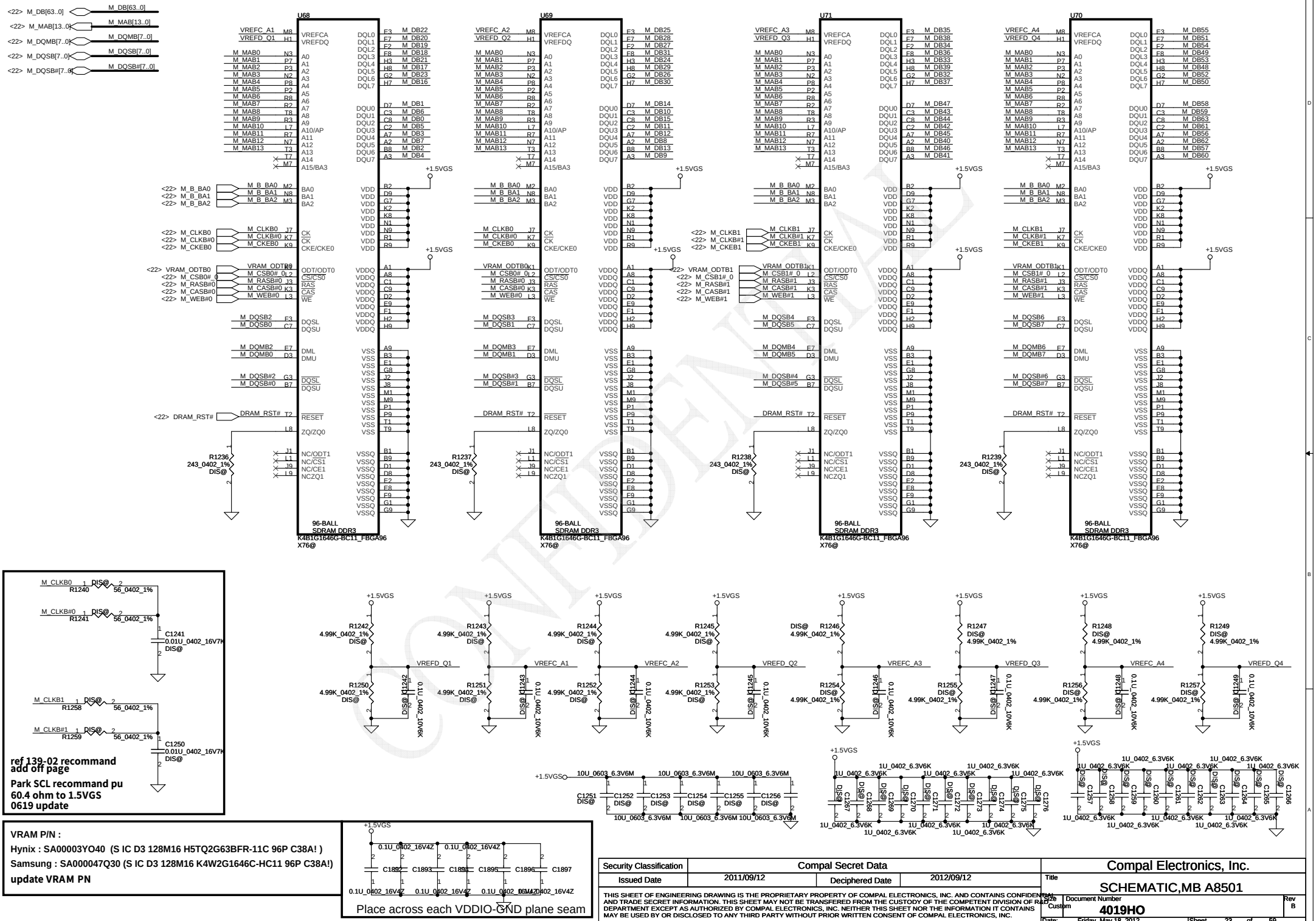
Size: Custom | Document Number: 4019HO | Rev: B

Date: Friday, May 18, 2012 | Sheet 22 of 59


M_DB[63..0]
M_MAB[13..0]
M_DQMB[7..0]
M_DQSB[7..0]
M_DQSB#[7..0]
U68
U69
U71
U70
96-BALL SDRAM DDR3
K4B1G1646G-BC11_FBGA96
X76@
+1.5VGS
R1236 243_0402_1% DIS@
R1237 243_0402_1% DIS@
R1238 243_0402_1% DIS@
R1239 243_0402_1% DIS@
R1240 56_0402_1%
R1241 56_0402_1%
R1258 56_0402_1%
R1259 56_0402_1%
C1241 0.01U_0402_16V7K DIS@
C1250 0.01U_0402_16V7K DIS@
ref 139-02 recommand add off page
Park SCL recommand pu 60.4 ohm to 1.5VGS 0619 update
VRAM P/N :
Hynix : SA00003YO40 (S IC D3 128M16 H5TQ2G63BFR-11C 96P C38A! )
Samsung : SA000047Q30 (S IC D3 128M16 K4W2G1646C-HC11 96P C38A!)
update VRAM PN
Place across each VDDIO-GND plane seam
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Size
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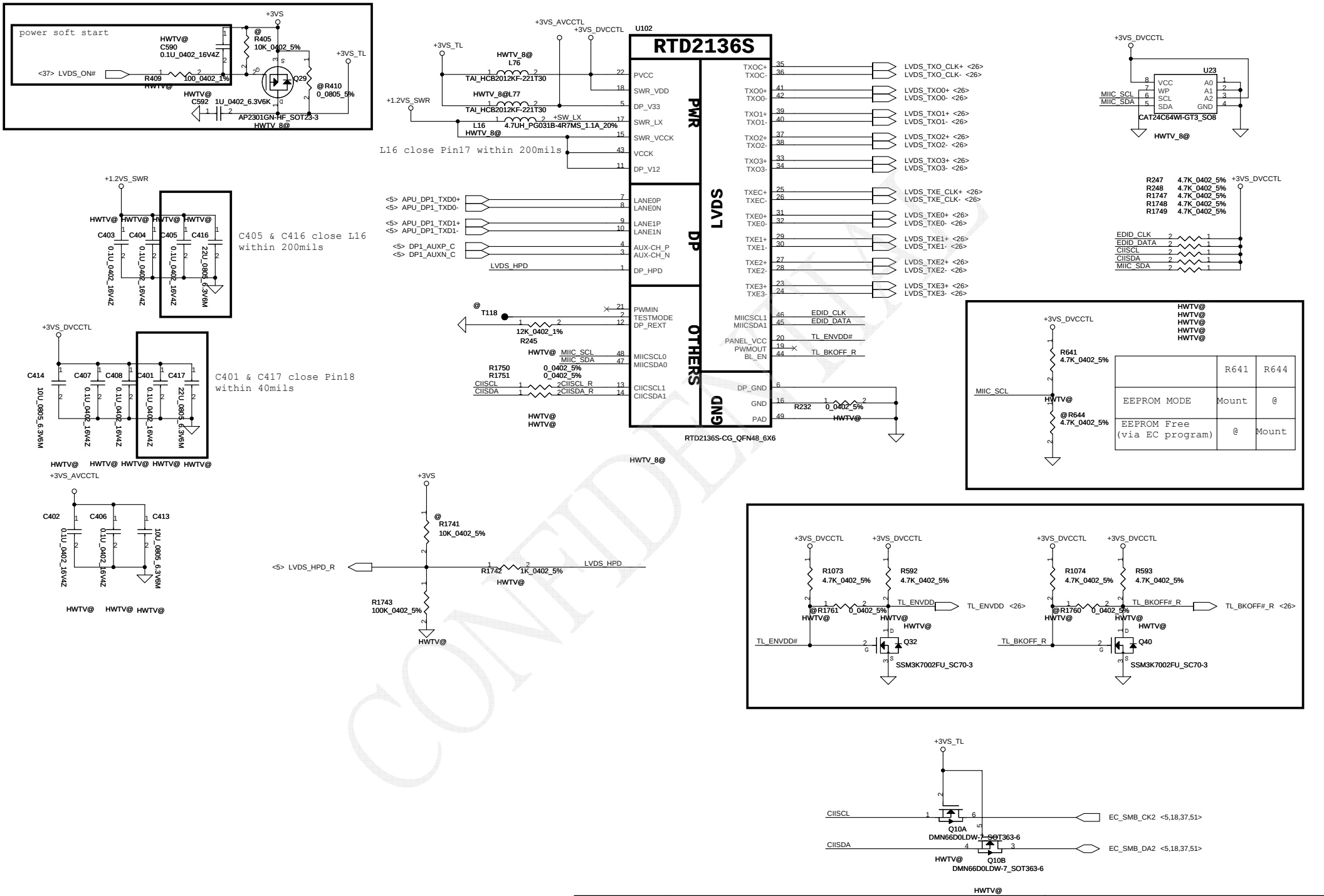
4019HO
Rev
B
Date:
Friday, May 18, 2012
Sheet
23
of
59



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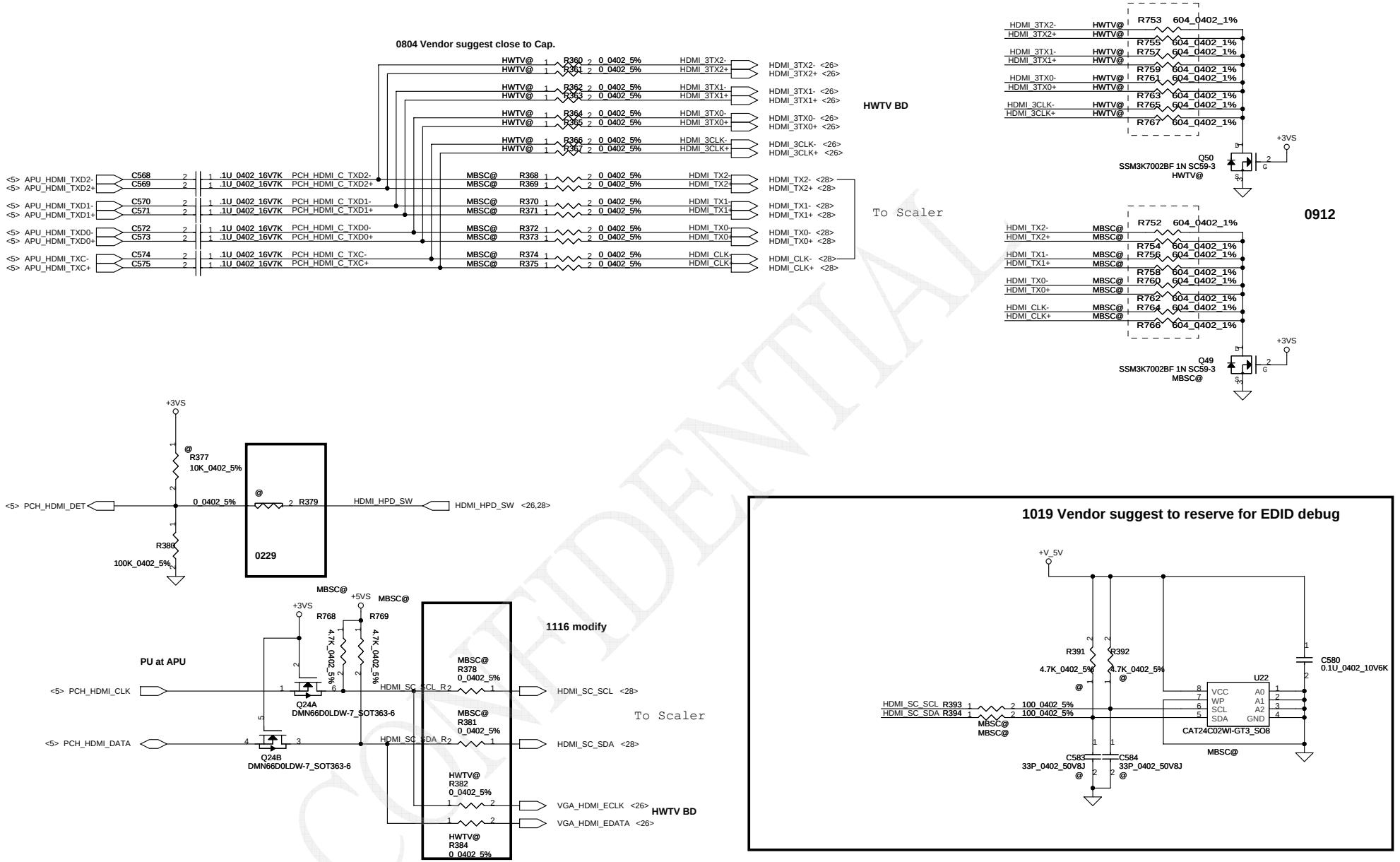
Size: Custom | Document Number: 4019HO | Rev: B

Date: Friday, May 18, 2012 | Sheet 24 of 59



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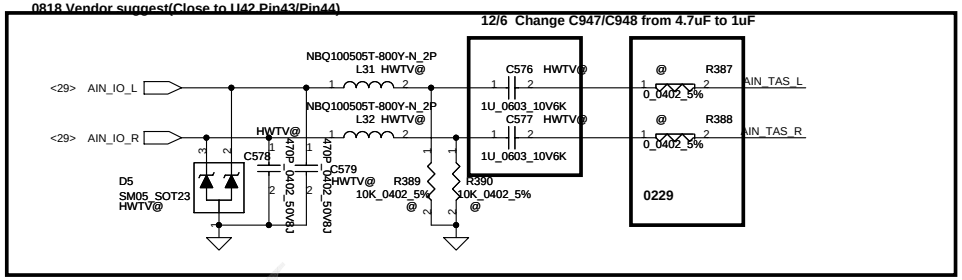
| Size | Document Number | Rev |
|---|---|---|
| Custom | 4019HO | B |

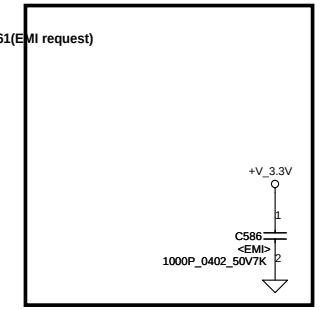
Date: Friday, May 18, 2012 | Sheet 25 of 59

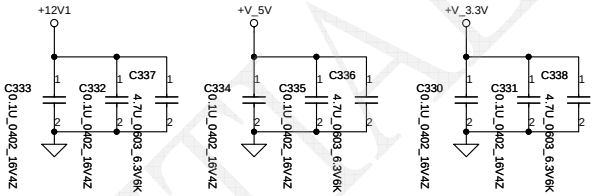
0818 Vendor suggest(Close to U42 Pin43/Pin44)

12/6 Change C947/C948 from 4.7uF to 1uF




10/27 Add C558~C561(EMI request)



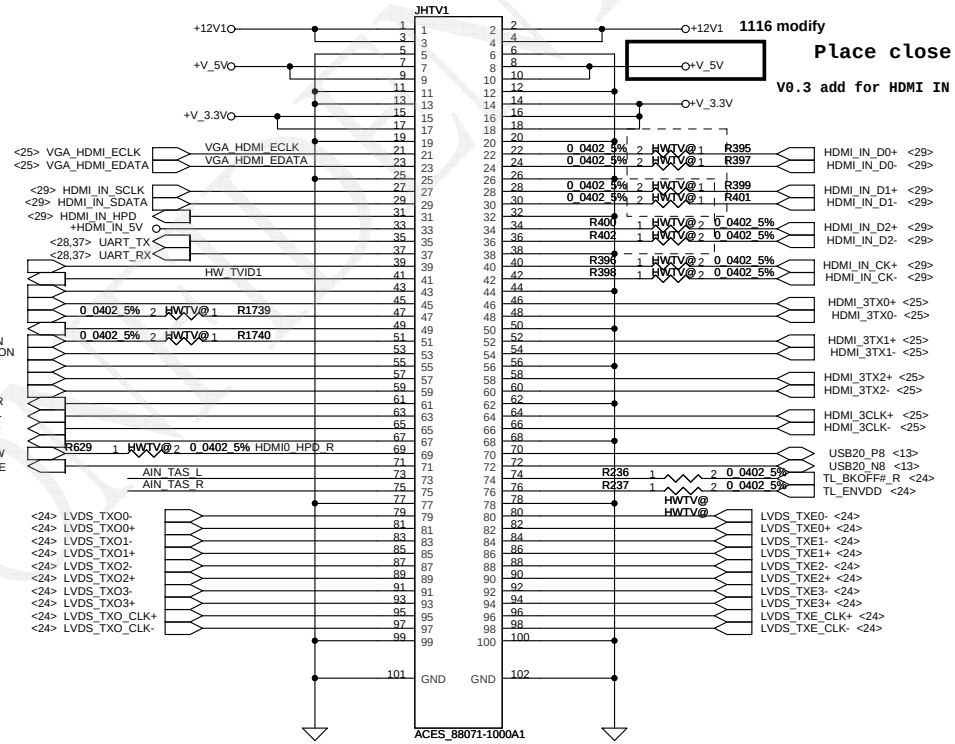

12/11 HWTV Pin define update

HWTV@ HWTV@ HWTV@ HWTV@ HWTV@ HWTV@ HWTV@ HWTV@ HWTV@

1116 modify

Place close to J4 side

V0.3 add for HDMI IN signal quality

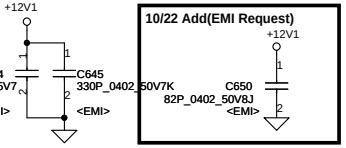



Source

HW_TV_ID1
GPIO_1
GPIO_2
TV_ON#

EC_HWTV_POWER_ON

10/22 Add(EMI Request)




0919 Change symbol of J4 from SP010011B00(88pin to 100pin)ACES_88079-1000A1



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| Size | Document Number | Rev |
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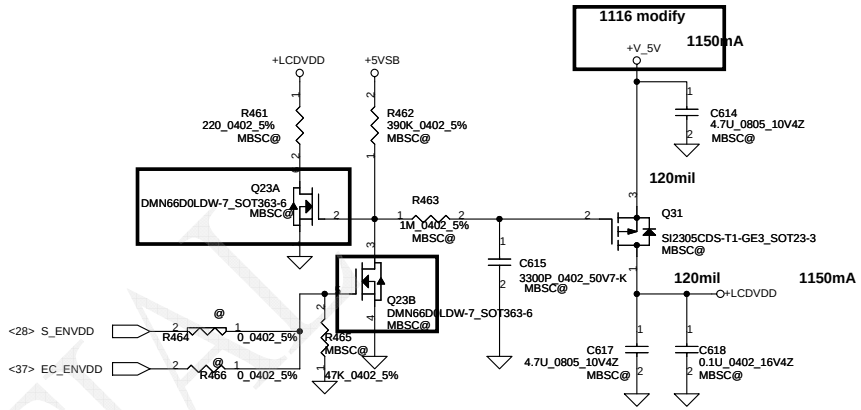
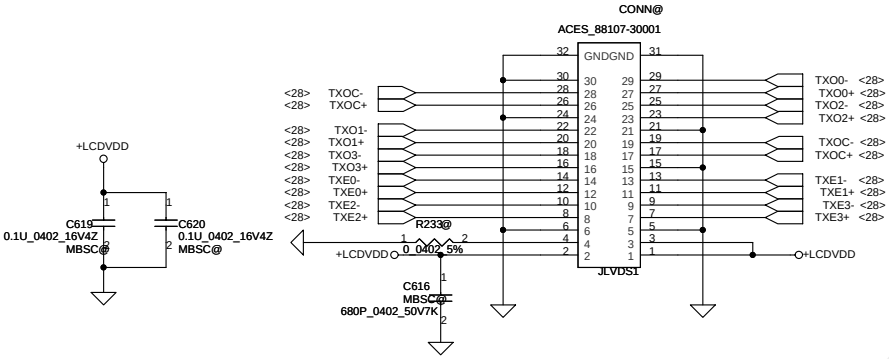
Date: Friday, May 18, 2012 Sheet 26 of 59

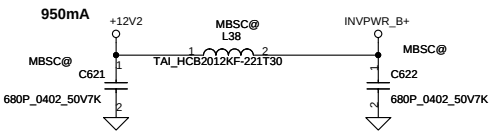
## LVDS POWER



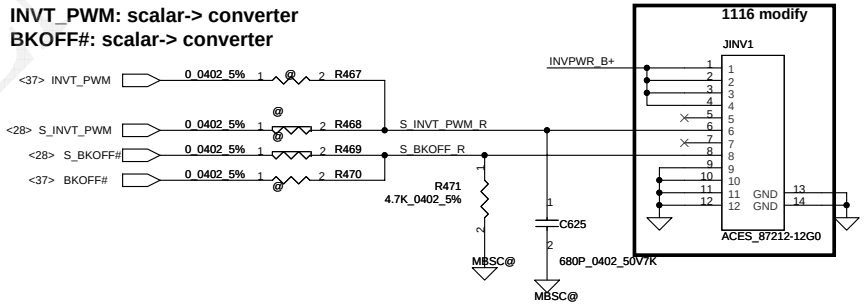

## LVDS CONN




## Converter




**INVT_PWM: scalar-> converter**
**BKOFF#: scalar-> converter**



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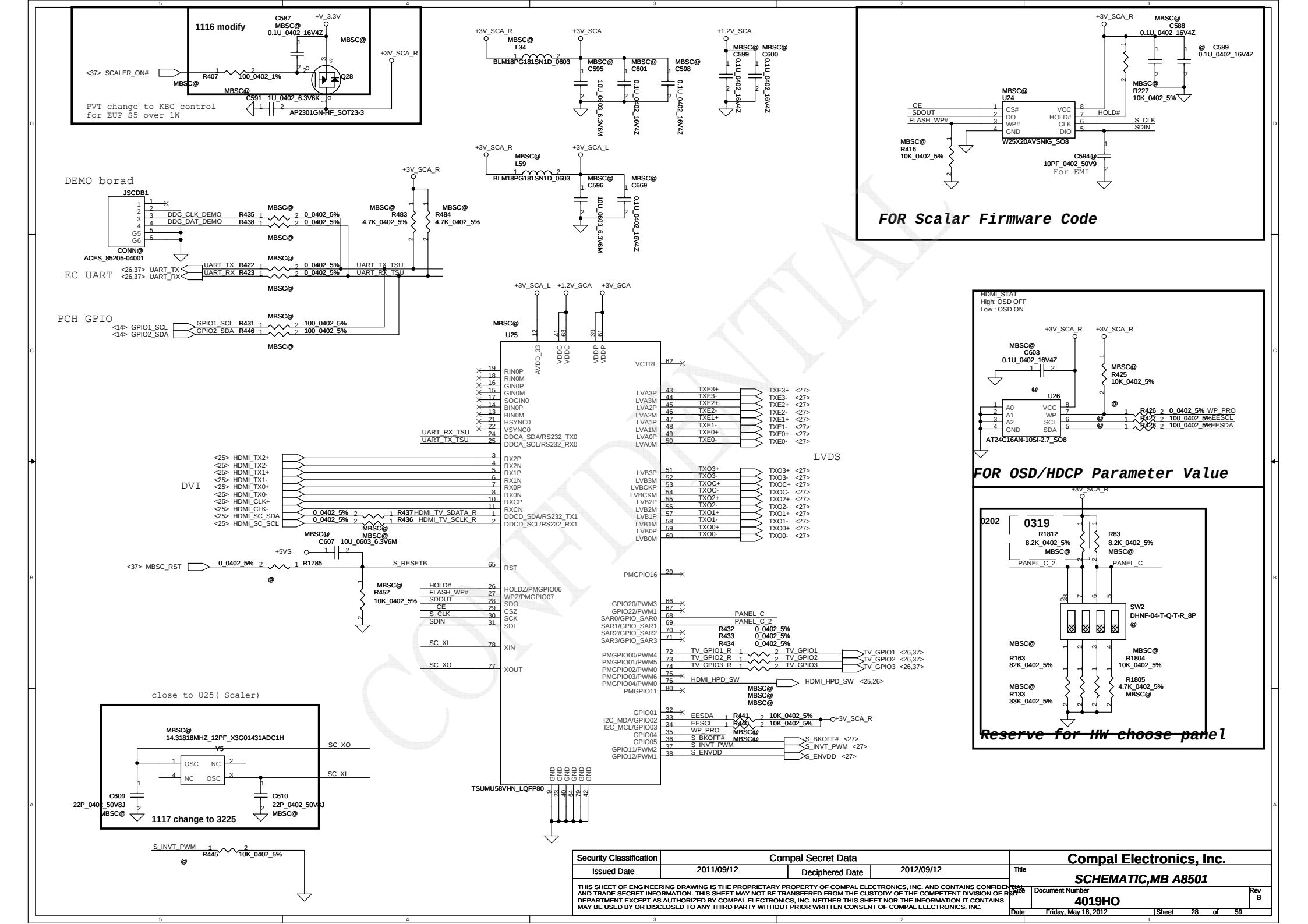
Size: | Document Number: **4019HO** | Rev: **B**

Date: Friday, May 18, 2012 | Sheet 27 of 59



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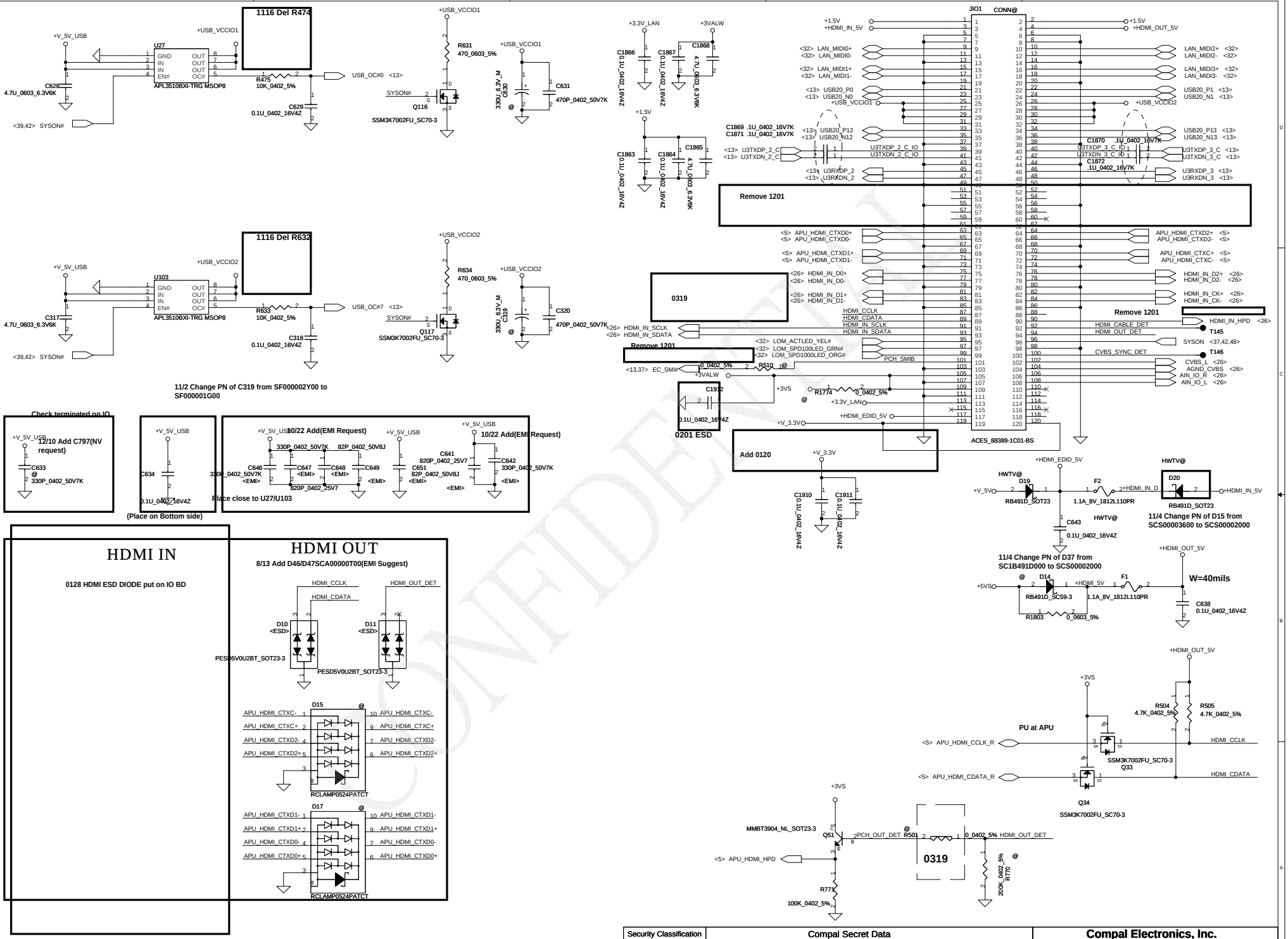
| Size | Document Number 4019HO | | Rev B |
| Date: Friday, May 18, 2012 | Sheet 28 of 59 | | |



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| Size | Document Number | Rev |
|---|---|---|
| Custom | 4019HO | B |

Date: Friday, May 18, 2012 Sheet 29 of 59

## HDD POWER Conn

+12VS 8/18 Add C918~C921

C652 0.1U_0402_16V4Z
C653 10U_0805_25V_K
C656 0.1U_0402_16V4Z
C657 10U_0805_6.3V6M

Layout Note:Place C918/C919/C920/C921 close to JWAFER1

## HDD

JWAF1
ACES_88290-044G
CONN@

12/6 Change footprint of JWAF1 from SP02000AO00 to SP02000EB00

## SATA HDD Conn.

JHDD1
TYCO_4-1775058-8
CONN@

<14> SATA_PTX_C_DRX_P0
<14> SATA_PTX_C_DRX_N0
<14> SATA_PRX_C_DTX_N0
<14> SATA_PRX_C_DTX_P0
C654 0.01U_0402_16V7K
C655 0.01U_0402_16V7K
SATA_DTX_PRX_N0
SATA_DTX_PRX_P0

## ODD POWER Conn

+12VS 10/29 Add C930/C931

C658 0.1U_0402_16V4Z
C659 10U_0805_25V_K
C662 0.1U_0402_16V4Z
C663 10U_0805_6.3V6M

10/28 Add C928/C929

Layout Note:Place C928/C929 close to JWAFER2

## ODD

JWAF2
ACES_88290-044G
CONN@

12/6 Change footprint of JWAF1 from SP02000AO00 to SP02000EB00

## SATA ODD Conn.

JODD1
TYCO_4-1775058-5
CONN@

<14> SATA_PTX_C_DRX_P1
<14> SATA_PTX_C_DRX_N1
<14> SATA_PRX_C_DTX_N1
<14> SATA_PRX_C_DTX_P1
C660 0.01U_0402_16V7K
C661 0.01U_0402_16V7K
SATA_DTX_PRX_N1
SATA_DTX_PRX_P1

+1.5VS
1U_0402_6.3V6K
C1857 10U_0805_6.3V6M
C1858
C1859
C1860 1000P_0402_50V7K
0.1U_0402_16V4Z

+3VS
1U_0402_6.3V6K
C1853 1000P_0402_50V7K
C1854
C1855
C1856
0.1U_0402_16V4Z
10U_0805_6.3V6M

## MINI SSD Conn.

JMINI3
BELLW_80003-1021
CONN@

<14> SATA_PRX_C_DTX_P2
<14> SATA_PRX_C_DTX_N2
C1861 0.01U_0402_16V7K
C316 0.01U_0402_16V7K
SATA_DTX_PRX_P0_RC
SATA_DTX_PRX_N0_RC
<14> SATA_PTX_C_DRX_N2
<14> SATA_PTX_C_DRX_P2

R1775 0_0402_5%
R1776 0_0402_5%
<33,37> E51TXD_P80DATA
<33,37> E51RXD_P80CLK
R1777 0_0402_5% @
<37> SSD_DET#

@ R1744 0_0402_5%
@ R1745 0_0402_5%
FCH_SMCLK0 <10,11,13,33>
FCH_SMDAT0 <10,11,13,33>



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| Size | Document Number | Rev |
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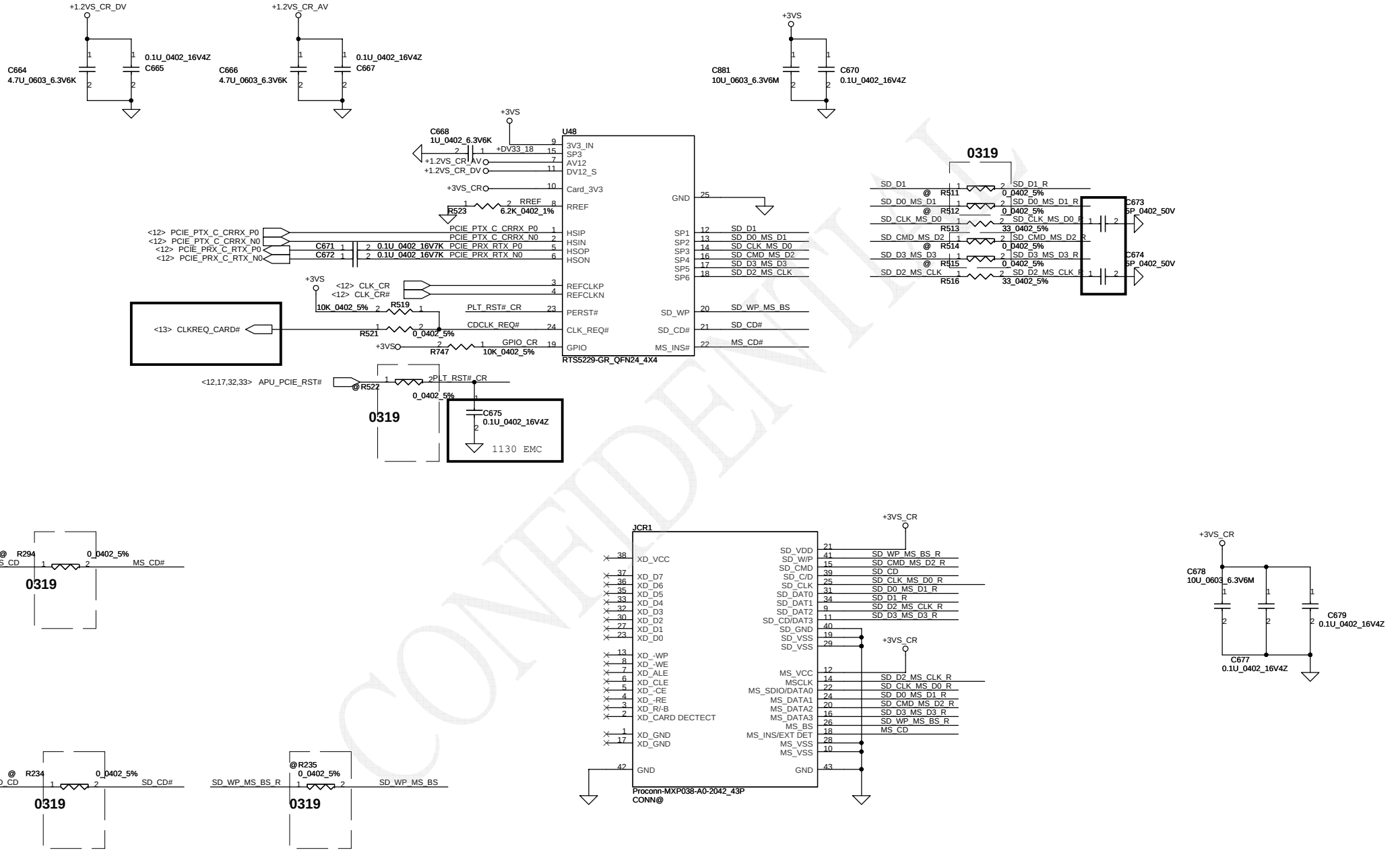
Date: Friday, May 18, 2012 Sheet 30 of 59



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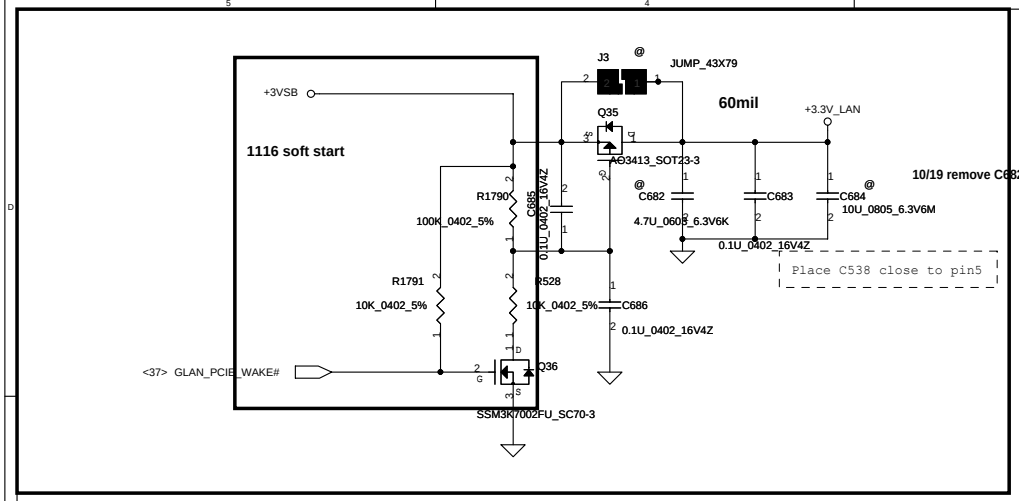
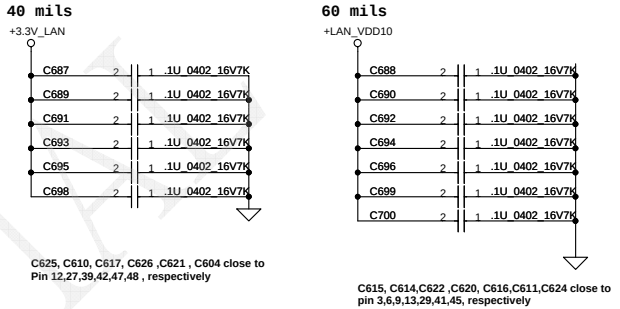
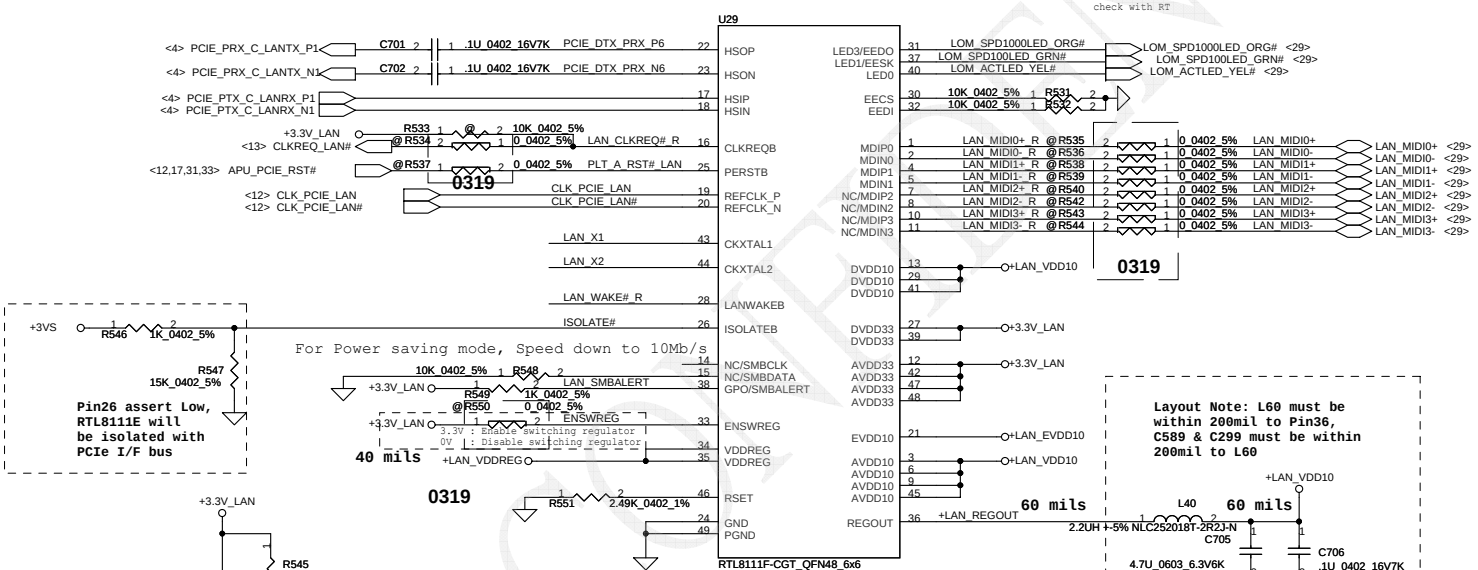
Size | Document Number: 4019HO | Rev: B

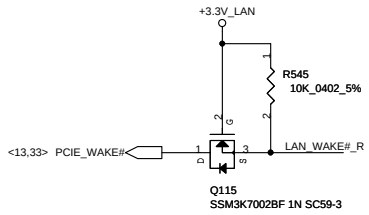
Date: Friday, May 18, 2012 | Sheet 31 of 59

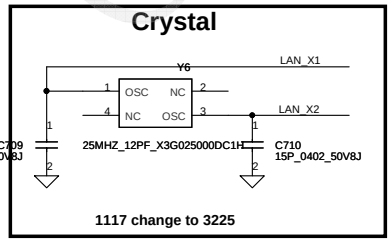



## Power ( Decoupling Cap. )

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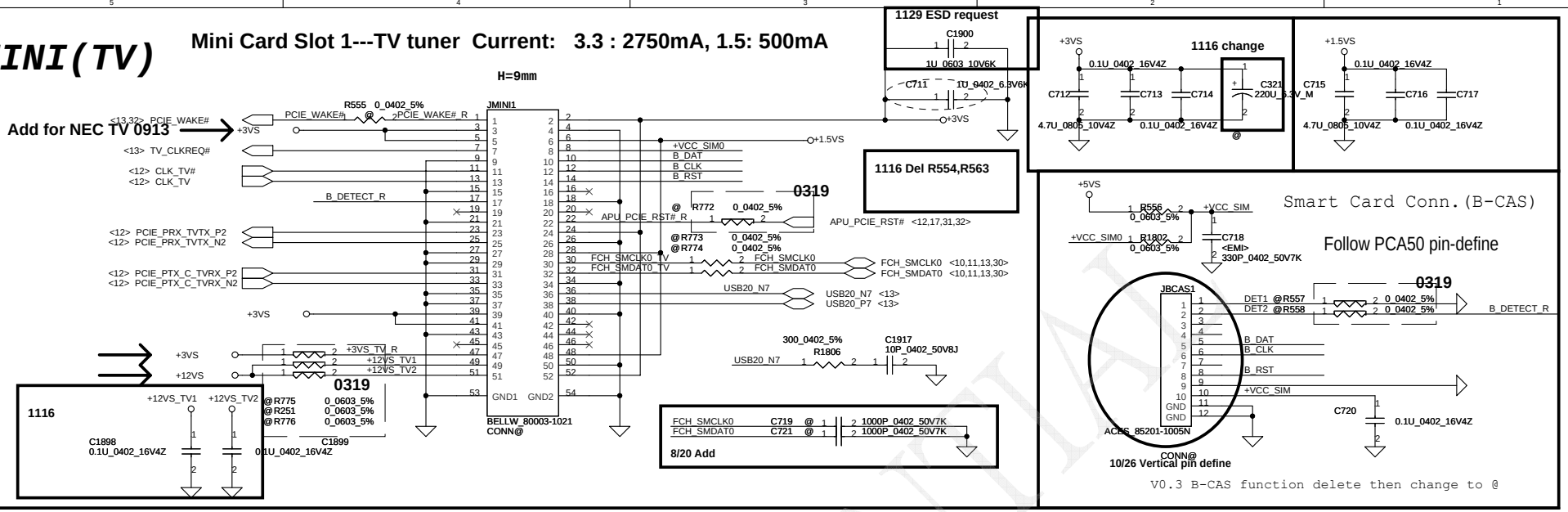
| Size: Custom | Document Number: 4019HO |
| Rev | B |
| Date: Friday, May 18, 2012 | Sheet 32 of 59 |

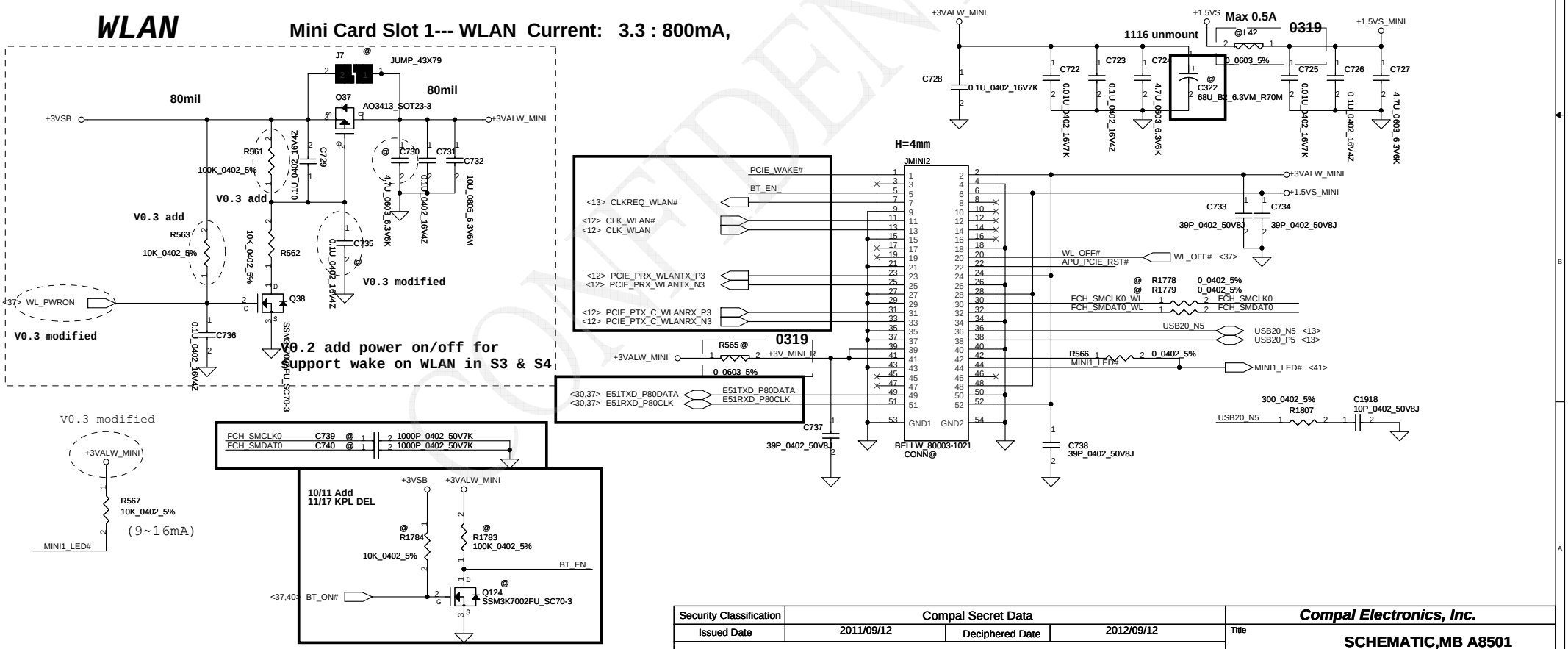
# MINI(TV)

## Mini Card Slot 1---TV tuner Current: 3.3 : 2750mA, 1.5: 500mA




# WLAN

## Mini Card Slot 1--- WLAN Current: 3.3 : 800mA,



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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/09/12 | Deciphered Date | 2012/09/12 |



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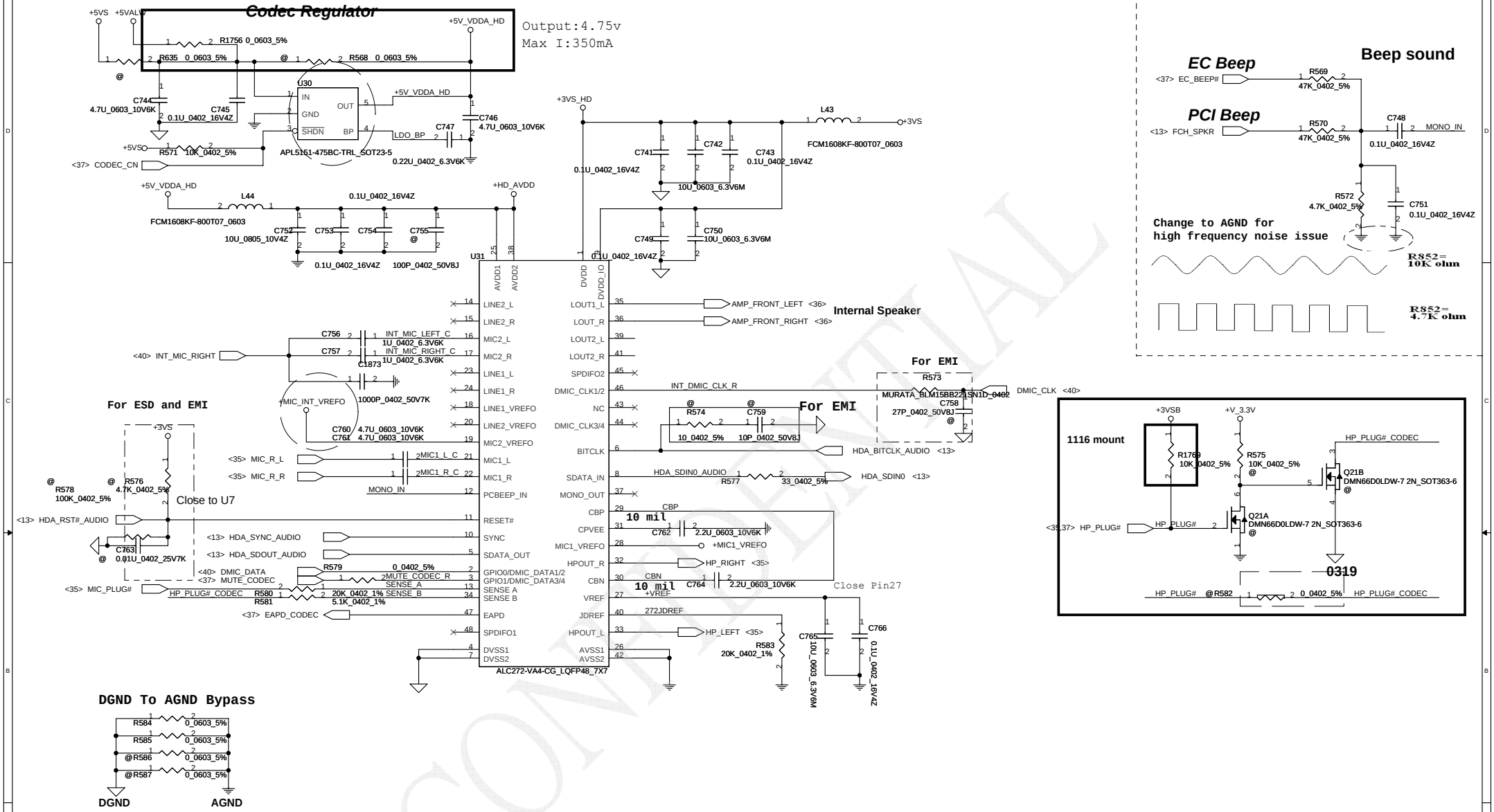
| Size | Document Number | Rev |
|---|---|---|
| Custom | 4019HO | B |

Date: Friday, May 18, 2012 | Sheet 33 of 59




| Sense Pin | Impedance | Codec Signals |
|---|---|---|
| SENSE A | 39.2K | LOUT2 (PIN 39, 41) |
| | 20K | MIC1 (PIN 21, 22) |
| | 10K | LINE1 (PIN 23, 24) |
| | 5.1K | LOUT1 (PIN 35,36) |
| SENSE B | 39.2K | LINE2 (PIN 14, 15) |
| | 20K | MIC2 (PIN 16, 17) |
| | 10K | |
| | 5.1K | HP-OUT (PIN 32,33) |



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Title: SCHEMATIC,MB A8501

Size: B | Document Number: 4019HO | Rev: B

Date: Friday, May 18, 2012 | Sheet 34 of 59

1026 Add Diode for MIC_L_VREFO
12/10 Change symbol of D24/D25 from SC1H751H010 to SCS00002G00

## EXT MIC IN

+MIC1_VREFO
D21 RB751V40_SC76-2
D22 RB751V40_SC76-2
R588 4.7K_0402_5%
R589 4.7K_0402_5%
<34> MIC_R_R
<34> MIC_R_L
MIC_R_R 1K_0402_5% R590 MIC_CEN_R
MIC_R_L 1K_0402_5% R591 MIC_LFE_L
L45 FBM-11-160808-601-T_0603
L46 FBM-11-160808-601-T_0603
Need 600 Ohm 500 mA
<34> MIC_PLUG#
MIC_PLUG#
MIC_CEN_R_1
MIC_LFE_L_1
JMIC1 CONN@
SINGATRON 2SJ-B351-S39
C767 330P_0402_50V7K
C768 330P_0402_50V7K
C769 .1U_0402_16V7K ESD request
C770 .1U_0402_16V7K ESD request
Add for EMC suggest

+PVDD
C323 1U_0402_6.3V4Z
U28 TS5A22364DRCR_SON10_3X3
<34> HP_RIGHT
<34> HP_LEFT
<37> HPOUT_SEL
INTSPK_CR+
INTSPK_CL+
HPOUT_SEL
NC1 NO1 NC2 NO2 IN1 IN2 V+ COM1 COM2 GND TP
HP_RIGHT_SW
HP_LEFT_SW
R636 100K_0402_5%

D23 PESD5V0U2BT_SOT23-3 <EMI>
MIC_PLUG#
HP_PLUG#
8/13 Change symbol of D29 to SCA00000T00(EMI Suggest)

D24 PESD5V0U2BT_SOT23-3 <EMI>
8/13 Change symbol of D28 to SCA00000T00(EMI Suggest)

## HP OUT

HP_RIGHT_SW
HP_LEFT_SW
R596 75_0603_1%
R597 75_0603_1%
HP_RIGHT_SW_R
HP_LEFT_SW_R
@R598 20K_0402_5%
@R599 20K_0402_5%
<34,37> HP_PLUG#
L49 FBM-11-160808-601-T_0603
L50 FBM-11-160808-601-T_0603
Need 600 Ohm 500 mA
HP_PLUG#
PR
PL
JHP1 CONN@
SINGATRON 2SJ-B351-S39
C771 330P_0402_50V7K
C772 330P_0402_50V7K
ESD request
C773 .1U_0402_16V7K

10/22 Change U56 from SA00001ZW00 to SA00004IS00

+PVDD
0.1U_0402_16V4Z
10U_0805_10V6K @ C774
C775 HWTV@
C776 HWTV@ 10U_0805_10V6K
U32 APA2176A
C777 2.2U_0603_16V6K HWTV@
HPAMP_CP+
HPAMP_CP-
CP+ CP- PVDD VDD LOUT ROUT /RSD NC /LSD PGND VSS CVSS GND
INTSPK_CL+_R
INTSPK_CR+_R
HWTV@ R1770 0_0402_5% INTSPK_CL+
HWTV@ R1771 0_0402_5% INTSPK_CR+
+PVDD
R600 @ 100K_0402_5%
C778 1U_0603_10V6K HWTV@
C779 1U_0603_10V6K HWTV@
<26> TV_HPOUT_L
<26> TV_HPOUT_R
TV_HPOUT_L_C
TV_HPOUT_R_C
HP_AMP_DOWN#
HP_AMP_DOWN# <37>
C780 2.2U_0603_16V6K HWTV@

8/13 Change symbol of D21 to SCA00000T00(EMI Suggest)
D26 PESD5V0U2BT_SOT23-3 <EMI>
PR
PL

8/13 Change symbol of D30 to SCA00000T00(EMI Suggest)
D25 PESD5V0U2BT_SOT23-3 <EMI>
MIC_CEN_R_1
MIC_LFE_L_1



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Title: SCHEMATIC,MB A8501

| Size | Document Number | Rev |
|---|---|---|
| Custom | 4019HO | B |

Date: Friday, May 18, 2012 Sheet 35 of 59

Vo=0.8(1+R606/R607)
Output:4.8V
Max I:7.5A

v0.2 modified
4.7U_0805_25V6K
C781
1/10 Change U33 to APL5610
U33
APL5610CI-TRG_SOT23-6
R601 10K_0402_5%
C782 1U_0402_6.3V4Z
Q39 FDS8884_SO8
R604 10K_0402_5%
R605 0_0402_5%
R606 12K_0402_1%
C785 47P_0402_50V8J
R607 2.4K_0402_1%
C786 22U_0805_6.3V6M
C783 C784 4.7U_0805_10V6K
L51 TAI_HCB2012KF-221T30
L52 TAI_HCB2012KF-221T30
120 mil
C787 C788 C789 C790 4.7U_0805_10V4Z
10U_0805_10V4Z 0.1U_0402_16V4Z
C791 1U_0402_6.3V4Z
+12V1 +V_5V +3VS +V_3.3V +PVDD

+5CH_AUDIO
R619 R620 0_0603_5%
+PVDD +V_3.3V

+V_3.3V
R602 R603 4.7K_0402_5%
<37,41> VOL_SCL
<37,41> VOL_SDA
Q26A Q26B DMN66D0LDW-7_SOT363-6
VOL_SCL_AMP
VOL_SDA_AMP

<37> EC_MUTE#
<26,37> TV_AMP_MUTE
R609 R610 0_0402_5%
MUTE_AMP
1116 Add
R1792 100K_0402_5%
U35
MUTEb
INPUT-R
SDb
INPUT-L
BYPASS
OUT-RP
OUT-RN
OUT-LP
OUT-LN
VOL_SCL
SE_BTLb/SDA
PVDD2 PVDD1 AVDD I2CVDD AGND EPAD
OUTPR OUTNR OUTPL OUTNL
VOL_SCL_AMP VOL_SDA_AMP
ALC106-GR_ESOP16

HWTV BD
Codec
Codec
HWTV BD

R611 300_0402_5%
ALC106_R
C795 ALC106_R_C 1U_0402_6.3V4Z
<37> AMP_POWER_DOWN#
AMP_POWER_DOWN#
ALC106_L
C797 ALC106_L_C 1U_0402_6.3V4Z
1116 Add
R1793 100K_0402_5%
+PVDD
R614 5.1K_0402_5%
C799 2.2U_0805_25V6K
R615 5.1K_0402_5%
R616 300_0402_5%
R617 0_0402_5%

+5CH_AUDIO
C805 C806 0.1U_0402_16V4Z
4.7U_0603_6.3V6K
10/17 Modify to GND

@R608 0_0603_5%
U34
OUTNR_SW
OUTPR_SW
AV_AUDIO_SEL# <37>
G3205P71U_MSOP10
@R612 0_0603_5%
10/17 Modify to GND

v0.2 delete U34,U36; stuff R8579~R8582

@R613 0_0603_5%
U36
OUTPL_SW
OUTNL_SW
AV_AUDIO_SEL# <37>
G3205P71U_MSOP10
@R618 0_0603_5%
10/17 Modify to GND

<34> AMP_FRONT_RIGHT
<26> TV_AMPOUT_R
<34> AMP_FRONT_LEFT
<26> TV_AMPOUT_L
C794 C793 C796 C798 HWTV@ 4.7U_0603_6.3V6K 1U_0402_6.3V4Z
AMP_FRONT_R_SW
TV_AMPOUT_R_SW
AMP_FRONT_L_SW
TV_AMPOUT_L_SW
<37> AMPIN_SEL
AMPIN_SEL
U104
TS5A22364DRCR_SON10_3X3
ALC106_R
ALC106_L
R637 100K_0402_5%
+PVDD
C324 1U_0402_6.3V4Z

OUTNR_SW
OUTPR_SW
OUTPL_SW
OUTNL_SW
L53 L54 L55 L56 CHILI_PBY160808T-121Y-N
3A/120ohm/100MHz
SPKR- SPKR+ SPKL+ SPKL-
C801 C802 C803 C804 C807 C808 C809 C810
470P_0603_50V8J 1000P_0603_50V7K
R621 R622 R623 R624 22_1206_5%

ACES_87212-04G0
JSPK1
SPKL+ SPKL- SPKR- SPKR+ GND GND
CONN@
D27 D28 <EMI> @
PESD5V0U2BT_SOT23-3



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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/09/12 | Deciphered Date | 2012/09/12 |



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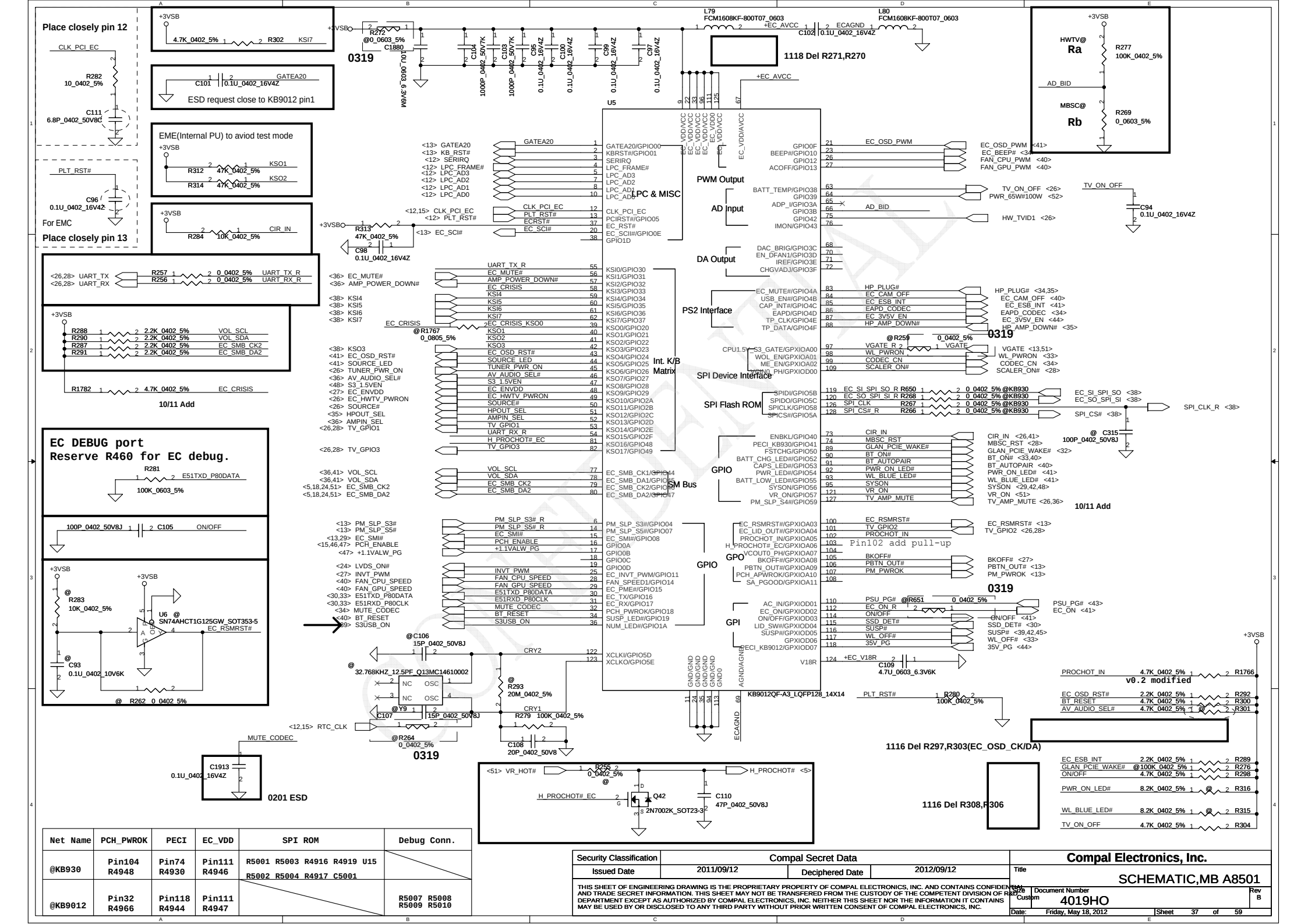
Title: SCHEMATIC,MB A8501

| Size | Document Number | Rev |
|---|---|---|
| Custom | 4019HO | B |

Date: Friday, May 18, 2012 Sheet 36 of 59




| Net Name | PCH_PWROK | PECI | EC_VDD | SPI ROM | Debug Conn. |
|---|---|---|---|---|---|
| @KB930 | Pin104<br>R4948 | Pin74<br>R4930 | Pin111<br>R4946 | R5001 R5003 R4916 R4919 U15<br>R5002 R5004 R4917 C5001 | |
| @KB9012 | Pin32<br>R4966 | Pin118<br>R4944 | Pin111<br>R4947 | | R5007 R5008<br>R5009 R5010 |

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|---|---|---|---|
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| Issued Date | 2011/09/12 | Deciphered Date | 2012/09/12 |



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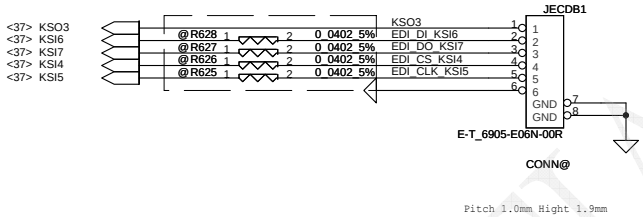
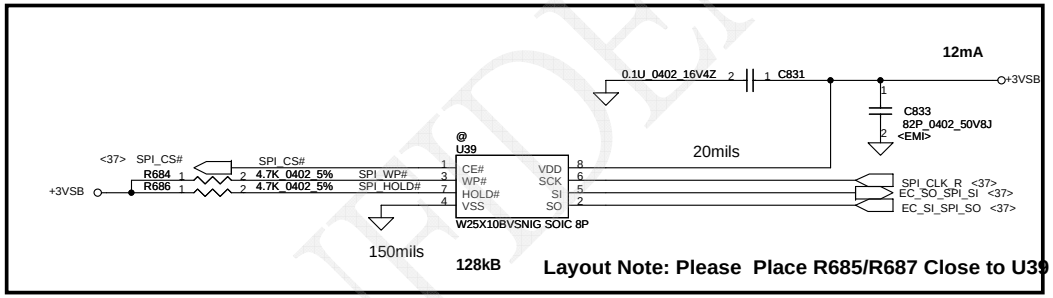
| Title | SCHEMATIC,MB A8501 | | |
| Size: Custom | Document Number: 4019HO | | Rev: B |
| Date: Friday, May 18, 2012 | Sheet 37 of 59 | | |

# EC DEBUG CONNECTOR

0319



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| Security Classification | Compal Secret Data | | |
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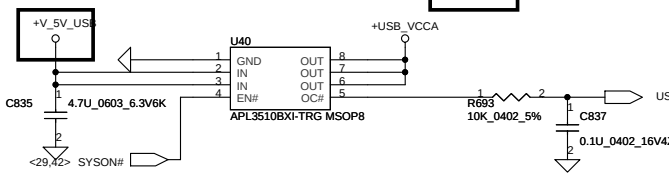
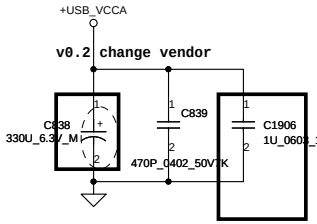
Title: SCHEMATIC,MB A8501

| Size | Document Number | Rev |
|---|---|---|
| Custom | 4019HO | B |

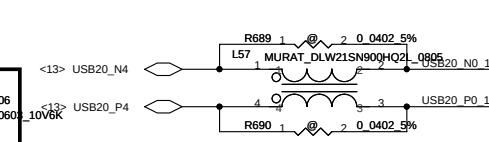
Date: Friday, May 18, 2012 Sheet 38 of 59

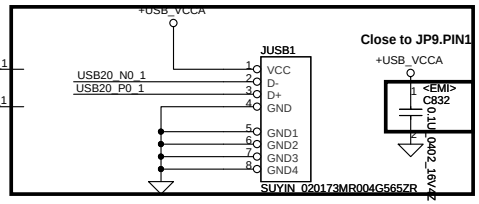
1116 Del R691



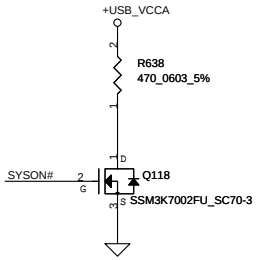



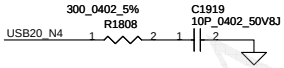

01/28 Add for ESD close C839

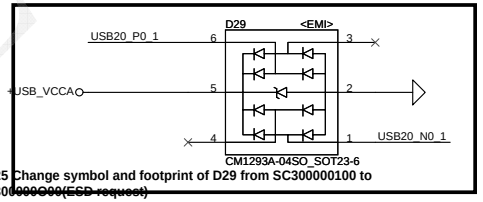


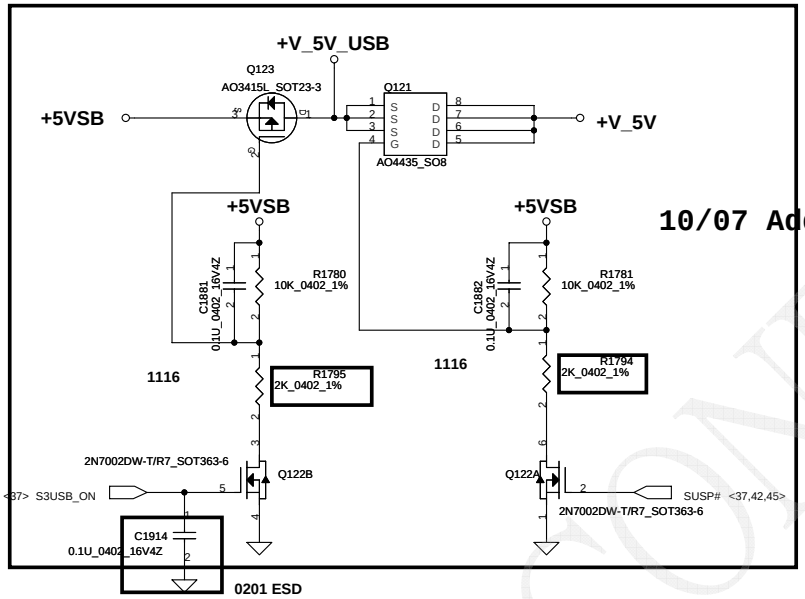

CONN@



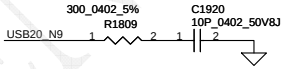



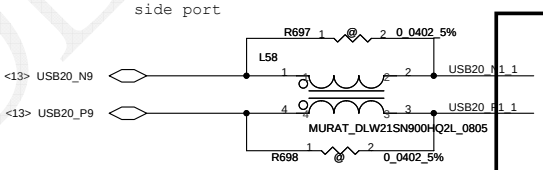

10/25 Change symbol and footprint of D29 from SC300000100 to SC300000O00(ESD request)

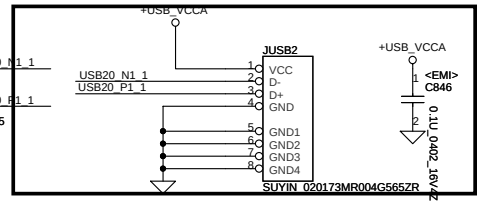



0201 ESD

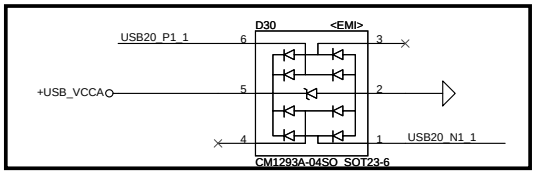



side port

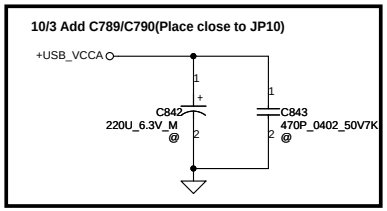


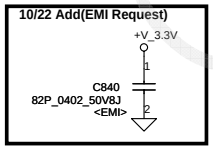



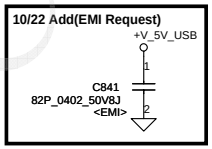

CONN@

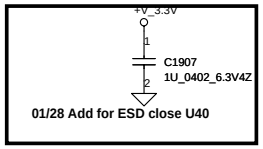



10/25 Change symbol and footprint of D30 from SC300000100 to SC300000O00(ESD request)




01/28 Add for ESD close U40



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
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Title: SCHEMATIC,MB A8501

| Size | Document Number | Rev |
|---|---|---|
| Custom | 4019HO | B |

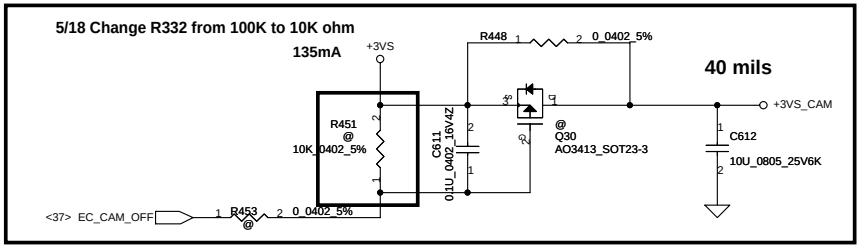
Date: Friday, May 18, 2012 | Sheet 39 of 59

# WebCam+Digital Mic

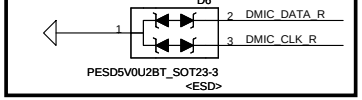
5/18 Change R332 from 100K to 10K ohm

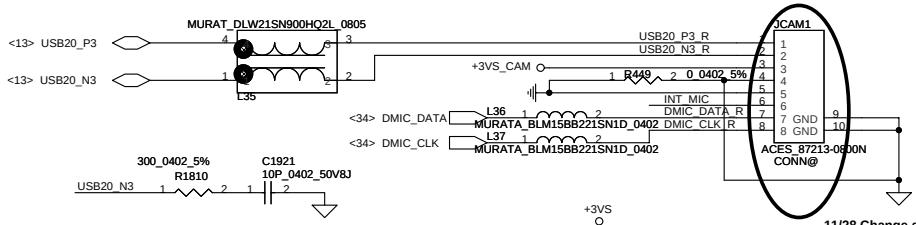
135mA

40 mils

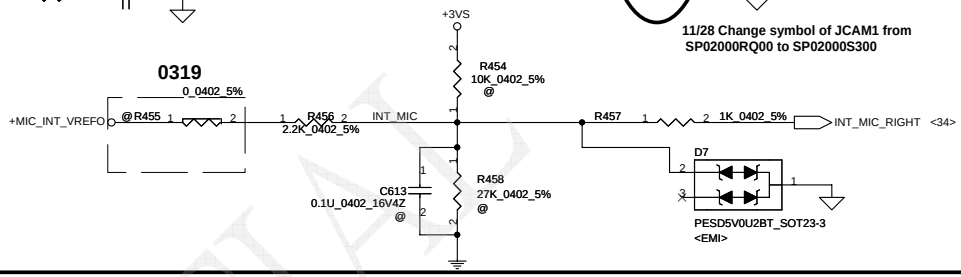



10/27 Add D49(ESD request)



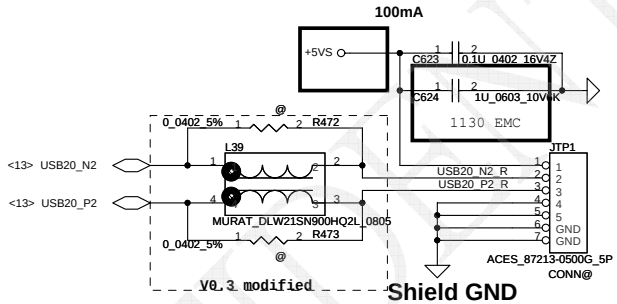



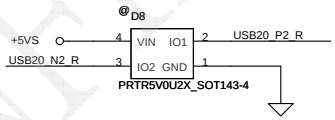

11/28 Change symbol of JCAM1 from SP02000RQ00 to SP02000S300



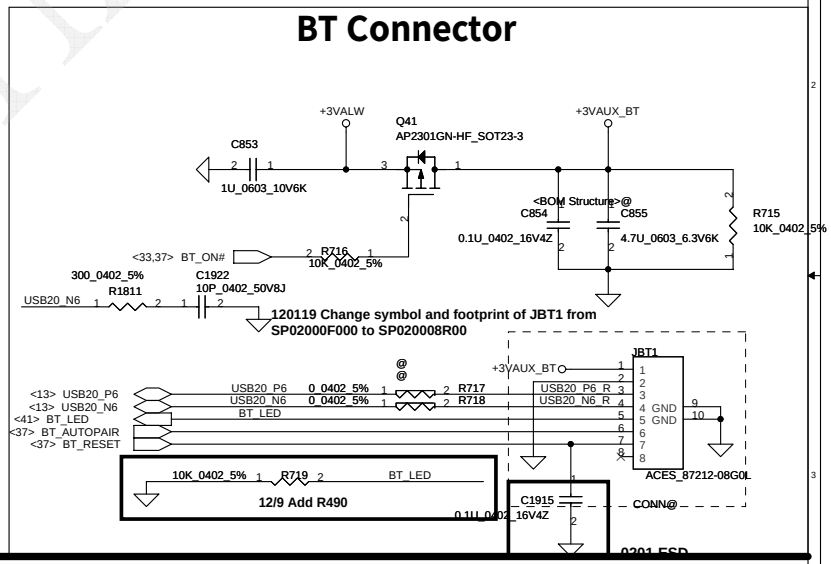

# Touch Panel

PVT change from alw to vs for EUP.

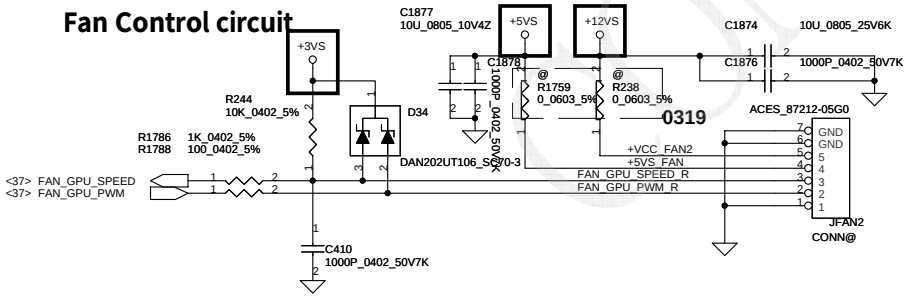


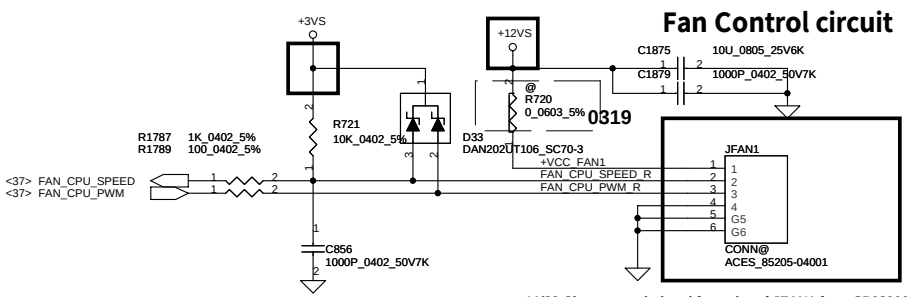




# BT Connector




# Fan Control circuit




11/29 Change symbol and footprint of JFAN1 from SP02000U900 to SP020008X00



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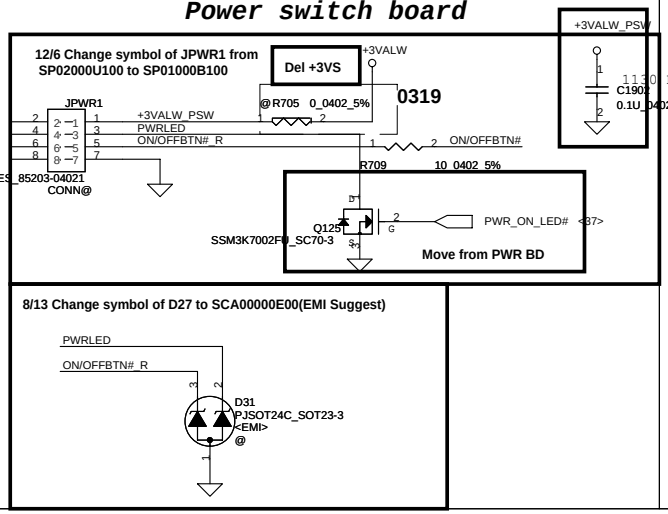
Title: SCHEMATIC,MB A8501

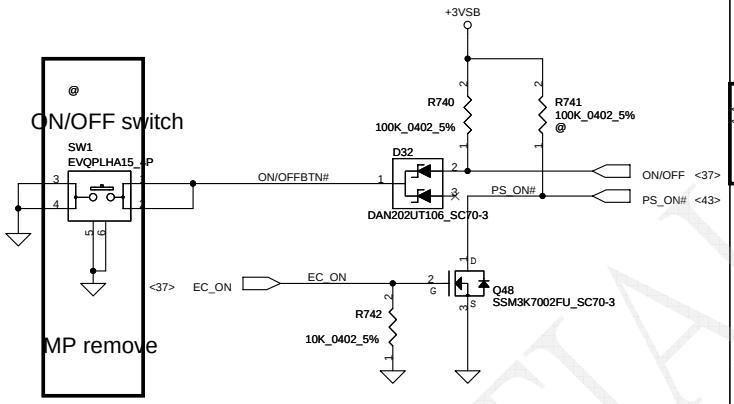
| Size | Document Number | Rev |
|---|---|---|
| Custom | 4019HO | B |

Date: Friday, May 18, 2012 Sheet 40 of 59

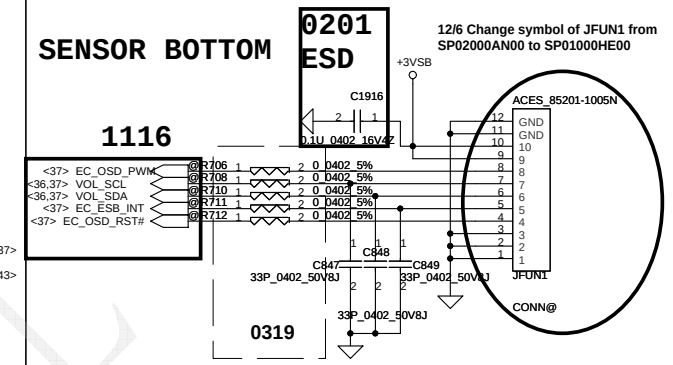
## Power switch board



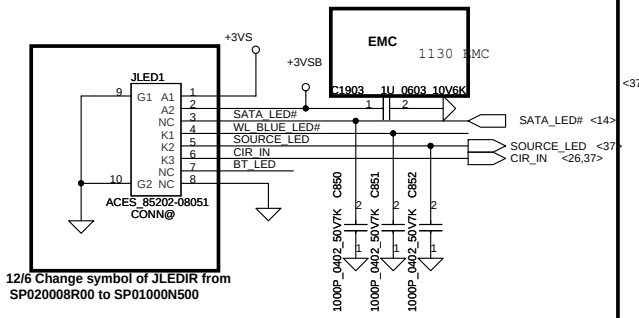

## Power Button

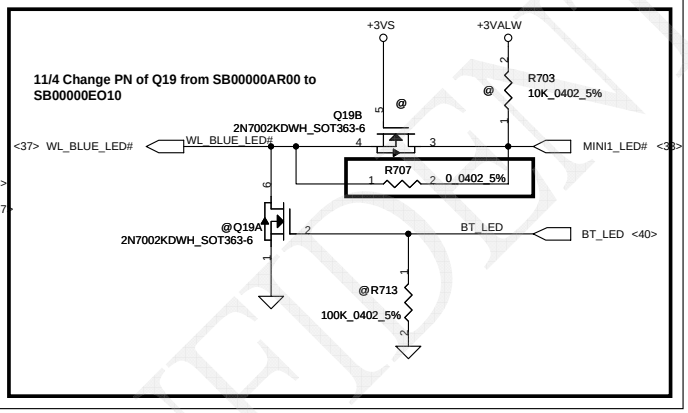



## SENSOR BOTTOM




## LED board conn.



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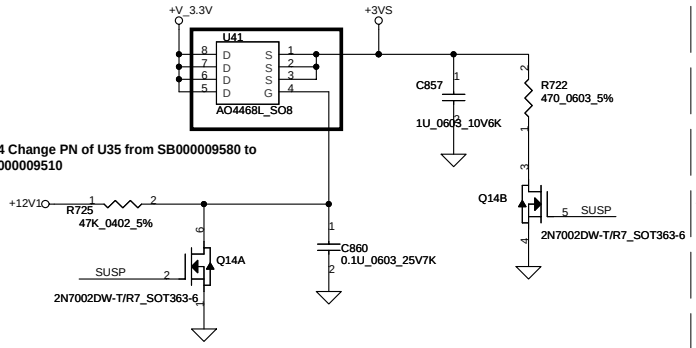
Title: **SCHEMATIC,MB A8501**

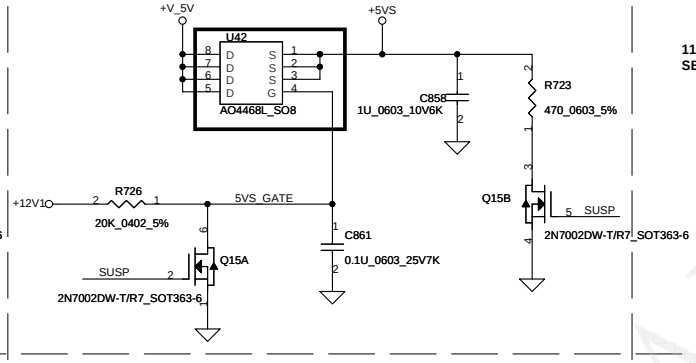
| Size | Document Number | Rev |
|---|---|---|
| Custom | 4019HO | B |
| Date: Friday, May 18, 2012 | Sheet 41 of 59 | |

## +V_3.3V TO +3VS



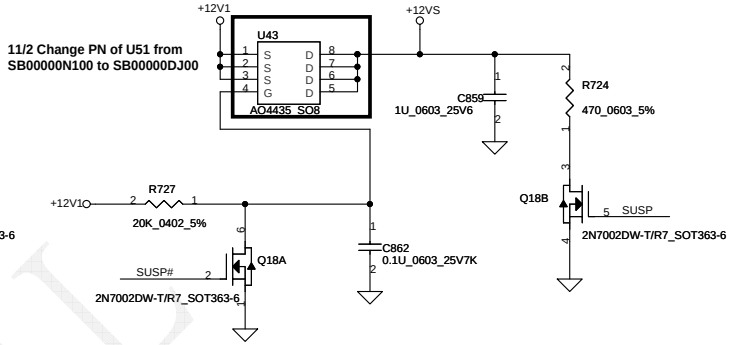

## +V_5V TO +5VS

11/4 Change PN of U34 from SB000009580 to SB000009510

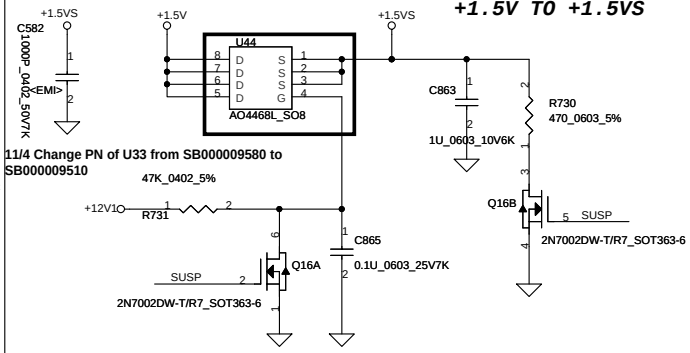



## +12V1 TO +12VS

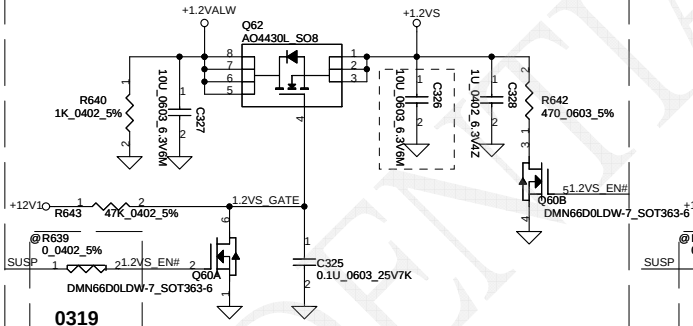
11/2 Change PN of U51 from SB00000N100 to SB00000DJ00




## +1.5V TO +1.5VS

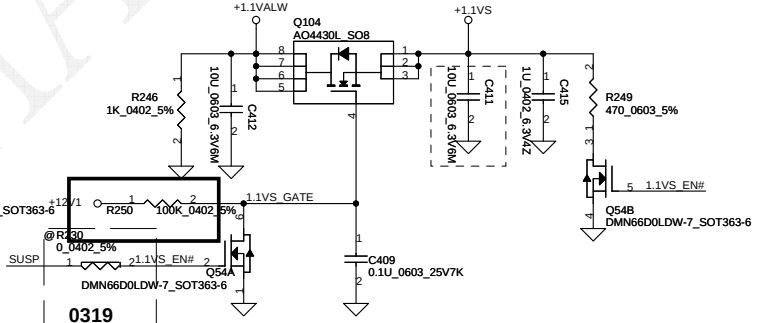



## +1.2VALW TO +1.2VS



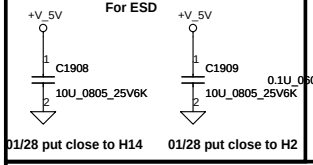

0319

## +1.1VALW TO +1.1VS

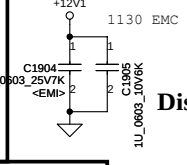



0319

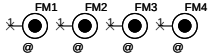
For ESD



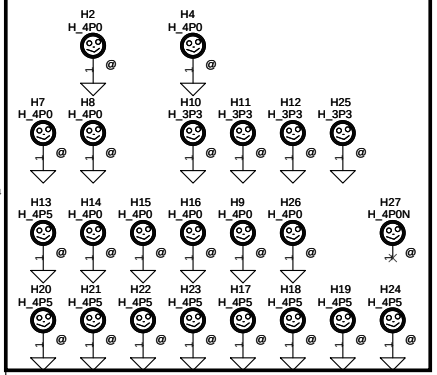

01/28 put close to H14 01/28 put close to H2



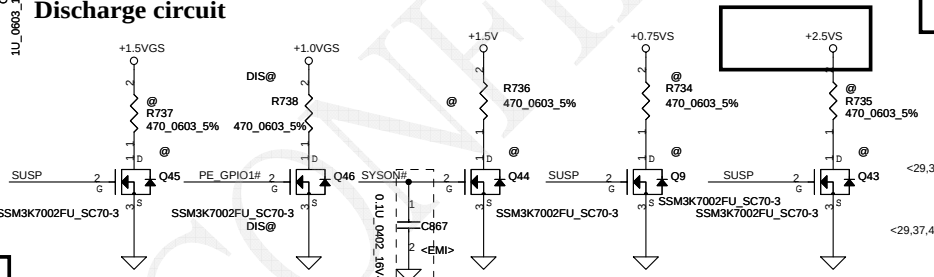

## NON-PDH




## Screw

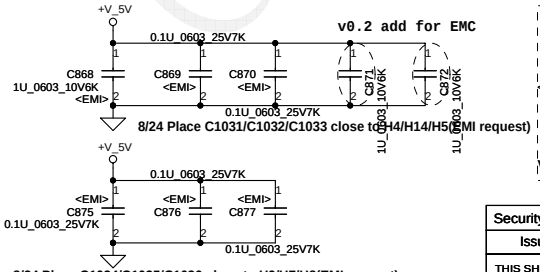


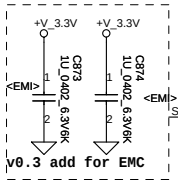

## Discharge circuit

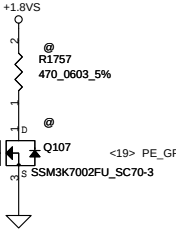


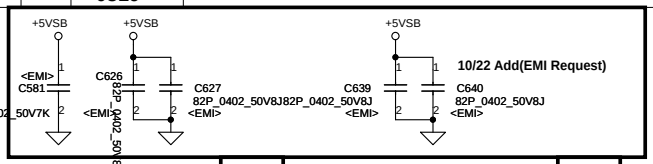

V0.3 add for EMC

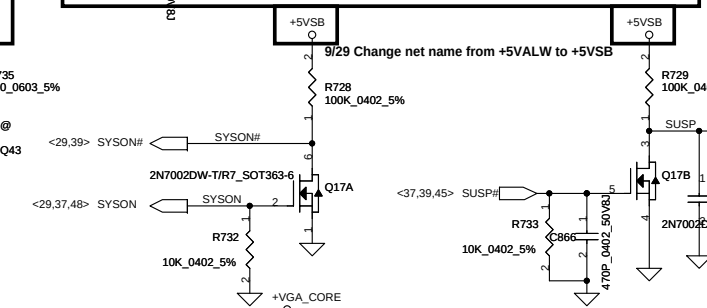
8/24 Add C1031~C1036

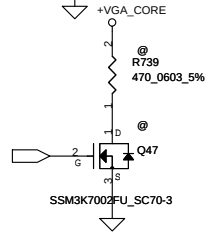


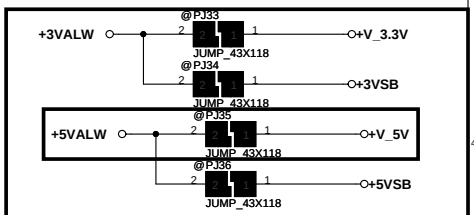

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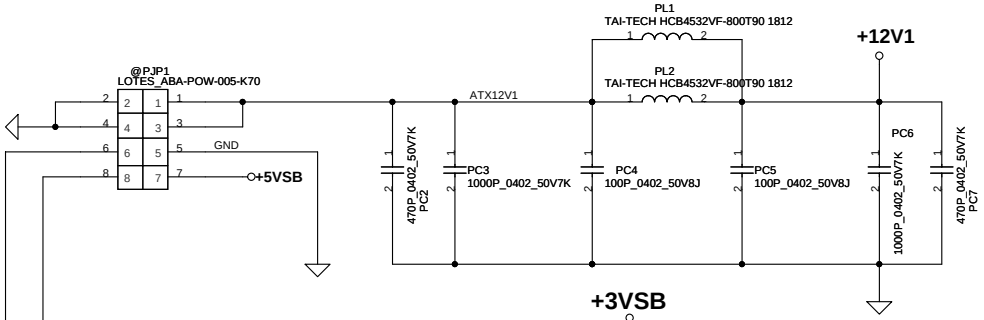
Title: SCHEMATIC,MB A8501

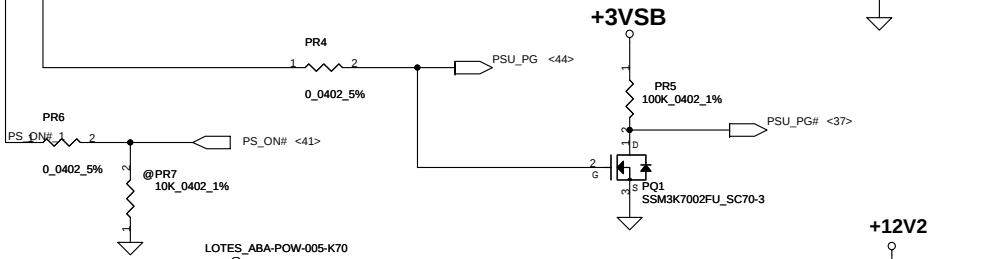
Size: Custom | Document Number: 4019HO | Rev: B

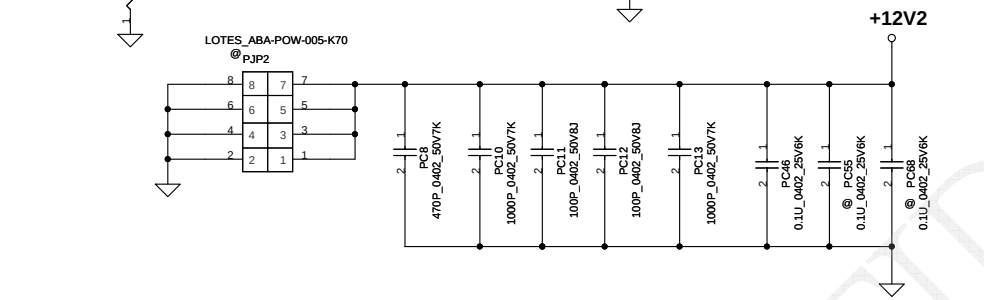
Date: Friday, May 18, 2012 | Sheet 42 of 59

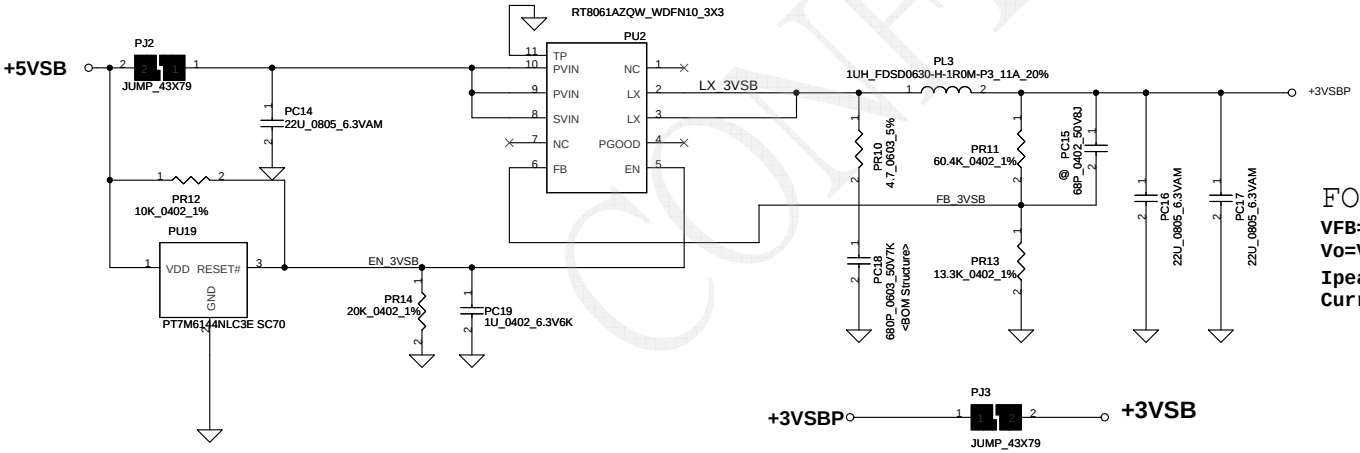
**PH1 under CPU botten side :**

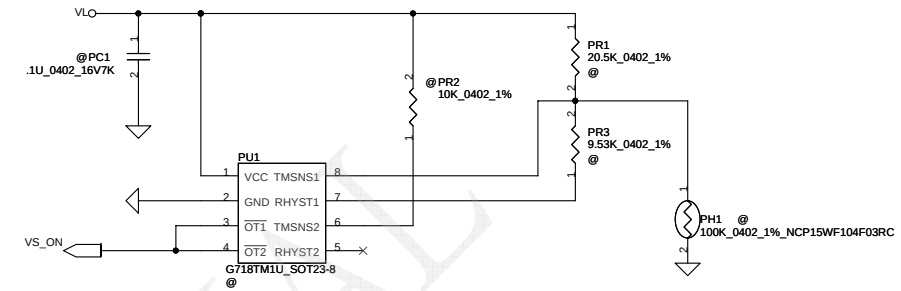
CPU thermal protection at 92 degree C
Recovery at 57 degree C

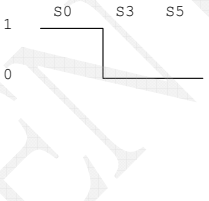


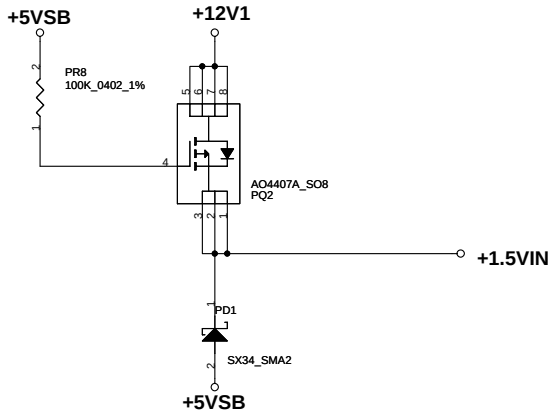



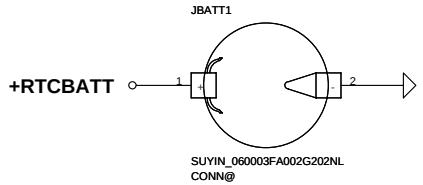




FOR EC suspend
**VFB=0.6V**
**Vo=VFB*(1+PR7/PR9)=3.318 V**
**Ipeak=0.926A, Imax=0.7*0.755=0.648A**
**Current limit >4A**



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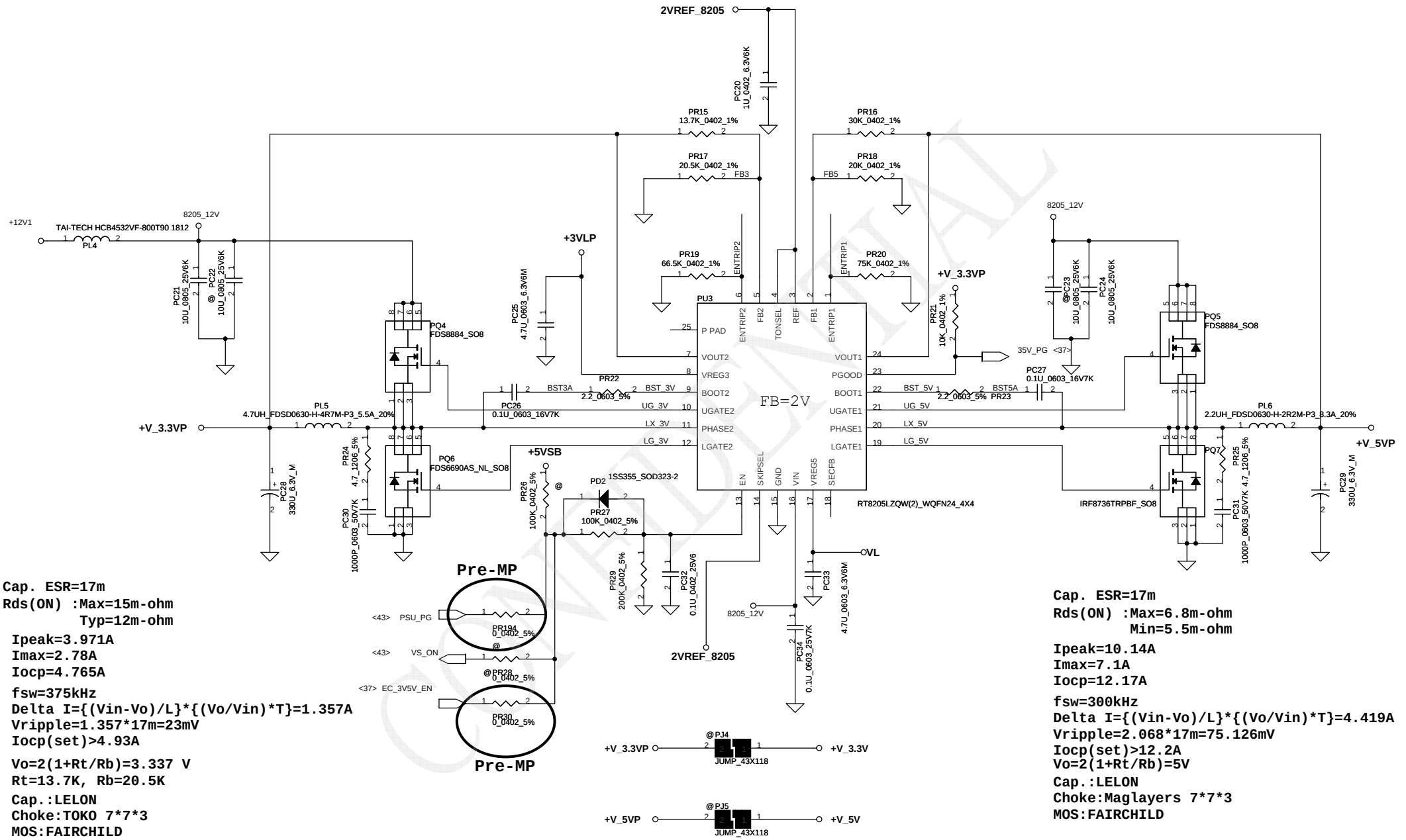
Title: SCHEMATIC,MB A8501

| Size | Document Number | Rev |
|---|---|---|
| Custom | 4019HO | B |

Date: Friday, May 18, 2012 | Sheet 43 of 59




Cap. ESR=17m
Rds(ON) :Max=15m-ohm
Typ=12m-ohm
Ipeak=3.971A
Imax=2.78A
Iocp=4.765A
fsw=375kHz
Delta I={(Vin-Vo)/L}*{(Vo/Vin)*T}=1.357A
Vripple=1.357*17m=23mV
Iocp(set)>4.93A
Vo=2(1+Rt/Rb)=3.337 V
Rt=13.7K, Rb=20.5K
Cap.:LELON
Choke:TOKO 7*7*3
MOS:FAIRCHILD
IC:RICHTEK
Bead:
Diode:PANJIT

Cap. ESR=17m
Rds(ON) :Max=6.8m-ohm
Min=5.5m-ohm
Ipeak=10.14A
Imax=7.1A
Iocp=12.17A
fsw=300kHz
Delta I={(Vin-Vo)/L}*{(Vo/Vin)*T}=4.419A
Vripple=2.068*17m=75.126mV
Iocp(set)>12.2A
Vo=2(1+Rt/Rb)=5V
Cap.:LELON
Choke:Maglayers 7*7*3
MOS:FAIRCHILD



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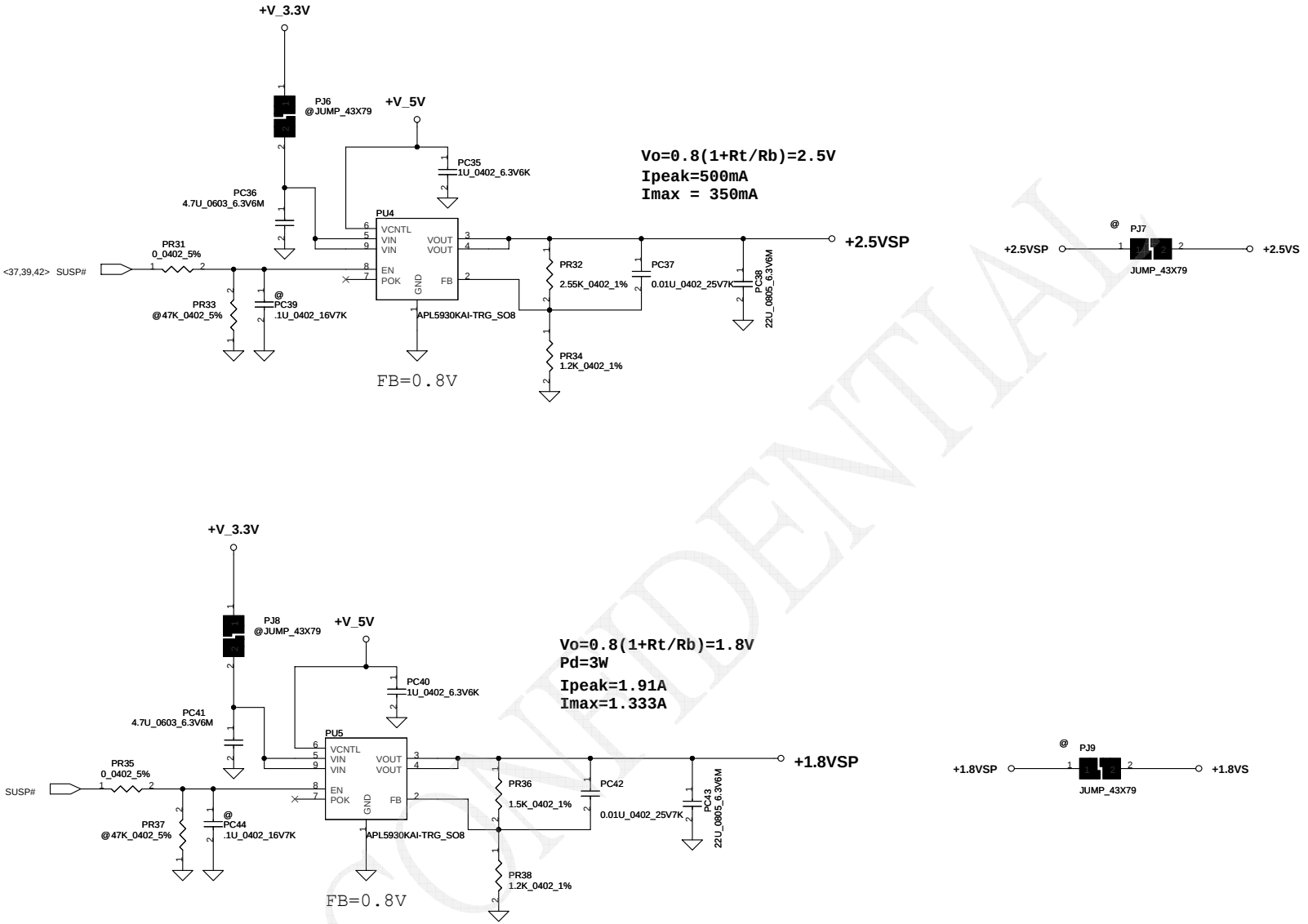
| Issued Date | 2011/09/12 | Deciphered Date | 2012/09/12 |
| Title | SCHEMATIC,MB A8501 | | |
| Size: Custom | Document Number: 4019HO | | Rev: B |
| Date: Friday, May 18, 2012 | Sheet 44 of 59 | | |



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| Issued Date | 2011/09/12 | Deciphered Date | 2012/09/12 |

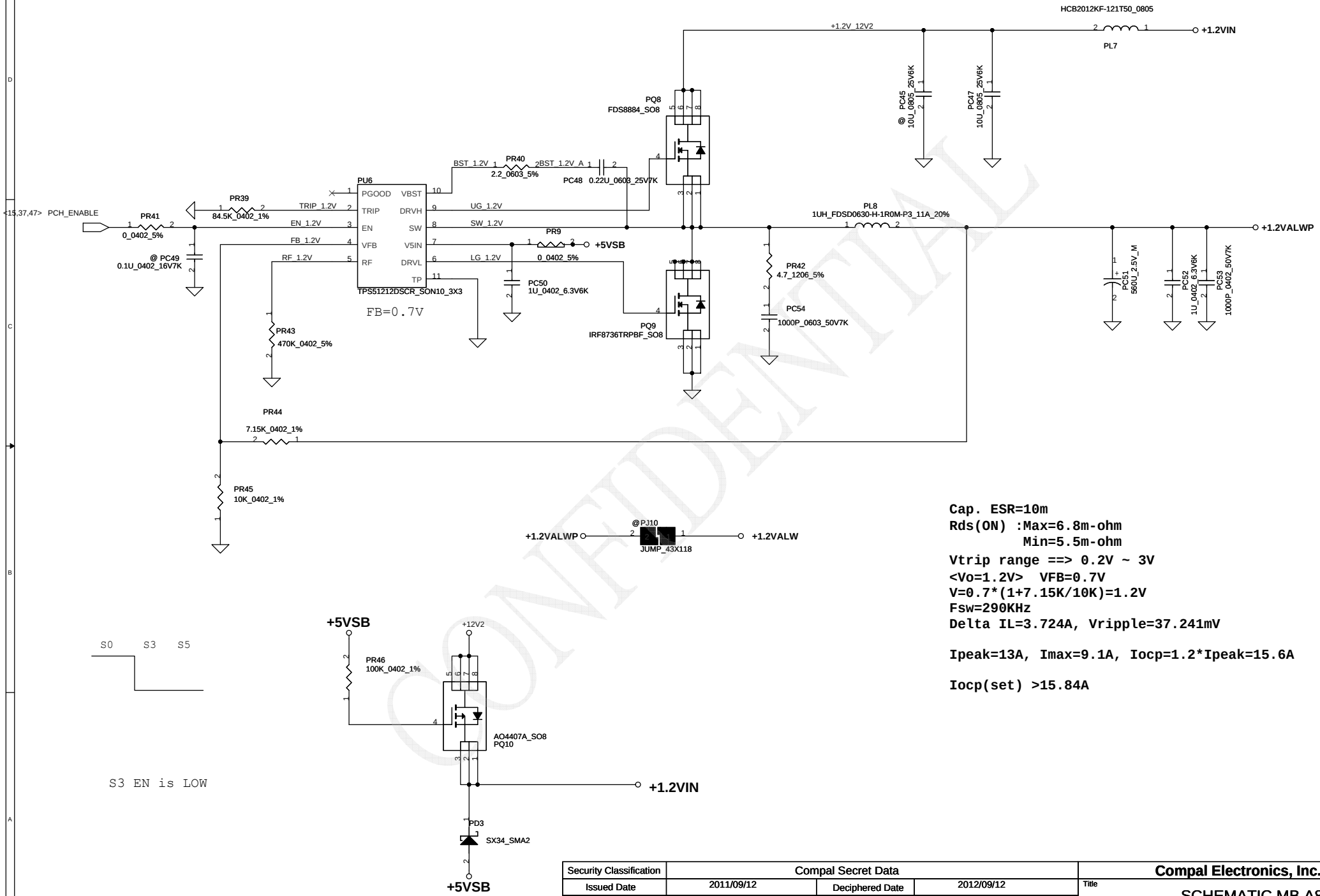


**Compal Electronics, Inc.**

Title: SCHEMATIC,MB A8501

| Size | Document Number | Rev |
|---|---|---|
| Custom | 4019HO | B |

Date: Friday, May 18, 2012 | Sheet 45 of 59



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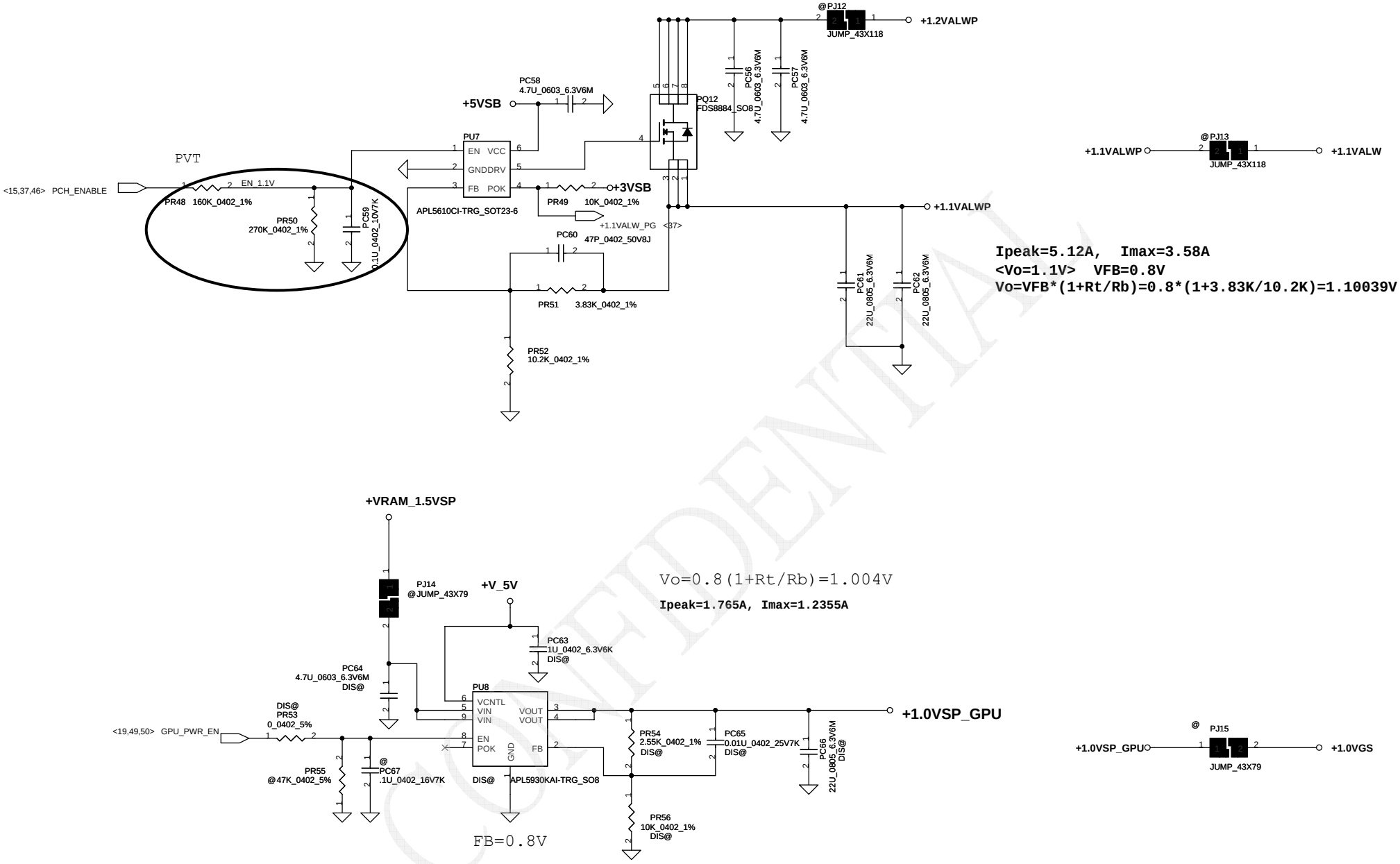
**Compal Electronics, Inc.**

Title: SCHEMATIC,MB A8501

Size: Custom | Document Number: 4019HO | Rev: B

Date: Friday, May 18, 2012 | Sheet 46 of 59



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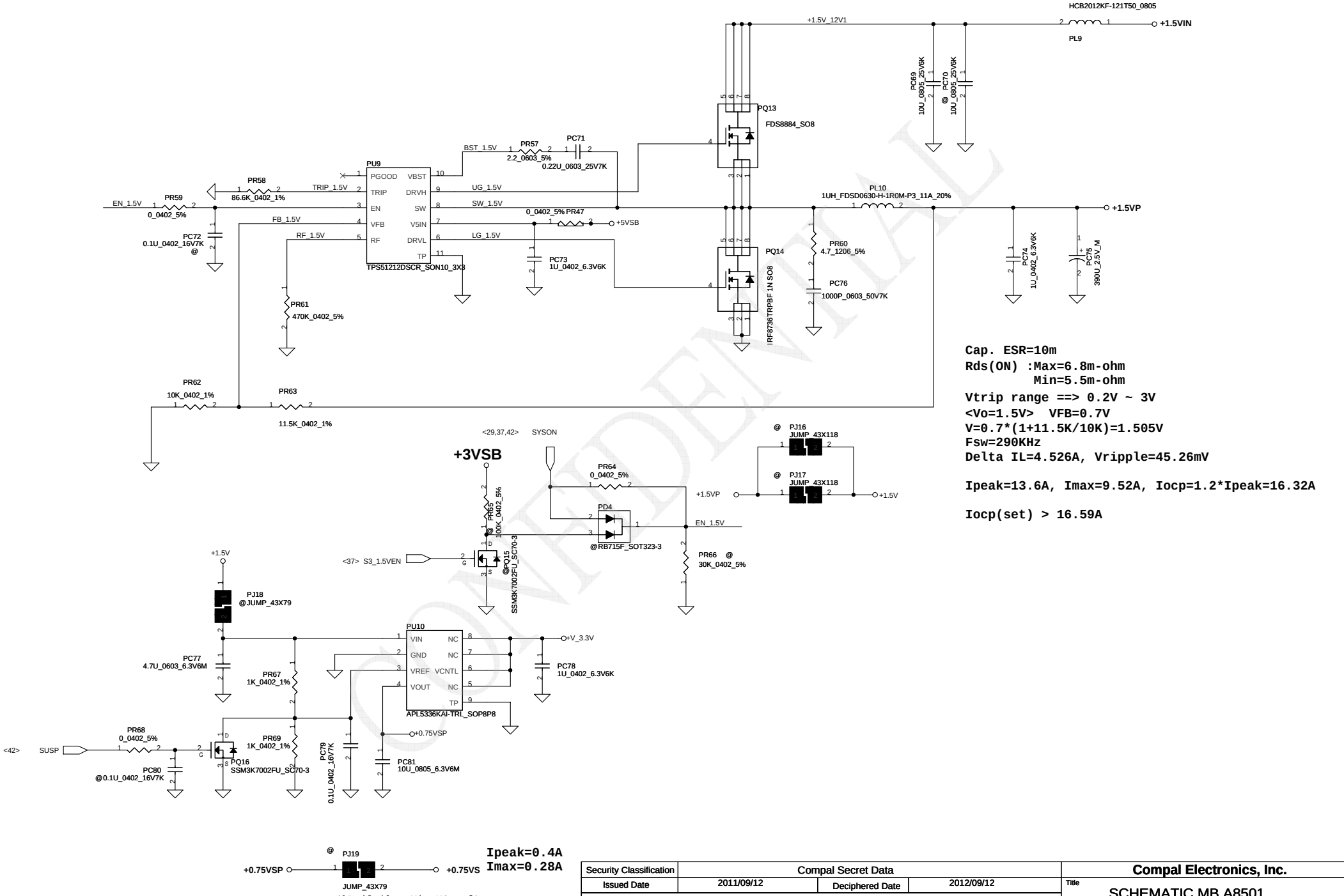
| Issued Date | 2011/09/12 | Deciphered Date | 2012/09/12 |
| Title | SCHEMATIC,MB A8501 | | |
| Size: Custom | Document Number: 4019HO | | Rev: B |
| Date: Friday, May 18, 2012 | Sheet 47 of 59 | | |




Cap. ESR=10m
Rds(ON) :Max=6.8m-ohm
Min=5.5m-ohm
Vtrip range ==> 0.2V ~ 3V
<Vo=1.5V> VFB=0.7V
V=0.7*(1+11.5K/10K)=1.505V
Fsw=290KHz
Delta IL=4.526A, Vripple=45.26mV

Ipeak=13.6A, Imax=9.52A, Iocp=1.2*Ipeak=16.32A

Iocp(set) > 16.59A



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| Issued Date | 2011/09/12 | Deciphered Date | 2012/09/12 |



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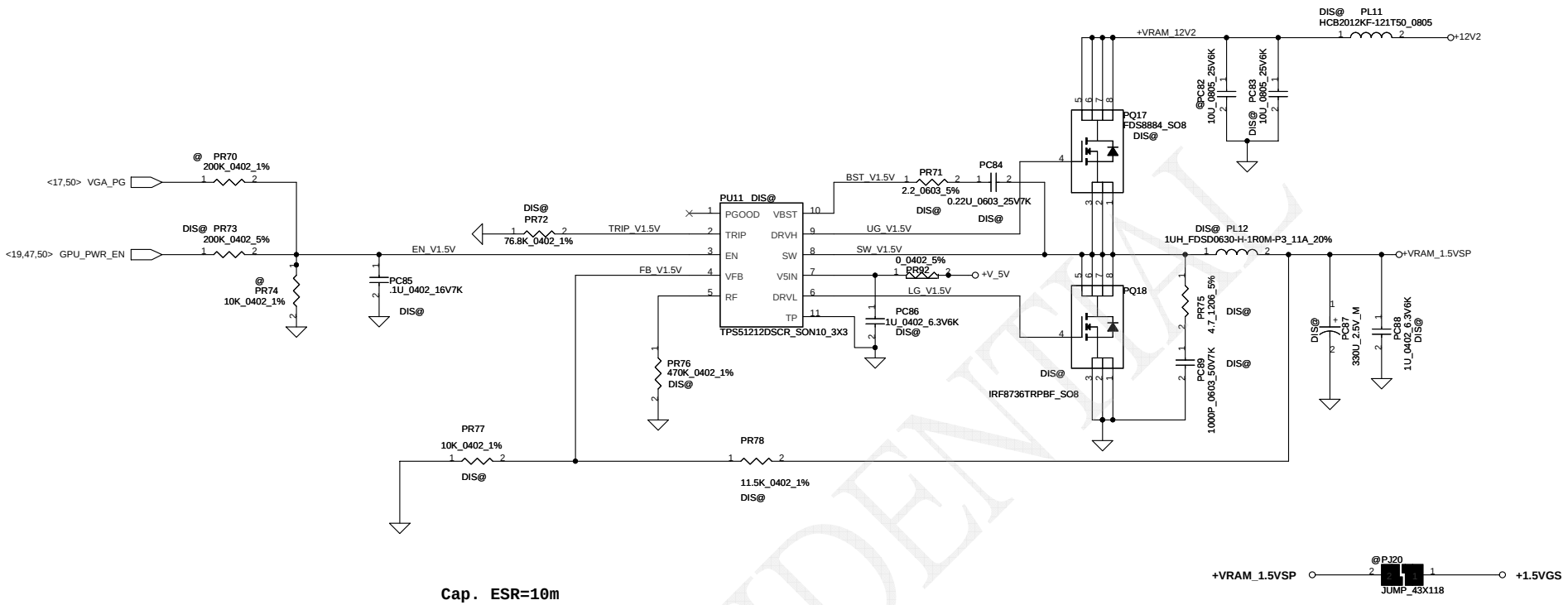
Title: SCHEMATIC,MB A8501

Size: Custom | Document Number: 4019HO | Rev: B

Date: Friday, May 18, 2012 | Sheet 48 of 59




**Cap. ESR=10m**
**Rds(ON) :Max=6.8m-ohm**
**Min=5.5m-ohm**
**Vtrip range ==> 0.2V ~ 3V**
**<Vo=1.5V> VFB=0.7V**
**V=0.7*(1+11.5K/10K)=1.505V**
**Fsw=290KHz**
**Delta IL=4.526A, Vripple=45.26mV**

**Ipeak=12.35A, Imax=8.65A, Iocp=1.2*Ipeak=14.83A**

**Iocp(set) >14.97A**



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| Issued Date | 2011/09/12 | Deciphered Date | 2012/09/12 |

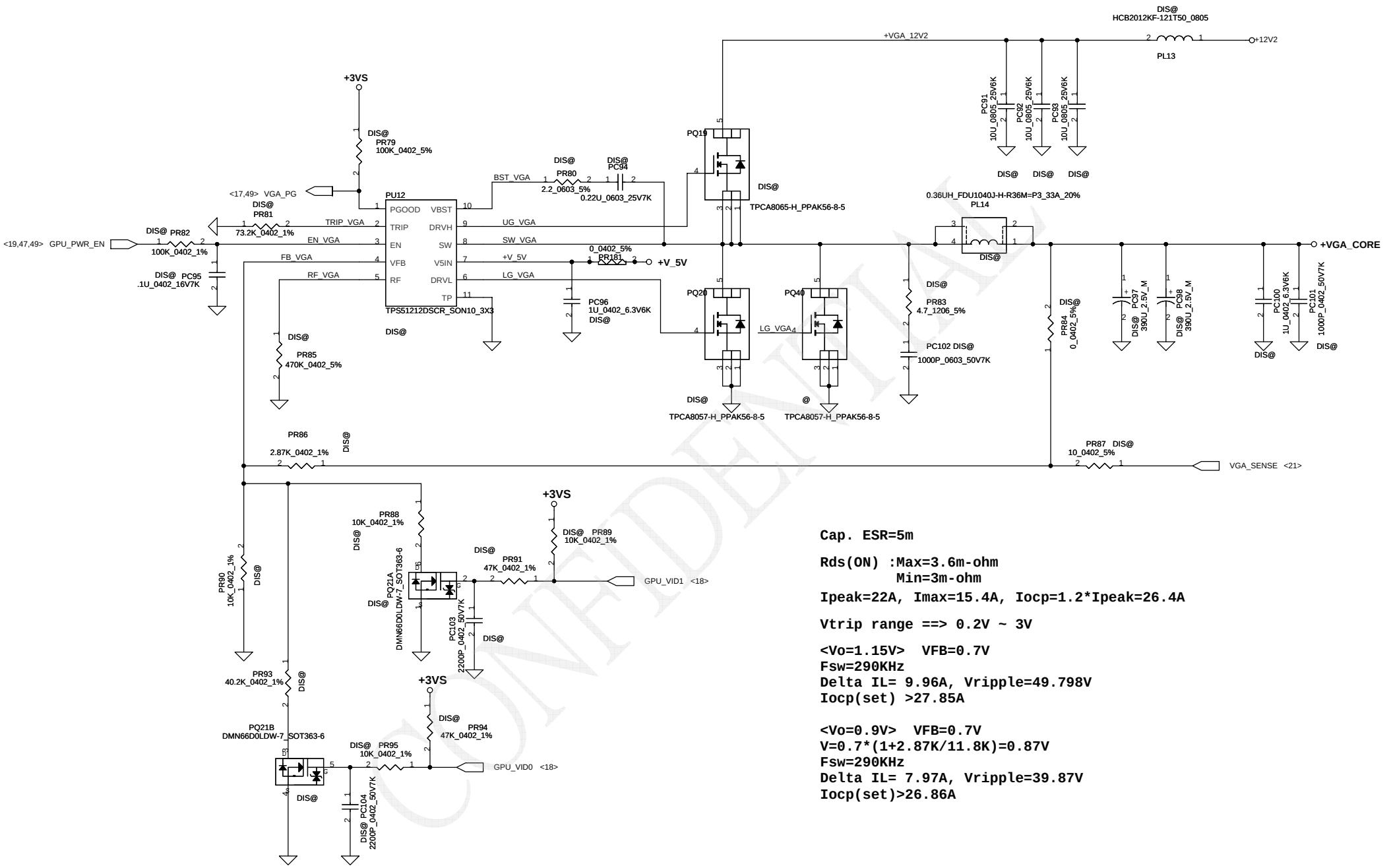


**Compal Electronics, Inc.**

Title: SCHEMATIC,MB A8501

Size: Custom | Document Number: 4019HO | Rev: B

Date: Friday, May 18, 2012 | Sheet 49 of 59




**Cap. ESR=5m**

**Rds(ON) :Max=3.6m-ohm**
**Min=3m-ohm**

**Ipeak=22A, Imax=15.4A, Iocp=1.2*Ipeak=26.4A**

**Vtrip range ==> 0.2V ~ 3V**

**<Vo=1.15V> VFB=0.7V**
**Fsw=290KHz**
**Delta IL= 9.96A, Vripple=49.798V**
**Iocp(set) >27.85A**

**<Vo=0.9V> VFB=0.7V**
**V=0.7*(1+2.87K/11.8K)=0.87V**
**Fsw=290KHz**
**Delta IL= 7.97A, Vripple=39.87V**
**Iocp(set)>26.86A**

| GPU_VID1 | GPU_VID0 | VGA_CORE | |
|---|---|---|---|
| 0 | 0 | 0.90V | |
| 0 | 1 | 0.95V | |
| 1 | 0 | 1.10V | |
| 1 | 1 | 1.15V | (Default) |



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| Issued Date | 2011/09/12 | Deciphered Date | 2012/09/12 |



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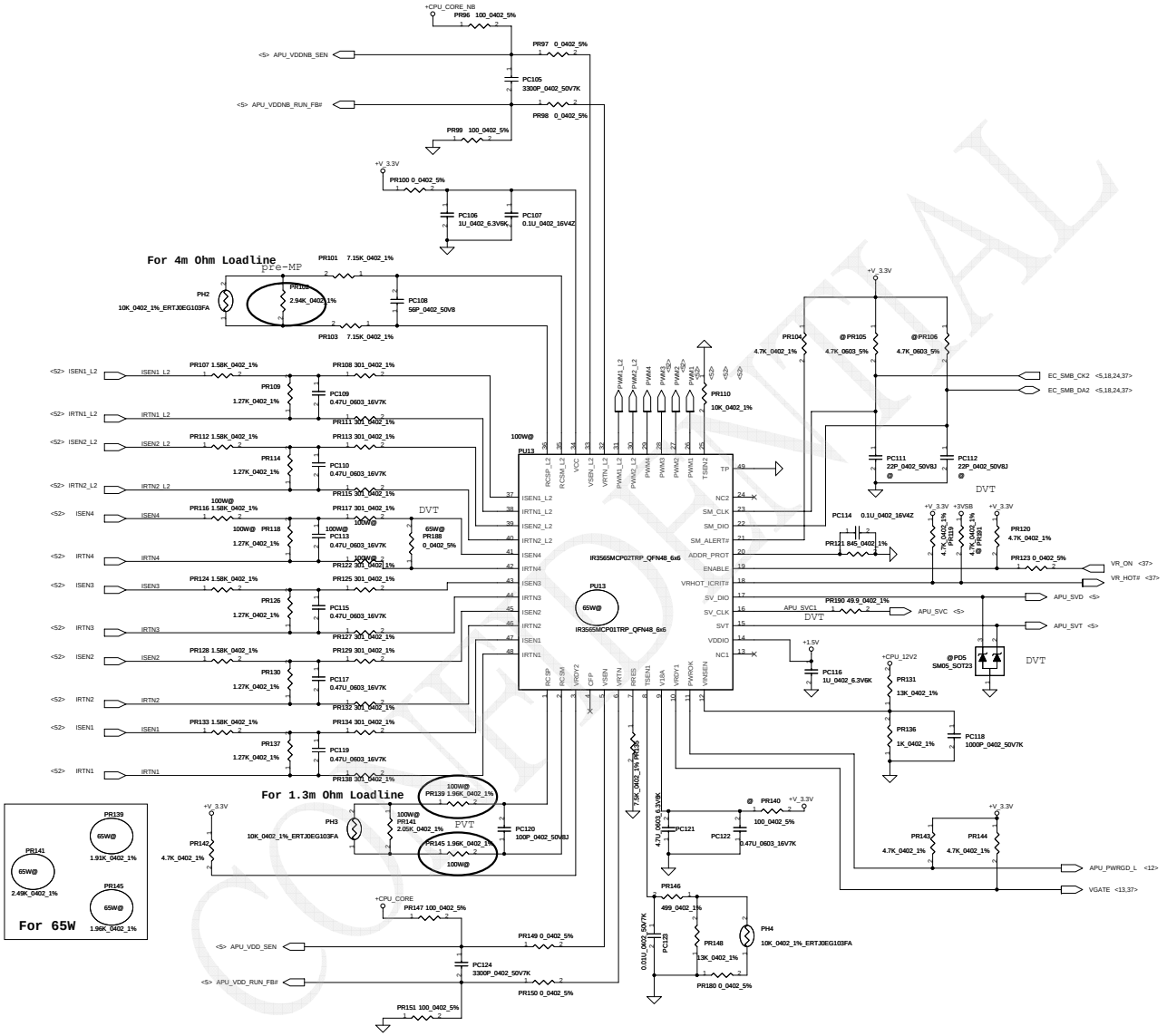
Title: SCHEMATIC,MB A8501

Size: Custom | Document Number: 4019HO | Rev: B

Date: Friday, May 18, 2012 | Sheet 50 of 59

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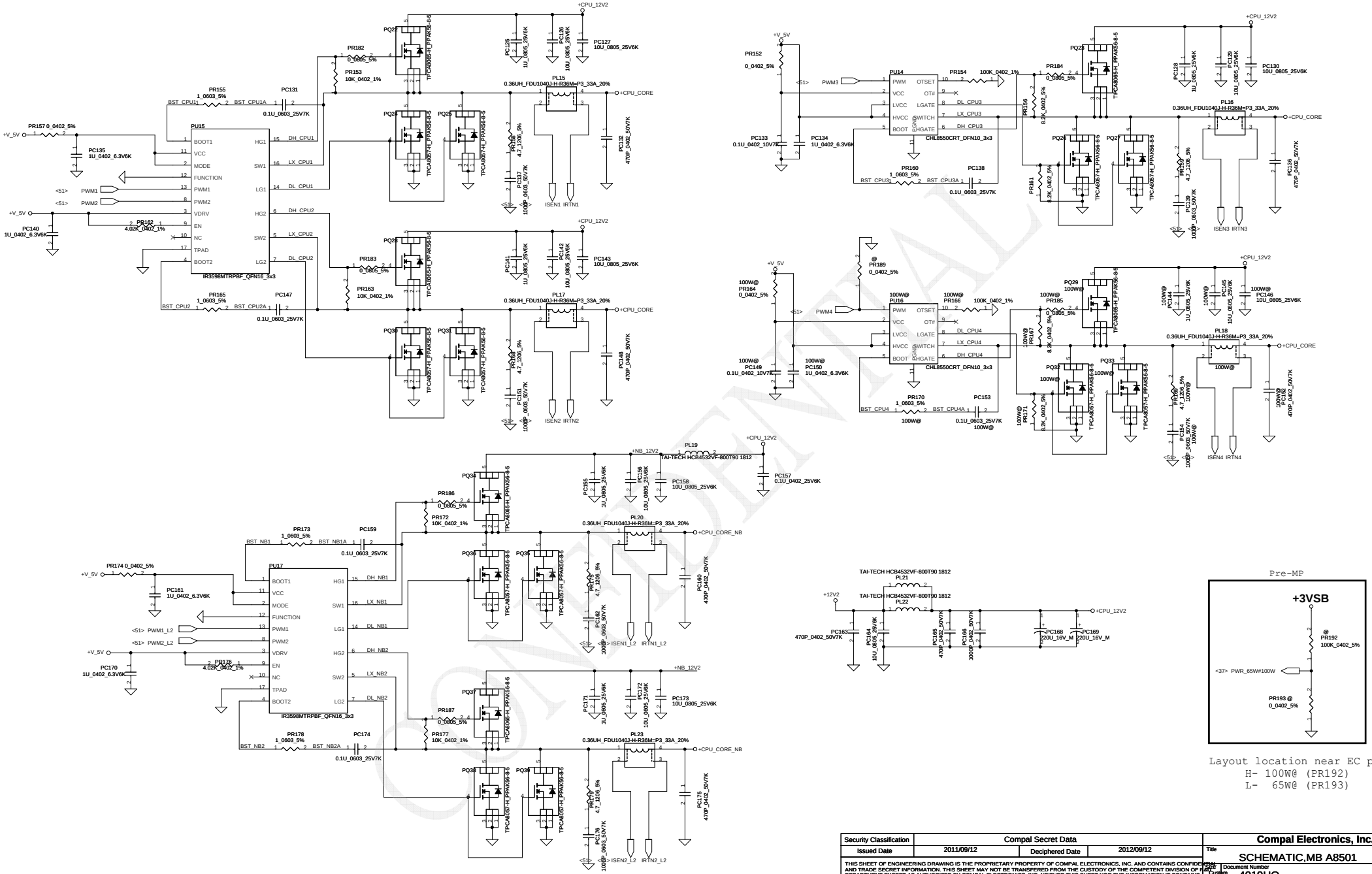




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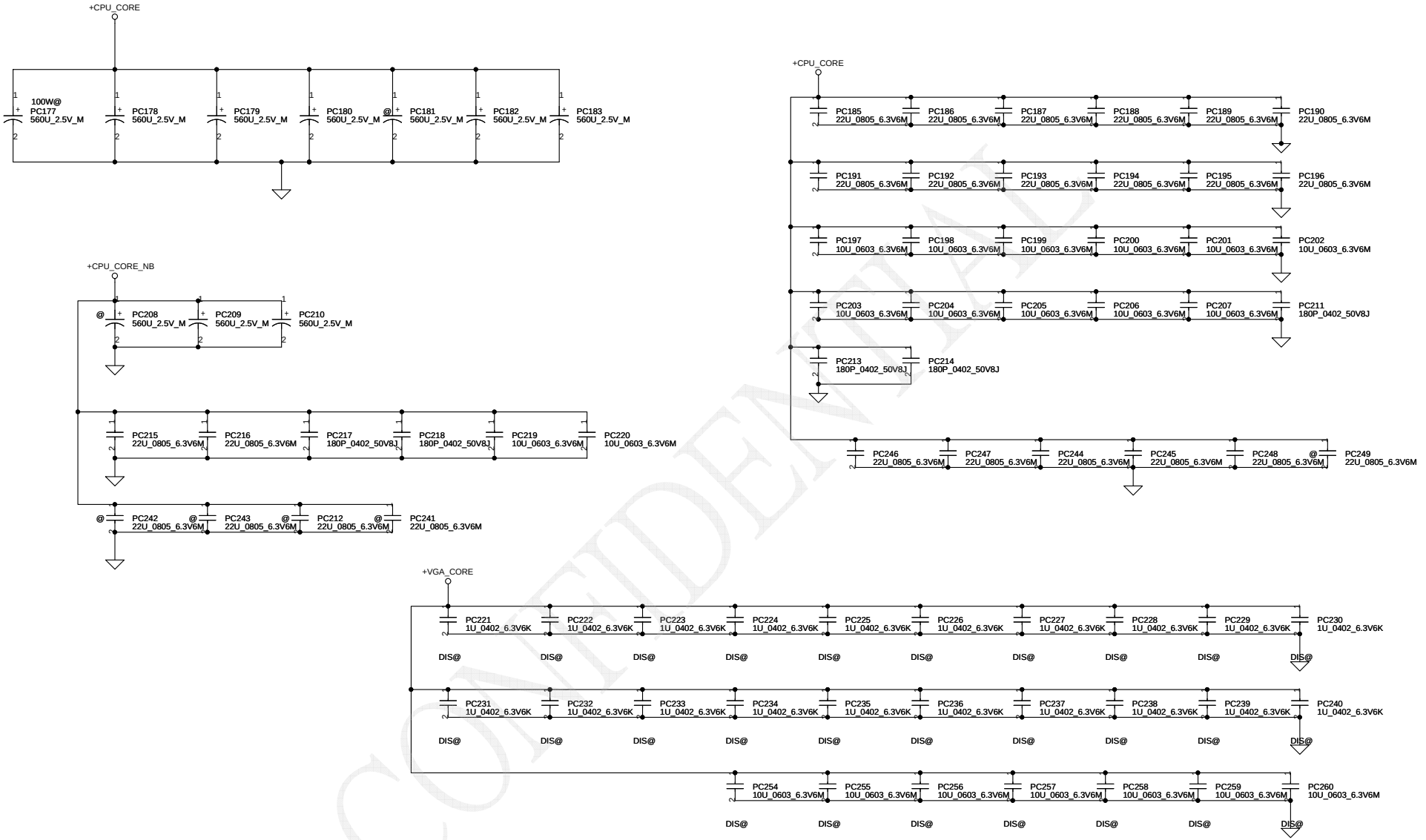




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| Custom | 4019HO | B |

Date: Friday, May 18, 2012 | Sheet 53 of 59

| NO | DATE | PAGE | MODIFICATION LIST | PURPOSE |
|---|---|---|---|---|
| 1 | 2011/9/21 | P50 | Change PR88 to 10k ohm | Modify VGA_CORE VID setting value |
| 2 | 2011/9/22 | P47/P50 | Change EN pin netname to GPU_PWR_EN | For HW request |
| 3 | 2011/9/27 | P50 | Change PL14 connection to pin 1 and pin 4 | For Layout |
| 4 | 2011/9/28 | P52 | Change PC153 PIN2 to LX_CPU4 | Modify PU16 bootstrap circuit |
| | 2011/9/28 | P49/P49/P50 | Change +1.2ALWP/+VRAM_1.5VSP/+VGA_CORE input to +CPU_12V2 | For layout easily |
| 5 | 2011/9/28 | P50/P52 | Change PC90/91/92/93/126/127/129/130/142/143/145/146/156/158/164/172/173 PN from SE14210WL0 to SE00000QK00 | For Cost saving |
| 6 | 2011/9/28 | P50/P46 | Change PL13/PL7 PN to SM01000C000 | For Cost saving |
| | | P51 | Net name:+CPU_12V2 | |
| | | P50 | Remove PC90 | For Layout |
| 7 | 2011/9/28 | P43/P46 | remove PR9/PQ3/PC9/PJ1/ PR47/PQ11/PC55/PJ11 | For Layout space |
| 8 | 2011/9/29 | P49 | change PC87 from 390u/6h to 330u/4.2h | For Layout space |
| 9 | 2011/10/03 | P52 | change PR146 PIN1 connect to PR148 | IR FAE suggest |
| 10 | 2011/10/03 | | change PC20,PC50,PC52,PC73,PC74,PC78, PC86,PC88,PC96,PC100,PC106,PC134,PC135, PC140,PC150,PC161,PC170to SE000000KL0<br><br>change PC25,PC33,PC36,PC41,PC56,PC58,PC64, PC77 to SE107475M80 | For Cost saving |
| 11 | 2011/10/04 | P50 | add PQ40 | co-lay VGA |
| 12 | 2011/10/04 | P52 | Modify PU14 and PU16 footprint form QFN10_3*3 to DFN10_3*3 | Modify to correct footprint |
| 13 | 2011/10/05 | P50 | Connect PL14 Pin2 to Pin1 & Pin3 to Pin4 | For Layout shape |
| 14 | 2011/10/11 | P51 | Modify PR97,98,149,150 connection<br>Add short pad PR180 | IR FAE suggest |
| 15 | 2011/10/11 | P51 | Change PH2,PH3,PH4 to SLZ00001D00<br>Change PR146 to 500 ohm | For Cost saving<br>OTP Tuner |
| 16 | 2011/10/12 | P49/P49/P50 | Change +1.2ALWP/+VRAM_1.5VSP/+VGA_CORE input to +12V2 | For layout easily |
| | | P51 | Update PU13 (IR3565) part number | New part number released |
| 17 | 2011/10/12 | P51 | Update P146 to 499 ohm | old part x code |
| 18 | 2011/10/14 | P44/P46/P48/P49 | Remove PC46/PC68<br>Change PC22/ PC23/PC47/PC70/PC82 bom structure to "@"<br>Change PC21/PC24/PC45/PC69/PC83 PN to SE00000QK00 | For C38 request |
| 19 | 2011/10/14 | P43 | add PC46/PC55/PC68<br>add PR9/PR47/PR92/PR181 | For ESD request<br>For C38 request |
| 20 | 2011/10/14 | P51 | Change PC122 PN to SE026474K80 | For PJE request |
| 21 | 2011/10/17 | P52 | add PR182/PR183/PR184/PR185/PR186/PR187 | For EMI request |
| 22 | 2011/10/18 | P52 | change PR182/PR183/PR184/PR185/PR186/PR187 to 0805 size | For C38 request |
| 23 | 2011/10/18 | P52 | Midify PU14,15,PU16,17 Enable Signal | Modify enable signal error |
| 24 | 2011/10/25 | P44 | Remove PR26 in BOM | Modify PSU_PG signal |
| 25 | 2011/11/09 | P46 | Change PR9 net name from +V_5V to +5VSB | |
| | | P47 | Change PC58 net name from +V_5V to +5VSB<br>Change PC58 net name from +V_3.3V to +3VSB | Design change |
| | | P51 | add BOM Structure "@" at PR105 and PR106 | |
| 26 | 2011/11/14 | P51 | change PR105 and PR106 to 0805 size | |
| | | P53 | remove POSCAP PC184 and PC212<br>add BOM structure "100W8" to PC177<br>add BOM structure "@" to PC181 and remove "@" from PC183<br>add PC244, PC245, PC246,PC247<br>add PC242, PC243, PC212, PC241,PC248,PC249 with BOM Structure"@"<br>add BOM structure "@" to PC208 | Design change |
| 27 | 2011/11/16 | P50 | add BOM structure "DIS@" to PR88,PR90,PR93, PC221-PC260 | BOM control |
| 28 | 2011/11/17 | P43, P48 | change PN from SB000009610 to SB000009Q80 of PQ1,PQ15,PQ16 | Material shortage |
| 29 | 2011/11/18 | P55 | change PR93 to 27K, and PR88 to 20K | Design change |
| 30 | 2011/11/18 | P48 | change PR47.2 net name from "+V_5V" to "+5VSB" | Design change |
| 31 | 2011/11/23 | P48 | Add BOM Structure "100W8" in PR116, PR117, PR118, PR122 and PC113 | cost down |
| 32 | 2011/11/24 | P51 | Add PR188 with BOM structure "65W8" | Design change |
| | | P52 | Add PR189 with BOM structure "@" | |
| 33 | 2011/11/28 | P50 | change PR88 to 10K and PR93 to 40.2K | Design change |
| | | P53 | remove BOM Structure"@" of PC248 | |
| 34 | 2011/11/29 | P50 | change PR107,PR112,PR116,PR124,PR128,PR133===1.58K<br>change PR109,PR114,PR118,PR126,PR130,PR137===1.27K<br>change PC109,PC110,PC113,PC115,PC117,PC119===0.47U(X7R)<br>PR141==2.05K<br>PR139==1.78K<br>PR145==1.82K | Design change |
| | | P48,P49 | change PR57, PR71 to ZR2 | |
| 35 | 2011/12/01 | P51 | add PR191=4.7K<br>add PR190=49.9-ohm<br>add PD5<br>add PR188 | |
| 36 | 2011/12/7 | P50 | Change PR86,PR88,PR90,PR93 resistor value | Change VGA_CORE VID |
| | | P43 | remove BOM Structure"@" of PC46 | For EMC request |
| 37 | 2011/12/13 | P51 | Add PU13 BOM Structure "65W8" for SA00005IJ00<br>Add PU13 BOM Structure"100W8" for SA00005BF00 | Part Number divided |
| 38 | 2012/1/31 | P43 | PU2 change to SA00003RU00 (ST8033) | Design change |
| | | P50 | PR139,PR145 change to 1.96K | Loadline finetune |
| | | P47 | PC59=0.1UF , PR48=160K , PR50=270K | Design change |
| 39 | 2012/2/1 | P43 | PU2 change to SA00004CY10 (RT8061)<br>Add PU19 | Design change<br>Design change |



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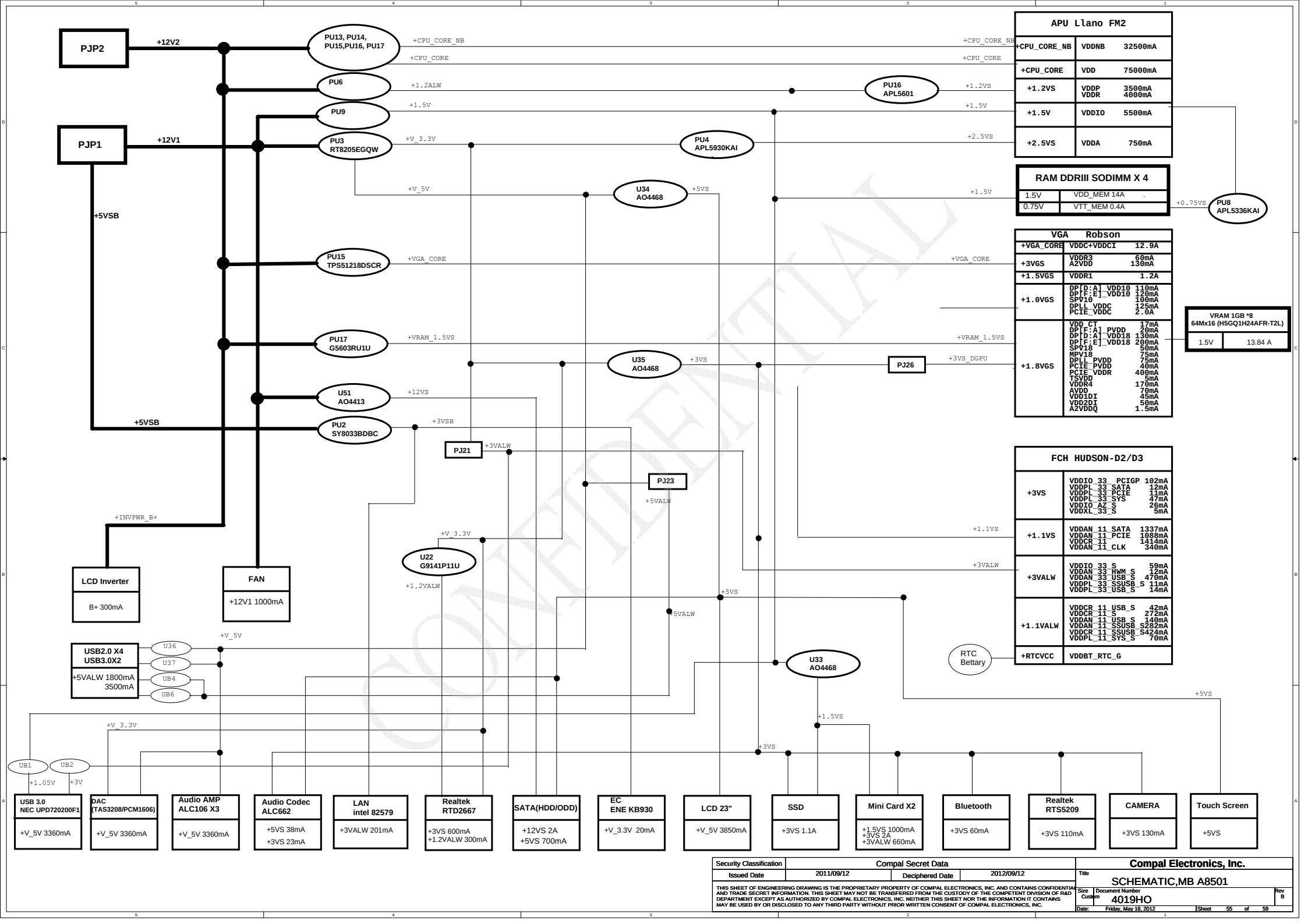
PJP2
+12V2
PJP1
+12V1
+5VSB
PU13, PU14, PU15,PU16, PU17
+CPU_CORE_NB
+CPU_CORE
PU6
+1.2ALW
PU9
+1.5V
PU3
RT8205EGQW
+V_3.3V
+V_5V
PU16
APL5601
+1.2VS
PU4
APL5930KAI
+2.5VS
U34
AO4468
+5VS
PU15
TPS51218DSCR
+VGA_CORE
PU17
G5603RU1U
+VRAM_1.5VS
U35
AO4468
+3VS
PJ26
+3VS_DGPU
U51
AO4413
+12VS
PU2
SY8033BDBC
+3VSB
PJ21
+3VALW
PJ23
+5VALW
+INVPWR_B+
U22
G9141P11U
+1.2VALW
+1.1VS
+3VALW
+1.5VS
U33
AO4468
RTC
Bettary
+5VS
+1.5VS
+3VS
+V_5V
+V_3.3V
UB1
UB2
+1.05V
+3V
U36
U37
UB4
UB6
LCD Inverter
B+ 300mA
FAN
+12V1 1000mA
USB2.0 X4
USB3.0X2
+5VALW 1800mA
3500mA
USB 3.0
NEC UPD720200F1
+V_5V 3360mA
DAC
(TAS3208/PCM1606)
+V_5V 3360mA
Audio AMP
ALC106 X3
+V_5V 3360mA
Audio Codec
ALC662
+5VS 38mA
+3VS 23mA
LAN
intel 82579
+3VALW 201mA
Realtek
RTD2667
+3VS 600mA
+1.2VALW 300mA
SATA(HDD/ODD)
+12VS 2A
+5VS 700mA
EC
ENE KB930
+V_3.3V 20mA
LCD 23"
+V_5V 3850mA
SSD
+3VS 1.1A
Mini Card X2
+1.5VS 1000mA
+3VS 2A
+3VALW 660mA
Bluetooth
+3VS 60mA
Realtek
RTS5209
+3VS 110mA
CAMERA
+3VS 130mA
Touch Screen
+5VS
APU Llano FM2
+CPU_CORE_NB VDDNB 32500mA
+CPU_CORE VDD 75000mA
+1.2VS VDDP 3500mA VDDR 4000mA
+1.5V VDDIO 5500mA
+2.5VS VDDA 750mA
RAM DDRIII SODIMM X 4
1.5V VDD_MEM 14A
0.75V VTT_MEM 0.4A
PU8
APL5336KAI
VGA Robson
+VGA_CORE VDDC+VDDCI 12.9A
+3VGS VDDR3 60mA A2VDD 130mA
+1.5VGS VDDR1 1.2A
+1.0VGS DP[D:A]_VDD10 110mA DP[F:E]_VDD10 120mA SPV10 100mA DPLL_VDDC 125mA PCIE_VDDC 2.0A
+1.8VGS VDD_CT 17mA DP[F:A]_PVDD 20mA DP[D:A]_VDD18 130mA DP[F:E]_VDD18 200mA SPV18 50mA MPV18 75mA DPLL_PVDD 75mA PCIE_PVDD 40mA PCIE_VDDR 400mA TSVDD 5mA VDDR4 170mA AVDD 70mA VDD1DI 45mA VDD2DI 50mA A2VDDQ 1.5mA
VRAM 1GB *8
64Mx16 (H5GQ1H24AFR-T2L)
1.5V 13.84 A
FCH HUDSON-D2/D3
+3VS VDDIO_33_PCIGP 102mA VDDPL_33_SATA 12mA VDDPL_33_PCIE 11mA VDDPL_33_SYS 47mA VDDIO_AZ_S 26mA VDDXL_33_S 5mA
+1.1VS VDDAN_11_SATA 1337mA VDDAN_11_PCIE 1088mA VDDCR_11 1414mA VDDAN_11_CLK 340mA
+3VALW VDDIO_33_S 59mA VDDAN_33_HWM_S 12mA VDDAN_33_USB_S 470mA VDDPL_33_SSUSB_S 11mA VDDPL_33_USB_S 14mA
+1.1VALW VDDCR_11_USB_S 42mA VDDCR_11_S 272mA VDDAN_11_USB_S 140mA VDDAN_11_SSUSB_S282mA VDDCR_11_SSUSB_S424mA VDDPL_11_SYS_S 70mA
+RTCVCC VDDBT_RTC_G
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Title
SCHEMATIC,MB A8501
Size
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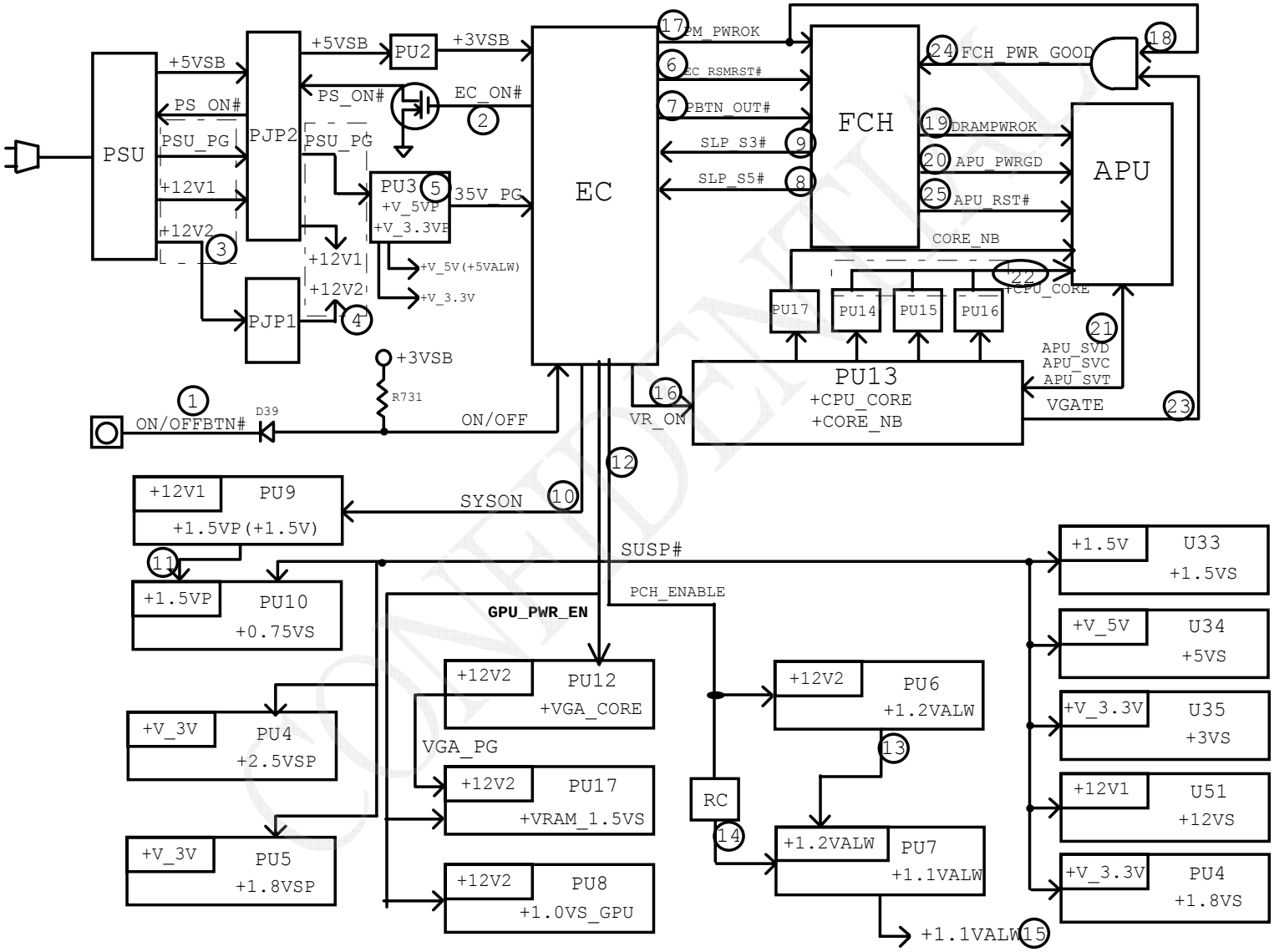
Document Number
4019HO
Rev
B
Date:
Friday, May 18, 2012
Sheet
55
of
59

# COMPAL CONFIDENTIAL

**MODEL NAME:** *QLA13 Power Sequence Block Diagram (Discrete)*
**PCB NAME:** *LA8501P*
**REVISION:** *0.1*
**DATE:** *2010/10/26*



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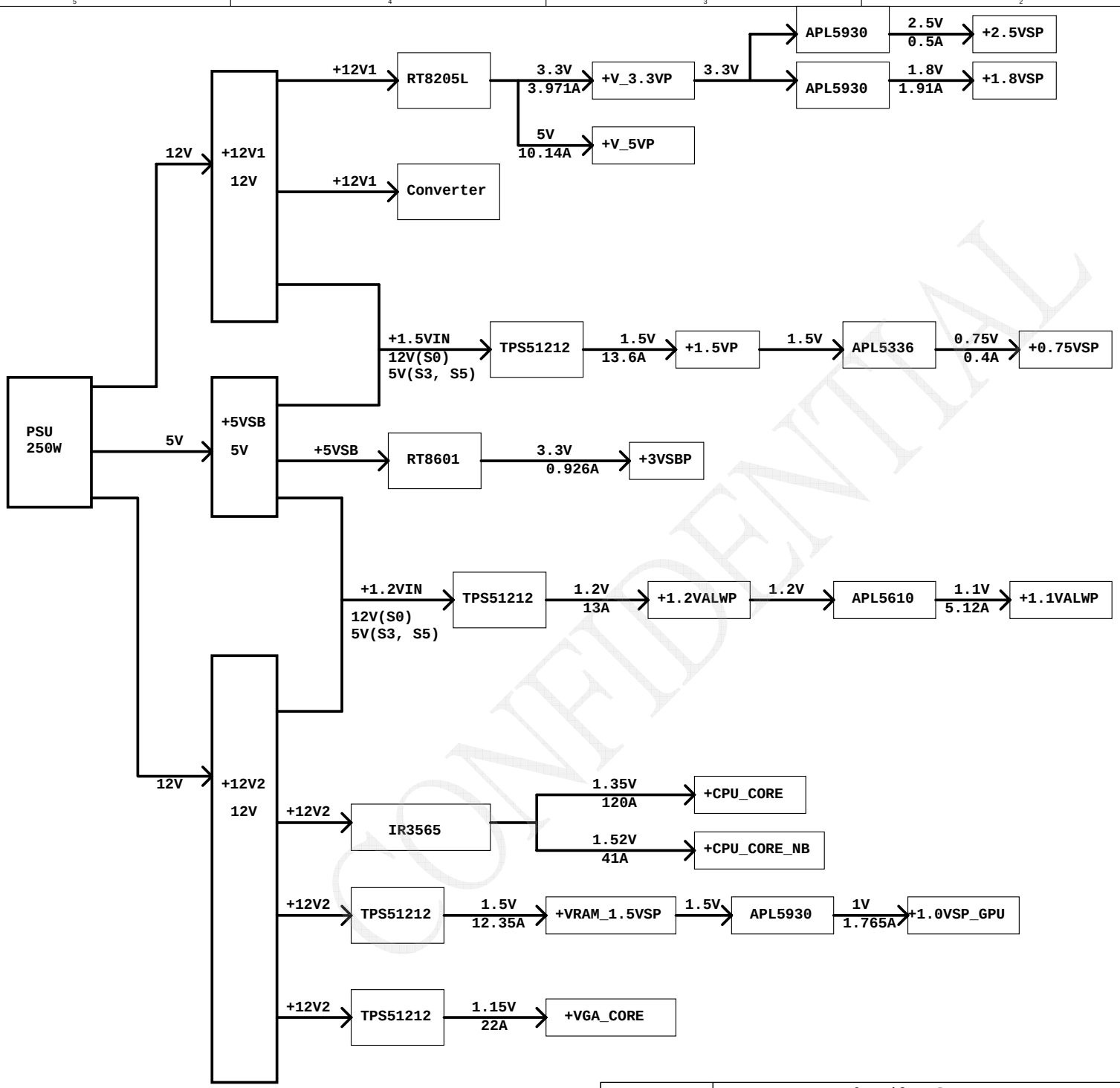




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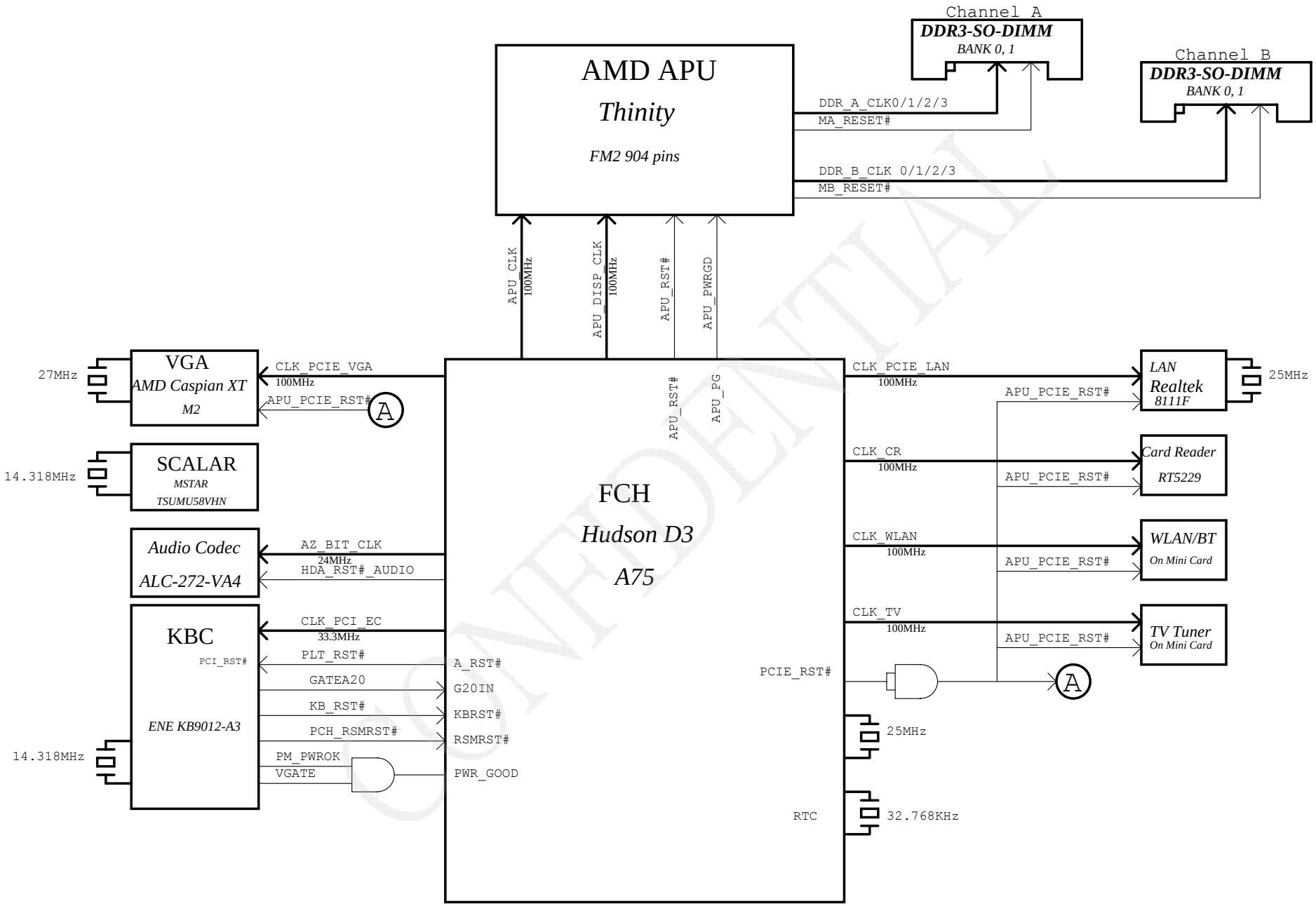
# Clock and Reset Diagram



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| Date: Friday, May 18, 2012 | Sheet 58 of 59 | | |

# HW schematic change list

| NO | DATE | PAGE | MODIFICATION LIST | PURPOSE |
|---|---|---|---|---|
| 1 | 01/20 | P15 | R1764 change to 1M | BOM ERROR |
| 2 | 01/20 | P18 | R1737,R1738 BOM change to @ | BOM ERROR |
| 3 | 01/20 | P29 | Add R1803 | For HDMI Votage |
| 4 | 01/20 | P40 | C612 change to 0805 | For DFX |
| 5 | 01/20 | P40 | JBT1 change to 8 pin ACES_87212-08G0L | For ASSY to move location |
| 6 | 01/20 | P31 | Remove R525,C681 & R524,C681 | For EMI |
| 7 | 01/28 | P42 | H2,H4 change to 4P0 | For ME |
| 8 | 01/28 | P42 | Add 10u C1908,C1909 for +V_5V | For ESD |
| 9 | 01/28 | P39 | Add 1u C1906,C1907 for +V_3.3V&+USB_VCCA | For ESD |
| 10 | 01/28 | P29 | Add C1910,C1911 for +V_3.3V | For HDMI IN Re-driver |
| 11 | 01/28 | P29 | Remove ESD DIODE D12,D13,D16,D18 | For HDMI IN Re-driver |
| 12 | 01/29 | P05 | Remove HDT1 | For ESD |
| 13 | 01/29 | P31 | Remove Q102,Q120 | For EMI |
| 14 | 02/01 | P41<br>P39<br>P29<br>P37<br>P40<br>P16 | Add C1916 0.1u on SENSE BD +3VSB<br>Add C1914 0.1u on S3USB_ON<br>Add C1912 0.1u on IO Conn. +3VALW<br>Add C1913 0.1u on MUTE_CODEC<br>Add C1915 0.1u on BT_RESET<br>Change C247 2.2u to 10u | For ESD |
| 16 | 02/24 | P33<br>P39<br>P40 | Add RC on external& internal USB D- | AMD Errata 40 |
| 17 | 03/16 | P37 | Add PWR_65W#100W GPIO | |
| 18 | 03/19 | P28 | Add PANEL_C_2 | |
| 19 | 04/16 | P41 | Del SW1 | |
| 20 | 05/04 | P29 | Add D10/D11 for ESD | |
| 21 | | | | |
| 22 | | | | |
| 23 | | | | |



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