Model Name : Q5LJ1(MA51-HX)
File Name : LA-8203P
BOM P/N:43

Compal Confidential

Q5LJ1 M/B Schematics Document

Intel Ivy Bridge ULV Processor + Panther Point PCH
Nvidia N13P-GS

2012-05-08

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.		
Title: SCHEMATIC MB A8203		
Size: Custom	Document Number: 4019J1	Rev: C
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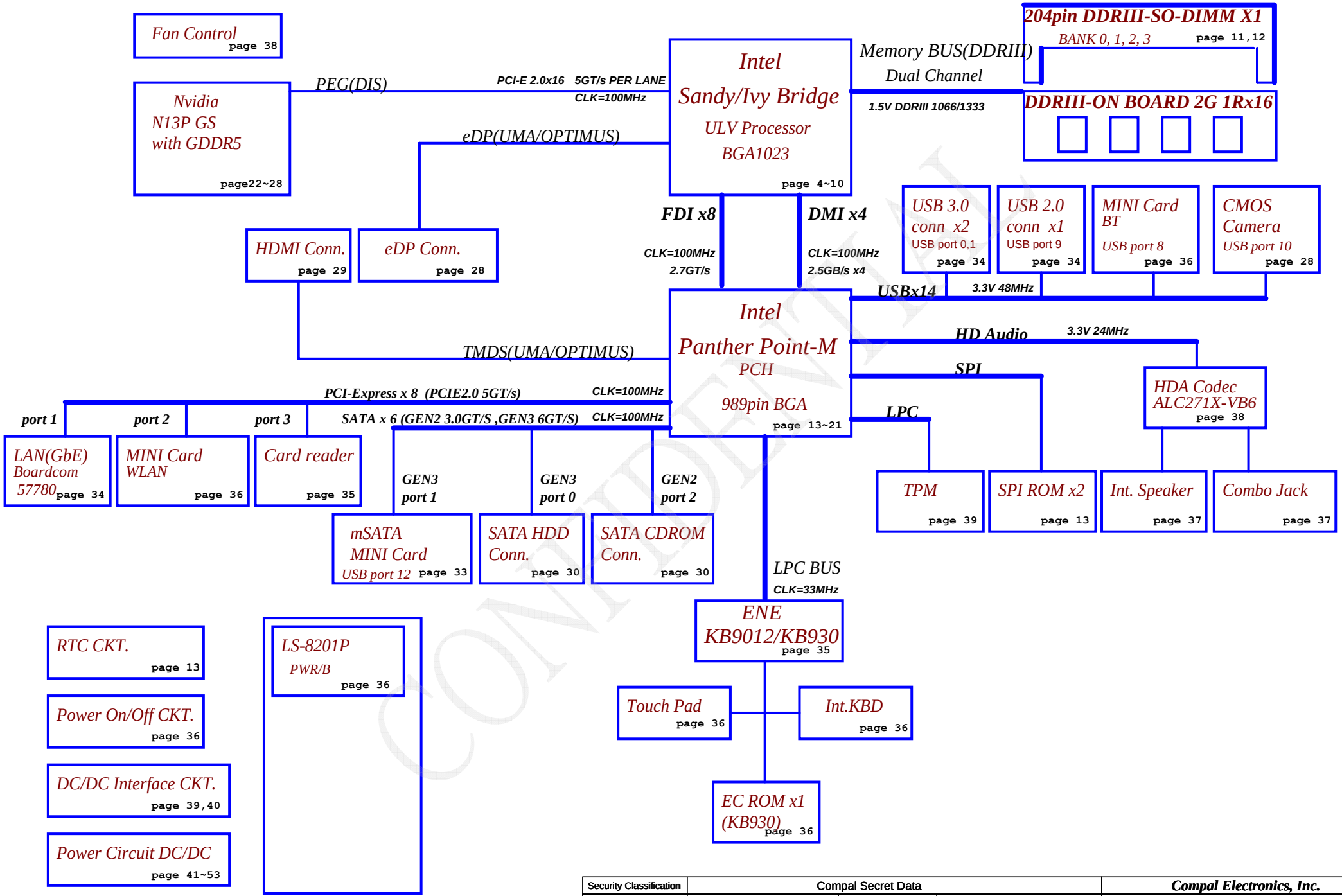

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Voltage Rails

Power Plane	Description	AC S0	AC S3	AC S4	AC S5	DC DS3	DC DS4	DC DS5
+RTCVCC	RTC power	ON	ON	ON	ON	ON	ON	ON
VIN	Adapter power supply (19V)	N/A	ON	ON	ON	OFF	OFF	OFF
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A	N/A	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON	ON	ON	ON
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	OFF	OFF	OFF	OFF	OFF
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF	OFF	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF	OFF	OFF	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON	ON	ON	ON	ON
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH	ON	ON	ON	OFF	OFF	OFF	OFF
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF	OFF	OFF	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON	ON	ON	ON	ON
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH	ON	ON	ON	OFF	OFF	OFF	OFF
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF	OFF	OFF	OFF	OFF
+VCCSA	+VCCSA POWER RAIL TO CPU	ON	OFF	OFF	OFF	OFF	OFF	OFF
+1.8VS	+3VALW to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF	OFF	OFF	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF	OFF	ON	OFF	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF	OFF	OFF	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF	OFF	OFF	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF	OFF	OFF	OFF	OFF
+3V_LAN	LAN CHIP POWER RAIL	ON	ON	ON	ON	OFF	OFF	OFF
+3VS_WLAN	WLAN MODULE POWER RAIL	ON	OFF*	OFF*	OFF	OFF	OFF	OFF
+USB3_VCCA	USB SLEEP CHARGER & PORT0 POWER POWER RAIL	ON*	ON	ON	ON	ON*	ON*	ON*
+USB3_VCCB/C	USB PORT1/9 POWER POWER RAIL	ON	ON	OFF	OFF	OFF	OFF	OFF
+3VSDGPU	+3VS to +3VSDGPU power rail	ON**	OFF	OFF	OFF	OFF	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON**	OFF	OFF	OFF	OFF	OFF	OFF
+1.5VSDGPU	+1.5V to +1.5VSDGPU switched power rail for GPU	ON**	OFF	OFF	OFF	OFF	OFF	OFF
+1.05VSDGPU	+1.05VSDGPU switched power rail for GPU	ON**	OFF	OFF	OFF	OFF	OFF	OFF

Note : ON* WILL DEPEND ON BATTERY CAPACITY TO TURN ON OR OFF

Note : ON** Depend on Optimus ON/OFF.

Note : OFF* Depend on IOAC SPEC support or not.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
On Board Thermal Senser	1001_101xb

PCH SM Bus address

Device			Address	
ChannelA	DIMM0	A0	1010 000X	JDIMM1(SPD)
ChannelB	DIMM0	A4	1010 010X	On Board RAM(SPD)

CPU BOM Config

I32367@	I3-2367M	HR	1.4G	SA000051H60 (S IC AV8062701047904 SR0CV J1 1.4G ABO!)	
I32377@	I3-2377M	HR	1.5G	SA00005MX10 (S IC AV8062701048004 QAXQ J1 1.5G BGA)	
I52467@	I5-2467M	HR	1.6G	SA00004X010 (S IC AV8062701047504 SR0D6 J1 1.6G ABO!)	
I33217@	I3-3217U	CR	1.8G	SA00005L5C0(S IC AV8063801058401 SR0N9 L1 1.8G BGA 1023 ABO !)	
I53317@	I5-3317U	CR	1.7G	SA00005K6B0(S IC AV8063801058002 SR0N8 L1 1.7G ABO!)	
I73517@	I7-3517U	CR	1.9G	SA00005K5B0(S IC AV8063801057605 SR0N6 L1 1.9G BGA 1023 ABO !)	

GPU BOM Config + GPIO

N13P-GS-A2	R3	SA0000518A0 (S IC N13P-GS-A2 FCBGA 908P GPU ABO !)	

VRAM BOM Config

X76364BOL03:	1G HYN	GDDR5	64*32	2G	SA00004GD30(S IC D5 64M32/2.5G H5GQ2H24MFR-T2C ABO!)	HYNMFR@/
X76364BOL04:	1G HYN	GDDR5	64*32	2G	SA00004GD50(S IC D5 64M32/2.5G H5GQ2H24AFR-T2C ABO!)	HYNAFR@/

RAM BOM Config

X76364BOL11:	2GB*4 HYNIX	HYNIX	2GB	1333	SA00005FV10(S IC D3 256MX16/1333 H5TC4G63MFR-H9A FBGA 96P ABO !)	RAM@//HYNIX@/
X76364BOL12:	2GB*4 ELPDIA	ELPDIA	2GB	1333	SA000059110(S IC D3 256M16 EDJ4216EBBG-DJ-F ABO!)	RAM@//ELPIDA@/

BOM Config

LA8203 UMA :	9012@/UMAO@/DRAM@/	+CPU config
LA8203 Optimus :	9012@/DIS@/DRAM@/VRAM@/	+CPU config

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

	Board ID	PCB Revision
	0	
	1	
	2	0.1
	3	0.2
*	4	1.0
	5	
	6	
	7	

USB Port Table

USB 2.0	Port	3 External USB Port
EHCI1	0	USB Port(Right 2.0),USB Charger
	1	USB Port(Mid 2.0)
	2	
	3	
	4	
	5	
	6	
	7	
EHCI2	8	BT (WLAN)
	9	USB port(Left 2.0)
	10	Camera
	11	Mini Card(MSATA)
	12	
	13	

USB 3.0	Port	
XHCI	1	USB Port(Right 3.0)
	2	USB Port(Mid 3.0)
	3	
	4	

BTO Option Table

BTO Item	BOM Structure	
Unpop	@	
EC 9012	9012@	
EC 930	930@	
Connector	CONN@	
ALC281	281@	
UMA Only	UMAO@	
OPT	DIS@	
HR CPU I3-2367M	I32367@	P.56
HR CPU I3-2377M	I32377@	P.56
HR CPU I5-2467M	I52467@	P.56
CR CPU I3-3217M	I33217@	P.56
CR CPU I5-3317M	I53317@	P.56
CR CPU I7-3517M	I73517@	P.56
GDDR5 HYNIX MFR	HYNMFR@	X76364BOL03 P.27
GDDR5 HYNIX AFR	HYNAFR@	X76364BOL04 P.27
DRAM	RAM@	for X76 RAM GPIO P.18
DRAM HYNIX	HYNIX@	for X76364BOL11: P.56
DRAM ELPIDA	ELPIDA@	for X76364BOL12: P.56
VRAM X76	VRAM@	MB VRAM X76 P.56
DRAM X76	DRAM@	MB DRAM X76 P.56

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PEG_ICOMPI and RCOMPO signals should be shorted and routed
with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils
- typical impedance = 14.5 mohms

+1.05VS_VTT

R249
24.9_0402_1%

W=12mil L=500mil S=15mil

PEG_COMP

PEG_GTX_HRX_N[0..15] 22
PEG_GTX_HRX_P[0..15] 22
PEG_HTX_C_GRX_N[0..15] 22
PEG_HTX_C_GRX_P[0..15] 22

UCPU1A

DMI
Intel(R) FDI
PCI EXPRESS -- GRAPHICS
eDP

15 DMI_CRX_PTX_N0	M2	DMI_RX#[0]	
15 DMI_CRX_PTX_N1	P6	DMI_RX#[1]	
15 DMI_CRX_PTX_N2	P1	DMI_RX#[2]	
15 DMI_CRX_PTX_N3	P10	DMI_RX#[3]	
15 DMI_CRX_PTX_P0	N3	DMI_RX[0]	
15 DMI_CRX_PTX_P1	P7	DMI_RX[1]	
15 DMI_CRX_PTX_P2	P3	DMI_RX[2]	
15 DMI_CRX_PTX_P3	P11	DMI_RX[3]	
15 DMI_CTX_PRX_N0	K1	DMI_TX#[0]	
15 DMI_CTX_PRX_N1	M8	DMI_TX#[1]	
15 DMI_CTX_PRX_N2	N4	DMI_TX#[2]	
15 DMI_CTX_PRX_N3	R2	DMI_TX#[3]	
15 DMI_CTX_PRX_P0	K3	DMI_TX[0]	
15 DMI_CTX_PRX_P1	M7	DMI_TX[1]	
15 DMI_CTX_PRX_P2	P4	DMI_TX[2]	
15 DMI_CTX_PRX_P3	T3	DMI_TX[3]	
15 FDI_CTX_PRX_N0	U7	FDI0_TX#[0]	
15 FDI_CTX_PRX_N1	W11	FDI0_TX#[1]	
15 FDI_CTX_PRX_N2	W1	FDI0_TX#[2]	
15 FDI_CTX_PRX_N3	AA6	FDI0_TX#[3]	
15 FDI_CTX_PRX_N4	W6	FDI1_TX#[0]	
15 FDI_CTX_PRX_N5	V4	FDI1_TX#[1]	
15 FDI_CTX_PRX_N6	Y2	FDI1_TX#[2]	
15 FDI_CTX_PRX_N7	AC9	FDI1_TX#[3]	
15 FDI_CTX_PRX_P0	U6	FDI0_TX[0]	
15 FDI_CTX_PRX_P1	W10	FDI0_TX[1]	
15 FDI_CTX_PRX_P2	W3	FDI0_TX[2]	
15 FDI_CTX_PRX_P3	AA7	FDI0_TX[3]	
15 FDI_CTX_PRX_P4	W7	FDI1_TX[0]	
15 FDI_CTX_PRX_P5	T4	FDI1_TX[1]	
15 FDI_CTX_PRX_P6	AA3	FDI1_TX[2]	
15 FDI_CTX_PRX_P7	AC8	FDI1_TX[3]	
15 FDI_FSYNC0	AA11	FDI0_FSYNC	
15 FDI_FSYNC1	AC12	FDI1_FSYNC	
15 FDI_INT	U11	FDI_INT	
15 FDI_LSYNC0	AA10	FDI0_LSYNC	
15 FDI_LSYNC1	AC8	FDI1_LSYNC	

PEG_ICOMPI	G3		
PEG_ICOMPO	G1		
PEG_RCOMPO	G4		
PEG_RX#[0]	H22	PEG_GTX_C_HRX_N15	C262 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N15
PEG_RX#[1]	J21	PEG_GTX_C_HRX_N14	C244 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N14
PEG_RX#[2]	B22	PEG_GTX_C_HRX_N13	C264 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N13
PEG_RX#[3]	D21	PEG_GTX_C_HRX_N12	C246 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N12
PEG_RX#[4]	A19	PEG_GTX_C_HRX_N11	C267 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N11
PEG_RX#[5]	D17	PEG_GTX_C_HRX_N10	C248 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N10
PEG_RX#[6]	B14	PEG_GTX_C_HRX_N9	C268 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N9
PEG_RX#[7]	D13	PEG_GTX_C_HRX_N8	C250 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N8
PEG_RX#[8]	A11	PEG_GTX_C_HRX_N7	C270 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N7
PEG_RX#[9]	B10	PEG_GTX_C_HRX_N6	C252 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N6
PEG_RX#[10]	G8	PEG_GTX_C_HRX_N5	C272 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N5
PEG_RX#[11]	A8	PEG_GTX_C_HRX_N4	C254 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N4
PEG_RX#[12]	B6	PEG_GTX_C_HRX_N3	C274 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N3
PEG_RX#[13]	H8	PEG_GTX_C_HRX_N2	C257 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N2
PEG_RX#[14]	E5	PEG_GTX_C_HRX_N1	C276 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N1
PEG_RX#[15]	K7	PEG_GTX_C_HRX_N0	C259 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_N0
PEG_RX[0]	K22	PEG_GTX_C_HRX_P15	C263 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P15
PEG_RX[1]	K19	PEG_GTX_C_HRX_P14	C245 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P14
PEG_RX[2]	C21	PEG_GTX_C_HRX_P13	C265 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P13
PEG_RX[3]	D19	PEG_GTX_C_HRX_P12	C247 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P12
PEG_RX[4]	C19	PEG_GTX_C_HRX_P11	C266 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P11
PEG_RX[5]	D16	PEG_GTX_C_HRX_P10	C249 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P10
PEG_RX[6]	C13	PEG_GTX_C_HRX_P9	C269 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P9
PEG_RX[7]	D12	PEG_GTX_C_HRX_P8	C251 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P8
PEG_RX[8]	C11	PEG_GTX_C_HRX_P7	C271 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P7
PEG_RX[9]	C9	PEG_GTX_C_HRX_P6	C253 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P6
PEG_RX[10]	F8	PEG_GTX_C_HRX_P5	C273 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P5
PEG_RX[11]	C8	PEG_GTX_C_HRX_P4	C255 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P4
PEG_RX[12]	C5	PEG_GTX_C_HRX_P3	C275 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P3
PEG_RX[13]	H6	PEG_GTX_C_HRX_P2	C256 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P2
PEG_RX[14]	F6	PEG_GTX_C_HRX_P1	C277 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P1
PEG_RX[15]	K6	PEG_GTX_C_HRX_P0	C258 1 2 DIS@ 0.22U_0402_6.3V6K PEG_GTX_HRX_P0
PEG_TX#[0]	G22	PEG_HTX_GRX_N15	C597 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N15
PEG_TX#[1]	C23	PEG_HTX_GRX_N14	C576 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N14
PEG_TX#[2]	D23	PEG_HTX_GRX_N13	C594 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N13
PEG_TX#[3]	F21	PEG_HTX_GRX_N12	C574 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N12
PEG_TX#[4]	H19	PEG_HTX_GRX_N11	C593 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N11
PEG_TX#[5]	C17	PEG_HTX_GRX_N10	C572 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N10
PEG_TX#[6]	K15	PEG_HTX_GRX_N9	C591 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N9
PEG_TX#[7]	F17	PEG_HTX_GRX_N8	C570 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N8
PEG_TX#[8]	F14	PEG_HTX_GRX_N7	C589 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N7
PEG_TX#[9]	A15	PEG_HTX_GRX_N6	C568 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N6
PEG_TX#[10]	J14	PEG_HTX_GRX_N5	C587 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N5
PEG_TX#[11]	H13	PEG_HTX_GRX_N4	C566 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N4
PEG_TX#[12]	M10	PEG_HTX_GRX_N3	C584 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N3
PEG_TX#[13]	F10	PEG_HTX_GRX_N2	C564 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N2
PEG_TX#[14]	D9	PEG_HTX_GRX_N1	C582 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N1
PEG_TX#[15]	J4	PEG_HTX_GRX_N0	C562 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_N0
PEG_TX[0]	F22	PEG_HTX_GRX_P15	C596 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P15
PEG_TX[1]	A23	PEG_HTX_GRX_P14	C575 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P14
PEG_TX[2]	D24	PEG_HTX_GRX_P13	C595 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P13
PEG_TX[3]	E21	PEG_HTX_GRX_P12	C573 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P12
PEG_TX[4]	G19	PEG_HTX_GRX_P11	C592 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P11
PEG_TX[5]	B18	PEG_HTX_GRX_P10	C571 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P10
PEG_TX[6]	K17	PEG_HTX_GRX_P9	C590 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P9
PEG_TX[7]	G17	PEG_HTX_GRX_P8	C569 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P8
PEG_TX[8]	E14	PEG_HTX_GRX_P7	C588 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P7
PEG_TX[9]	C15	PEG_HTX_GRX_P6	C567 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P6
PEG_TX[10]	K13	PEG_HTX_GRX_P5	C586 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P5
PEG_TX[11]	G13	PEG_HTX_GRX_P4	C565 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P4
PEG_TX[12]	K10	PEG_HTX_GRX_P3	C585 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P3
PEG_TX[13]	G10	PEG_HTX_GRX_P2	C563 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P2
PEG_TX[14]	D8	PEG_HTX_GRX_P1	C583 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P1
PEG_TX[15]	K4	PEG_HTX_GRX_P0	C561 1 2 DIS@ 0.22U_0402_6.3V6K PEG_HTX_C_GRX_P0

IVY-BRIDGE_BGA1023
@

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms
can't be left floating
,even if disable eDP function...

+1.05VS_VTT

R247
24.9_0402_1%

W=12mil L=500mil S=15mil

EDP_COMP
EDP_HPD#

	AF3	eDP_COMPIO
	AD2	eDP_ICOMPO
	AG11	eDP_HPD#
29 EDP_AUXN	AG4	eDP_AUX#
29 EDP_AUXP	AF4	eDP_AUX
29 EDP_TXN0	AC3	eDP_TX#[0]
	AC4	eDP_TX#[1]
	AE11	eDP_TX#[2]
	AE7	eDP_TX#[3]
29 EDP_TXP0	AC1	eDP_TX[0]
	AA4	eDP_TX[1]
	AE10	eDP_TX[2]
	AE6	eDP_TX[3]

Add eDP circuit

+1.05VS_VTT

R250
1K_0402_5%

29 EDP_HPD# — EDP_HPD#

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

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0921 LVDS@->@

+1.05VS_VTT

CLK_CPU_DPLL# R517 2 @ 1 1K_0402_5%

CLK_CPU_DPLL R516 2 @ 1 1K_0402_5%

Checklist1.5 P.67 Graphis Disable Guide
DIS only SKU eDP disable
DPLL_REF_SSCLK PD 1K_5% to GND
DPLL_REF_SSCLK# PH 1K_5% to +1.05VS_VTT

PCH->CPU
UNCOREPWRGOOD:非CORE外的電OK
SM_DRAMPWROK:DRAM power ok
RESET#:都ok後請CPU做reset

PROC_SELECT#
PH VCPLL and connect to PCH DF_TVS

偵測CPU有無安裝

XBOX 三紅功能

Follow DG 1.5& Tacoma_Fall2 1.0

reserve

C614 2 @ 1 0.1U_0402_16V4Z H_CPUPWRGD

R292 2 1 10K_0402_5%

follow Checklist 1.5

17 H_SNB_IVB#

T33_PAD @ H_CATERR#

18,36 H_PECI

+1.05VS_VTT R534 2 1 62_0402_5%

36,43 H_PROHOT#

R533 56_0402_5%

18 H_THRMTRIP#

UCPU1B

F49	PROC_SELECT#	MISC
C57	PROC_DETECT#	
C49	CATERR#	THERMAL
A48	PECI	
C45	PROCHOT#	
D45	THERMTRIP#	
C48	PM_SYNC	PWR MANAGEMENT
B46	UNCOREPWRGOOD	
BE45	SM_DRAMPWROK	
D44	RESET#	

IVY-BRIDGE_BGA1023

@

CLOCKS

BCLK	J3	CLK_CPU_DMI 14
BCLK#	H2	CLK_CPU_DMI# 14
DPLL_REF_CLK	AG3	CLK_CPU_DPLL
DPLL_REF_CLK#	AG1	CLK_CPU_DPLL#

CLK_CPU_DPLL 14
CLK_CPU_DPLL# 14

SM_RCOMP0,SM_RCOMP1
W=20mil L=500mil S=13mil

SM_RCOMP2
W=15mil L=500mil S=13mil

DDR3 MISC

SM_DRAMRST# AT30 SM_DRAMRST# SM_DRAMRST# 6

SM_RCOMP[0]	BF44	SM_RCOMP0 R272 2 1	140_0402_1%
SM_RCOMP[1]	BE43	SM_RCOMP1 R273 2 1	25.5_0402_1%
SM_RCOMP[2]	BG43	SM_RCOMP2 R267 2 1	200_0402_1%

DDR3 Compensation Signals

JTAG & BPM

PRDY#	N53	
PREQ#	N55	
TCK	L56	XDP_TCK @ PAD T19
TMS	L55	XDP_TMS @ PAD T20
TRST#	J58	XDP_TRST# @ PAD T21
TDI	M60	XDP_TDI @ PAD T34
TDO	L59	XDP_TDO @ PAD T35
DBR#	K58	XDP_DBRESET# XDP_DBRESET# 15

BPM#[0]	G58
BPM#[1]	E55
BPM#[2]	E59
BPM#[3]	G55
BPM#[4]	G59
BPM#[5]	H60
BPM#[6]	J59
BPM#[7]	J61

Follow DG 1.5 & Tacoma_Fall2 1.0
Buffered reset to CPU

Use open drain logic gate:
+1.05VS_VTT PH pop 75ohm
series resister pop 43ohm

+3VS

C617 0.1U_0402_16V4Z

R550 0_0402_5%

U45

+1.05VS_VTT

R546 75_0402_5%

R544 43_0402_1%

17,32,33,36,37 PLT_RST# PLT_RST# BUFO_CPU_RST# BUF_CPU_RST#

SN74LVC1G07DCKR_SC70-5

RESET#:都ok後請CPU做reset

18 H_CPUPWRGD R305 H_CPUPWRGD_R B46

0_0402_5%

UNCOREPWRGOOD:非CORE外的電OK

15 H_PM_SYNC

PM_DRAM_PWRGD_R BE45

SM_DRAMPWROK:DRAM power ok

BUF_CPU_RST#

Follow DG 1.5 & Tacoma_Fall2 1.0

Use open drain logic gate:
+1.5V_CPU_VDDQ PH pop 200ohm
series resister pop 130ohm

+3VALW

C228 0.1U_0402_16V4Z

+1.5V_CPU_VDDQ

R238 200_0402_5%

U18

15 SYS_PWROK

15 PM_DRAM_PWRGD

PM_SYS_PWRGD_BUF

R237

PM_DRAM_PWRGD_R 130_0402_5%

MC74VHC1G09DFT2G_SC70-5

+3VS

XDP_DBRESET# R312 2 1 1K_0402_5%

Tacoma_Fall2 1.0 PH 1K +3VS
Check list 1.5 PH 1K +3VS
Debug port DG1.1-1.3 50~5K ohm

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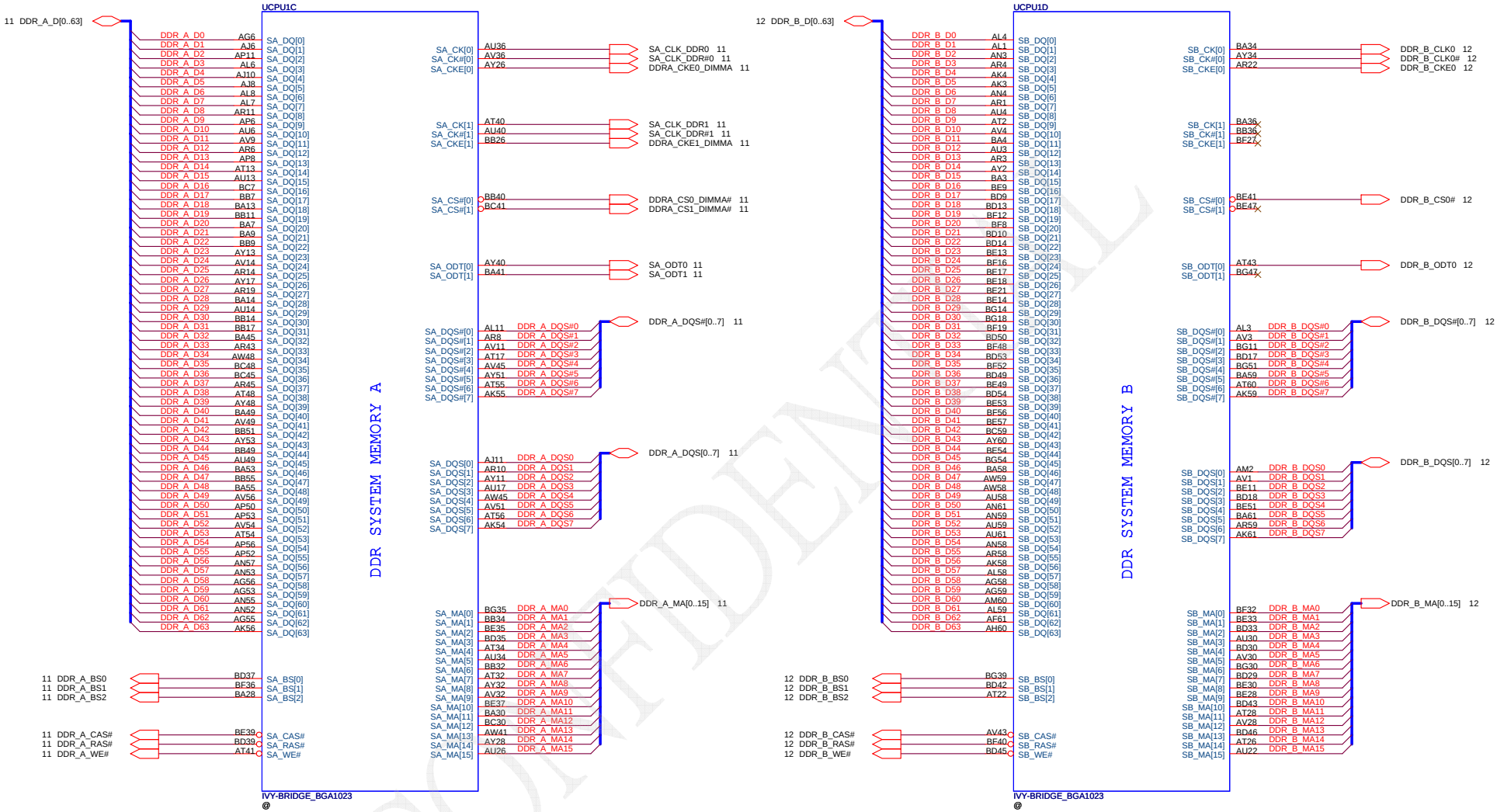

Follow CRB1.0

CPU通知DIMM做reset

5 SM_DRAMRST#

14 RST_GATE

36 EC_RST_GATE

R216 0_0402_5%

R212 1K_0402_5%

+1.5V

Q16 BSS138_G_SOT23-3

R219 1K_0402_5%

DIMM_DRAMRST# 11,12

R217 4.99K_0402_1%

R504 0_0402_5%

R505 0_0402_5%

C190 0.047U_0402_16V7K

RST_GATE_R 11,12

S0
DRAMRST_CNTRL_PCH hgih ,MOS ON
SM_DRAMRST# HIGH,DDR3 DRAMRST# HIGH
Dimm not reset

S3
DRAMRST_CNTRL_PCH Low ,MOS OFF
SM_DRAMRST# lo,DDR3 DRAMRST# HIGH
Dimm not reset

S4,5
DRAMRST_CNTRL_PCH Low ,MOS OFF
SM_DRAMRST# lo,DDR3 DRAMRST# low
Dimm reset

Address 0~13:For 128*16
Address 0~14:For 256*16
Address 0~15:For 512*16

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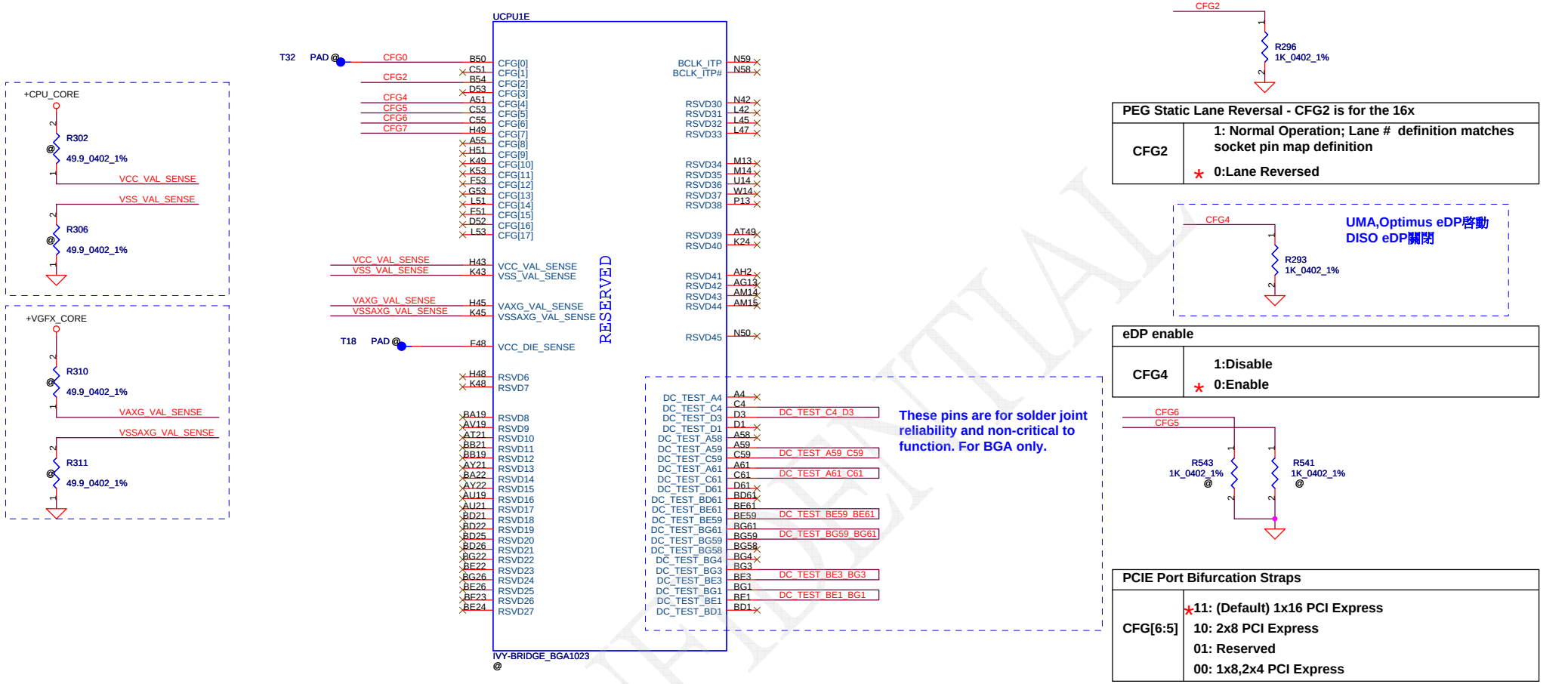
CFG Straps for Processor

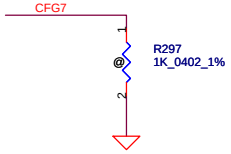


These pins are for solder joint reliability and non-critical to function. For BGA only.

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

eDP enable	
CFG4	1:Disable * 0:Enable

PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) 1x16 PCI Express 10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express



PEG DEFER TRAINING	Tacoma_Fall2 1.0 P.12
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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POWER

ULV type
DC 33A

8.5A

UCPU1F

+CPU_CORE

INTEL Recommend VCC
4*470UF,12*22uF(0805) and 35*2.2uF(0402)
PD0.8
CAP at P.51

CORE SUPPLY

VCC[1] A26
VCC[2] A29
VCC[3] A31
VCC[4] A34
VCC[5] A35
VCC[6] A38
VCC[7] A39
VCC[8] A42
VCC[9] C26
VCC[10] C27
VCC[11] C32
VCC[12] C34
VCC[13] C37
VCC[14] C39
VCC[15] C42
VCC[16] D27
VCC[17] D32
VCC[18] D34
VCC[19] D37
VCC[20] D39
VCC[21] D42
VCC[22] E26
VCC[23] E28
VCC[24] E32
VCC[25] E34
VCC[26] E37
VCC[27] E38
VCC[28] F25
VCC[29] F26
VCC[30] F28
VCC[31] F32
VCC[32] F34
VCC[33] F37
VCC[34] F38
VCC[35] F42
VCC[36] G42
VCC[37] H25
VCC[38] H26
VCC[39] H28
VCC[40] H29
VCC[41] H32
VCC[42] H34
VCC[43] H35
VCC[44] H37
VCC[45] H38
VCC[46] H40
VCC[47] J25
VCC[48] J26
VCC[49] J28
VCC[50] J29
VCC[51] J32
VCC[52] J34
VCC[53] J35
VCC[54] J37
VCC[55] J38
VCC[56] J40
VCC[57] J42
VCC[58] K26
VCC[59] K27
VCC[60] K29
VCC[61] K32
VCC[62] K34
VCC[63] K35
VCC[64] K37
VCC[66] K39
VCC[67] K42
VCC[68] L25
VCC[69] L28
VCC[70] L33
VCC[71] L36
VCC[72] L40
VCC[73] N26
VCC[74] N30
VCC[75] N34
VCC[76] N38

PEG IO AND DDR IO

+1.05VS_VTT

For DDR

VCCIO[1] AF46
VCCIO[3] AG48
VCCIO[4] AG50
VCCIO[5] AG51
VCCIO[6] AJ17
VCCIO[7] AJ21
VCCIO[8] AJ25
VCCIO[9] AJ43
VCCIO[10] AJ47
VCCIO[11] AK50
VCCIO[12] AK51
VCCIO[13] AL14
VCCIO[14] AL15
VCCIO[15] AL16
VCCIO[16] AL20
VCCIO[17] AL22
VCCIO[18] AL26
VCCIO[19] AL45
VCCIO[20] AL48
VCCIO[21] AM16
VCCIO[22] AM17
VCCIO[23] AM21
VCCIO[24] AM43
VCCIO[25] AM47
VCCIO[26] AN20
VCCIO[27] AN42
VCCIO[28] AN45
VCCIO[29] AN48

INTEL Recommend VCCIO
2*330UF,10*10uF(0603) and 26*1uF(0402)
PD0.8
CAP at P.51

For PEG

VCCIO[30] AA14
VCCIO[31] AA15
VCCIO[32] AB17
VCCIO[33] AB20
VCCIO[34] AC13
VCCIO[35] AD16
VCCIO[36] AD18
VCCIO[37] AD21
VCCIO[38] AE14
VCCIO[39] AE15
VCCIO[40] AE16
VCCIO[41] AF18
VCCIO[42] AF20
VCCIO[43] AG15
VCCIO[44] AG16
VCCIO[45] AG17
VCCIO[46] AG20
VCCIO[47] AG21
VCCIO[48] AJ14
VCCIO[49] AJ15

+1.05VS_VTT

VCCIO50 W16
VCCIO51 W17

+3VS

R521 10K_0402_5% @
VCCIO_SEL
R522 10K_0402_5% @

VCCIO_SEL after Ivy bridge ES2 Voltage support		
BC22	*	1/NC : (Default) +1.05VS_VTT 0: +1.0VS_VTT

QUIET RAILS

VCCIO_SEL
BC22 VCCIO_SEL

+1.05VS_VTT

VCCPQE[1] AM25
VCCPQE[2] AN22

C553 1U_0402_6.3V6K

+1.05VS_VTT

R531 130_0402_5%

+1.05VS_VTT

R529 75_0402_5%

Place the PU resistors close to CPU

SVID

VIDALERT# A44
VIDSCLK B43
VIDSOUT C44

H_CPU_SVIDALRT#
H_CPU_SVIDCLK
H_CPU_SVIDDAT

R528 43_0402_1%
R527 0_0402_5%
R530 0_0402_5%

VR_SVID_ALRT# 49
VR_SVID_CLK 49
VR_SVID_DAT 49

+CPU_CORE

Place the PU resistors close to VR

R281 100_0402_1%

SENSE LINES

VCC_SENSE F43
VSS_SENSE G43

VCCSENSE_R
VSSSENSE_R

R282 0_0402_5%
R289 0_0402_5%

VCCSENSE 49
VSSSENSE 49

R513 10_0402_5%

+1.05VS_VTT

VCCIO_SENSE AN16
VSS_SENSE_VCCIO AN17

VSSIO_SENSE

VCCIO_SENSE 47

R512 10_0402_5%

Check list 1.5

R288 100_0402_1%

Should change to connect form power cirucit & layout differential with VCCIO_SENSE.

IVY-BRIDGE_BGA1023
@

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POWER

UCPU1G

INTEL Recommend VAXG
2*470uF,6*22uF(0805) and 6*10uF(0603)
11*1U(0402)
PD0.8

+VGFX_CORE — DC 29A

VAXG[1..56] — GRAPHICS DDR3 - 1.5V RAILS

INTEL Recommend VCCPLL
1*330uF,2*1uF(0402)
PD0.8

CR CheckList Rev1.5

+VGFX_CORE
R308 100_0402_5%
R309 100_0402_5%

49 VCC_AXG_SENSE — F45 VAXG_SENSE
49 VSS_AXG_SENSE — G45 VSSAXG_SENSE
SENSE LINES

1.2A

+1.8VS — Place BOT OUT Conn

SGA00001700 S POLY C 220U
220U 2.5V M B2 ESR35 TPE H1.9

C261 @ 220U_B2_2.5VM_R35
C281 10U_0402_6.3V6K
C280 10U_0402_6.3V6K

BB3 VCCPLL[1]
BC1 VCCPLL[2]
BC4 VCCPLL[3]
1.8V RAIL

INTEL Recommend VCCSA
1*330uF,5*10uF(0603) ,5*1uF(0402)
PD0.8

+VCCSA — 6A

Place TOP IN BGA

SGA20331E10 S POLY C 330U
2V Y D2 LESR9M EEFSX H1.9

C242 330U_D2_2V_Y
C309 C302 C300 C301 C308 10U_0402_6.3V6K

Place BOT OUT BGA

C577 C560 C555 C579 C559 10U_0603_6.3V6M

L17 VCCSA[1]
L21 VCCSA[2]
N16 VCCSA[3]
N20 VCCSA[4]
N22 VCCSA[5]
P17 VCCSA[6]
P20 VCCSA[7]
R16 VCCSA[8]
R18 VCCSA[9]
R21 VCCSA[10]
U15 VCCSA[11]
V16 VCCSA[12]
V17 VCCSA[13]
V18 VCCSA[14]
V21 VCCSA[15]
W20 VCCSA[16]
SA RAIL

IVY-BRIDGE_BGA1023
@

SM_VREF — AY43 +V_SM_VREF
VREF

+V_SM_VREF should have 20 mil trace width

+1.5V_CPU_VDDQ
R266 1K_0402_5%
R268 1K_0402_5%

SA_DIMM_VREFDQ — BE7 SA_DIMM_VREFDQ
SB_DIMM_VREFDQ — BG7 SB_DIMM_VREFDQ
SA_DIMM_VREFDQ 12
SB_DIMM_VREFDQ 11
C352 0.1U_0402_16V4Z
R519 1K_0402_1%
R518 1K_0402_1%

SA_DIMM_VREFDQ
SB_DIMM_VREFDQ
Check list1.5 P18 M1 default M3 no stuff

INTEL Recommend VDDQ
1*330uF,8*10uF(0603) ,10*1uF(0402)
PD0.8

5A

VDDQ[1..26] — AJ28 AJ33 AJ36 AJ40 AL30 AL34 AL38 AL42 AM33 AM36 AM40 AN30 AN34 AN38 AR26 AR28 AR30 AR32 AR34 AR36 AR40 AV41 AW26 BA40 BB28 BG33
DDR3 - 1.5V RAILS

Place TOP IN BGA

+1.5V_CPU_VDDQ — J12 JUMP_43X118 @ — +1.5VS

C321 C329 C351 C348 C328 C312 C318 C320 C349 C316 10U_0402_6.3V6K
C286 330U_D2_2V_Y

Place BOT OUT BGA

C340 C337 C338 C296 C295 C299 C339 C298 10U_0603_6.3V6M

SGA20331E10 S POLY C 330U
2V Y D2 LESR9M EEFSX H1.9

VCCDQ[1] AM28
VCCDQ[2] AN26
+1.5V_CPU_VDDQ
C317 1U_0402_6.3V6K
QUIET RAILS

VDDQ_SENSE — BC43
VSS_SENSE_VDDQ — BA43
SENSE LINES

VCCSA_SENSE — U10
CPU EDS1.3 P.93
VCCSA_VID0 Must PD
VCCSA_SENSE 48

VCCSA_VID[0] — D48 H_VCCSA_VID0 — H_VCCSA_VID0 48
VCCSA_VID[1] — D49 H_VCCSA_VID1 — H_VCCSA_VID1 48
R248 0_0402_5%
VCCSA VID lines

VCCSA				
VID0	VID1	Vout	HR	CR
0	0	0.9V	V	V
0	1	0.85V	V	V
1	0	0.775V	X	V
1	1	0.75V	X	V

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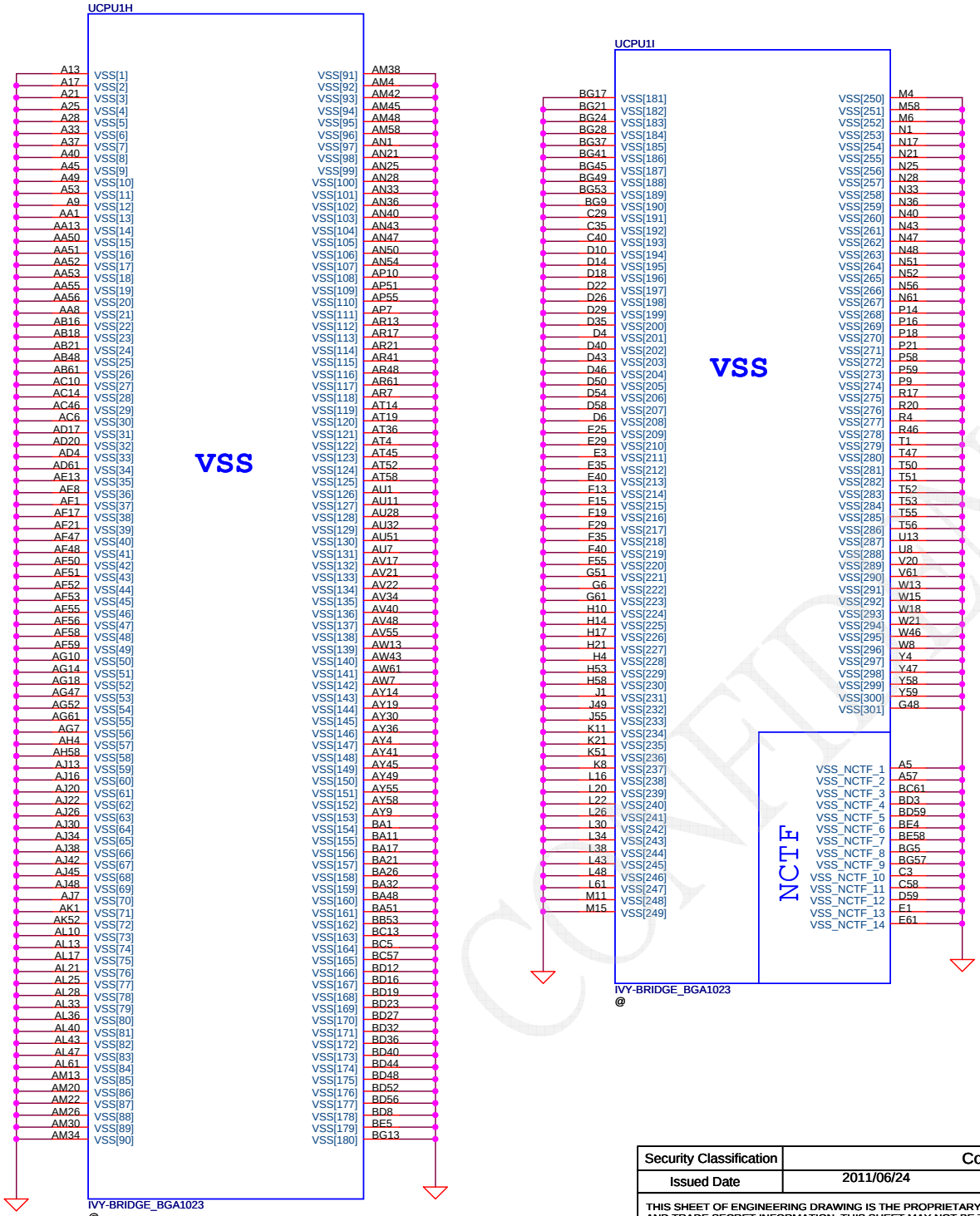

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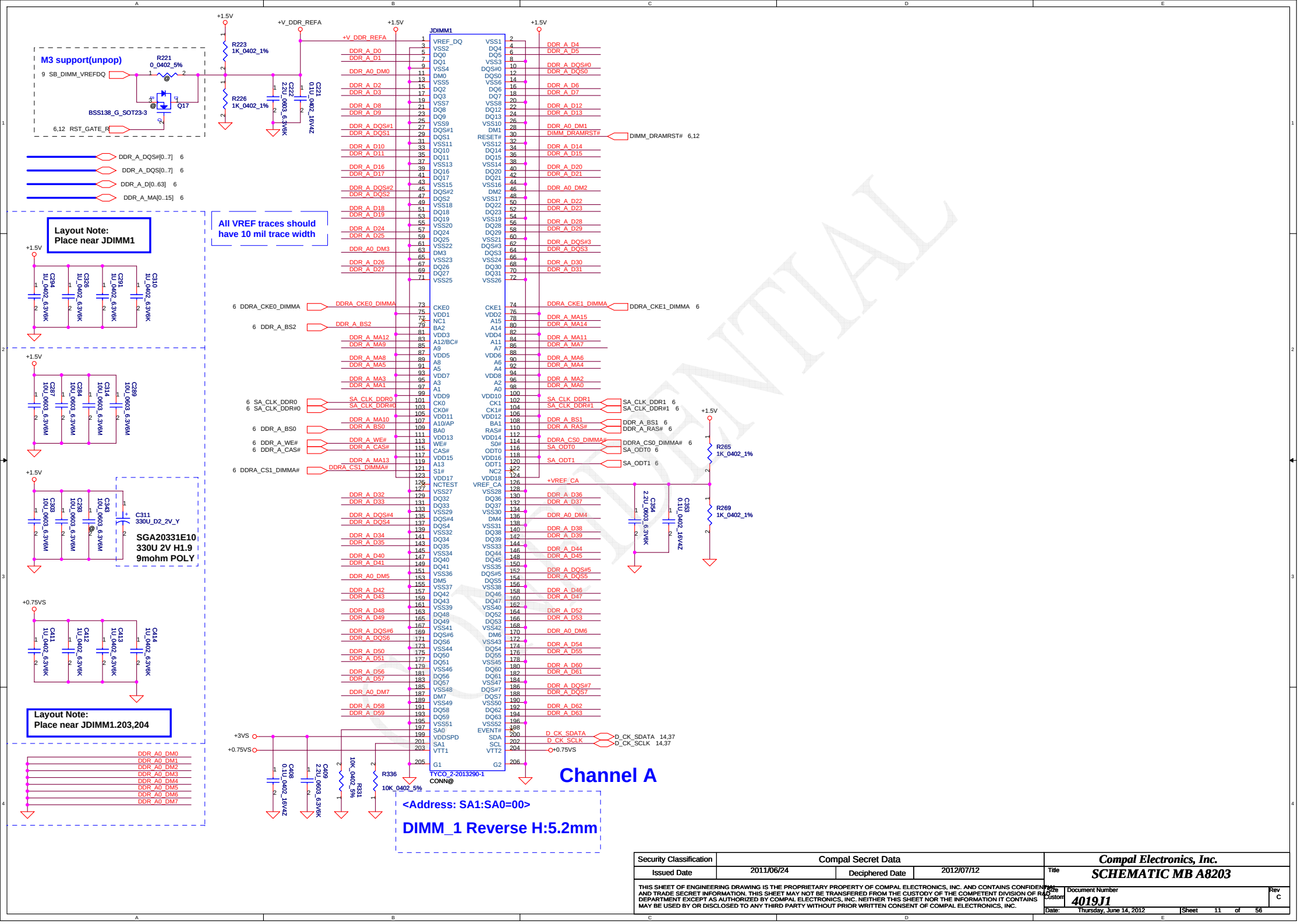

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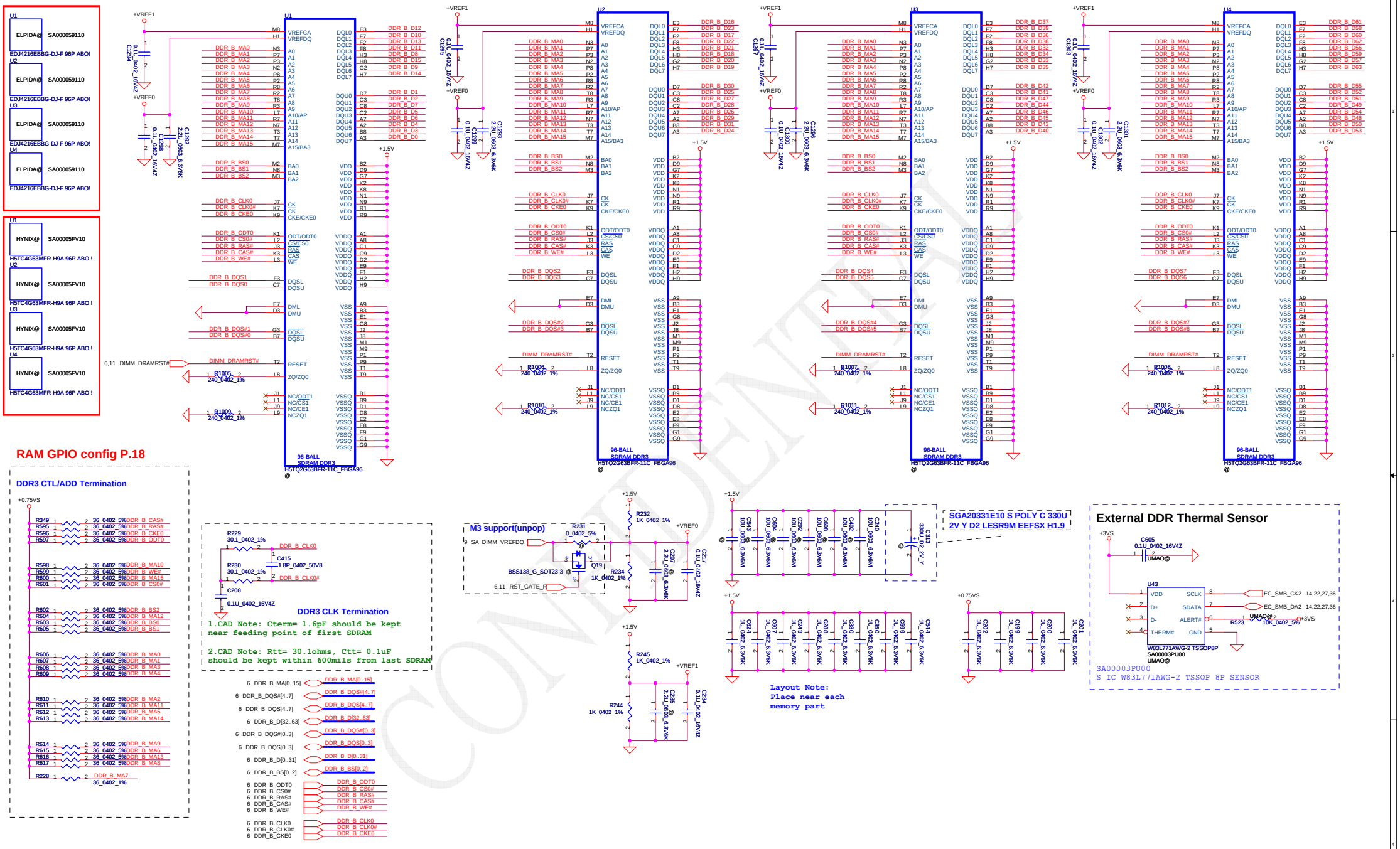

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RTCRST close RAM door J1

INTVRMEN
★ H：Integrated VRM enable
L：Integrated VRM disable
(INTVRMEN should always be pull high.)

HDA_SDO
ME debug mode,this signal has a weak internal PD
★ Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]

This signal has a weak internal pull-down

On Die PLL VR Select is supplied by
★1.5V when sampled high
1.8V when sampled low
Needs to be pulled High for Huron River platfrom

HIGH= Enable (No Reboot)Disable TCO timer system reboot feature
★ LOW= Disable (Default internal PD)

Prevent back drive issue.

20mil

20mil

20mil

L=500mil S=15mil

L=500mil S=15mil

SPI ROM FOR ME (4MB)
Footprint 200mil

SPI ROM FOR ME (2MB)
Footprint 200mil

Reserve for EMI

UM77 not support

UM77 not support

No use PH 10K +3VS

GPIO19 has internal Pull up

Debug Port DG 1.2 PH 4.7K +3VS

Switchable Graphic (MUX)	
	GPIO21
Switchable	0
★ Non SG	1

Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
-	1	0
★ SPI	1	1

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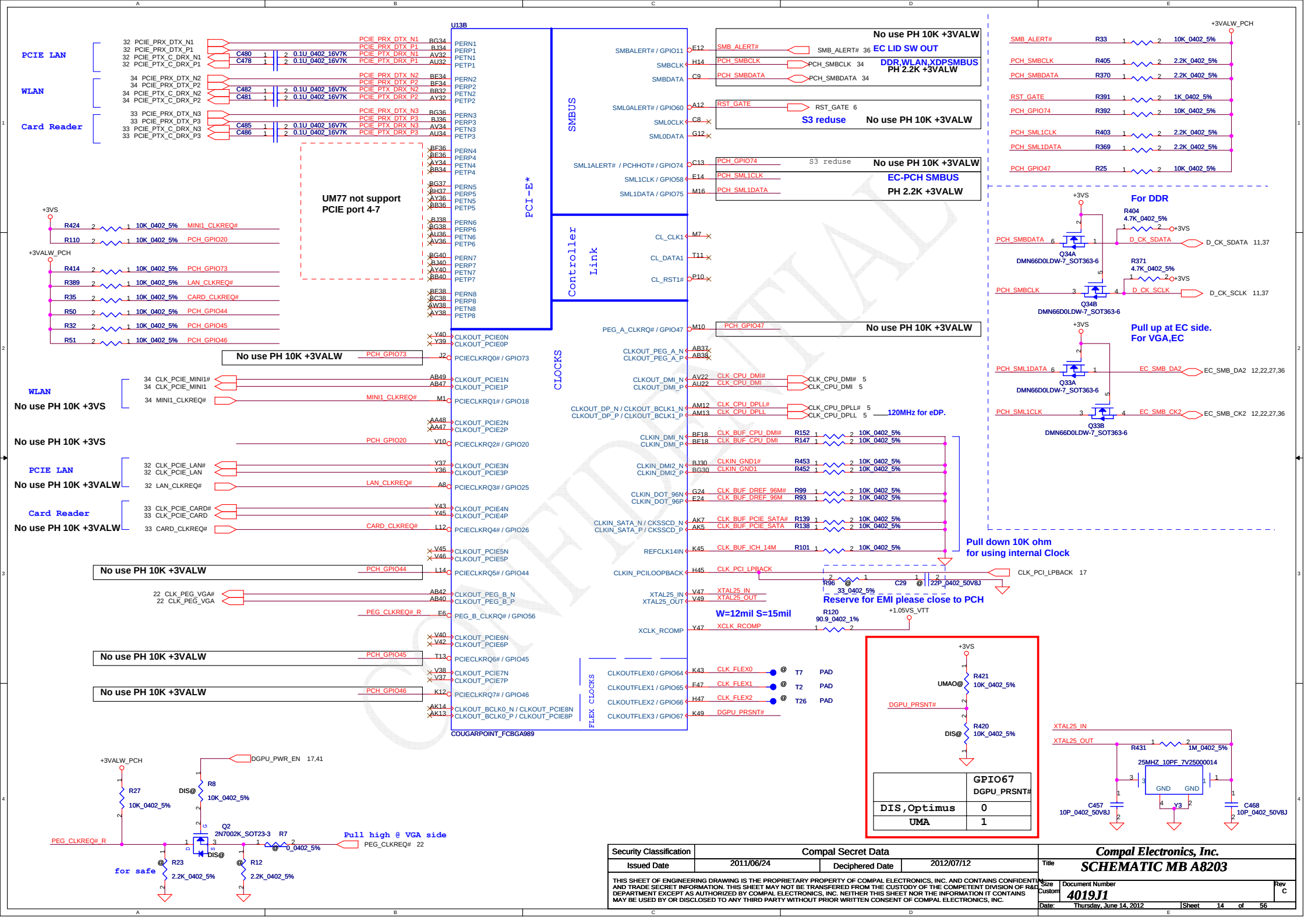

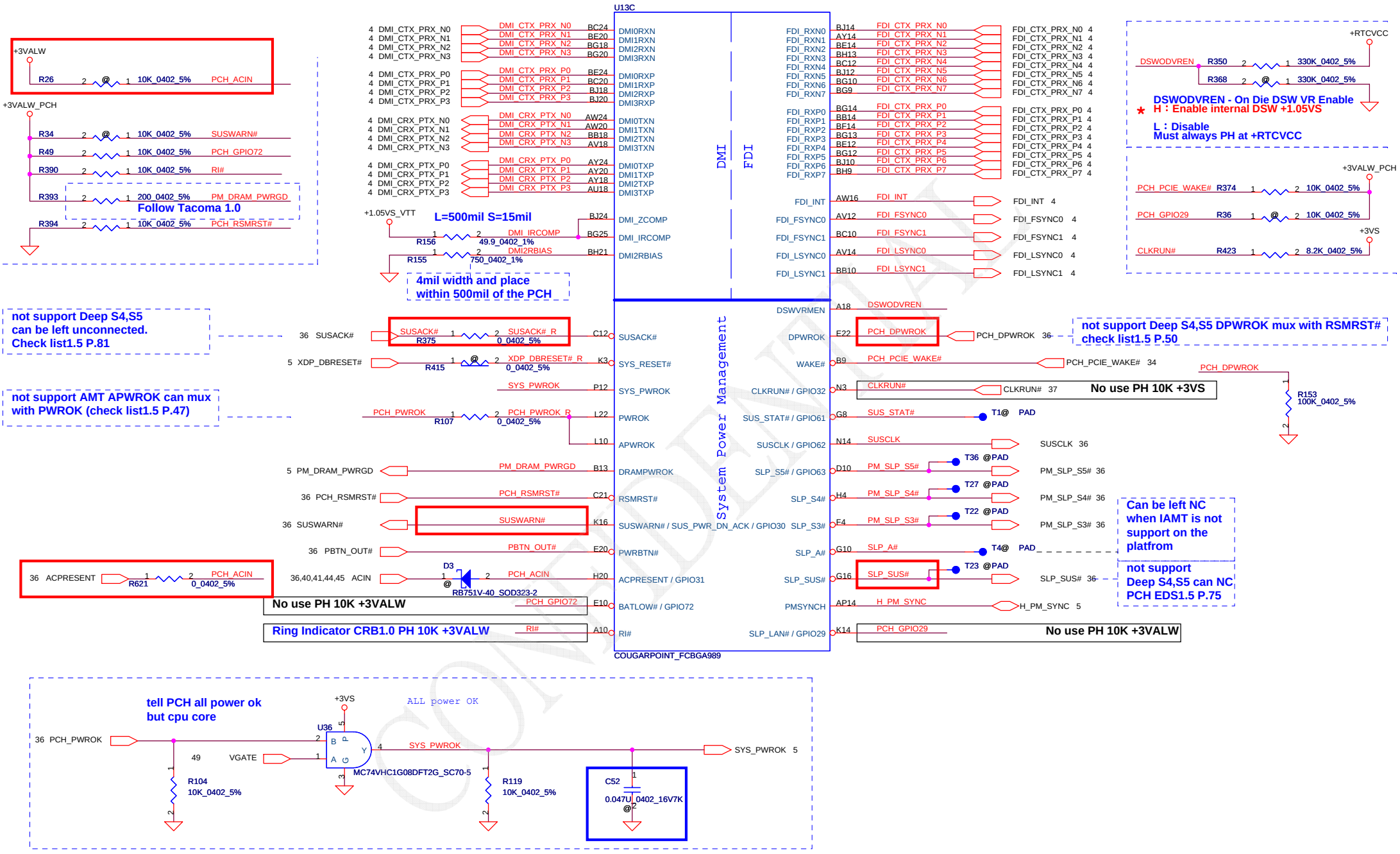

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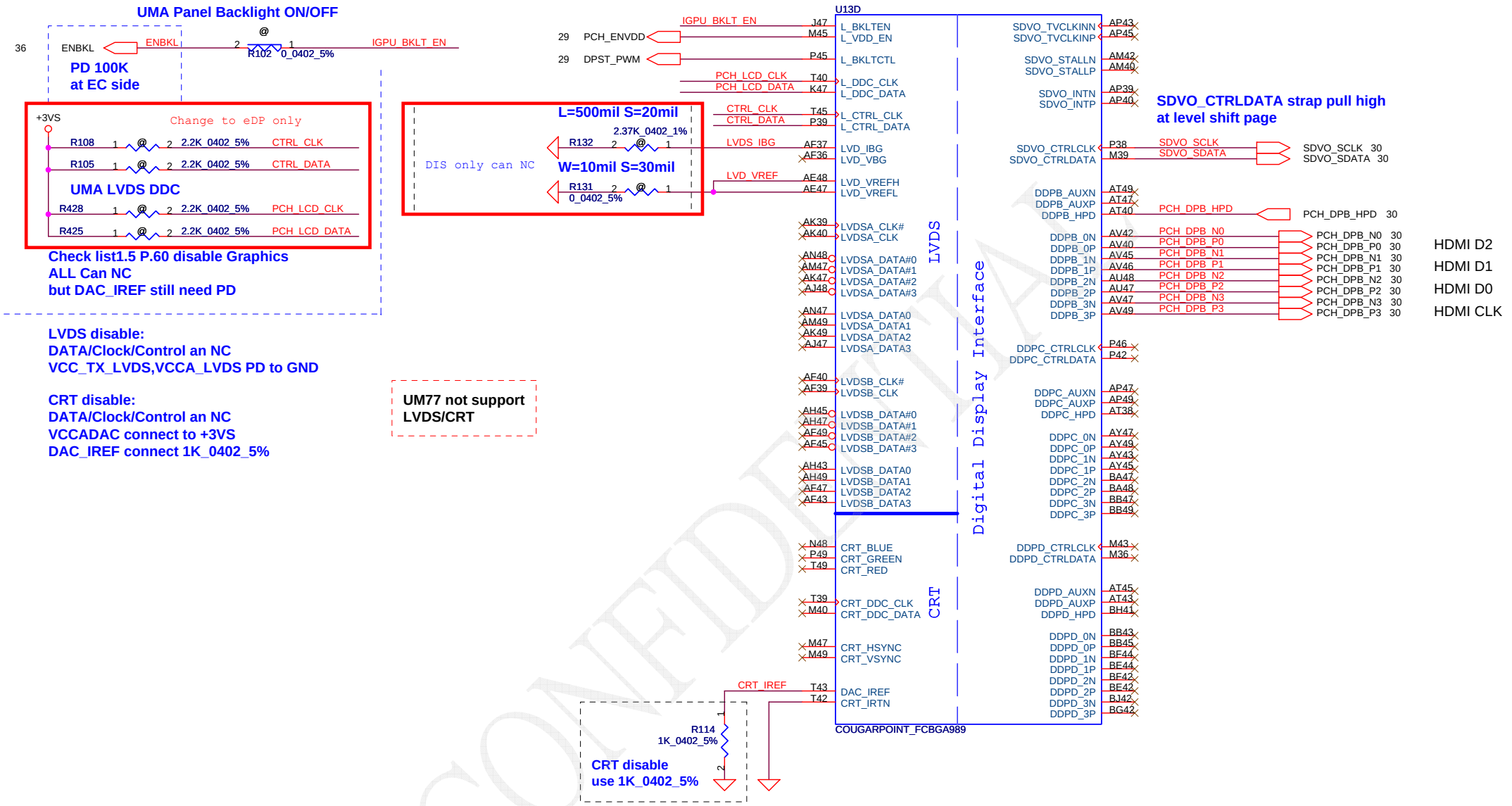

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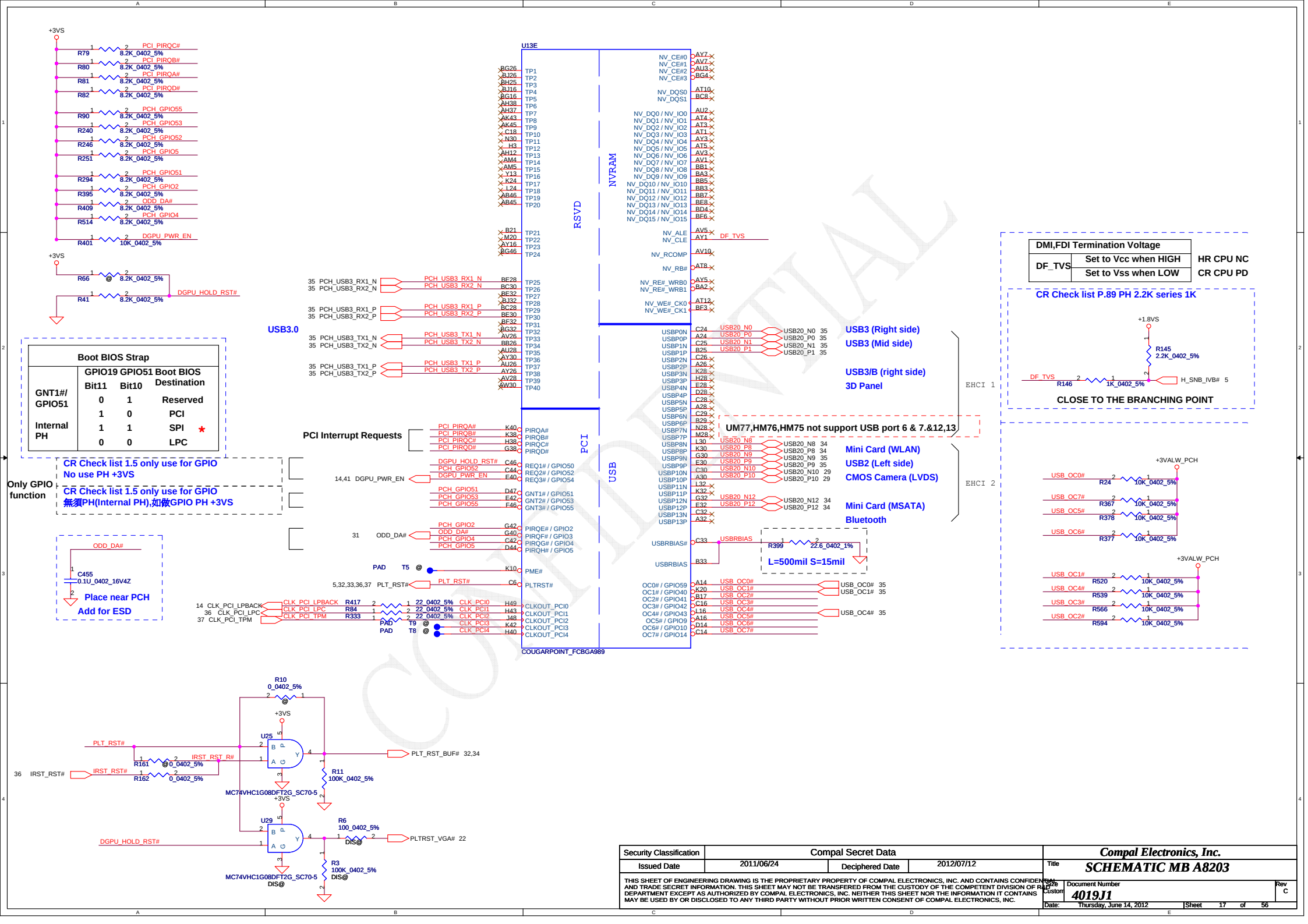

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HDA_SYNC PH(PLL =+1.5VS)

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die PLL voltage regulator enable
L : On-Die PLL Voltage Regulator disable

+3VALW_PCH
R411 4.7K_0402_5%
PCH_GPIO28
R413 1K_0402_5%
Debug Port DG 1.2 PH 4.7K +3VALW_PCH

Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal

R83 @ 10K_0402_5% PCH_GPIO27

+3VS
R439 200K_0402_5% ODD_DETECT#
+3VALW_PCH
R261 @ 1K_0402_5% EC_SMI#

SATA2GP/GPIO36 & SATA3GP/GPIO37
Sampled at Rising edge of PWROK.
Weak internal pull-down.
(weak internal pull-down is disabled after PLTRST# de-asserts)
NOTE: This signal should NOT be pulled high when strap is sampled

+3VS
R112 10K_0402_5% PCH_GPIO0
R402 10K_0402_5% PCH_GPIO1
R70 10K_0402_5% PCH_GPIO6
R115 10K_0402_5% MSATA_DET#
R71 10K_0402_5% DGPU_PWROK
R416 10K_0402_5% PCH_GPIO34
R128 10K_0402_5% PCH_GPIO48
R111 10K_0402_5% PCH_GPIO49
+3VALW_PCH
R376 10K_0402_5% PCH_GPIO12
R412 1K_0402_5% EC_LID_OUT#
R52 10K_0402_5% PCH_GPIO57

GPIO24 Unmultiplexed
NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.
CRB1.0 PH10K to +3VALW

Fan Tachometer Inputs
TACH1~7 only on server can insted to GPIO

12/19 modify

	GPIO71
GDDR5	1
GDDR3	0

+3VS
R68 10K_0402_5% PCH_GPIO71
R43 10K_0402_5% @
R67 10K_0402_5% @ PCH_GPIO69
R42 10K_0402_5%
R69 10K_0402_5% @ PCH_GPIO70
R44 10K_0402_5%

Project ID		GPIO69	GPIO70
* x	0	0	0
x	0	0	1
x	0	1	0
x	0	1	1
x	1	0	0
x	0	0	1
x	0	1	0
x	0	1	1
x	1	0	0
x	1	0	1
x	1	1	0
x	1	1	1

U13F

No use PH 10K +3VS			PCH_GPIO0	T7	BMBUSY# / GPIO0
No use PH 10K +3VS			PCH_GPIO1	A42	TACH1 / GPIO1
No use PH 10K +3VS			PCH_GPIO6	H36	TACH2 / GPIO6
No use PH 10K +3VS	36	EC_SCI#	EC_SCI#	E38	TACH3 / GPIO7
No use PH 10K +3VALW	36	EC_SMI#	EC_SMI#	C10	GPIO8
No use PH +3VALW			PCH_GPIO12	C4	LAN_PHY_PWR_CTRL / GPIO12
No use PH +3VALW	36	EC_LID_OUT#	EC_LID_OUT#	G2	GPIO15
No use PH +3VS	34	MSATA_DET#	MSATA_DET#	U2	SATA4GP / GPIO16
No use PH +3VS	50	VGA_PWROK R45 0_0402_5%	DGPU_PWROK	D40	TACH0 / GPIO17
No use PH 10K +3VS	RAM flag		PCH_GPIO22	T5	SCLOCK / GPIO22
No use PH +3VALW	DDR3/DDR3L		PCH_GPIO24	E8	GPIO24 / MEM_LED
No use PD 10K to GND			PCH_GPIO27	E16	GPIO27
No use PH 10K +3VALW			PCH_GPIO28	P8	GPIO28
No use PH 10K +3VS	BT ON/OFF		PCH_GPIO34	K1	STP_PCI# / GPIO34
No use can NC		PAD T12 @	PCH_GPIO35	K4	GPIO35
Can't PH		31 ODD_DETECT#	ODD_DETECT#	V8	SATA2GP / GPIO36
Can't PH		PAD T10 @	PCH_GPIO37	M5	SATA3GP / GPIO37
No use PH 10K +3VS	Optimus(L)/ non optimus(H)		OPTIMUS_EN#	N2	SLOAD / GPIO38
No use PH 10K +3VS	RAM flag		PCH_GPIO39	M3	SDATAOUT0 / GPIO39
No use PH 10K +3VS			PCH_GPIO48	V13	SDATAOUT1 / GPIO48
SATA5GP&TEMP_ALERT# CRB PH 10K +3VS			PCH_GPIO49	V3	SATA5GP / GPIO49
No use PH +3VALW			PCH_GPIO57	D6	GPIO57

GPIO

TACH4 / GPIO68	C40	ODD_EN#	ODD_EN# 31
TACH5 / GPIO69	B41	PCH_GPIO69	
TACH6 / GPIO70	C41	PCH_GPIO70	
TACH7 / GPIO71	A40	PCH_GPIO71	

CPU/MISC

A20GATE	P4		GATEA20 36
PECI	AU16	PCH_PECI_R 0_0402_5% R158	H_PECI 5,36
RCIN#	P5	EC_KBRST#	EC_KBRST# 36
PROCPWRGD	AY11		H_CPUPWRGD 5
THRMTRIP#	AY10	PCH_THRMTRIP#_R R159 390_0402_5%	H_THRMTRIP#
INIT3_3V#	T14		

+3VS
R106 10K_0402_5%

PECI CPU-EC
CTRL+ALT+DEL
non CPU power ok
130c shut down

INIT3_3V Checklist1.5 P.69
This signal has weak internal PU, can't pull low,leave NC

NC_1	AH8	
NC_2	AK11	
NC_3	AH10	
NC_4	AK10	
NC_5	P37	

TS_VSS1~4
PD to GND

+3VS
EC_KBRST# R103 10K_0402_5%
ODD_EN# R400 10K_0402_5%

NCTF

VSS_NCTF_1	A4	VSS_NCTF_15	BG2
VSS_NCTF_2	A44	VSS_NCTF_16	BG48
VSS_NCTF_3	A45	VSS_NCTF_17	BH3
VSS_NCTF_4	A46	VSS_NCTF_18	BH47
VSS_NCTF_5	A5	VSS_NCTF_19	BJ4
VSS_NCTF_6	A6	VSS_NCTF_20	BJ44
VSS_NCTF_7	B3	VSS_NCTF_21	BJ45
VSS_NCTF_8	B47	VSS_NCTF_22	BJ46
VSS_NCTF_9	BD1	VSS_NCTF_23	BJ5
VSS_NCTF_10	BD49	VSS_NCTF_24	BJ6
VSS_NCTF_11	BE1	VSS_NCTF_25	C2
VSS_NCTF_12	BE49	VSS_NCTF_26	C48
VSS_NCTF_13	BF1	VSS_NCTF_27	D1
VSS_NCTF_14	BF49	VSS_NCTF_28	D49
		VSS_NCTF_29	E1
		VSS_NCTF_30	E49
		VSS_NCTF_31	F1
		VSS_NCTF_32	F49

COUGARPOINT_FCBGA989

9/15 Layout request remove Test point They will route by itself

9/15 Layout request remove Test point They will route by itself

+3VS
R427 UMAO@ 10K_0402_5% OPTIMUS_EN#
R426 DIS@ 10K_0402_5%

	GPIO38 OPTIMUS_EN#
* Muxless	0
nonMuxless	1

+3VALW_PCH
R92 10K_0402_5% PCH_GPIO24
R94 @ 10K_0402_5%

	GPIO24 PCH_GPIO24
DDR3L	0
* DDR3	1

on board ram flag

	GPIO39	GPIO23	GPIO22
EVT MICRON 4G	0	0	0
EVT ELPIDA 4G	0	0	1
DVT HYNIX 2G	0	1	0
DVT ELPIDA 2G	0	1	1

+3VS
R419 10K_0402_5% @
PCH_GPIO39
R418 10K_0402_5% RAM@
+3VS
R398 10K_0402_5% RAM@
PCH_GPIO23
R397 1K_0402_5% @
PCH_GPIO23 13
+3VS
R97 10K_0402_5% ELPIDA@
PCH_GPIO22
R98 10K_0402_5% HYNIX@

GPIO36/GPIO37 is Strap functionality
that requires internal pull down to be sampled at rising PWROK.
When uses as SATA2GP/SATA3GP for mechanical presence detect
use a external pull up 150K-200K ohm to Vcc3_3
When used as GP input
ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA*GP
use 8.2K-10K pull-down
check list page 47

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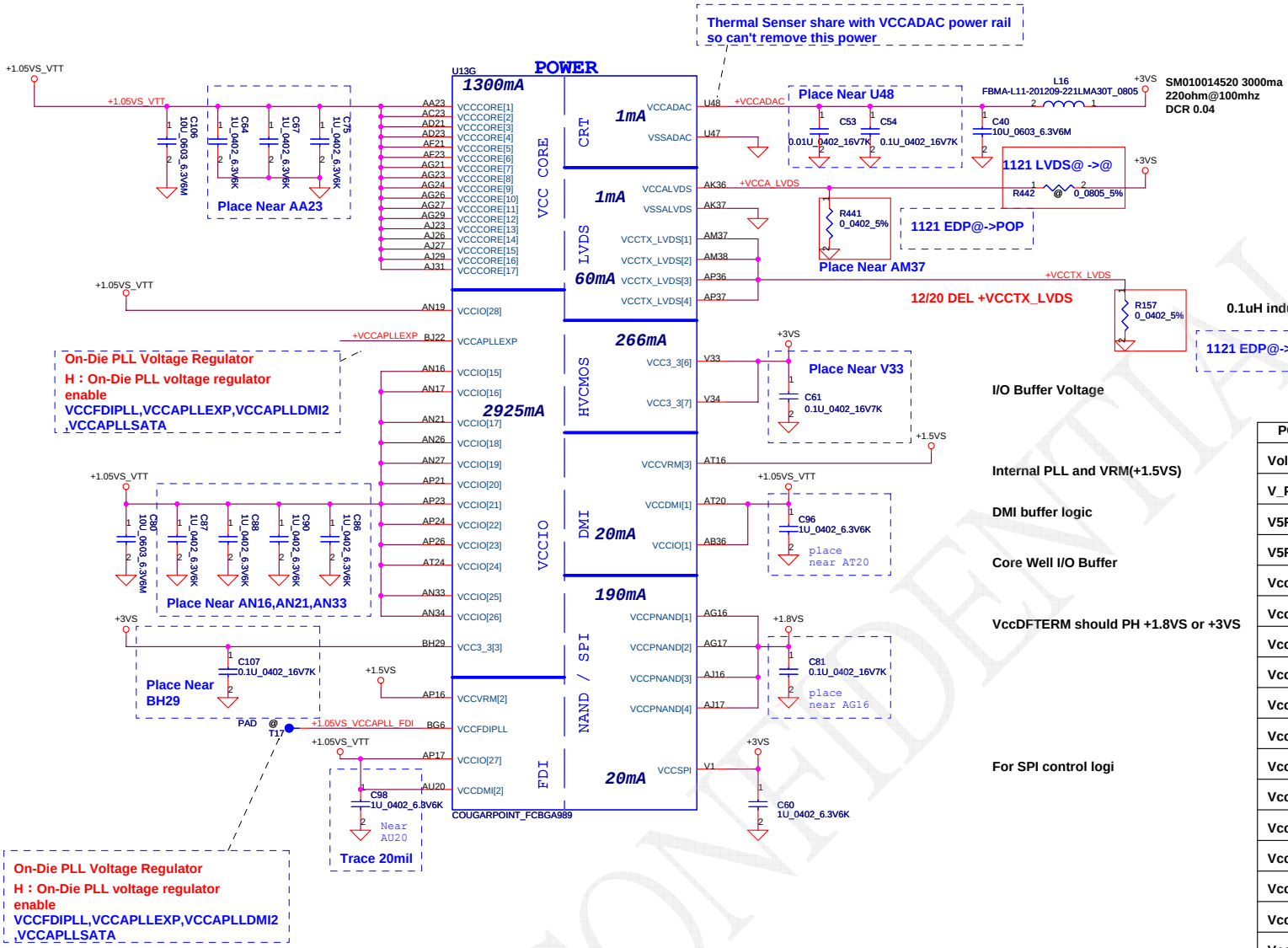

PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

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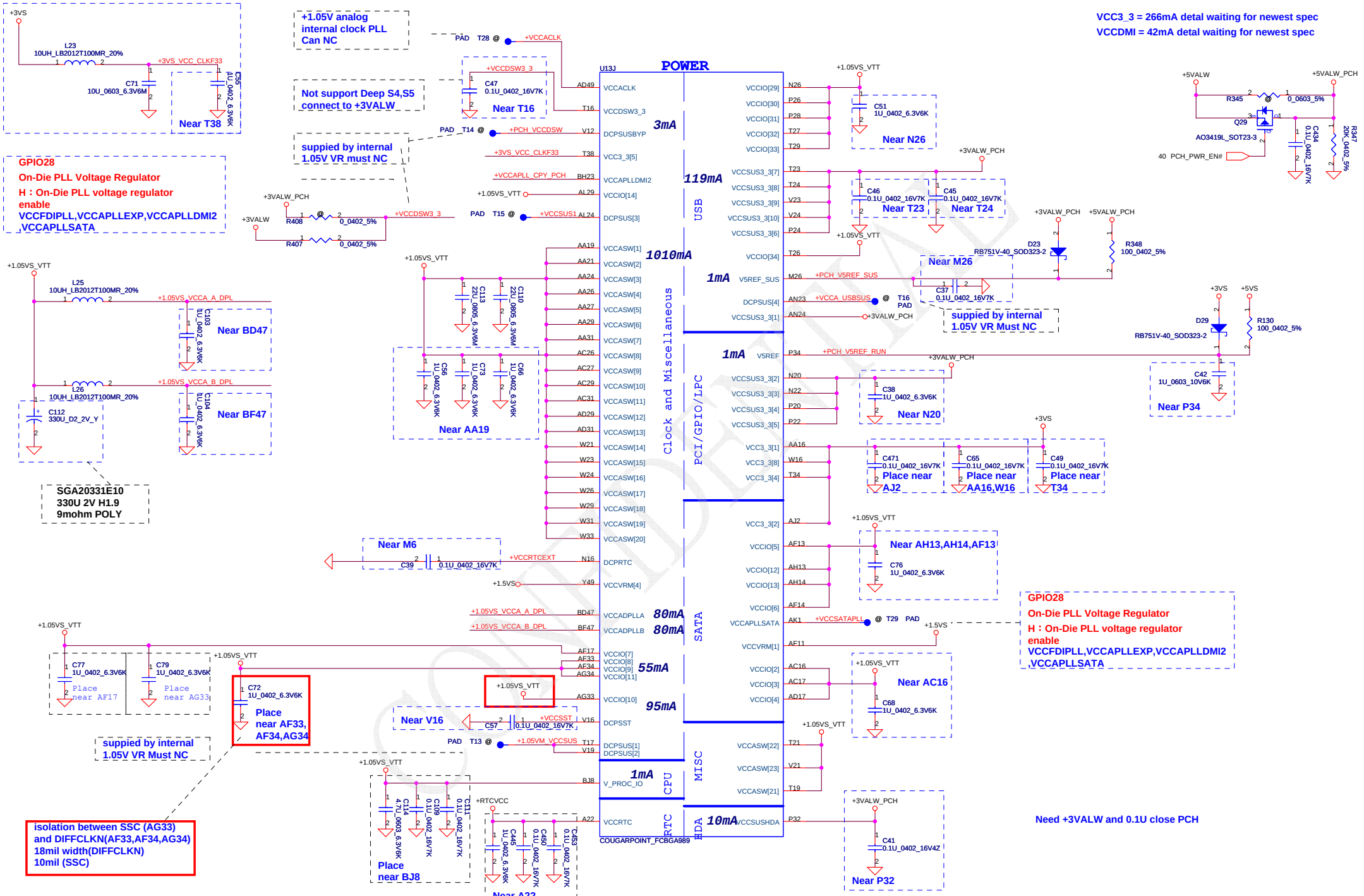
VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec
POWER
U13J
+1.05V analog internal clock PLL Can NC
Not support Deep S4,S5 connect to +3VALW
suppied by internal 1.05V VR must NC
GPIO28
On-Die PLL Voltage Regulator
H : On-Die PLL voltage regulator enable
VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2 ,VCCAPLLSATA
SGA20331E10
330U 2V H1.9
9mohm POLY
isolation between SSC (AG33) and DIFFCLKN(AF33,AF34,AG34)
18mil width(DIFFCLKN)
10mil (SSC)
Need +3VALW and 0.1U close PCH
3mA
119mA
1010mA
1mA
80mA
55mA
95mA
10mA
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
CPU
MISC
RTC
HDA
COUGARPOINT_FCBGA989
Near T38
Near T16
Near T23
Near T24
Near N26
Near M26
Near BD47
Near BF47
Near AA19
Near N20
Near P34
Near AH13,AH14,AF13
Near AC16
Near M6
Near V16
Near A22
Near P32
Place near AJ2
Place near AA16,W16
Place near T34
Place near AF17
Place near AG33
Place near AF33, AF34,AG34
Place near BJ8
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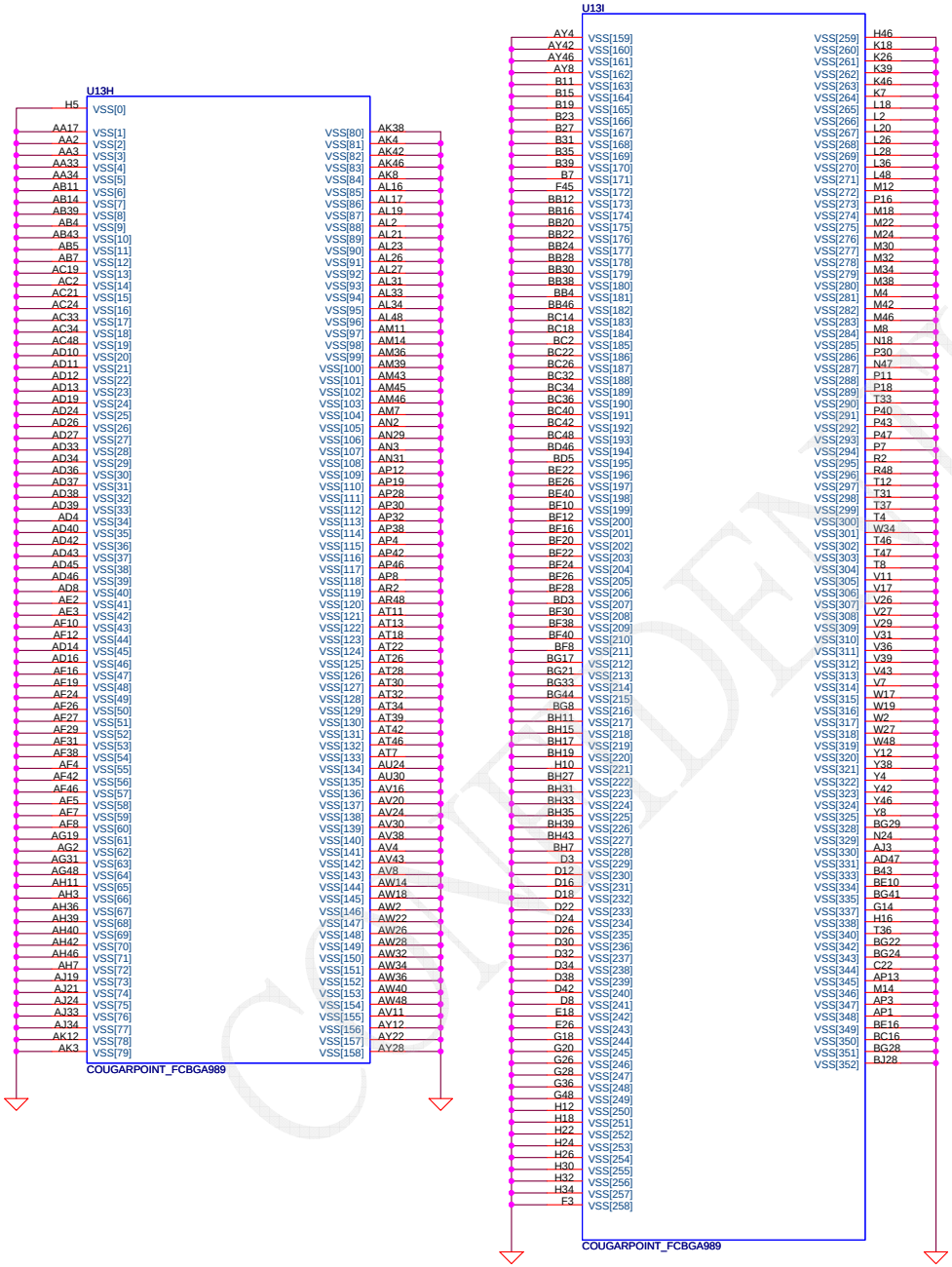

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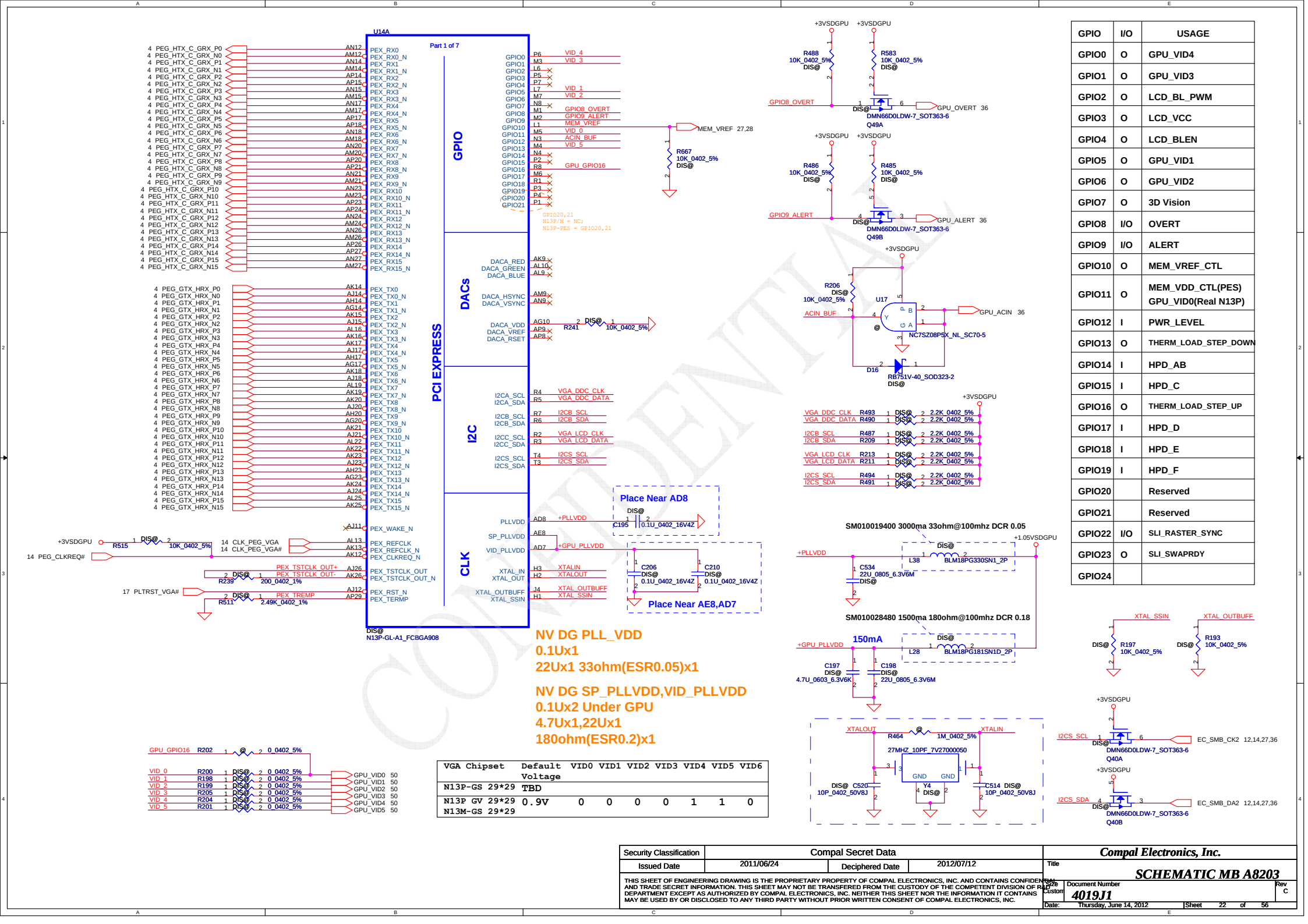

GPIO	I/O	USAGE
GPIO0	O	GPU_VID4
GPIO1	O	GPU_VID3
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	GPU_VID1
GPIO6	O	GPU_VID2
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	MEM_VDD_CTL(PES) GPU_VID0(Real N13P)
GPIO12	I	PWR_LEVEL
GPIO13	O	THERM_LOAD_STEP_DOWN
GPIO14	I	HPD_AB
GPIO15	I	HPD_C
GPIO16	O	THERM_LOAD_STEP_UP
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F
GPIO20		Reserved
GPIO21		Reserved
GPIO22	I/O	SLI_RASTER_SYNC
GPIO23	O	SLI_SWAPRDY
GPIO24		

VGA Chipset	Default Voltage	VID0	VID1	VID2	VID3	VID4	VID5	VID6
N13P-GS 29*29	TBD							
N13P GV 29*29 N13M-GS 29*29	0.9V	0	0	0	0	1	1	0

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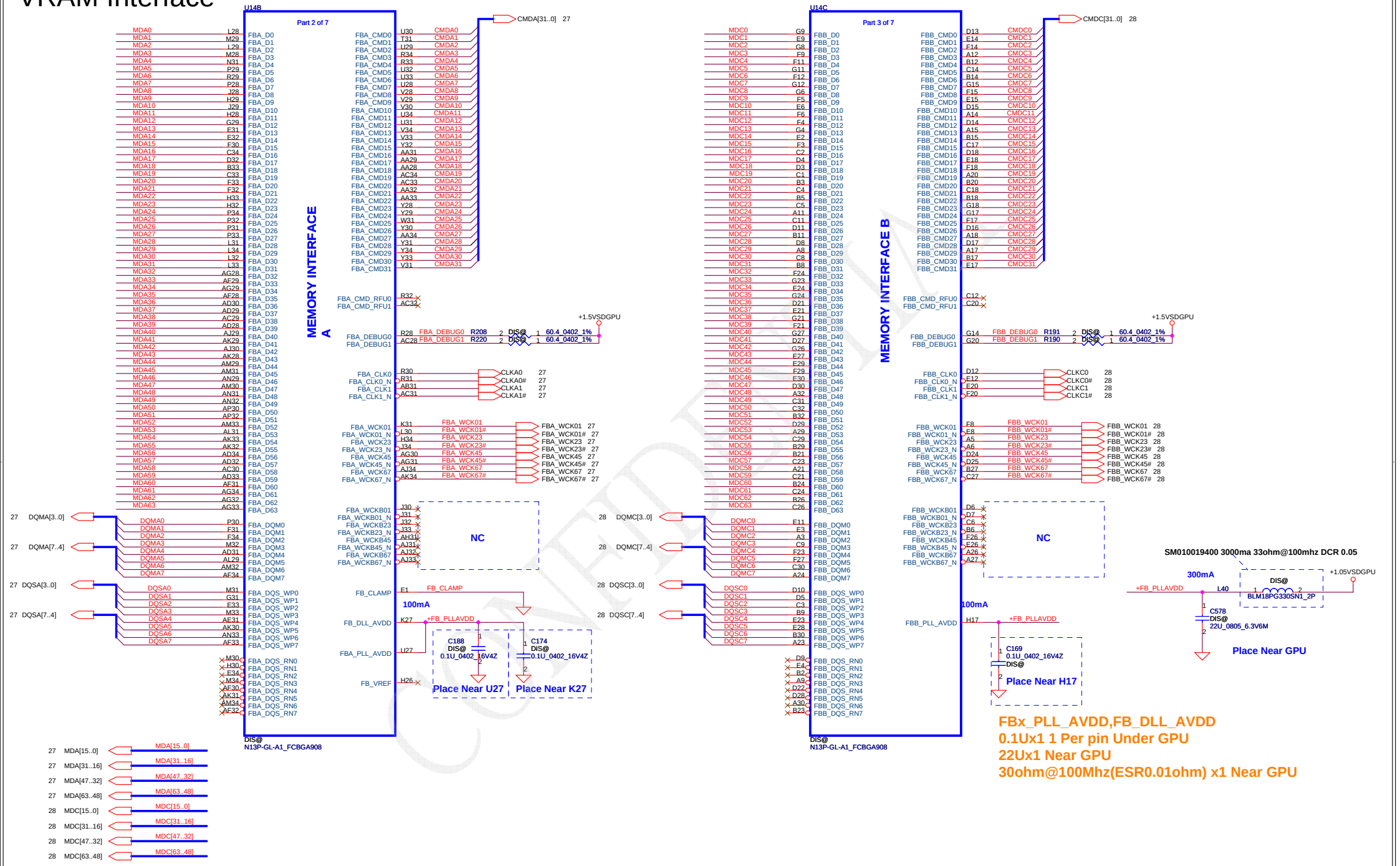
VRAM Interface



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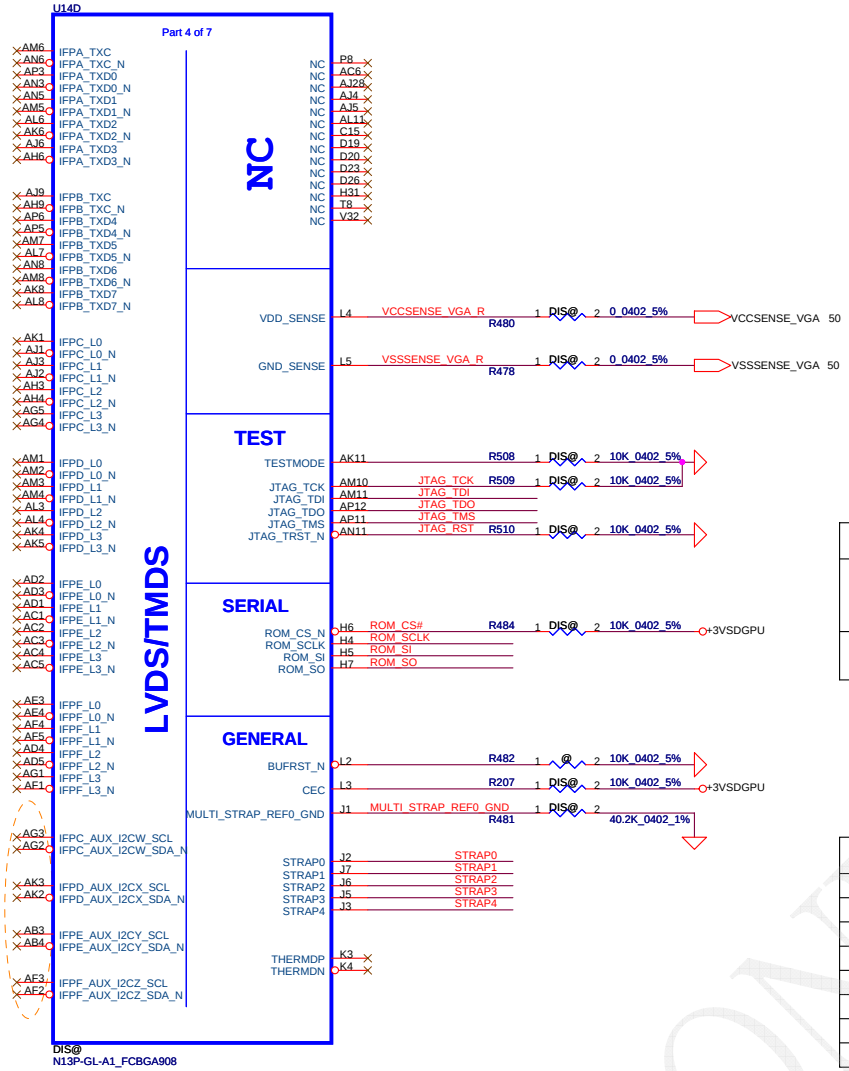

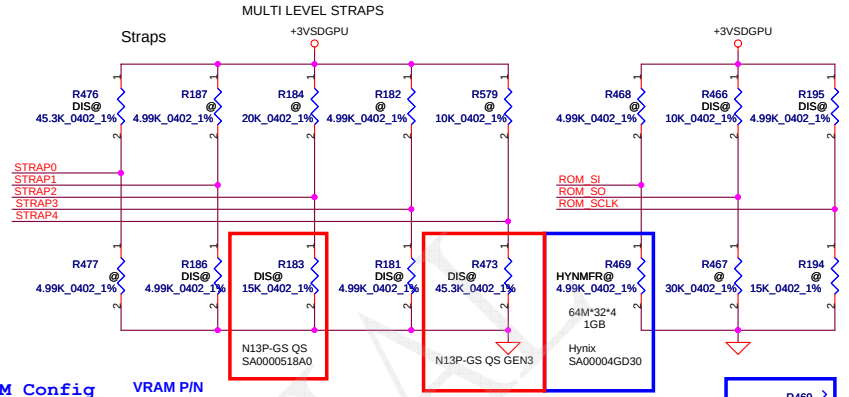

VRAM BOM Config — **VRAM P/N**

X76364BOL03: 64Mx32x4 HYN 64*32 2000M SA00004GD30 (S IC D5 64M32/2.5G H5GQ2H24MFR-T2C ABO!)

X76364BOL04: 64Mx32x4 HYN 64*32 2000M SA00004GD50(S IC D5 64M32/2.5G H5GQ2H24AFR-T2C ABO!)

R469 HYNAFR@ 24.9K_0402_1%
64M*32*4 1GB
Hynix SA00004GD50

GDDR5	Vendor	Strap	ROM_SI
64M x 32	Hynix(M)	Ox0	PD 5K
	Samsung	Ox1	PD 10K
	Hynix(A)	Ox4	PD 25K
32M x 32	Hynix	Ox2	PD 15K
	Samsung	Ox3	PD 20K

For N13P-GS-A1(ES2) A2(QS) strap table Decive ID : 0x0FD2

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GS	2000 MHZ	64M* 32* 4 1GB	Hynix SA00004GD30						R PD 5K		
N13P-GS	2000 MHZ	64M* 32* 4 1GB	Samsung	R PU 45K	R PD 5K	R PD 15K	R PD 5K	R PD 45K	R PD 10K	R PU 5K	R PU 5K
N13P-GS	2000 MHZ	64M* 32* 4 1GB	Hynix SA00004GD50						R PD 25K		

Resistor Values	Pull-up to +3V	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

STRAP0	USER[3:0]
STRAP1	3GIO_PADCFG_LUT_ADR[3:0]
STRAP2	PCI_DEVID[3:0]
STRAP3	SOR[3:0]
STRAP4	PEX_MAX_SPEED, DP_PLLVDD33V
ROM_SCLK	PCI_DEV[4:5], SUB_VENDOR,PEX_PLL_EN_TERM
ROM_SI	RAM_CFG[3:0]
ROM_SO	FB_BAR_SIZE[1:0],SMB_ ALT_ADOOR, VGA_DEVICE

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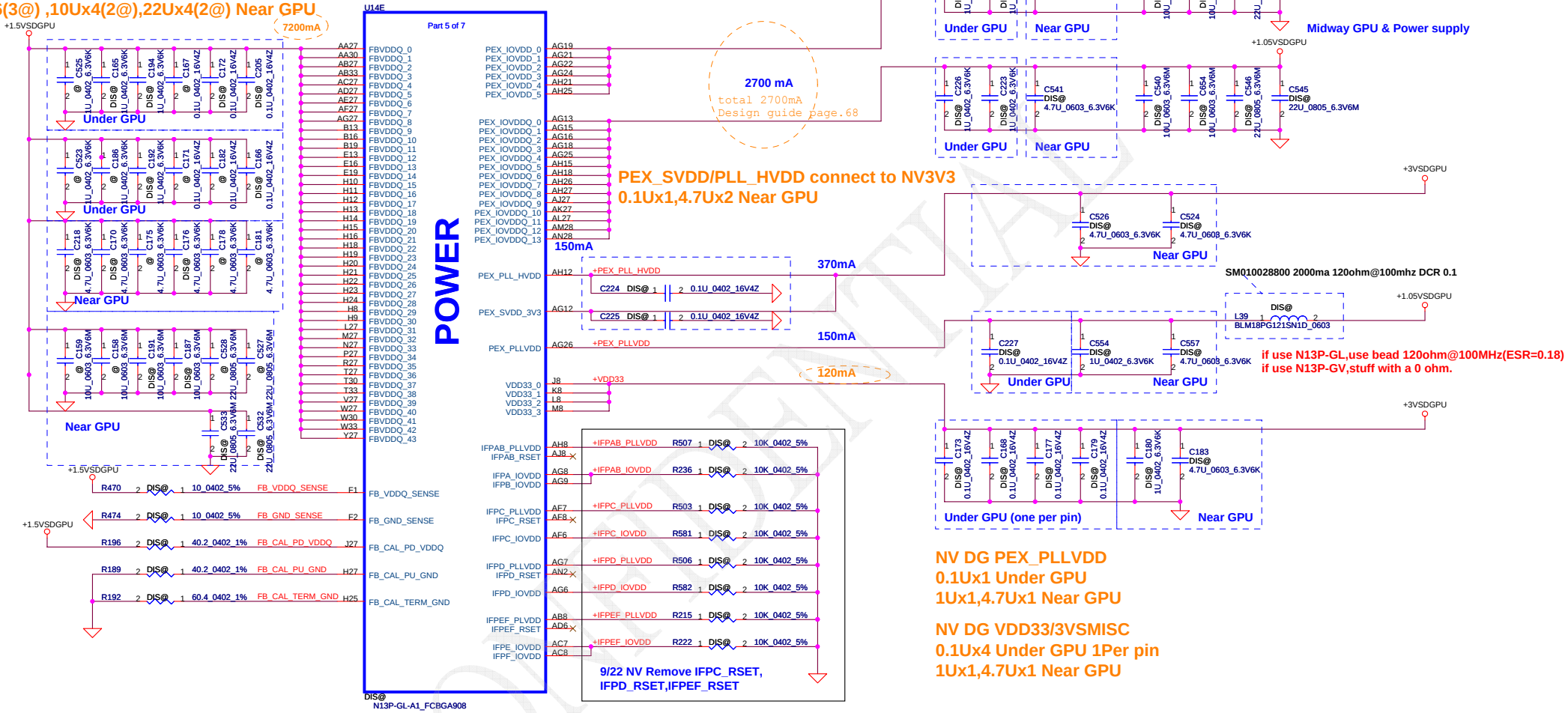
NV DG FBVDDQ(DDR3)
0.1Ux8,1Ux2,4.7Ux2 Under GPU
10Ux4 Near GPU
NV DG FBVDDQ(GDDR5)
0.1Ux6(3@),1Ux6(3@),Under GPU
4.7Ux6(3@) ,10Ux4(2@),22Ux4(2@) Near GPU

NV DG PEX_IOVVD/Q combined
1Ux4 Under GPU
4.7Ux2 Near GPU
10Ux4,22Ux4 Midway GPU & Power supply



NV DG PEX_PLLVDD
0.1Ux1 Under GPU
1Ux1,4.7Ux1 Near GPU

NV DG VDD33/3VSMISC
0.1Ux4 Under GPU 1Per pin
1Ux1,4.7Ux1 Near GPU

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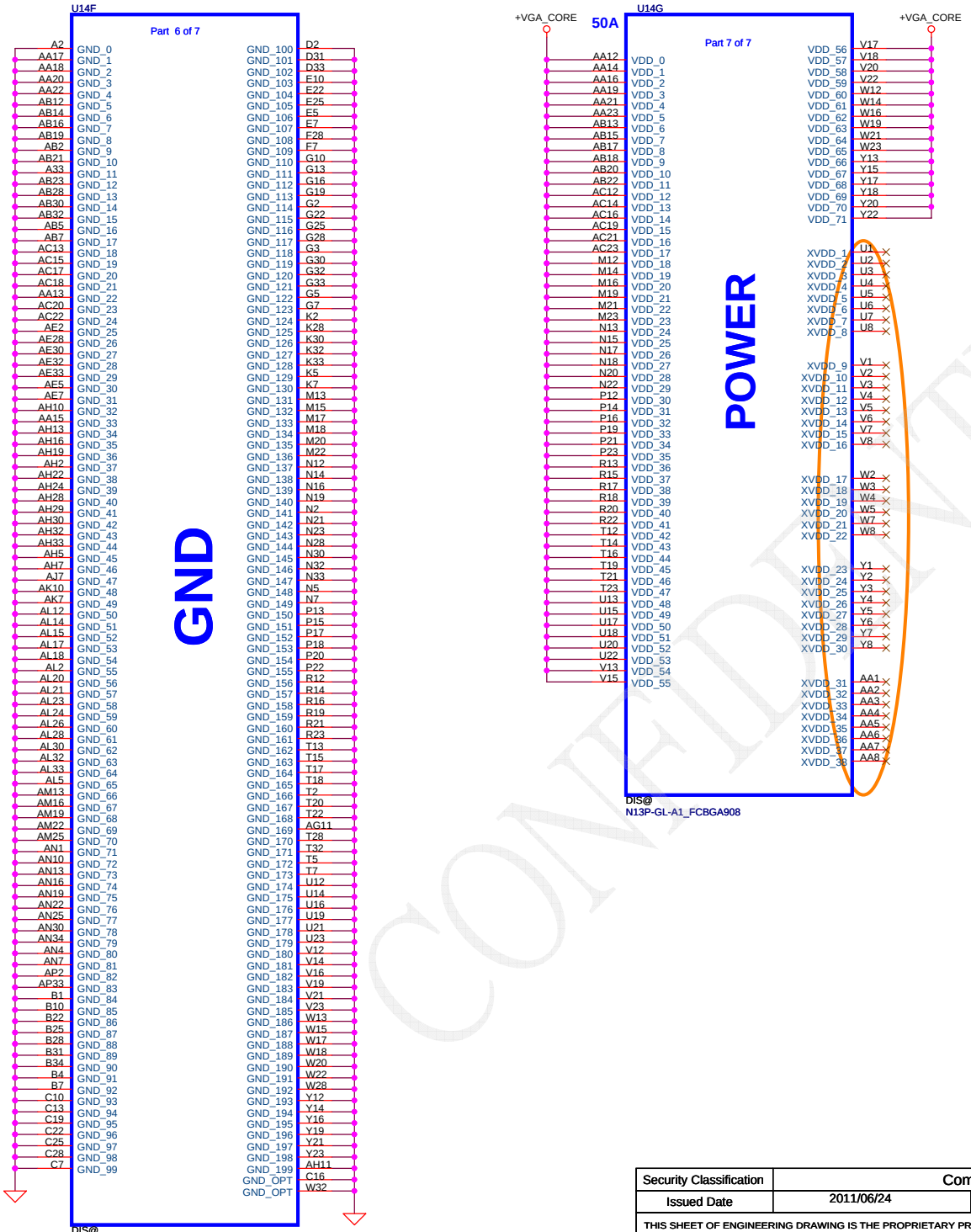

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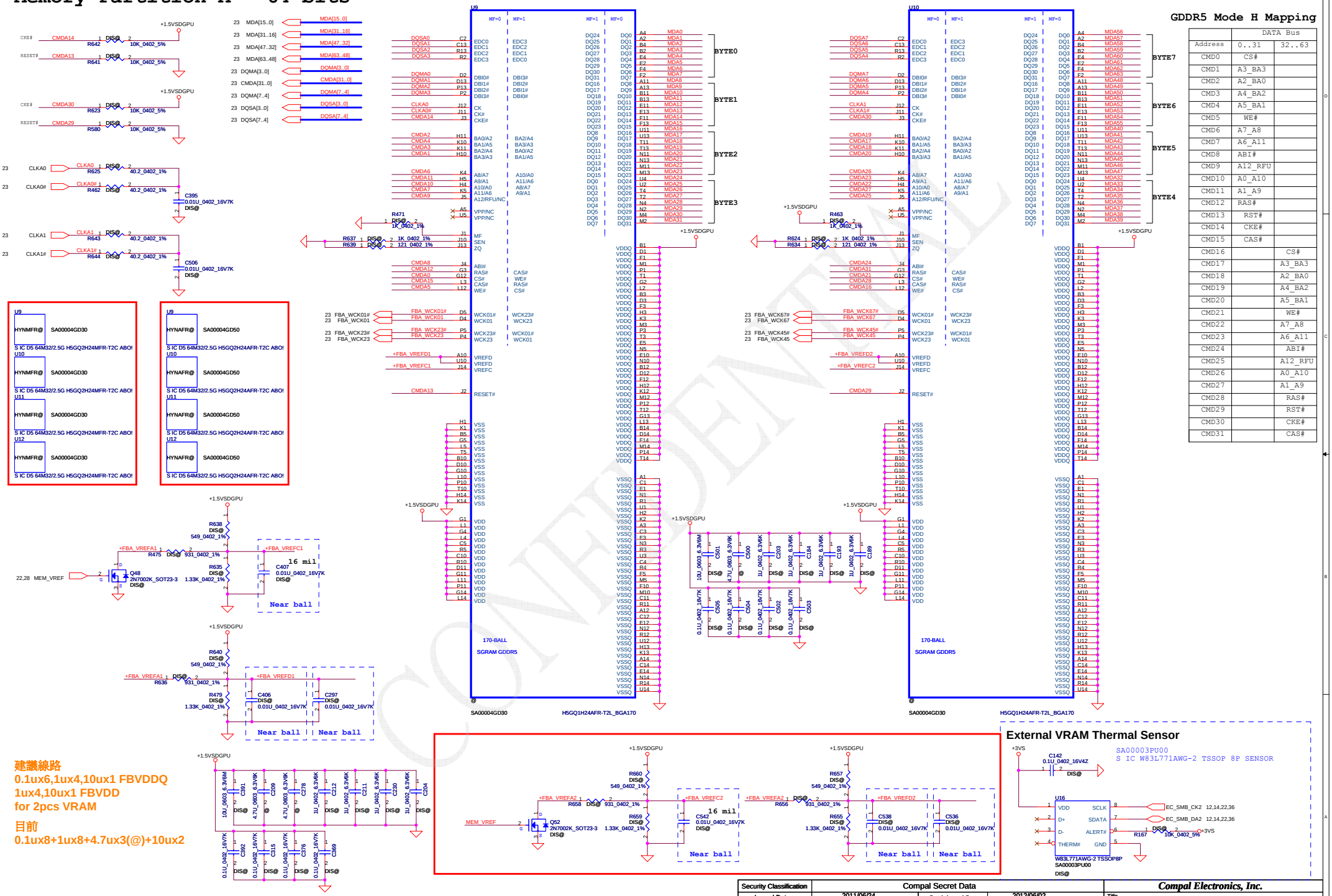
Memory Partition A - 64 bits



GDDR5 Mode H Mapping

Address	DATA Bus 0..31	DATA Bus 32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

建議線路
0.1ux6,1ux4,10ux1 FBVDDQ
1ux4,10ux1 FBVDD
for 2pcs VRAM

目前
0.1ux8+1ux8+4.7ux3(@)+10ux2

VRAM BOM Config

X76364BOL01: 1G HYN 128*16 2.5G SA00004GD30 (S IC D5 64M32/2.5G H5GQ2H24MFR-T2C ABO!)

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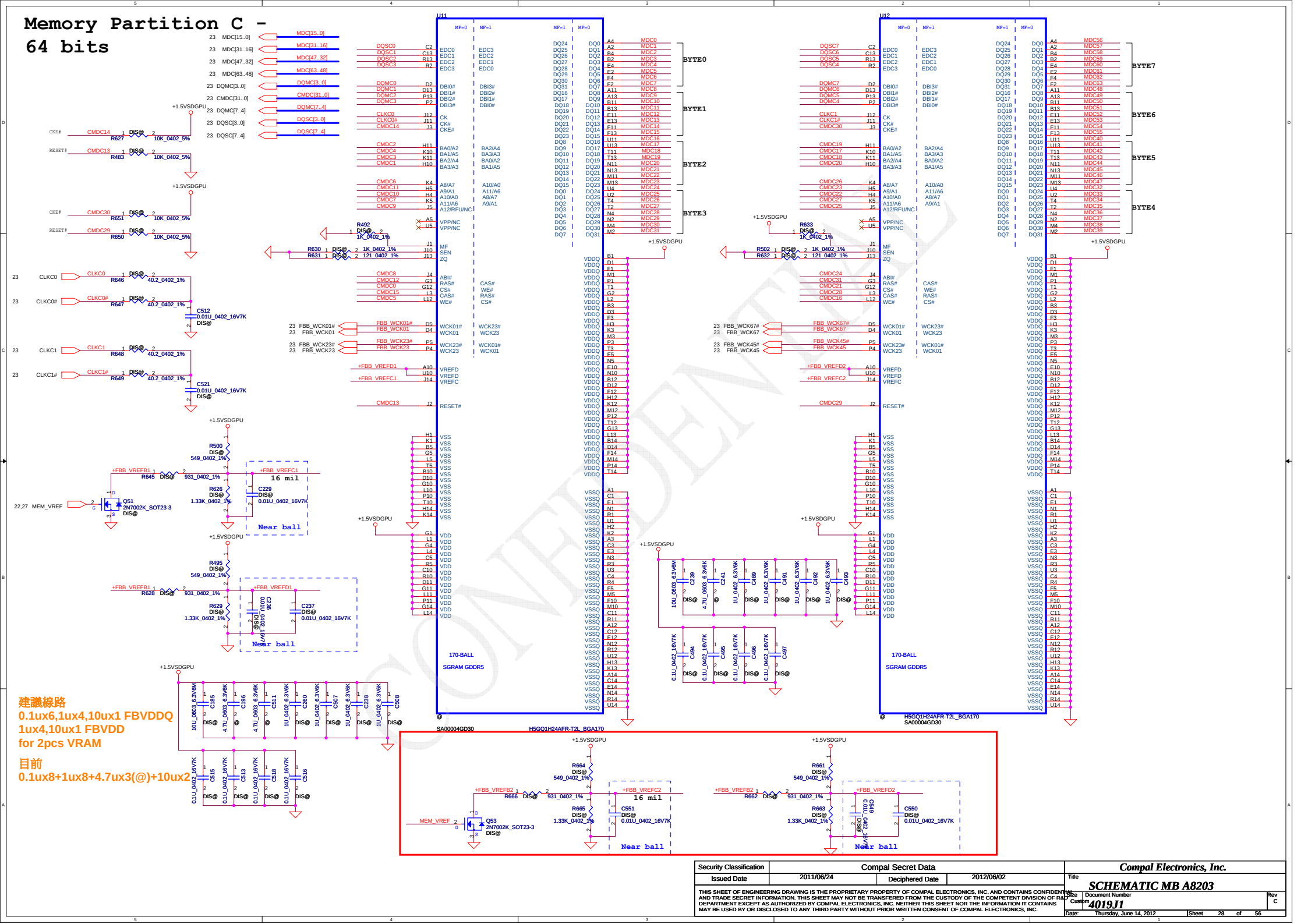
Memory Partition C - 64 bits



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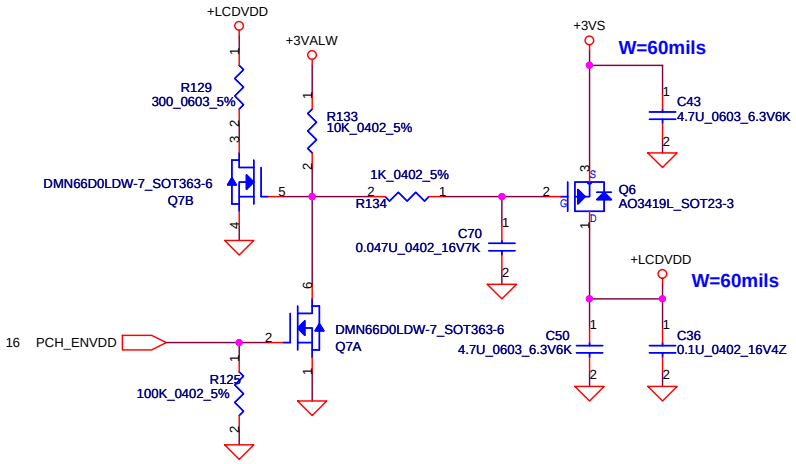
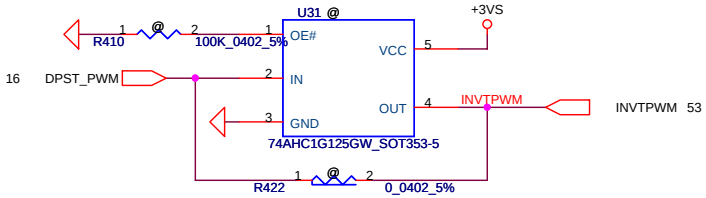
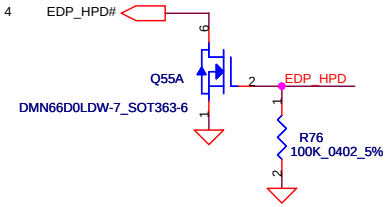
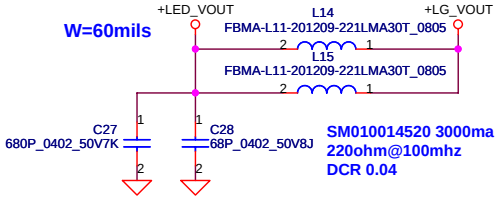
LCD POWER CIRCUIT

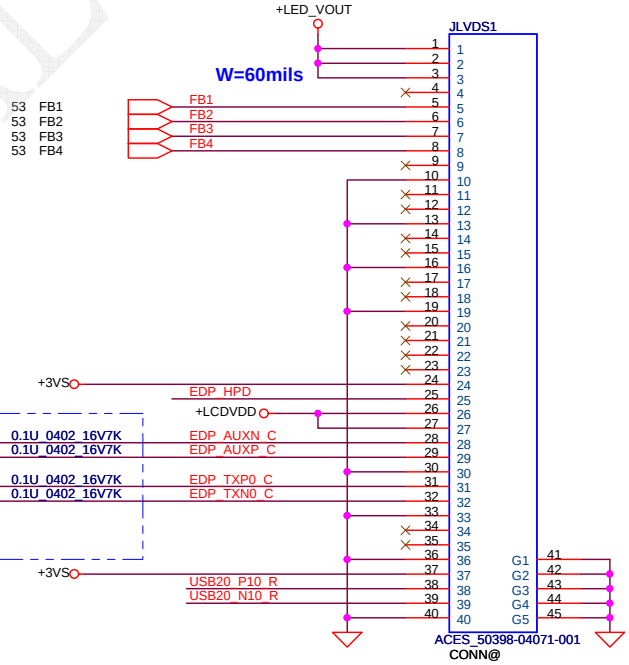


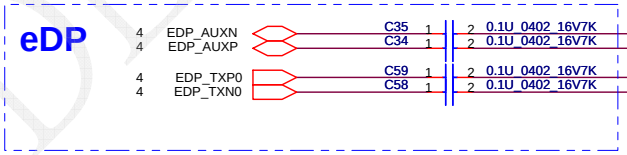


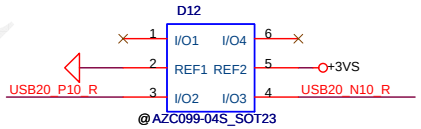


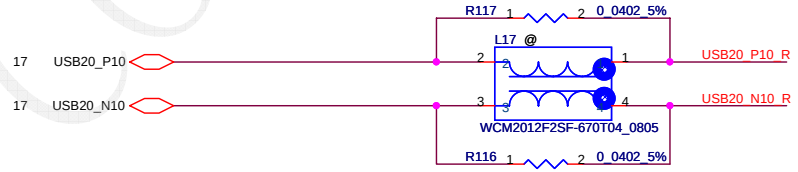


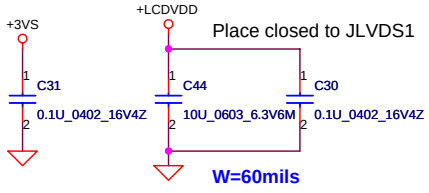
LCD/LED PANEL Conn.











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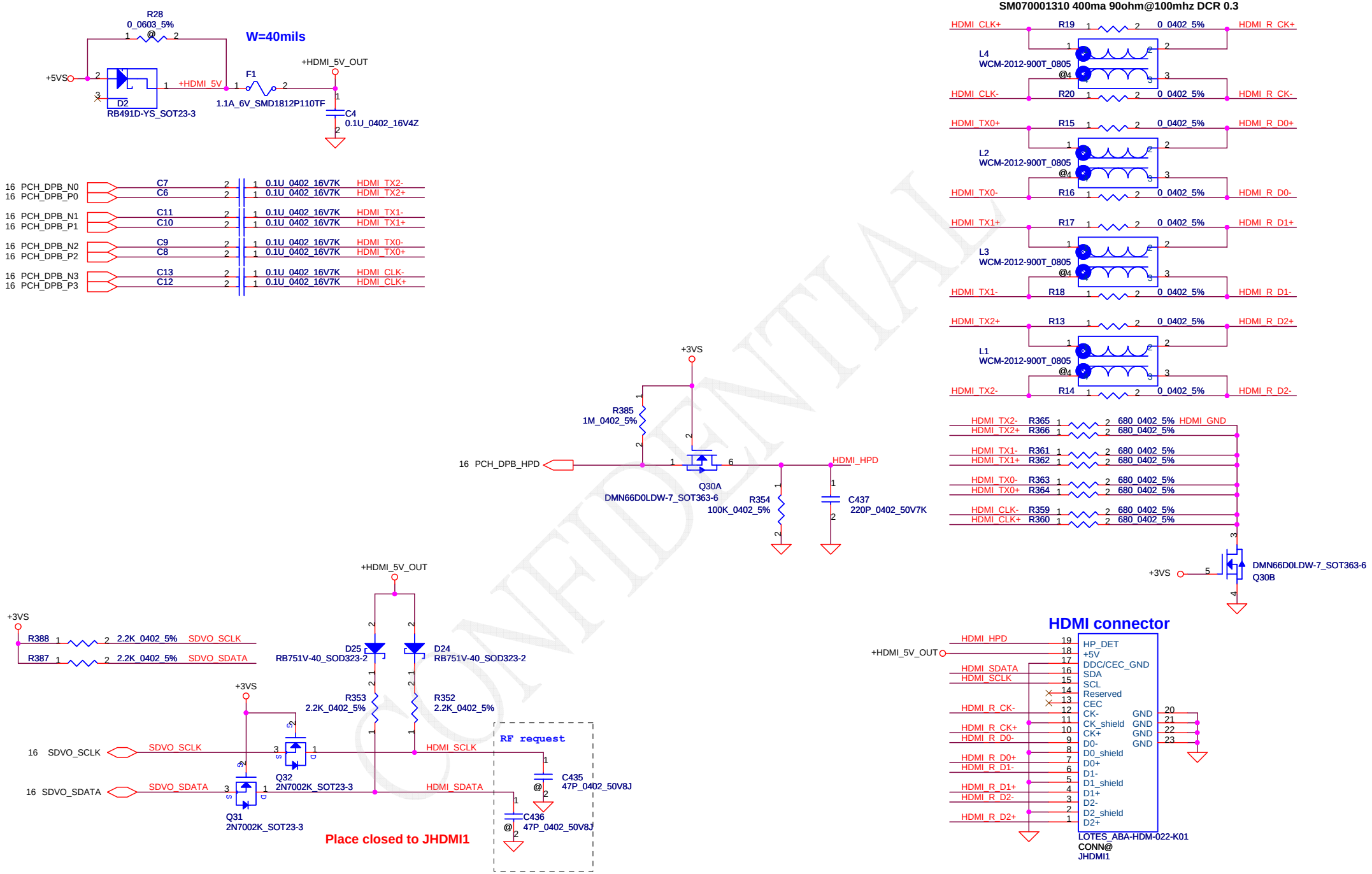

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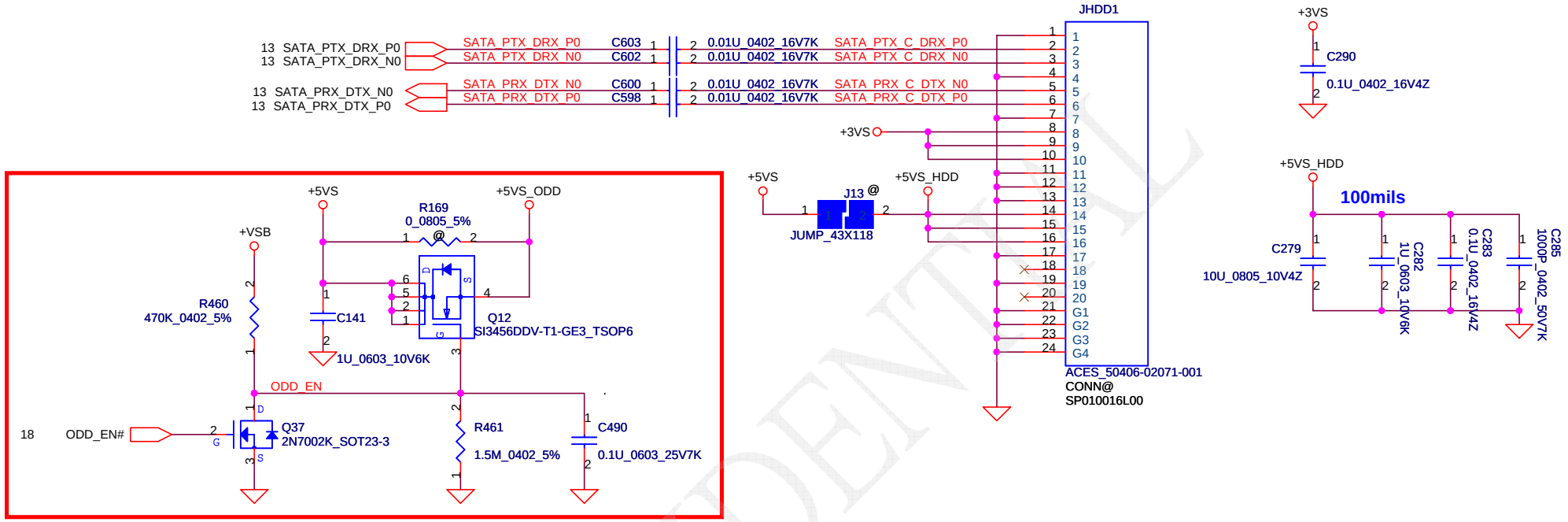
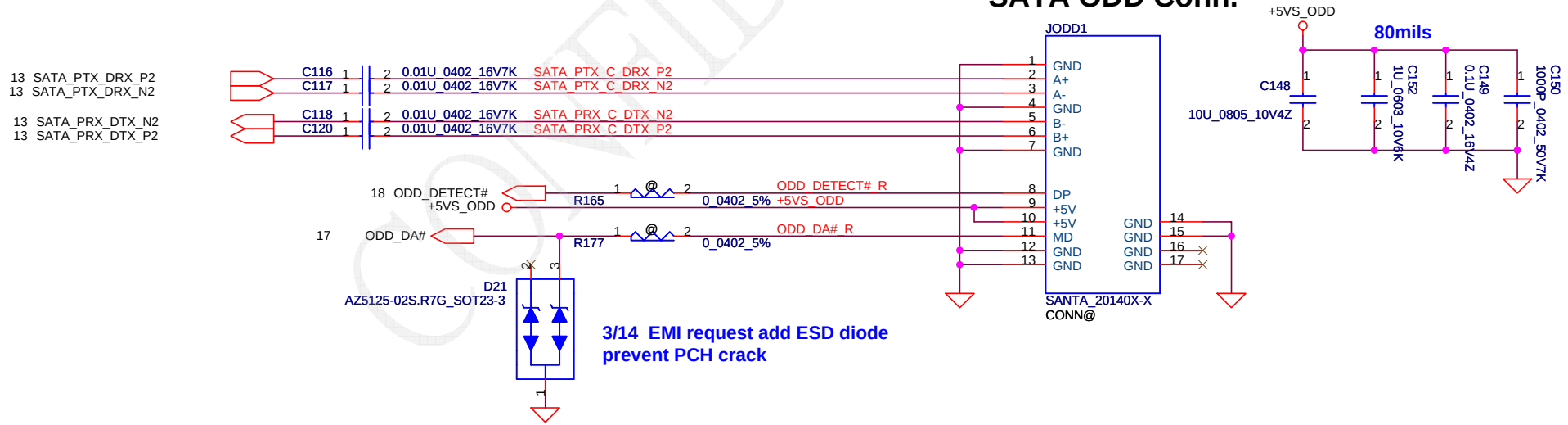
SATA HDD1 Conn.



SATA ODD Conn.



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091211 EMI add 1000P

U62

BCM57780A0KMLG_QFN48_7X7

0215 Reserve

SM010005500 500ma 600ohm@100mhz DCR 0.38

SM010005500 500ma 600ohm@100mhz DCR 0.38

LAN Connector

20120410
follow ESD cost down
remove

Place close to TCT pin

BOTHHAND: S X'FORM_ GST5009-D LF LAN, SP050006B00 40mil
TIMAG:S X'FORM_ IH-160 LAN , SP050006F00

	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

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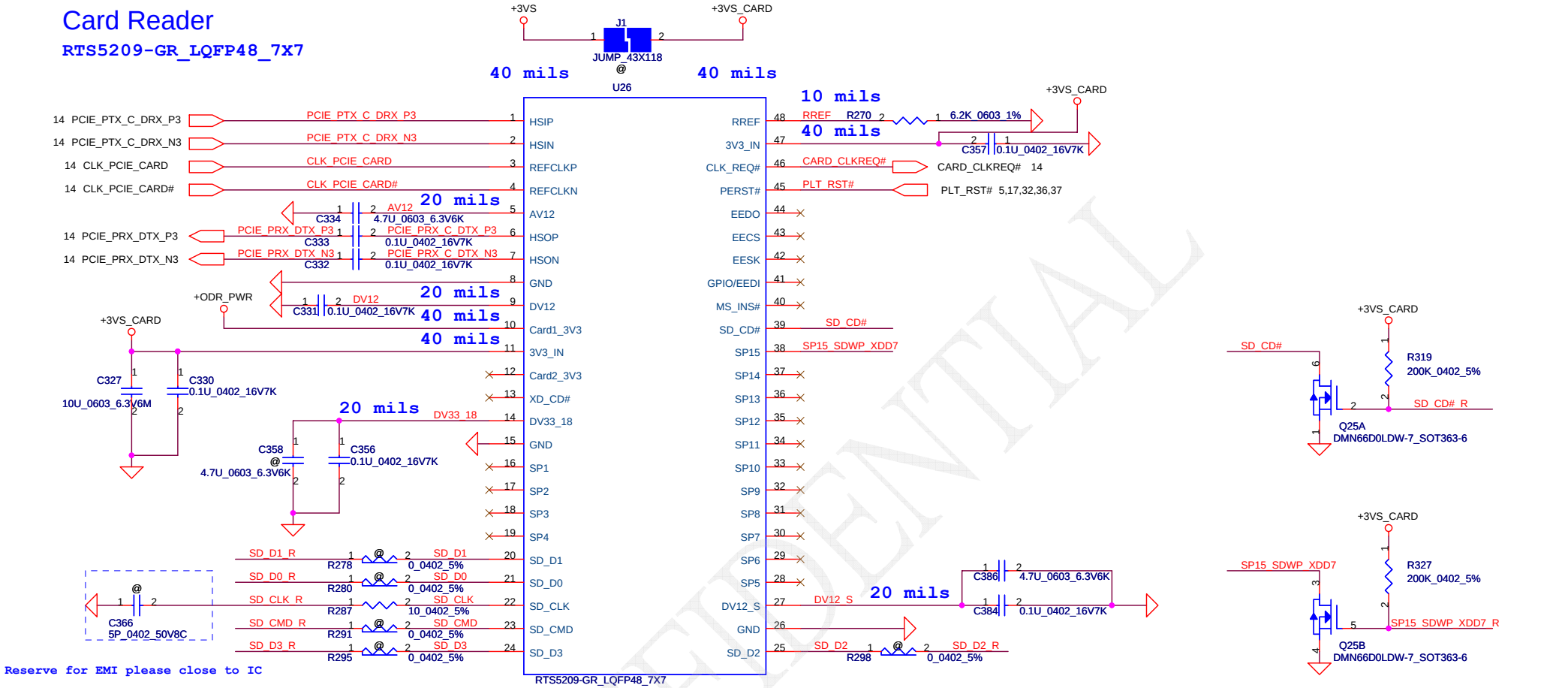
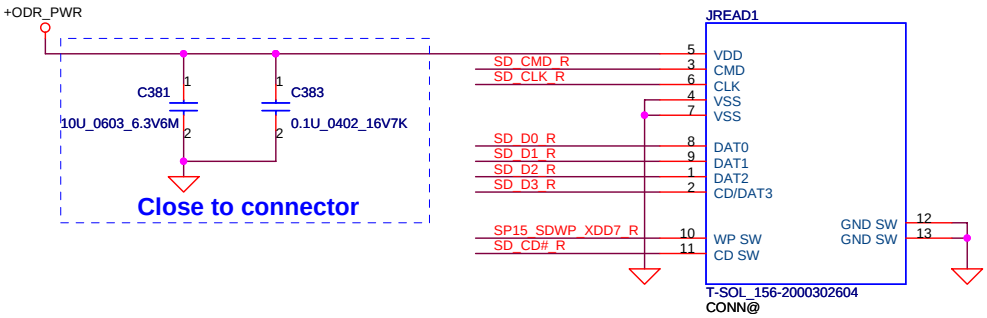
Card Reader

RTS5209-GR_LQFP48_7X7



Pin No.	Name
1	DAT2
2	DAT3
3	CMD
4	VSS
5	VDD
6	CLK
7	VSS
8	DAT0
9	DAT1
10	WP Pin (Normal close)
11	CD Pin (Normal close)



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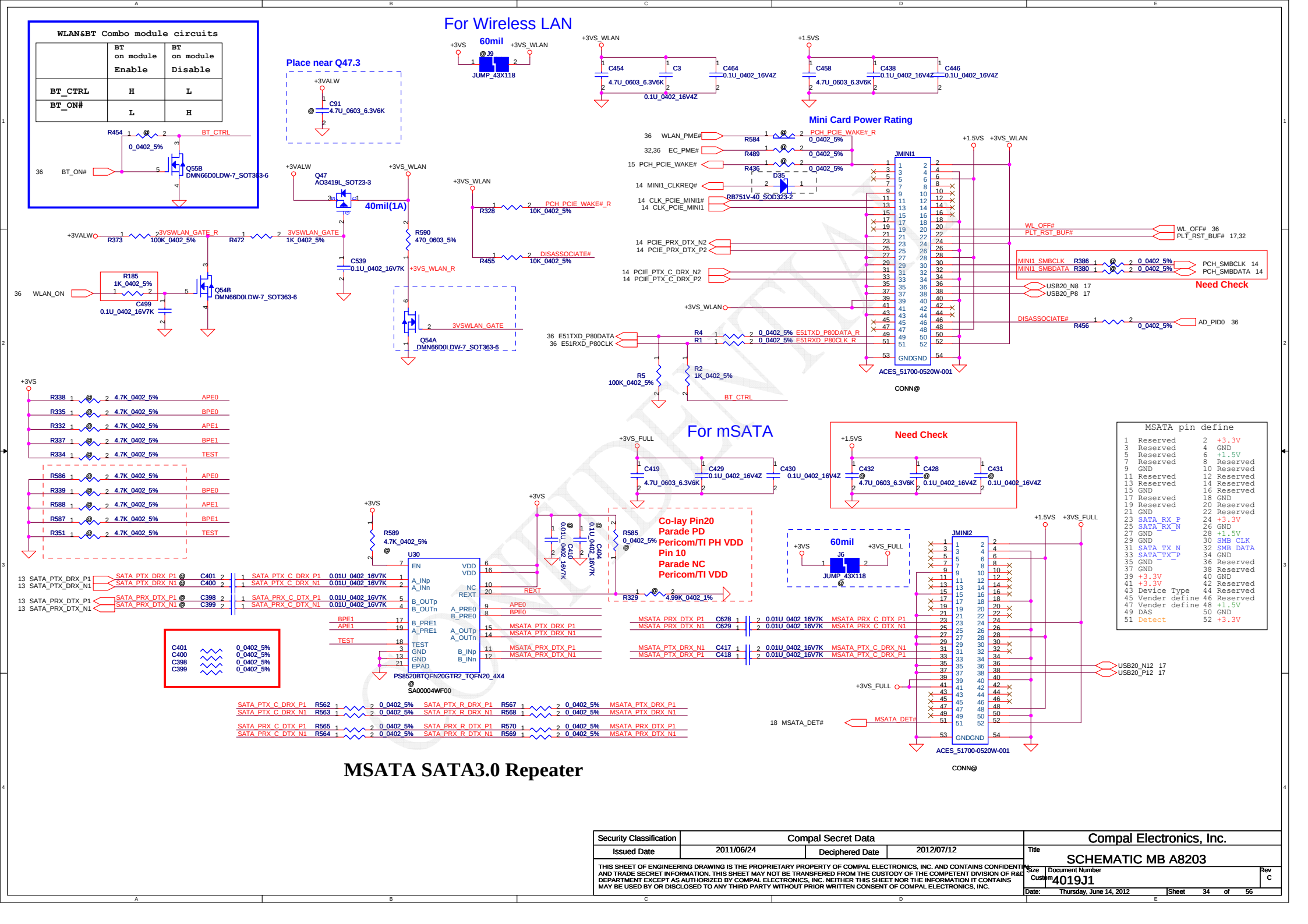
WLAN&BT Combo module circuits
BT on module Enable
BT on module Disable
BT_CTRL H L
BT_ON# L H
For Wireless LAN
Place near Q47.3
60mil
JUMP_43X118
Mini Card Power Rating
40mil(1A)
Need Check
For mSATA
Co-lay Pin20 Parade PD Pericom/TI PH VDD
Pin 10 Parade NC Pericom/TI VDD
MSATA pin define
PS8520BTQFN20GTR2_TQFN20_4X4
ACES_51700-0520W-001
CONN@
MSATA SATA3.0 Repeater
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SCHEMATIC MB A8203
4019J1
Thursday, June 14, 2012
Compal Secret Data
2011/06/24
2012/07/12
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USB Host Charger

CB	SELCDP	
0	X	DCP(Dedicated Charging Port) autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP(Standard Downstream Port) only
1	1	S0 charging with CDP(Charging Downstream Port) or SDP only

SM070000S80 WCM2012F2SF-670T04 67ohm

SM070000S80 WCM2012F2SF-670T04 67ohm

SM070000S80 WCM2012F2SF-670T04 67ohm

SM070000S80 WCM2012F2SF-670T04 67ohm

For ESD request

For USB2.0 ESD request

SM070000S80 WCM2012F2SF-670T04 67ohm

USB3.0 Conn.

SF000002Y00
220U 6.3V OSCON
ESR 17mohm@100Khz

DC23300AI00

SM070000S80 WCM2012F2SF-670T04 67ohm

For ESD request

For USB2.0 ESD request

SM070000S80 WCM2012F2SF-670T04 67ohm

USB3.0 Conn.

SF000002Y00
220U 6.3V OSCON
ESR 17mohm@100Khz

DC23300AI00

SM070000S80 WCM2012F2SF-670T04 67ohm

SM070000S80 WCM2012F2SF-670T04 67ohm

For USB2.0 ESD request

USB2.0 Conn.

SF000002Y00
220U 6.3V OSCON
ESR 17mohm@100Khz

DC23300AI00

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SM010015410 300ma 80ohm@100mhz DCR 0.3

2012/04/03 remove Q50 for connection wrong

2012/04/03 remove Q50 for connection wrong

Latest design guide suggest change to 74LVC1G06.

ESD request

PU at LAN side

Need check

Follow KB930 checking List

11/15 Power modify

KB930&9012 Co-Layout Item

Pin 111 is a power source for HW operation of KB9012.
So, power plan will be different between KB930 and KB9012.

Pin74(KB930),Pin118(KB9012) are with different PECI pin location, so HW must co-layout for it.
Please make sure which EC pin will be connected to PECI circuit.

Pin104 This co-layouted circuit is for power fail function of KB930 and KB9012.At KB930, PCH_PWROK will be connected to pin 104. At KB9012,PCH_PWROK will be connected to pin 32, and VCOUT0_PH will be connected to pin 104.

KB930&9012 Co-Layout Item KB930 use 128KB ROM KB9012 Embedded 128KB ROM

SM010015410 300ma 80ohm@100mhz DCR 0.3

Board ID
Analog Board ID definition, Please see page 3.

Project ID
Analog Board ID definition, Please see page 3.

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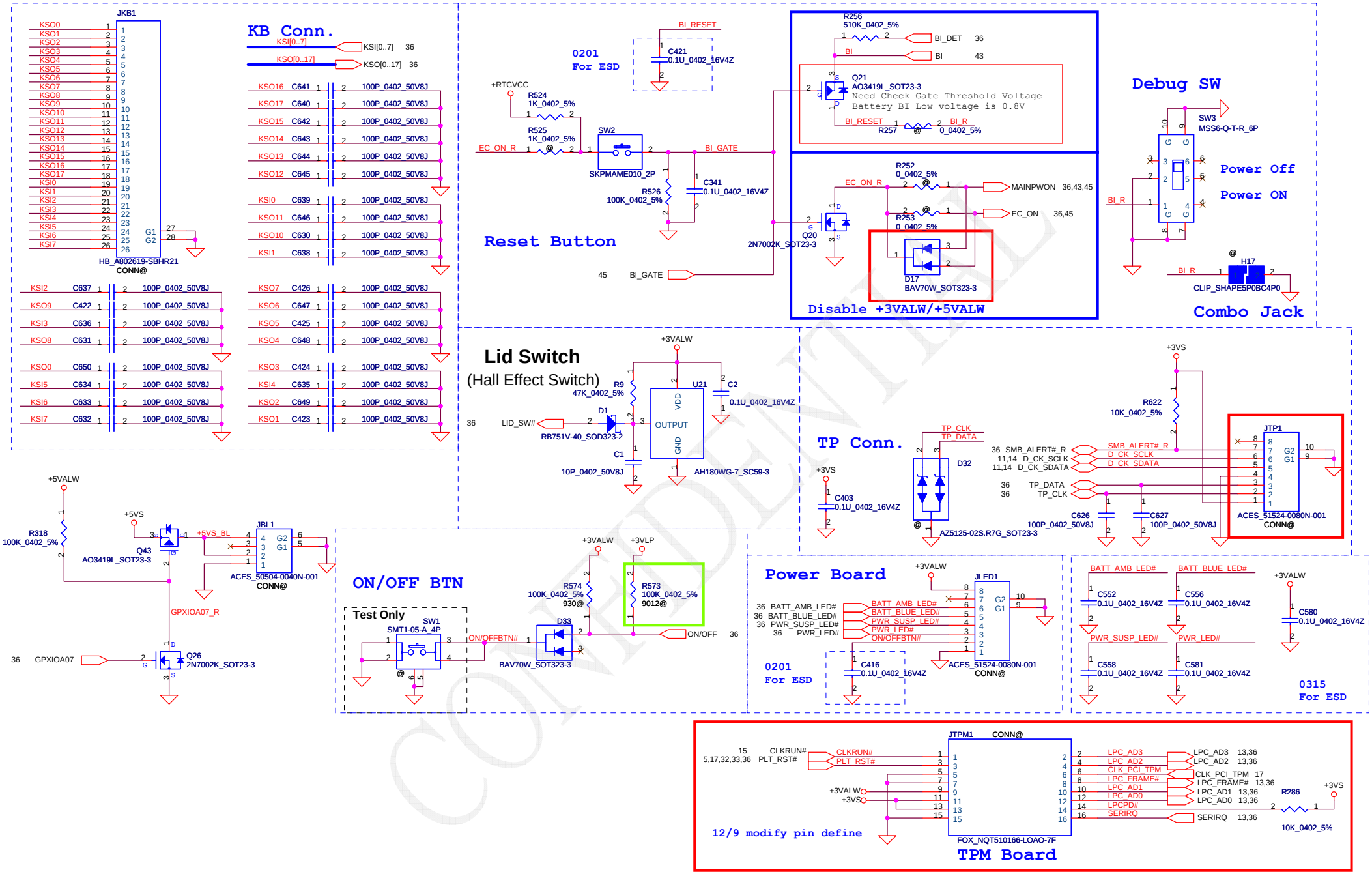

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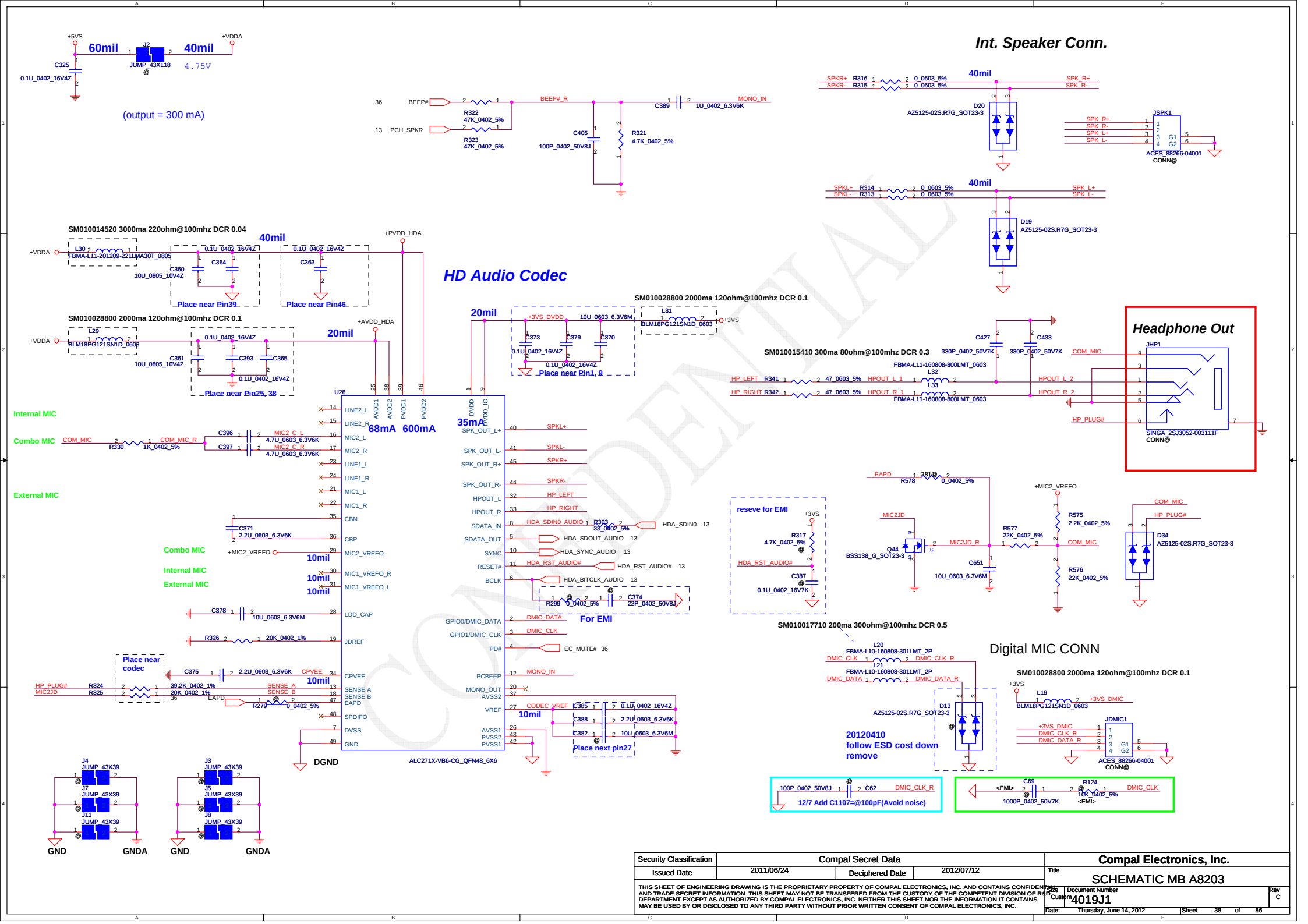

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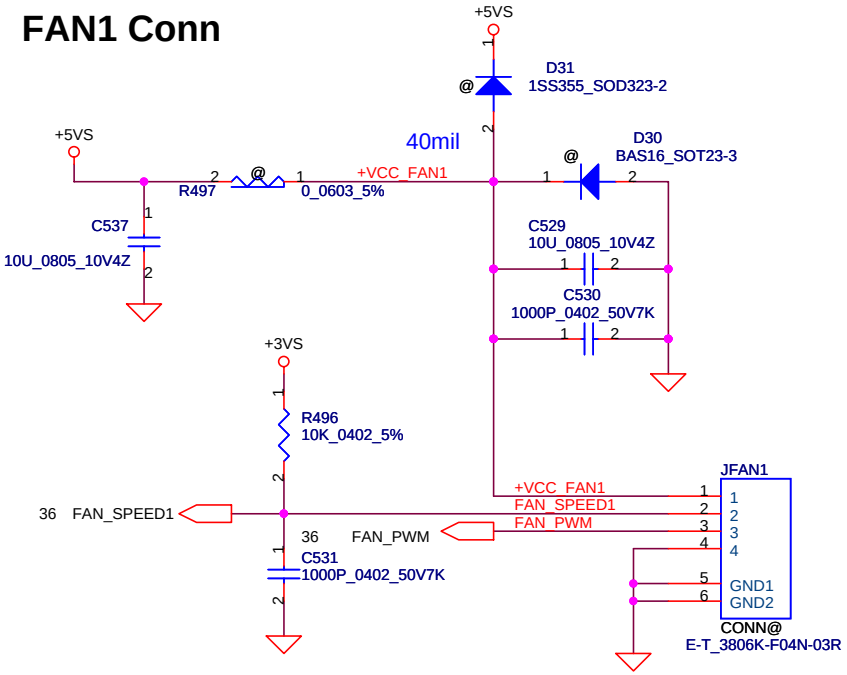
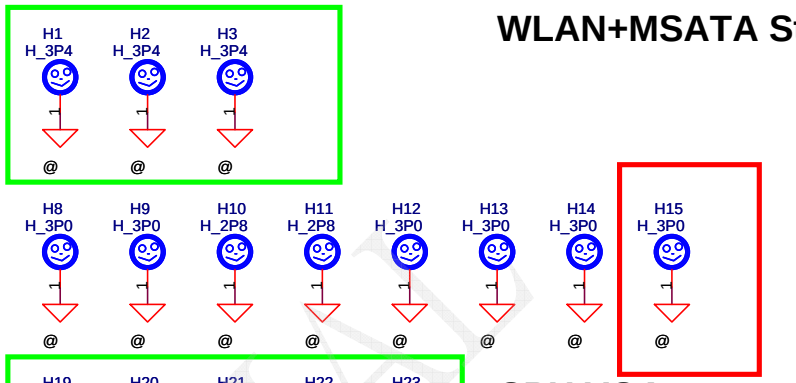
FAN1 Conn

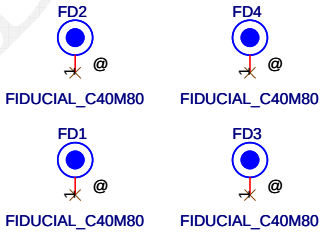


WLAN+MSATA Stand off



CPU,VGA support plate

locate MB



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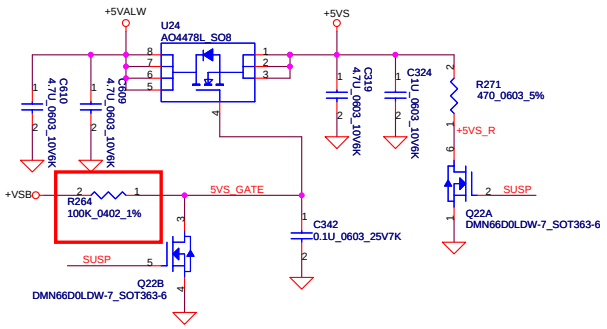
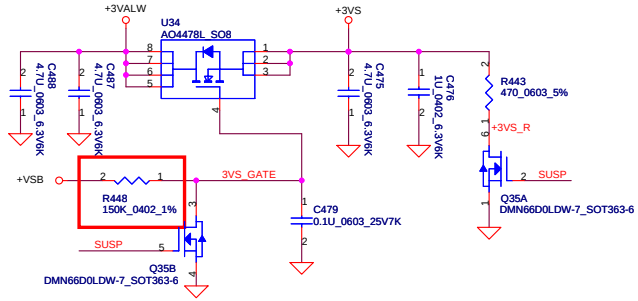
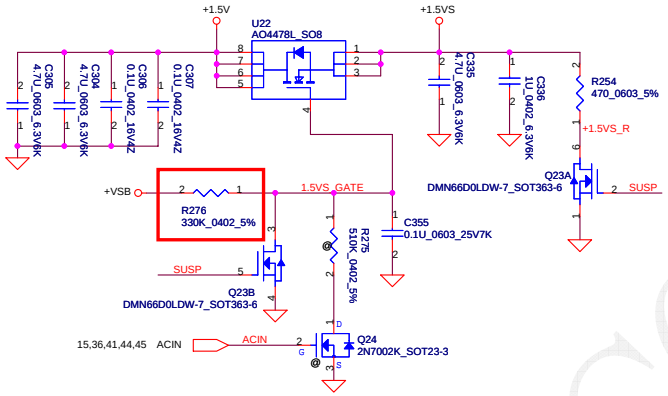
+5VALW TO +5VS

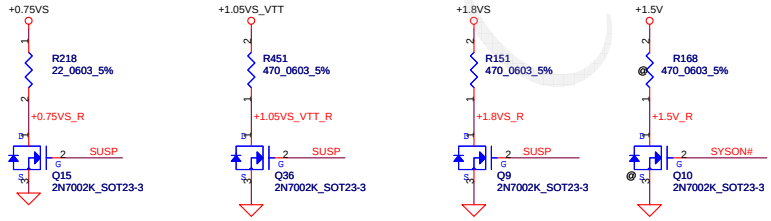


+3VALW TO +3VS



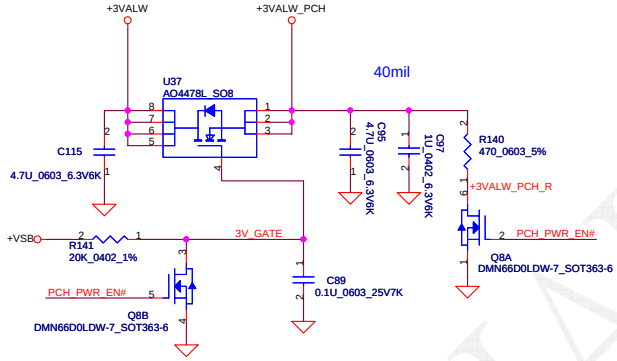
+1.5V to +1.5VS

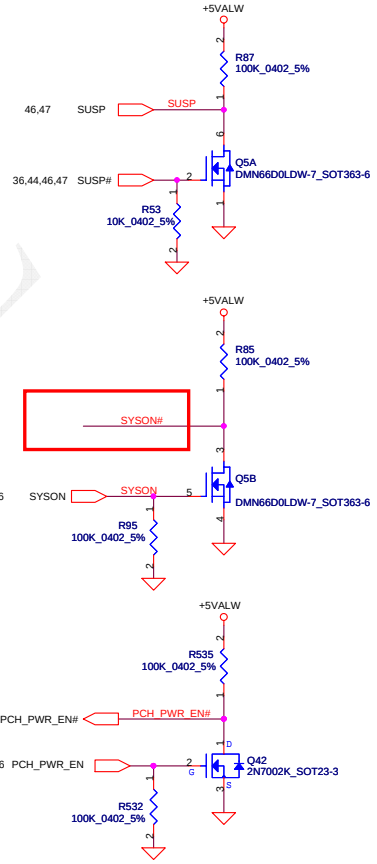




+3VALW TO +3VALW(PCH AUX Power)

Short J5 for PCH VCCSUS3.3





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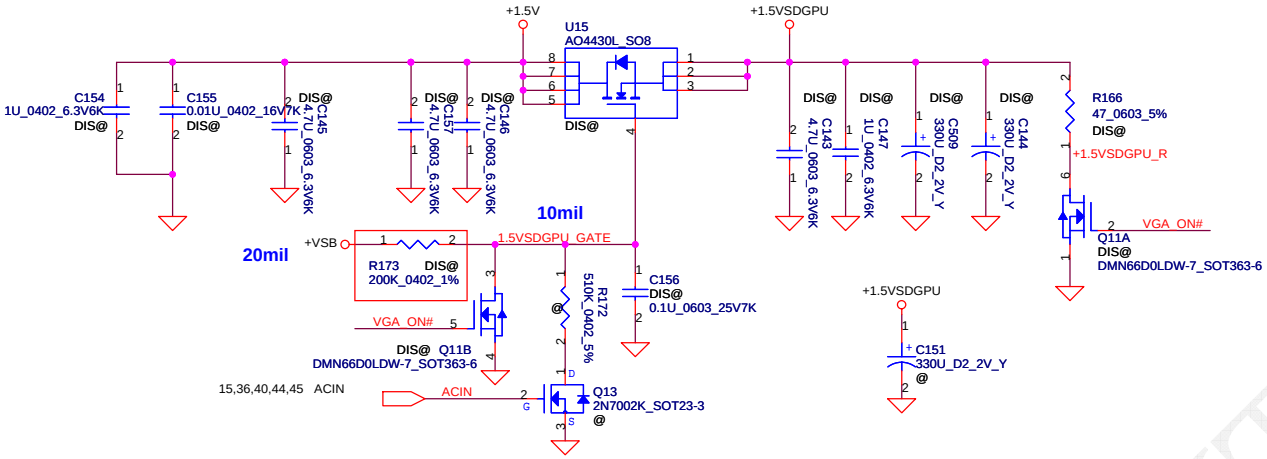
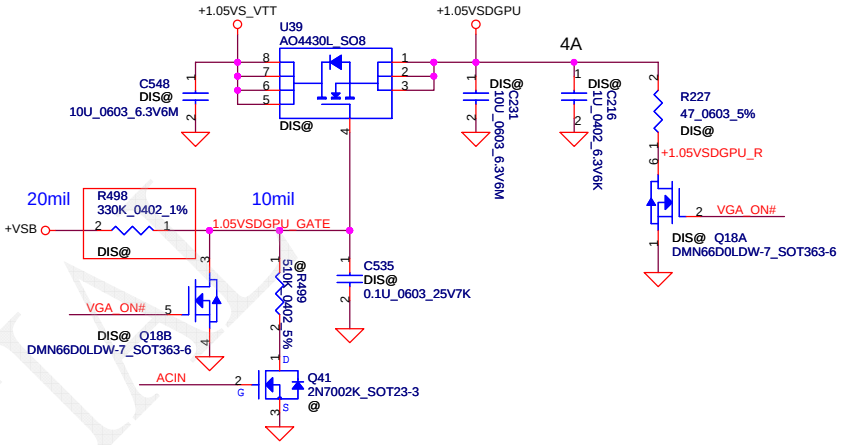
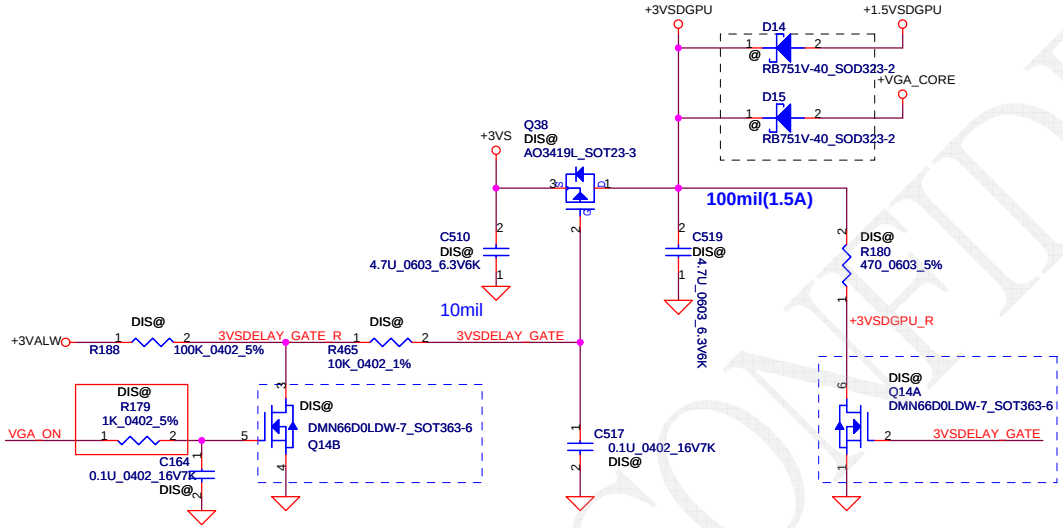
+1.5VSDGPUH to +1.5VSDGPU for GPU

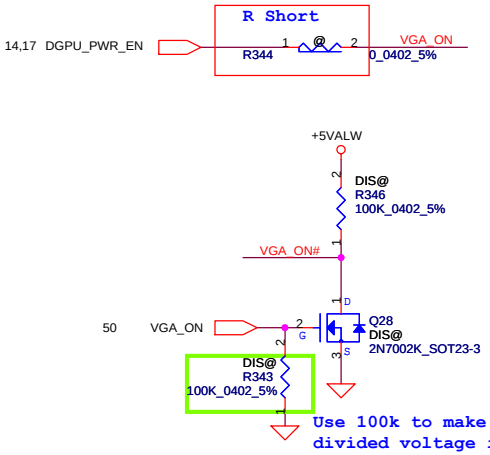


+1.05VS_VTT to +1.05VSDGPU for GPU



+3VS to +3VSDGPU for GPU





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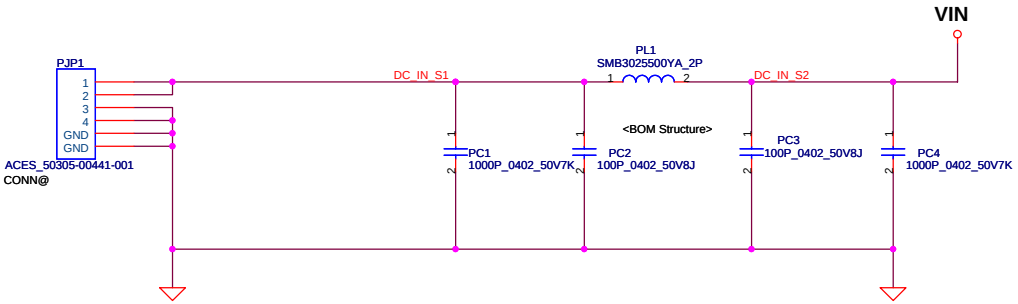

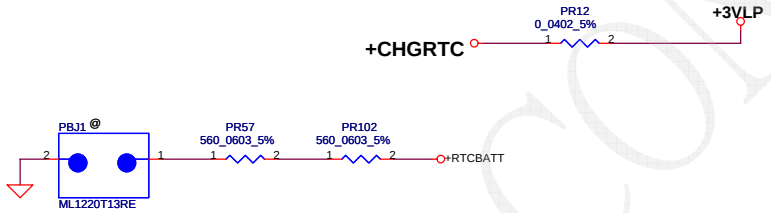

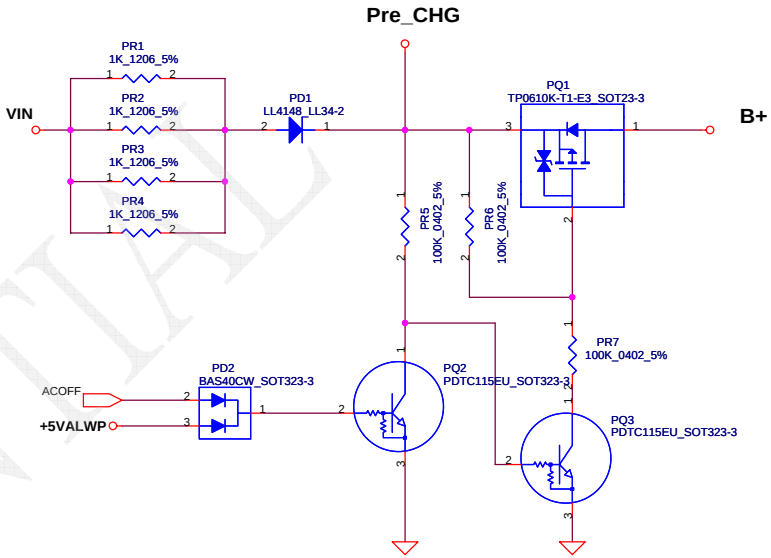

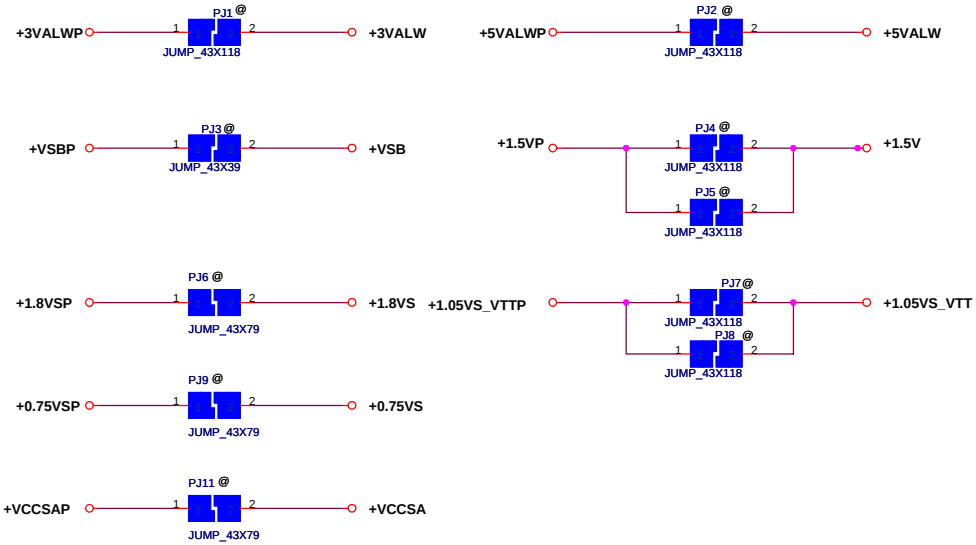

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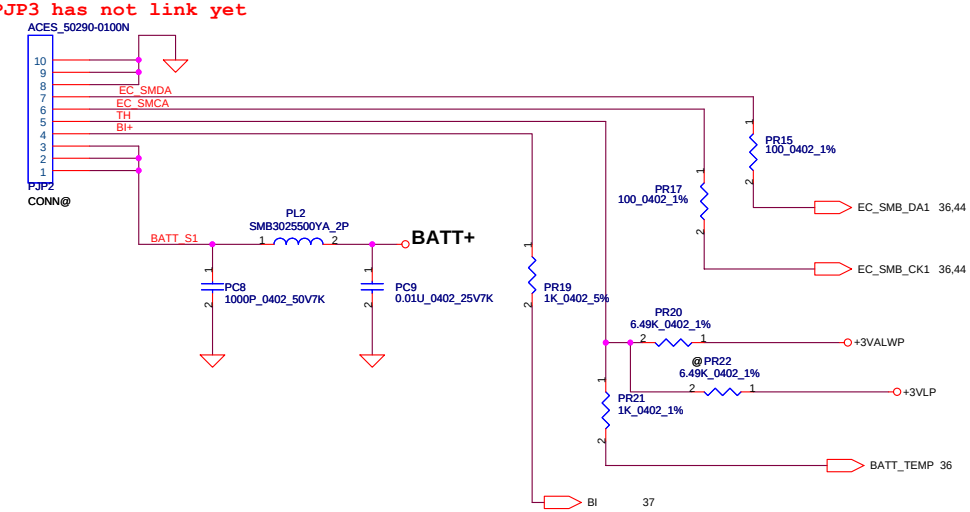
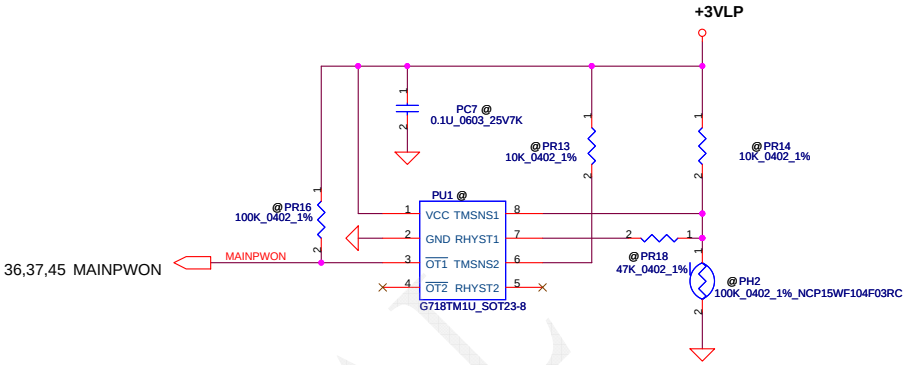
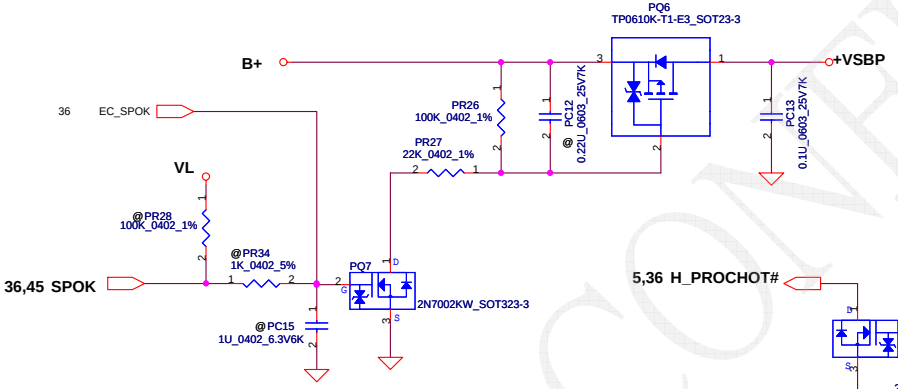
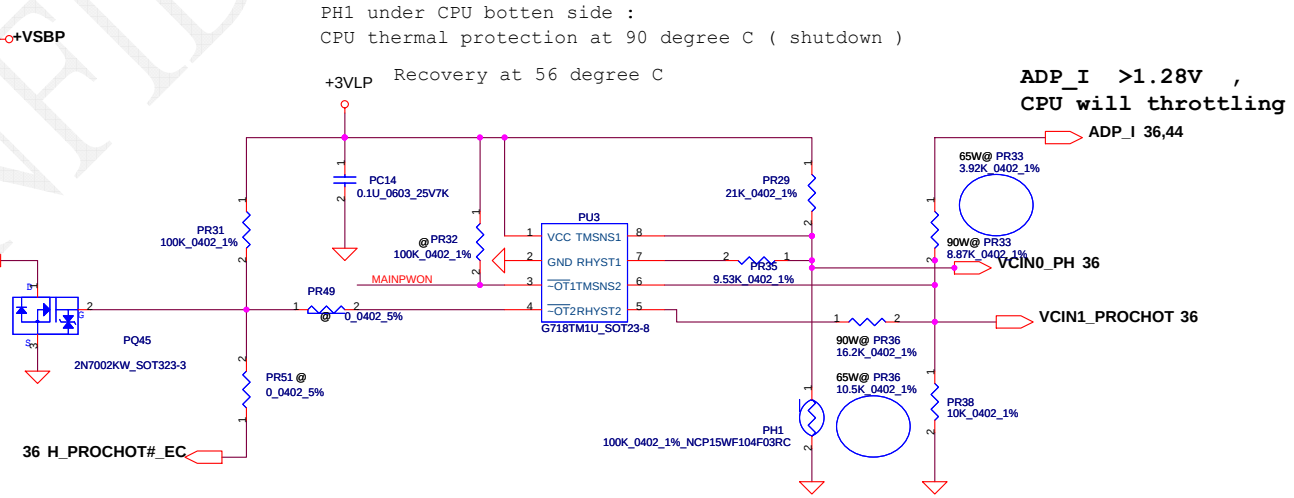
PJP3 has not link yet









For 65W adapter==>action 70W , Recovery 54W
For 90W adapter==>action 97W , Recovery 75W

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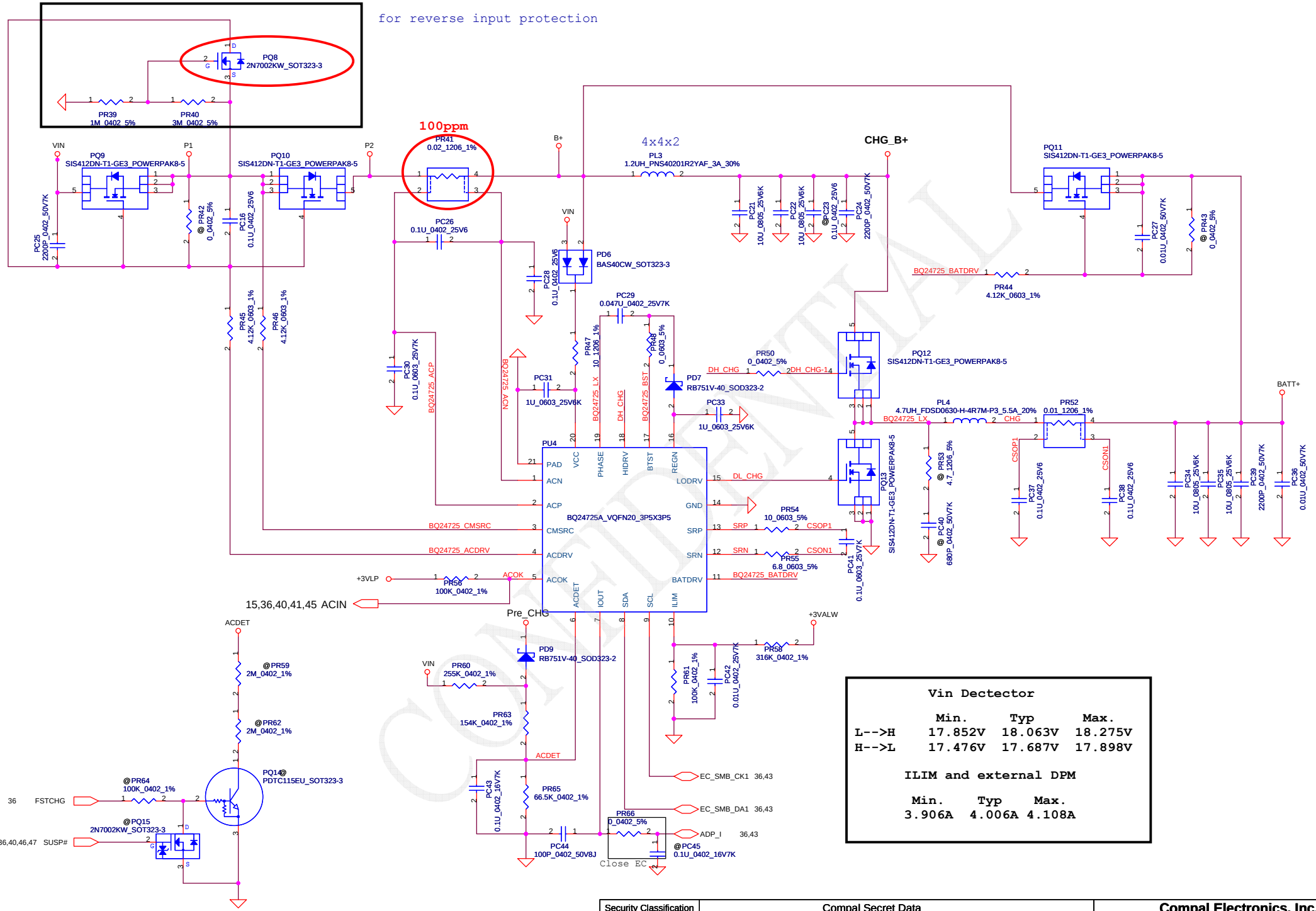

Vin Dectector

	Min.	Typ	Max.
L-->H	17.852V	18.063V	18.275V
H-->L	17.476V	17.687V	17.898V

ILIM and external DPM

Min.	Typ	Max.
3.906A	4.006A	4.108A

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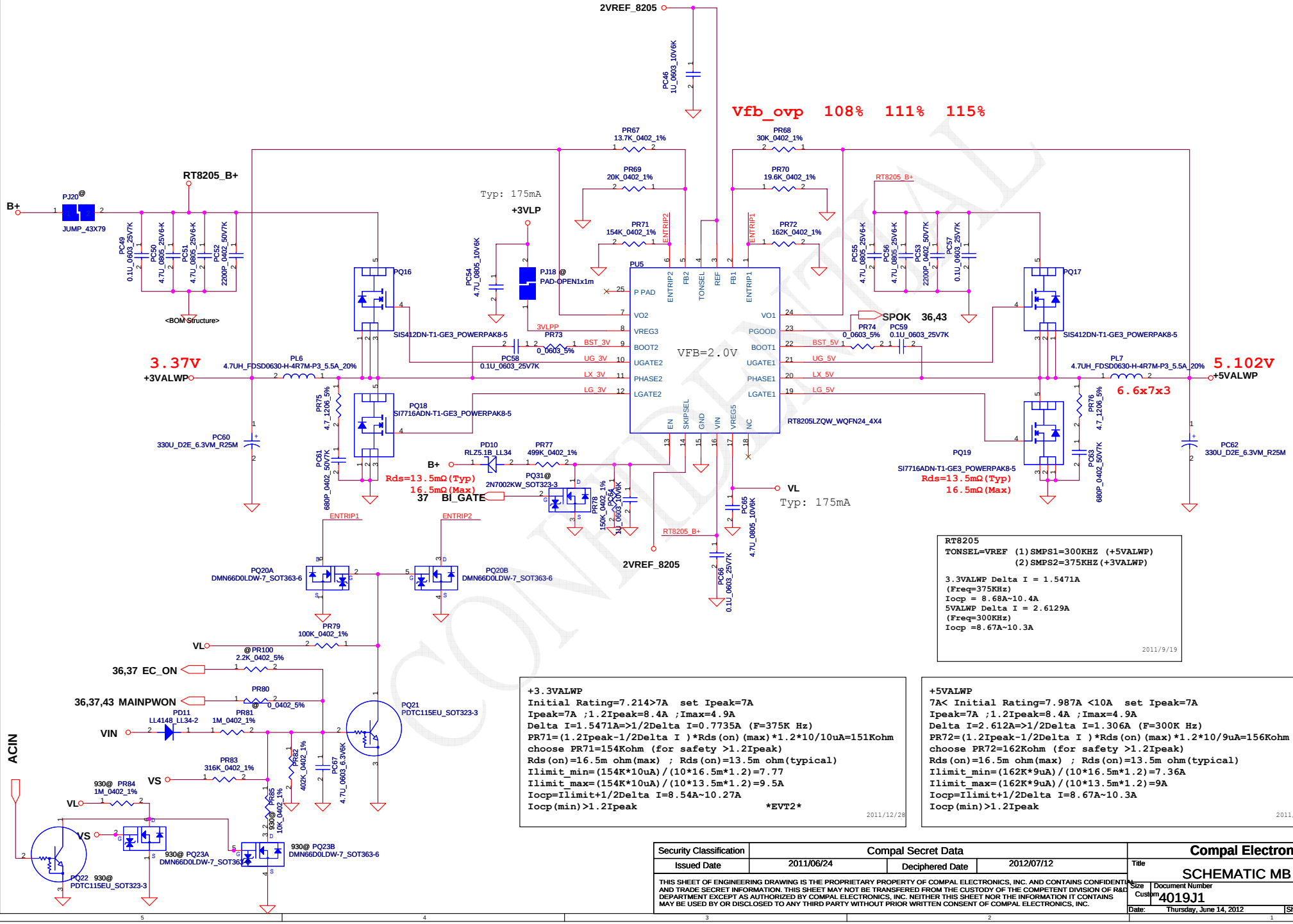
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



RT8205
TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)
(2)SMPS2=375KHZ(+3VALWP)

3.3VALWP Delta I = 1.5471A
(Freq=375KHz)
Iocp = 8.68A~10.4A
5VALWP Delta I = 2.6129A
(Freq=300KHz)
Iocp =8.67A~10.3A

2011/9/19

+3.3VALWP
Initial Rating=7.214>7A set Ipeak=7A
Ipeak=7A ;1.2Ipeak=8.4A ;Imax=4.9A
Delta I=1.5471A=>1/2Delta I=0.7735A (F=375K Hz)
PR71=(1.2Ipeak-1/2Delta I)*Rds(on)(max)*1.2*10/10uA=151Kohm
choose PR71=154Kohm (for safety >1.2Ipeak)
Rds(on)=16.5m ohm(max) ; Rds(on)=13.5m ohm(typical)
Ilimit_min=(154K*10uA)/(10*16.5m*1.2)=7.77
Ilimit_max=(154K*10uA)/(10*13.5m*1.2)=9.5A
Iocp=Ilimit+1/2Delta I=8.54A~10.27A
Iocp(min)>1.2Ipeak *EVT2*

2011/12/28

+5VALWP
7A< Initial Rating=7.987A <10A set Ipeak=7A
Ipeak=7A ;1.2Ipeak=8.4A ;Imax=4.9A
Delta I=2.612A=>1/2Delta I=1.306A (F=300K Hz)
PR72=(1.2Ipeak-1/2Delta I)*Rds(on)(max)*1.2*10/9uA=156Kohm
choose PR72=162Kohm (for safety >1.2Ipeak)
Rds(on)=16.5m ohm(max) ; Rds(on)=13.5m ohm(typical)
Ilimit_min=(162K*9uA)/(10*16.5m*1.2)=7.36A
Ilimit_max=(162K*9uA)/(10*13.5m*1.2)=9A
Iocp=Ilimit+1/2Delta I=8.67A~10.3A
Iocp(min)>1.2Ipeak

2011/9/19

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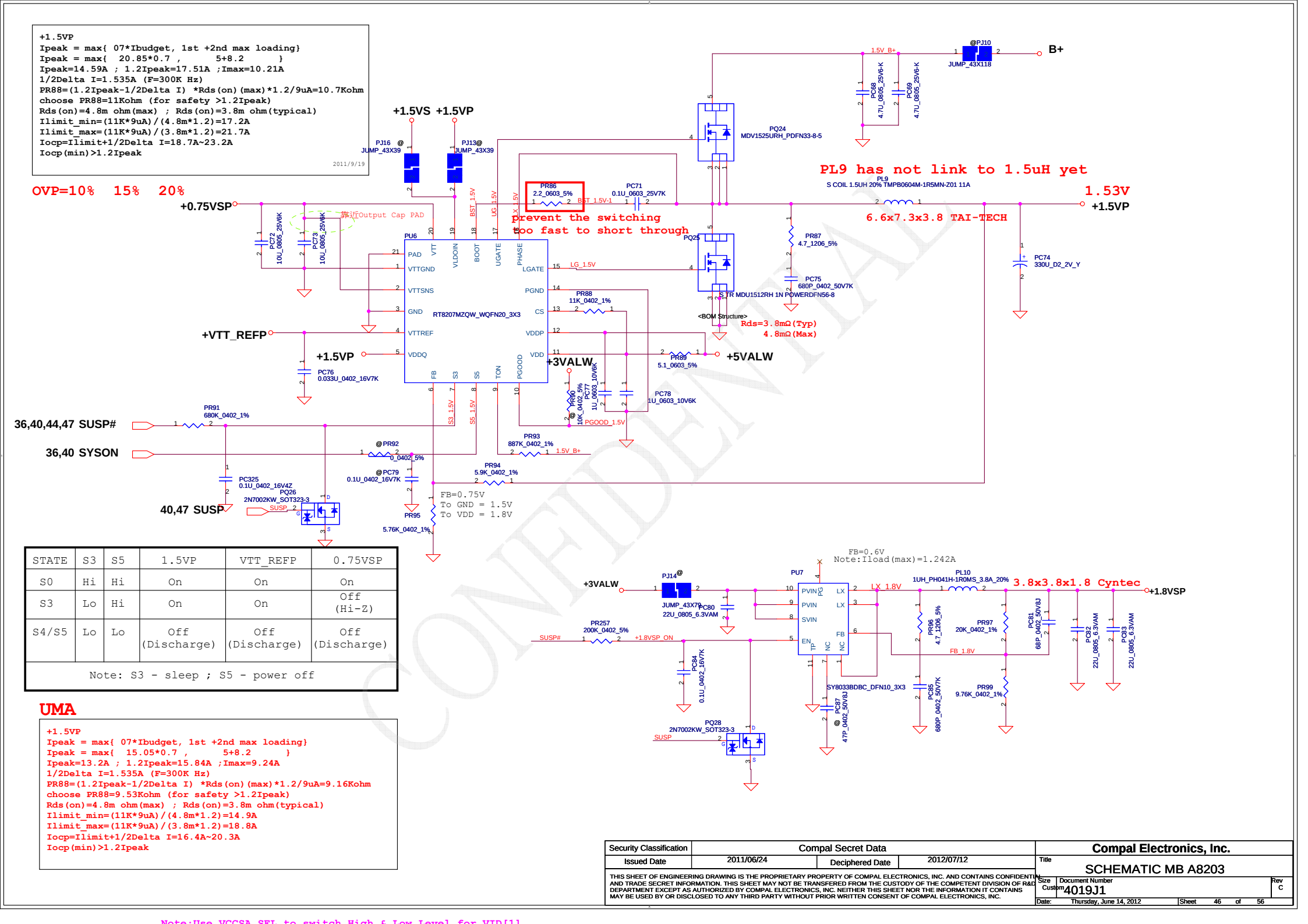

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

UMA

```
+1.5VP
Ipeak = max{ 07*Ibudget, 1st +2nd max loading}
Ipeak = max{  15.05*0.7 ,      5+8.2       }
Ipeak=13.2A ; 1.2Ipeak=15.84A ;Imax=9.24A
1/2Delta I=1.535A (F=300K Hz)
PR88=(1.2Ipeak-1/2Delta I) *Rds(on)(max)*1.2/9uA=9.16Kohm
choose PR88=9.53Kohm (for safety >1.2Ipeak)
Rds(on)=4.8m ohm(max) ; Rds(on)=3.8m ohm(typical)
Ilimit_min=(11K*9uA)/(4.8m*1.2)=14.9A
Ilimit_max=(11K*9uA)/(3.8m*1.2)=18.8A
Iocp=Ilimit+1/2Delta I=16.4A~20.3A
Iocp(min)>1.2Ipeak
```

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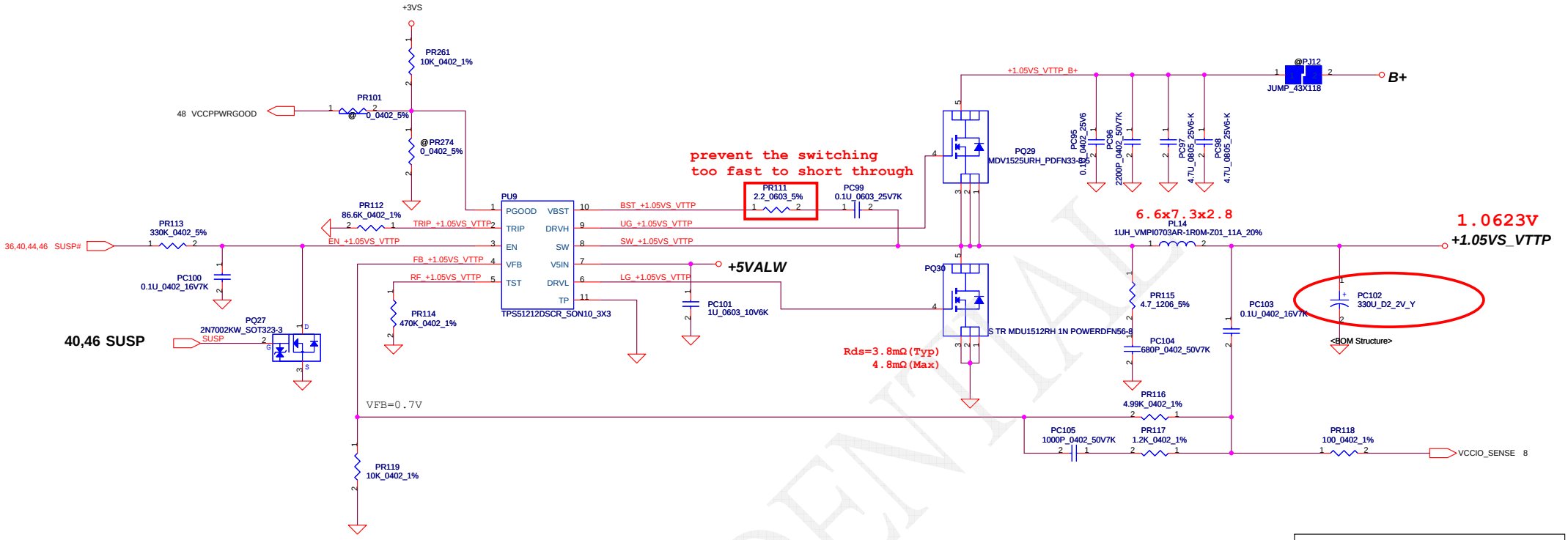

VFB= 0.704V
Vo=VFB*(1+PR116+PR118/PR119)= 1.05V
Freq= 266~314KHz , 290KHz(typ)

OVP 120% 125% 130%

+1.05VS
Ipeak=max(Ibudgt*0.7=13.42 , 8.5+6.842=15.34)
Ipeak=15.34A ;1.2Ipeak=18.408A ;Imax=10.732A
1/2Delta I=1.7102A (F=290K Hz)
PR112=(1.2Ipeak-1/2Delta I) *Rds(on)(max)*1.2*8/9uA=85.5Kohm
choose PR112=86.6Kohm (for safety >1.2Ipeak)
Rds(on)=4.8m ohm(max) ; Rds(on)=3.8m ohm(typical)
Ilimit_min=(86.6K*9uA)/(8*4.8m*1.2)=16.9A
Ilimit_max=(86.6K*9uA)/(8*3.8m*1.2)=21.4A
Iocp=Ilimit+1/2Delta I=18.6A~23.1A
Iocp(min)>1.2Ipeak

2011/9/19

UMA Ipeak value equal to discrete

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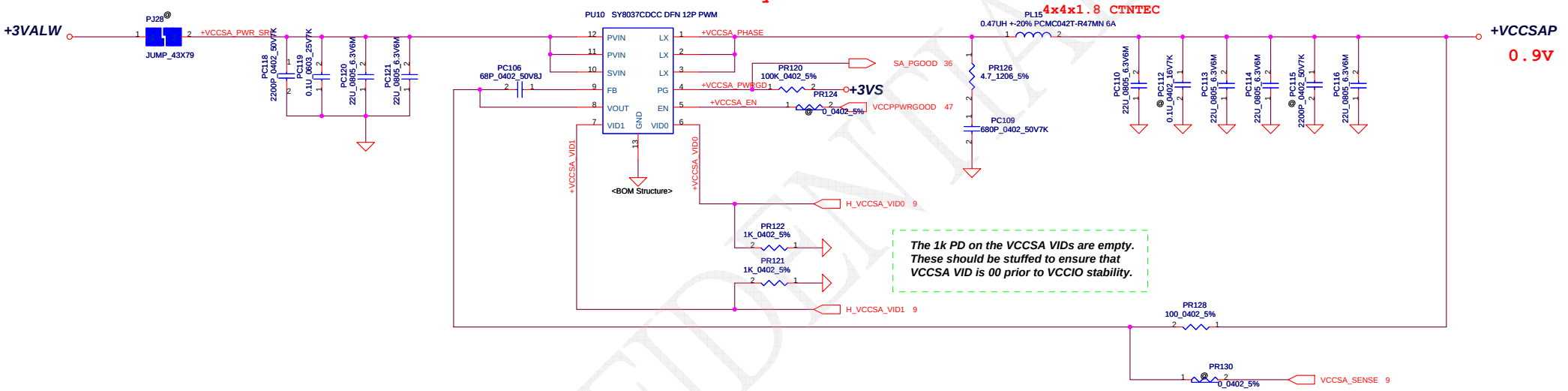
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

PU10 Has not Link 8037C yet



The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

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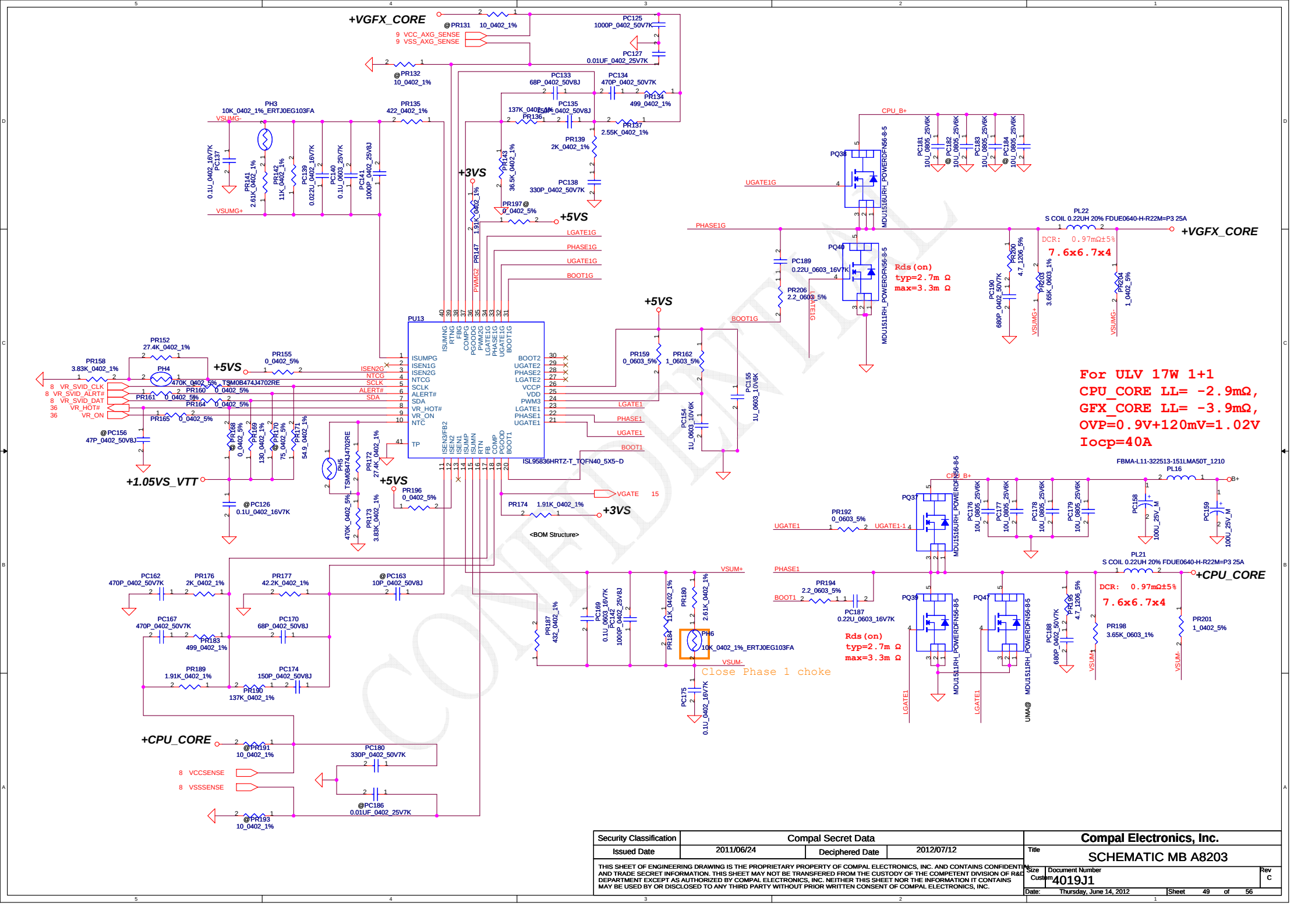

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VGA Chipset	Default Voltage	VID6	VID5	VID4	VID3	VID2	VID1	VID0
N13P GS	0.9V	0	1	1	0	0	0	0

boot resistor to 1.1V

GPU_HOT#

Rds(on)
typ=2.7m Ω
max=3.3m Ω

Rds(on)
typ=2.7m Ω
max=3.3m Ω

LL Disable
N13P_GS with turbo
Iccmax=50A
Iocp =60A

DCR: 0.97mΩ±5%
7.6x6.7x4

DCR: 0.97mΩ±5%
7.6x6.7x4

Layout Note:
Place near Phase1 Choke

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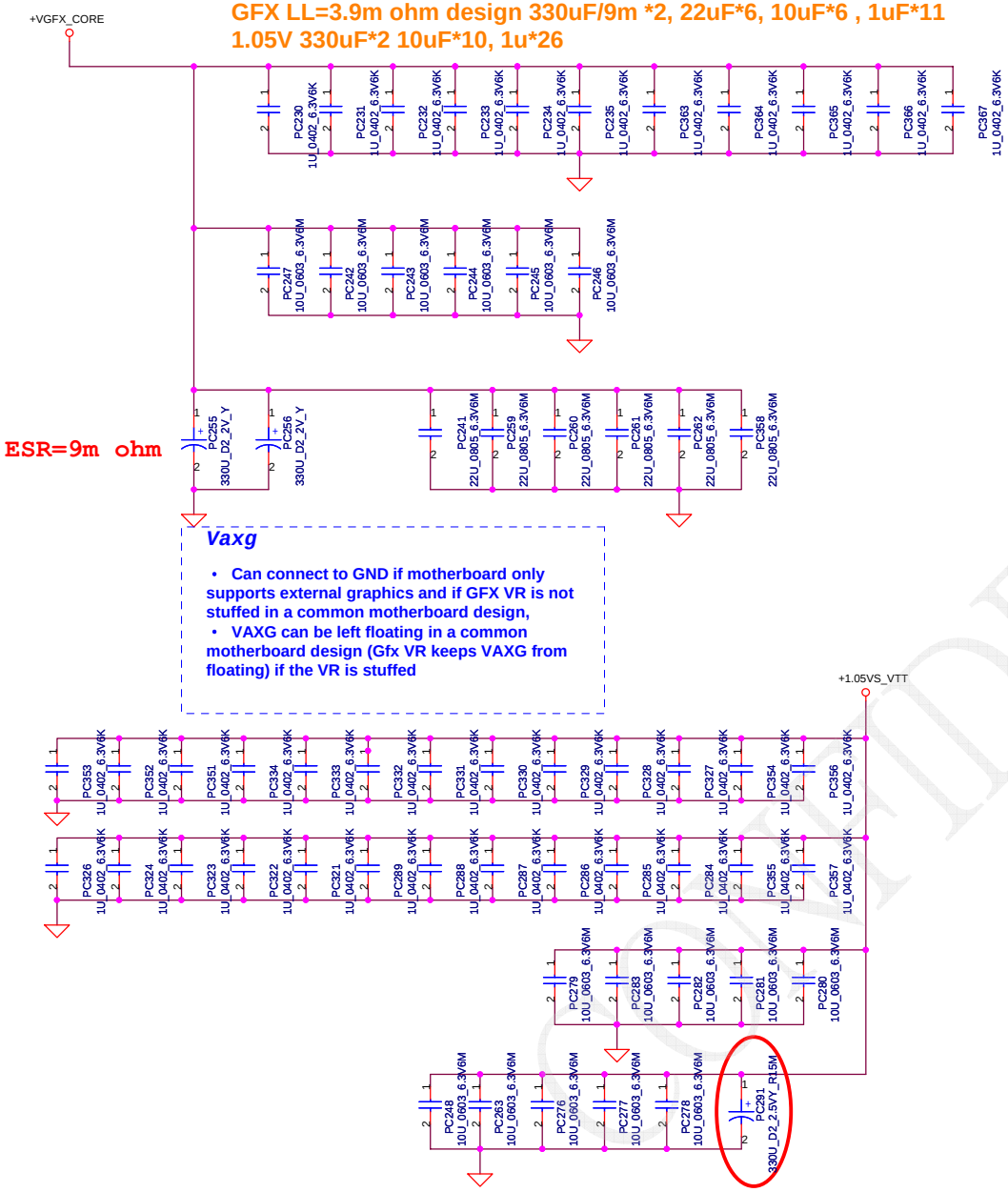
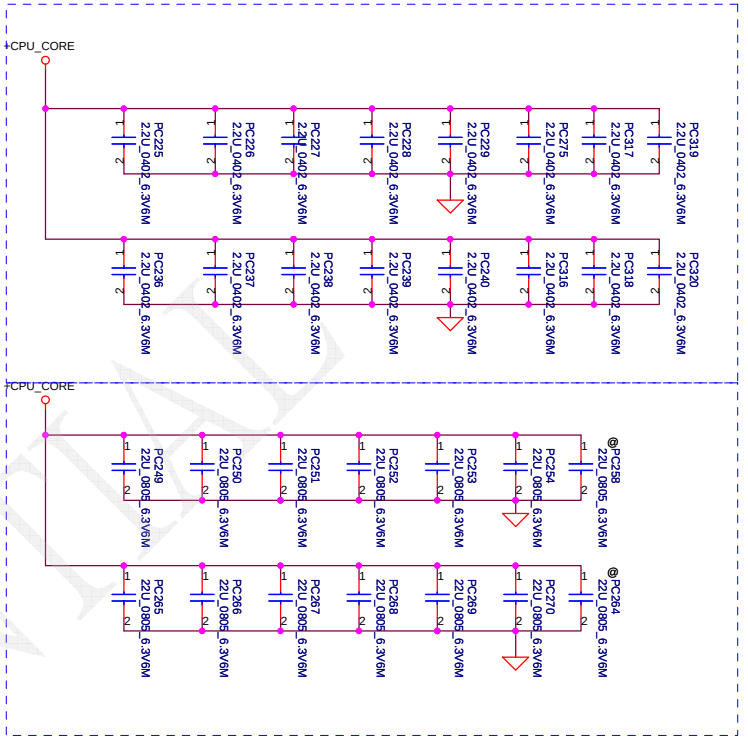
PWR Rule
CPU LL=2.9m ohm dedign 330uF/9m *4, 22uF *12, 2.2uF*16
GFX LL=3.9m ohm design 330uF/9m *2, 22uF*6, 10uF*6 , 1uF*11
1.05V 330uF*2 10uF*10, 1u*26

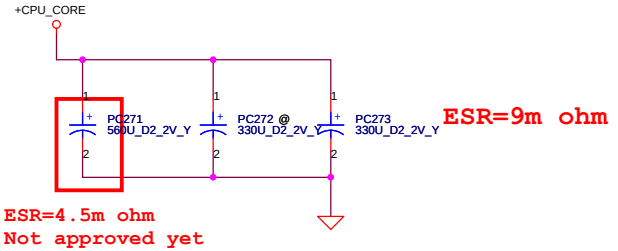


Vaxg

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

INTEL Recommend
3*330uF(1 in other page),12*22uF, 5 no stuff
from PDDG 1.0





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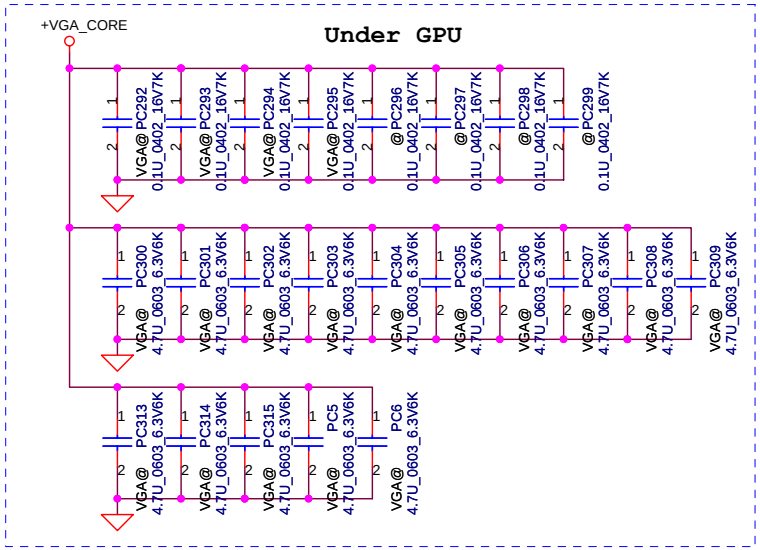
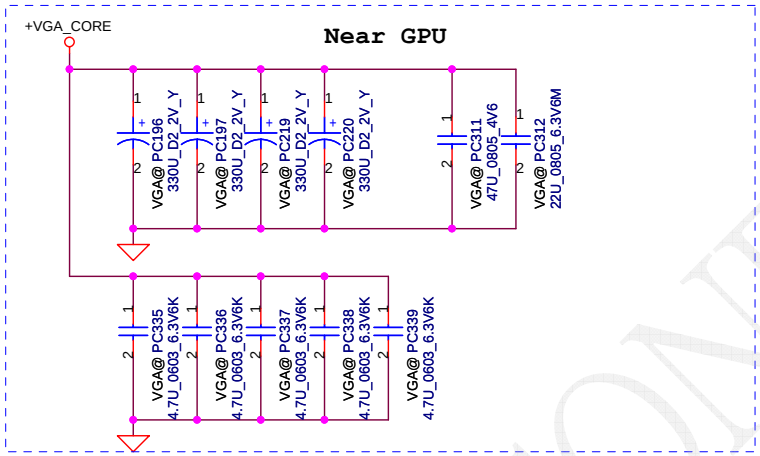


NV DG NVVDD
N13P-GS GB4-128
4.7Ux15,0.1Ux8(4@) Under GPU
330Ux4 , 47Ux1,22Ux1,4.7Ux5 Near GPU



330u=> ESR=9m ohm

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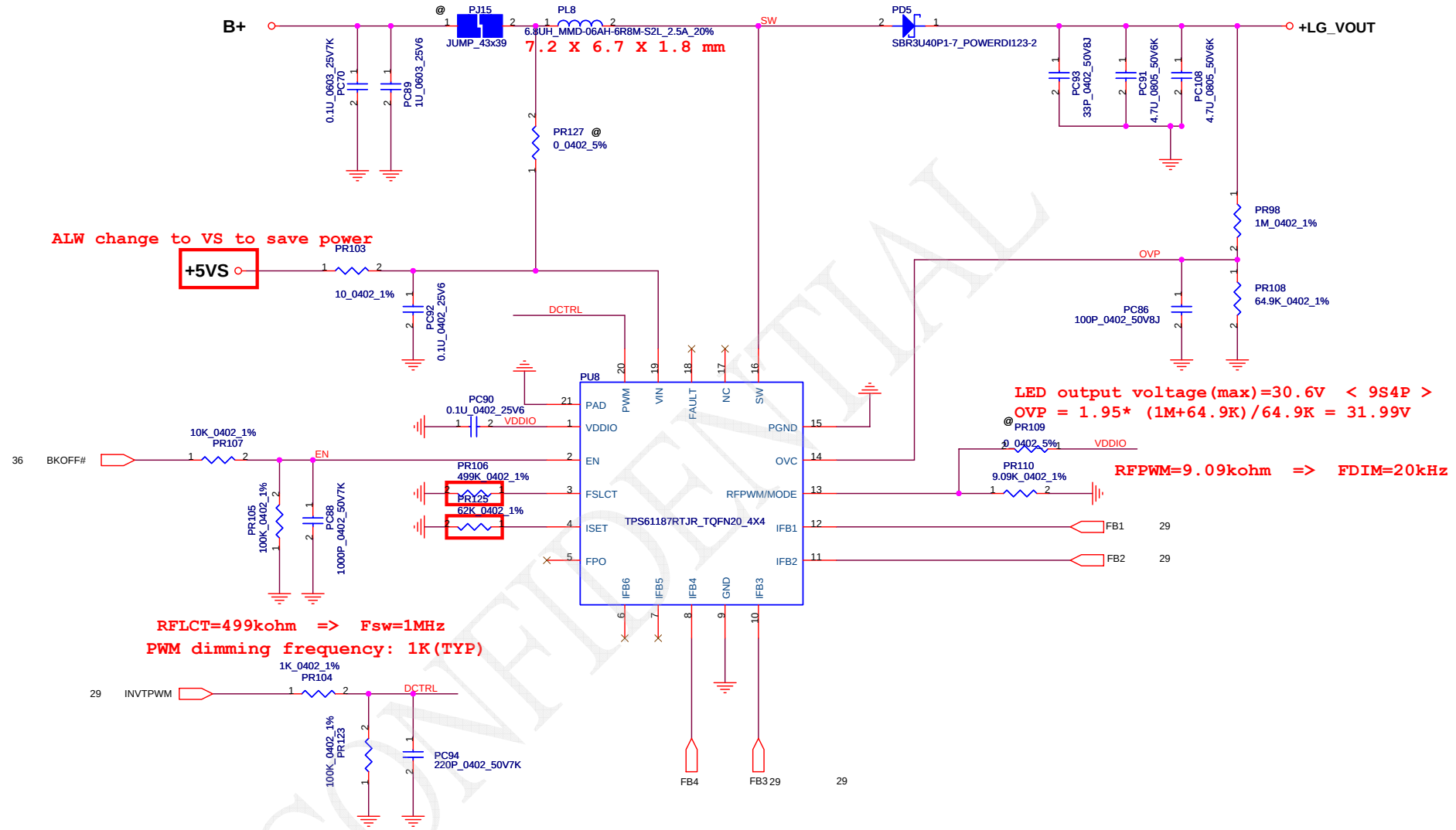

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	VGA boot voltage	Vboot Voltage can not allow to boot to 1.1V		VGA	take off the PR212	11/22	EVT2
2	HW sequence	tune the correct sequence		VGA	PR209 set to 100k ohm ,PC107 set to 0.1u	11/22	EVT2
3	HW sequence	tune the correct sequence		1.05	put on the PQ27	11/20	EVT2
4	HW sequence	tune the correct sequence		1.8	put on the PQ28	11/20	EVT2
5	HW sequence	tune the correct sequence		0.75	put on the PR91 680k,Pc325 0.1u, PQ26,PJ16	11/20	EVT2
6	CPU overshoot	in order to follow the intel spec to reduce the overshoot		CPU	change the original 330u X3 to 330u + 560u	11/25	EVT2
7	HW sequence	tune the correct sequence		1.5V	add PJ16 and PQ26	11/22	EVT2
8	Panel demand	change the cap 35V to 50V		LED driver	change pc91 and pc108 to 50V cap	11/28	EVT2
9	ME demand	can see the cap throuth the thermal hole		CPU	take out the pc158 replace by pc159	3/13	PVT
10	acoustic demand	can't pass acoustic acer spec		CPU	add PC158 PC159	3/22	PVT2
11	component Vgs not satisfy	afraid Vgs is too small		charger	change PQ8 material	3/22	PVT2
12	0ohm resister cost down	PPM request cost down			R_SHORT PR49,PR80,PR92,PR124,PR101, PR130,PR207,PR218,PR236,PR243	3/22	PVT2
13							
14							
15							
16							
17							

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Change R558 to @(0_0402),C618(0.1U_0402) for AD_PID0
ADD R455 PH 4.7K_0402(SD028470180)(DISASSOCIATE#) <- ?K
ADD R454(@) (0_0402) for cost down BT power control
ADD R456 (0_0402)(SD028000080) for IOAC Pin46
POP Q46,R590 for Boardcom WLAN discharge

1/31
ADD R160 (0_0402) for USB_OC1# USB_OC0# colay

2/1
R549.1,R548.1 change from +3VLP to +3VALW_EC
remove stand along BT
remove USB20_N13 USB20_P13

for ESD:
ADD C416 0.1U_0402 ON/OFFBTN#
ADD C420 0.1U_0402 ON/OFF
ADD C421 0.1U_0402 BI_RESET
POP C345 0.01U_0402 PLT_RST#

Y2,X1 main source change from SJ10000DM00 to SJ100004Z00

2/2
ADD C151(@) 330U_D2
change U13 from SA00005AGE0 to SA00005AG00 (QS PCH)

2/6
ADD C91 @ 4.7U_0603 for WLAN Power CAP(SE107475K80)

2/7
for N13P-GS QS,MP strap
change R186 from 35K to 5K (Strap1 PD)

2/10
ADD Q43 (S TR AO3419L 1P SOT23-3) and JBL2 (S H-CONN ACES 50578-0040N-001 4P P1) for back light

2/13
for NV strap P.24
Change R184 from ES2GPU@ to @ (strap 2)
Delete R473 ES2GPU@ 10K_0402_1% (strap4)
Delete R469 HYN2G@ 34.8K_0402_1% (ROM_SCLK)
Add Hynix VRAM SA00004GD50 strap table (ROM_SI PD25K)

for Option Component
Delete PCB 8202@
Delete GPU U14 ES2GPU@ (SA000051800),QS2GPU@ (SA000051800)
Delete VRAM GDDR3@
Delete PCH U13 QSPCH@ (SA00005AG00),ES2PCH@ (SA00004NQB0)
Change VRAM X76 GDDR5@ to VRAM@ and add X76364BOL04

for PCH
Change U13 from SA00005AGE0 to SA00005AG00

for WLAN
Change R328,R455 from 4.7K_0402_5% to 10K_0402_5%
Change R73,R7,R102,R257,R279 from 0_0402_5% to 0 R_SHORT

2/14
for KB back light
Change location JBL2 to JBL1
Add Q26 (2N7002K_SOT23-3) and R318 510K_0402_5%

for GDDR5 GPIO define
Change R43 GDDR3@ to R43 @
Change R68 GDDR5@ to R68 DIS@

For GPU strap
Change R183 QSGPU@ to DIS@ (strap2)
Change R473 QSGPU@ to DIS@ (strap4)
Change R469 4.99K_0402_1% HYN2G@ to HYNMFR@ (ROM_SI)
Add R469 24.9K_0402_1% HYNAFR@ for VRAM Hynix AFR strap

2/15
for WLAN LED
Change EC pin102 net name fron VCIN1_PROCHOT_R to IRST_RST# P.38
Add net IRST_RST_R# on U25 pin1 and link R162 0_0402_5% to IRST_RST# P.17
Add R161 0_0402_5% on PLT_RST# P.17
Add net name PLT_RST_R# between R161 and R10 P.17

for LAN
Change net name from PLT_RST# to PLT_RST_BUF# P.34
Add net name PLT_RST_BUF_R# between R149.2 and U62.2

for KB back light
Add net name GPXIOA07_R between Q43.2 and Q26.1
Change R559 18K_0402_5% to 33K_0402_5%

2/15A
L27 change main source from SHI00007400 to SH00000JM00
ADD R163(0_0402_5%) for PLT_RST_LAN#

2/16
R422,R619,R65 change to 0ohm-Rshort
C452 change from 15P to 18P
Chang JBL1 footprint from 抽屜式 SP01000ZW00 to 掀蓋式 SP01000Z300
SW1 change to unpop

02/17
Q45,Q46 2N7002 change to Q54 dual 2N7002
3VSWLAN_R change name to +3VS_WLAN_R trace 20mil

2/18
R34 unpop(SUSWARN# PH 10K)
R26 unpop(PCH_ACIN PH 10K)

2/21
R466 change from 5K to 10K(for device manager 3D device)

Rev1.0
3/14
ADD D21 ESD diode near ODD prevent PCH crack
Q1 Q4 2N7002 combine to Dual 2N7002 Q55
R559 change 33K to 56K_0402_5% SD028560280(for Board ID 4)
R318 change 510K to 100K (BL KB)

3/15
R415 R150,R278,R280,R291,R295,R298 ,R584,R86,R160 change 0_0402_5# ot Rshort_0402
R450,R497 0_0603_5% to Rshort_0603
ADD C552,C556,C558,C580,C581 for ESD
(BATT_AMB_LED#,BATT_BLUE_LED#,PWR_SUSP_LED#,PWR_LED#,+3VALW) Place near JLED1
Q3,Q16,Q17,Q19,Q44 change from SB501380020 to SB501380050 (HF)

3/22
change PCH to MP version to SA00005AGI0

4/5
CR CPU P/N change to MP PN
SA00005L5C0,SA00005K6B0,SA00005K5B0
remove Q50 for PROCHOT# connection issue
4/10
follow ESD suggest remove D28,D13 for cost down

Rev1A 4/10 Fix Q50 PROCHOT# connection issue

5/8
Change SA00005MX10 (S IC AV8062701048004 QAXQ J1 1.5G BGA) to SA00005MX60 (S IC AV8062701048004 SR0CW J1 1.5G ABO!
Rev1A 5/9 Change R559 from 56K to 100K(Board ID update)

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PCB

ZZZ

LA-8203P MB Rev0: DA80000T600
LA-8203P MB Rev1: DA80000T610
LA-8203P MB with Small Board Rev1: DAZ0O200100

LA-8203P REV1 M/B
DAZ0O200100

CPU

UCPU1
I32367@
S IC AV8062701047904 SR0CV J1 1.4G ABO!
SA000051H60
AV8062701047904 SR0CV J1 1.4G ABO!

UCPU1
I32377@
S IC AV8062701048004 SR0CW J1 1.5G ABO!
SA00005MX60
AV8062701048004 SR0CW J1 1.5G ABO!

UCPU1
I52467@
S IC AV8062701047504 SR0D6 J1 1.6G ABO!
SA00004X010
AV8062701047504 SR0D6 J1 1.6G ABO!

SANDY BRIDGE

UCPU1
I33217@
S IC AV8063801058401 SR0N9 L1 1.8G BGA 1023 ABO !
SA00005L5C0
AV8063801058401 SR0N9 L1 1.8G BGA 1023 ABO !

UCPU1
I53317@
S IC AV8063801058002 SR0N8 L1 1.7G ABO!
SA00005K6B0
AV8063801058002 SR0N8 L1 1.7G ABO!

UCPU1
I73517@
S IC AV8063801057605 SR0N6 L1 1.9G BGA 1023 ABO !
SA00005K5B0
AV8063801057605 SR0N6 L1 1.9G BGA 1023 ABO !

IVY BRIDGE

UCPU1
QBP8@
S IC AV8063801057401 QBP8 K0 1.5G BGA
SA00005AZ00
AV8063801057401 QBP8 K0 1.5G BGA

UCPU1
QBP7@
S IC AV8063801057400 QBP7 K0 1.7G BGA
SA00005B000
AV8063801057400 QBP7 K0 1.7G BGA

EVT2

VRAM

ZZZ
VRAM@
ALT. GROUP PARTS VRAM X4 HYN 1G Q5LJ1
ALT. GROUP PARTS VRAMX4 HYN1G 38NM Q5LJ1
X76364BOL03|X76364BOL04
ALT. GROUP PARTS VRAM X4 HYN 1G Q5LJ1

DRAM

ZZZ
DRAM@
ALT. GROUP PARTS DRAM X4 ELP 2G Q5LJ1
ALT. GROUP PARTS DRAM X4 HYN 2G Q5LJ1
X76364BOL11|X76364BOL12
ALT. GROUP PARTS DRAM X4 HYN 2G Q5LJ1

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