Compal Confidential

QAL30 Project

LA-8061P REV 0.4 Schematic

Intel Ivy Bridge/Panther Point

2012-01-13 Rev. 0.4

Security Classification	Compal Secret Data		
Issued Date	2011/05/23	Deciphered Date	2012/12/31

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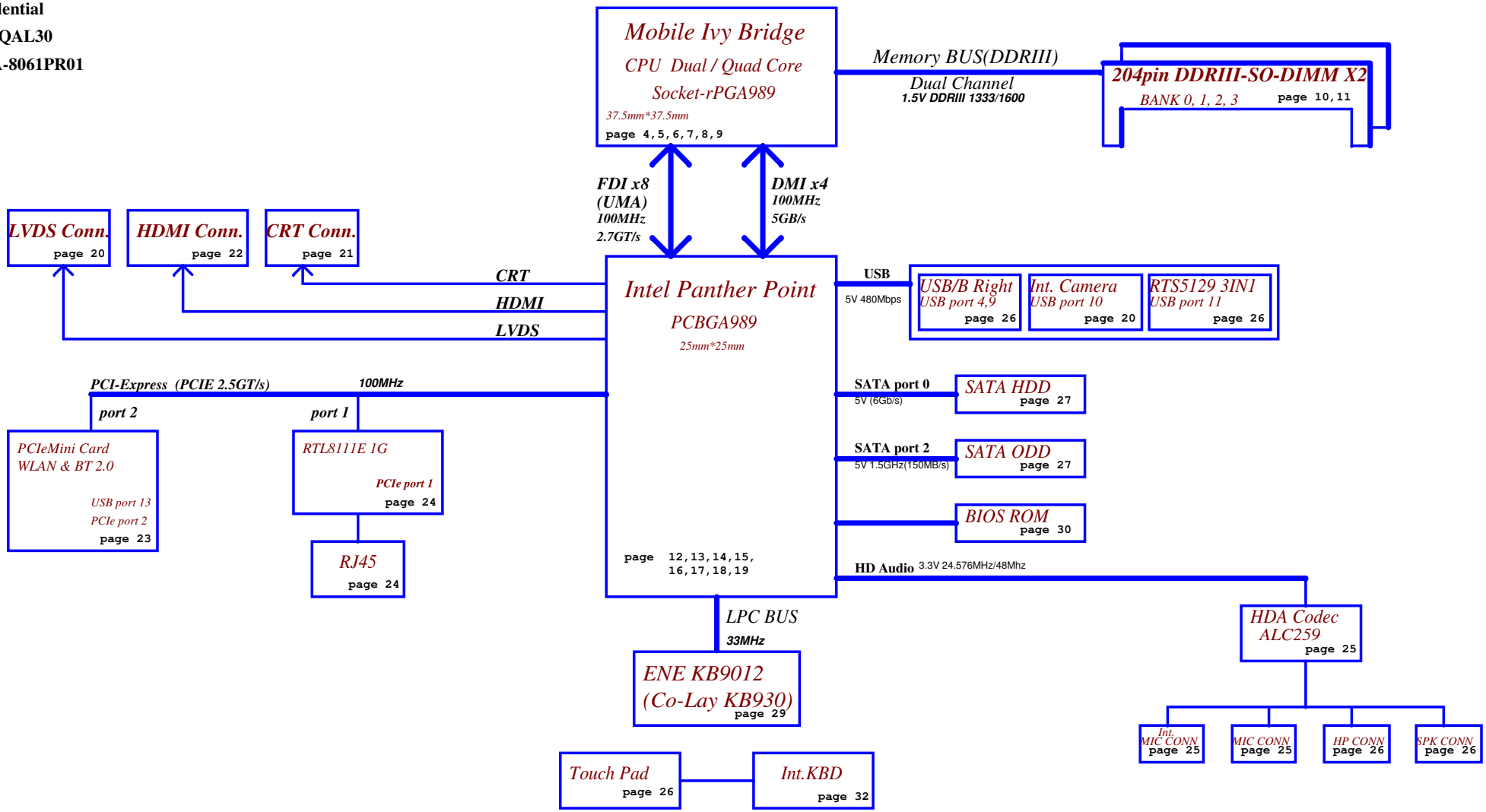
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Title: Cover Sheet

Size: Custom | Document Number: QAL30 LA-8061P MB | Rev: 0.1

Date: Friday, January 13, 2012 | Sheet 1 of 46

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Model Name : QAL30
File Name : LA-8061PR01



USB/B page 26	RTC CKT. page 12
Power/B page 31	DC/DC Interface CKT. page 34
Fan Control page 31	Power Circuit DC/DC page 35~44

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Title	Block Diagrams		
Size	Document Number		Rev
	QAL30 LA-8061P MB		0.1
Date: Wednesday, December 21, 2011	Sheet 2 of 46		

Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.168V	0.250 V	0.362 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	QAL30
1	
2	
3	
4	
5	
6	
7	

	USB PORT#	DESTINATION
PCH	0	USB2/3 (Left Hand dise front)
	1	USB2/3 (Left Hand dise back)
	2	None
	3	None
	4	USB2 (Right Hand side front)
	5	None
	6	None
	7	None
	8	None
	9	USB2 (Left Hand side back)
	10	CAMERA
	11	Card Reader
	12	None
	13	BT Comb

SMBUS Control Table

	SOURCE	MINI1	BATT 0001 011x b	SODIMM 1001 000x b	SODIMM 1001 010x b	PCH		
EC_SMB_CK1 EC_SMB_DA1	KB930 KB9012	X	V	X	X	X		
EC_SMB_CK2 EC_SMB_DA2	KB930 KB9012	X	X	X	X	V		
PCH_SMBCLK PCH_SMBDATA	PCH	V	X	V	V			
PCH_SML1CLK PCH_SML1DATA	PCH	X	X	X	X			

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	TPM
PCI3	None
PCI4	None

OPTIMUS: XDP@/D@

	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
CLK	CLKOUT_PCIE0	LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_A	VGA		
	CLKOUT_PEG_B	None		

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	LAN
Lane 2	WLAN
Lane 3	None
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

Symbol Note :

: means Digital Ground

: means Analog Ground

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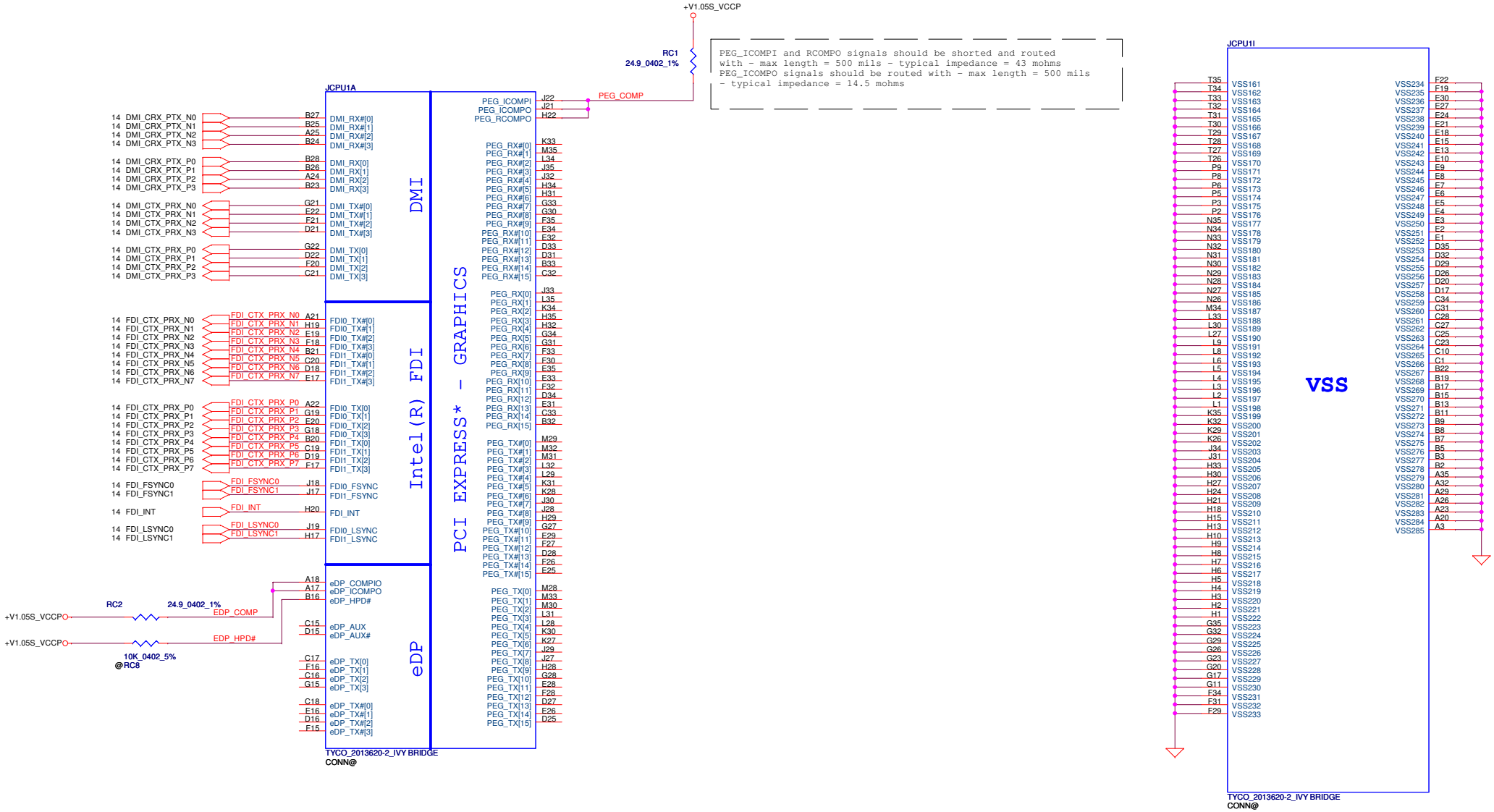
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Title: Notes List

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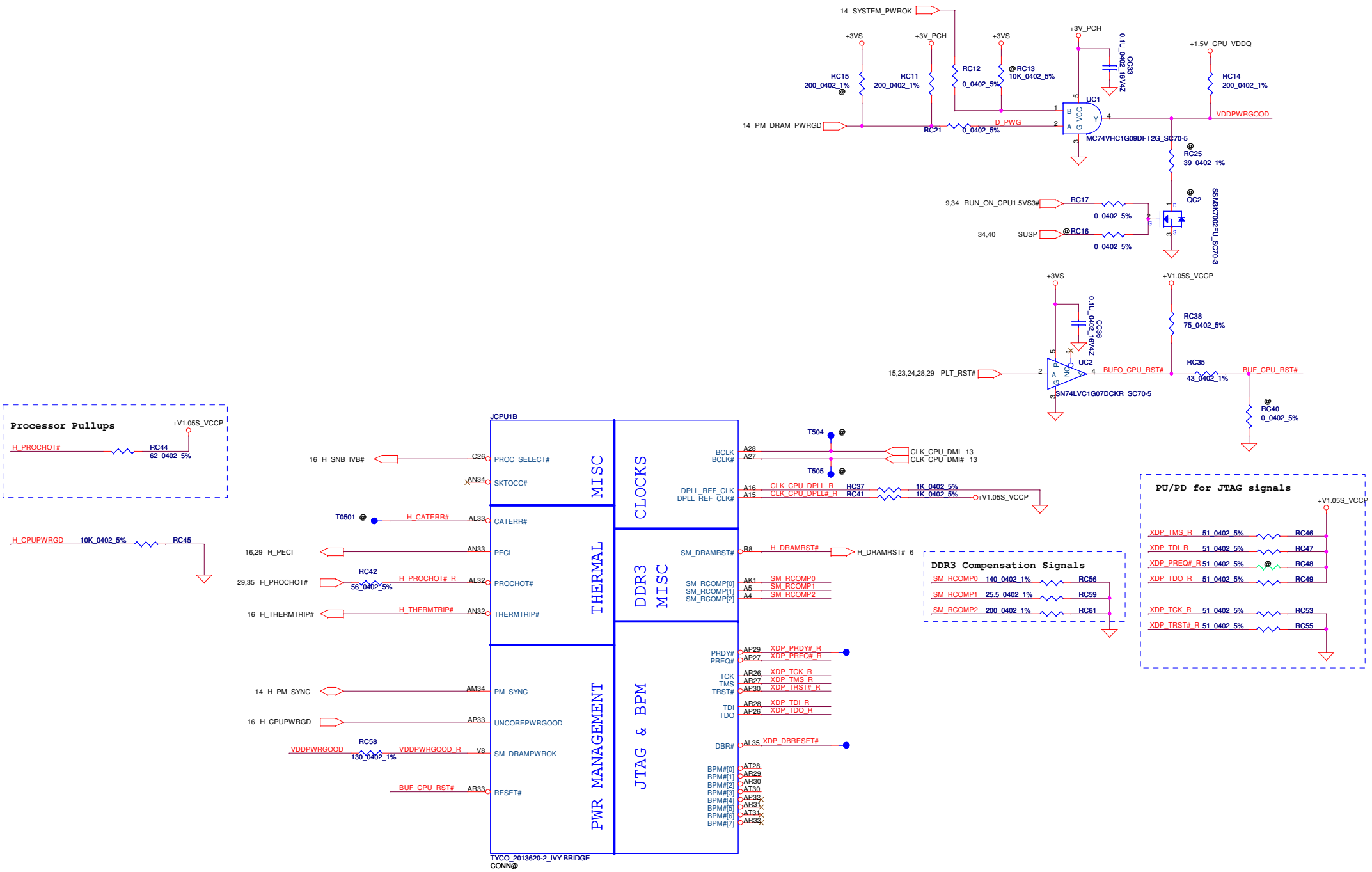
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Title: PROCESSOR(1/6) DMI,FDI,PEG

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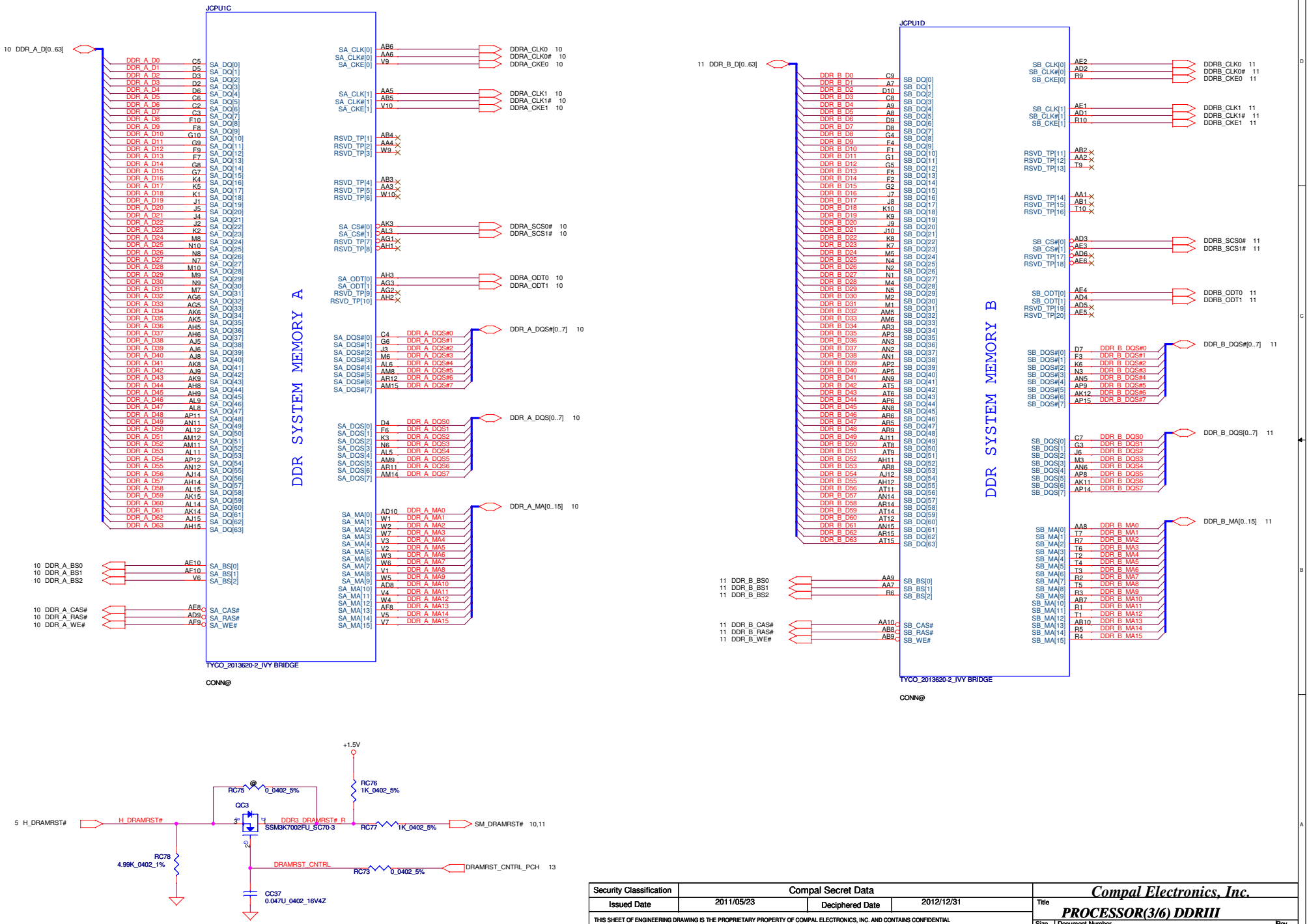
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Compal Electronics, Inc.

Title: PROCESSOR(2/6) PM,XDP,CLK

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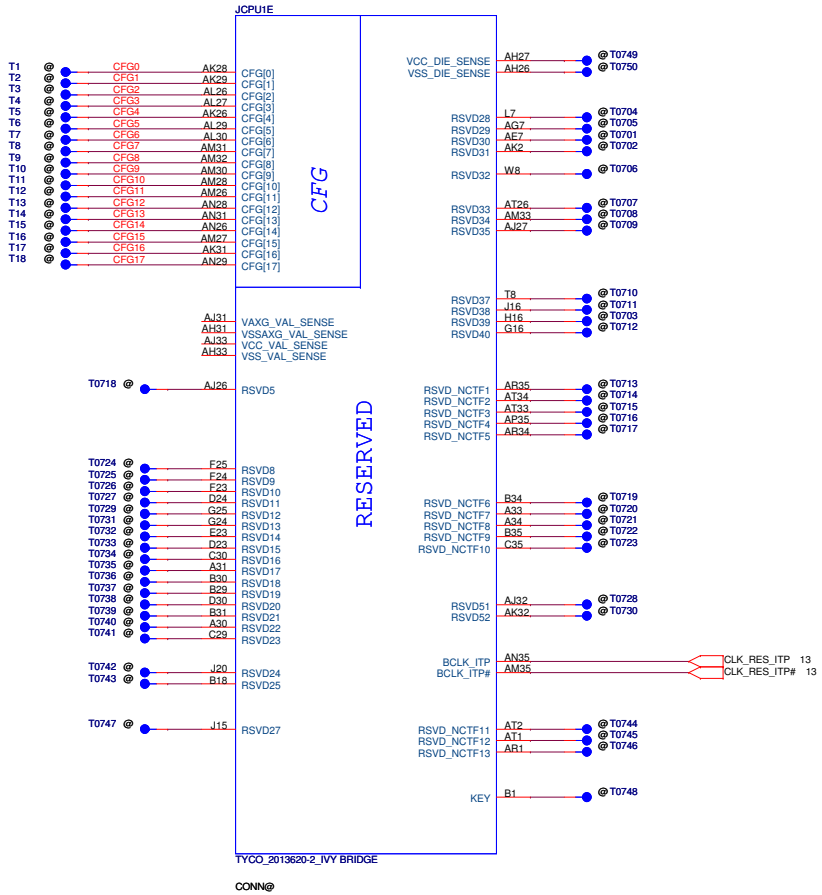
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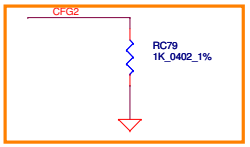
Title: PROCESSOR(3/6) DDRIII

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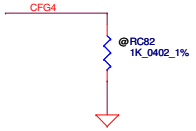
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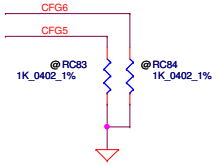
CFG Straps for Processor



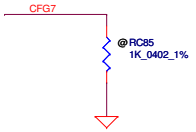
PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following RESETB de assertion 0: PEG Wait for BIOS for training

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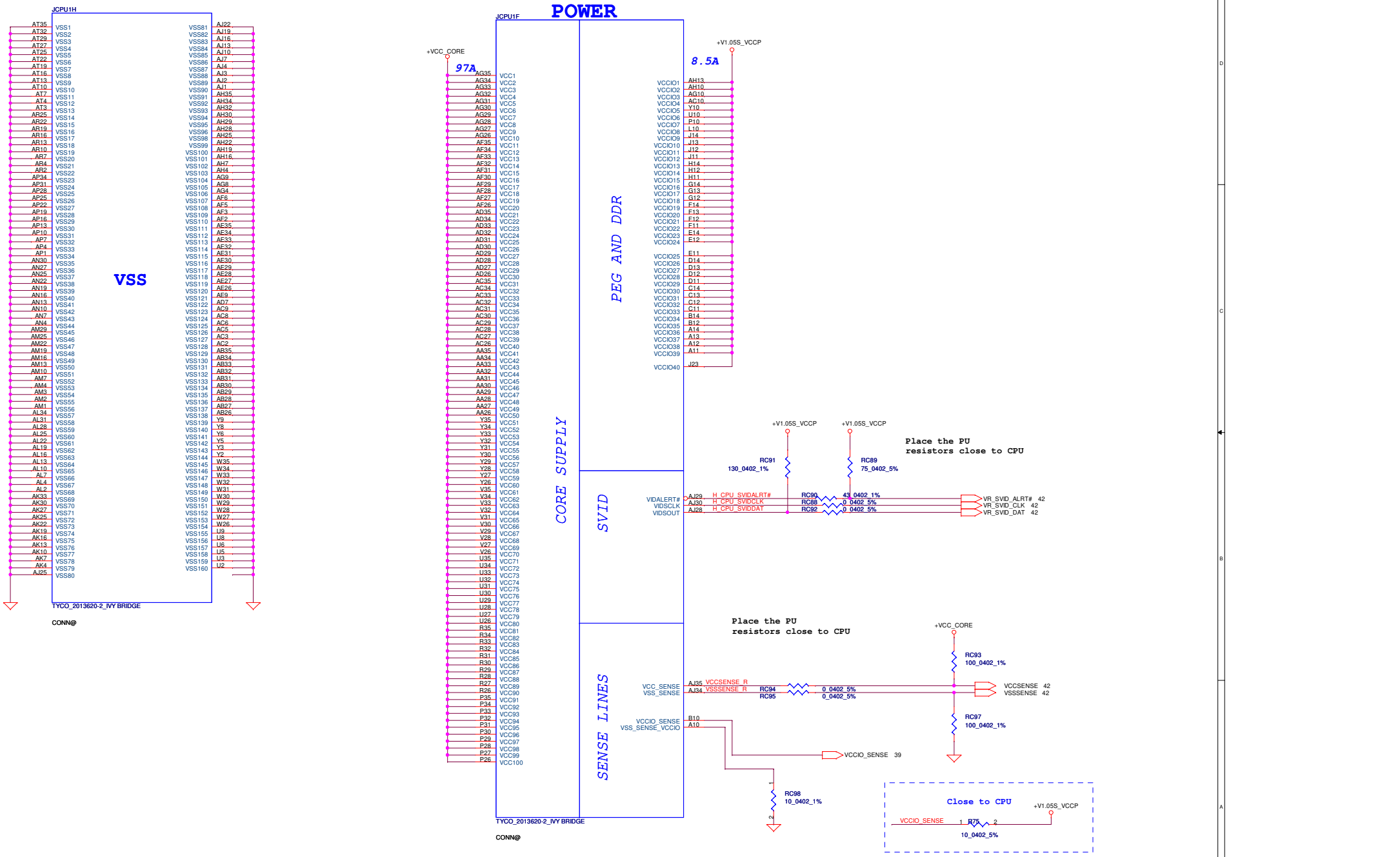
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Title: PROCESSOR(4/6) RSVD,CFG

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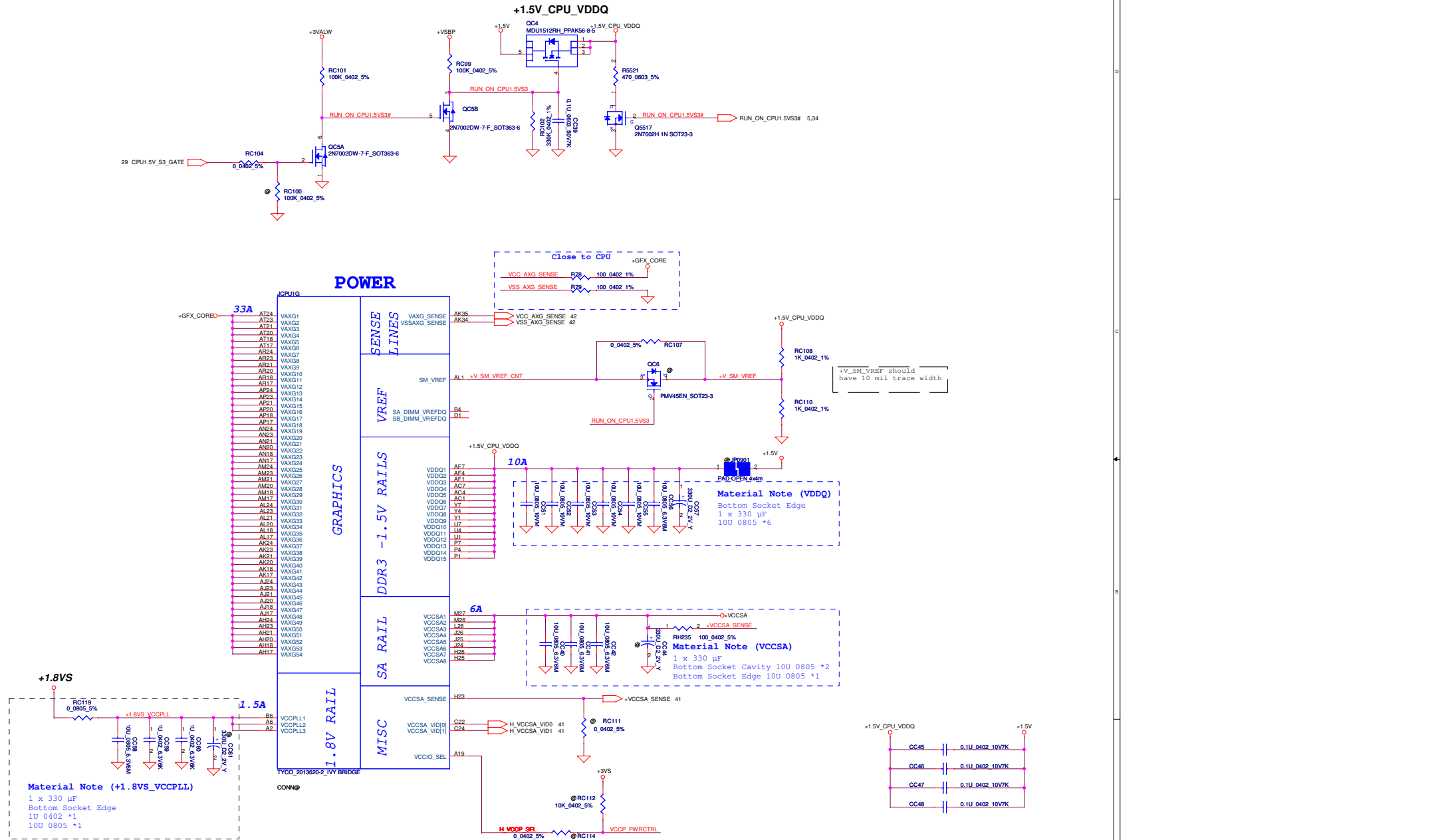
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Title: PROCESSOR(5/6) PWR,BYPASS

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IVY Bridge drives VCCIO_SEL low
VCCP_PWRCTRL:0

Sandy Bridge is NC for A19
VCCP_PWRCTRL:1

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Title: PROCESSOR(6/6) PWR,VSS

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DDR3 SO-DIMM A

3A@1.5V

@JDDRL

TYCO_2-2013022-2

6 DDR_A_D[0..63]
6 DDR_A_DQS[0..7]
6 DDR_A_DQS#[0..7]
6 DDR_A_MA[0..15]

SM_DRAMRST# 6,11

6 DDRA_CKE0
6 DDR_A_BS2
6 DDRA_CLK0
6 DDRA_CLK0#
6 DDR_A_BS0
6 DDR_A_WE#
6 DDR_A_CAS#
6 DDRA_SCS1#

DDRA_CKE1 6
DDRA_CLK1 6
DDRA_CLK1# 6
DDR_A_BS1 6
DDR_A_RAS# 6
DDRA_SCS0# 6
DDRA_ODT0 6
DDRA_ODT1 6

PCH_SMBDATA 11,13,23
PCH_SMBCLK 11,13,23

Layout Note:
Place near JDDRL

Layout Note: Place these 4 Caps near
Command and Control signals of JDDRL

Layout Note:
Place near JDDRL.203,204

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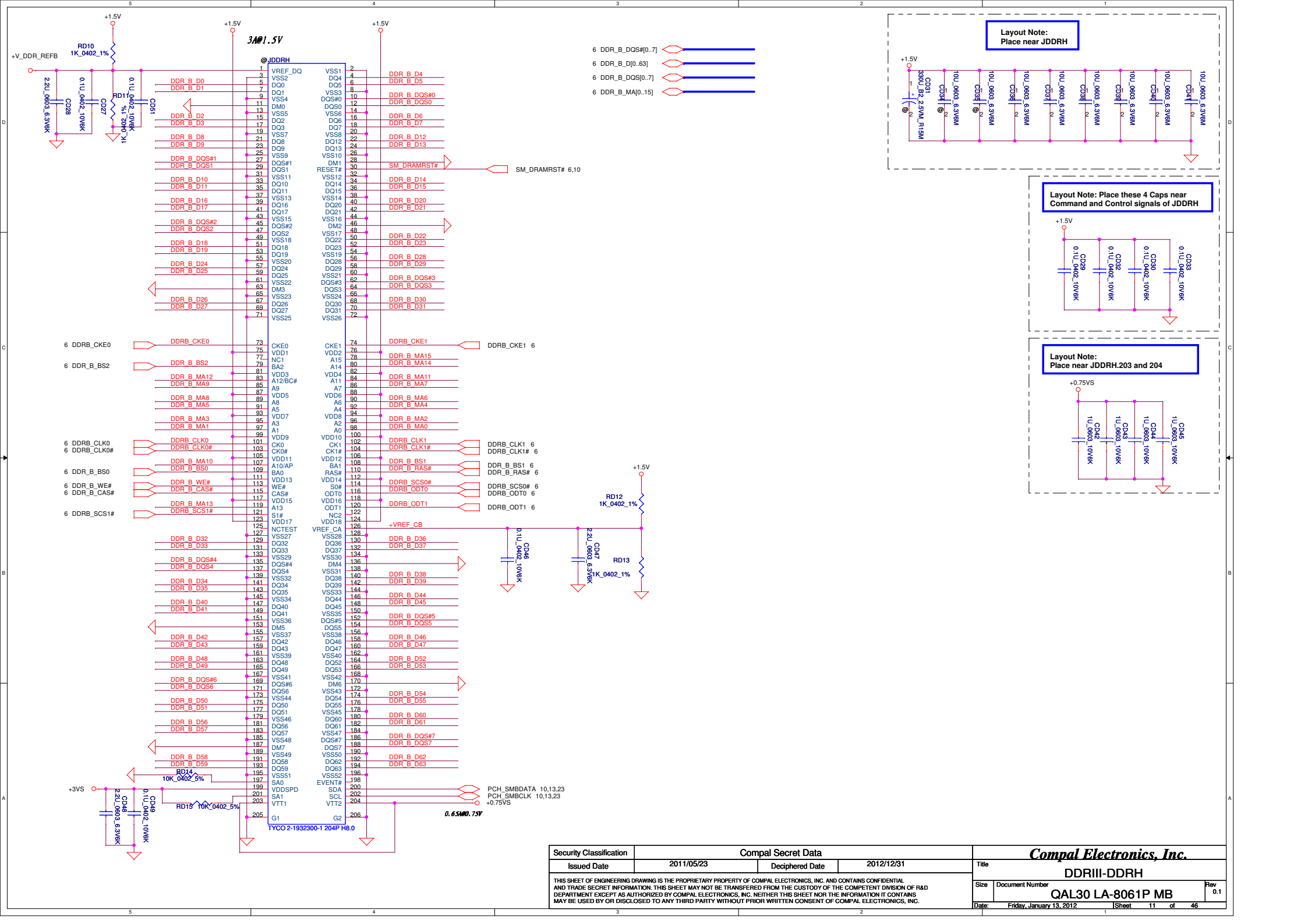
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Title: DDRIII-DDRL

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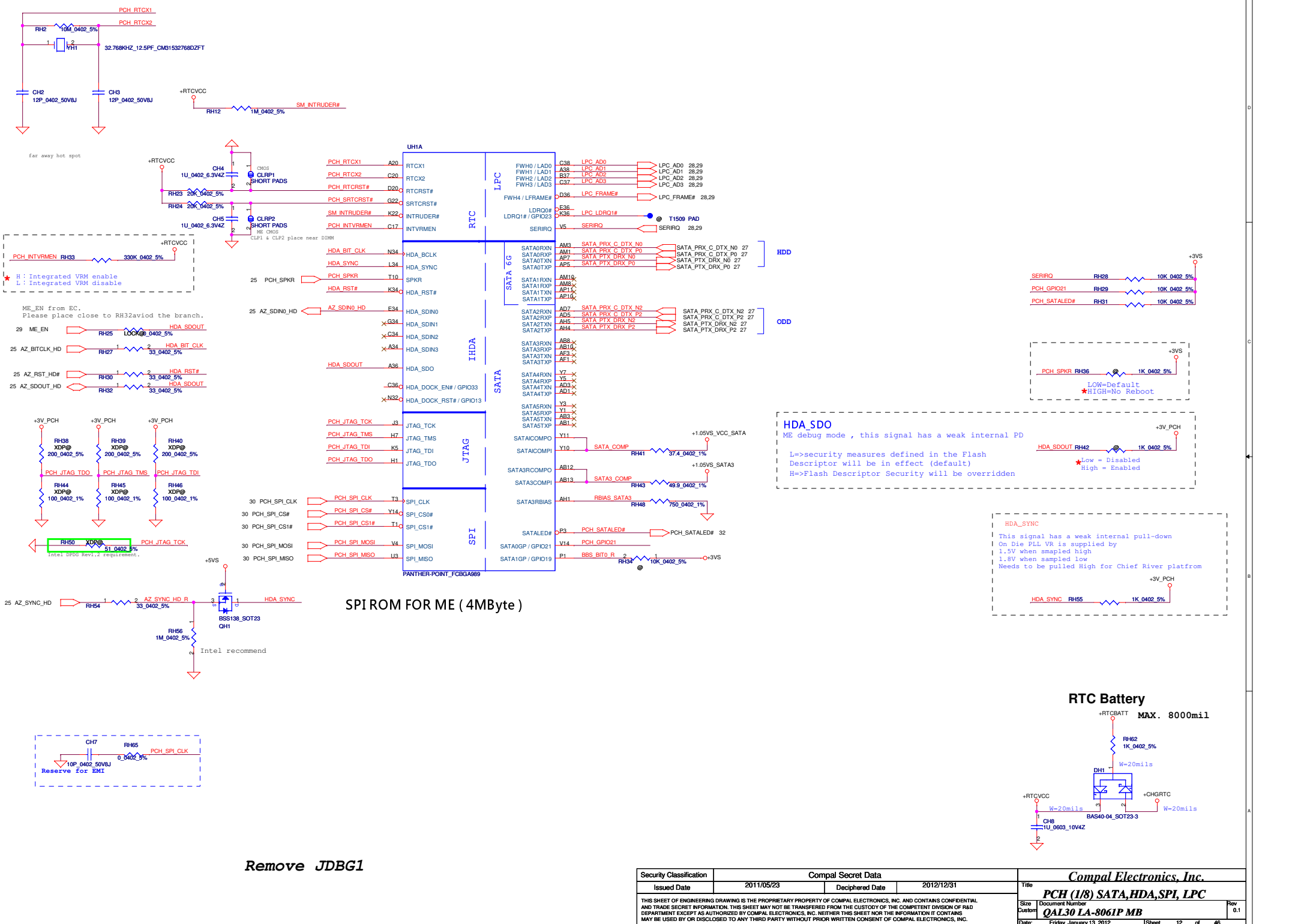
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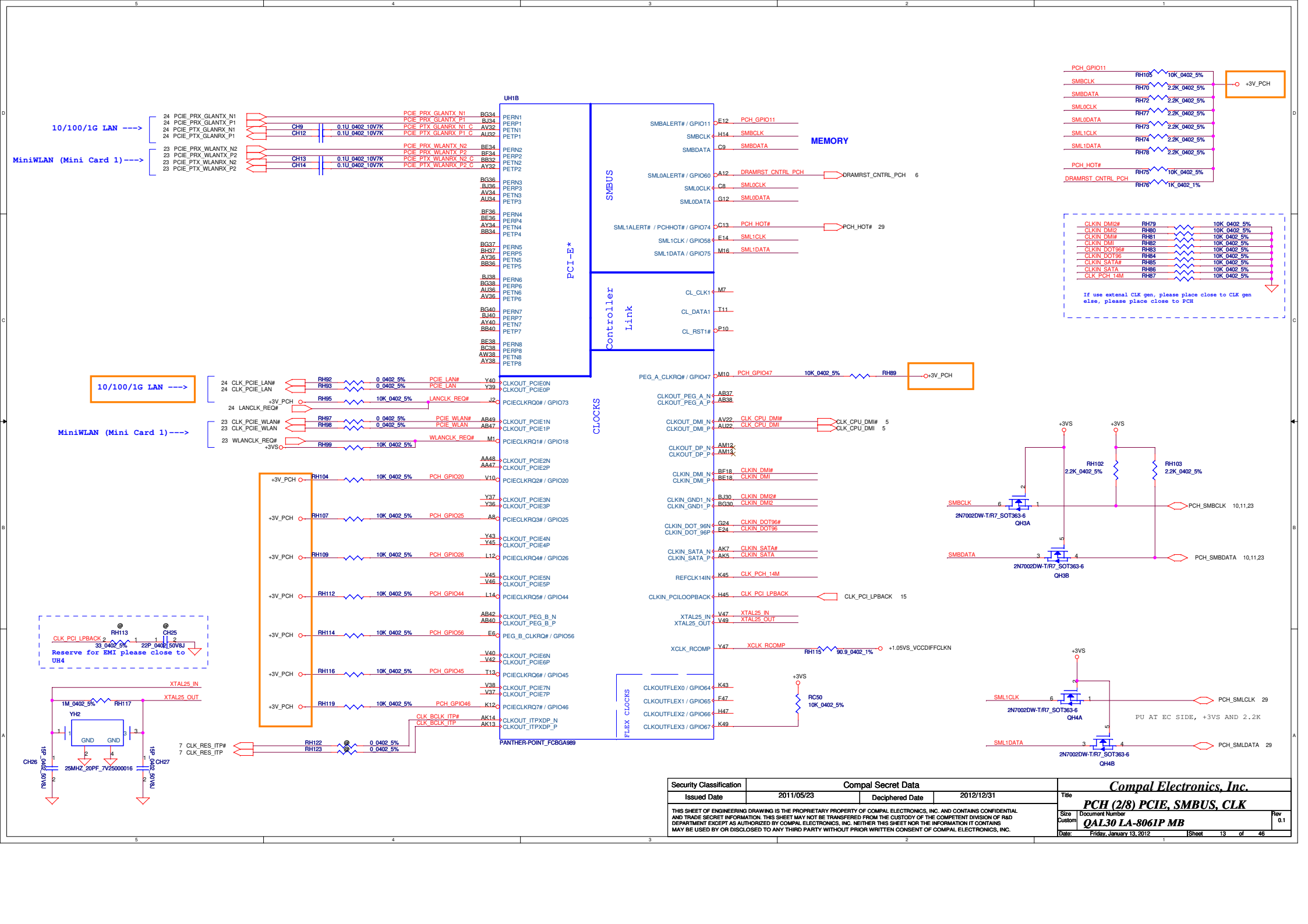
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Title: PCH (1/8) SATA,HDA,SPI, LPC

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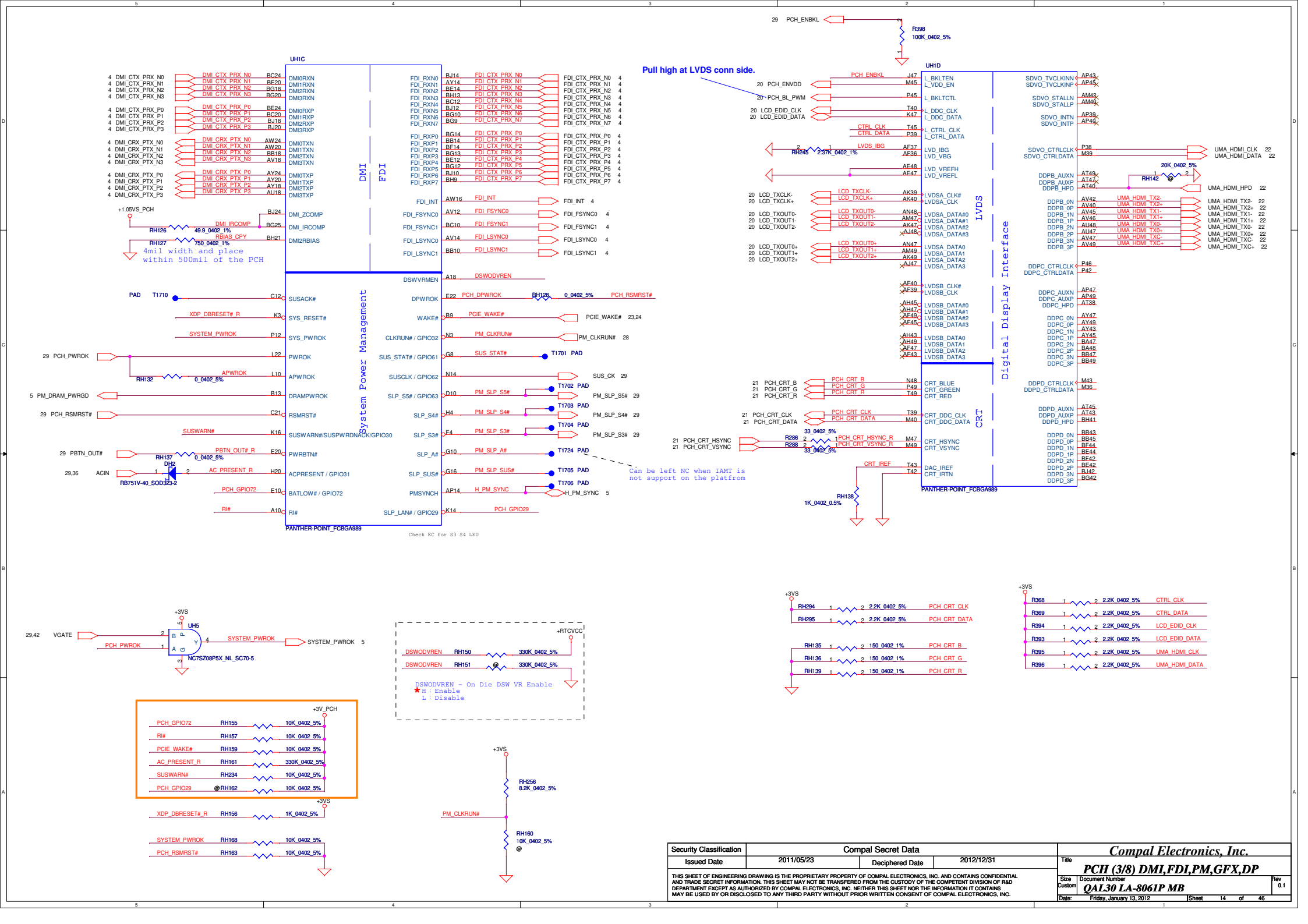
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Title: PCH (2/8) PCIE, SMBUS, CLK

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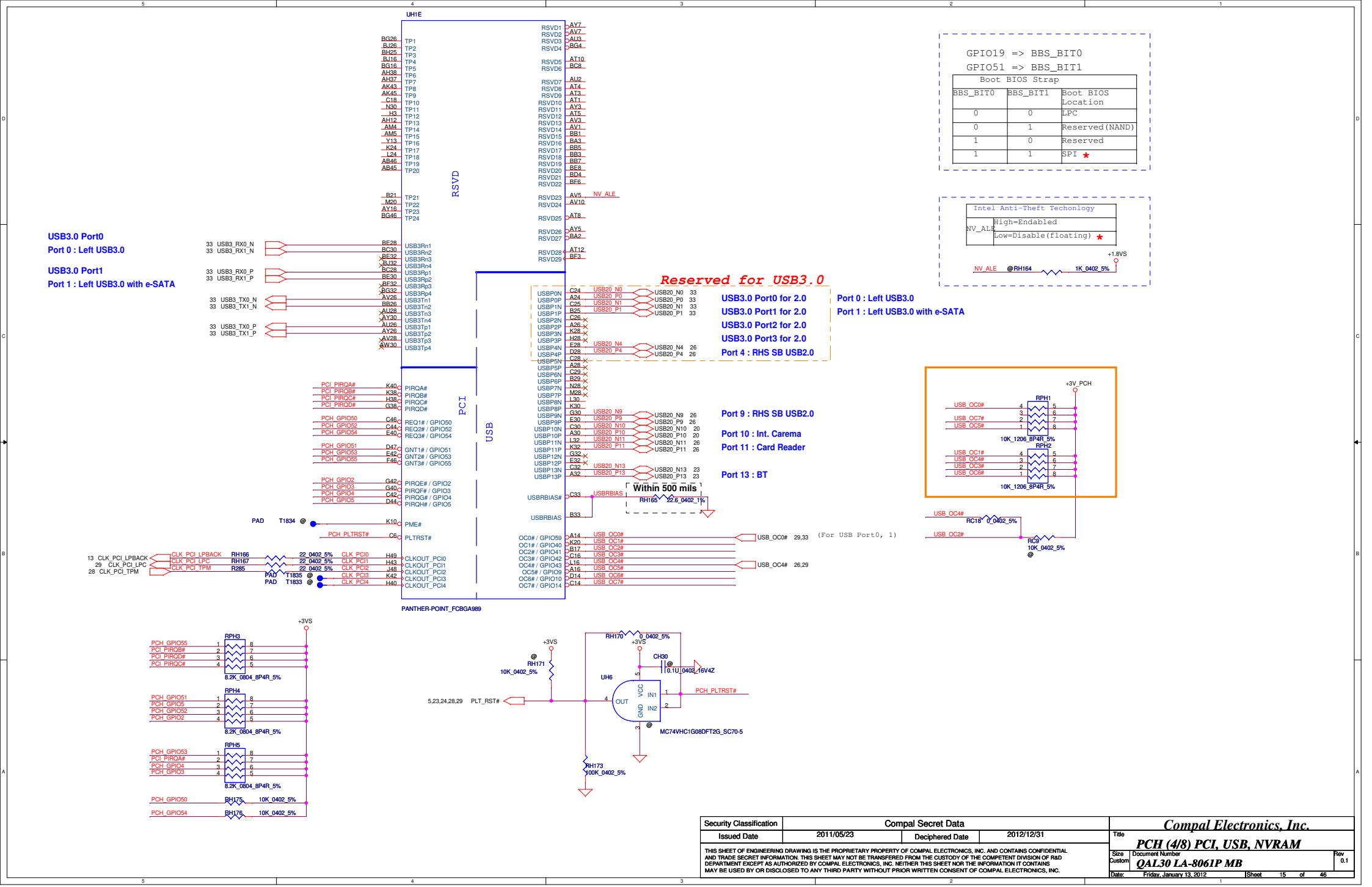
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Title: PCH (3/8) DMI,FDI,PM,GFX,DP

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Title: PCH (4/8) PCI, USB, NVRAM

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PID :	210	
QAL30	000	(UMA)
QAL31	001	(DIS)
QAL50	010	(UMA)
QAL51	011	(DIS)
KSPD Q0000	1XX	

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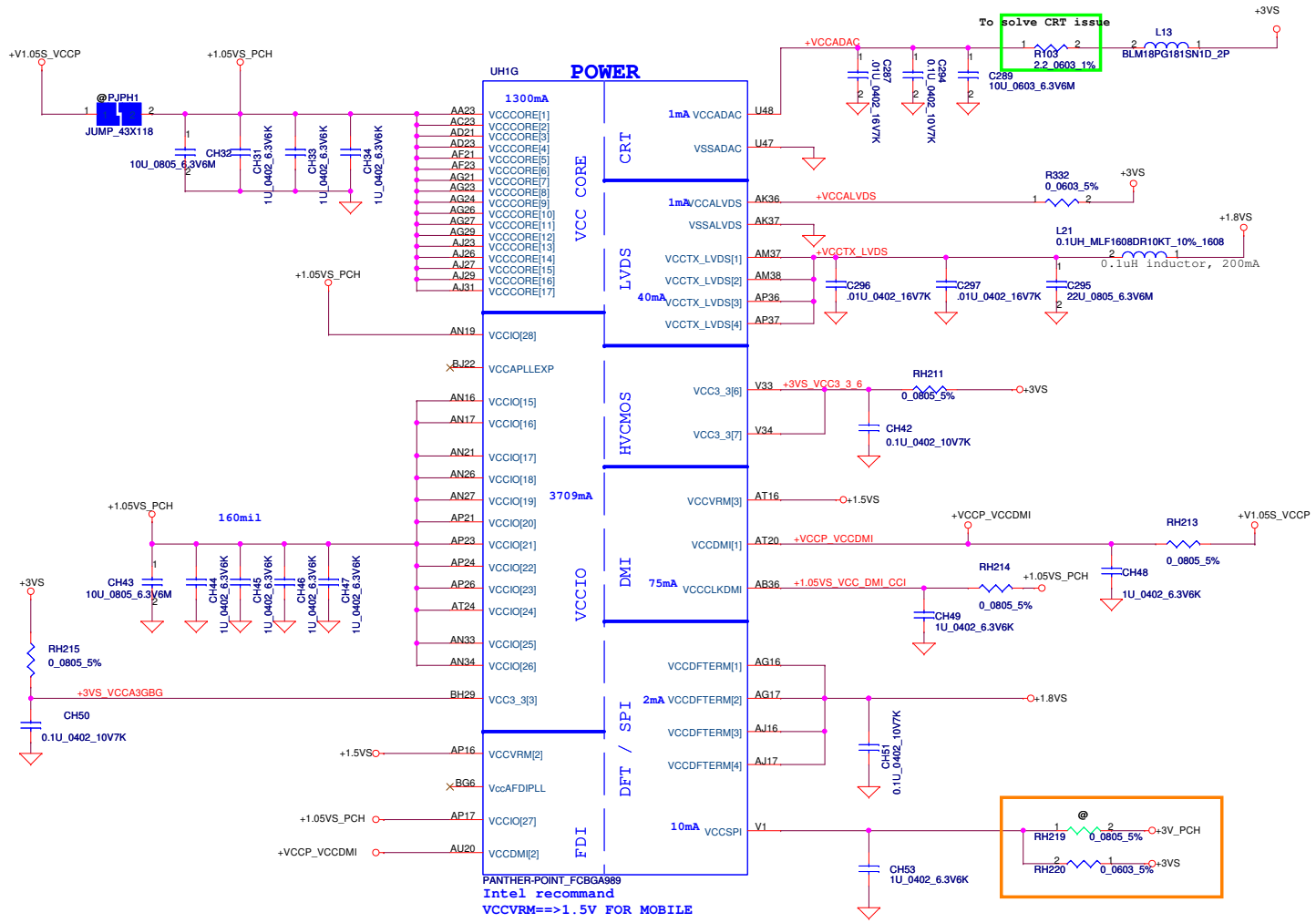
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Title: PCH (5/8) GPIO, CPU, MISC

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PCH Power Rail Table
Refer to CPU EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Security Classification	Compal Secret Data		
Issued Date	2011/05/23	Deciphered Date	2012/12/31

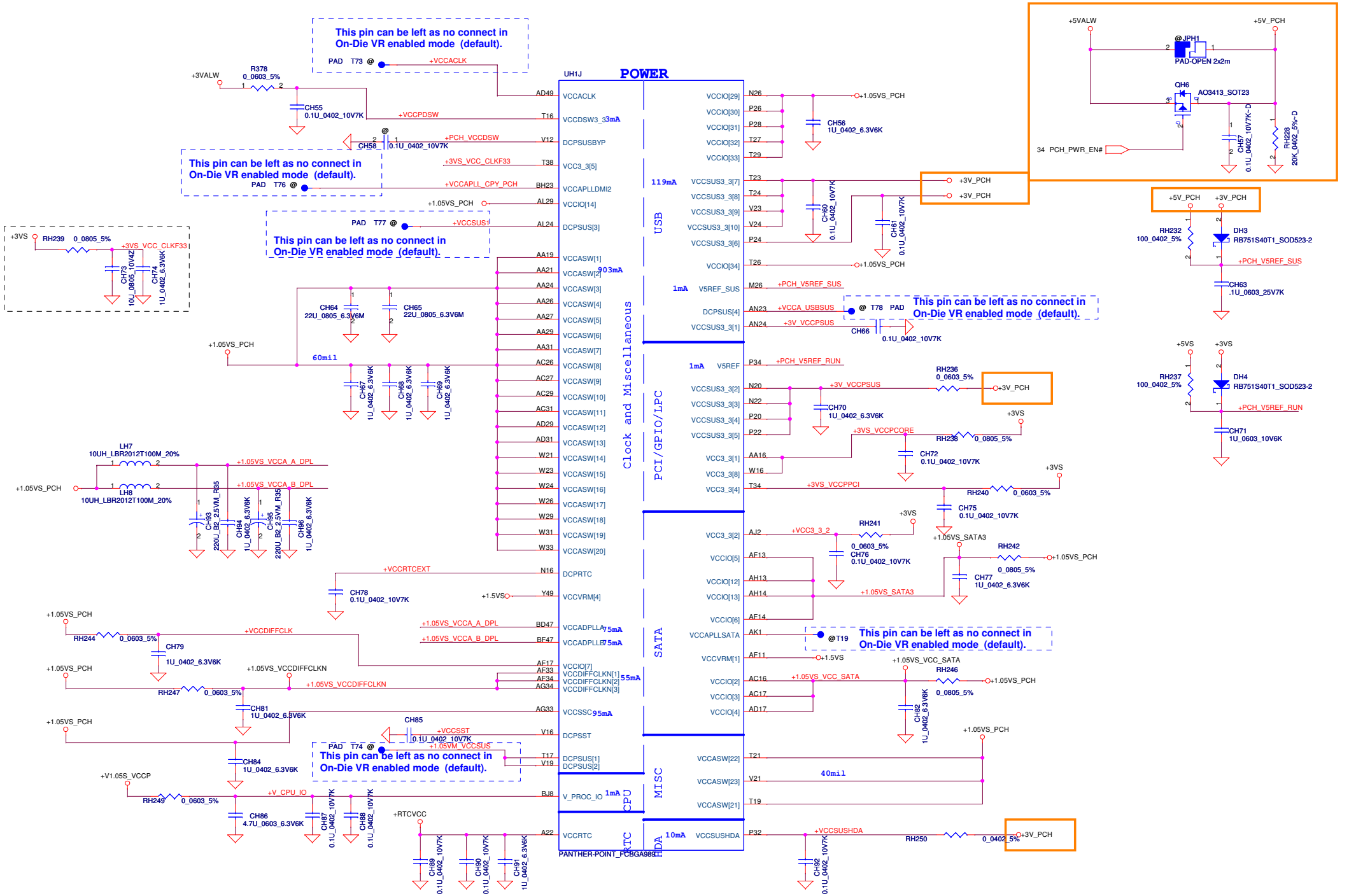
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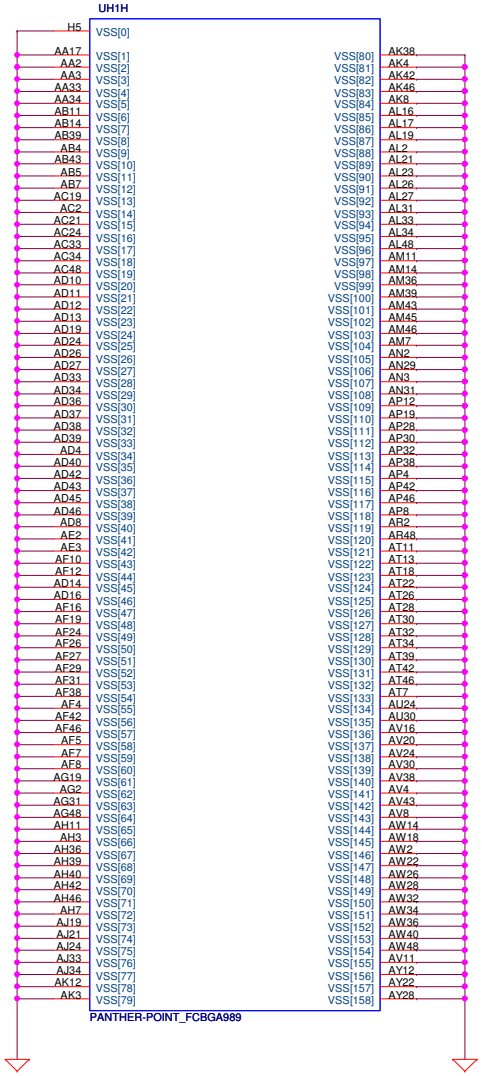
Compal Electronics, Inc.

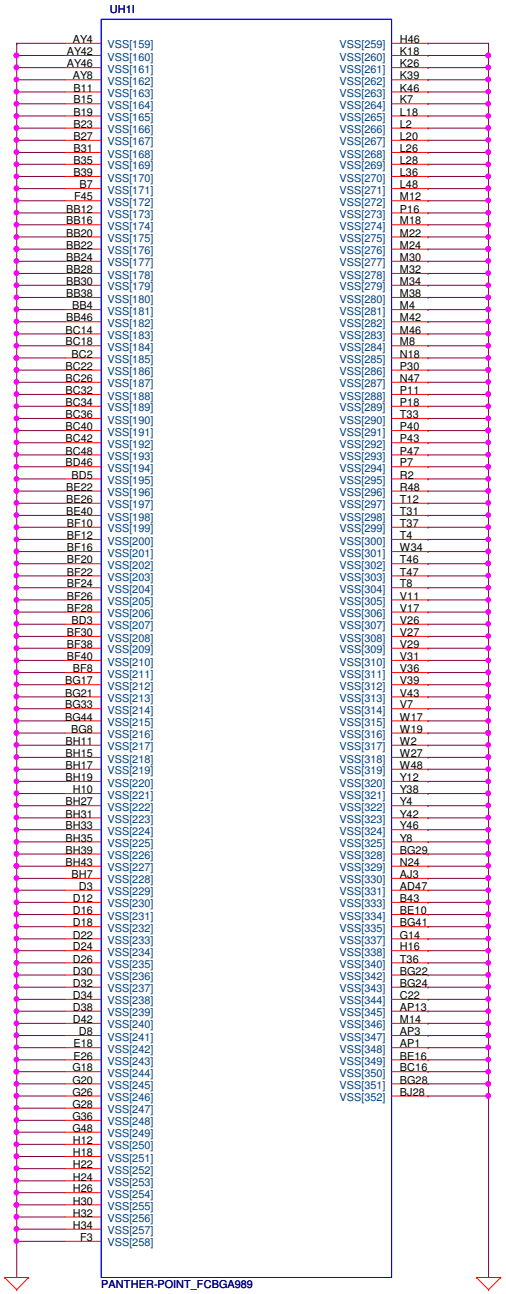
Title: PCH (6/8) PWR

Size: Custom | Document Number: QAL30 LA-8061P MB | Rev: 0.1

Date: Friday, November 11, 2011 | Sheet 17 of 46


POWER
UH1J
PANTHER-POINT_FCBGA989
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
MISC
RTC
HDA
This pin can be left as no connect in On-Die VR enabled mode (default).
+VCCACLK
+VCCPDSW
+PCH_VCCDSW
+3VS_VCC_CLKF33
+VCCAPLL_CPY_PCH
+VCCSUS1
+1.05VS_PCH
+3V_PCH
+5V_PCH
+5VALW
+3VS
+1.5VS
+V_CPU_IO
+RTCVCC
+V1.05S_VCCP
+VCCRTCEXT
+1.05VS_VCCA_A_DPL
+1.05VS_VCCA_B_DPL
+1.05VS_VCCDIFFCLKN
+VCCSST
+1.05VM_VCCSUS
+3V_VCCPSUS
+PCH_V5REF_SUS
+PCH_V5REF_RUN
+VCCA_USBSUS
+3VS_VCCPCORE
+3VS_VCCPPCI
+VCC3_3_2
+1.05VS_SATA3
+1.05VS_VCC_SATA
+VCCSUSHDA
PCH_PWR_EN#
PAD-OPEN 2x2m
AO3413_SOT23
Security Classification
Compal Secret Data
Issued Date
2011/05/23
Deciphered Date
2012/12/31
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Compal Electronics, Inc.
Title
PCH (7/8) PWR
Size
Custom
Document Number
QAL30 LA-8061P MB
Rev
0.1
Date:
Friday, January 13, 2012
Sheet
18
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46





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Issued Date	2011/05/23	Deciphered Date	2012/12/31

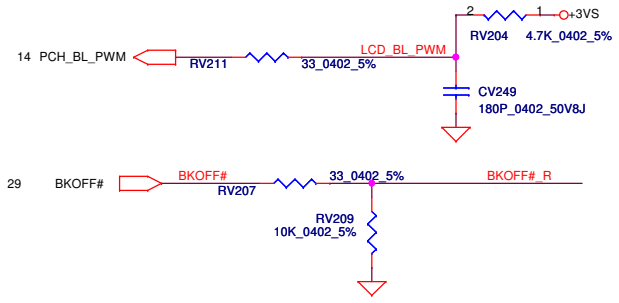
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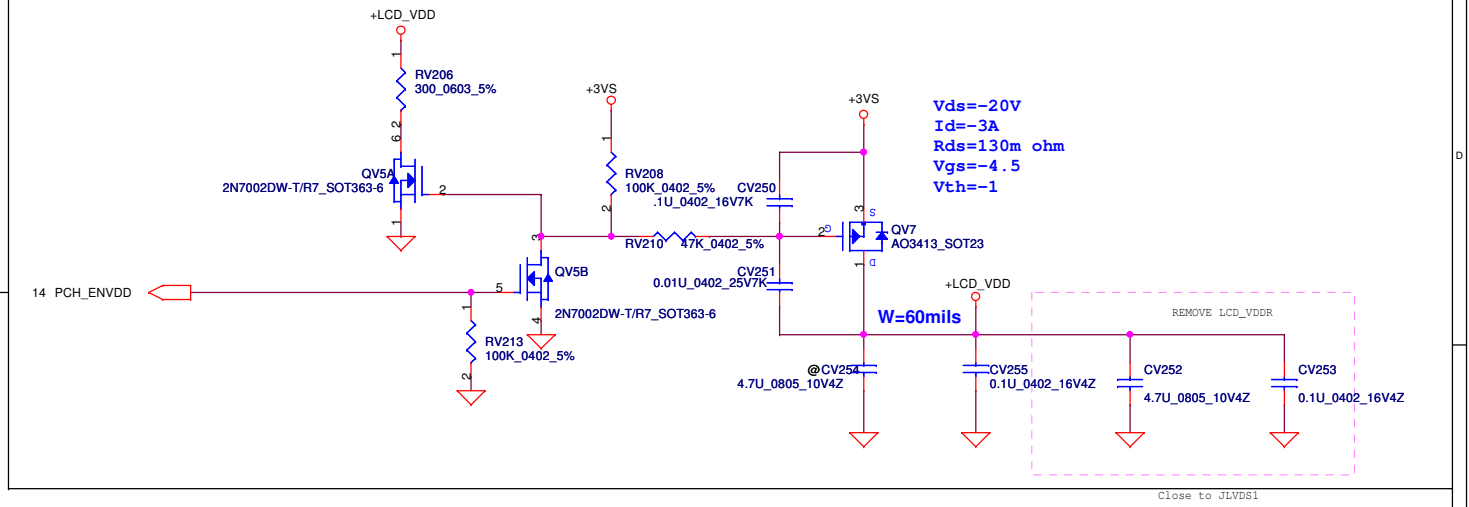
Compal Electronics, Inc.

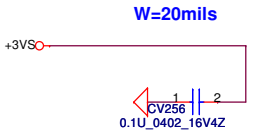
Title: PCH (8/8) VSS

Size	Document Number	Rev
Custom	QAL30 LA-8061P MB	0.1

Date: Friday, October 28, 2011 Sheet 19 of 46



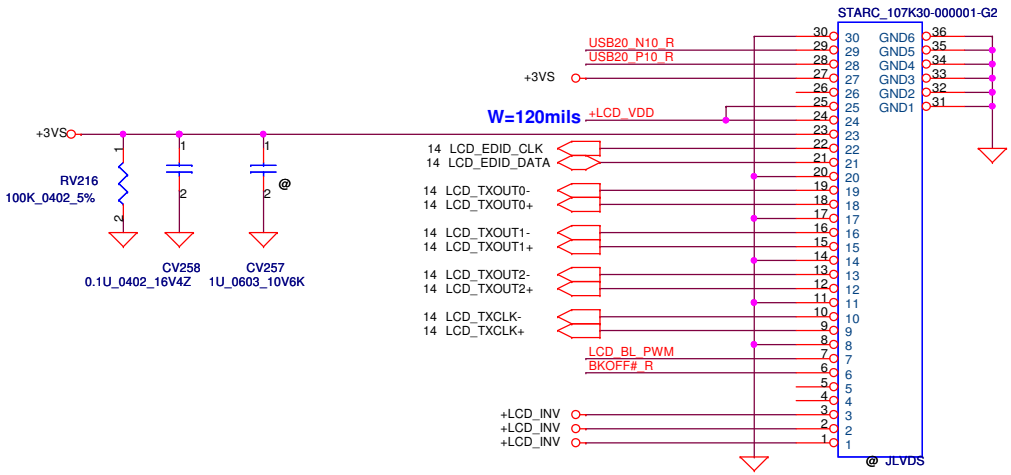


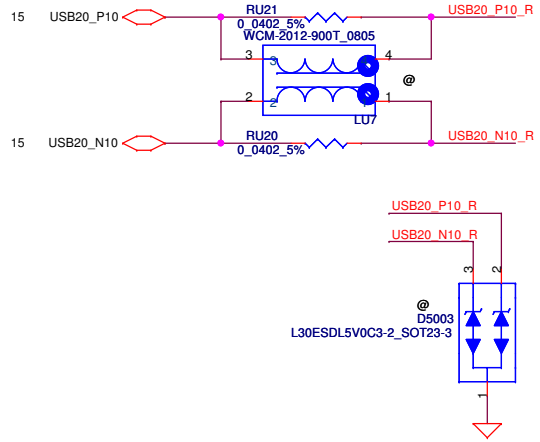


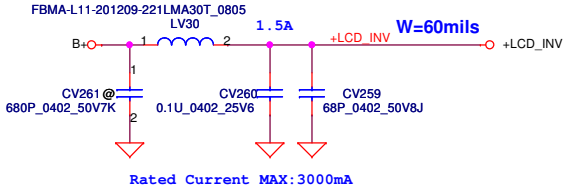
Close to JLVDS

Change to 30 pin.

Single Channel LVDS







LCD/PANEL BD. Conn.

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Issued Date	2011/05/23	Deciphered Date	2012/12/31

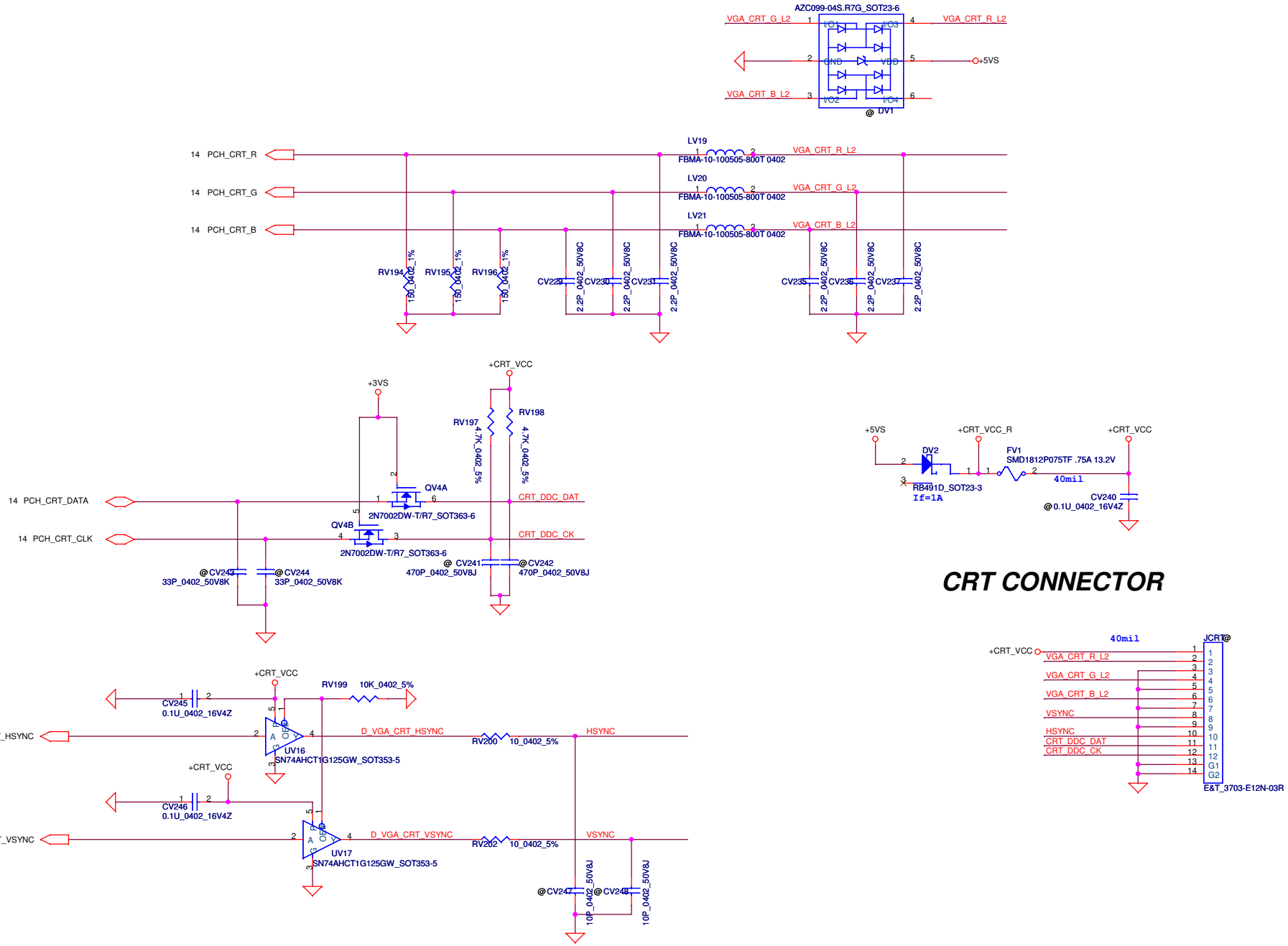
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Title: LVDS

Size	Document Number	Rev
	QAL30 LA-8061P MB	0.1

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Issued Date	2011/05/23	Deciphered Date	2012/12/31

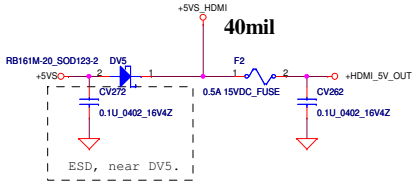
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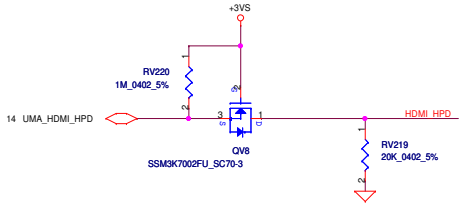
Compal Electronics, Inc.

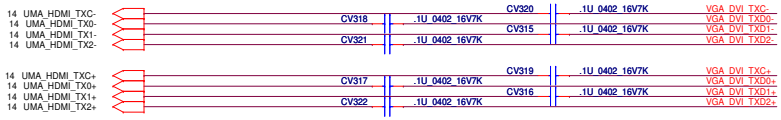
Title: CRT

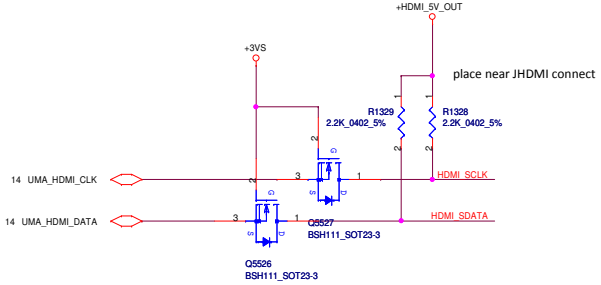
Size | Document Number: QAL30 LA-8061P MB | Rev: 0.1

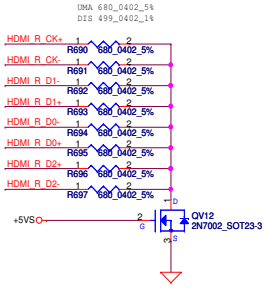
Date: Friday, January 13, 2012 | Sheet 21 of 46

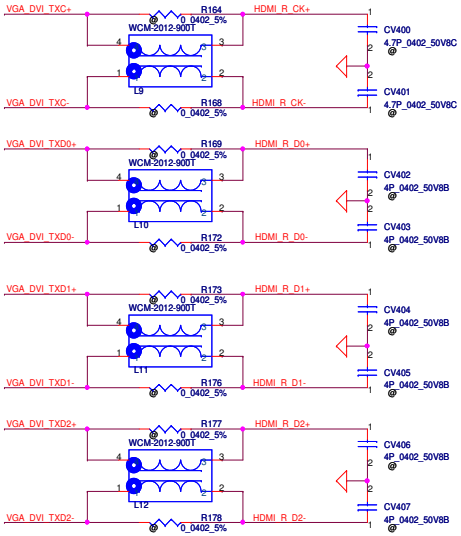


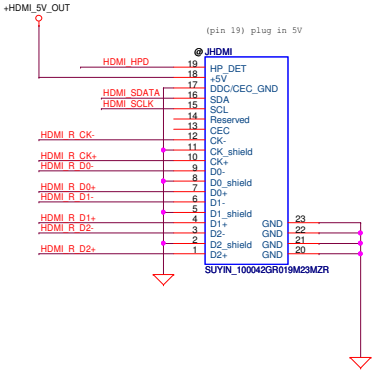












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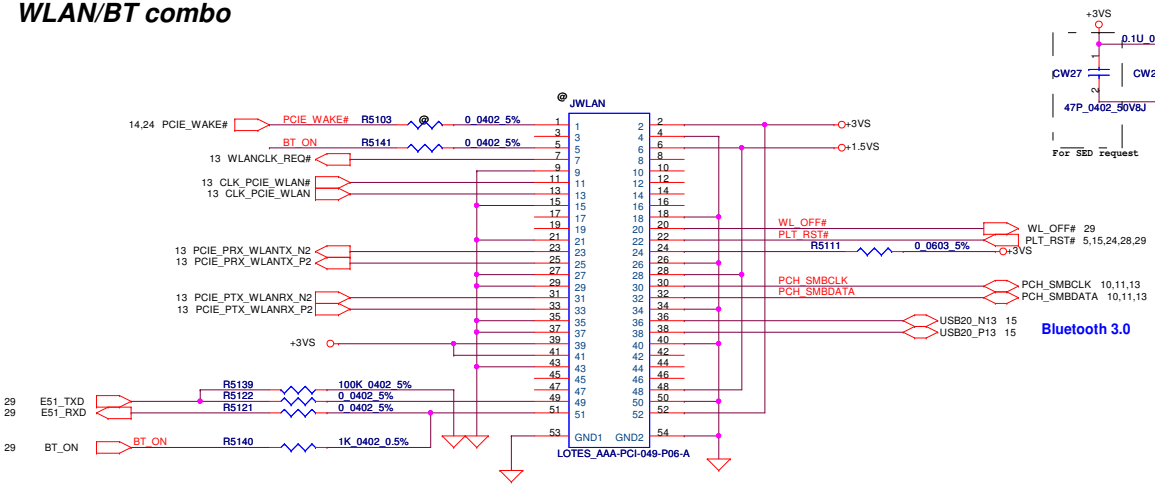
Compal Electronics, Inc.

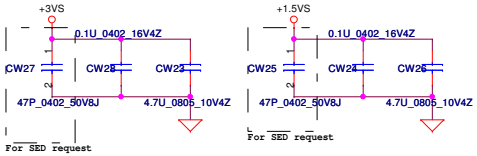
Title: HDMI Connector

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WLAN/BT combo





Security Classification	Compal Secret Data		
Issued Date	2011/05/23	Deciphered Date	2012/12/31

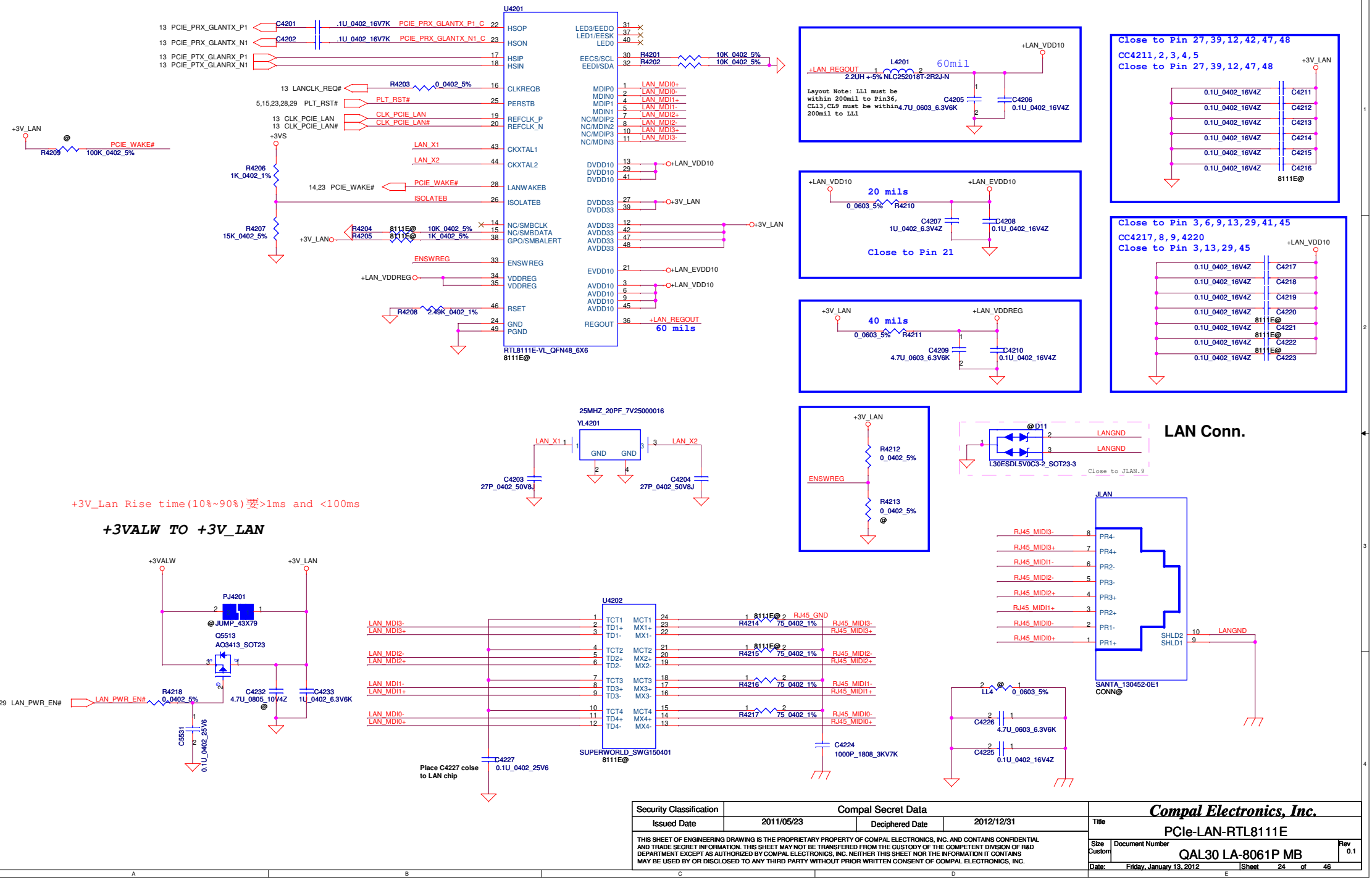
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Compal Electronics, Inc.

Title: WLAN

Size: Custom | Document Number: QAL30 LA-8061P MB | Rev: 0.1

Date: Friday, January 13, 2012 | Sheet 23 of 46



Security Classification	Compal Secret Data		
Issued Date	2011/05/23	Deciphered Date	2012/12/31

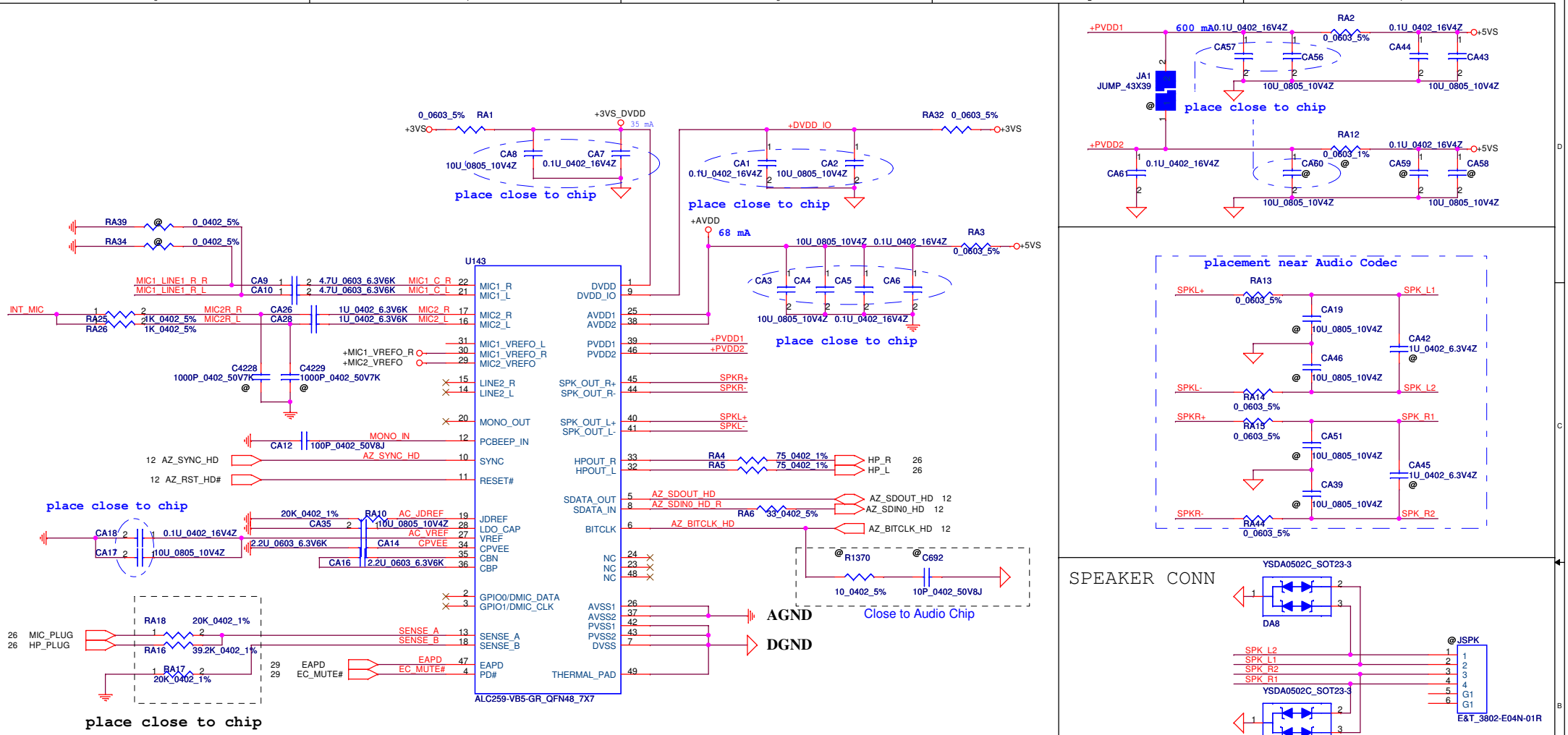
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Compal Electronics, Inc.

Title: PCIe-LAN-RTL8111E

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Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
SENSE B	20K	PORT-F (PIN 16, 17)	Int. MIC

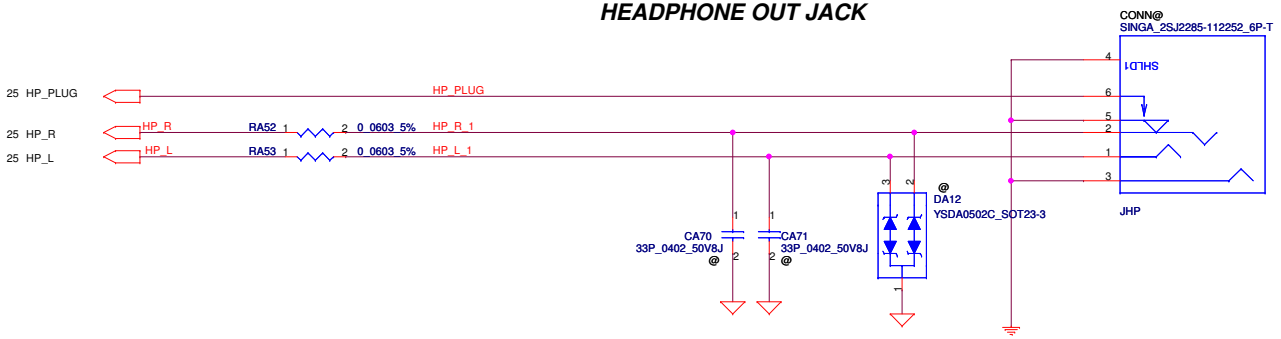
Security Classification	Compal Secret Data		
Issued Date	2011/05/23	Deciphered Date	2012/12/31

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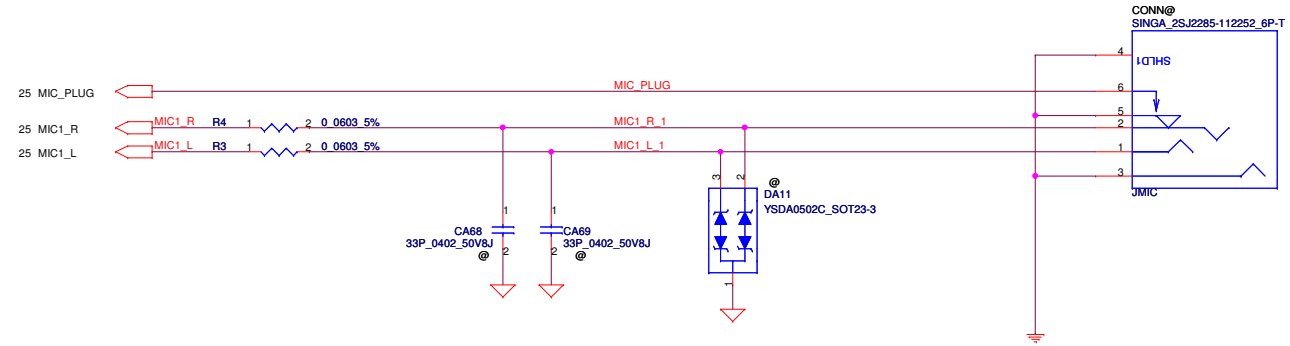
Compal Electronics, Inc.

Title	HD CODEC ALC259		
Size	Document Number		Rev
	QAL30 LA-8061P MB		0.1
Date:	Friday, January 13, 2012	Sheet	25 of 46

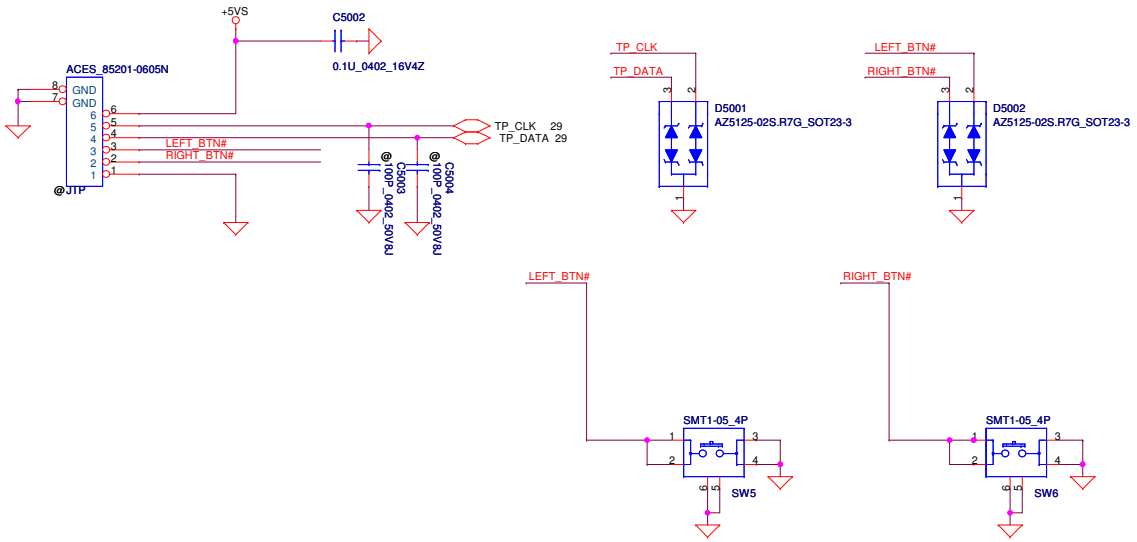
HEADPHONE OUT JACK



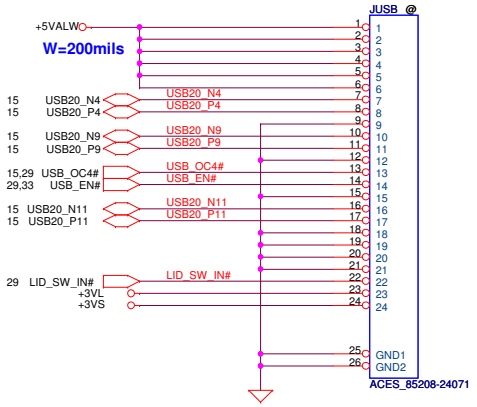
MICROPHONE IN JACK



Touch/B Connector

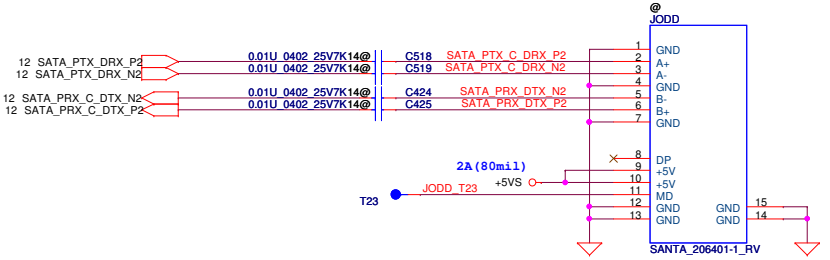


USB + LID SB

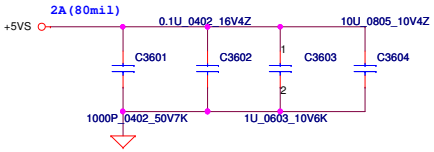


Title	AUDIO CONN/TP/FUNB	
Size	Document Number QAL30 LA-8061P MB	Rev 0.1
Date: Friday, January 13, 2012	Sheet 26 of 46	

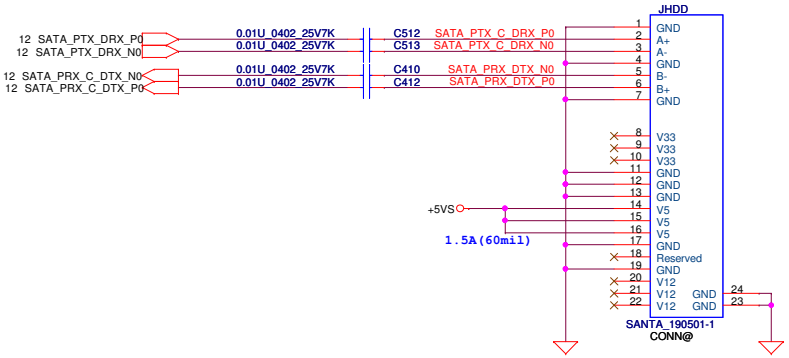
SATA ODD Conn.

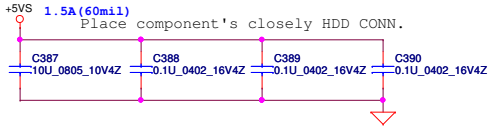


Placea caps. near ODD CONN.



SATA HDD Conn.





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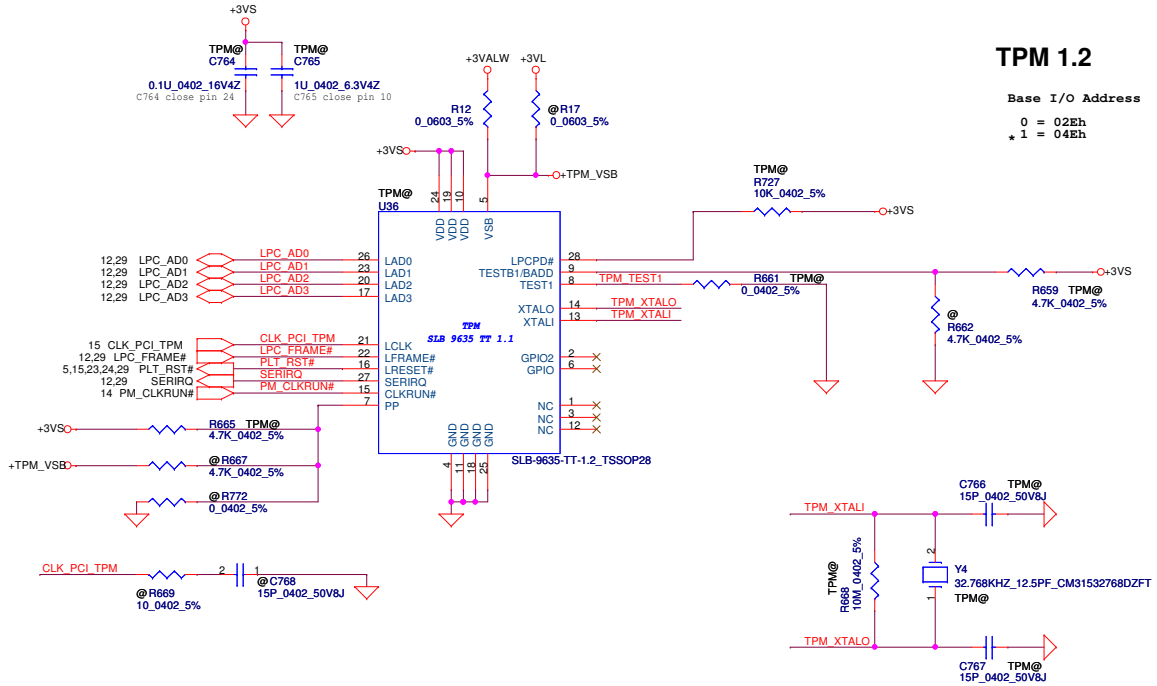
Compal Electronics, Inc.

Title: SATA HDD / ODD

Size: Custom | Document Number: QAL30 LA-8061P MB | Rev: 0.1

Date: Friday, January 13, 2012 | Sheet 27 of 46

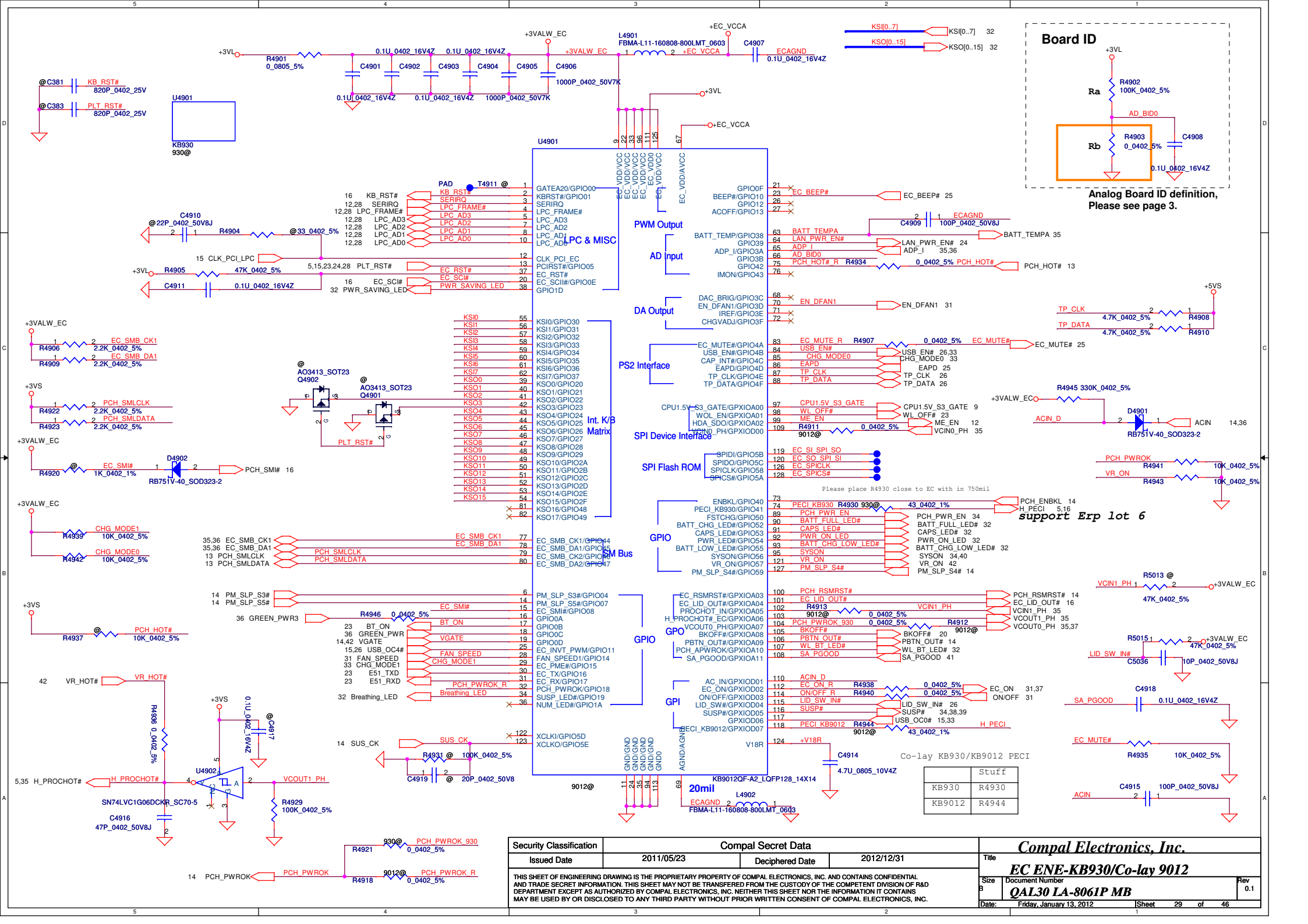
SPI ROM For Basic ME ROM size
(w/o Braidwood & system BIOS):
4MByte



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Title	TPM		
Size	Document Number	QAL30 LA-8061P MB	Rev 0.1
Date: Friday, January 13, 2012	Sheet 28 of 46		

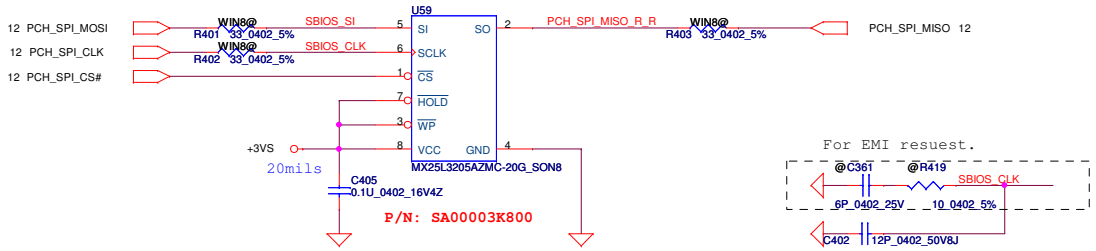

Board ID
Ra
Rb
R4902 100K_0402_5%
R4903 0_0402_5%
C4908 0.1U_0402_16V4Z
AD_BID0
Analog Board ID definition, Please see page 3.
U4901
KB930
930@
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
SM Bus
GPIO
GPO
GPI
PAD T4911 @
KB_RST#
SERIRQ
LPC_FRAME#
LPC_AD3
LPC_AD2
LPC_AD1
LPC_AD0
CLK_PCI_EC
PCIRST#/GPIO05
EC_RST#
EC_SCI#/GPIO0E
GPIO1D
PWR_SAVING_LED
BATT_TEMP/GPIO38
GPIO39
ADP_I/GPIO3A
GPIO3B
GPIO42
IMON/GPIO43
DAC_BRIG/GPIO3C
EN_DFAN1/GPIO3D
IREF/GPIO3E
CHGVADJ/GPIO3F
EC_MUTE#/GPIO4A
USB_EN#/GPIO4B
CAP_INT#/GPIO4C
EAPD/GPIO4D
TP_CLK/GPIO4E
TP_DATA/GPIO4F
CPU1.5V_S3_GATE/GPXIOA00
WOL_EN/GPXIOA01
HDA_SDO/GPXIOA02
VCIN0_PH/GPXIOD00
SPIDI/GPIO5B
SPIDO/GPIO5C
SPICLK/GPIO58
SPICS#/GPIO5A
ENBKL/GPIO40
PECI_KB930/GPIO41
FSTCHG/GPIO50
BATT_CHG_LED#/GPIO52
CAPS_LED#/GPIO53
PWR_LED#/GPIO54
BATT_LOW_LED#/GPIO55
SYSON/GPIO56
VR_ON/GPIO57
PM_SLP_S4#/GPIO59
KSI0/GPIO30
KSI1/GPIO31
KSI2/GPIO32
KSI3/GPIO33
KSI4/GPIO34
KSI5/GPIO35
KSI6/GPIO36
KSI7/GPIO37
KSO0/GPIO20
KSO1/GPIO21
KSO2/GPIO22
KSO3/GPIO23
KSO4/GPIO24
KSO5/GPIO25
KSO6/GPIO26
KSO7/GPIO27
KSO8/GPIO28
KSO9/GPIO29
KSO10/GPIO2A
KSO11/GPIO2B
KSO12/GPIO2C
KSO13/GPIO2D
KSO14/GPIO2E
KSO15/GPIO2F
KSO16/GPIO48
KSO17/GPIO49
EC_SMB_CK1/GPIO44
EC_SMB_DA1/GPIO45
EC_SMB_CK2/GPIO46
EC_SMB_DA2/GPIO47
PM_SLP_S3#/GPIO04
PM_SLP_S5#/GPIO07
EC_SMI#/GPIO08
GPIO0A
GPIO0B
GPIO0C
GPIO0D
EC_INVT_PWM/GPIO11
FAN_SPEED1/GPIO14
EC_PME#/GPIO15
EC_TX/GPIO16
EC_RX/GPIO17
PCH_PWROK/GPIO18
SUSP_LED#/GPIO19
NUM_LED#/GPIO1A
XCLKI/GPIO5D
XCLKO/GPIO5E
EC_RSMRST#/GPIOA03
EC_LID_OUT#/GPIOA04
PROCHOT_IN/GPIOA05
H_PROCHOT#_EC/GPIOA06
VCOUT0_PH/GPIOA07
BKOFF#/GPIOA08
PBTN_OUT#/GPIOA09
PCH_APWROK/GPIOA10
SA_PGOOD/GPIOA11
AC_IN/GPXIOD01
EC_ON/GPXIOD02
ON/OFF/GPXIOD03
LID_SW#/GPXIOD04
SUSP#/GPXIOD05
GPXIOD06
PECI_KB9012/GPXIOD07
V18R
KB9012QF-A2_LQFP128_14X14
20mil
L4902
FBMA-L11-160808-800LMT_0603
L4901
FBMA-L11-160808-800LMT_0603
Please place R4930 close to EC with in 750mil
support Erp lot 6
Co-lay KB930/KB9012 PECI
Stuff
KB930 R4930
KB9012 R4944
SN74LVC1G06DCKR_SC70-5
Security Classification
Compal Secret Data
Issued Date
2011/05/23
Deciphered Date
2012/12/31
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Compal Electronics, Inc.
Title
EC ENE-KB930/Co-lay 9012
Size B
Document Number
QAL30 LA-8061P MB
Rev 0.1
Date: Friday, January 13, 2012
Sheet 29 of 46

BIOS Bus switch

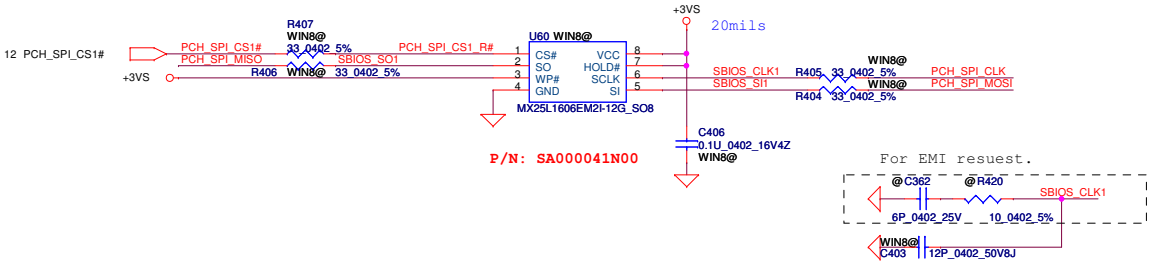
R401 0_0402_5% NOW8@
R402 0_0402_5% NOW8@
R403 0_0402_5% NOW8@

When use single ROM, use 0 ohm.

BIOS SPI Flash (4MByte*1)



BIOS SPI Flash (2MByte*1) For Win8



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Compal Electronics, Inc.

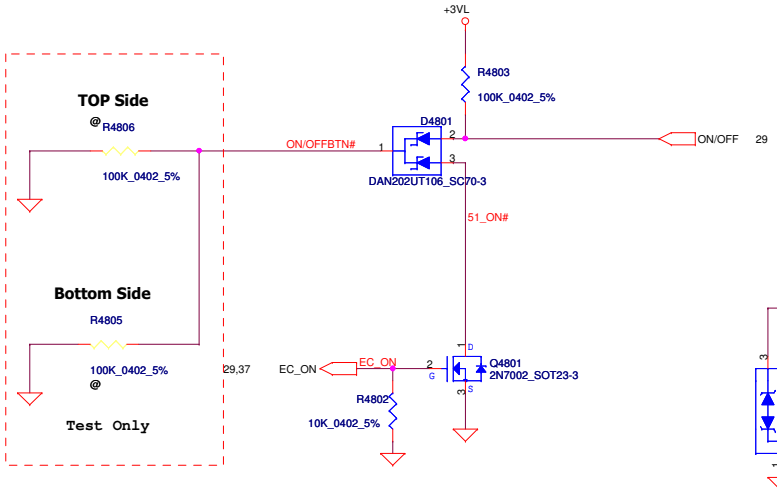
Title: SBIOS & EC ROM

Size | Document Number: QAL30 LA-8061P MB | Rev: 0.1

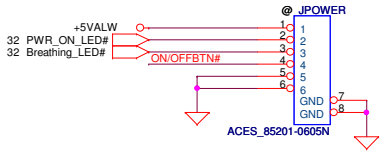
Date: Friday, January 13, 2012 | Sheet 30 of 46

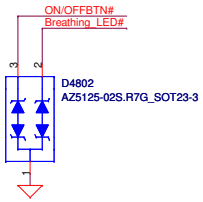
Power Button

ON/OFF switch



To POWER/B

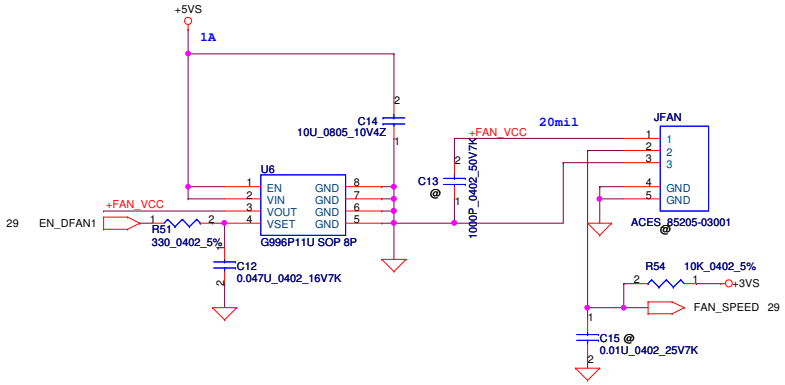




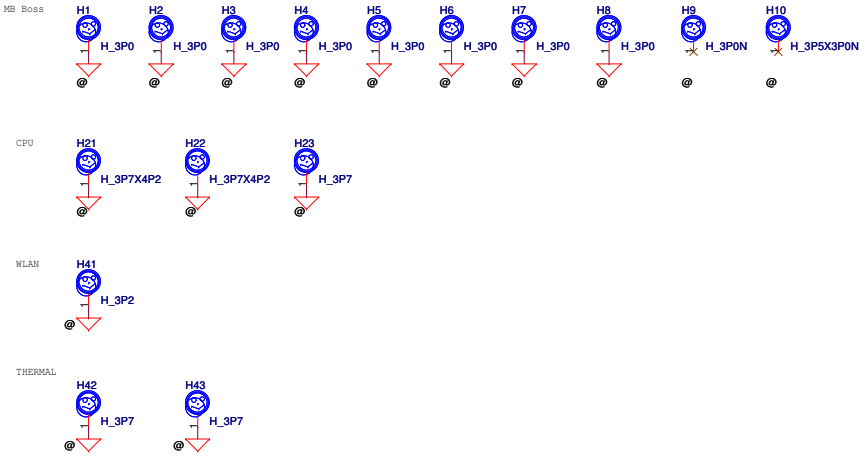




Fan Control Circuit



Screw Hole



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Compal Electronics, Inc.

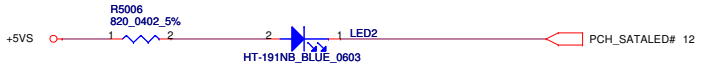
Title: PWRBTN/ FAN / Screws

Size: Custom | Document Number: QAL30 LA-8061P MB | Rev: 0.1

Date: Friday, January 13, 2012 | Sheet 31 of 46

LED

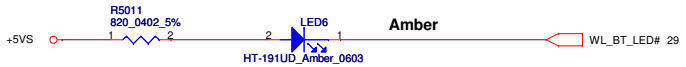
SATA



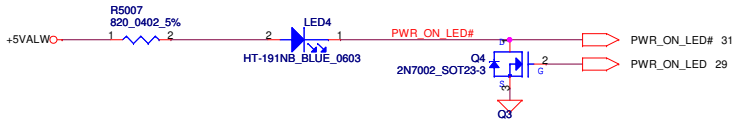
Battery



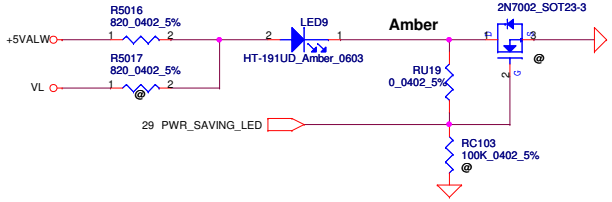
Wireless



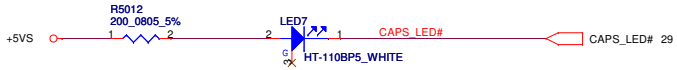
Power



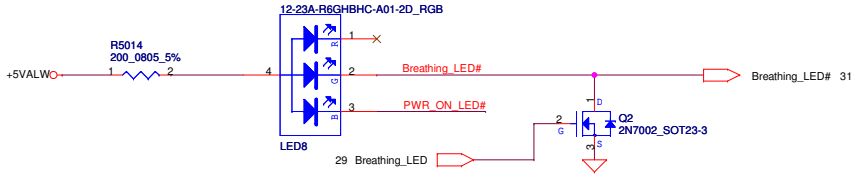
Power Saving



CAP Lock



Breathing



INT_KBD Conn.



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Title: KB/EC ROM/TP/FUN/LED

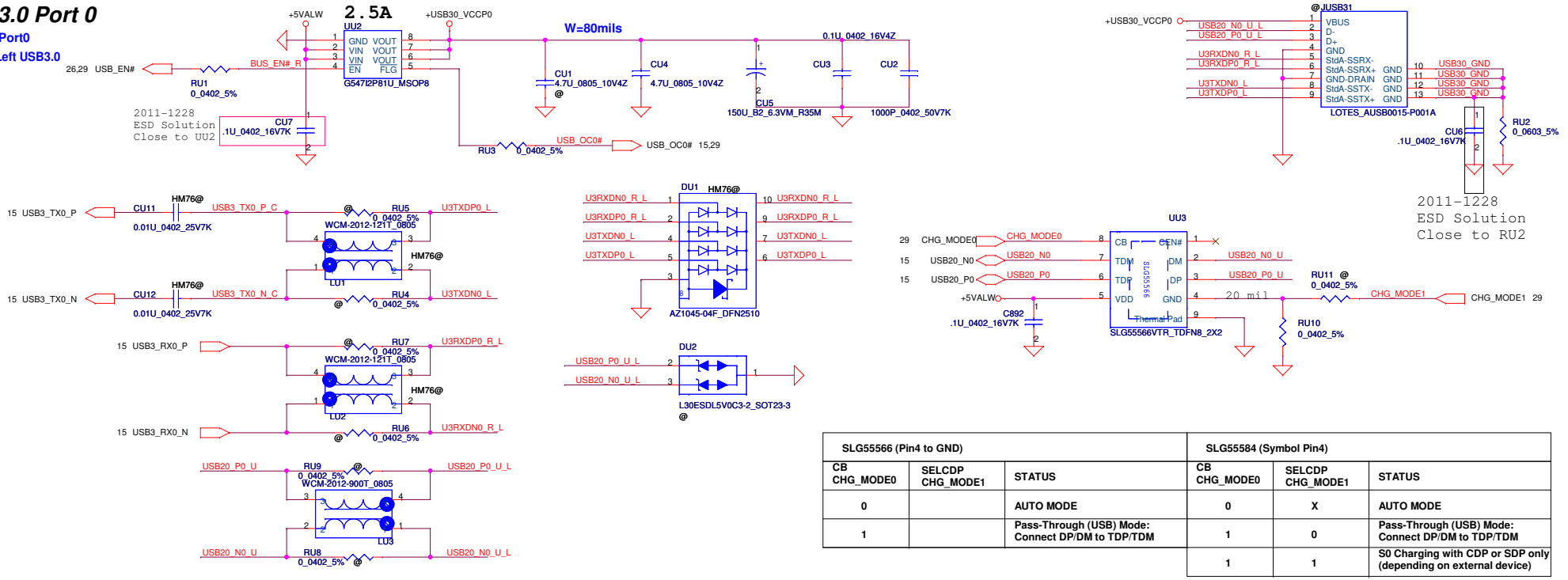
Size	Document Number	Rev
B	QAL30 LA-8061P MB	0.1

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USB3.0 Port 0

USB3.0 Port0

Port 0 : Left USB3.0

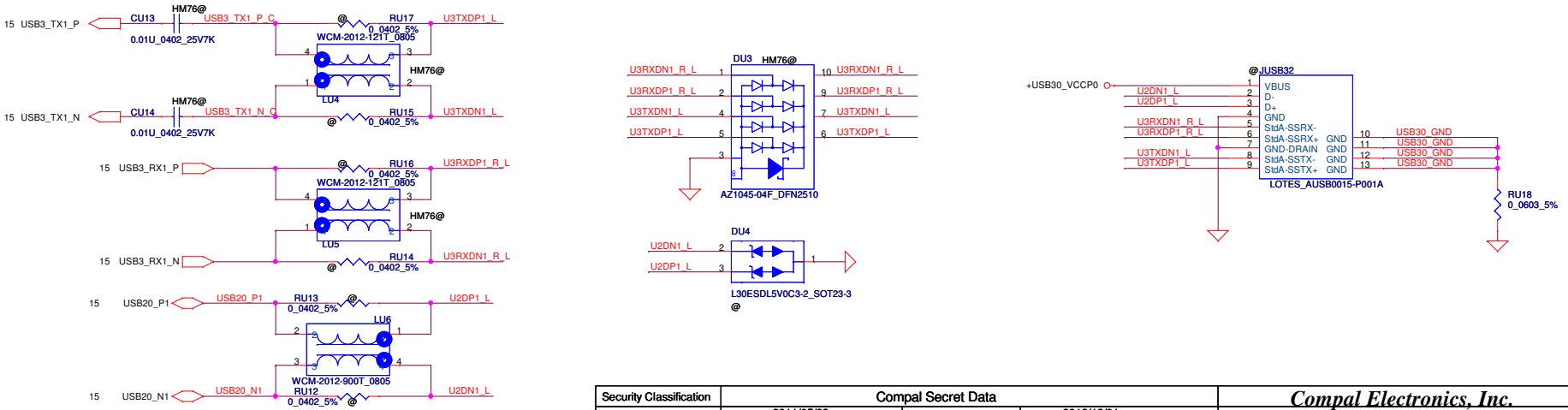


SLG55566 (Pin4 to GND)			SLG55584 (Symbol Pin4)		
CB CHG_MODE0	SELCDP CHG_MODE1	STATUS	CB CHG_MODE0	SELCDP CHG_MODE1	STATUS
0		AUTO MODE	0	X	AUTO MODE
1		Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM	1	0	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM
			1	1	S0 Charging with CDP or SDP only (depending on external device)

USB3.0 Port 1

USB3.0 Port1

Port 1 : Left USB3.0



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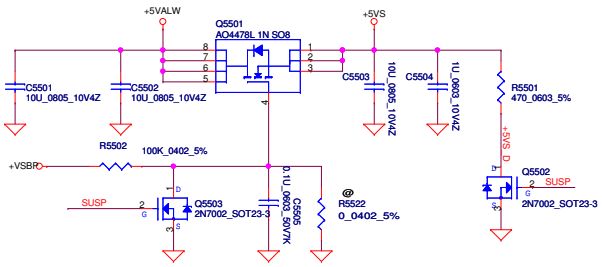
Compal Electronics, Inc.

Title: Power share ENE3810

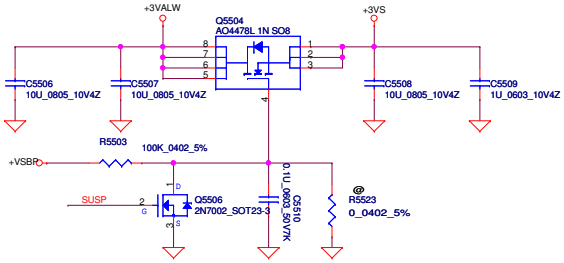
Size: Custom | Document Number: QAL30 LA-8061P MB | Rev: 0.1

Date: Friday, January 13, 2012 | Sheet 33 of 46

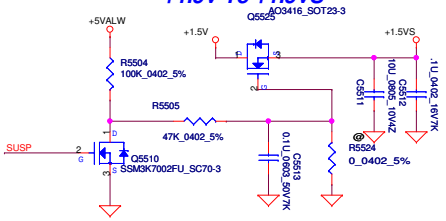
+5VALW to +5VS



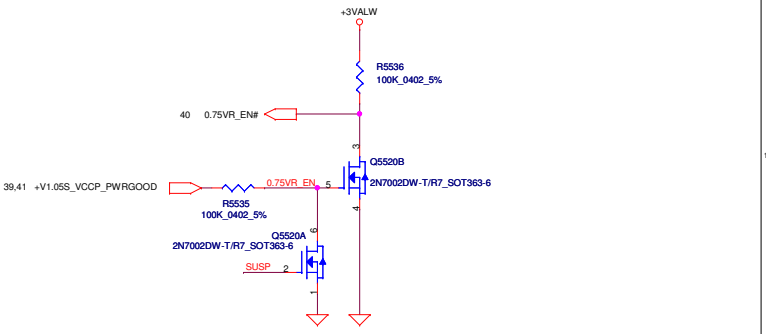
+3VALW to +3VS

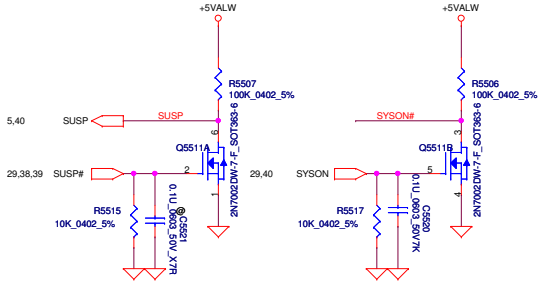


+1.5V To +1.5VS

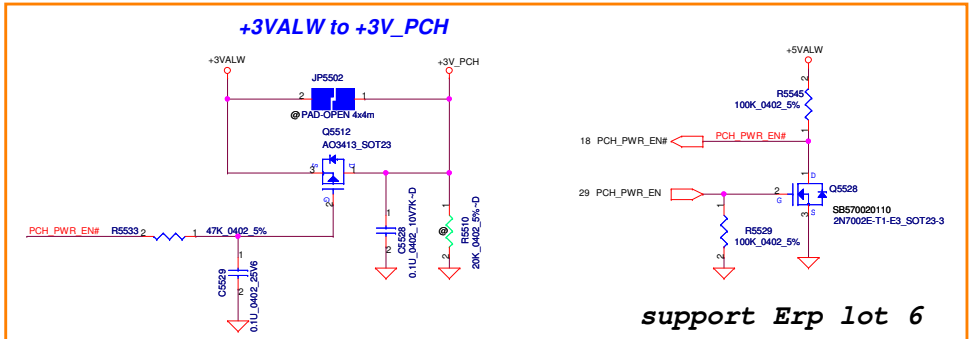


CHECK WITH CPU memory power

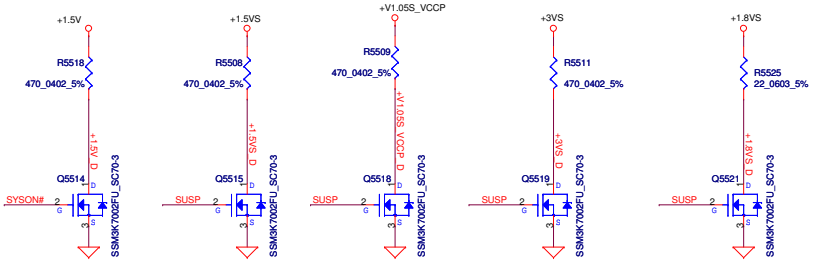


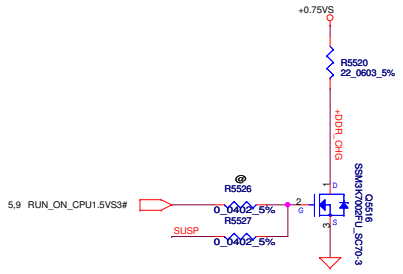


+3VALW to +3V_PCH



support Erp lot 6





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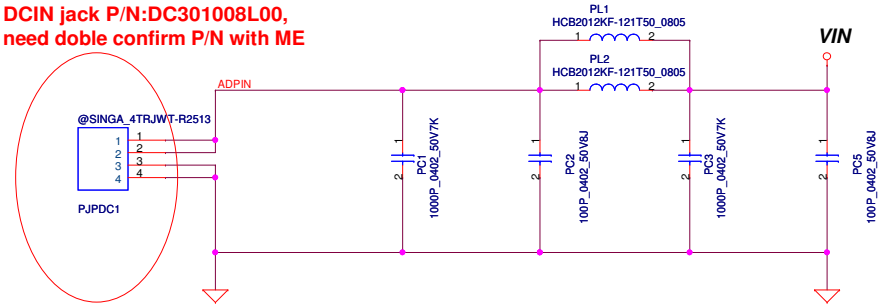
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Title: DC/DC Interface

Size	Document Number	Rev
Custom	QAL30 LA-8061P MB	0.1

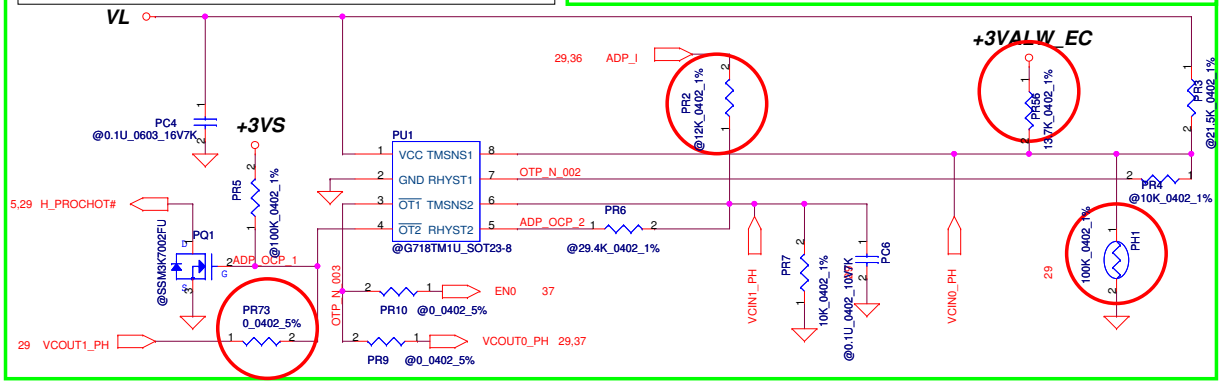
Date: Friday, January 13, 2012 Sheet 34 of 46

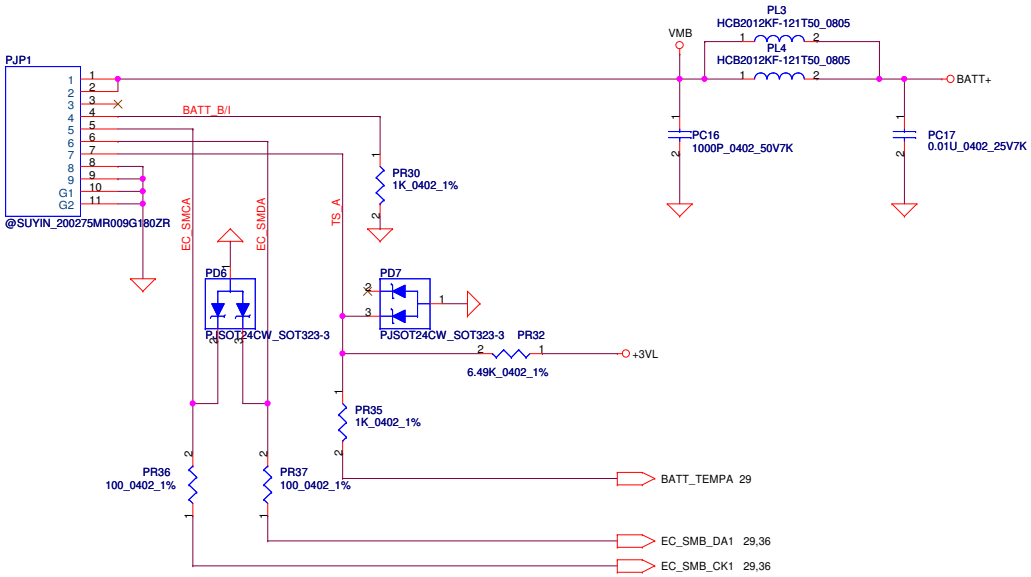
DCIN jack P/N:DC301008L00,
need doble confirm P/N with ME

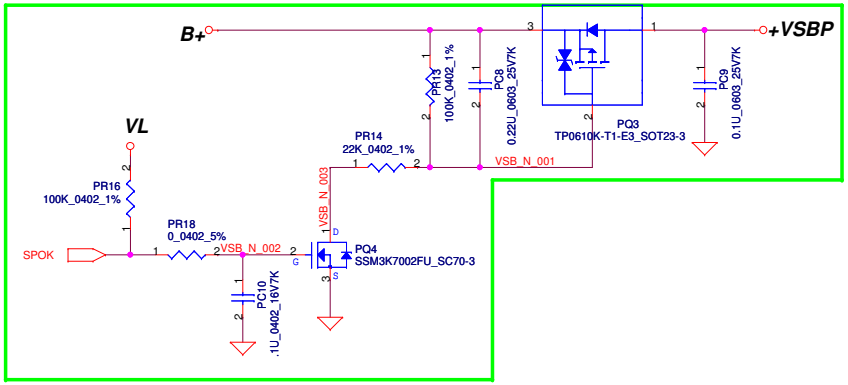


PH1 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

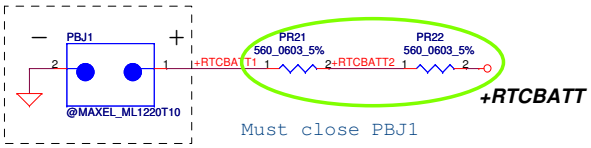
For KB930 --> Keep PU1 circuit
(Vth = 0.825V)
For KB9012 (Red square) --> Remove PU1 circuit, but keep PR56
PH1, PR2, PQ1, PR7,PQ15,PR73,PR56







RTC Battery



Must close PBJ1

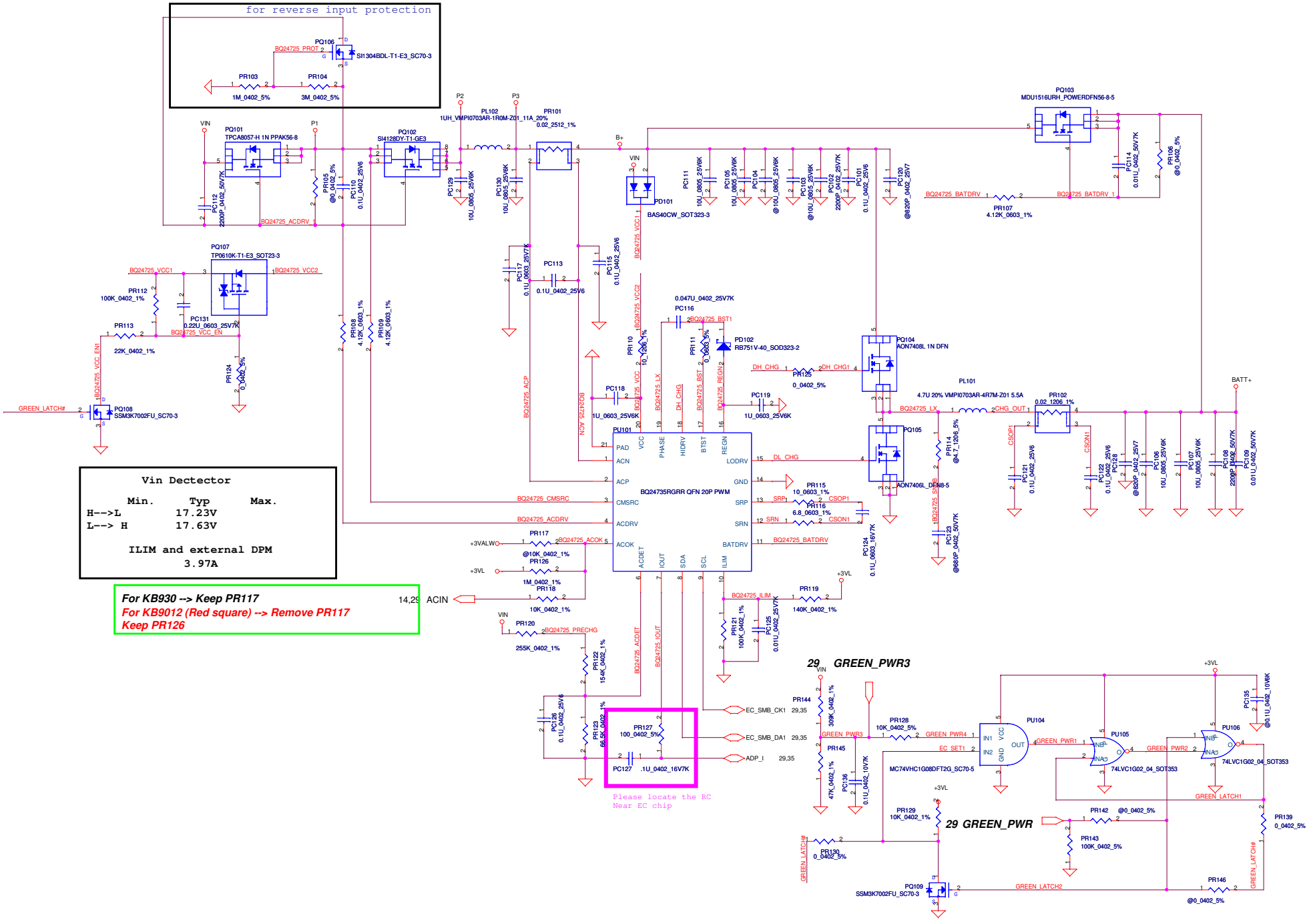
SP093MX0000
Change RTC For Cost Down

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Issued Date	2011/05/23	Deciphered Date	2012/12/31

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Title	PWR-DCIN / BATT CONN / OTP
Size	Document Number: PBL22 LA-7391P M/B
Rev	0.1
Date:	Friday, January 13, 2012
Sheet	35 of 46



Security Classification	Compal Secret Data		
Issued Date	2011/05/23	Deciphered Date	2012/12/31

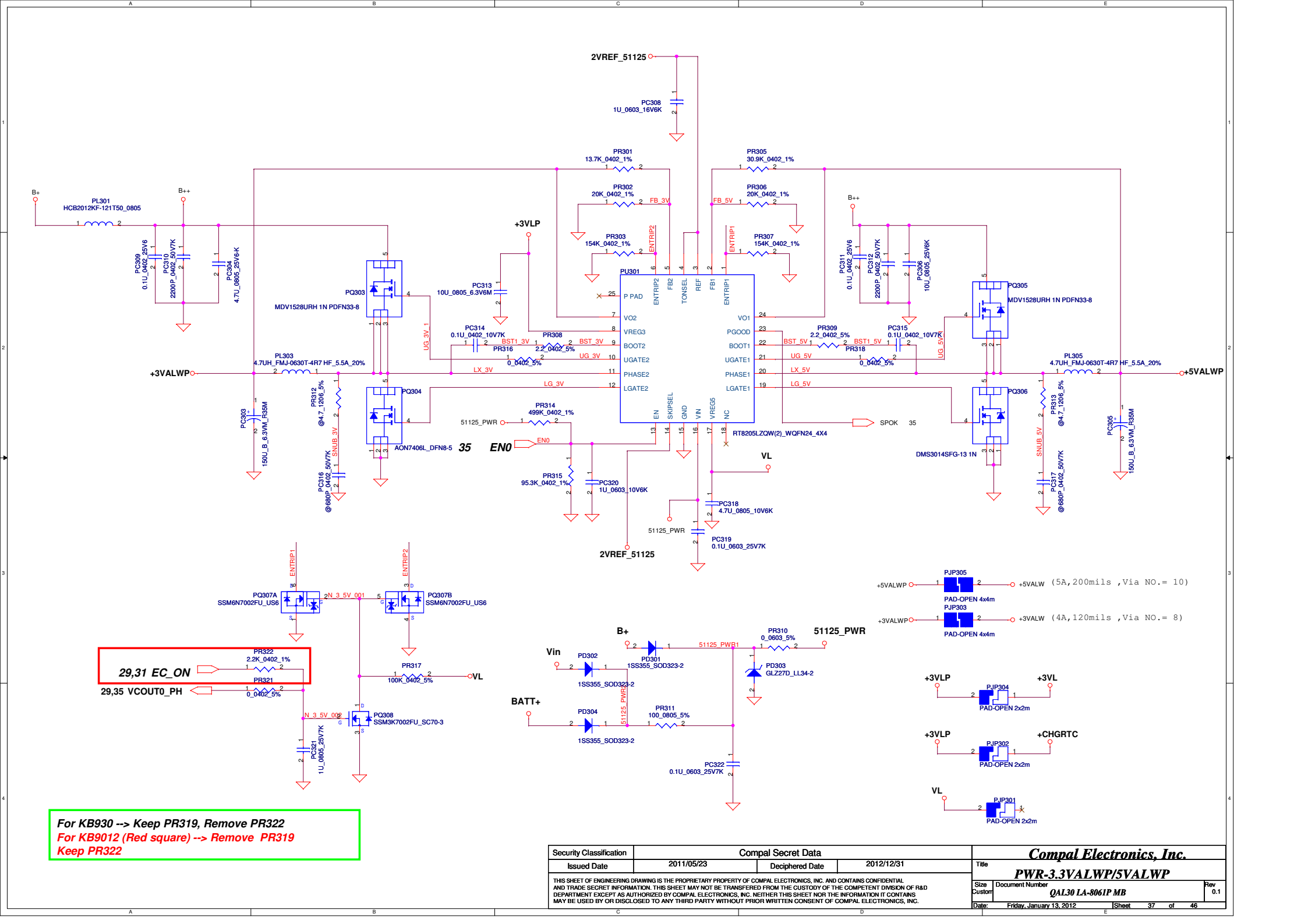
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Compal Electronics, Inc.

Title: **PWR-CHARGER**

Size	Document Number	Rev
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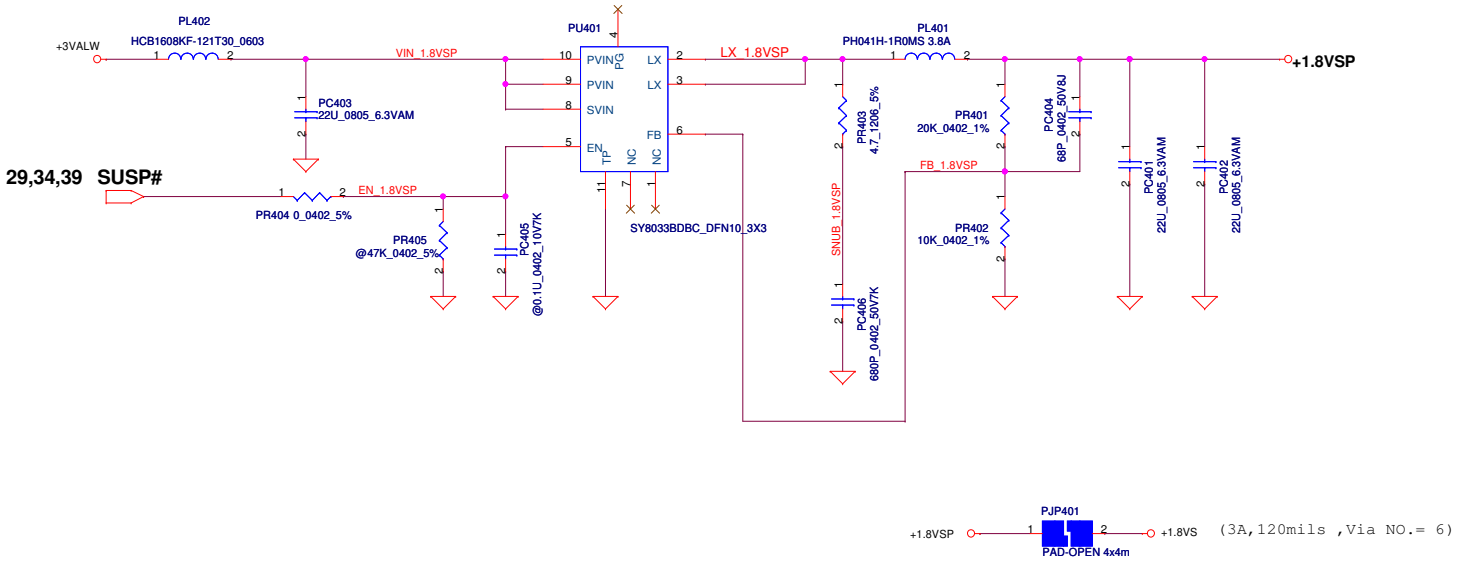
Date: Friday, January 13, 2012 Sheet 36 of 46



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Issued Date	2011/05/23	Deciphered Date	2012/12/31

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Compal Electronics, Inc.			
Title	PWR-3.3VALWP/5VALWP		
Size: Custom	Document Number: QAL30 LA-8061P MB		Rev: 0.1
Date: Friday, January 13, 2012	Sheet 37 of 46		



Security Classification	Compal Secret Data		
Issued Date	2011/05/23	Deciphered Date	2012/12/31

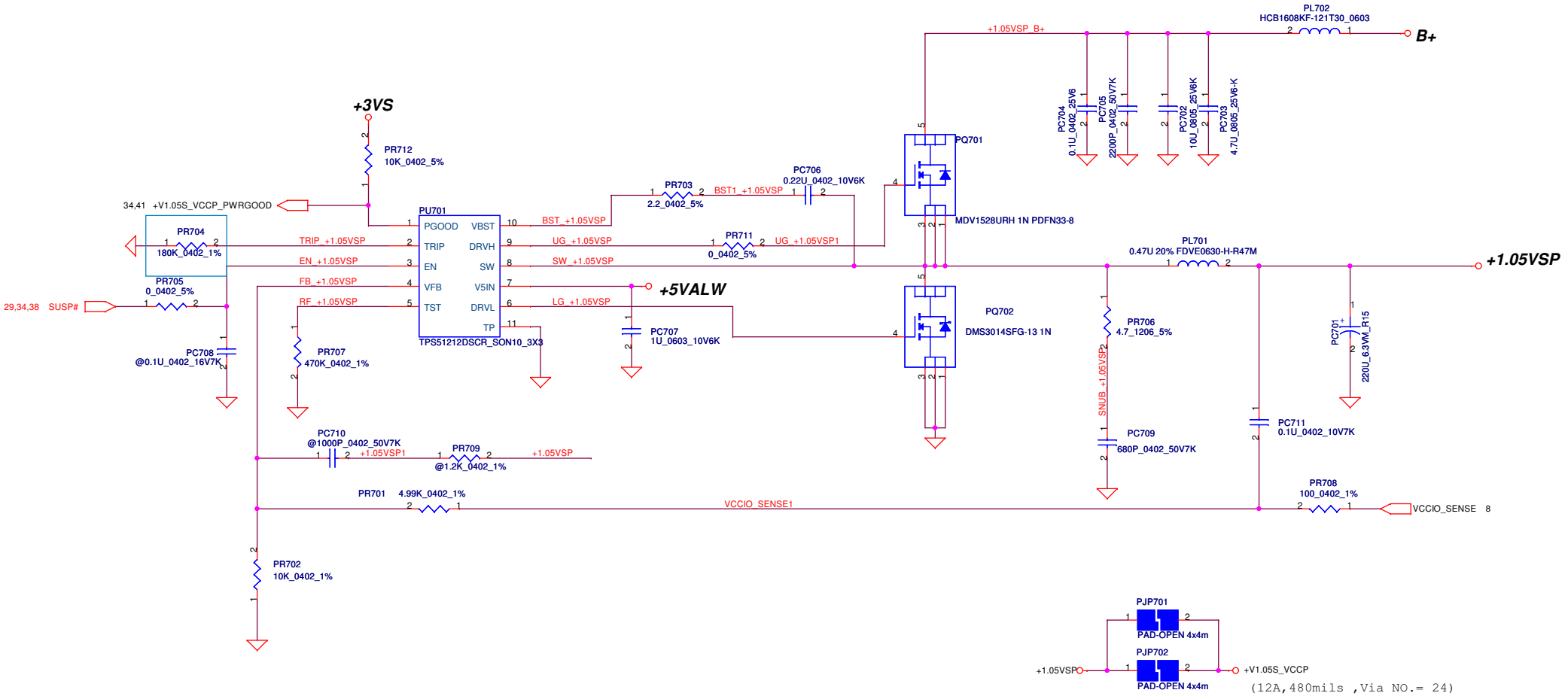
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Compal Electronics, Inc.

Title: **PWR-1.8VSP**

Size	Document Number	Rev
	PBL22 LA-7391P M/B	0.1

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Security Classification	Compal Secret Data		
Issued Date	2011/05/23	Deciphered Date	2012/12/31

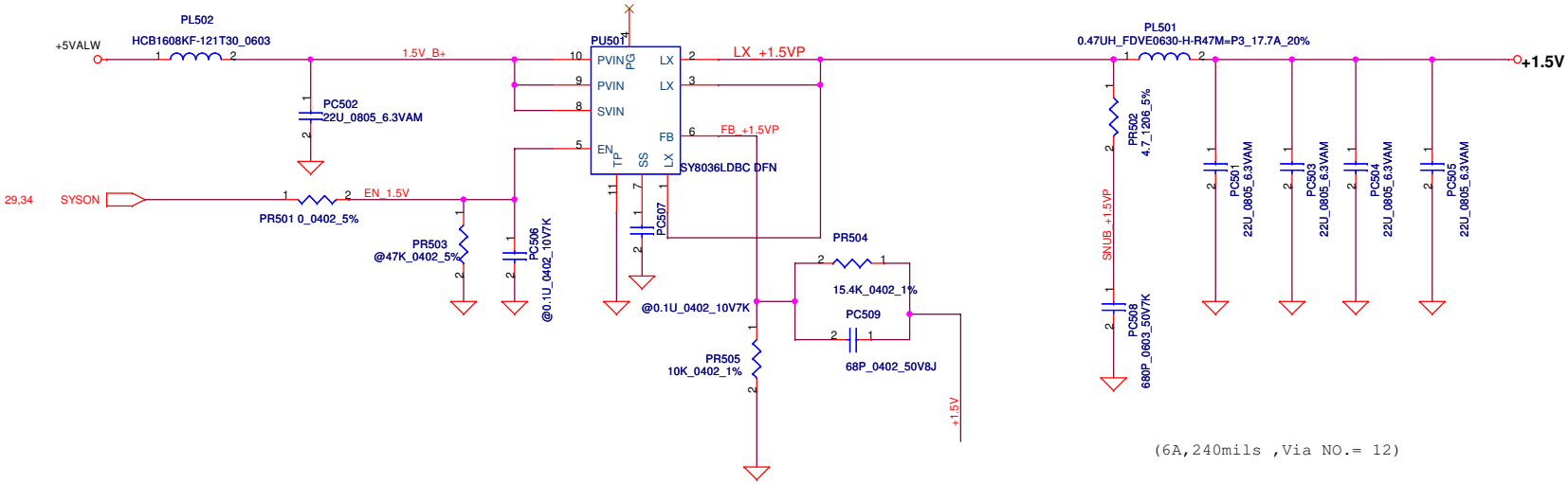
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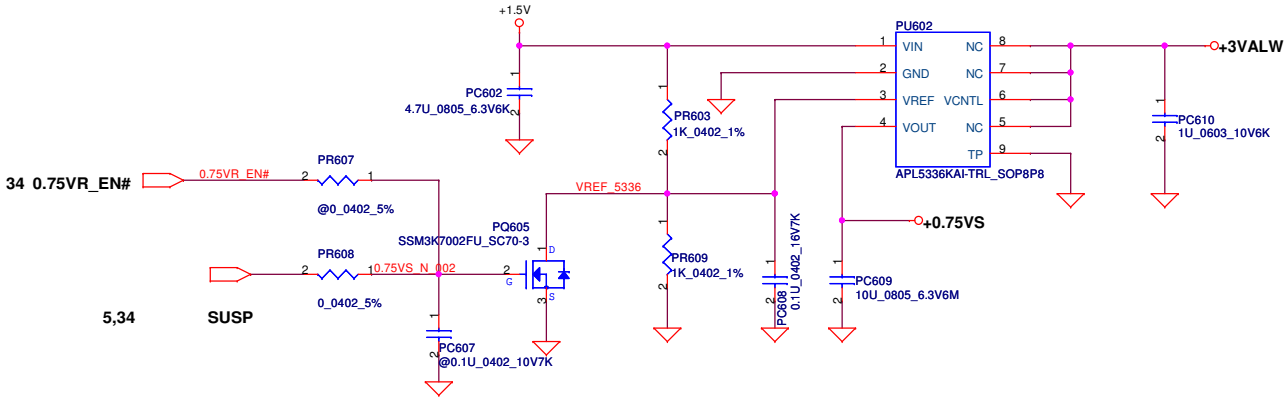
Compal Electronics, Inc.

Title: **PWR-V1.05SP**

Size	Document Number	Rev
Custom	PBL22 LA-7391P M/B	0.1

Date: Friday, January 13, 2012 | Sheet 39 of 46





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Compal Electronics, Inc.

Title: **PWR-1.5VP / +0.75VSP**

Size	Document Number	Rev
Custom	PBL22 LA-7391P M/B	0.1

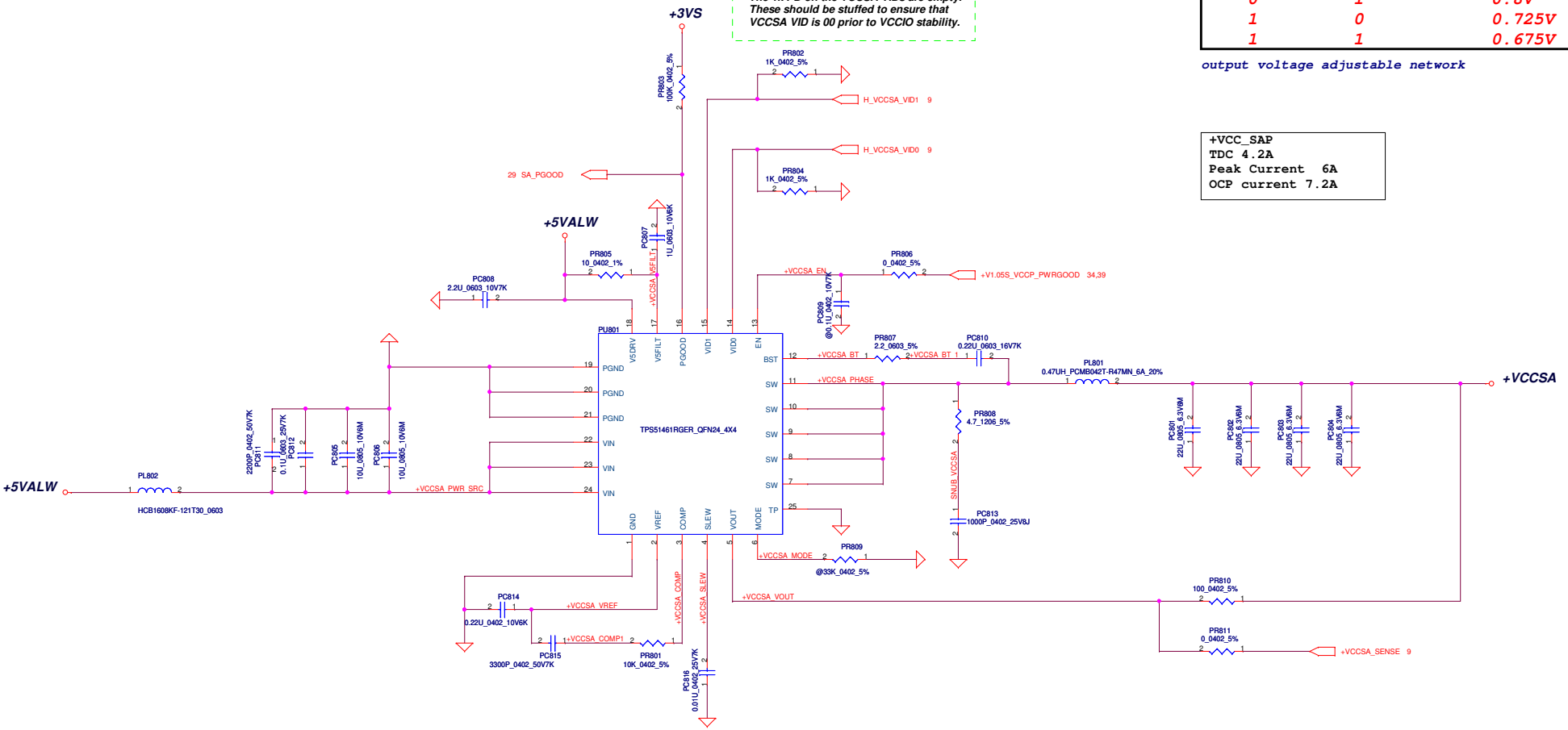
Date: Friday, January 13, 2012 | Sheet 40 of 46

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



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Compal Electronics, Inc.

Title: PWR-VCC_SAP

Size	Document Number	Rev
C	PBL22 LA-7391P M/B	0.1

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CSP1A, CSP2A to +5VS.

+5VS — PR272 — CSP1A @0_0402_5%

LGA, SWA, HGA, BSTA, DIFFA, TRBSTA#, ILIMA, PWMA are float.

VSPA, VSNA to GND (HW side).
CSREFA, TSNSA, IOUTA to GND.

FBA and COMPA are short.
CSCOMPA, CSSUMA, DROOPA are short.

DIS only:
All AXG components are @.
Except
PR272 and PR273 are 0ohm.
PC223, PC226, PR202 are 0ohm.
PC220, PC215, PR206 are 0ohm.

PR201 10_0402_1% FBA3 — PC213 0.033U_0402_16V7K
TRBSTA# — PR203 8.06K_0402_1% <BOM Structure> — FBA1 — PR204 806_0402_1%
PC217 0.015U_0402_16V7K
PR207 10_0402_1% FBA2 — PC219 680P_0402_50V7K <BOM Structure>
PC220
PR209 1K_0402_1%
PR210 10P_0402_50V8J COMPA1 — PC221 1500P_0402_50V7K
PR210 5.11K_0402_1%

PC214 .1U_0402_16V7K
PR202 24.9K_0402_1%
2P: 24K
1P: 24.9K

PC215 1000P_0402_50V7K
PC216 <BOM Structure>
@330P_0402_50V7K
PR205 75K_0402_1%
PR208 165K_0402_1%
PH203 220K_0402_5%_ERTJ0EV224J <BOM Structure>
NTC_PH203

PUT COLSE TO GT Inductor

CSCOMPA — PR206 1K_0402_1% — DROOPA — PC218 1000P_0402_50V7K — CSREFA
2P: 1.65K
1P: 1K

CSREFA — PC222 0.047U_0402_16V7K
CSP1A — PR213 5.49K_0402_1% SW1A

PR212 SW1A
113K +-1% 0603
PC223 1000P_0402_50V7K CSREFA 43

2P: 21.5K
1P: 15.8K
PR214 15.8K_0402_1%

9 VCC_AXG_SENSE
9 VSS_AXG_SENSE
PC224 1000P_0402_50V7K

+5VS
PC226 .1U_0402_16V7K

TSENSEA
PR215 8.25K_0402_1%
PH204 100K_0402_1%_TSM0B104F4251RZ
PUT COLSE TO V_GT HOT SPOT

PR218 26.1K_0402_1%
2P: 36K
1P: 26.1K

+V1.05S_VCCP
PC229 .1U_0402_16V7K
PR220 130_0402_1%
PR221 54.9_0402_1%
PC230 1U_0402_16V7K
PR226 0_0402_5%
8 VR_SVID_DAT
8 VR_SVID_ALRT#
8 VR_SVID_CLK
VR_SVID_DAT1

+5VS
PR219 2_0603_5%
PC228 2.2U_0603_10V7K
6132_VCC
PR222 0_0402_5%
29 VR_ON — VR_ON_CPU
VR_SVID_DAT1
VR_SVID_ALRT#
VR_SVID_CLK
PR227 95.3K_0402_1%
PR225 10K_0402_1% ROSC_CPU
VBOOT
CPU_B+ — PR230 1K_0402_1%
VRMP
VR_HOT#
VGATE
PC233
DIFF_CPU

PU201 NCP6132AMNR2G_QFN60_7X7 <BOM Structure>
PAD VSNA VSPA DIFFA TRBSTA# FBA COMPA IOUTA ILIMA DROOPA CSCOMPA CSSUMA CSREFA CSP2A CSP1A TSNSA
VCC VDDBP VRDYA EN SDIO ALERT# SCLK VBOOT ROSC VRMP VRHOT# VRDY VSN VSP DIFF
PWMA BSTA HGA SWA LGA BST2 HG2 SW2 LG2 PVCC PGND LG1 SW1 HG1 BST1
TRBST# FB COMP IOUT ILIM DROOP CSCOMP CSREF CSP3 CSP2 CSP1 TSNS TSNSEN PWM

BSTA1 — PR223 2.2_0603_5% — PC227 0.22U_0402_10V6K
HG1A 43
LG1A 43
BST2 — PR224 2.2_0603_5% — PC231 0.22U_0402_10V6K
HG2 43
LG2 43
6132P_VCC — PR228 0_0402_5% — PC232 2.2U_0603_10V7K
LG1 43
BST1 — PR231 2.2_0603_5% — PC234 0.22U_0402_10V6K
HG1 43
SW1A 43
SW2 43
+5VS
SW1 43

+V1.05S_VCCP
PR232 @75_0402_1%
+3VS
PR233 10K_0402_5%
29 VR_HOT#
14,29 VGATE
8 VSSSENSE
8 VCCSENSE
PC235 1000P_0402_50V7K

3P: 73.2K
2P: 41.2K
PR234 41.2K_0402_1%

3P: 22p
2P: 10p

PC236 1.1U_0402_16V7K
TSBNSE
CSP1
CSP2
+5VS

3P: 330p
2P: 1000p
PR240 1K_0402_1%
PC238 10P_0402_50V8J

3P: 21K
2P: 12.4K
PR239 12.4K_0402_1%

PR242 49.9_0402_1% FB_CPU1 — PC240 560P_0402_50V7K
PR243 6.34K_0402_1% COMP_CPU1 — PC241 1200P_0402_50V7K
3P: 6.04K
2P: 4.32K

CSREF 43
PC243 1000P_0402_50V7K
CSCOMP

3P: 1500p
2P: 1200p

CSP2 — PR241 5.49K_0402_1% SW2
PC239 0.047U_0402_16V7K
CSREF
CSP1 — PR245 5.49K_0402_1% SW1
PC244 0.047U_0402_16V7K
CSREF

PR244 10_0402_1% FB_CPU3 — PC242 0.033U_0402_16V7K
TRBST#
PR247 8.06K_0402_1% <BOM Structure>
FB_CPU2
PR248 806_0402_1%
PC245 0.015U_0402_16V7K

CSSUM
PC246 1000P_0402_50V7K <BOM Structure>
PR249 191K +-1% 0603 SW1
PR251 191K +-1% 0603 SW2
PC248 330P_0402_50V7K
PR252 75K_0402_1% NTC_PH201 PR253 165K_0402_1%
PH201 220K_0402_5%_ERTJ0EV224J

3P: 23.7K
2P: 24.9K
PR250 24.9K_0402_1%
PC247 1U_0402_16V7K

PUT COLSE TO VCORE Phase 1 Inductor

CSCOMP — PR255 1K_0402_1% — DROOP — PC249 1000P_0402_50V7K — CSREF
3P: 806
2P: 1K

TSENSE
PR246 8.25K_0402_1%
PH202 100K_0402_1%_TSM0B104F4251RZ
PUT COLSE TO VCORE HOT SPOT

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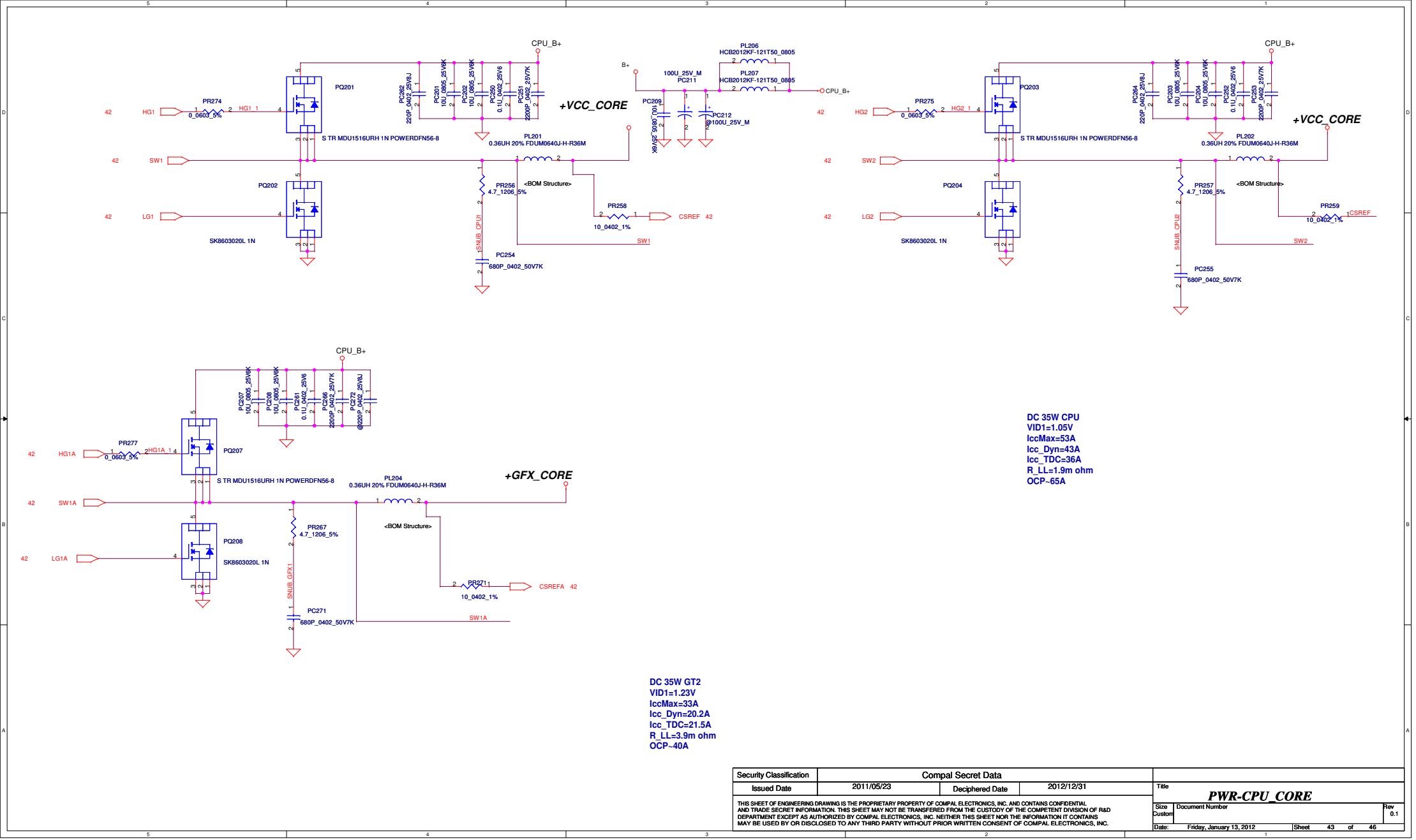
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Title: PWR-CPU_CORE

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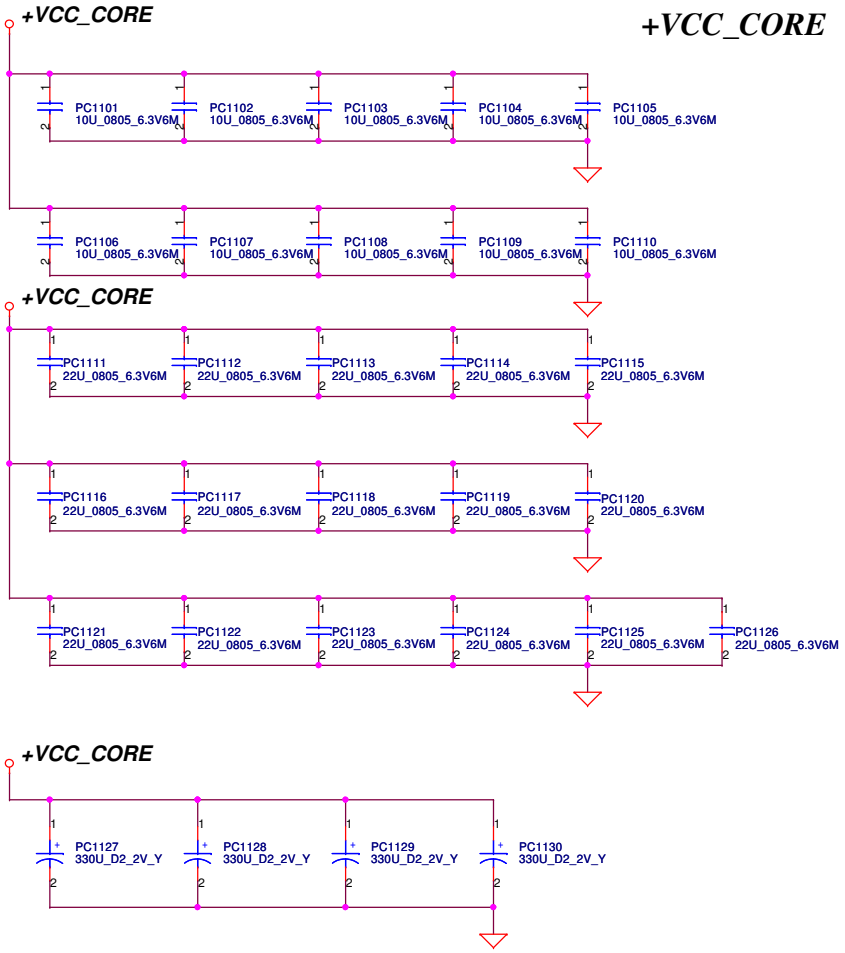
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Title: **PWR-CPU_CORE**

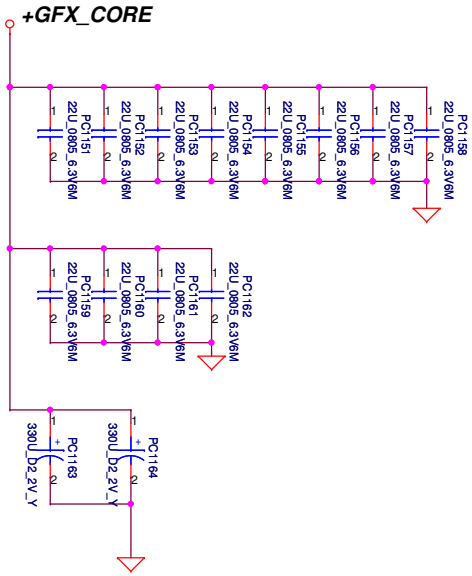
Size	Document Number	Rev
Custom		0.1

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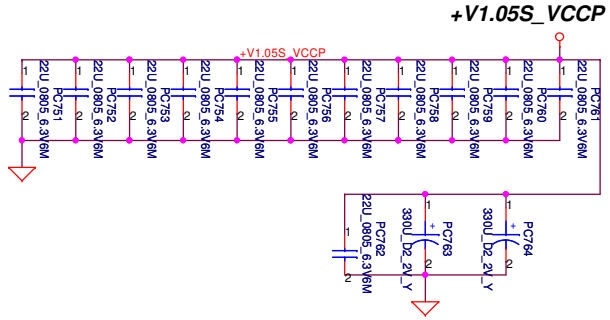
+VCC_CORE

+GFX_CORE



Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



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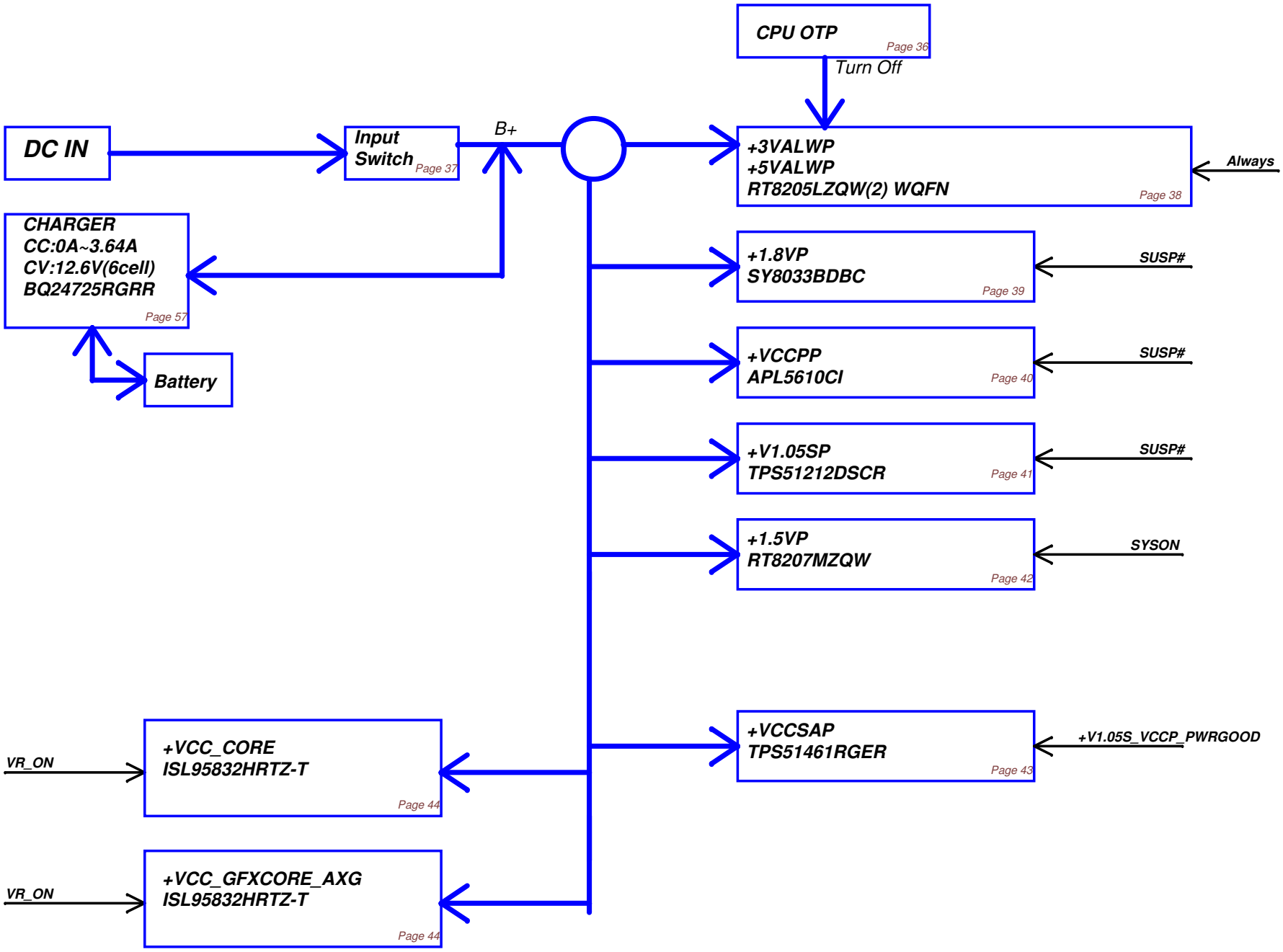
Compal Electronics, Inc.

Title: PWR - PROCESSOR DECOUPLING

Size	Document Number	Rev
	QAL30 LA-8061P MB	0.1

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Power block



Security Classification	Compal Secret Data		
Issued Date	2011/05/23	Deciphered Date	2012/12/31

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Title: POWER BLOCK DIAGRAM

Size	Document Number	Rev
Custom	QAL30 LA-8061P MB	0.1

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1					PR504 change from 15K to 15.4K		
2					charger IC change form bq24725A to bq24735		
3					PQ104,PQ303,PQ305,PQ701 charge form SIS412DN to MDV1528URH		
4					PQ306 charge from AON7702L to FDMC7692S		

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Title: PWR - PIR

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