Compal Confidential

QAZ00 (Shuriken 13.3) M/B Schematics Document

Intel Sandy Bridge ULV Processor with DDRIII + Cougar Point PCH SFF

LA-7531P **Date : 2011/04/10**
Version 0.1 modify

Security Classification	Compal Secret Data		
Issued Date	2010/08/03	Deciphered Date	

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Title: *Cover Page*

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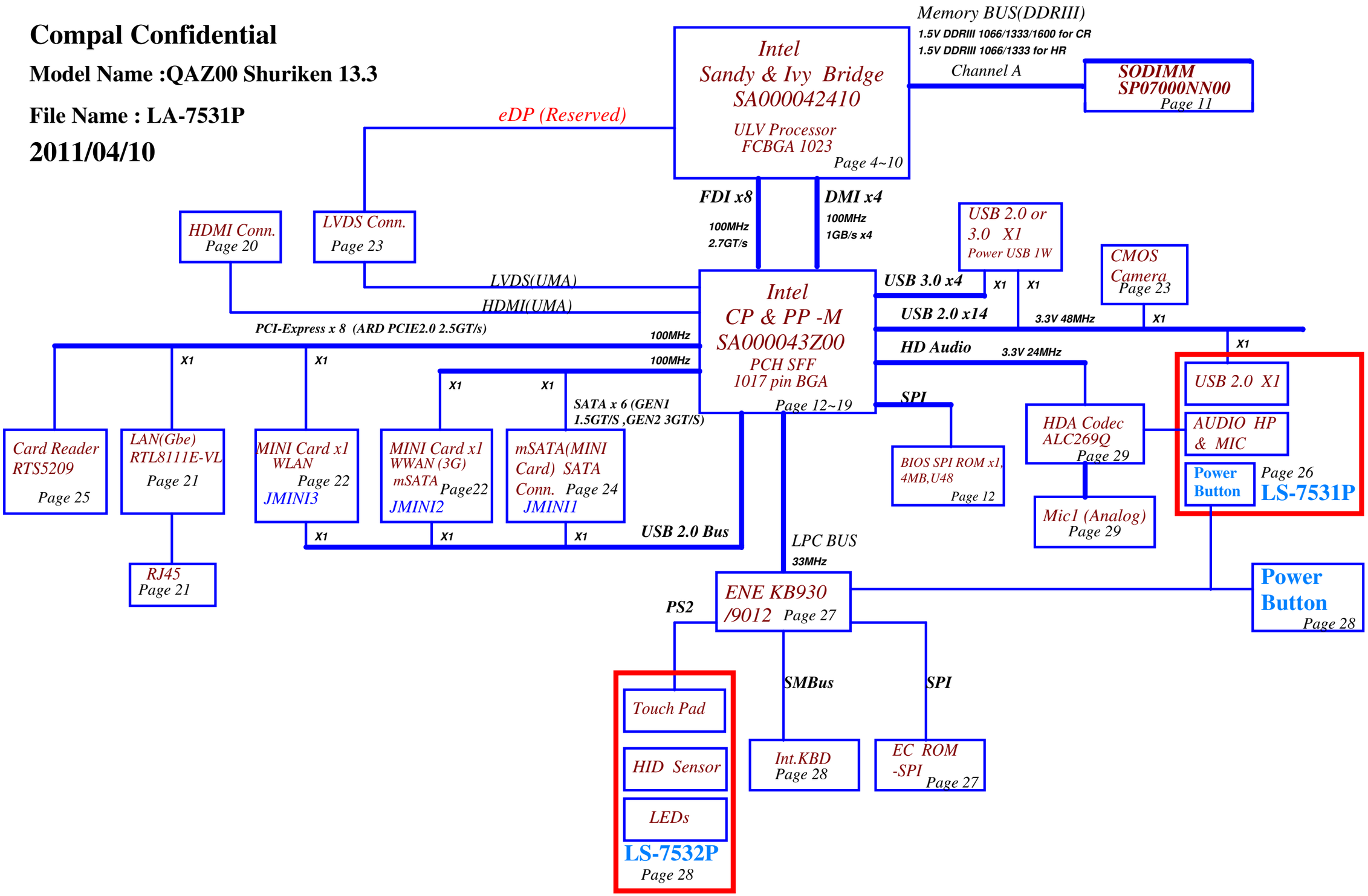
Model Name :QAZ00 Shuriken 13.3

File Name : LA-7531P

2011/04/10



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VCCP	+V1.05SP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+VCCP	+VCCP (1.05V) power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII (1.35V OR 1.5V)	ON	ON	OFF
+1.5VS	+1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+5VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+LAN_IO	+3VALW to +LAN_IO power rail for LAN	ON	ON	ON*
+3V_PCH	+3VALW to +3V_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V_PCH	+5VALW to +5V_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	B+ to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
PCH (Reserve)	1010 0110b

PCH SM Bus address

Device	Address
DDR DIMM0	1010 0000b
Mini Card1	
Mini Card2	
Mini Card3	

SMBUS Control Table

2011/04/07 Modify

	SOURCE	BATT	MIINI1	MINI2	MINI3	SODIMM	EC_SMB_CK2 PCH_SMBDATA	PCH_SMBCLK PCH_SMBDATA
EC_SMB_CK1 EC_SMB_DA1	KB930	V	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB930	X	X	X	X	X	O	V
PCH_SMBCLK PCH_SMBDATA	PCH	X	V	V	V	V	V	O
PCH_SMLCLK PCH_SMLDATA	PCH	X	X	X	X	X	X	X

CLKOUT	DESTINATION
PCI0	PCH_LPBACK
PCI1	PCI_LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	m-SATA,JMINI1
SATA1	m-SATA,JMINI2
SATA2	None
SATA3	None
SATA4	None
SATA5	None

USB Port Table

2011/04/09 Check

USB 2.0	USB 1.1	Port	2 External USB Port
EHCI1	UHCI0	0	
		1	USB/B (Right Side)
	UHCI1	2	
		3	Camera
	UHCI2	4	Mini Card(WLAN)
		5	WWAN (3G)
	UHCI3	6	
		7	mSATA
EHCI2	UHCI4	8	
		9	USB/B (Right Side)
	UHCI5	10	
		11	
	UHCI6	12	
		13	

USB 3.0	Port	2 External USB Port
	1	
	2	USB/B (Right Side)
	3	
	4	

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	None
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	CARD READER	CLKOUTFLEX2	None
	CLKOUT_PCIE3	MINI CARD WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Option	@		HDMI@		EMI@
UMA	X	X	V	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

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Title: Notes List

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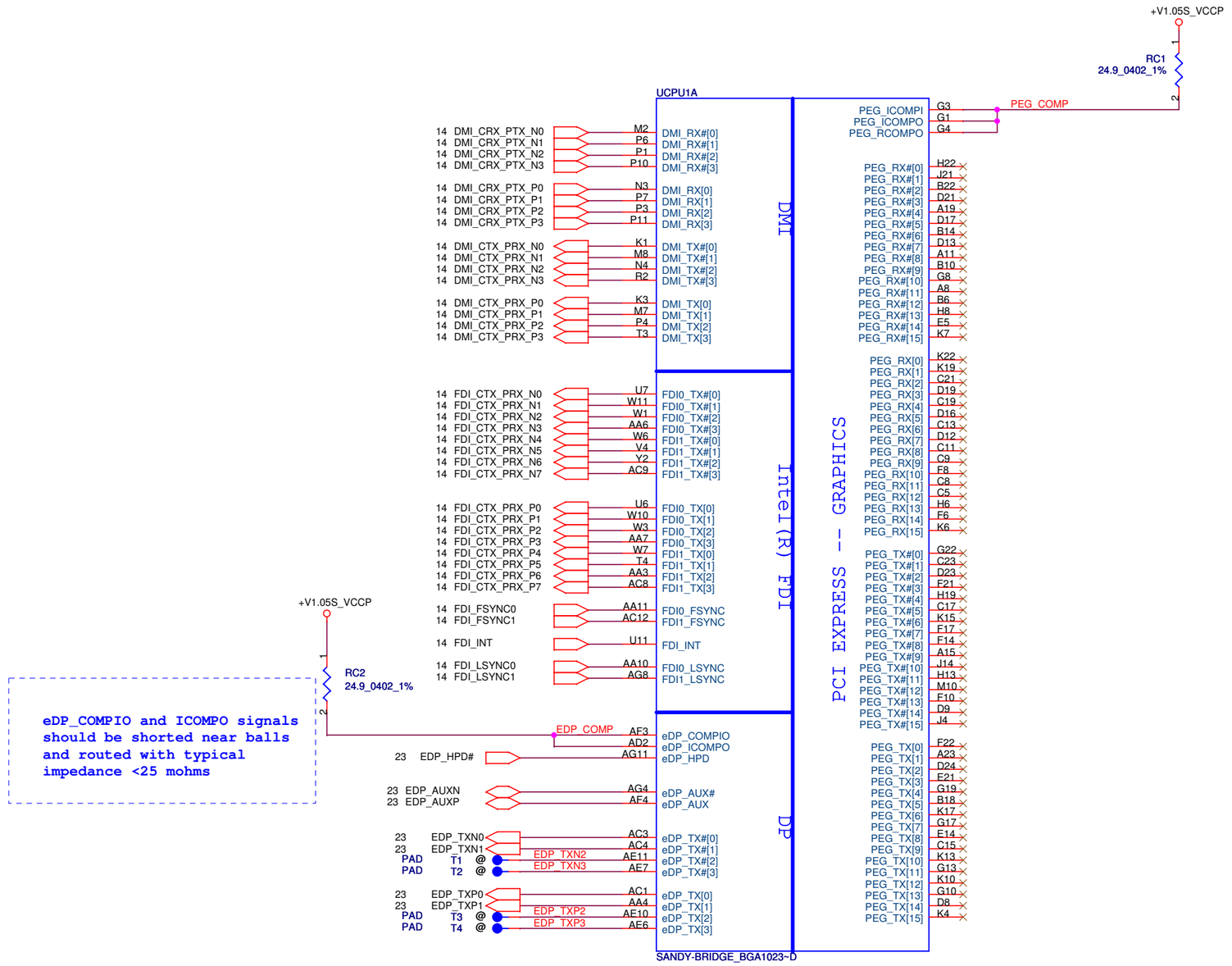
PEG_ICOMPI and RCOMPO signals should be shorted and routed
with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils
- typical impedance = 14.5 mohms



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Title: **PROCESSOR(1/7) DMI,FDI,PEG**

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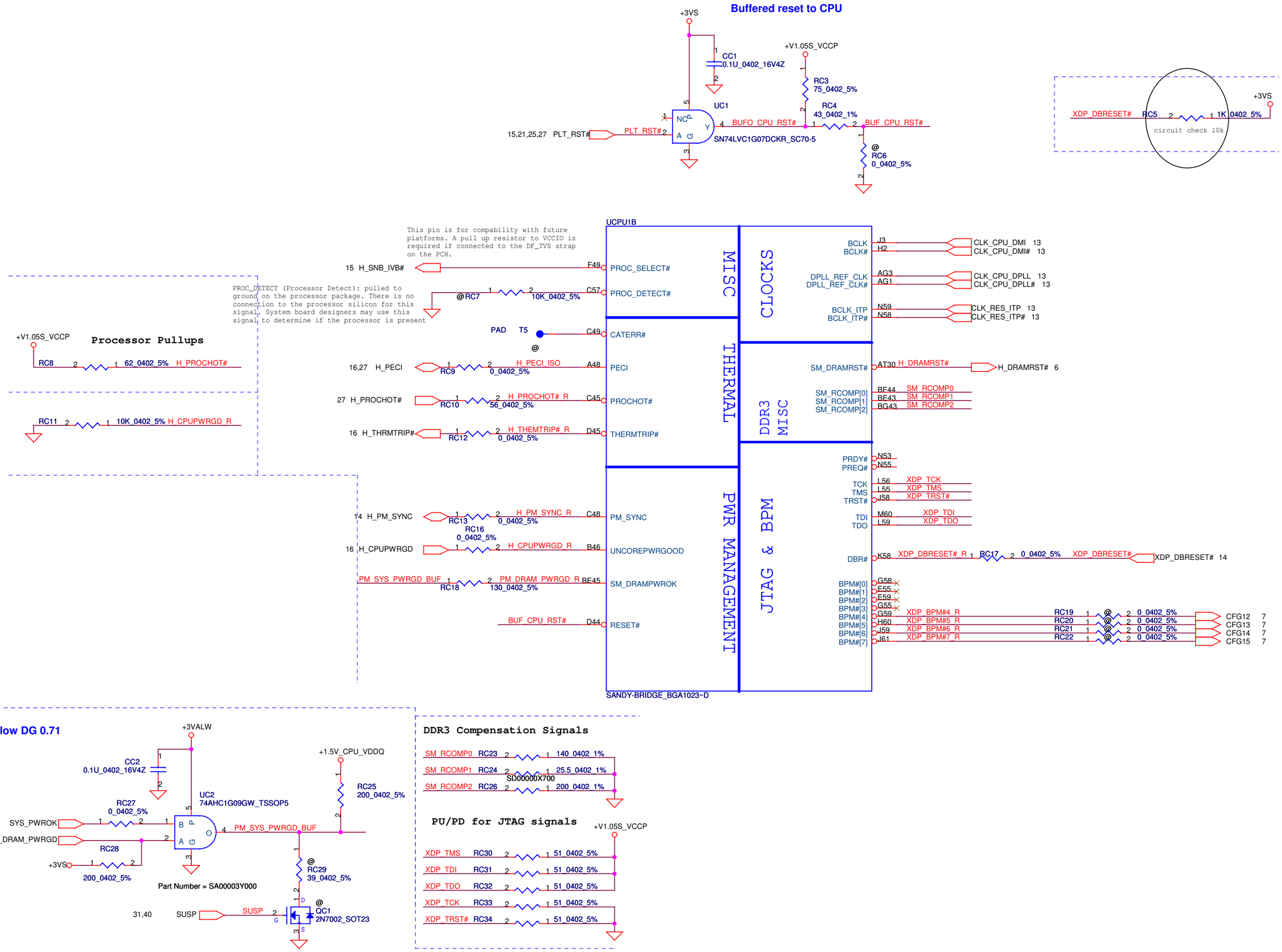

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Title: **PROCESSOR(2/7) PM,XDP,CLK**

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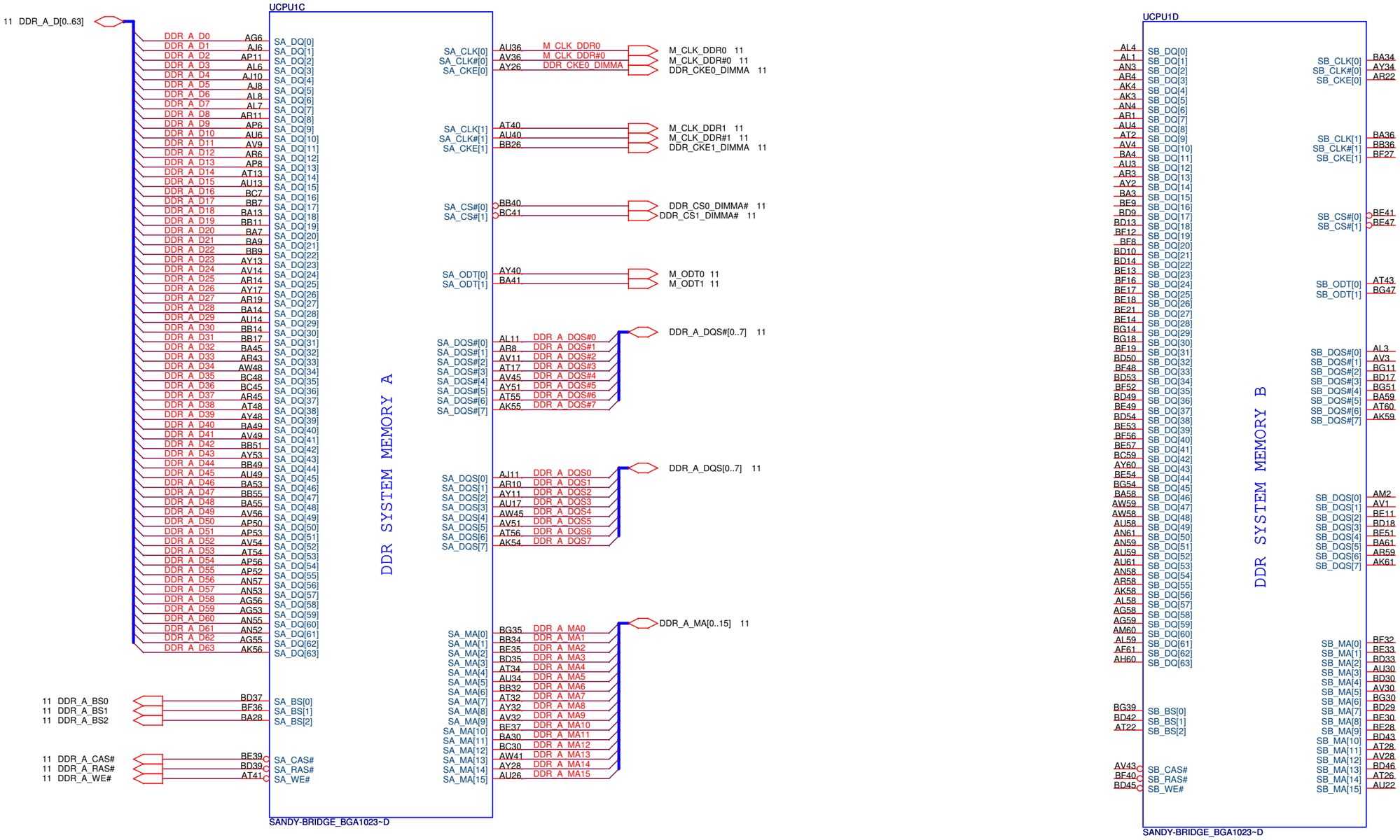

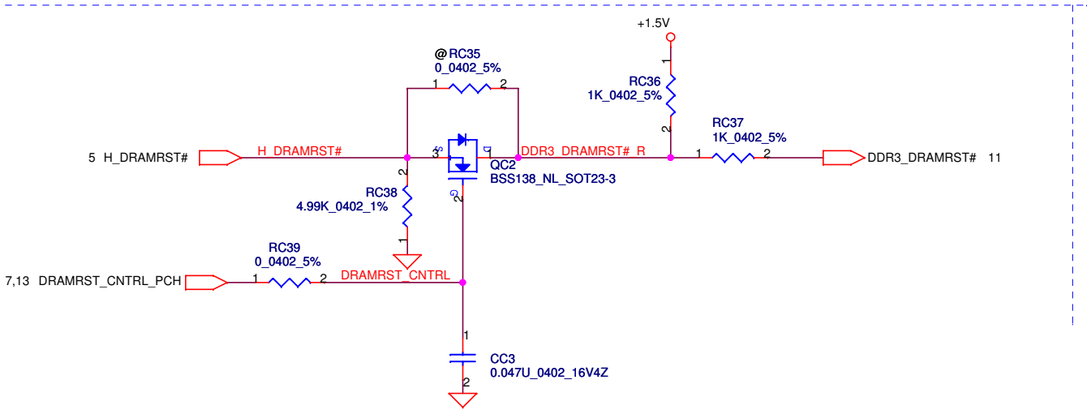

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Title: **PROCESSOR(3/7) DDRIII**

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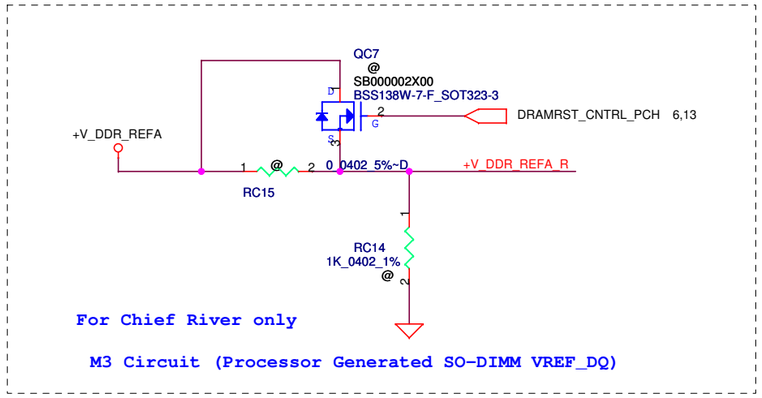
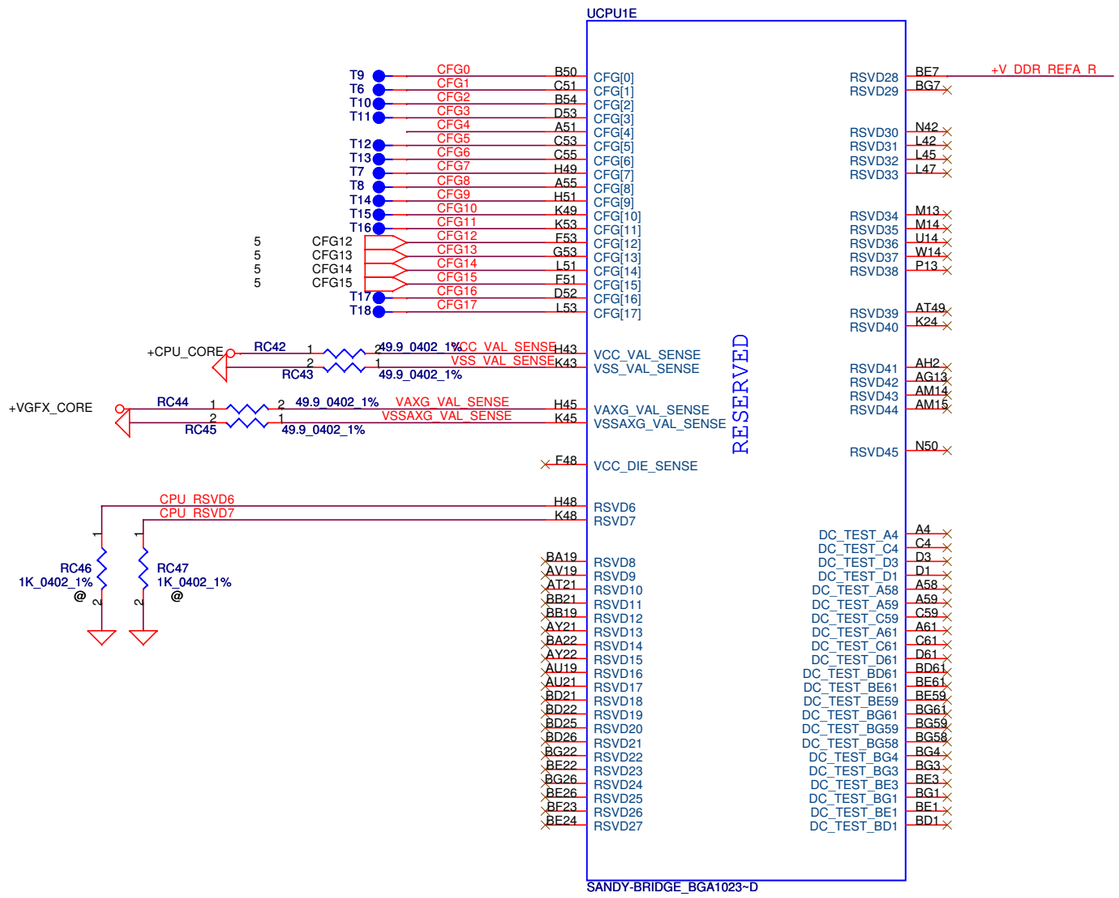
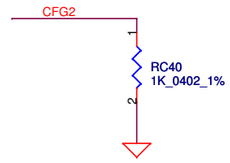
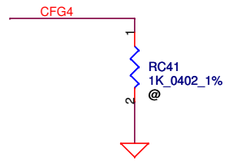




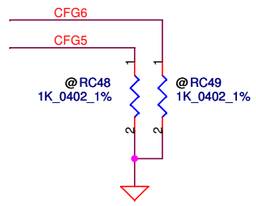
CFG Straps for Processor



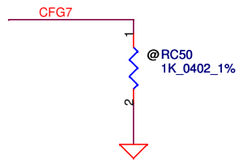
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: **PROCESSOR(4/7) RSVD,CFG**

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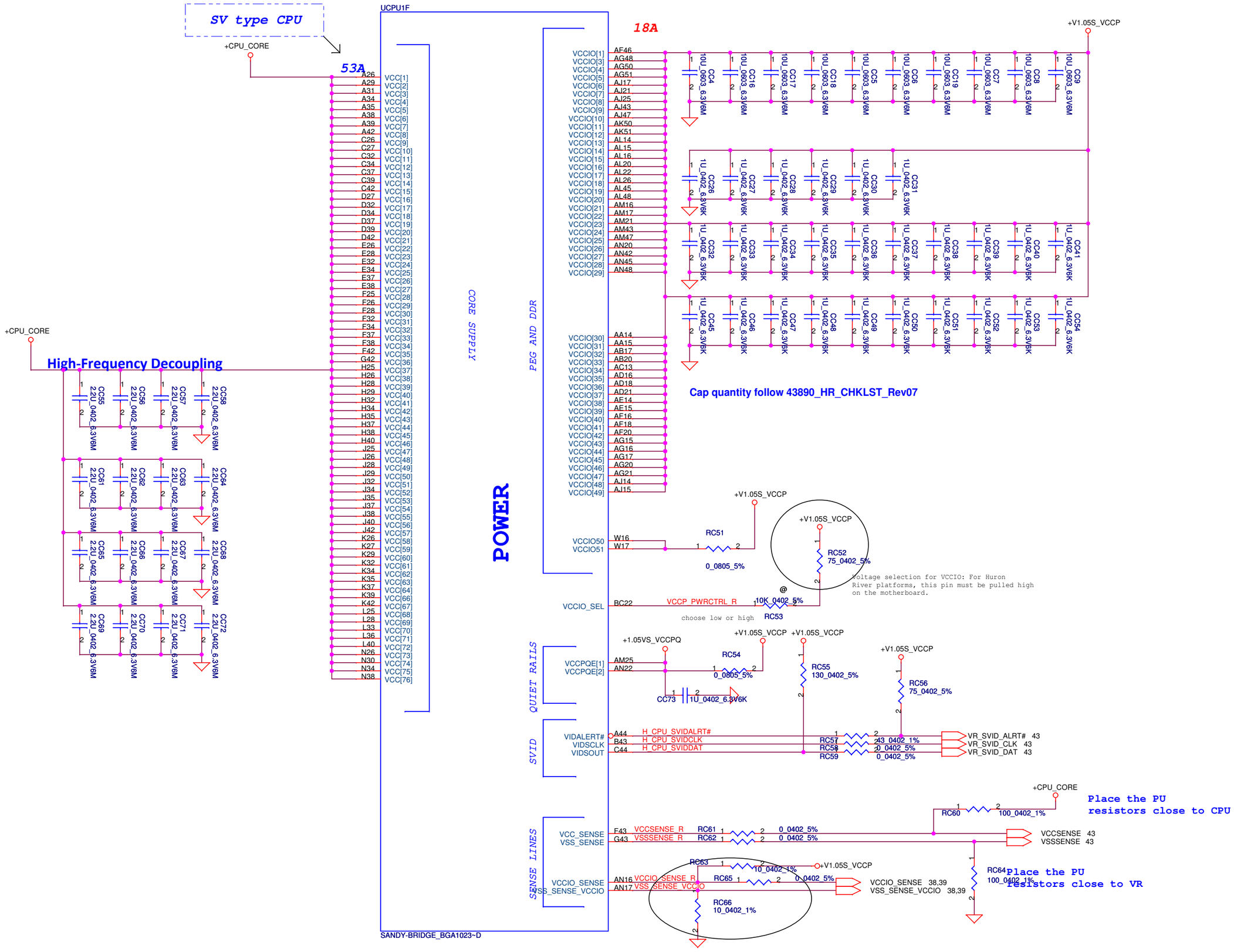

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Issued Date	2010/04/26	Deciphered Date	2010/05/28	Title: PROCESSOR(5/7) PWR,BYPASS
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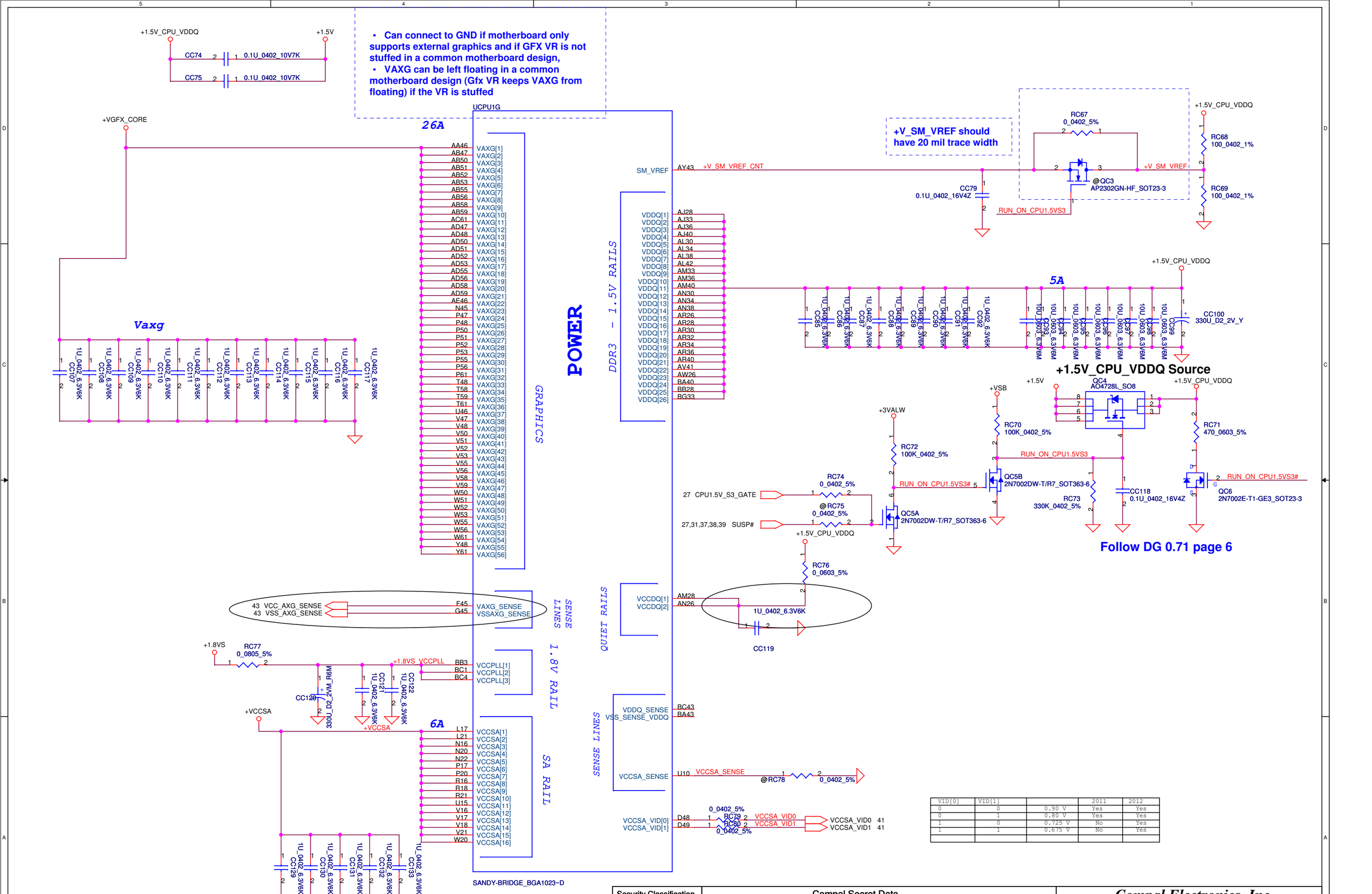

VID[0]	VID[1]		2011	2012
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0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes

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Title: **PROCESSOR(6/7) PWR**

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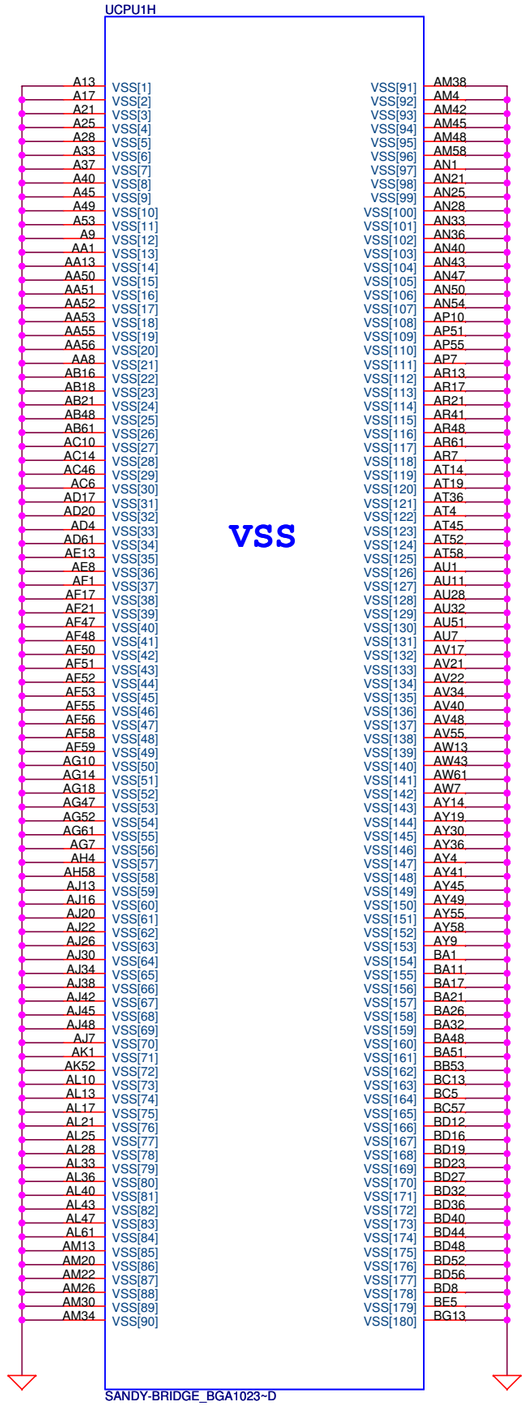

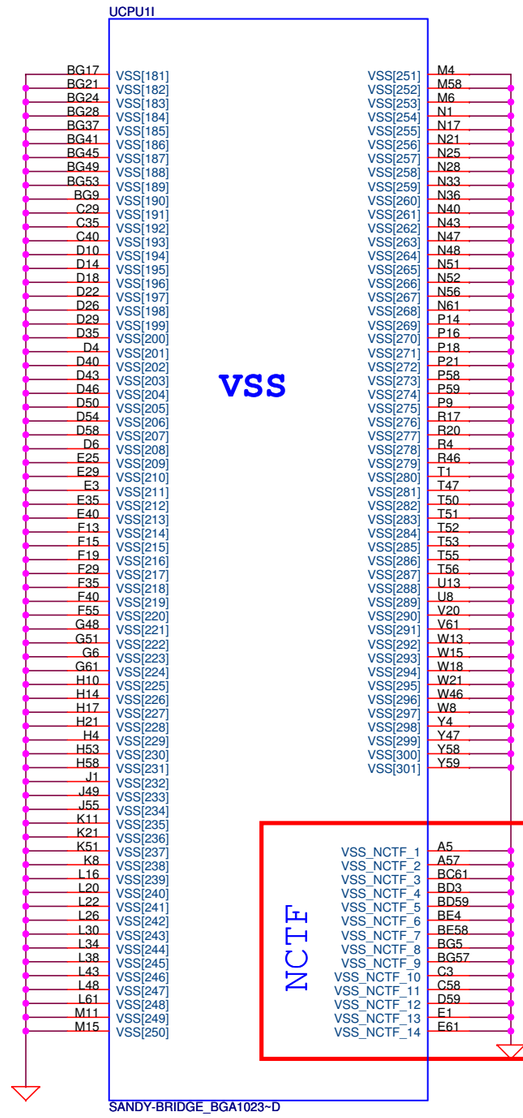

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Title: **PROCESSOR(7/7) VSS**

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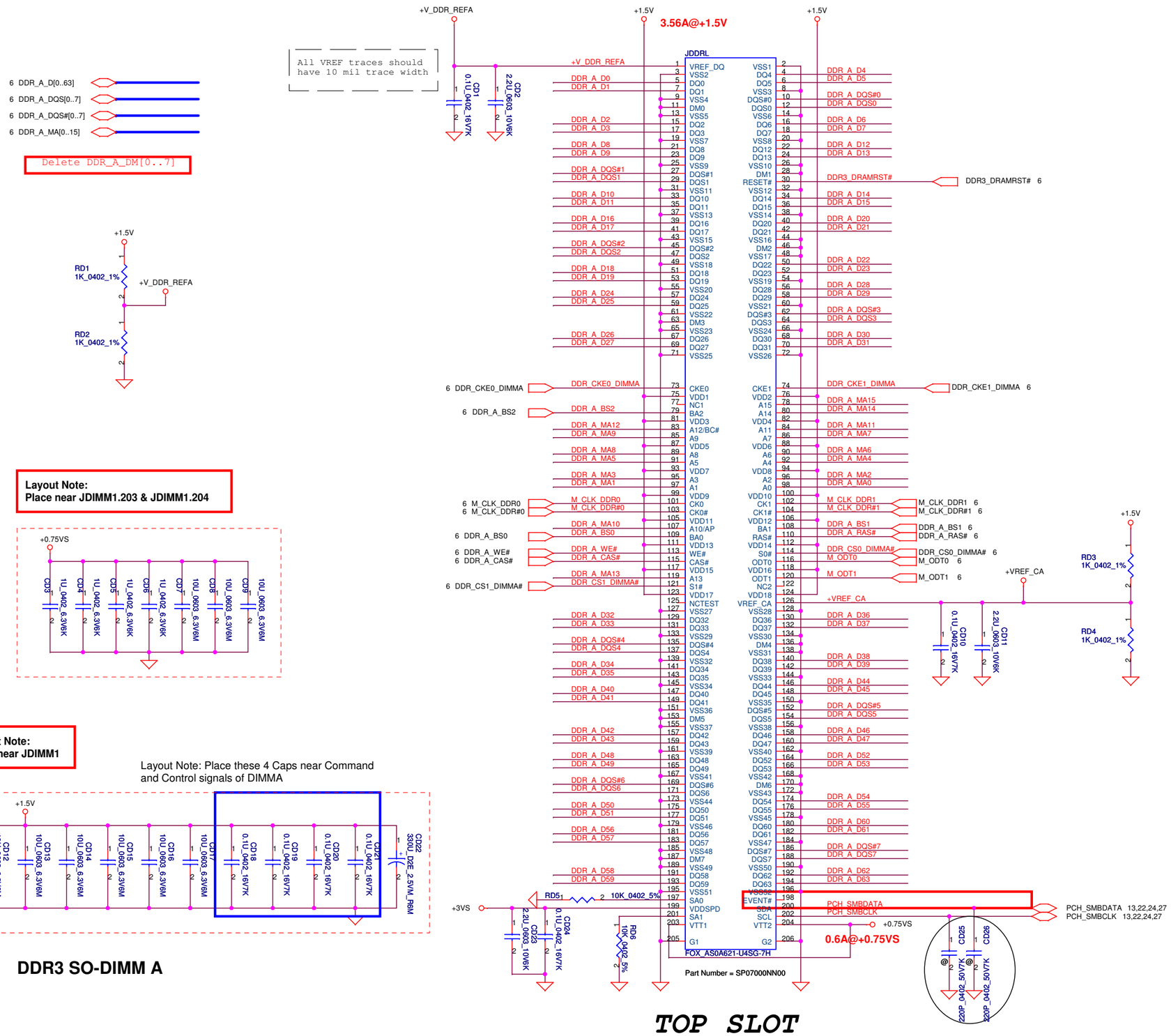
DDR3 SO-DIMM A



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LA-6961P

Title: **DDRIII DIMM**

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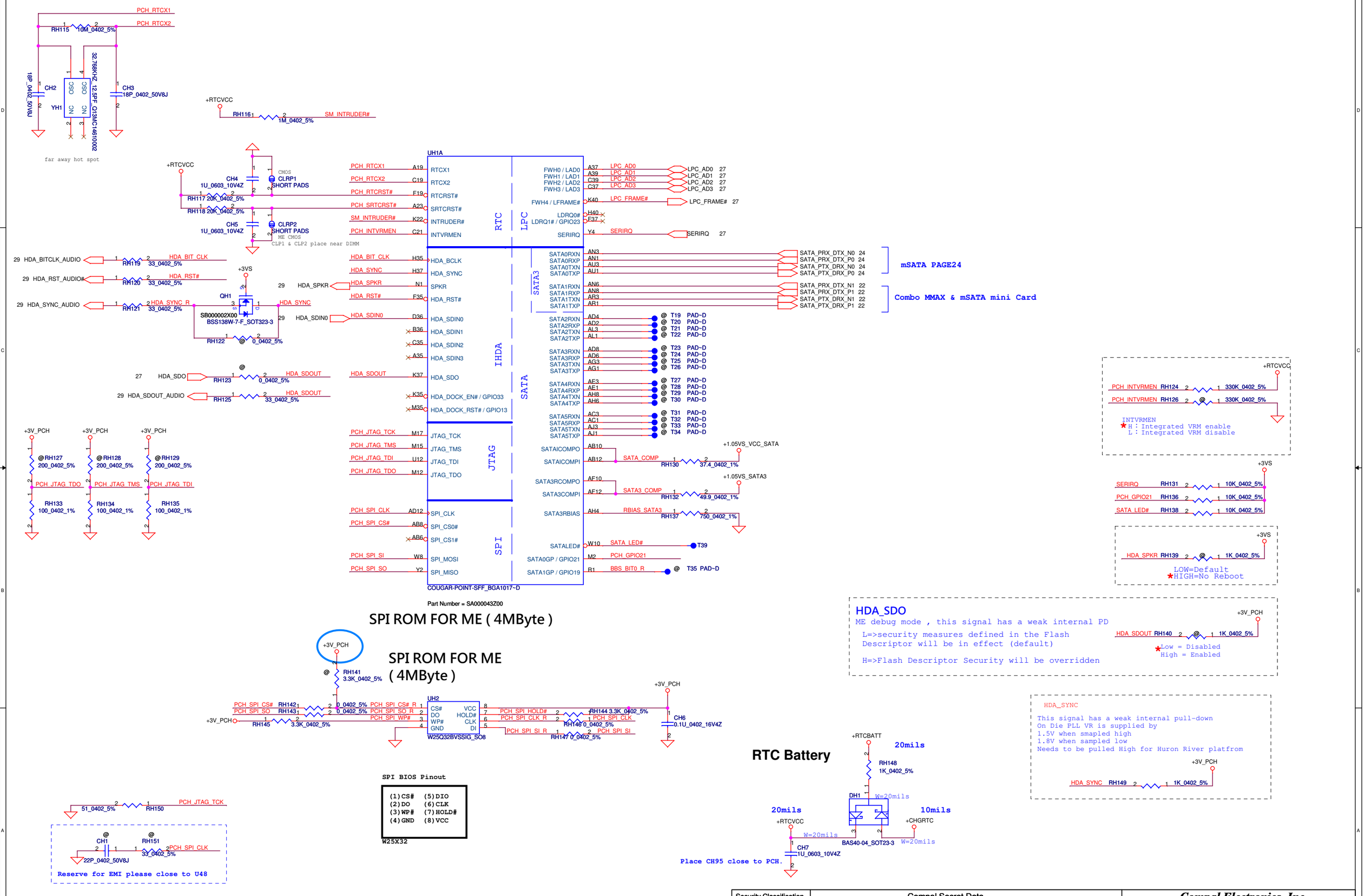

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Title: **PCH (1/8) SATA,HDA,SPI, LPC**

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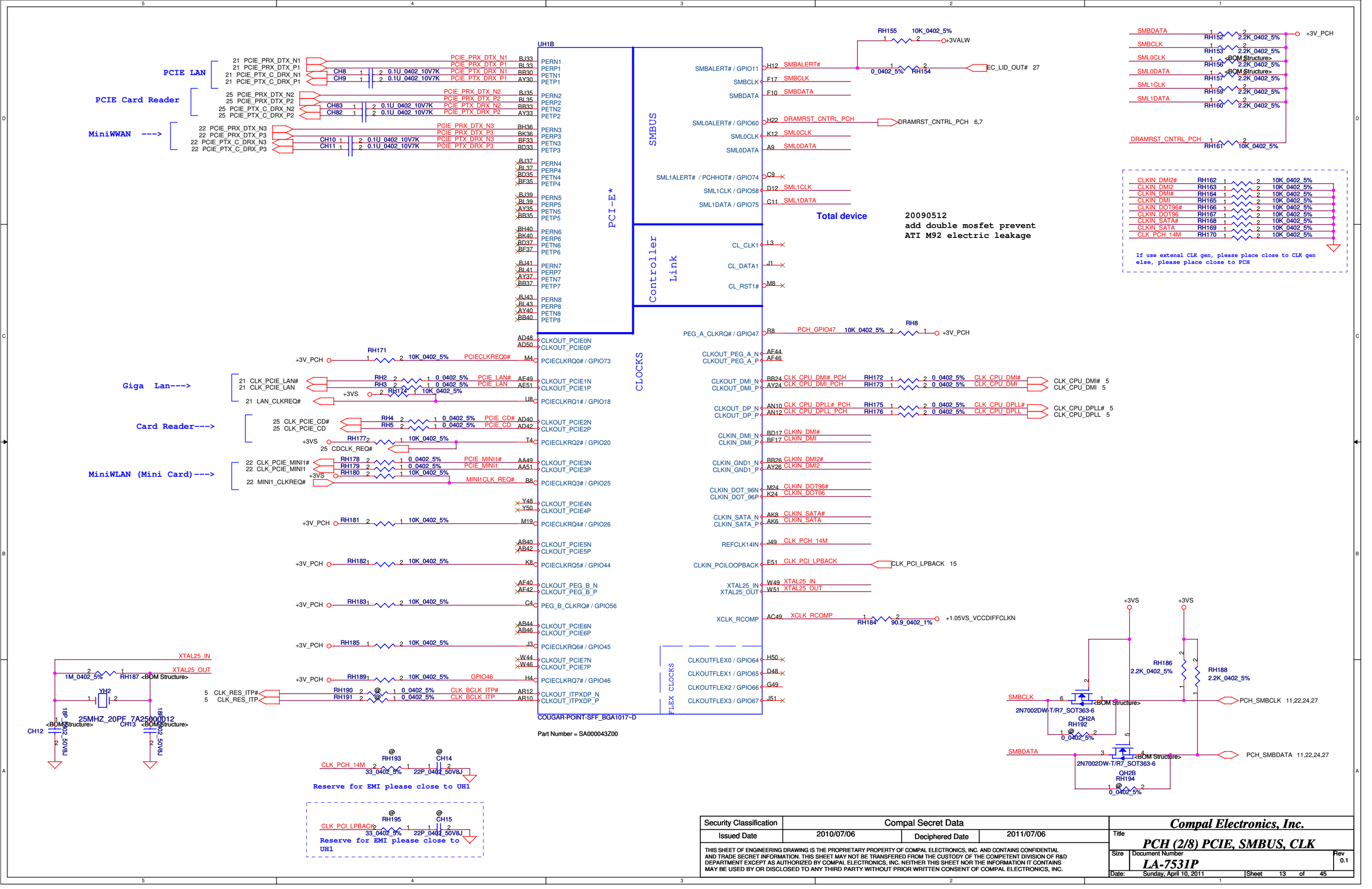

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Title: **PCH (2/8) PCIE, SMBUS, CLK**

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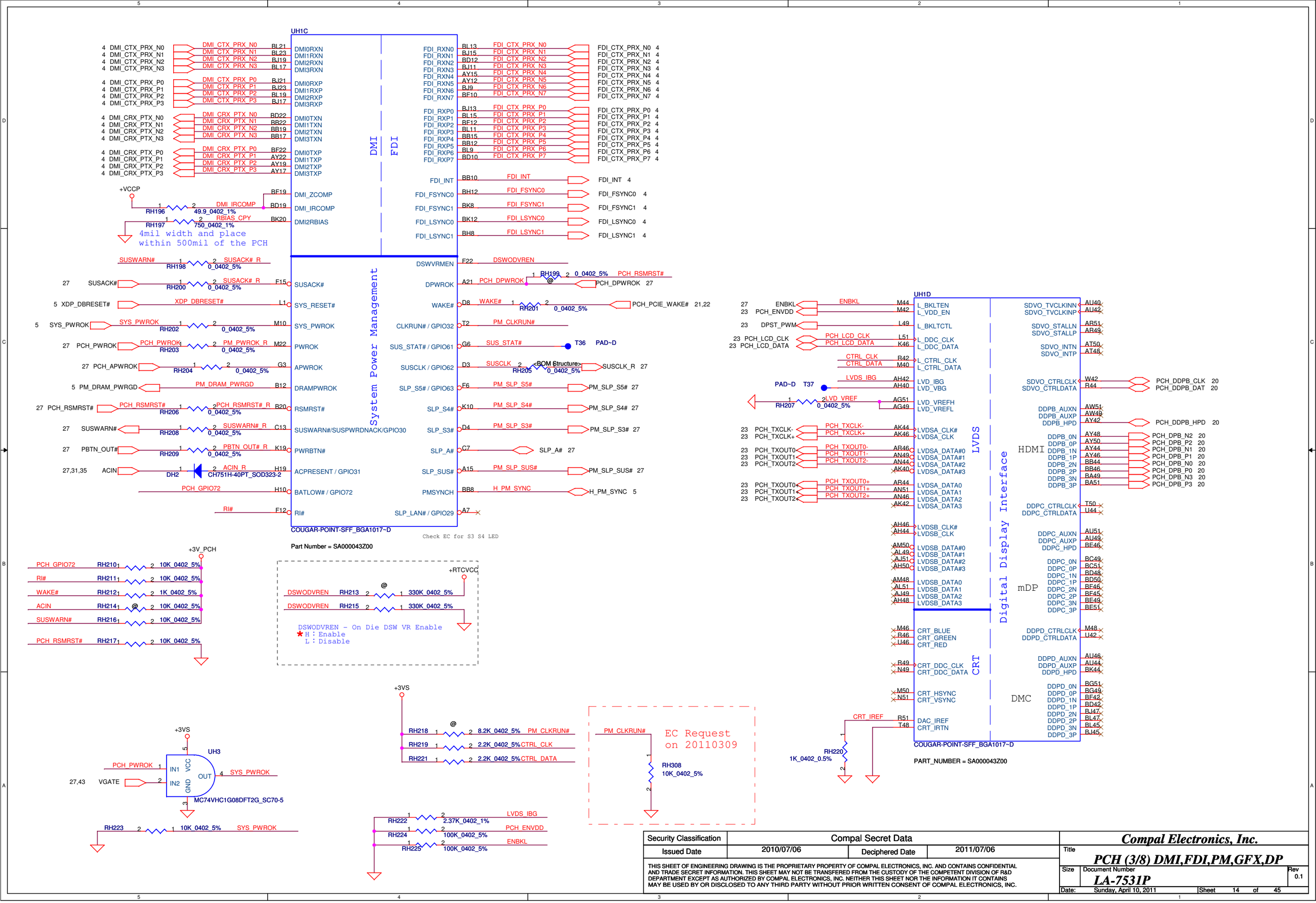

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Title: **PCH (3/8) DMI,FDI,PM,GFX,DP**

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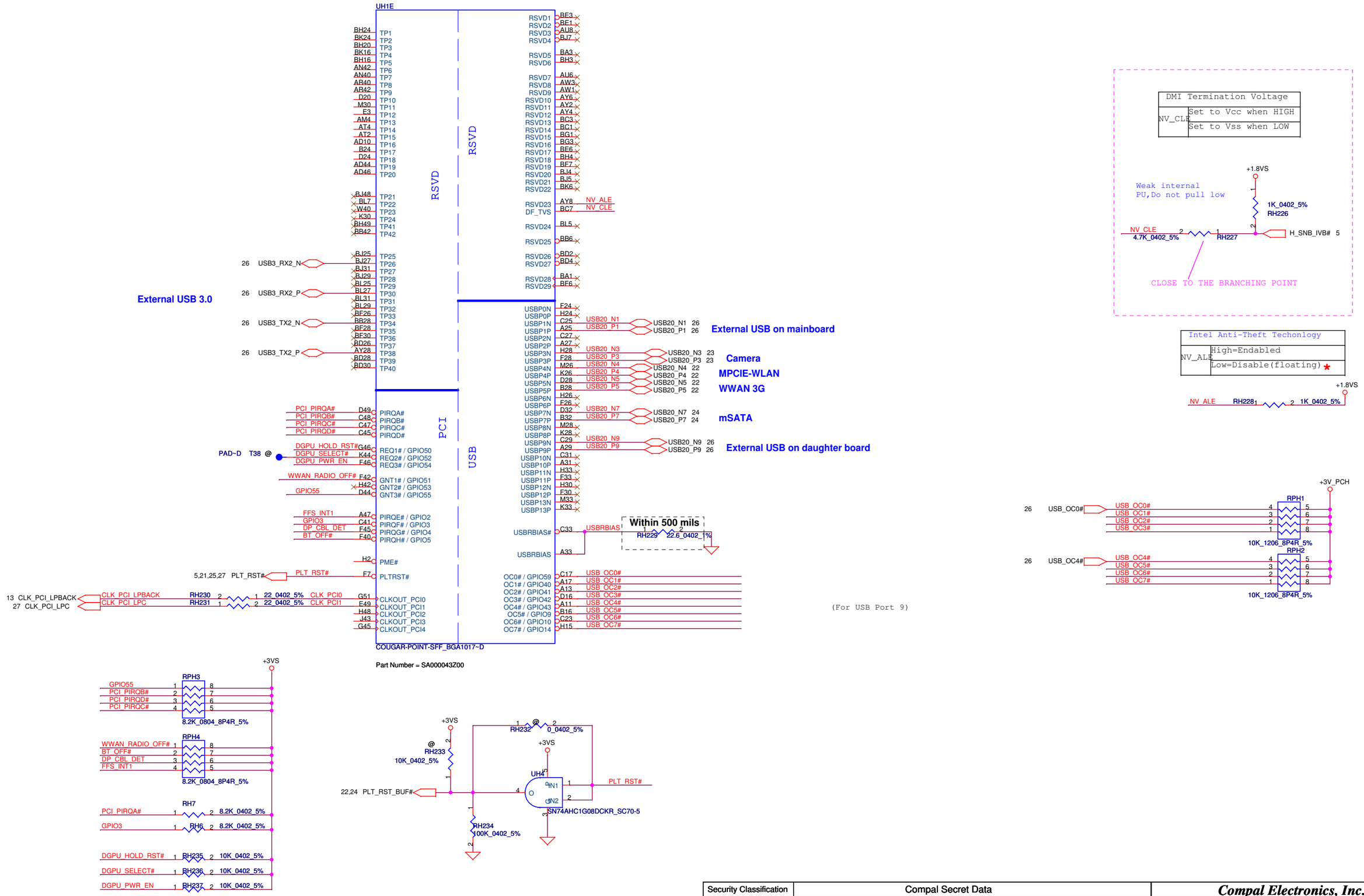

DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

Weak internal PU,Do not pull low

+1.8VS

RH226 1K_0402_5%

NV_CLE 4.7K_0402_5% RH227 H_SNB_IVB# 5

CLOSE TO THE BRANCHING POINT

Intel Anti-Theft Techonlogy	
NV_ALE	High=Endabled
	Low=Disable(floating) *

+1.8VS

NV_ALE RH228 1K_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2010/07/06	Deciphered Date	2011/07/06

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Compal Electronics, Inc.

Title: **PCH (4/8) PCI, USB, NVRAM**

Size: | Document Number: **LA-7531P** | Rev: 0.1

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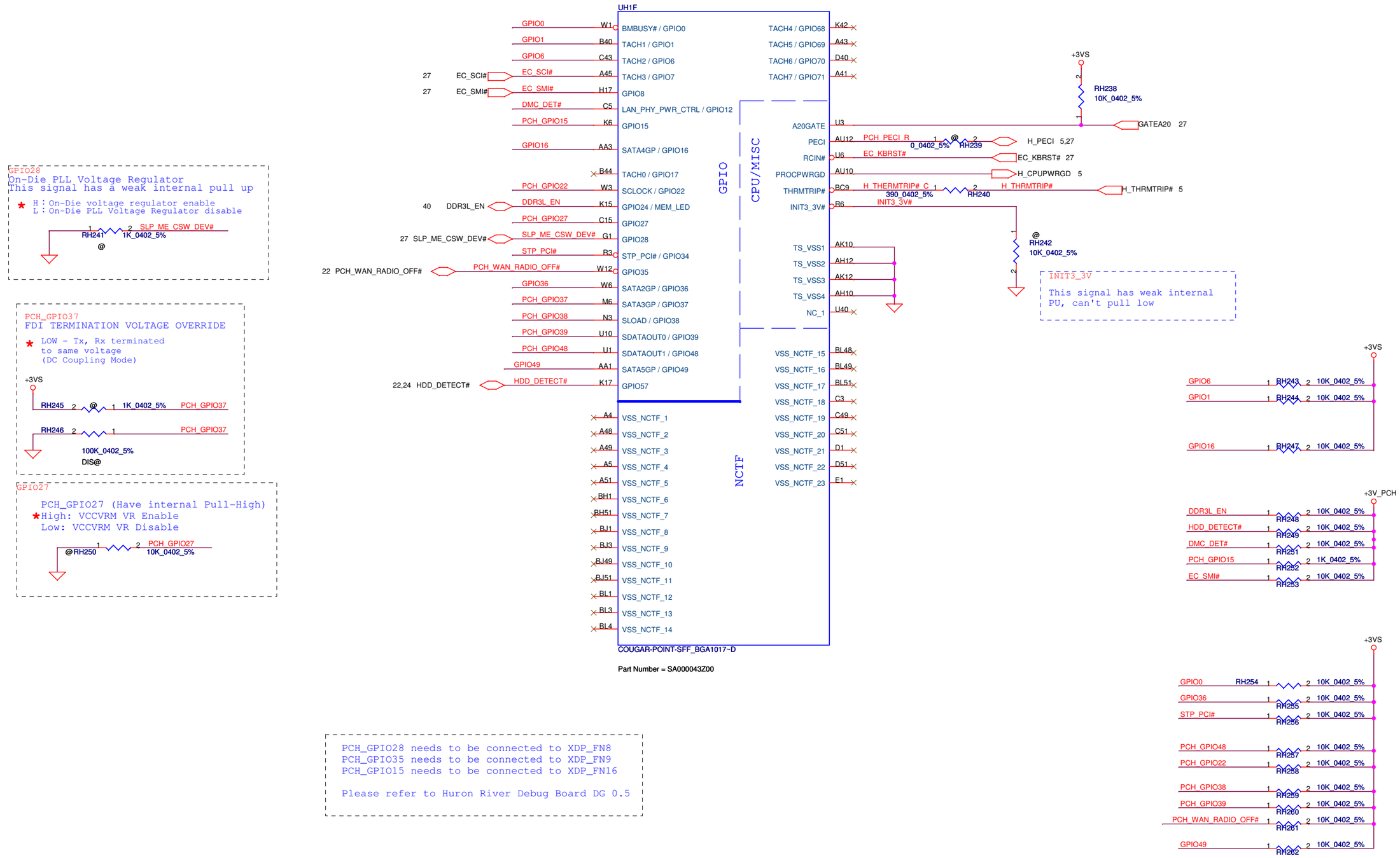

PCH_GPIO28 needs to be connected to XDP_FN8
PCH_GPIO35 needs to be connected to XDP_FN9
PCH_GPIO15 needs to be connected to XDP_FN16

Please refer to Huron River Debug Board DG 0.5

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Issued Date	2010/07/06	Deciphered Date	2011/07/06

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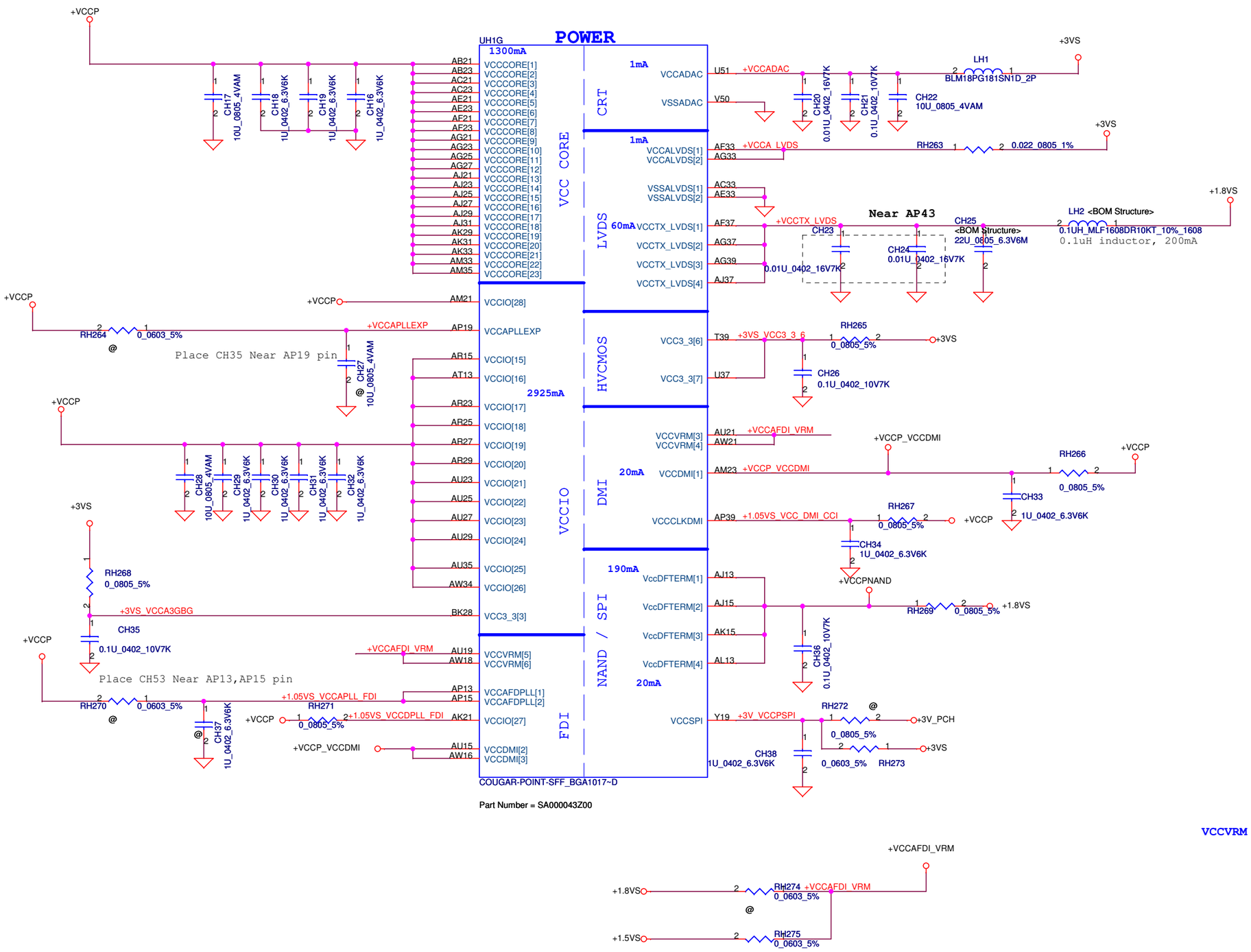
Compal Electronics, Inc.

Title: **PCH (5/8) GPIO, CPU, MISC**

Size: | Document Number: **LA-7531P** | Rev: 0.1

Date: Sunday, April 10, 2011 | Sheet 16 of 45



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

VCCVRM = 160mA detal waiting for newest spec

5/18 modified

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Compal Electronics, Inc.

Title: PCH (6/8) PWR

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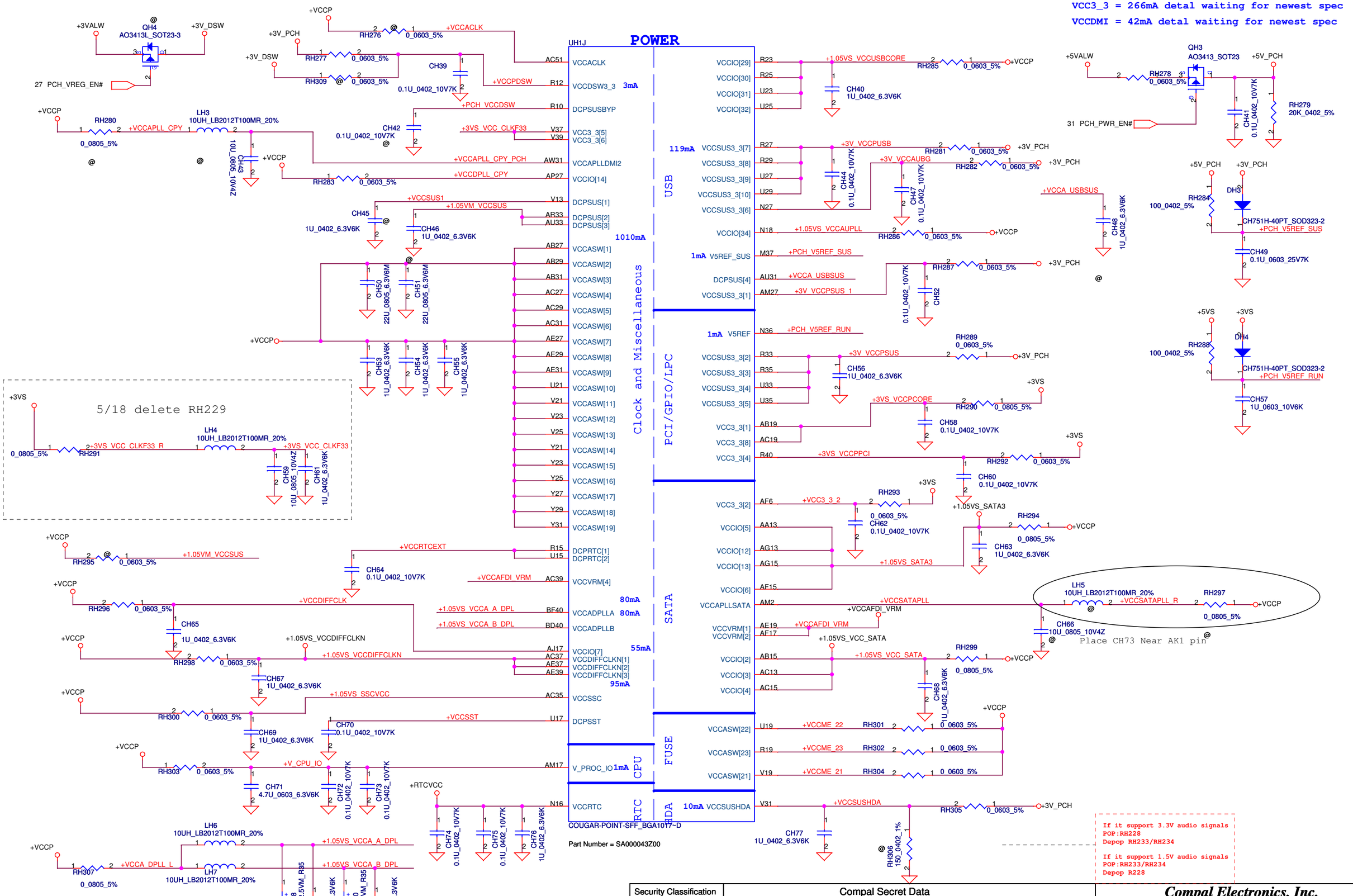
Date: Thursday, April 07, 2011 | Sheet 17 of 45

VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec



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Issued Date	2010/07/06	Deciphered Date	2011/07/06

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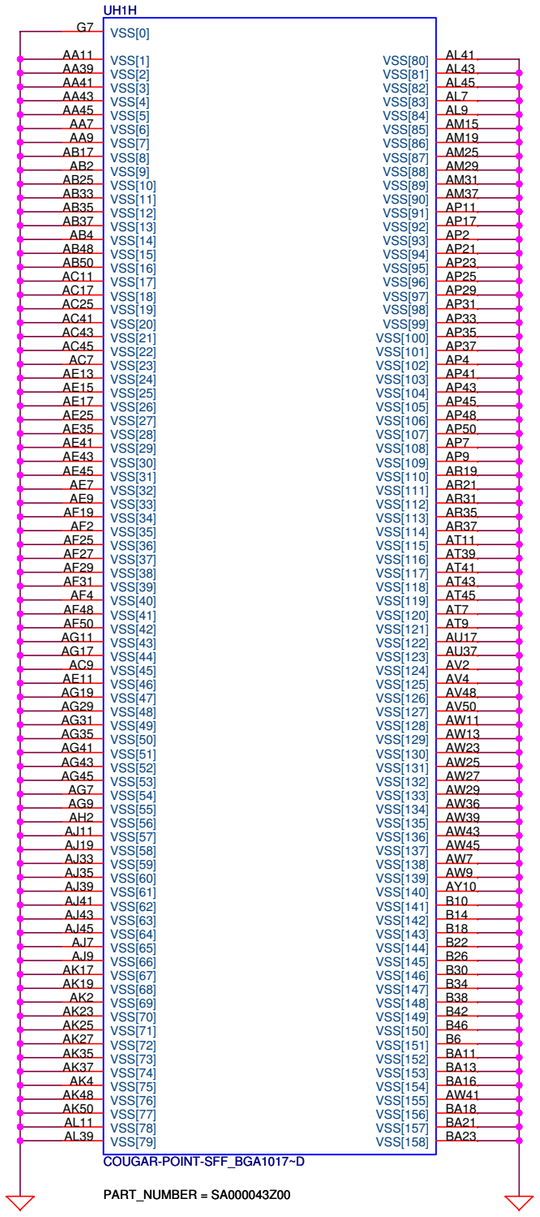
Compal Electronics, Inc.

Title: **PCH (7/8) PWR**

Size | Document Number: **LA-7531P** | Rev: 0.1

Date: Sunday, April 10, 2011 | Sheet 18 of 45



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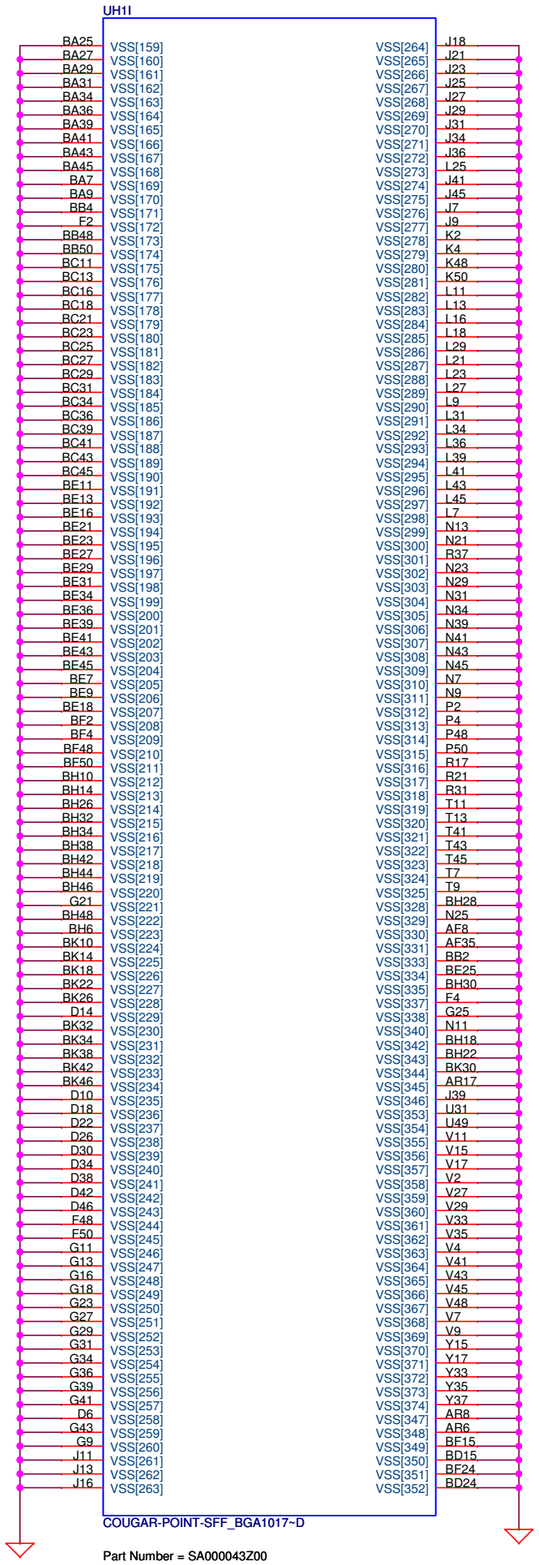

Part Number = SA000043Z00

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Issued Date	2010/07/06	Deciphered Date	2011/07/06

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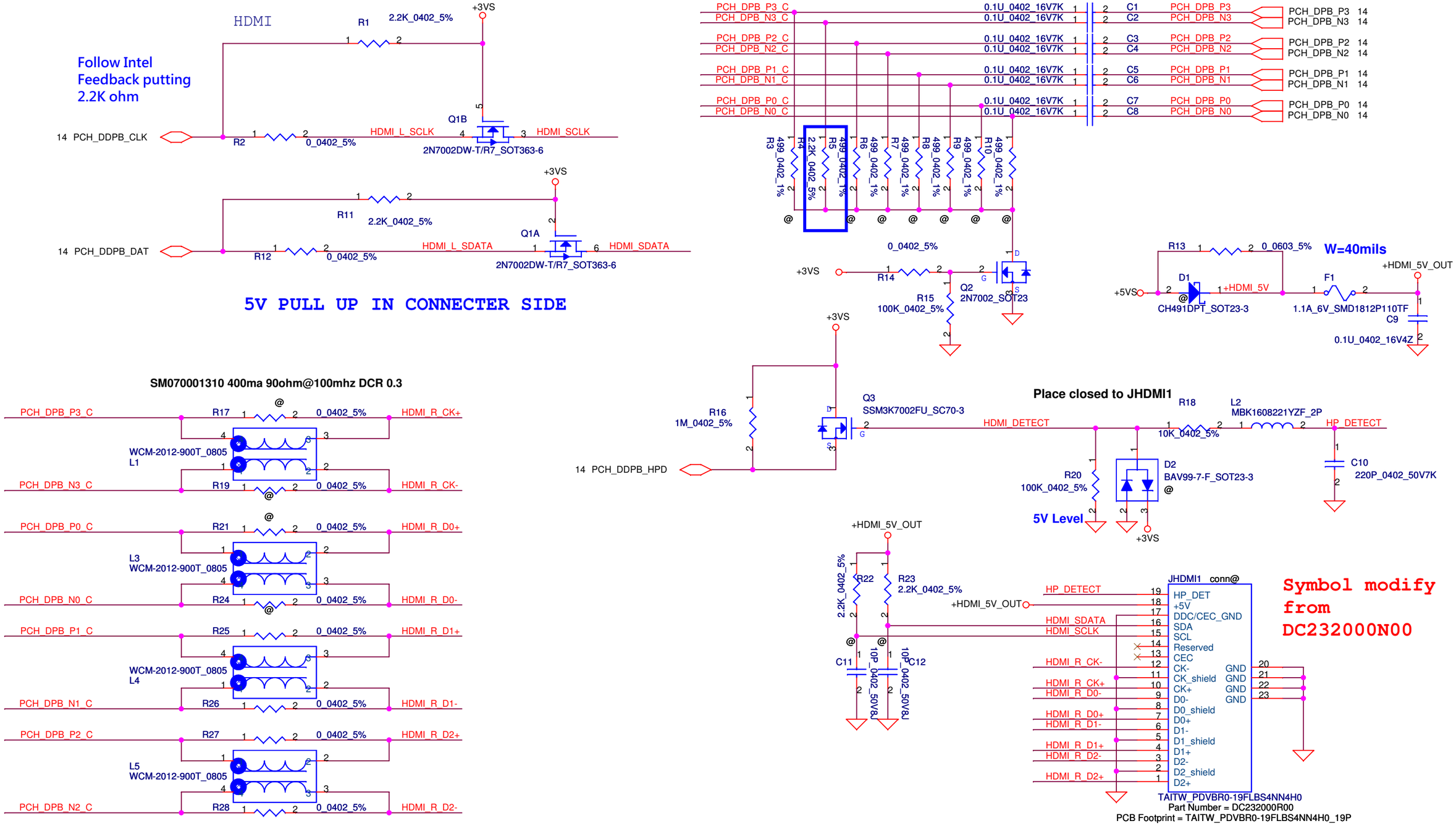
Compal Electronics, Inc.

Title: **PCH (8/8) VSS**

Size | Document Number: **LA-7531P** | Rev: 0.1

Date: Thursday, April 07, 2011 | Sheet 19 of 45



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Issued Date	2010/07/06	Deciphered Date	2011/07/06

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Compal Electronics, Inc.

Title: **HDMI Conn**

Size | Document Number: **LA-7531P** | Rev 0.1

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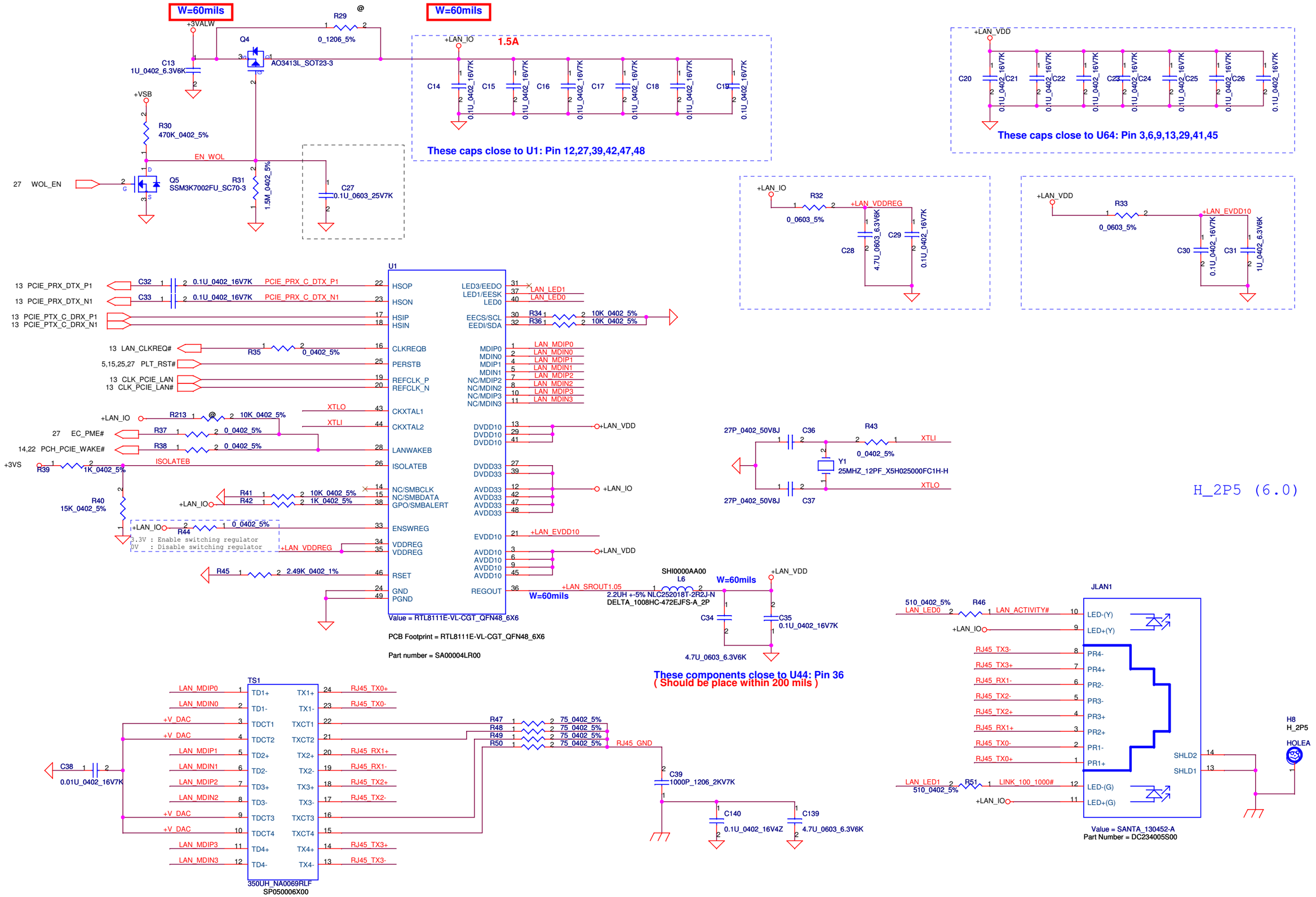

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Compal Electronics, Inc.

Title: **LAN Realtek RTL8111E**

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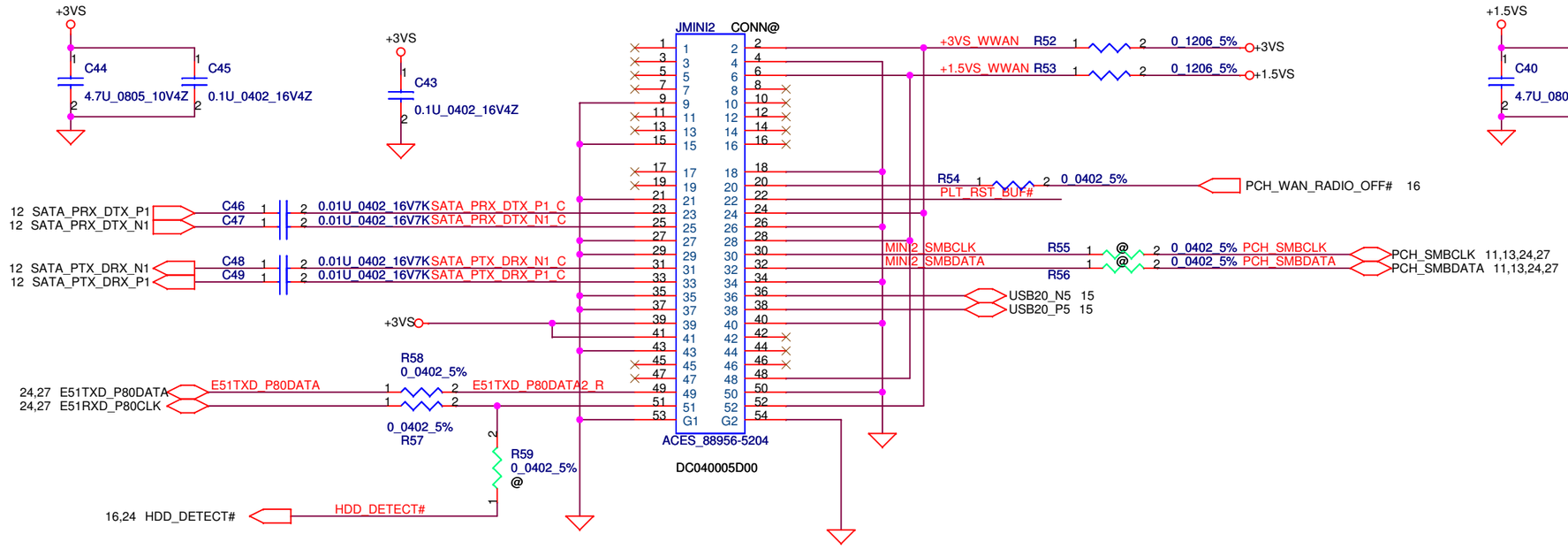
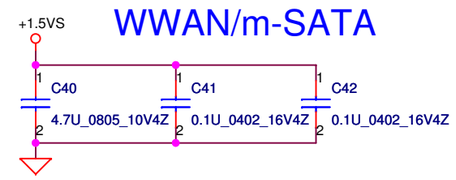
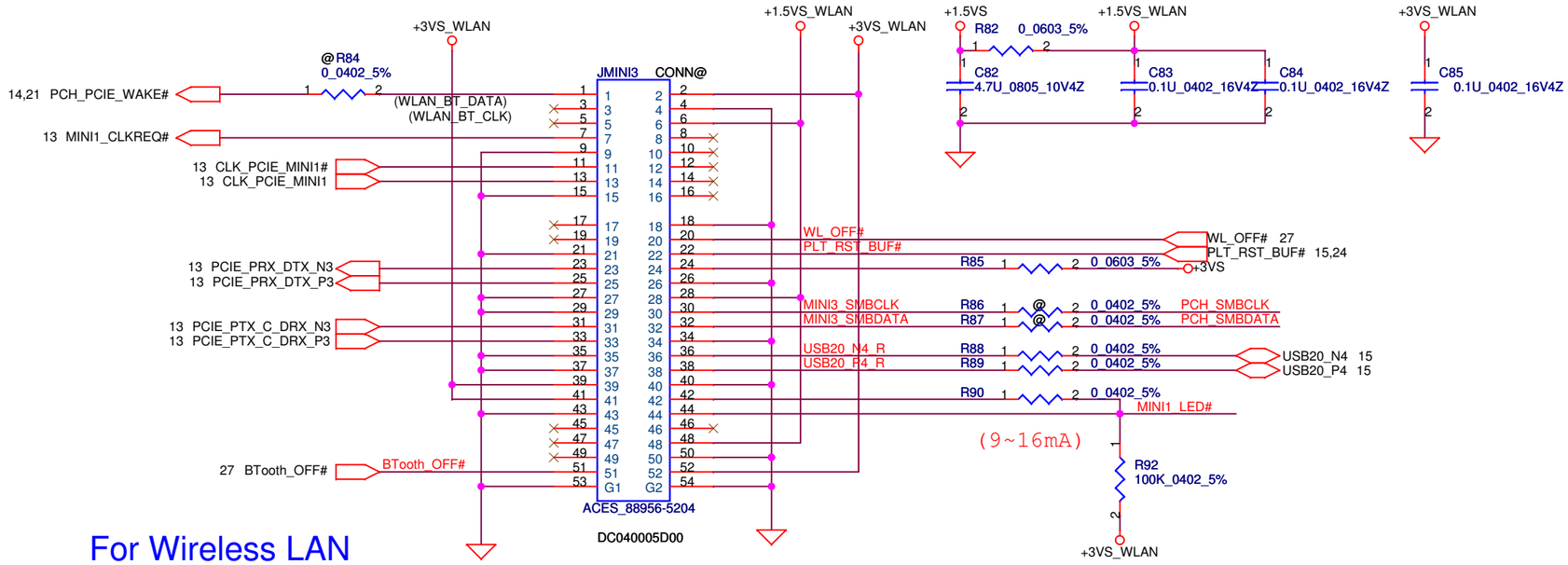
WWAN/m-SATA

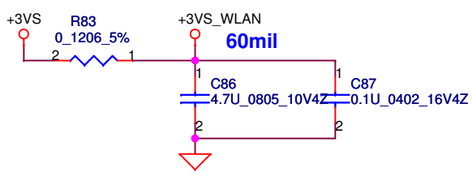






Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

For Wireless LAN



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Compal Electronics, Inc.

Title: **MiniCard WWAN & WLan**

Size | Document Number: **LA-7531P** | Rev: 0.1

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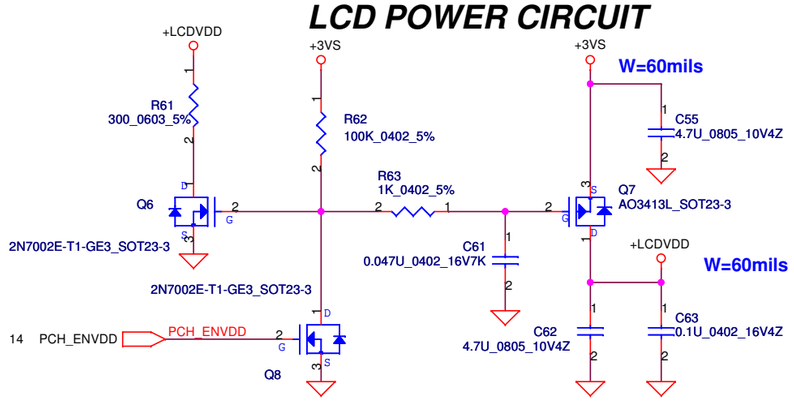
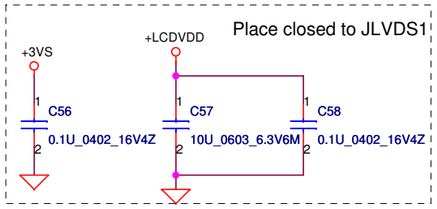
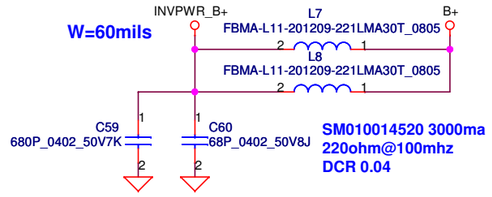
LCD POWER CIRCUIT

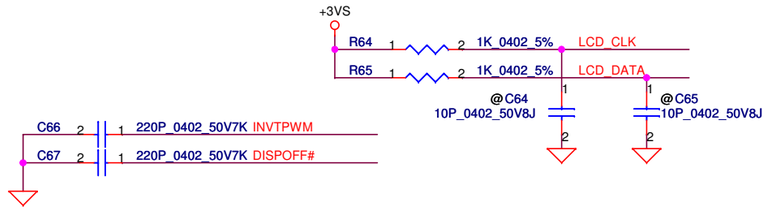


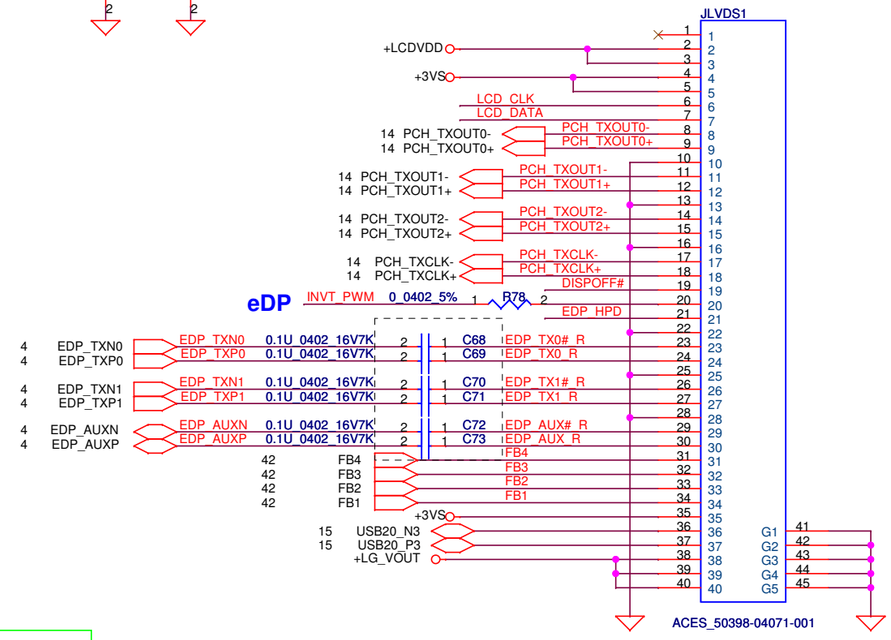




LCD/LED PANEL Conn.

W=60mils W=60mils





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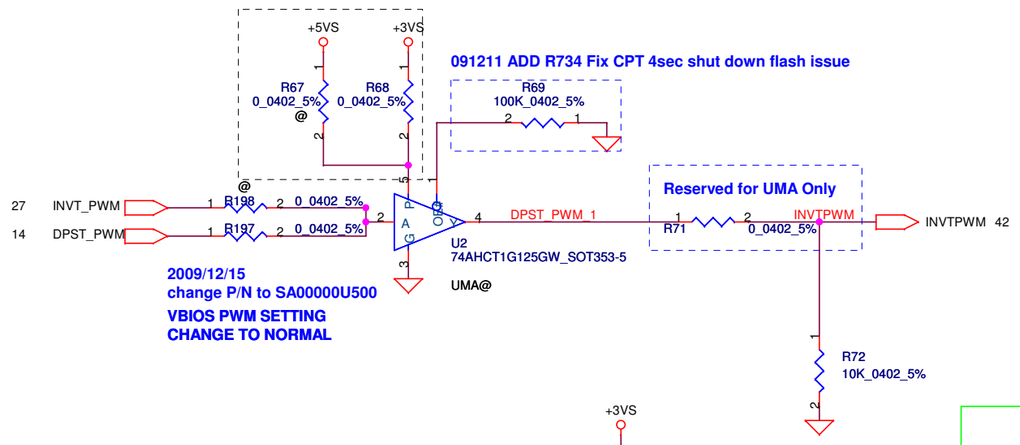
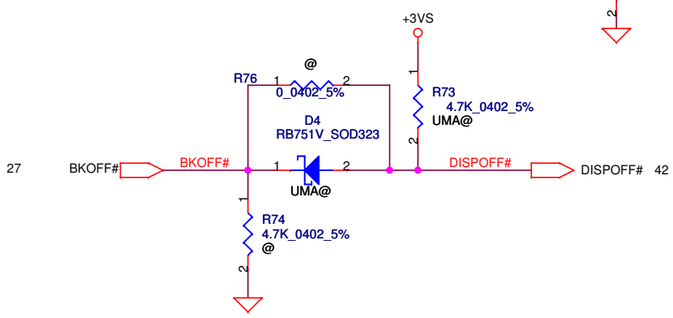
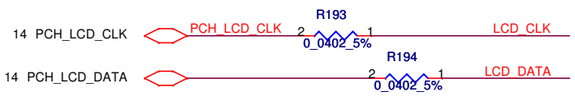
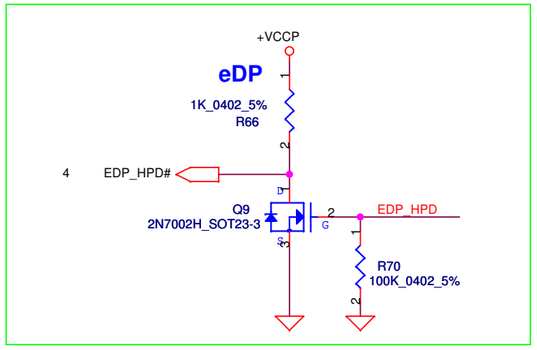
Part Number = SP010013I00









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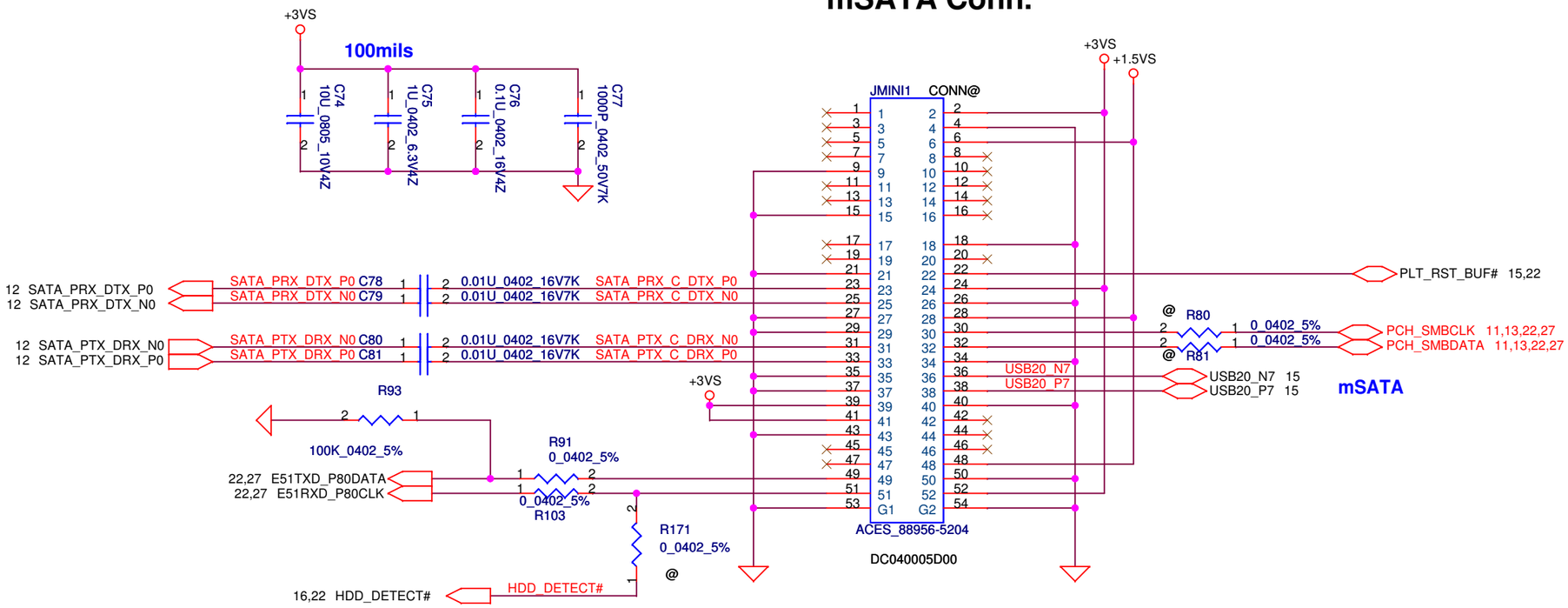
Compal Electronics, Inc.

Title: **LVDS Connector**

Size | Document Number: **LA-7531P** | Rev 0.1

Date: Sunday, April 10, 2011 | Sheet 23 of 45

mSATA Conn.



Security Classification	Compal Secret Data		
Issued Date	2010/04/26	Deciphered Date	2010/05/28

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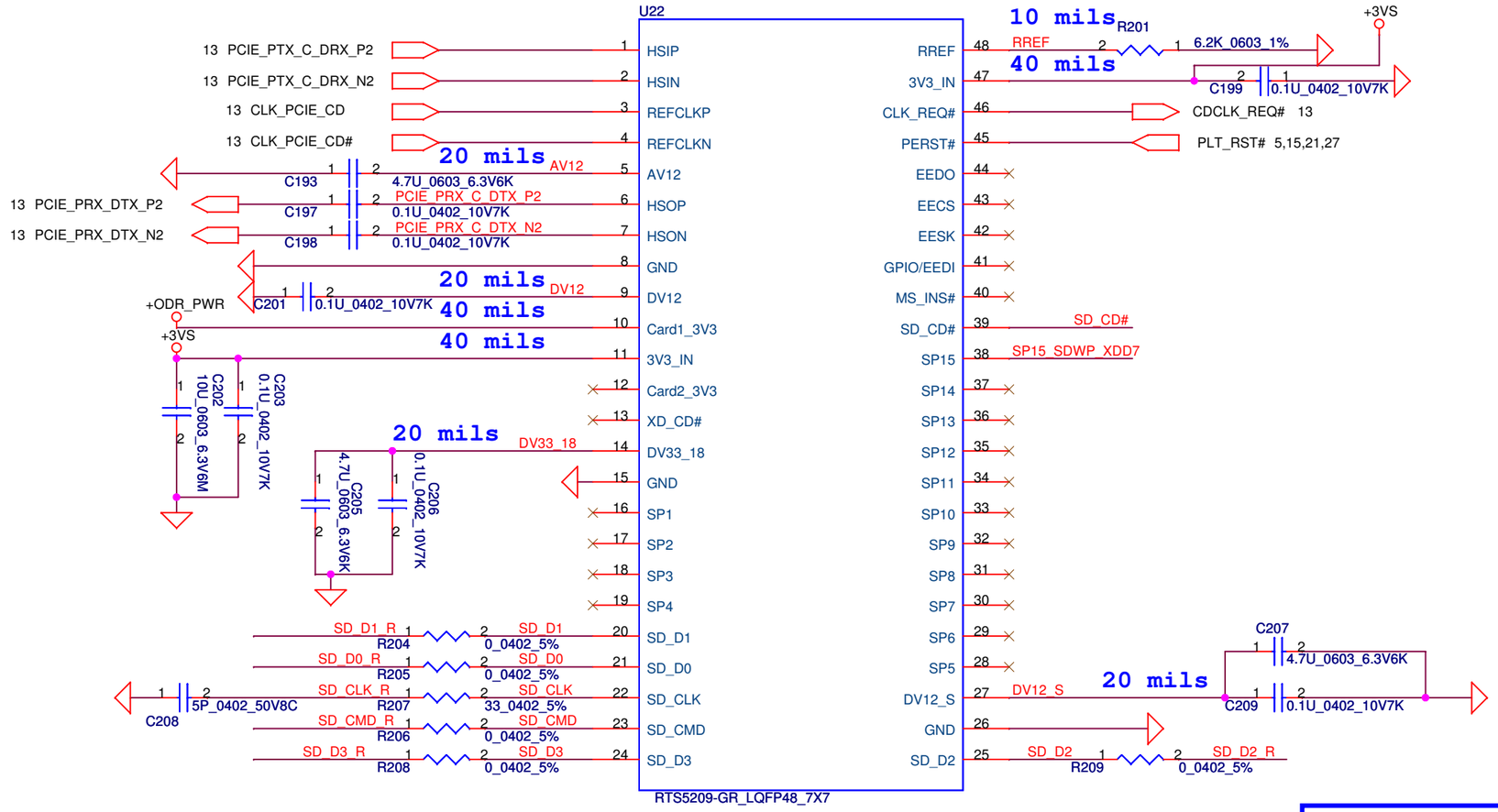
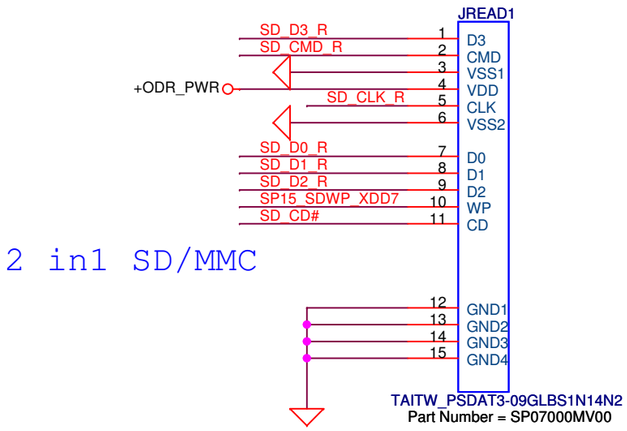
Compal Electronics, Inc.

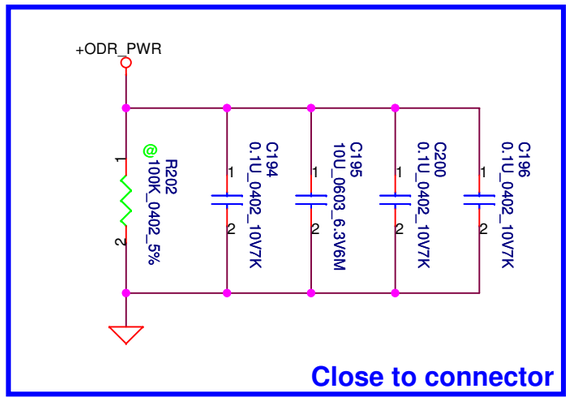
Title: mSATA Connector

Size: B | Document Number: LA-7531P | Rev: 0.1

Date: Sunday, April 10, 2011 | Sheet 24 of 45







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Issued Date	2010/04/26	Deciphered Date	2010/05/28

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Compal Electronics, Inc.

Title: Empty

Size: B | Document Number: LA-7531P | Rev: 0.1

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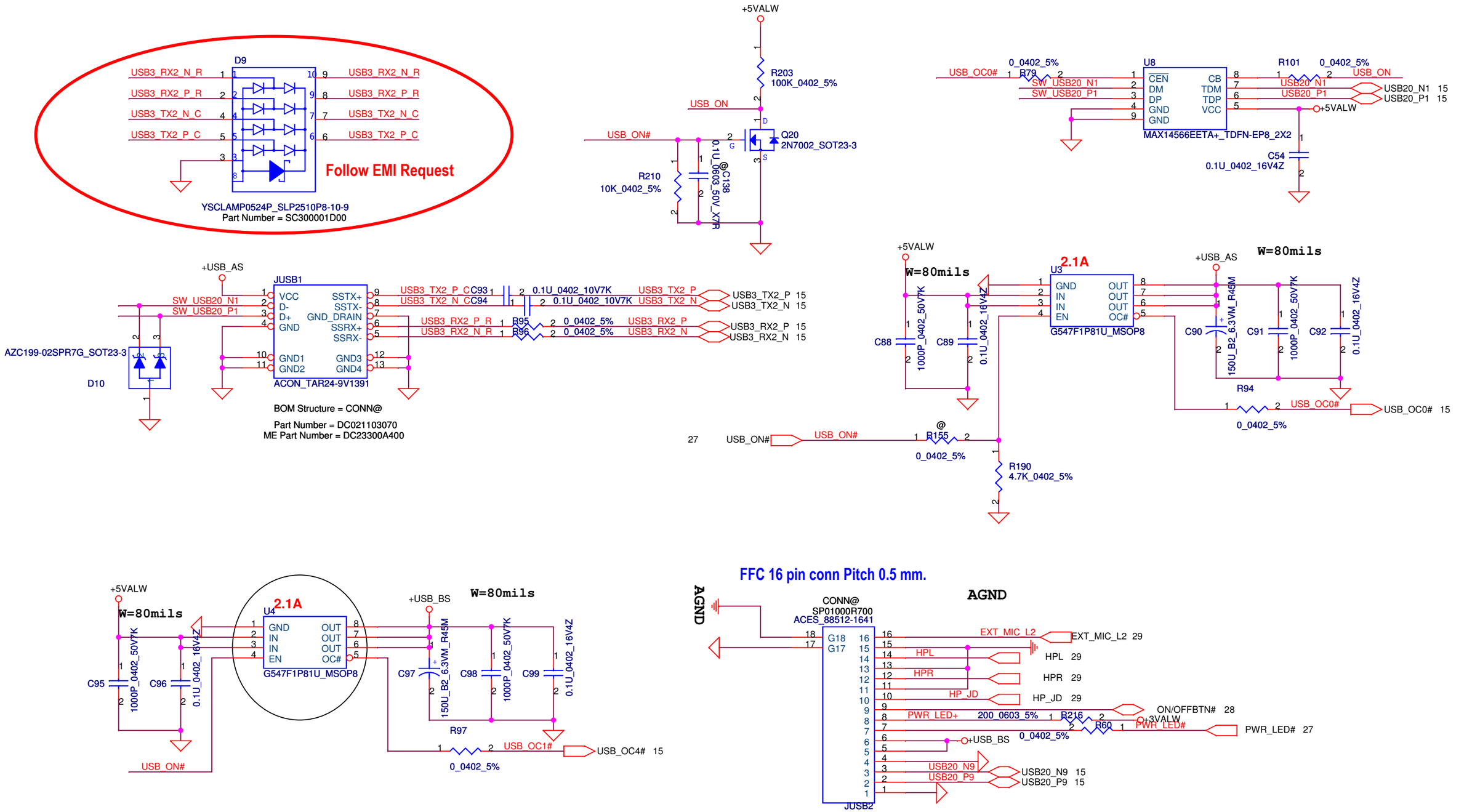

Security Classification	Compal Secret Data		
Issued Date	2010/04/26	Deciphered Date	2010/05/28

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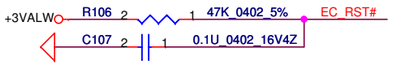
Compal Electronics, Inc.

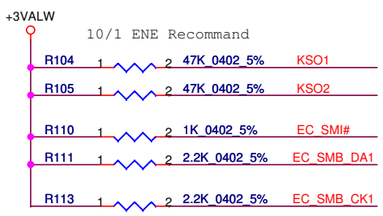
Title: USB Con & Daughter Con

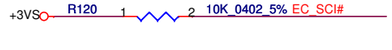
Size: B | Document Number: LA-7531P | Rev: 0.1

Date: Sunday, April 10, 2011 | Sheet 26 of 45

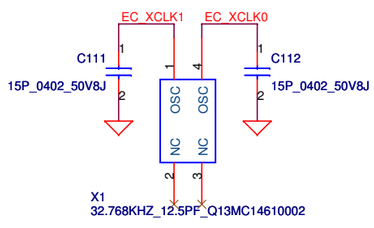
2011/04/09

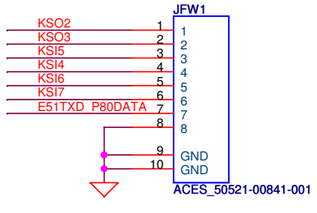






To prevent debug card unwork issue.





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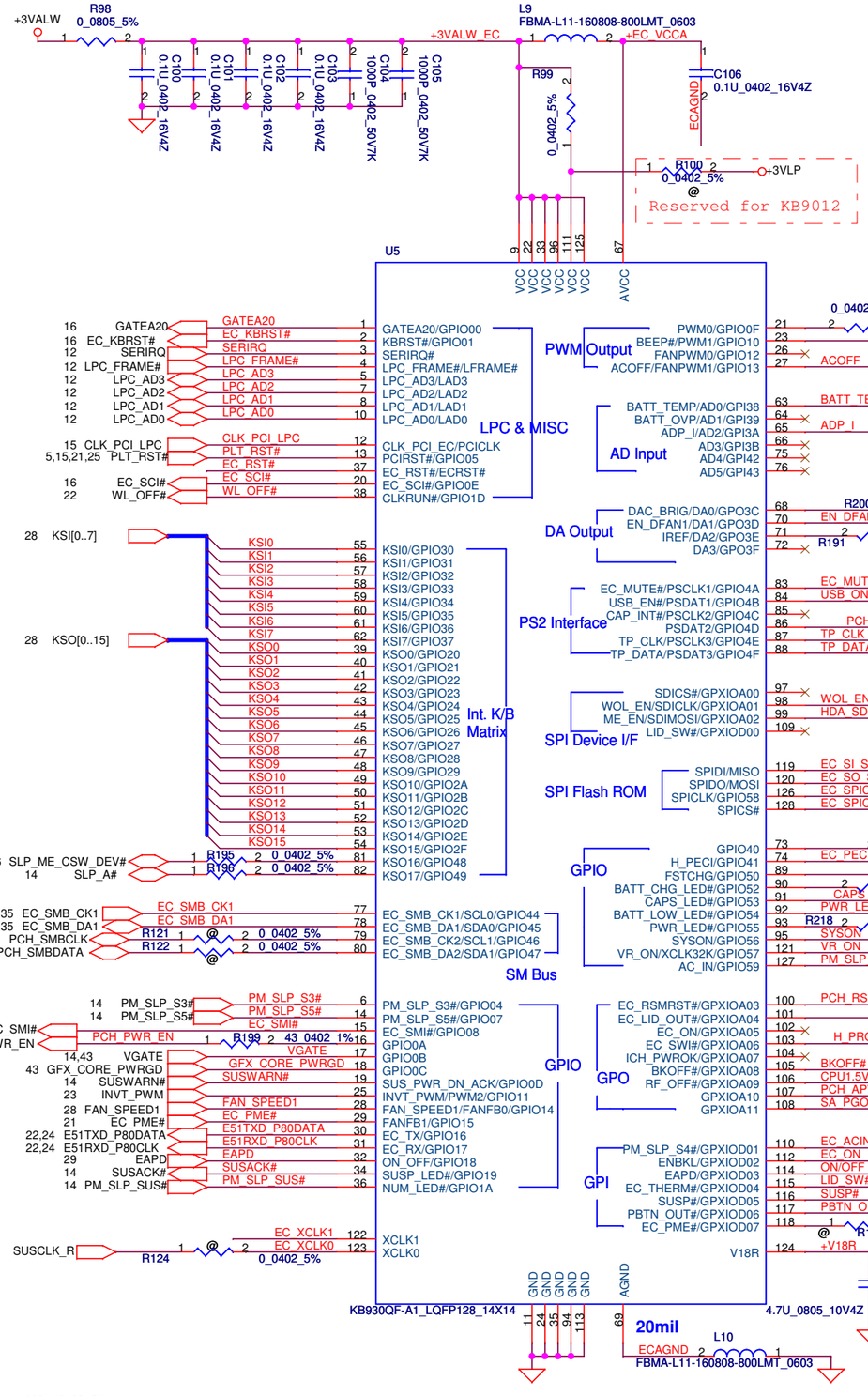
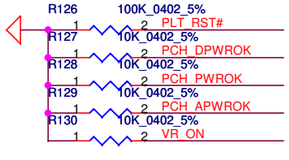
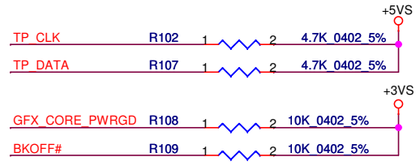


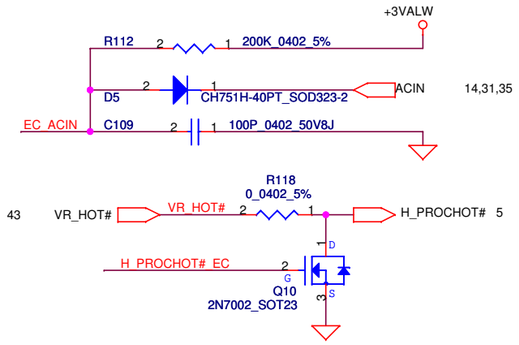
Reserved for KB9012

Co-lay KB930/KB9012 PECI

	Stuff
KB930	R119
KB9012	R123







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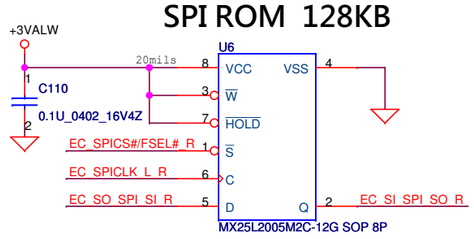
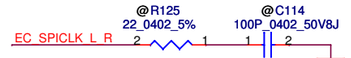


SA00002C100 (S IC FL 1MB MX25L1005AMC-12G SOP 8P 3.3V)



Reserve for EMI please close to U64

Security Classification	Compal Secret Data		
Issued Date	2010/04/26	Deciphered Date	2010/05/28

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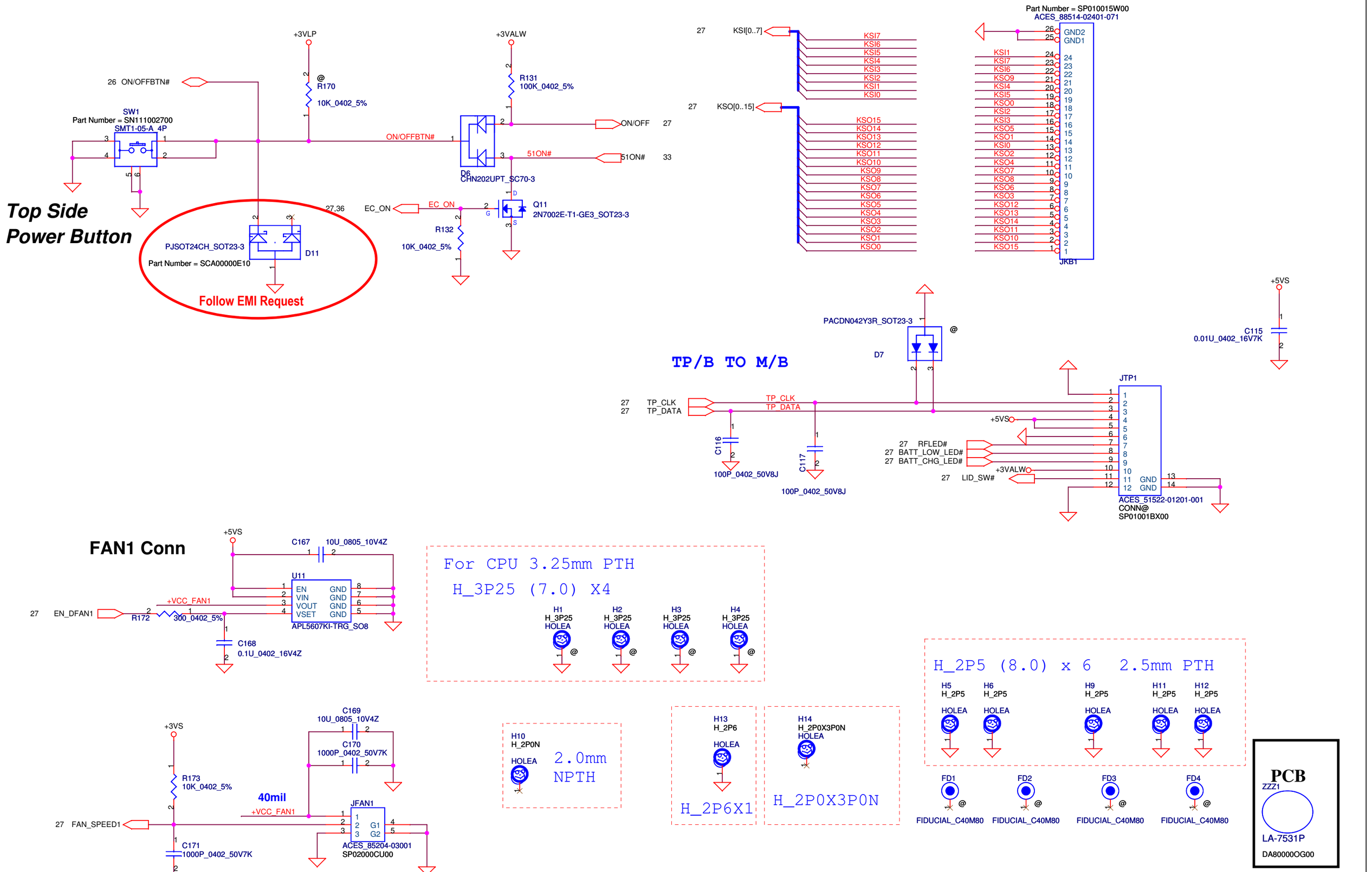
Compal Electronics, Inc.

Title: EC ENE-KB930 & 9012

Size: Custom | Document Number: LA-7531P | Rev: 0.1

Date: Sunday, April 10, 2011 | Sheet 27 of 45



Security Classification	Compal Secret Data		
Issued Date	2010/04/26	Deciphered Date	2010/05/28

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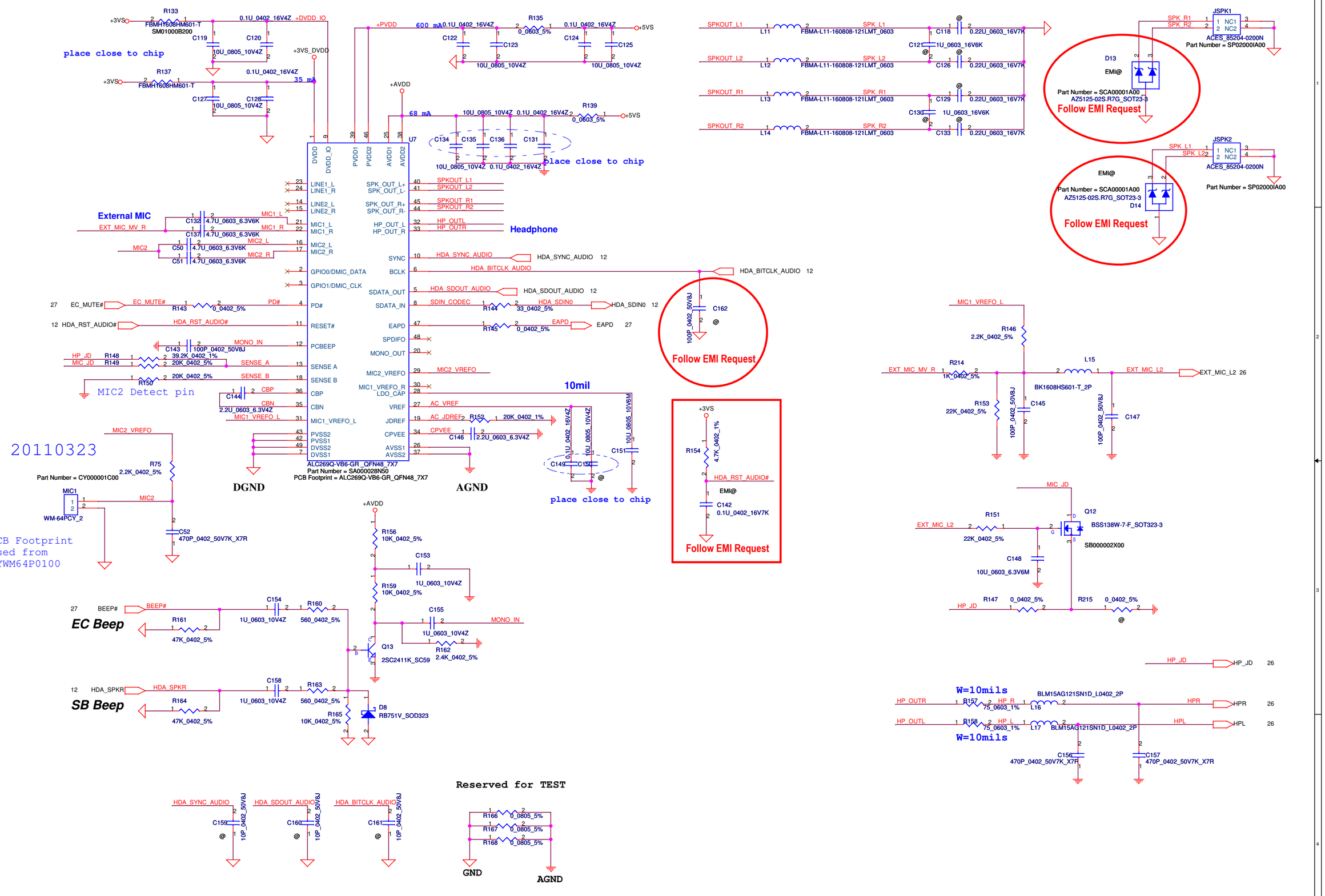
Compal Electronics, Inc.

Title: BIOS, I/O Port & K/B Connector

Size: A3 | Document Number: LA-7531P | Rev: 0.1

Date: Sunday, April 10, 2011 | Sheet 28 of 45



Security Classification	Compal Secret Data		
Issued Date	2010/04/26	Deciphered Date	2010/05/28

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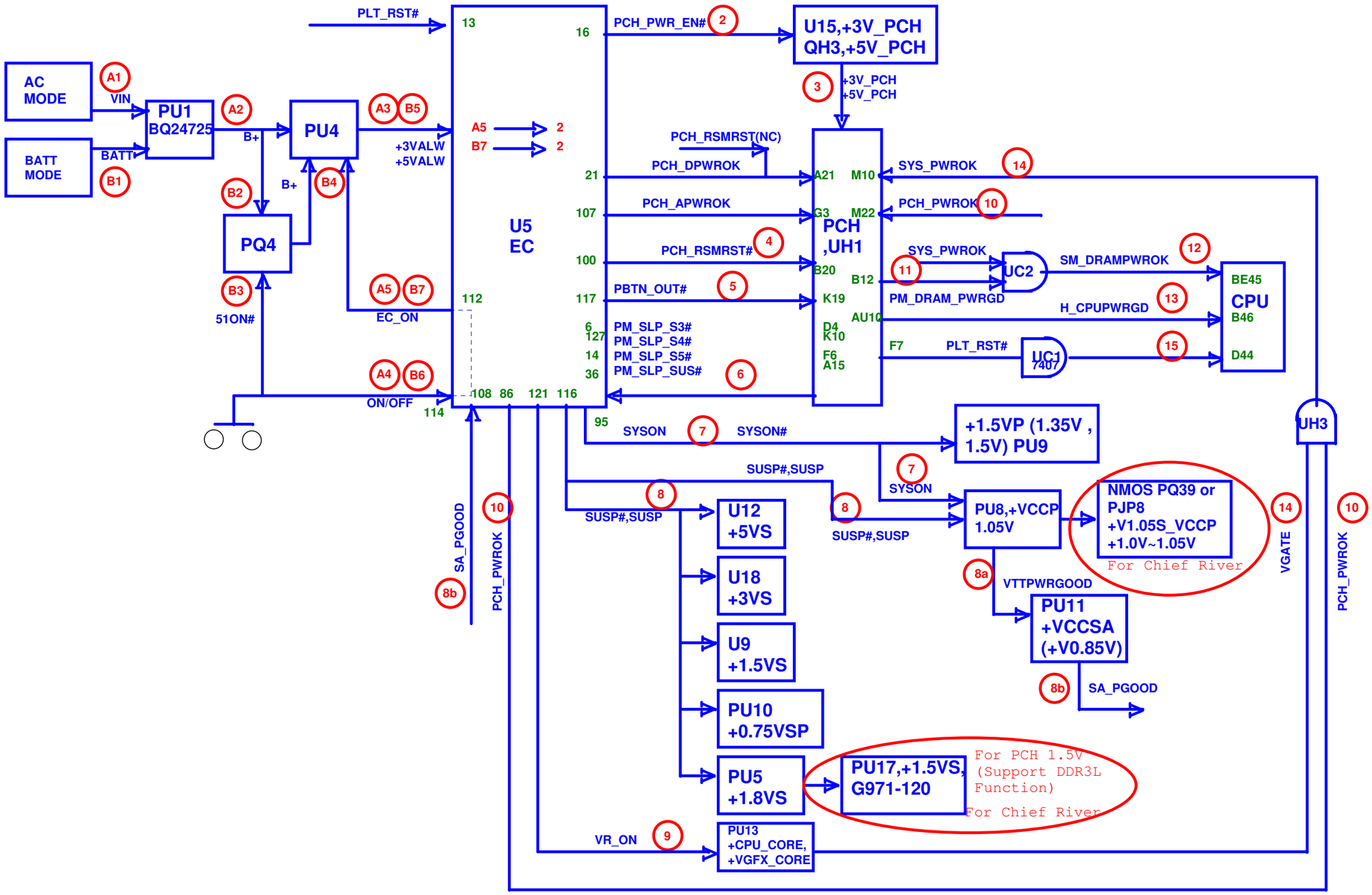
Compal Electronics, Inc.

Title: HD AUDIO CODEC ALC269

Size: C | Document Number: LA-7531P | Rev: 0.1

Date: Sunday, April 10, 2011 | Sheet 29 of 45

LA-7531P Power Sequence 2011/04/10



Security Classification	Compal Secret Data		
Issued Date	2010/04/26	Deciphered Date	2010/05/28

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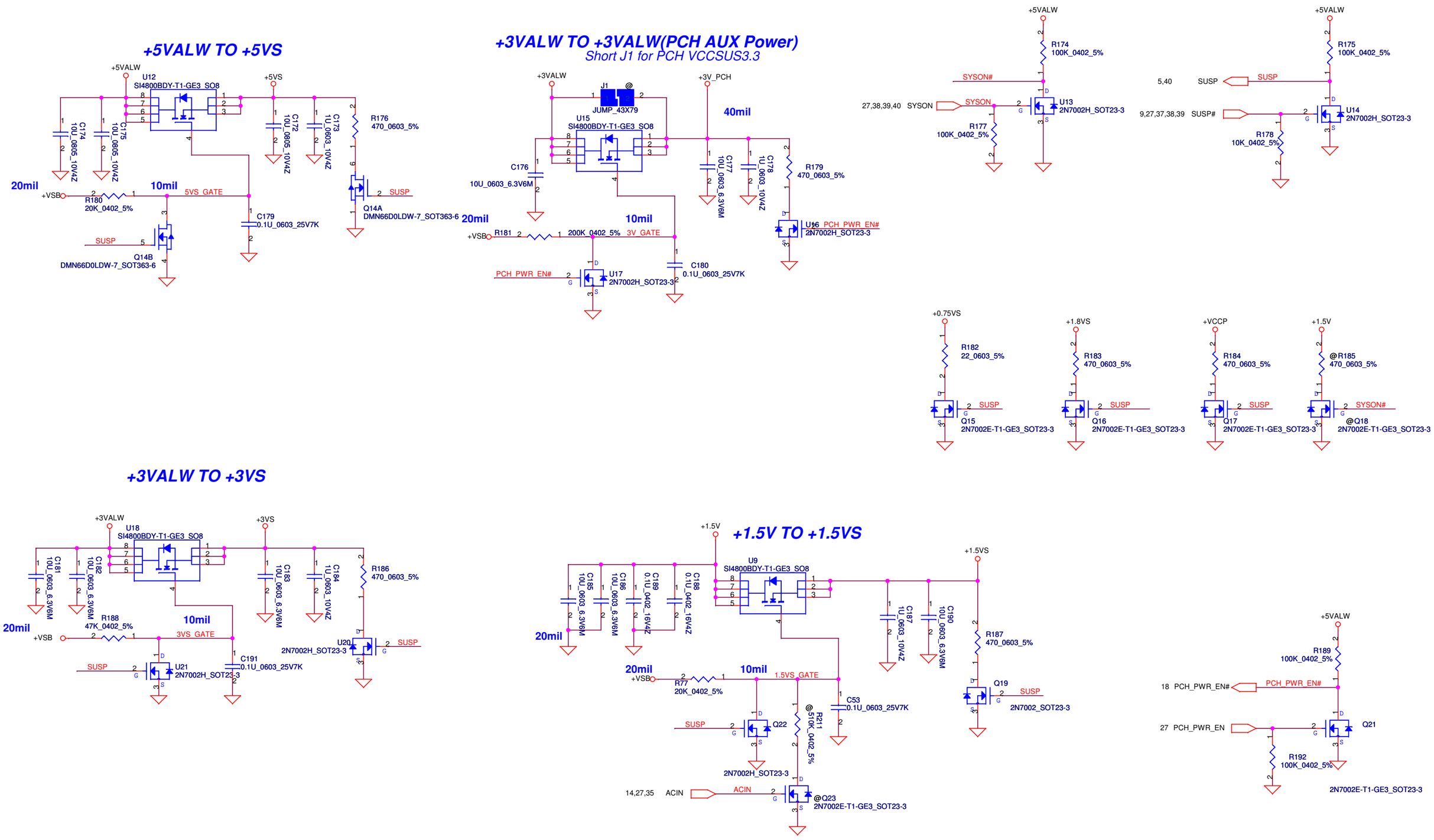
Compal Electronics, Inc.

Title: Power Sequence

Size: Custom | Document Number: LA-7531P | Rev: 0.1

Date: Sunday, April 10, 2011 | Sheet 30 of 45



Security Classification	Compal Secret Data		
Issued Date	2010/04/26	Deciphered Date	2010/05/28

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Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: LA-7531P | Rev: 0.1

Date: Sunday, April 10, 2011 | Sheet 31 of 45

Version Change List (P. I. R. List) Page 1

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	xx	xxx	2011/02/XX	XXXX XXXX	XXXX		Rev01

2

Security Classification	Compal Secret Data		
Issued Date	2010/04/26	Deciphered Date	2010/05/28

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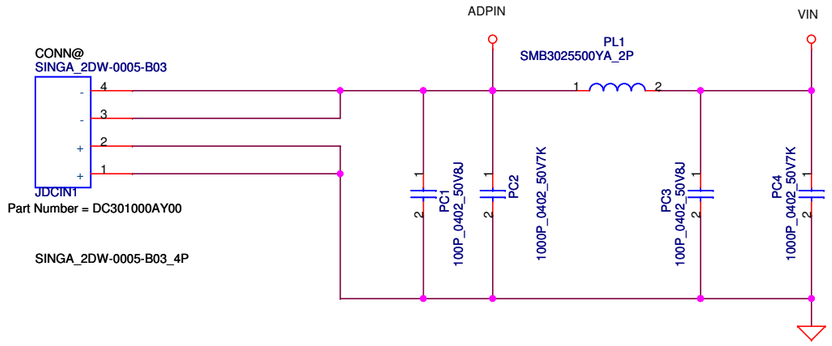
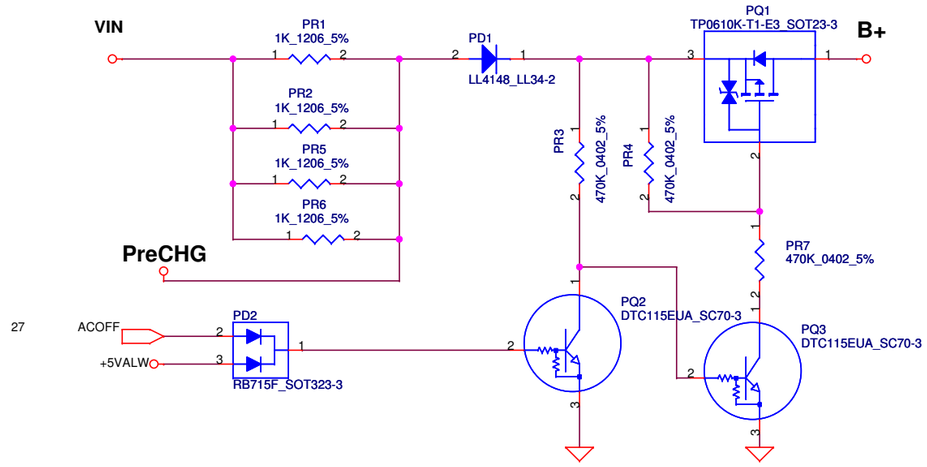
Compal Electronics, Inc.

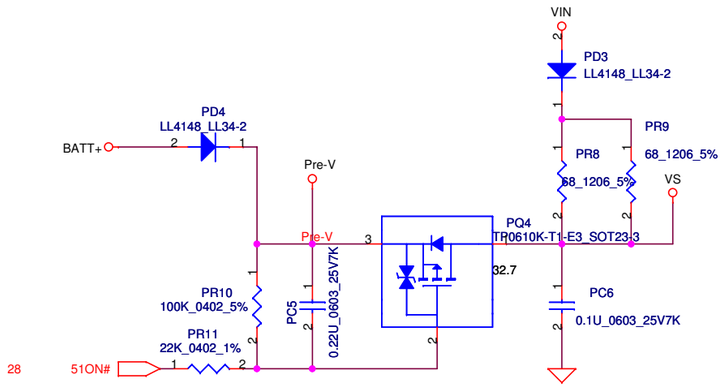
Title: EE P.I.R (1)

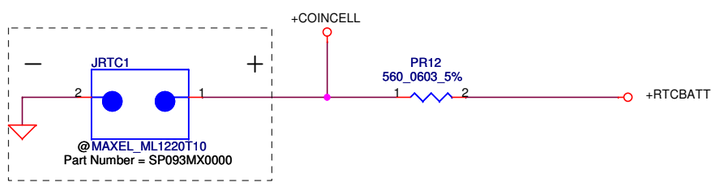
Size: Custom | Document Number: LA-7531P | Rev: 0.1

Date: Tuesday, March 15, 2011 | Sheet 32 of 45

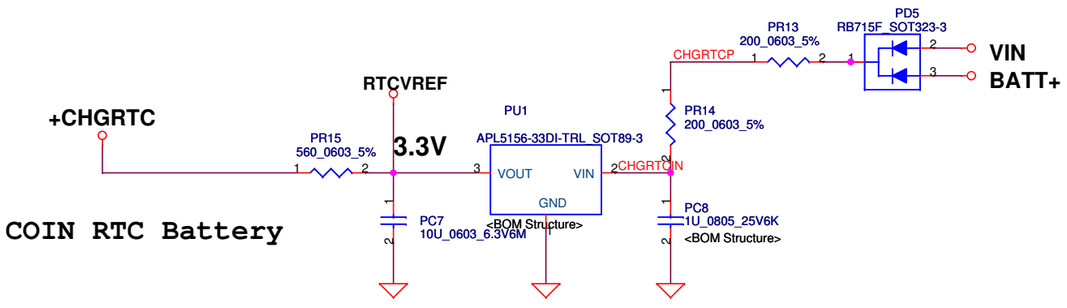








RTC Battery



COIN RTC Battery

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

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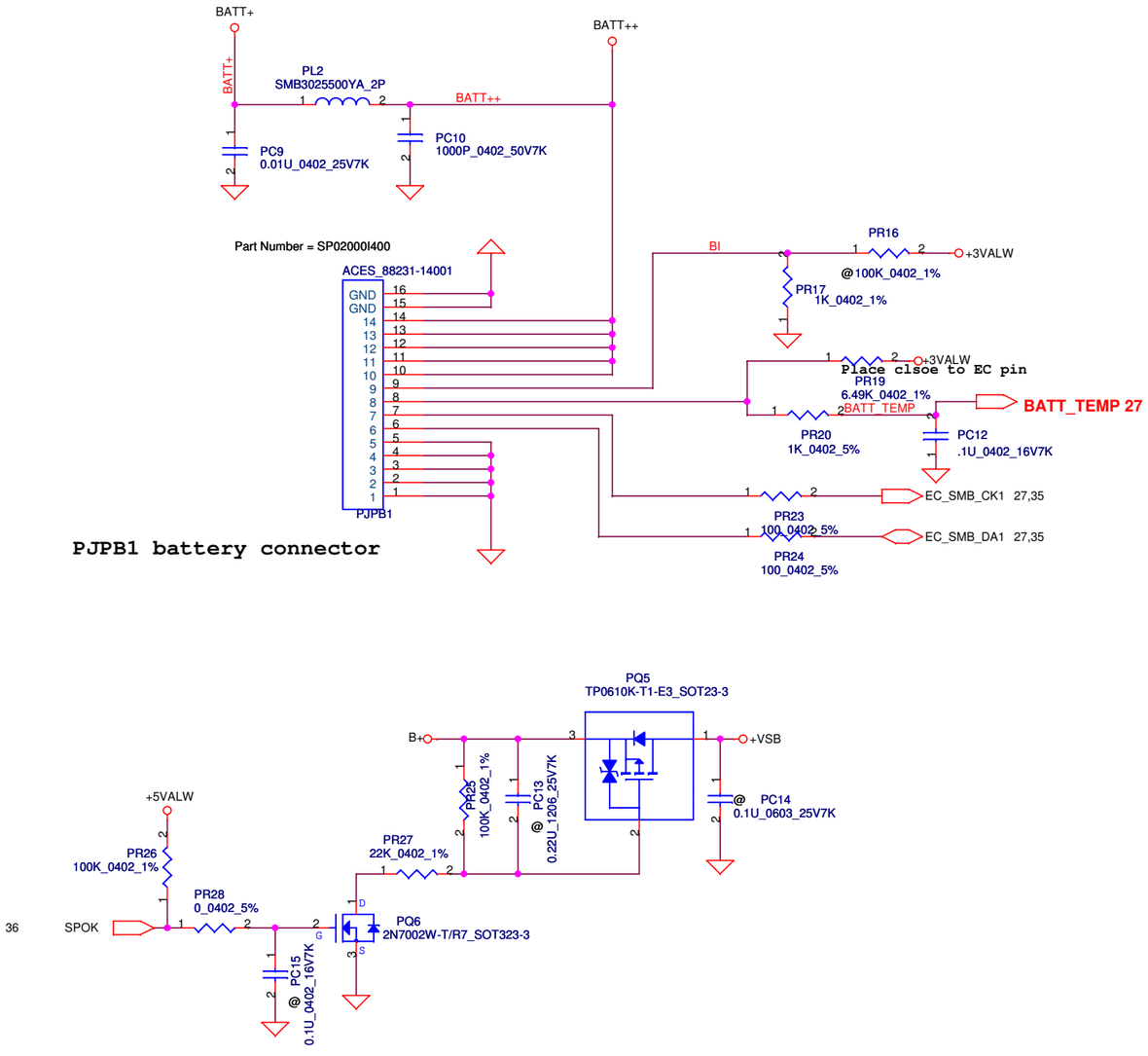
Compal Electronics, Inc.

Title: PWR-DCIN / Vin Detector

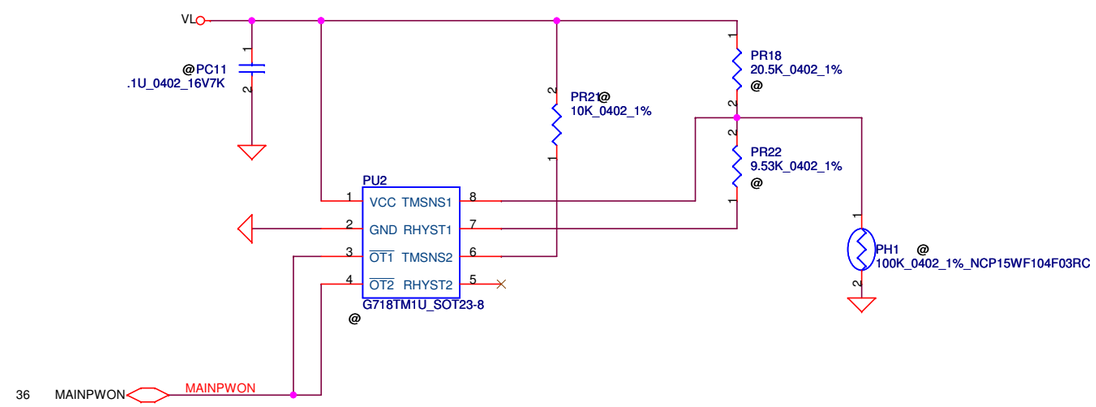
Size: Custom | Document Number: LA-7531P | Rev: 0.1

Date: Sunday, April 10, 2011 | Sheet 33 of 45



Battery Connect/OTP

PH3 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 50 degree C



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

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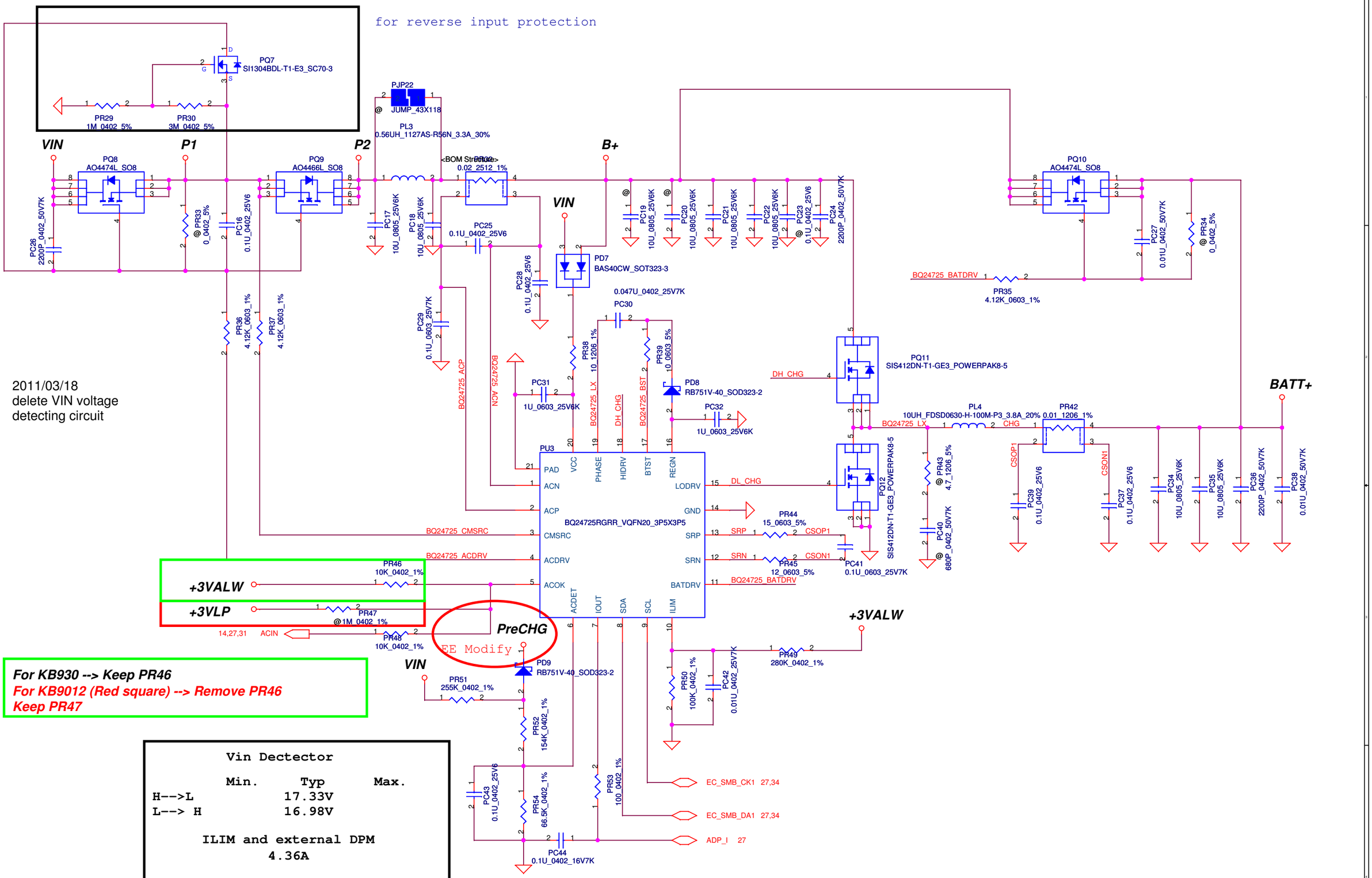
Compal Electronics, Inc.

Title: ***PWR-BATTERY CONN***

Size: Custom | Document Number: ***LA-7531P*** | Rev: 0.1

Date: Sunday, April 10, 2011 | Sheet 34 of 45



2011/03/18
delete VIN voltage
detecting circuit

For KB930 --> Keep PR46
For KB9012 (Red square) --> Remove PR46
Keep PR47

Vin Dectector

	Min.	Typ	Max.
H-->L		17.33V	
L--> H		16.98V	

ILIM and external DPM
4.36A

Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

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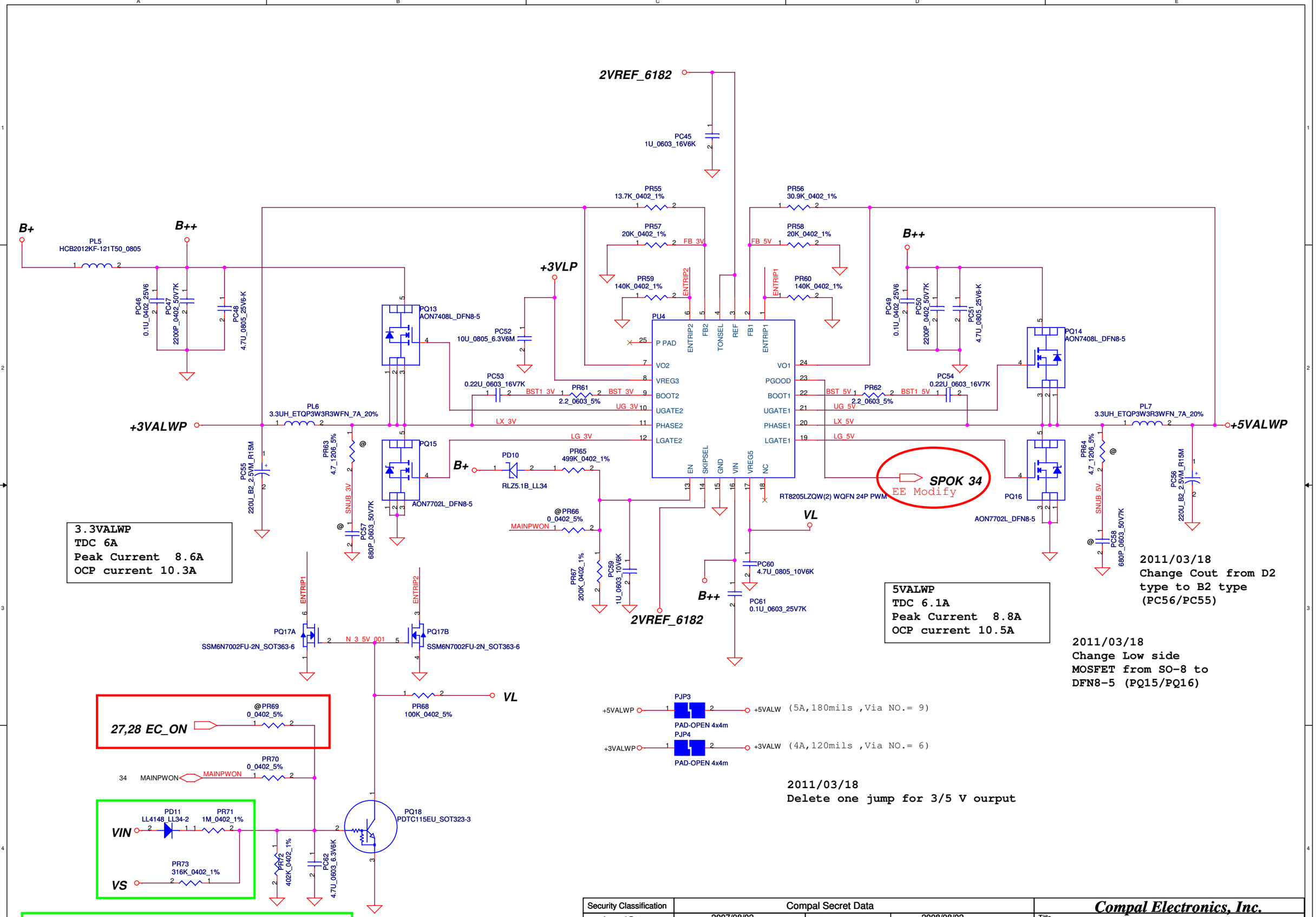
Compal Electronics, Inc.

Title: **PWR-CHARGER**

Size | Document Number: *LA-7531P* | Rev: 0.1

Date: Sunday, April 10, 2011 | Sheet 35 of 45



Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	2008/08/02

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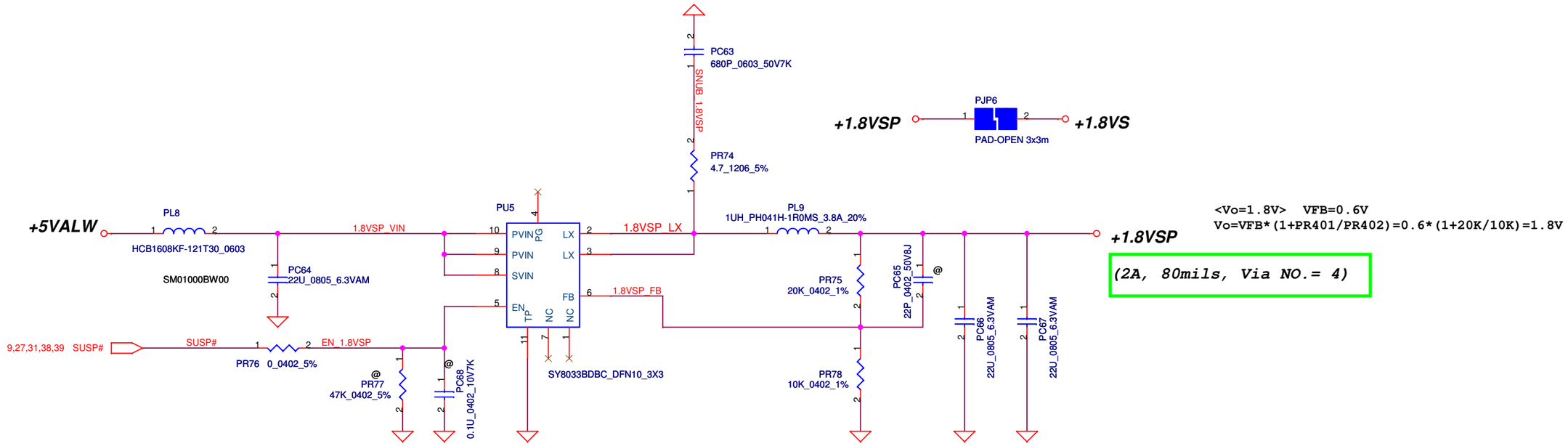
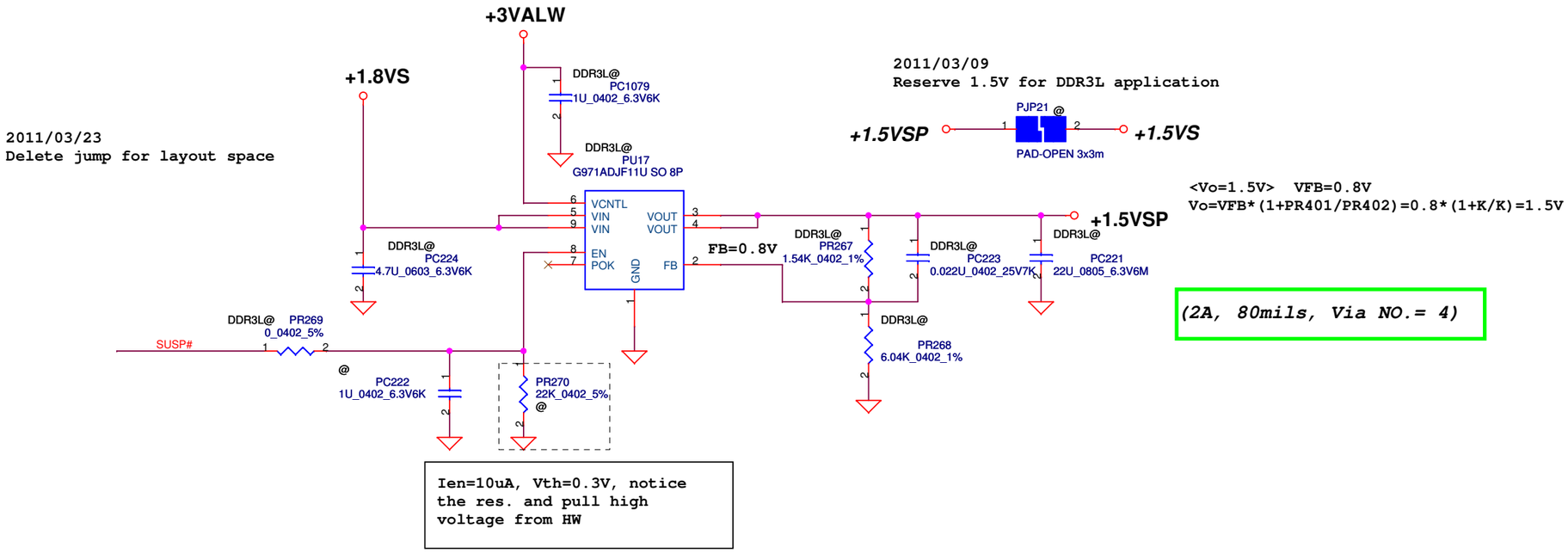
Compal Electronics, Inc.

Title: **PWR-3VALWP/5VALWP**

Size: Custom | Document Number: LA-7531P | Rev: 0.1

Date: Sunday, April 10, 2011 | Sheet 36 of 45





Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

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LA-7531P

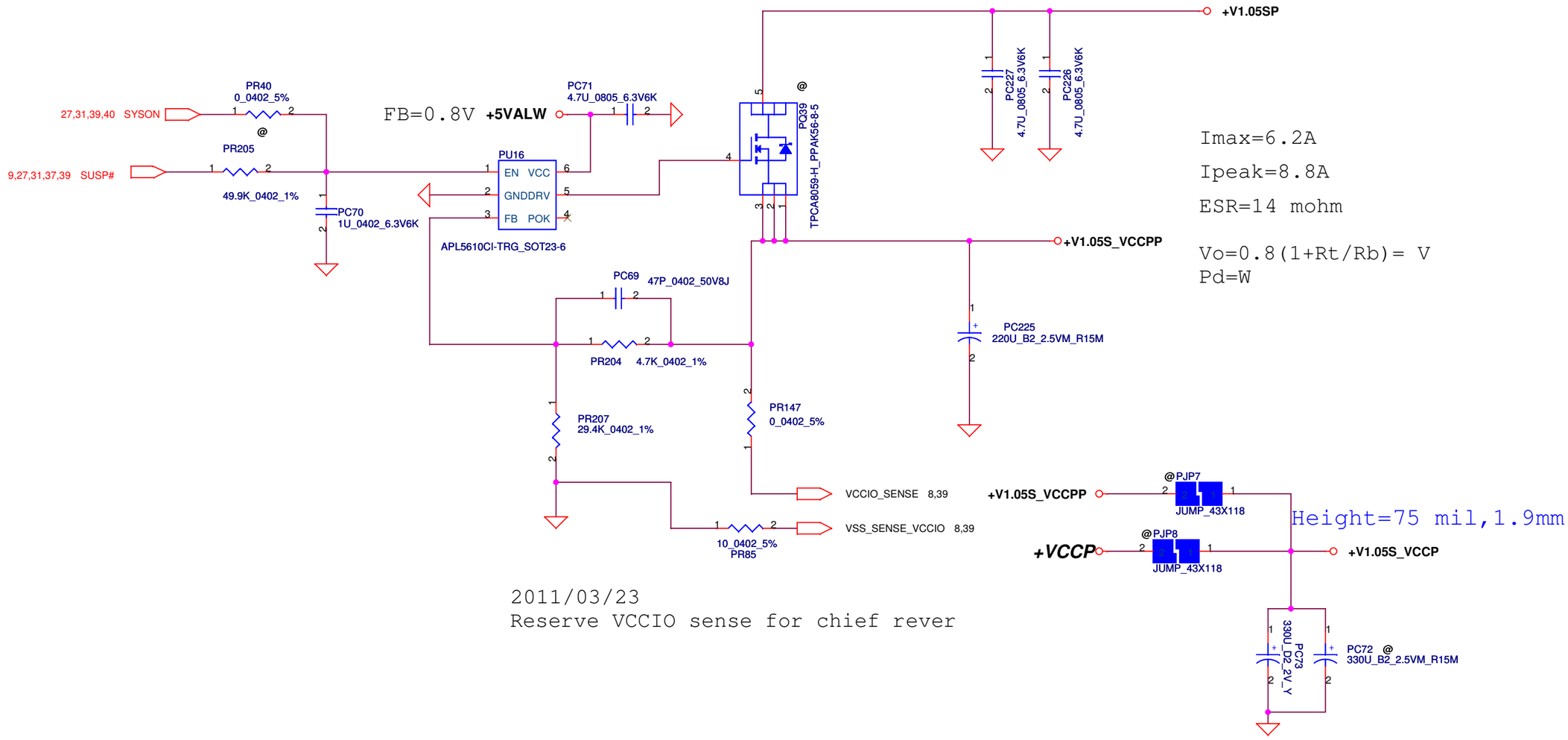
Compal Electronics, Inc.

Title: **PWR-1.8VSP**

Size | Document Number: LA-7531P | Rev: 0.1

Date: Sunday, April 10, 2011 | Sheet 37 of 45

2011/03/15
Change Cout to D2 type
Change PQ26 to TPCA8059(Rds-on)
2011/03/18
Change Cout from D2 type to B2
typt
2011/03/22
delete input jump



Imax=6.2A

Ipeak=8.8A

ESR=14 mohm

Vo=0.8(1+Rt/Rb)= V
Pd=W

Height=75 mil,1.9mm

2011/03/23
Reserve VCCIO sense for chief rever

2011/03/18
Change PR72 form D2 type to B2 type.
need to take care the ESR differentia

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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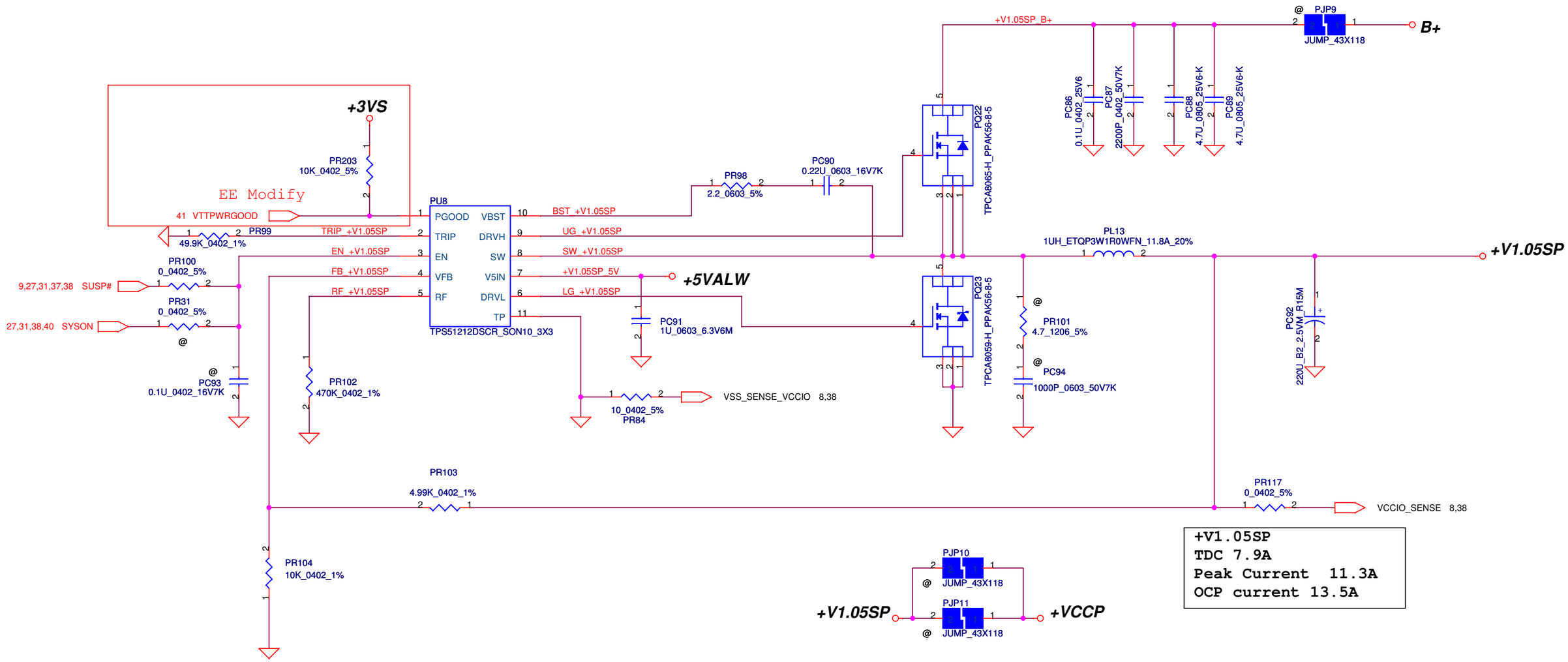
Compal Electronics, Inc.

Title: **PWR-V1.05S_VCCP**

Size: Custom | Document Number: LA-7531P | Rev: 0.1

Date: Sunday, April 10, 2011 | Sheet 38 of 45



+V1.05SP
TDC 7.9A
Peak Current 11.3A
OCP current 13.5A

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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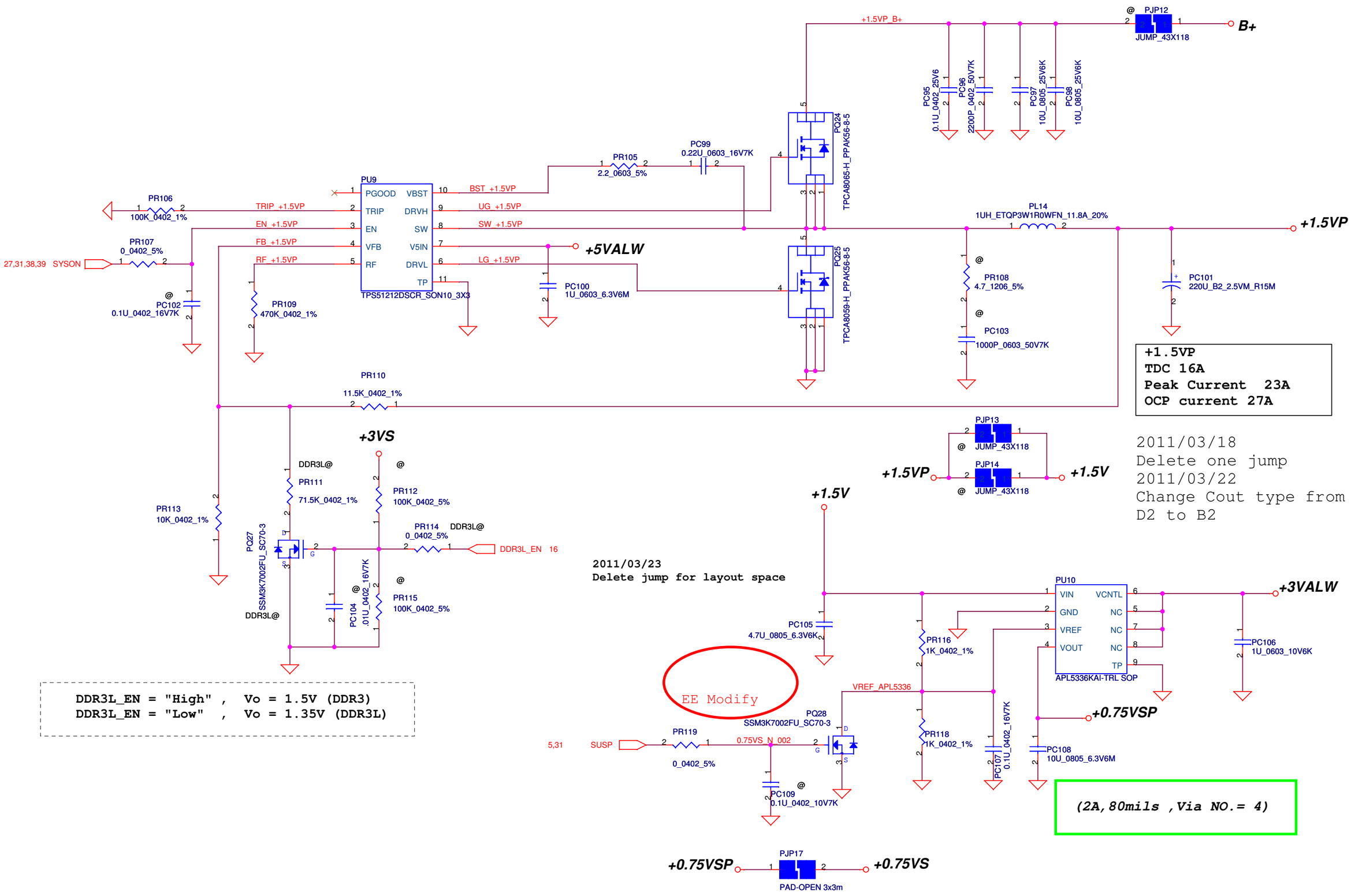
Compal Electronics, Inc.

Title: PWR-V1.05SP

Size: Custom | Document Number: LA-7531P | Rev: 0.1

Date: Sunday, April 10, 2011 | Sheet 39 of 45



Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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Compal Electronics, Inc.

Title: **PWR-1.5VP/0.75VSP**

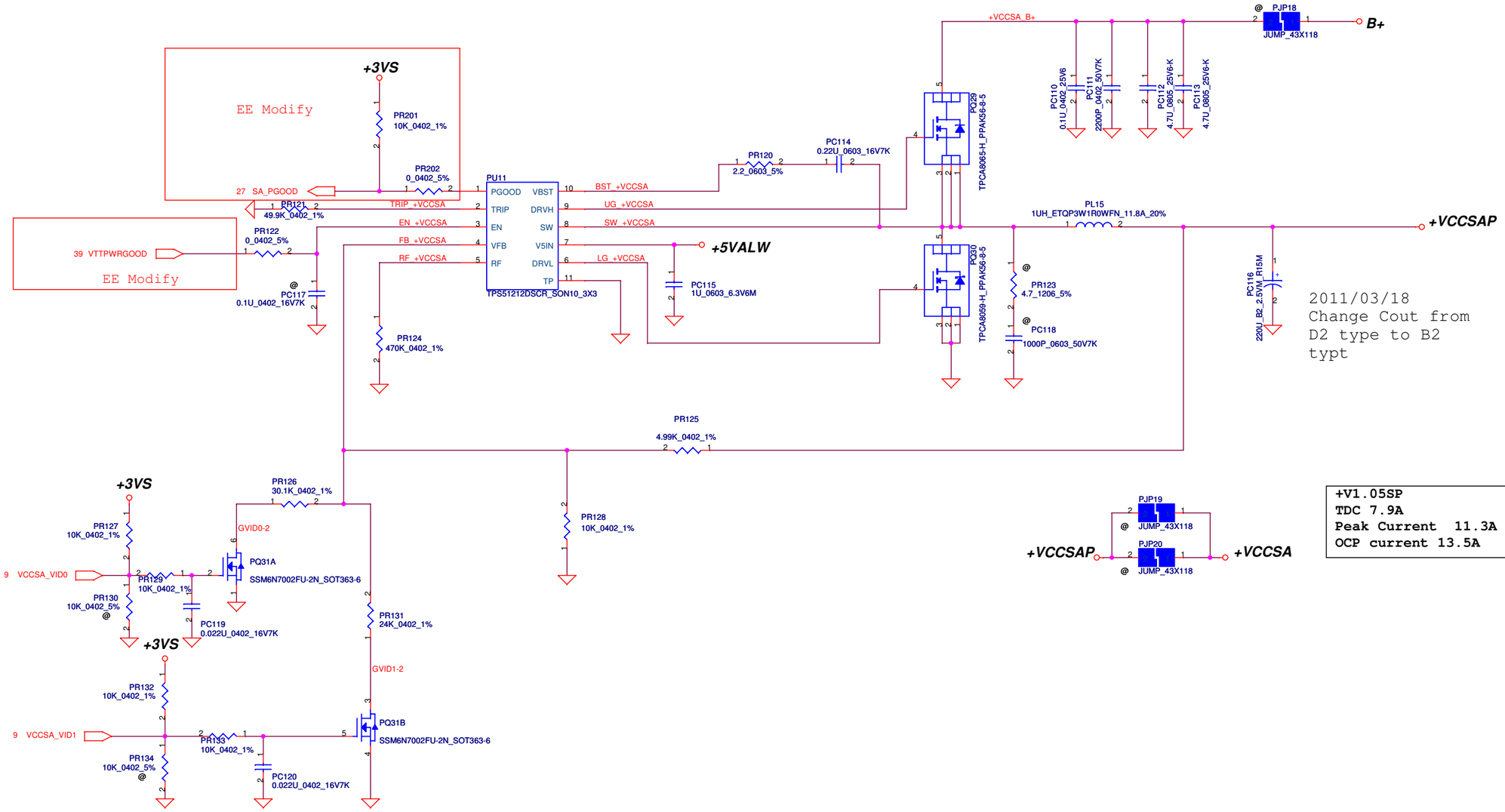
Size: Custom | Document Number: LA-7531P | Rev: 0.1

Date: Sunday, April 10, 2011 | Sheet 40 of 45

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network



+V1.05SP
TDC 7.9A
Peak Current 11.3A
OCP current 13.5A

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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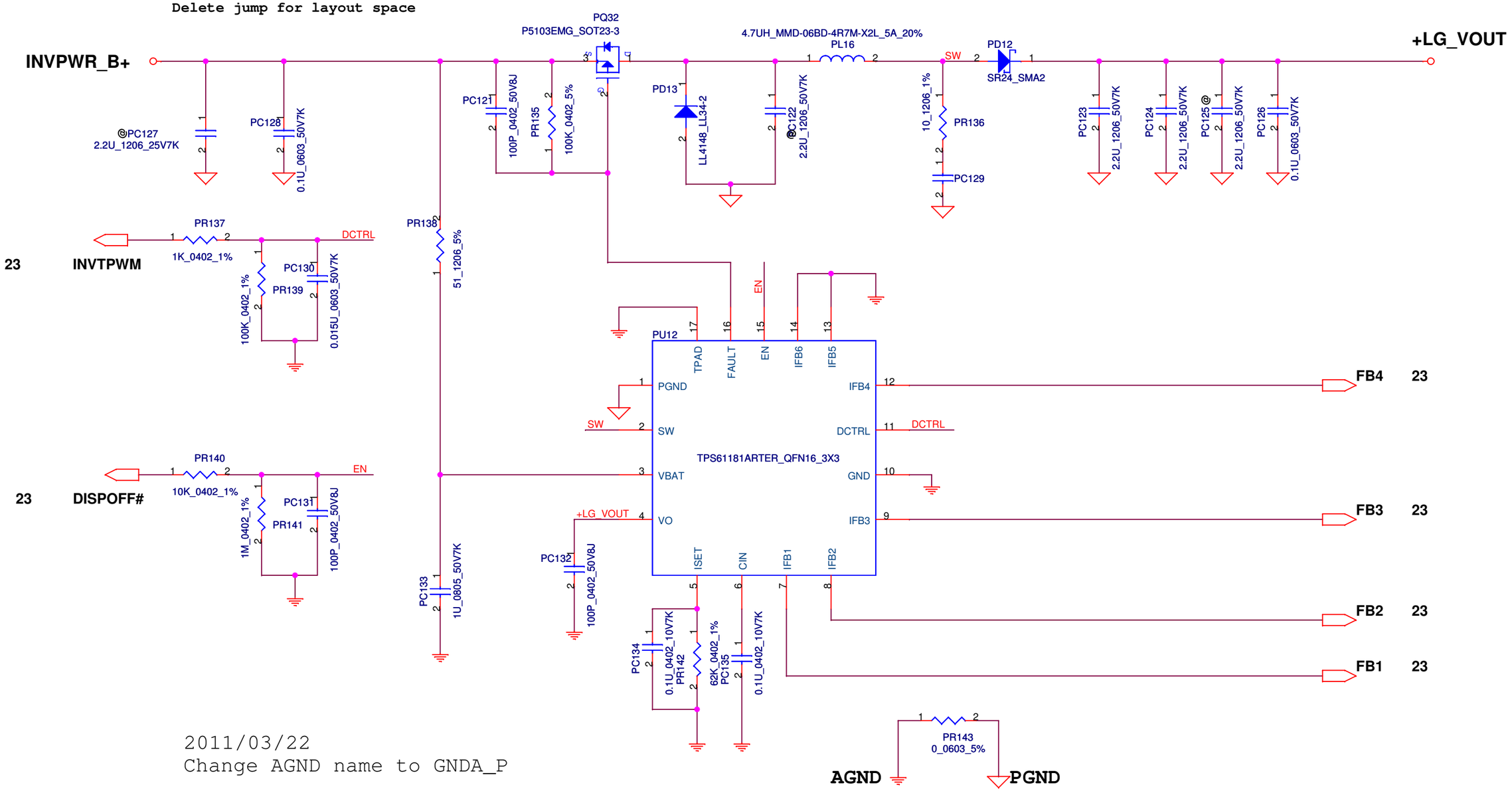
Compal Electronics, Inc.

Title: PWR-VCC_SAP

Size: C | Document Number: LA-7531P | Rev: 0.1

Date: Sunday, April 10, 2011 | Sheet 41 of 45

2011/03/23
Delete jump for layout space



2011/03/22
Change AGND name to GNDA_P

Security Classification	Compal Secret Data		
Issued Date	2010/07/20	Deciphered Date	2011/07/20

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Compal Electronics, Inc.

Title: **PWR-Panel Driver IC**

Size: B | Document Number: LA-7531P | Rev: 0.1

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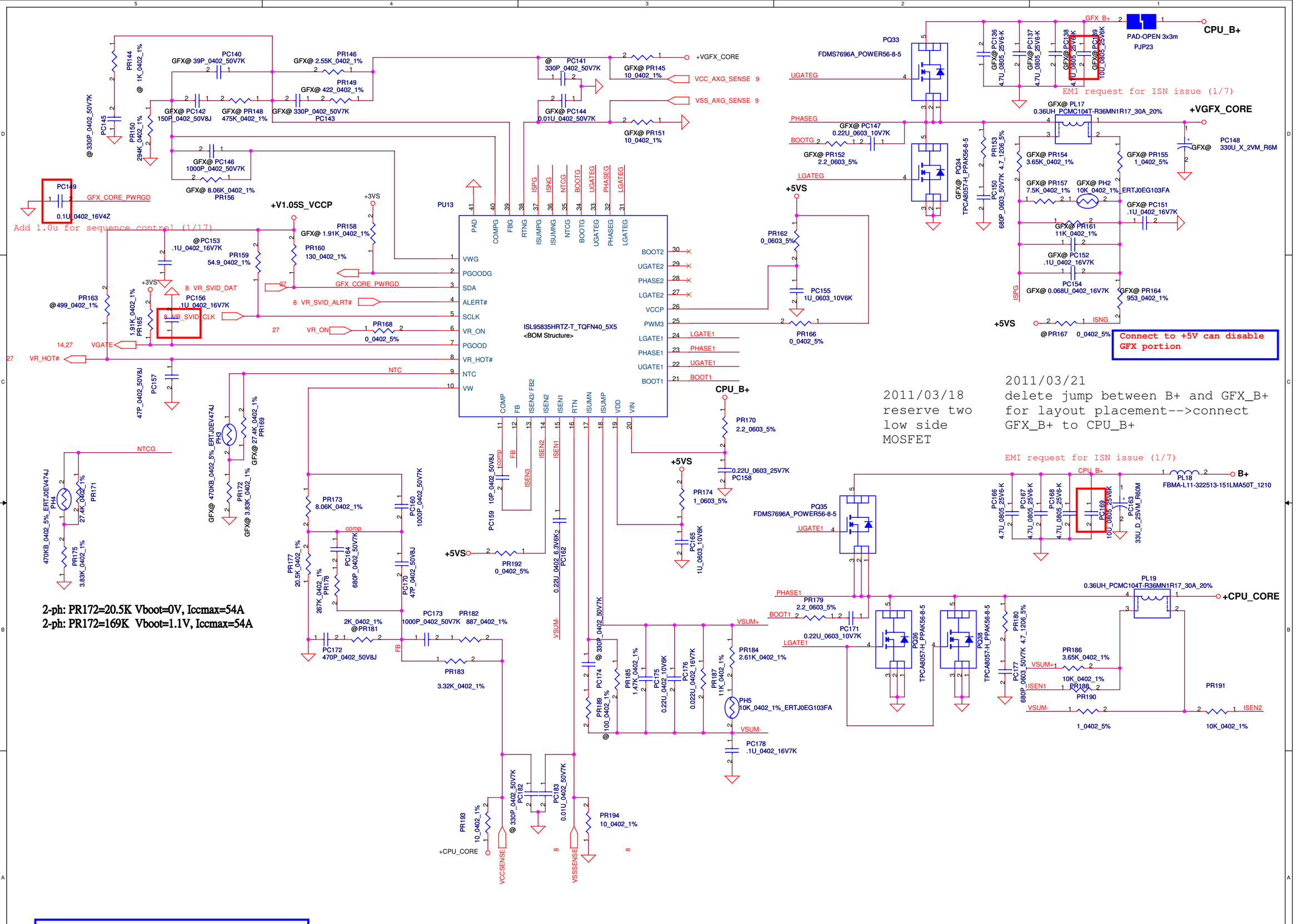

2011/03/18
reserve two
low side
MOSFET

2011/03/21
delete jump between B+ and GFX_B+
for layout placement-->connect
GFX_B+ to CPU_B+

+CPU_CORE	+GFX_CORE
Iocp=40A, IccMAX=28A	Iocp=20A, IccMAX=13A
Load line=1.9mohm	Load line=3.9mohm
DCR=1.1mohm	DCR=1.1mohm

Security Classification	Compal Secret Data		
Issued Date	2009/01/23	Deciphered Date	2010/01/23

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Title: **PWR-CPU_CORE/GFX**

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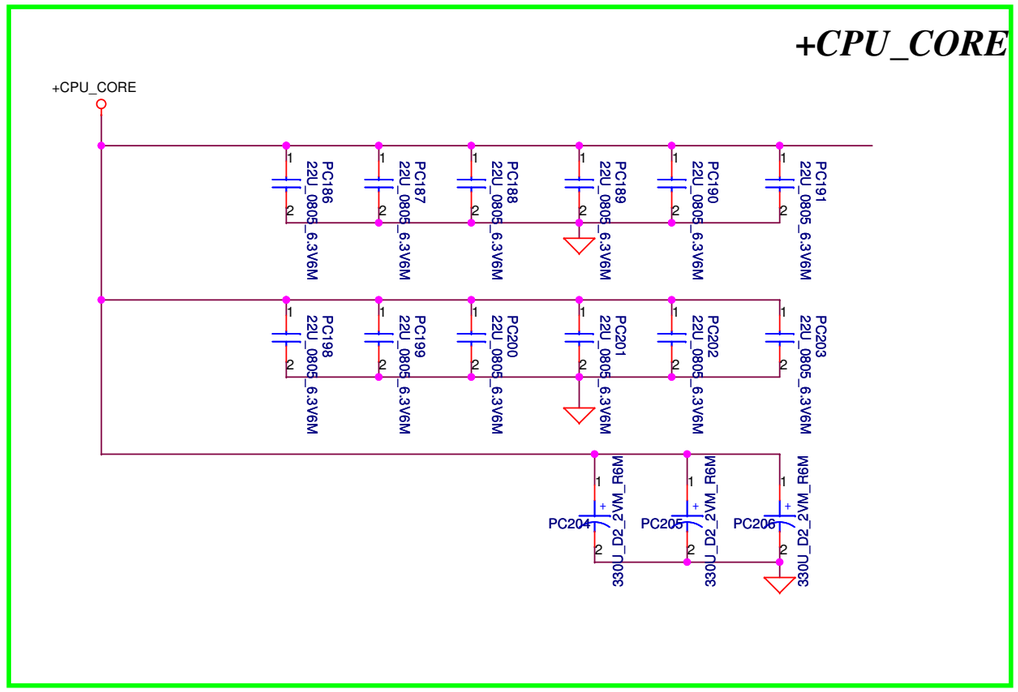

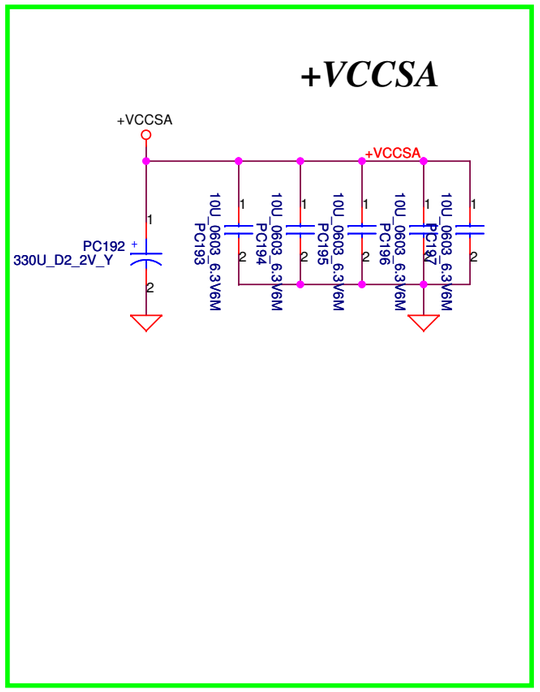

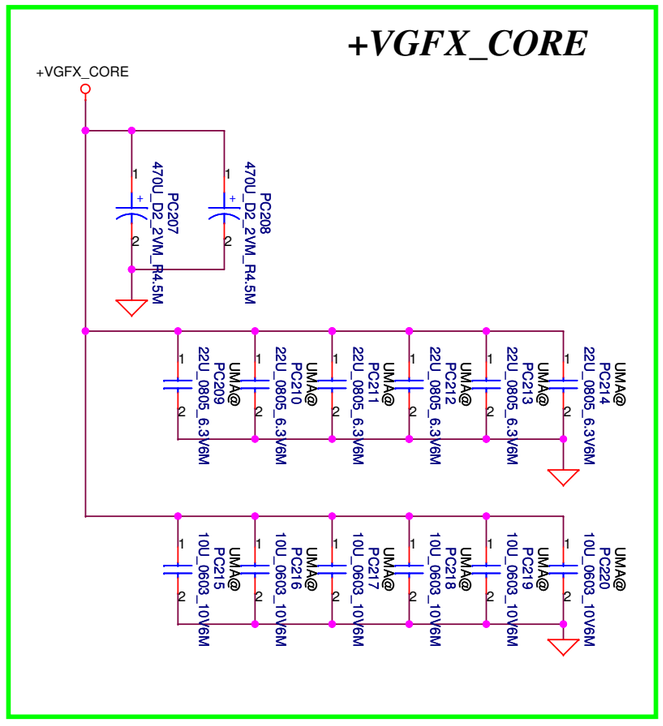

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Issued Date	2008/09/15	Deciphered Date	2009/09/15

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Title: **PWR - PROCESSOR DECOUPLING**

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Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

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Title: **PWR - PIR**

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