PCA70/61

Sugar Bay

LA-7521P REV 0.2
LA-7522P REV 0.1
Schematic

Intel Processor(Sandy Bridge) / PCH(Cougar Point)
Tuesday, April 12, 2011 Rev 0.2

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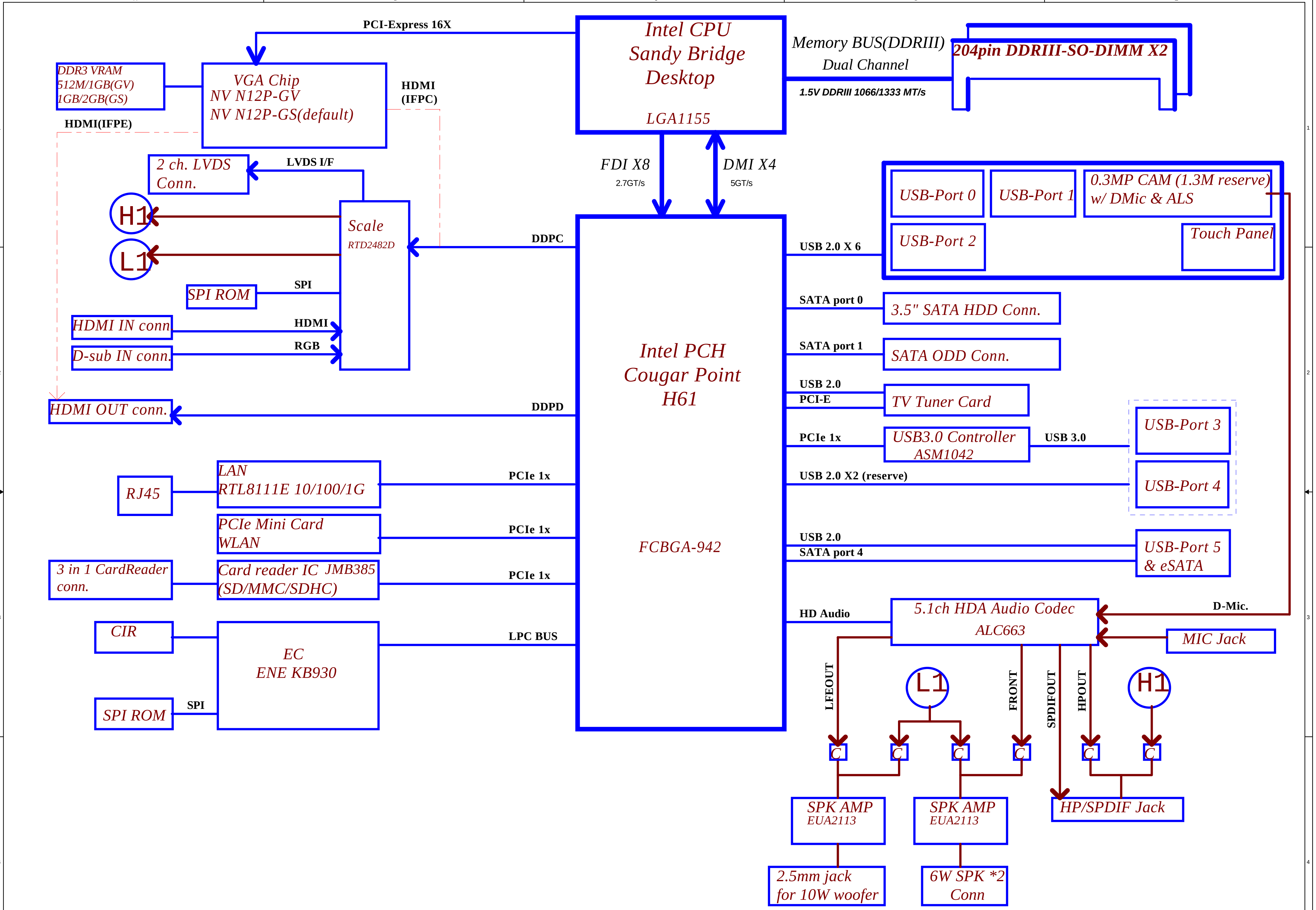

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Title: **Block Diagram**

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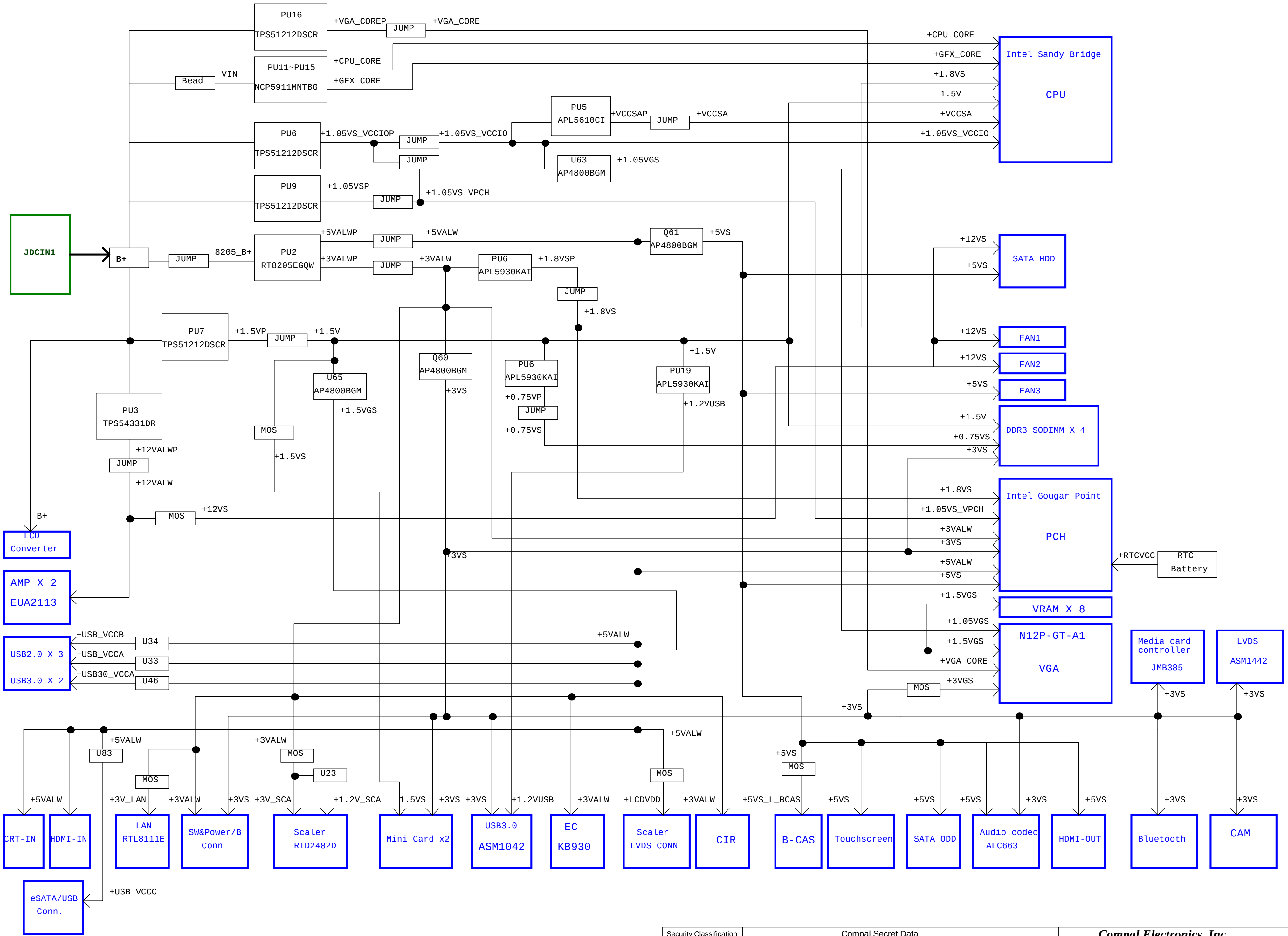

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Title: **Power Tree**

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Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+GFX_CORE	Graphics voltage for CPU	ON	OFF	OFF
+VCCSA	System Agent core voltage for CPU	ON	OFF	OFF
+1.05VS_VCCIO	1.05V power rail for CPU	ON	OFF	OFF
+1.05VS_VPCH	1.05V power rail for PCH	ON	OFF	OFF
+0.75VS	0.75V power rail for DDR terminator	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail once AC plug in	ON	ON	ON
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+3V_SCA	3.3V switched power rail for scaler	ON	N/A	N/A
+1.2V_SCA	1.2V switched power rail for scaler	ON	N/A	N/A
+1.2V_USB	1.2V power rail for USB3.0	ON	OFF	OFF
+5VALW	5V always on power rail once AC plug in	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+LCDVDD	5V switched power rail for panel	ON	N/A	N/A
+RTCVCC	RTC power	ON	ON	ON
+3VGS	3.3V power rail for GPU	ON	OFF	OFF
+VGA_CORE	Graphics power rail for GPU	ON	OFF	OFF
+1.05VGS	1.05VS switched power rail for GPU	ON	OFF	OFF
+1.5VGS	1.5VS power rail for GPU and VRAM	ON	OFF	OFF
+12VALW	12V always on power rail once AC plug in	ON	N/A	N/A
+12VS	5V switched power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR(JDDRL2)		1010 000X b
+3VS	DDR(JDDRH1)		1010 010X b

PCH SML1 Bus Address

Power	Device	HEX	Address
	VGA Ext. thermal sensor		1001_1010b
	VGA Int. thermal sensor (defaulta)		1001_1110b

EC SM Bus2 Address

Power	Device	HEX	Address
	Scaler		0000_0101b

Board ID	Rb	V_{BID} min	V_{BID} typ	V_{BID} max	EC AD3
0	0	0 V	0 V	0.155 V	0x00 - 0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D - 0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D - 0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31 - 0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A - 0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A - 0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F - 0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC - 0xFF

SIGNAL / STATE	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+VS
Full ON	*HIGH*	*HIGH*	*HIGH*	*ON*	*ON*
S1(Power On Suspend)	*HIGH*	*HIGH*	*HIGH*	*ON*	*ON*
S3 (Suspend to RAM)	*LOW*	*HIGH*	*HIGH*	*ON*	*OFF*
S4 (Suspend to Disk)	*LOW*	*LOW*	*HIGH*	*ON*	*OFF*
S5 (Soft OFF)	*LOW*	*LOW*	*LOW*	*OFF*	*OFF*

USB Port Table

USB 2.0	USB 1.1	Port	Device
EHCI1	UHCI0	0	Co-lay w/USB30 PORT0
		1	Co-lay w/USB30 PORT1
	UHCI1	2	Touch Screen
		3	Web Camera
	UHCI2	4	eSATA+USB Conn
		5	USB Conn 6
	UHCI3	6	Disabled on H61
		7	Disabled on H61
EHCI2	UHCI4	8	USB Conn 4
		9	USB Conn 3
	UHCI5	10	Mini Card(TV Tuner)
		11	Blue Tooth
	UHCI6	12	Disabled on H61
		13	Disabled on H61

SATA Port Table

	Port	Device
6G	0	HDD
	1	ODD
3G	2	Disabled on H61
	3	Disabled on H61
	4	eSATA+USB Conn
	5	NC

PCIE Port Table

Port	Device
1	NC
2	USB30
3	WLAN
4	TV
5	Card reader
6	LAN
7	Disabled on H61
8	Disabled on H61

BOARD ID Table

Board ID	PCB Revision
* 0	0.1
1	0.2
2	
3	
4	

BOM Structure Table

BTO Item	BOM Structure
ME components	CONN@
VGA-N12P-GS	GS@
VGA-N12P-GV	GV@
UMA Only	UMA@
DISCRETE ONLY	DIS@
USB30	USB30@
No USB30 SKU	USB20@
D-sub IN	VGAIN@
HDMI IN	HDMIIN@
HDMI OUT	HDMIO@
HDMI OUT from DIS	HDMIOD@
HDMI OUT from UMA	HDMIOU@
VGA w/o Senergy	DISO@
BCAS	TV@
VRAM select	X76@
VRAM 1G Hynix X7630488L01	X76_HY1G@
VRAM 1G Samsung X7630488L02	X76_SAM1G@
SKU IO Select	GPIO69_H@
	GPIO69_L@
	GPIO70_H@
	GPIO70_L@
	GPIO71_H@
	GPIO71_L@
Unpop	@
LA-7521P 6 Layer PCB	6LOCB@
LA-7522P 8 Layer PCB	8LPCB@

SKU ID(Project) Table

Project _ID2 (GPIO69)	Project _ID1 (GPIO70)	Project _ID0 (GPIO71)	Project	SKU	
0	0	0	PCA70	UMA USB30 w/o HDMI 4319D588L03	UMA@ USB30@ 8LPCB@ GPIO69_L@ GPIO70_L@ GPIO71_L@
0	0	1	PCA70	DIS-Hynix USB30 w/ HDMI 4319D588L04	GS@ DIS@ USB30@ VGAIN@ HDMIO@ HDMIOD@ DISO@ HDMIIN@ 8LPCB@ X76_HY1G@ GPIO69_L@ GPIO70_L@ GPIO71_H@
0	1	0	PCA70	UMA USB30 w/ HDMI 4319D588L05	UMA@ USB30@ VGAIN@ HDMIO@ HDMIOU@ DEBUG@ HDMIIN@ 8LPCB@ GPIO69_L@ GPIO70_H@ GPIO71_L@
0	1	1	PCA61	DIS-Hynix USB30 w/ HDMI 4319D588L11	GV@ DIS@ USB30@ VGAIN@ HDMIO@ HDMIOD@ DISO@ HDMIIN@ 6LOCB@ GPIO69_L@ GPIO70_H@ GPIO71_H@
1	0	0	PCA61	UMA USB20 w/ HDMI 4319D588L12	UMA@ USB20@ VGAIN@ HDMIO@ HDMIOU@ DEBUG@ HDMIIN@ 6LOCB@ GPIO69_H@ GPIO70_L@ GPIO71_L@
1	0	1		X	
1	1	0		X	
1	1	1		X	

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Title: ***Notes List***

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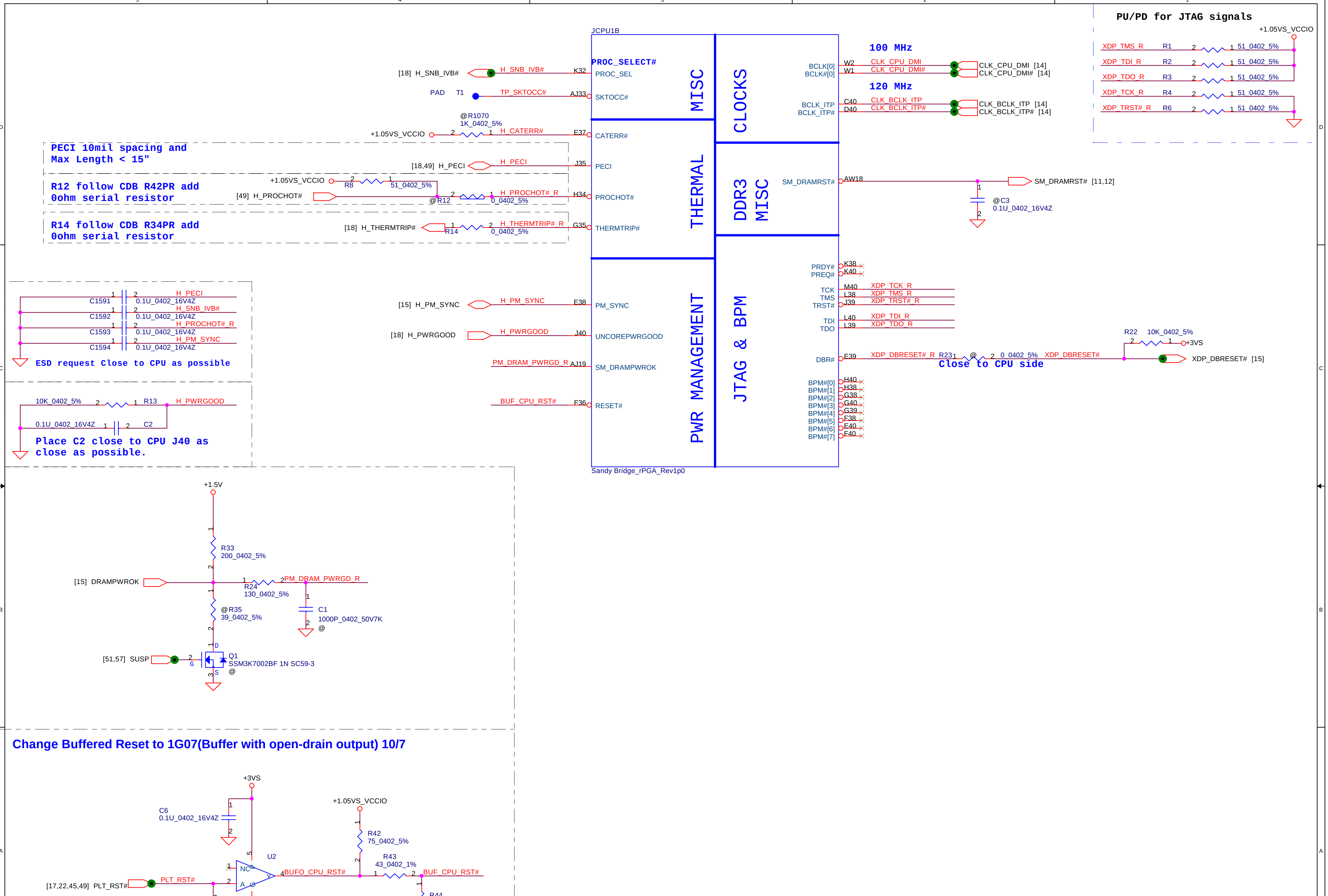

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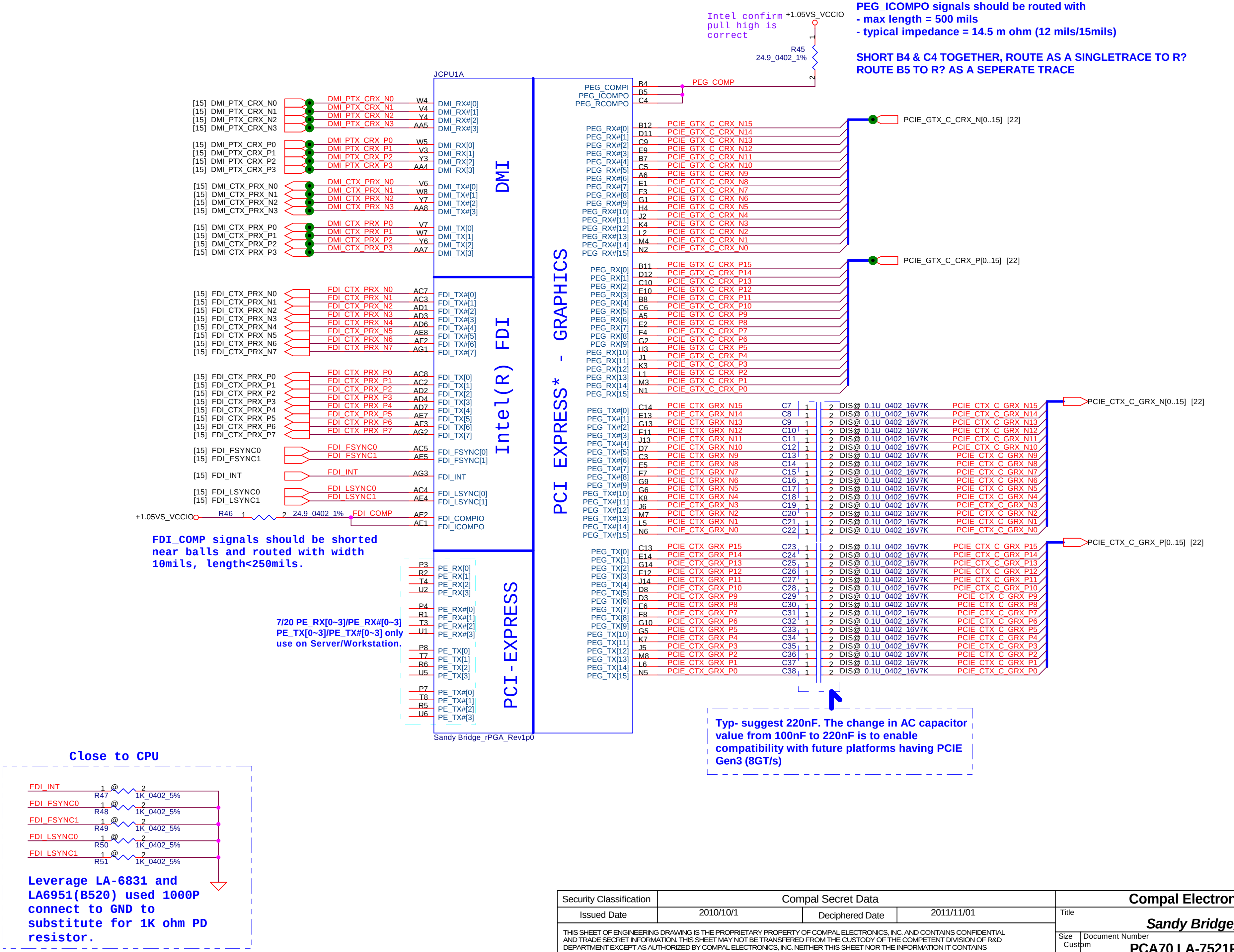
PEG_ICOMPI and RCOMPO signals should be shorted and routed with
- max length = 500 mils
- typical impedance = 43 m ohm (4 mils/15mils)

PEG_ICOMPO signals should be routed with
- max length = 500 mils
- typical impedance = 14.5 m ohm (12 mils/15mils)

SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLETRACE TO R?
ROUTE B5 TO R? AS A SEPERATE TRACE



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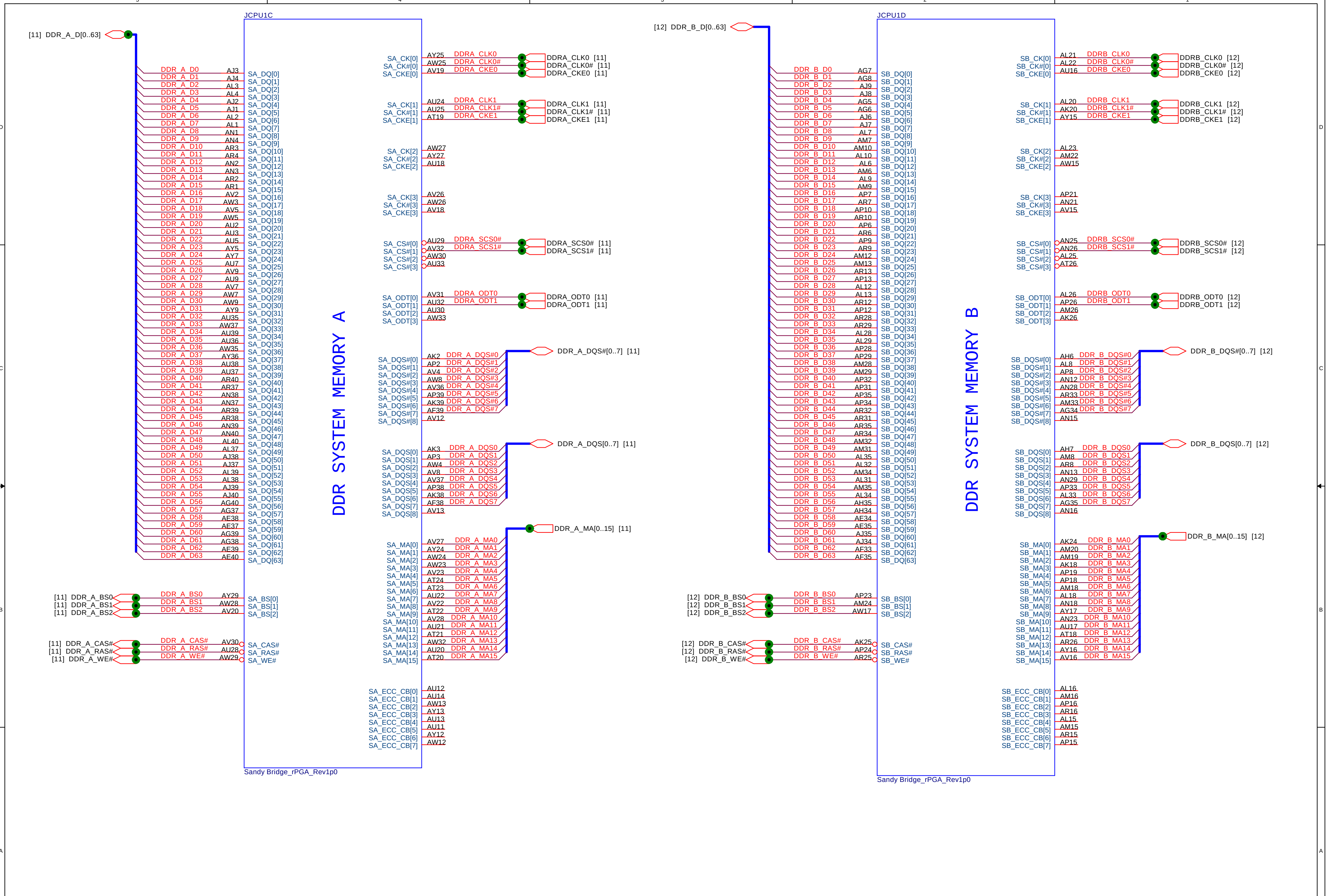

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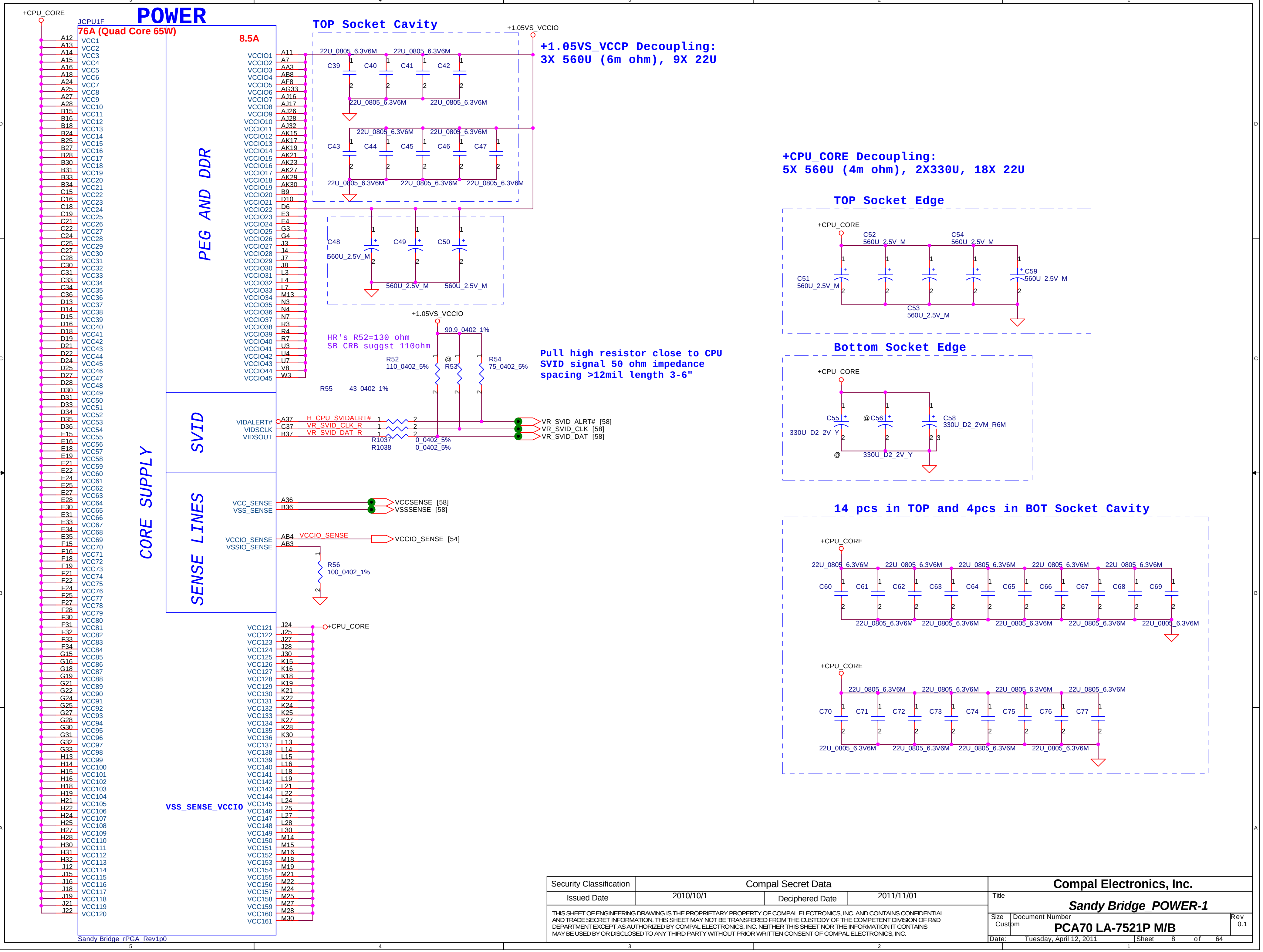

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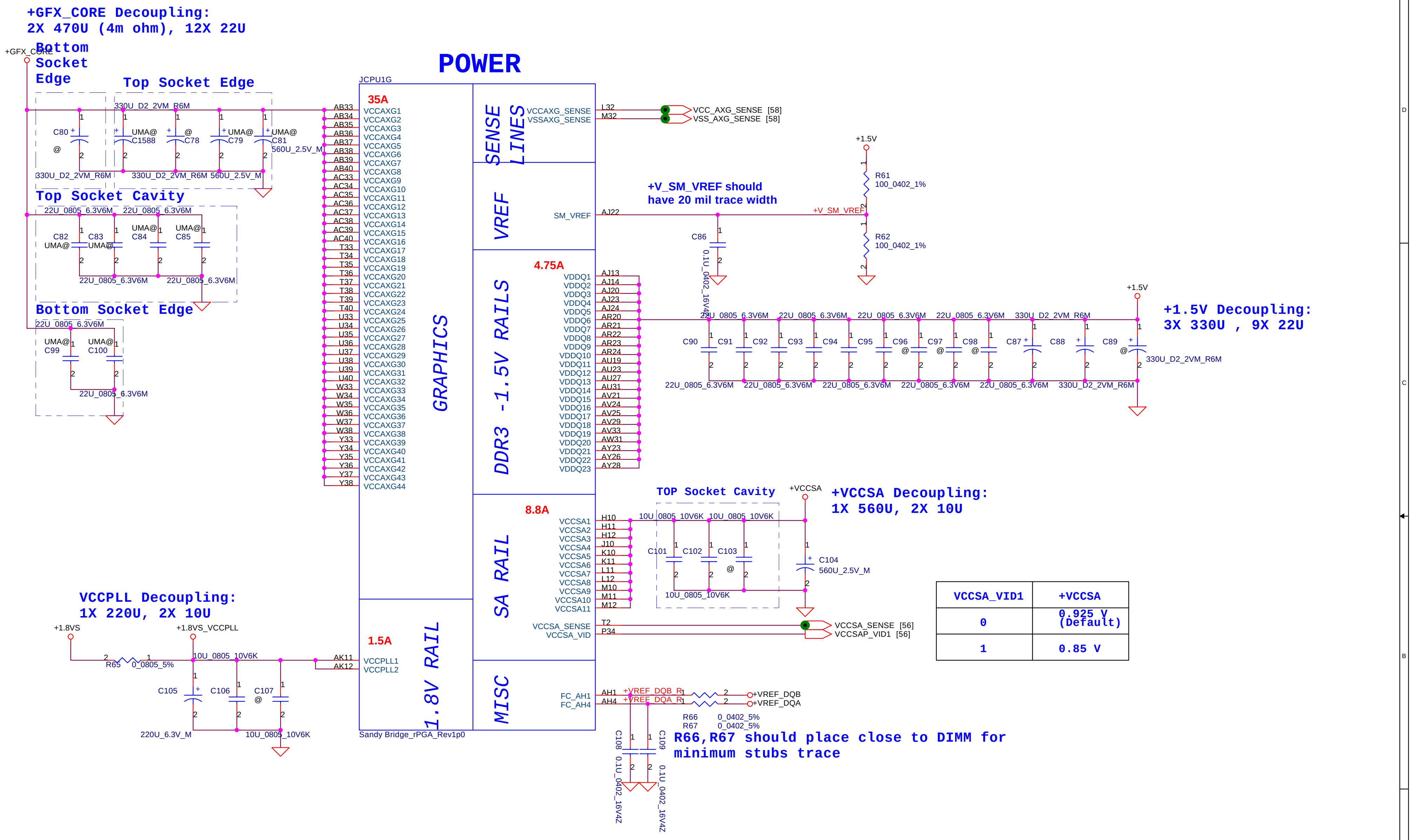

VCCSA_VID1	+VCCSA
0	0.925 V (Default)
1	0.85 V

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Title: Sandy Bridge_POWER-2

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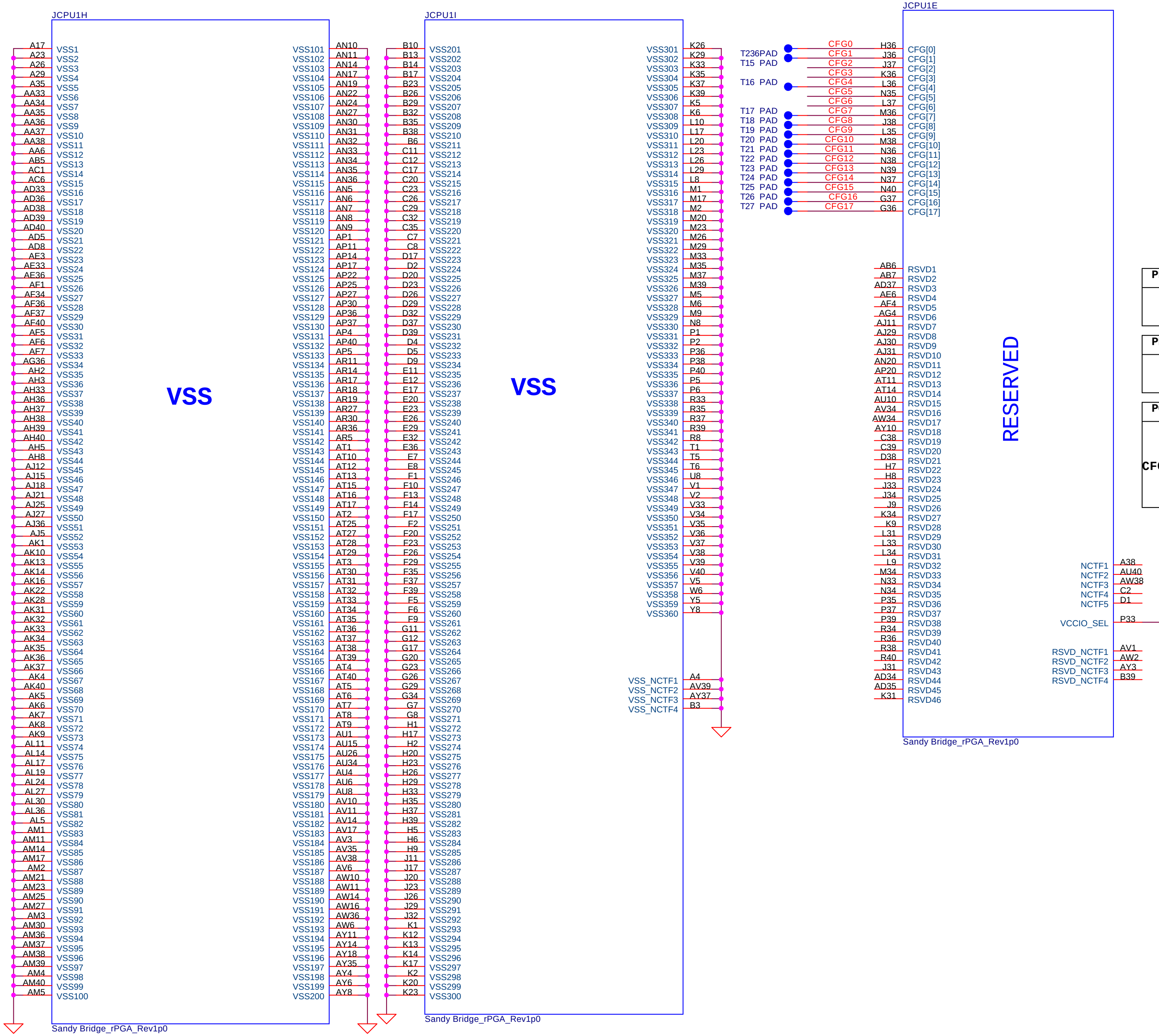
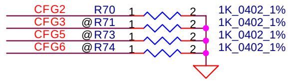


CFG Straps for Processor

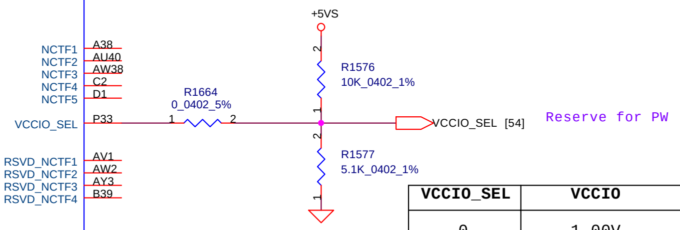
(CFG[17:0] internal pull high to VCCIO)



PEG Static x16 Lane Numbering Reversal.	
CFG2	1: Normal Operation
	* 0:Lane numbers Reversed

PEG Static x4 Lane Numbering Reversal.	
CFG3	* 1: Normal Operation
	0:Lane numbers Reversed

PCIE Port Bifurcation Straps	
CFG[6:5]	* 11: 1x16 PCI Express (Default)
	10: 2x8 PCI Express
	01: Reserved
	00: 1 x 8, 2 x 4 : PCI Express



VCCIO_SEL	VCCIO
0	1.00V
1	1.05V

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Title: *Sandy Bridge_GND/RSVD/CFG*

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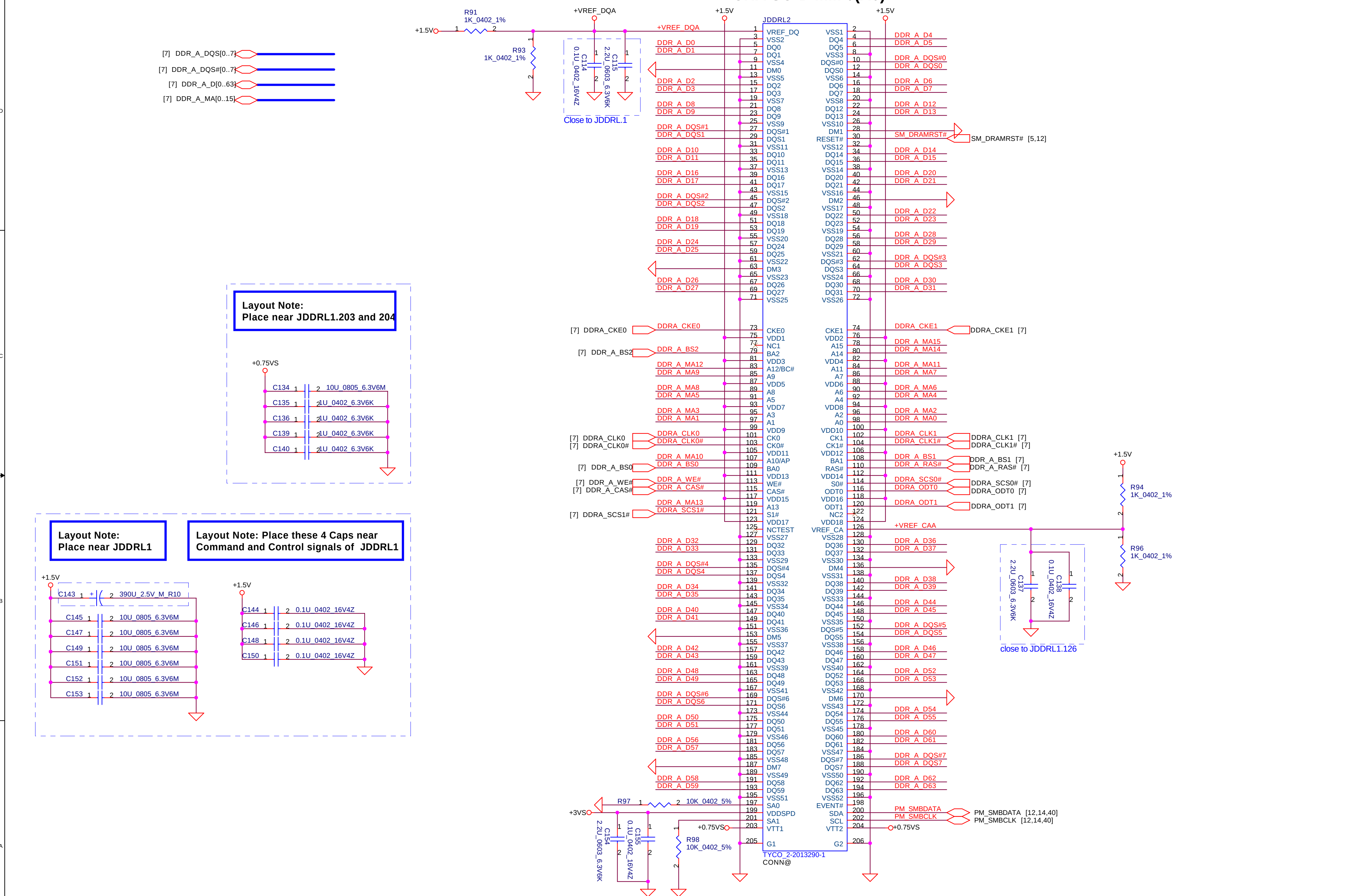
CHA SO-DIMM 0(A0)



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Title: *DDRIII-SODIMMA*

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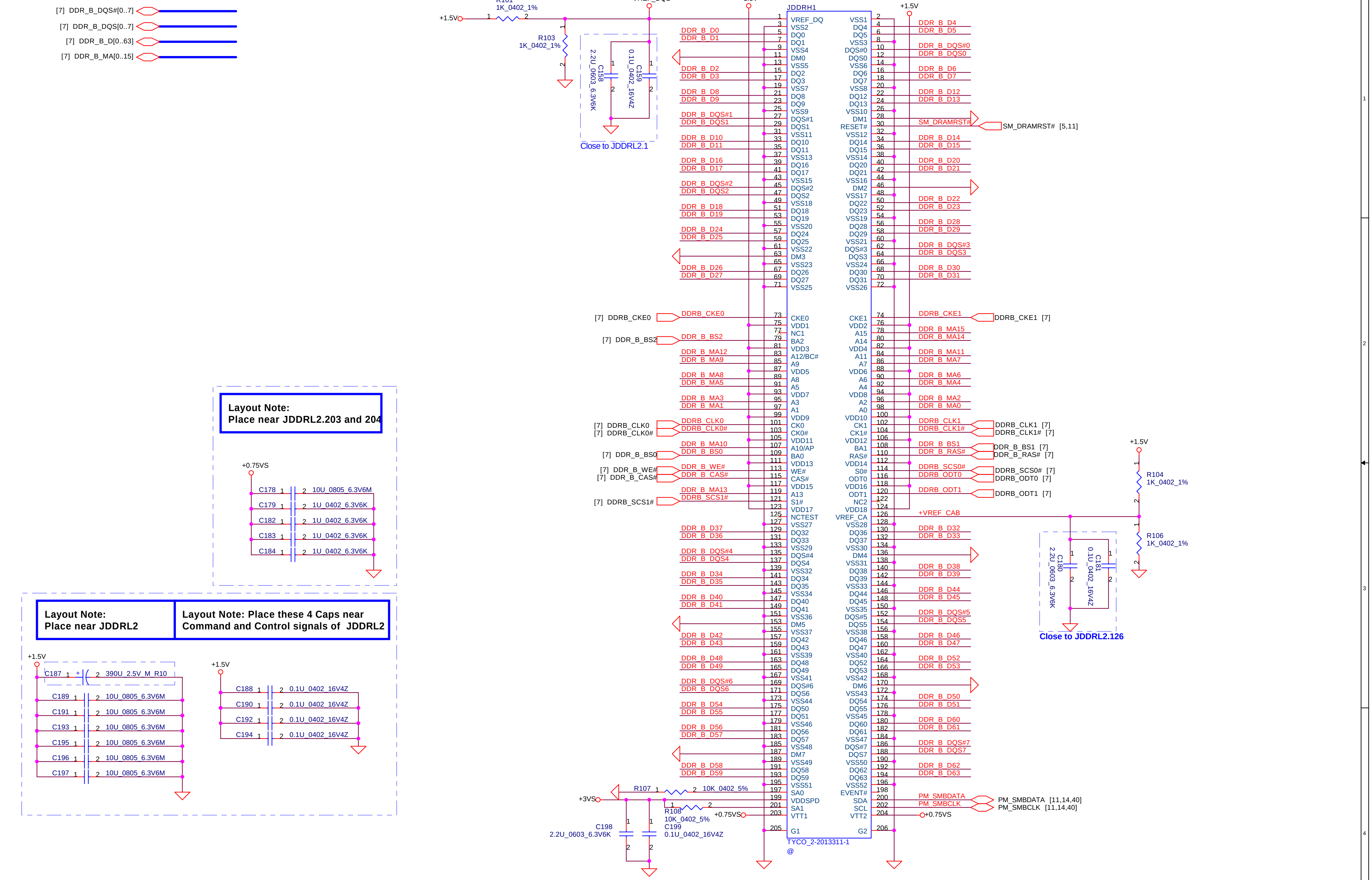
CHB SO-DIMM 0(A4)



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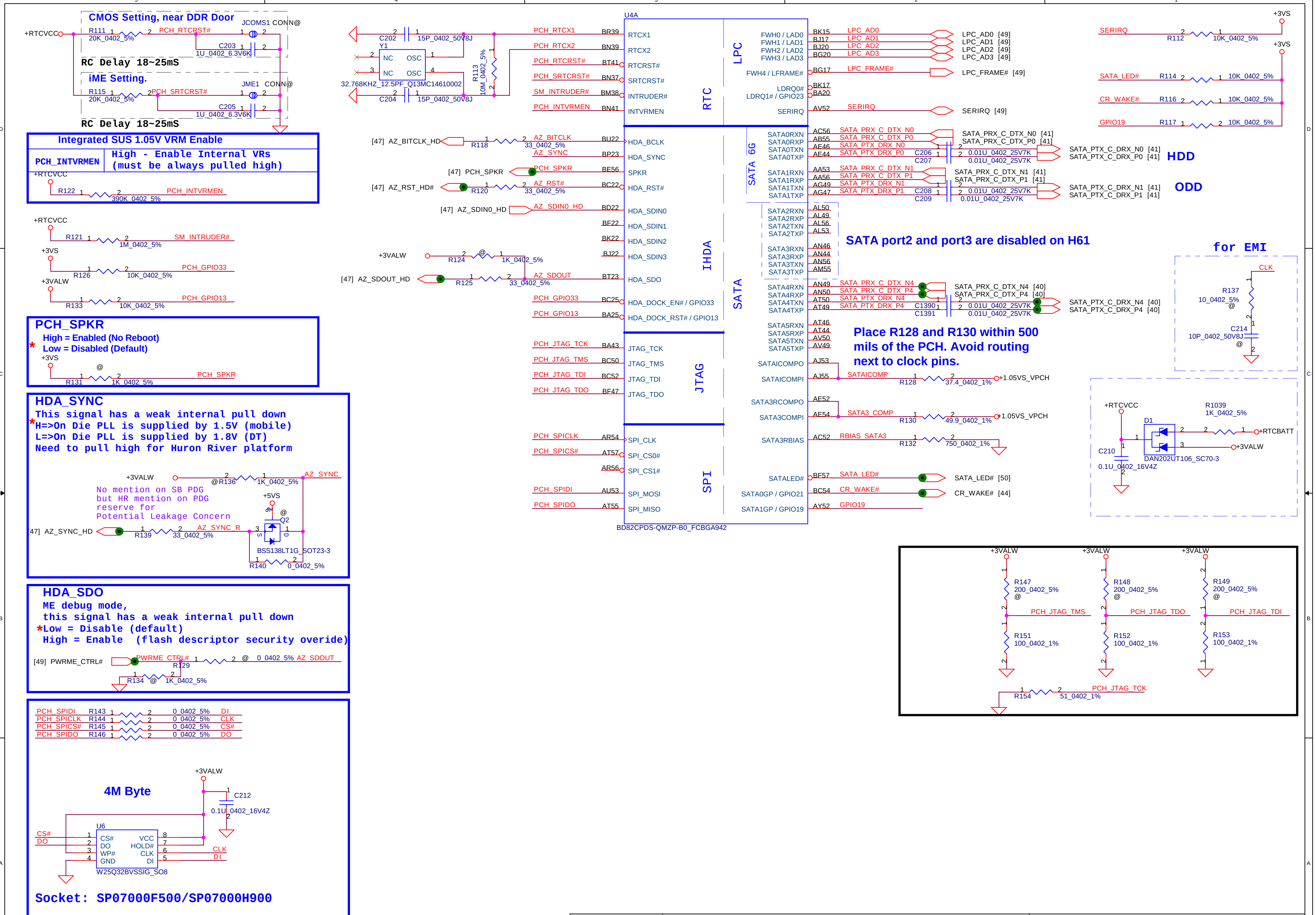

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Title: PCH_HDA/JTAG/SATA/SPI/LPC

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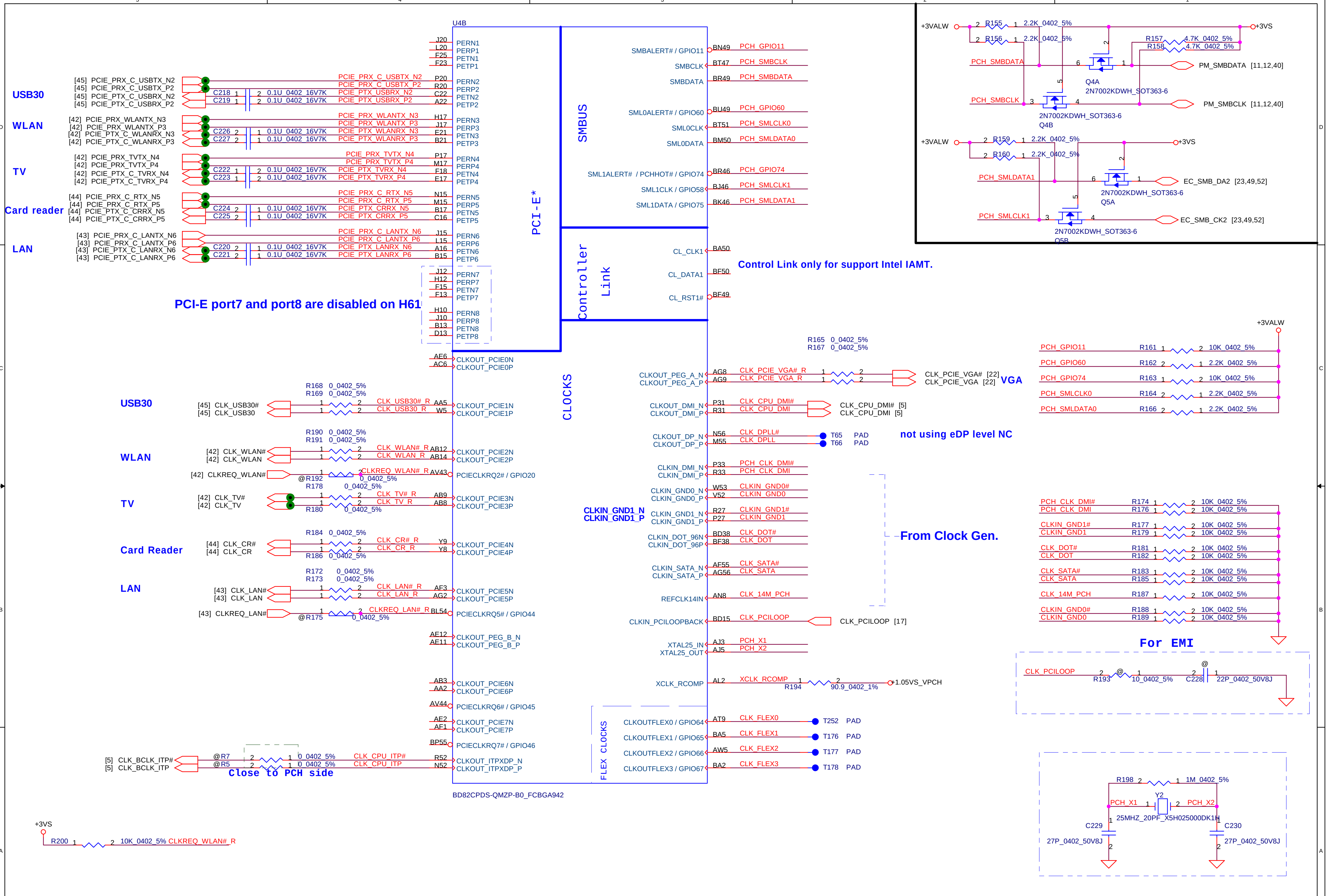

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Title: *PCH_PCI-E/SMBUS/CLK*

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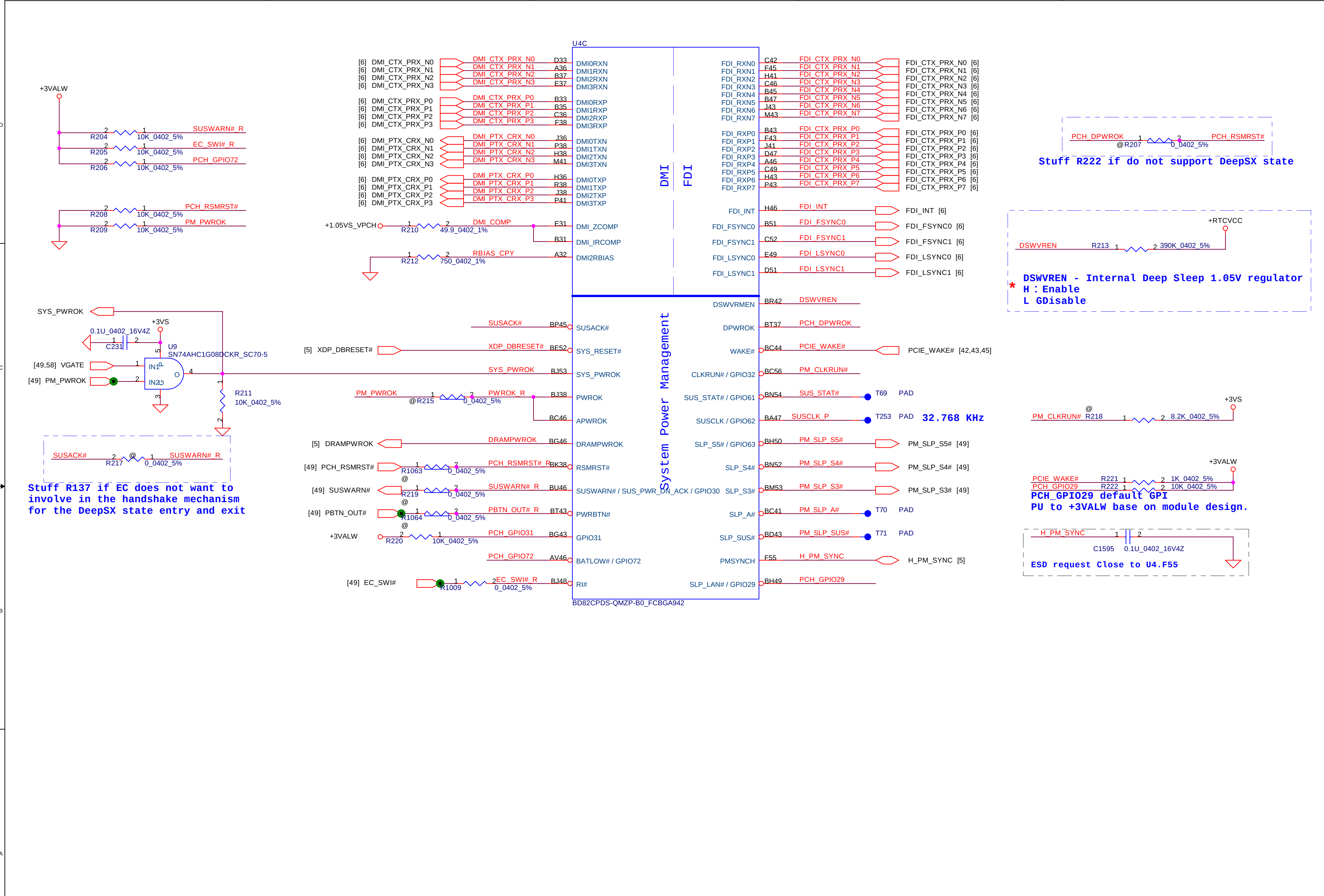

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NOTE:PCH adds support for panel power sequencing required for embedded DisplayPort support. L_VDDEN, L_BKLTEN and L_BKLTCTL pins are added on the PCH for panel power sequencing. It is important to note that a 6 layer board design may be required to access these pins on the PCH package in a fully featured platform design.

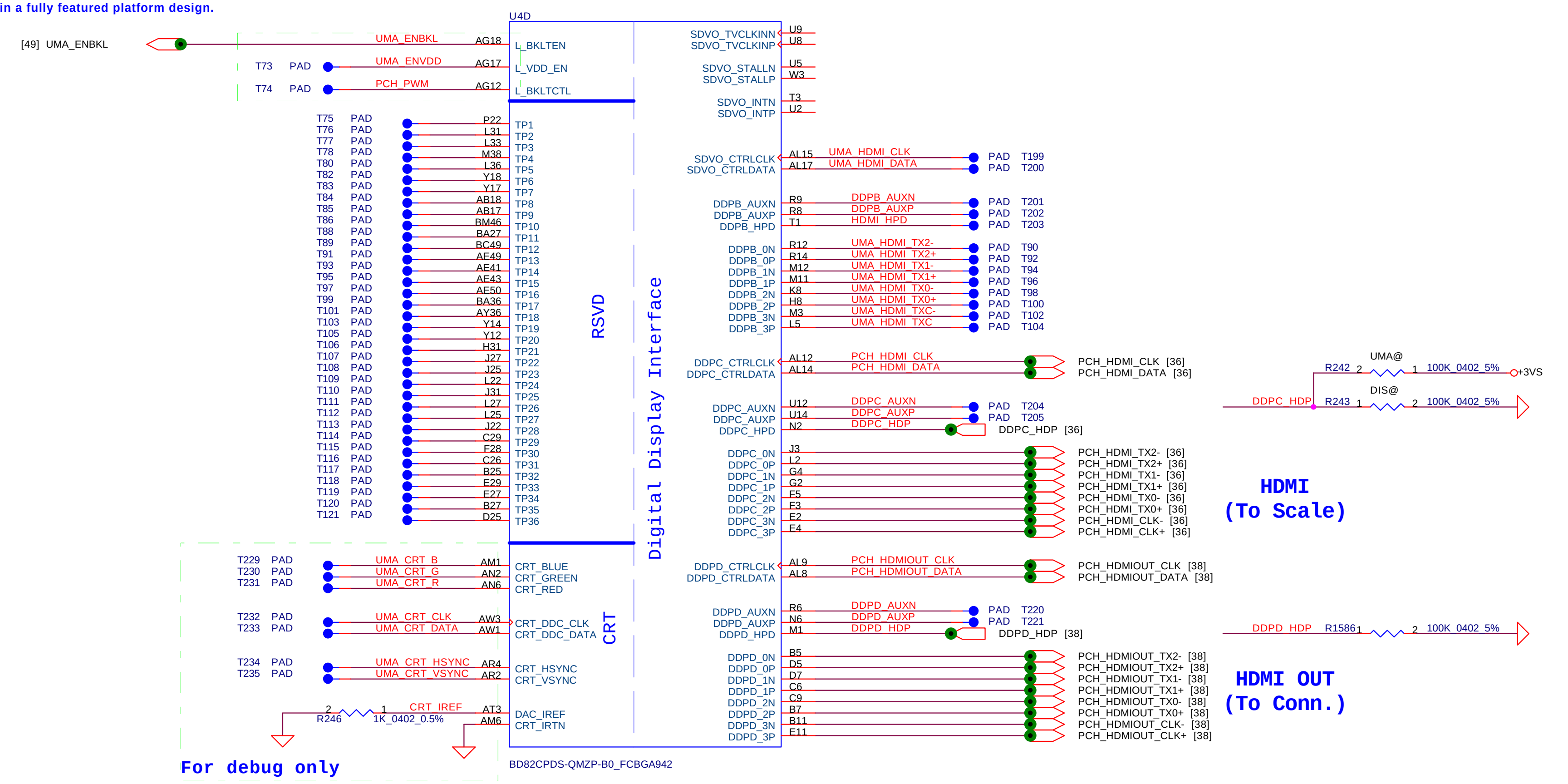

Table 5-60. PCH Digital Port Pin Mapping

Port Description	DisplayPort* Signals	HDMI* Signals	SDVO Signals	PCH Display Port Pin details
Port B	DPB_LANE3	TMDSB_CLK	SDVOB_CLK	DDPB_[3]P
	DPB_LANE3#	TMDSB_CLKB	SDVOB_CLK#	DDPB_[3]N
	DPB_LANE2	TMDSB_DATA0	SDVOB_BLUE	DDPB_[2]P
	DPB_LANE2#	TMDSB_DATA0B	SDVOB_BLUE#	DDPB_[2]N
	DPB_LANE1	TMDSB_DATA1	SDVOB_GREEN	DDPB_[1]P
	DPB_LANE1#	TMDSB_DATA1B	SDVOB_GREEN#	DDPB_[1]N
	DPB_LANE0	TMDSB_DATA2	SDVOB_RED	DDPB_[0]P
	DPB_LANE0#	TMDSB_DATA2B	SDVOB_RED*	DDPB_[0]N
	DPB_HPD	TMDSB_HPD		DDPB_HPD
	DPB_AUX			DDPB_AUXP
	DPB_AUXB			DDPB_AUXN
Port C	DPC_LANE3	TMDSC_CLK		DDPC_[3]P
	DPC_LANE3#	TMDSC_CLKB		DDPC_[3]N
	DPC_LANE2	TMDSC_DATA0		DDPC_[2]P
	DPC_LANE2#	TMDSC_DATA0B		DDPC_[2]N
	DPC_LANE1	TMDSC_DATA1		DDPC_[1]P
	DPC_LANE1#	TMDSC_DATA1B		DDPC_[1]N
	DPC_LANE0	TMDSC_DATA2		DDPC_[0]P
	DPC_LANE0#	TMDSC_DATA2B		DDPC_[0]N
	DPC_HPD	TMDSC_HPD		DDPC_HPD
	DPC_AUX			DDPC_AUXP
	DPC_AUXC			DDPC_AUXN
Port D	DPD_LANE3	TMDSD_CLK		DDPD_[3]P
	DPD_LANE3#	TMDSD_CLKB		DDPD_[3]N
	DPD_LANE2	TMDSD_DATA0		DDPD_[2]P
	DPD_LANE2#	TMDSD_DATA0B		DDPD_[2]N
	DPD_LANE1	TMDSD_DATA1		DDPD_[1]P
	DPD_LANE1#	TMDSD_DATA1B		DDPD_[1]N
	DPD_LANE0	TMDSD_DATA2		DDPD_[0]P
	DPD_LANE0#	TMDSD_DATA2B		DDPD_[0]N
	DPD_HPD	TMDSD_HPD		DDPD_HPD
	DPD_AUX			DDPD_AUXP
	DPD_AUXD			DDPD_AUXN

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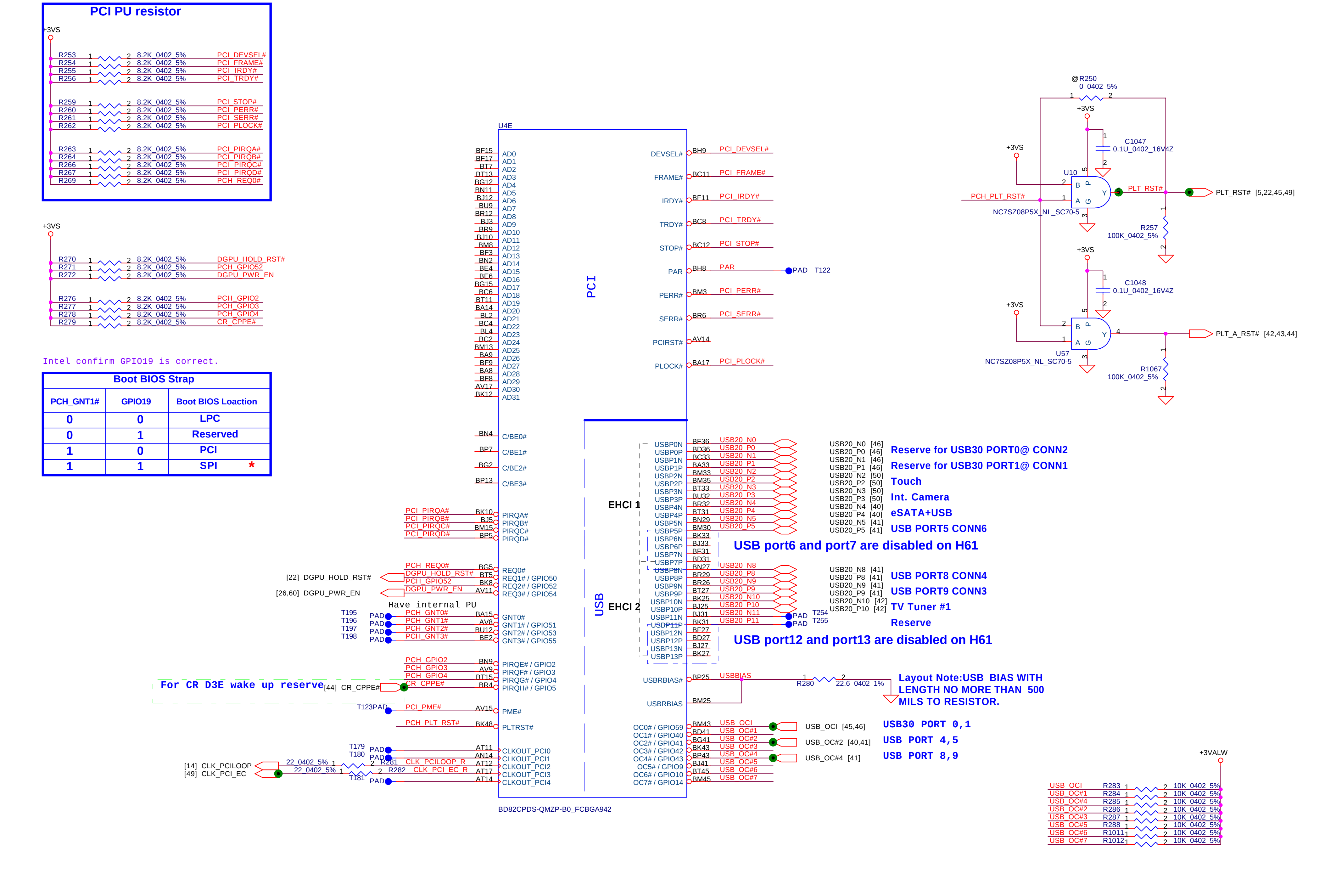

Boot BIOS Strap

PCH_GNT1#	GPIO19	Boot BIOS Loaction
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI *

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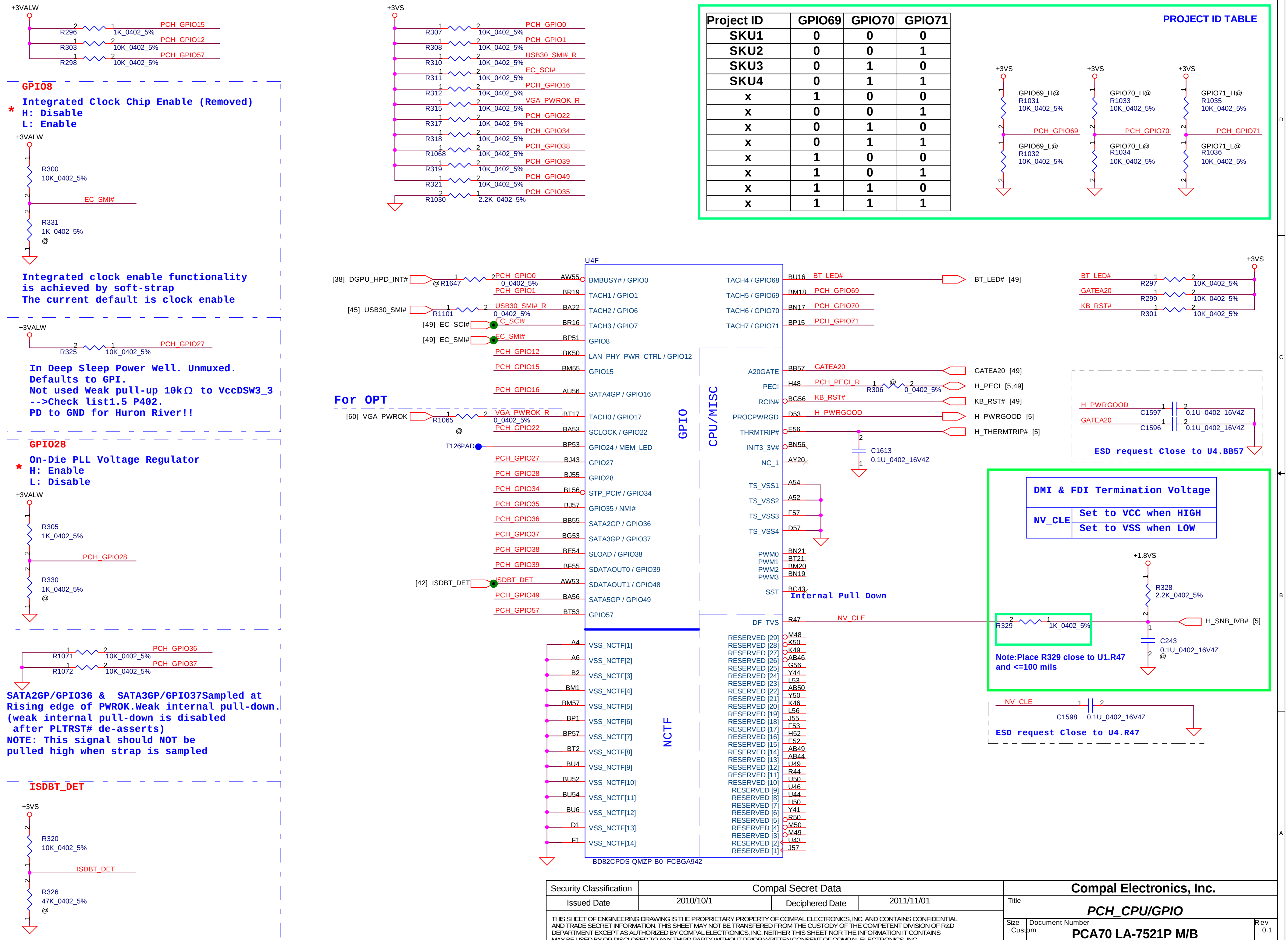


PROJECT ID TABLE

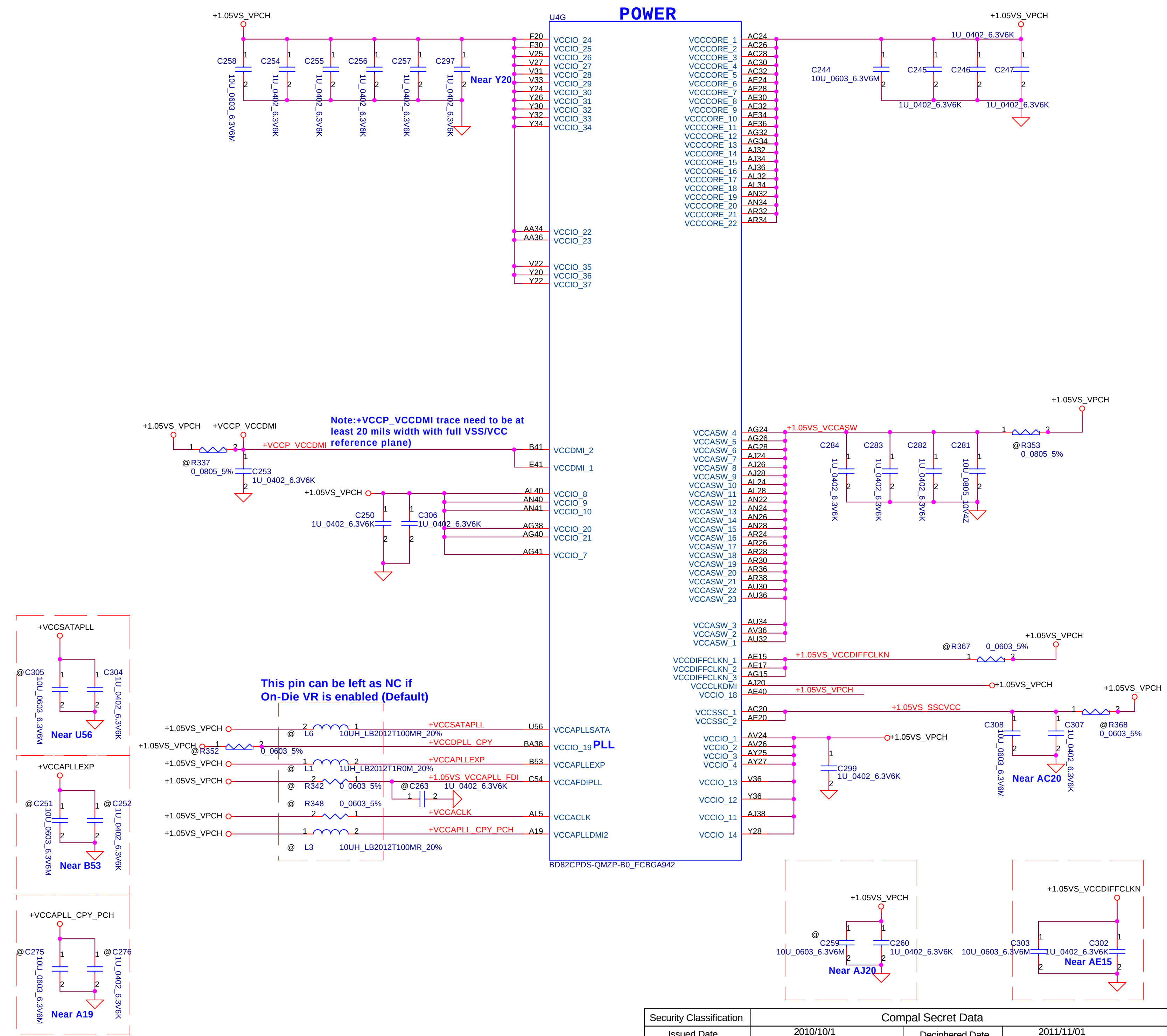
Project ID	GPIO69	GPIO70	GPIO71
SKU1	0	0	0
SKU2	0	0	1
SKU3	0	1	0
SKU4	0	1	1
x	1	0	0
x	0	0	1
x	0	1	0
x	0	1	1
x	1	0	0
x	1	0	1
x	1	1	0
x	1	1	1

Security Classification	Compal Secret Data		
Issued Date	2010/10/1	Deciphered Date	2011/11/01

Compal Electronics, Inc.

Title: PCH_CPU/GPIO

Size: Custom | Document Number: PCA70 LA-7521P M/B | Rev 0.1



PCH Power Rail Table

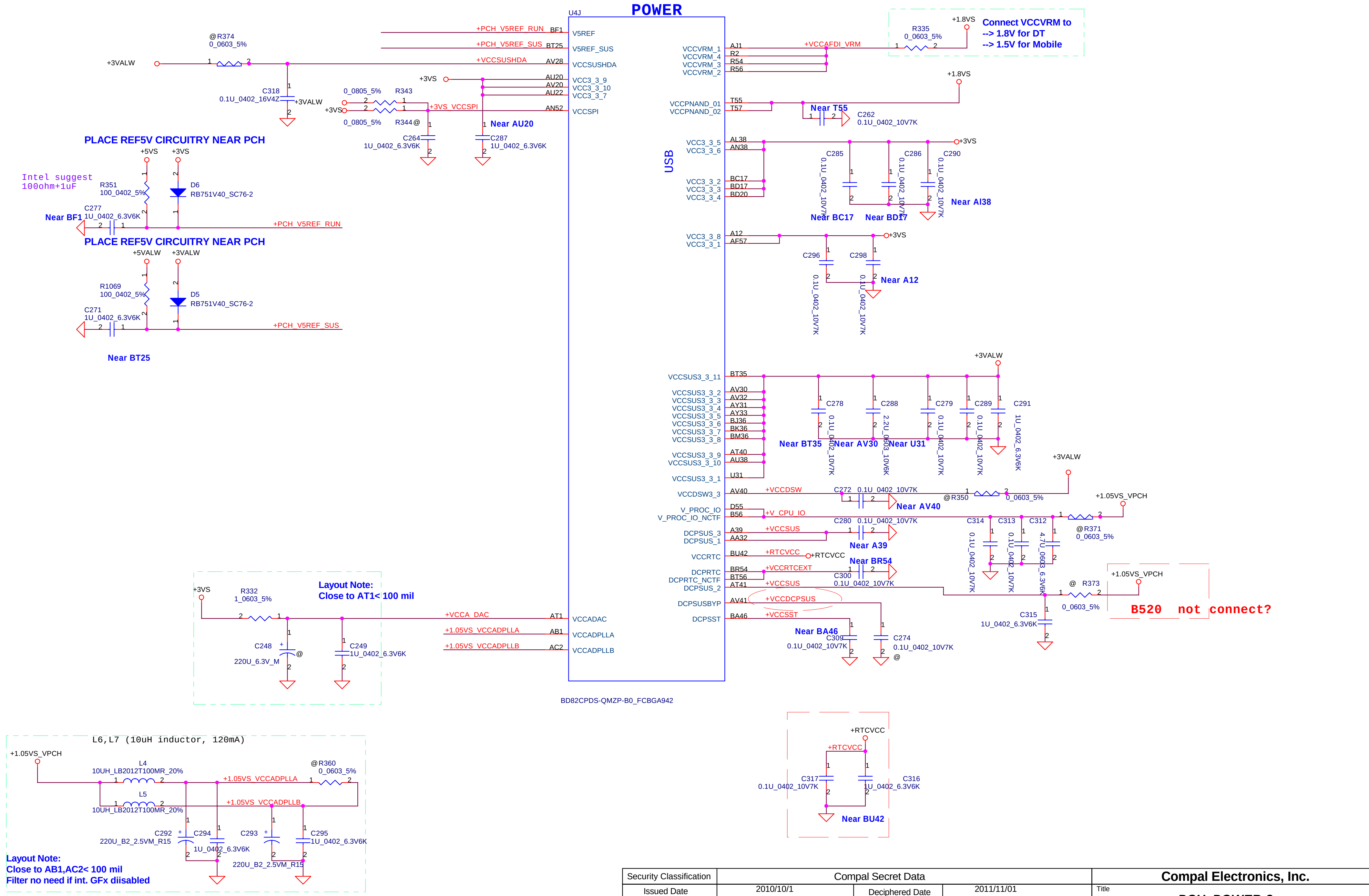
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	1mA
V5REF	5	1mA
V5REF_SUS	5	1mA
VCC3_3	3.3	409mA
VCCADAC	3.3	68mA
VCCADPLLA	1.05	100mA
VCCADPLLB	1.05	100mA
VCCCORE	1.05	1600mA
VCCDMI	1.05	57mA
VCCIO	1.05	4070mA
VCCASW	1.05	1610mA
VCCSPI	3.3	20mA
VCCDSW	3.3	3mA
VCCDFTERM	1.8	200mA
VCCRTC	3.3	6 uA
VCCSUS3_3	3.3	97mA
VCCSusHDA	3.3 / 1.5	10mA
VCCVRM	1.5	159mA
VCCCLKDMI	1.05	20mA
VCCSSC	1.05	105mA
VCCDIFFCLKN	1.05	55mA

Security Classification	Compal Secret Data		
Issued Date	2010/10/1	Deciphered Date	2011/11/01

Compal Electronics, Inc.

Title: PCH_POWER-1

Size: Custom | Document Number: PCA70 LA-7521P M/B | Rev 0.1



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Issued Date	2010/10/1	Deciphered Date 2011/11/01	Title: PCH_POWER-2
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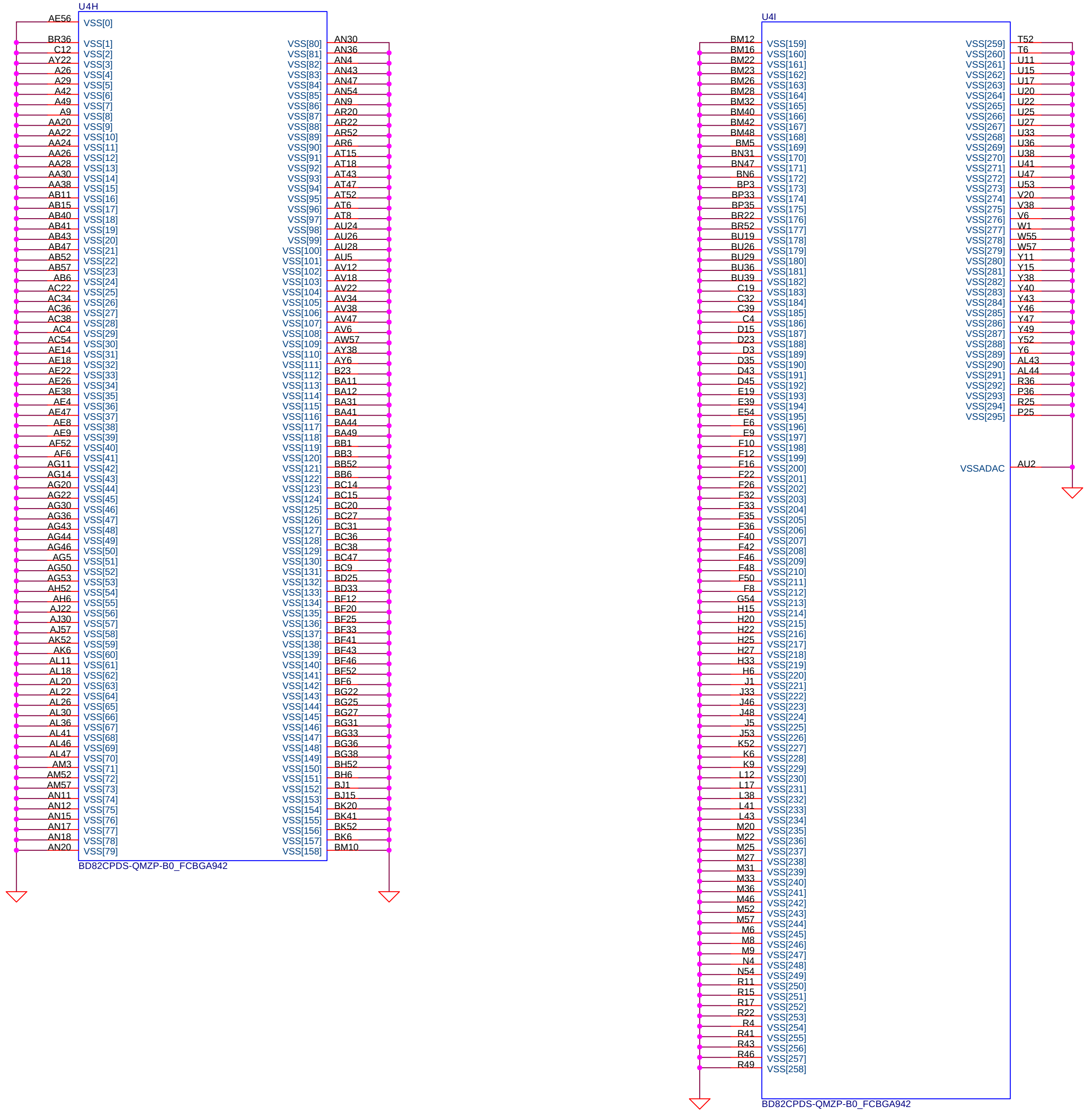
			Date: Tuesday, April 12, 2011; Sheet 20 of 64



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/10/1	Deciphered Date	2011/11/01	Title: PCH_GND
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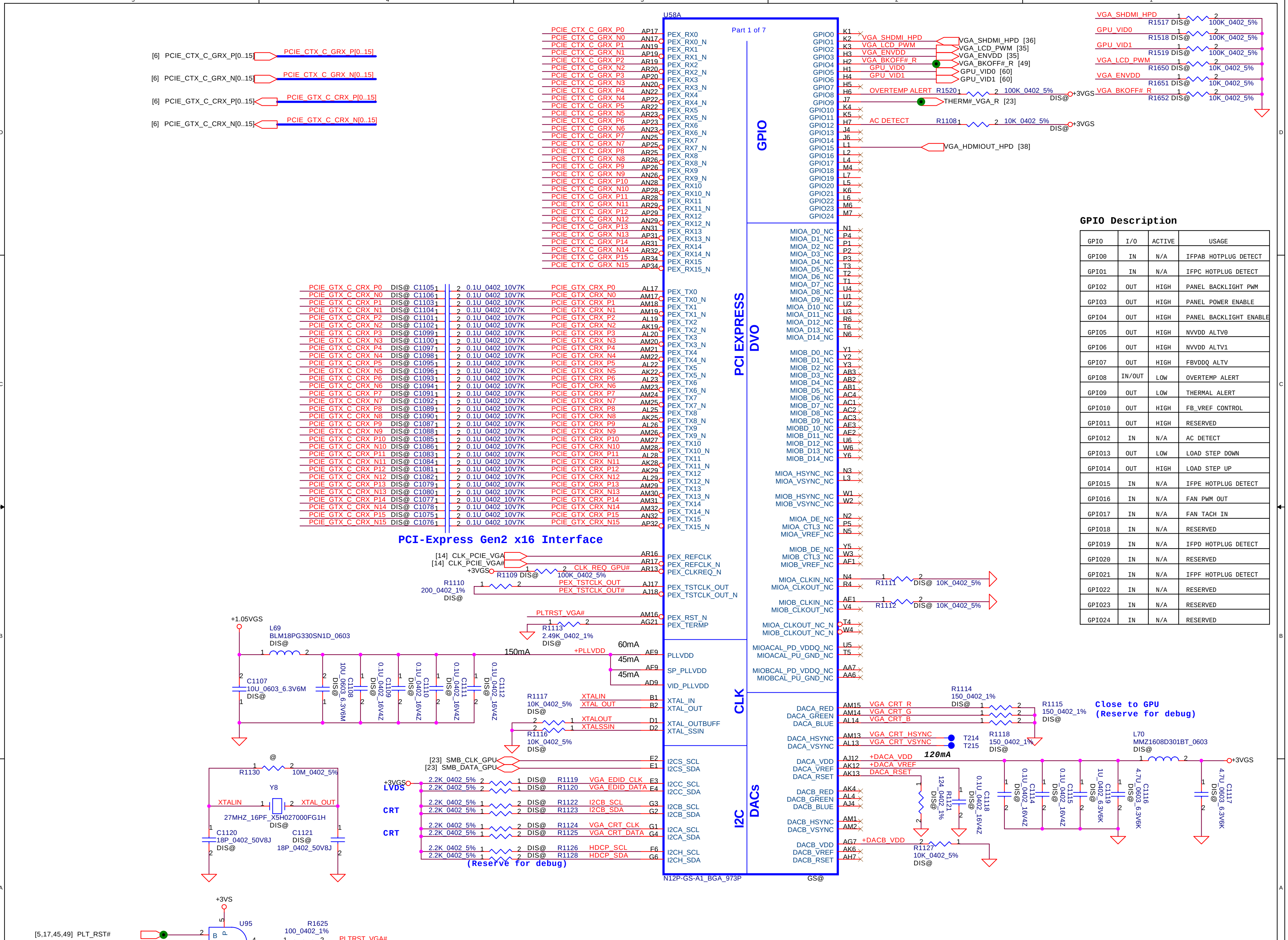
				Date: Tuesday, April 12, 2011; Sheet 21 of 64



GPIO Description

GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	IFPAB HOTPLUG DETECT
GPIO1	IN	N/A	IFPC HOTPLUG DETECT
GPIO2	OUT	HIGH	PANEL BACKLIGHT PWM
GPIO3	OUT	HIGH	PANEL POWER ENABLE
GPIO4	OUT	HIGH	PANEL BACKLIGHT ENABLE
GPIO5	OUT	HIGH	NVVDD ALTV0
GPIO6	OUT	HIGH	NVVDD ALTV1
GPIO7	OUT	HIGH	FBVDDQ ALTV
GPIO8	IN/OUT	LOW	OVERTEMP ALERT
GPIO9	OUT	LOW	THERMAL ALERT
GPIO10	OUT	HIGH	FB_VREF CONTROL
GPIO11	OUT	HIGH	RESERVED
GPIO12	IN	N/A	AC DETECT
GPIO13	OUT	LOW	LOAD STEP DOWN
GPIO14	OUT	HIGH	LOAD STEP UP
GPIO15	IN	N/A	IFPE HOTPLUG DETECT
GPIO16	IN	N/A	FAN PWM OUT
GPIO17	IN	N/A	FAN TACH IN
GPIO18	IN	N/A	RESERVED
GPIO19	IN	N/A	IFPD HOTPLUG DETECT
GPIO20	IN	N/A	RESERVED
GPIO21	IN	N/A	IFPF HOTPLUG DETECT
GPIO22	IN	N/A	RESERVED
GPIO23	IN	N/A	RESERVED
GPIO24	IN	N/A	RESERVED

Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

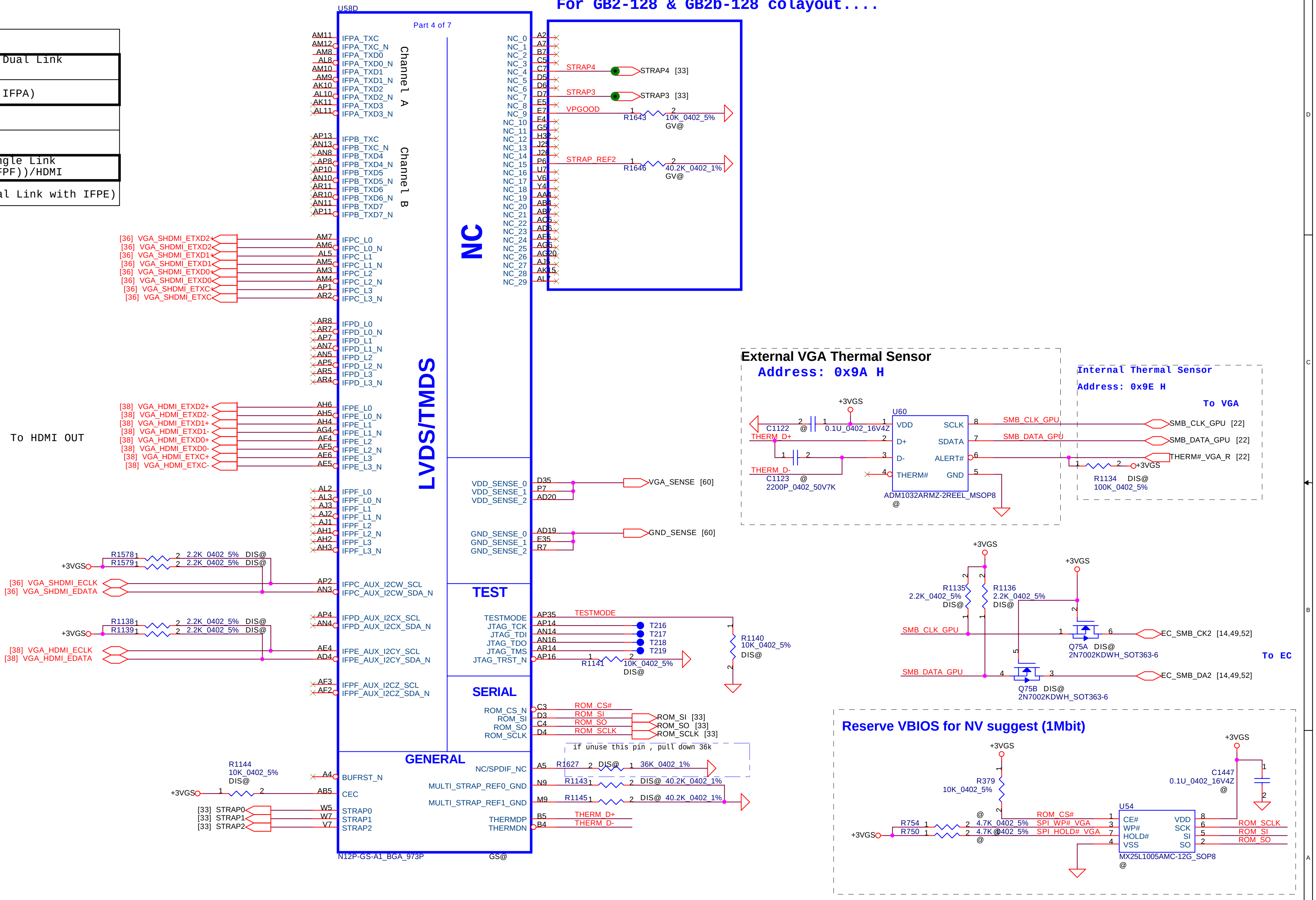
Compal Electronics, Inc.

Title: VGA_PCIE/DAC/GPIO

Size | Document Number: PCA70 LA-7521P M/B | Rev 0.1

Date: Tuesday, April 12, 2011 |

Display	Interface Support
LinkA	LVDS(Single Link or Dual Link with IFPB)
LinkB	LVDS(Dual Link with IFPA)
LinkC	Display Port/HDMI
LinkD	Display Port/eDP
LinkE	Display Port/DVI(Single Link or Dual Link with IFPF))/HDMI
LinkF	Display Port/DVI(Dual Link with IFPE)



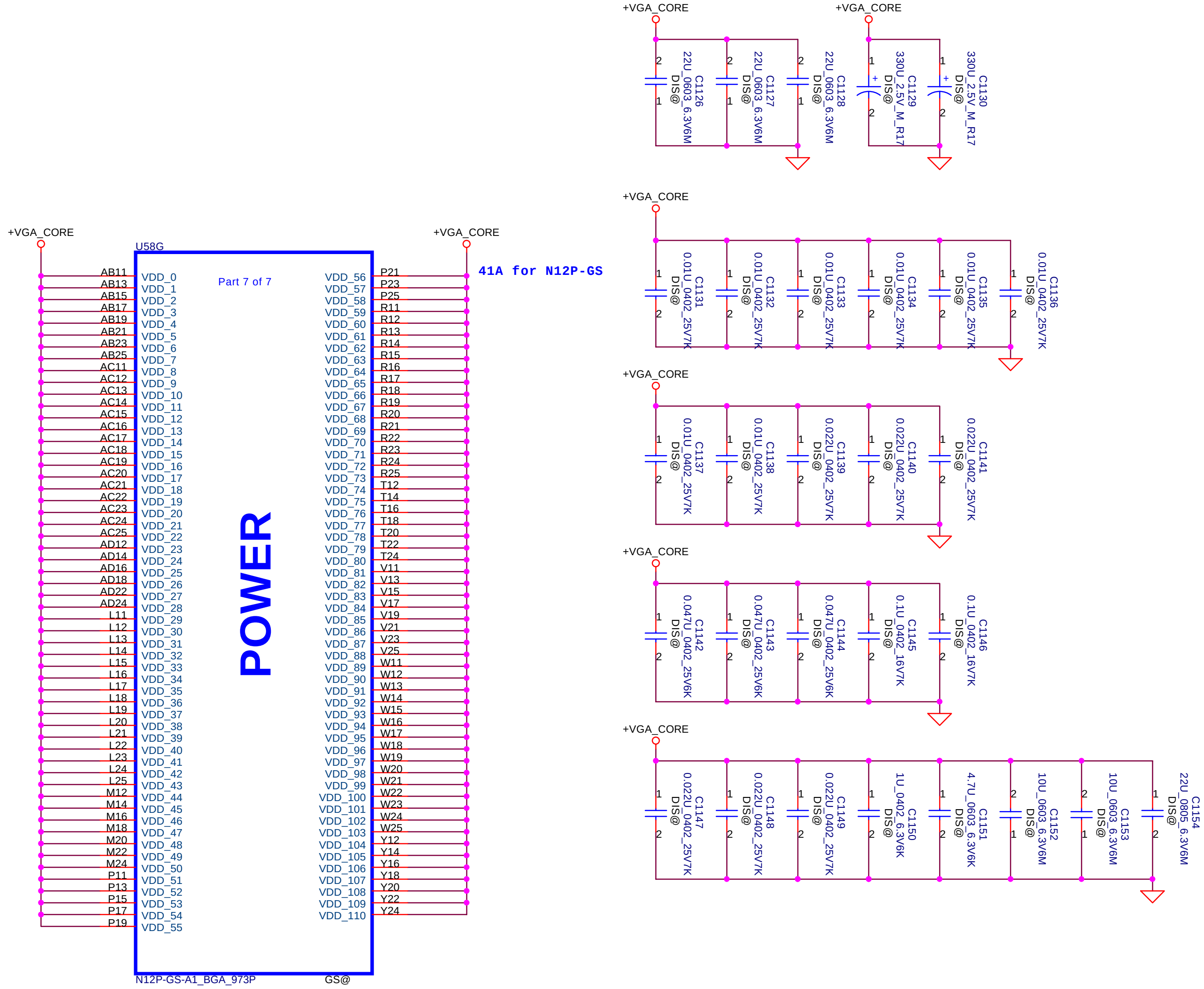
Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

Compal Electronics, Inc.

Title: VGA_LVDS/HDMI/THERM/eDP

Size | Document Number: PCA70 LA-7521P M/B | Rev 0.1

Date: Tuesday, April 12, 2011



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2009/01/01	Deciphered Date	2010/01/01	Title: VGA_VGA CORE	
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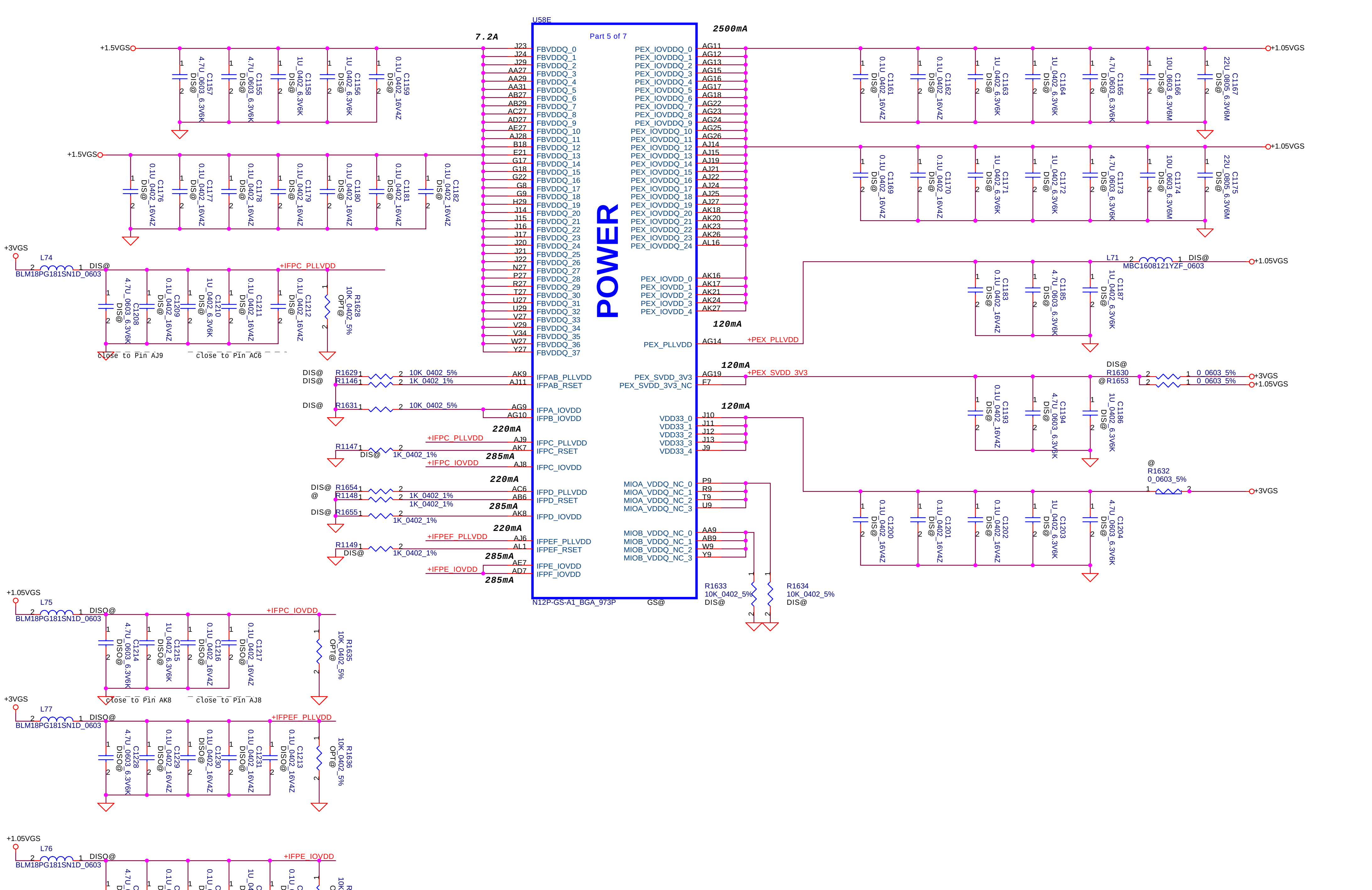
				Date: Tuesday, April 12, 2011	Sheet 24 of 64



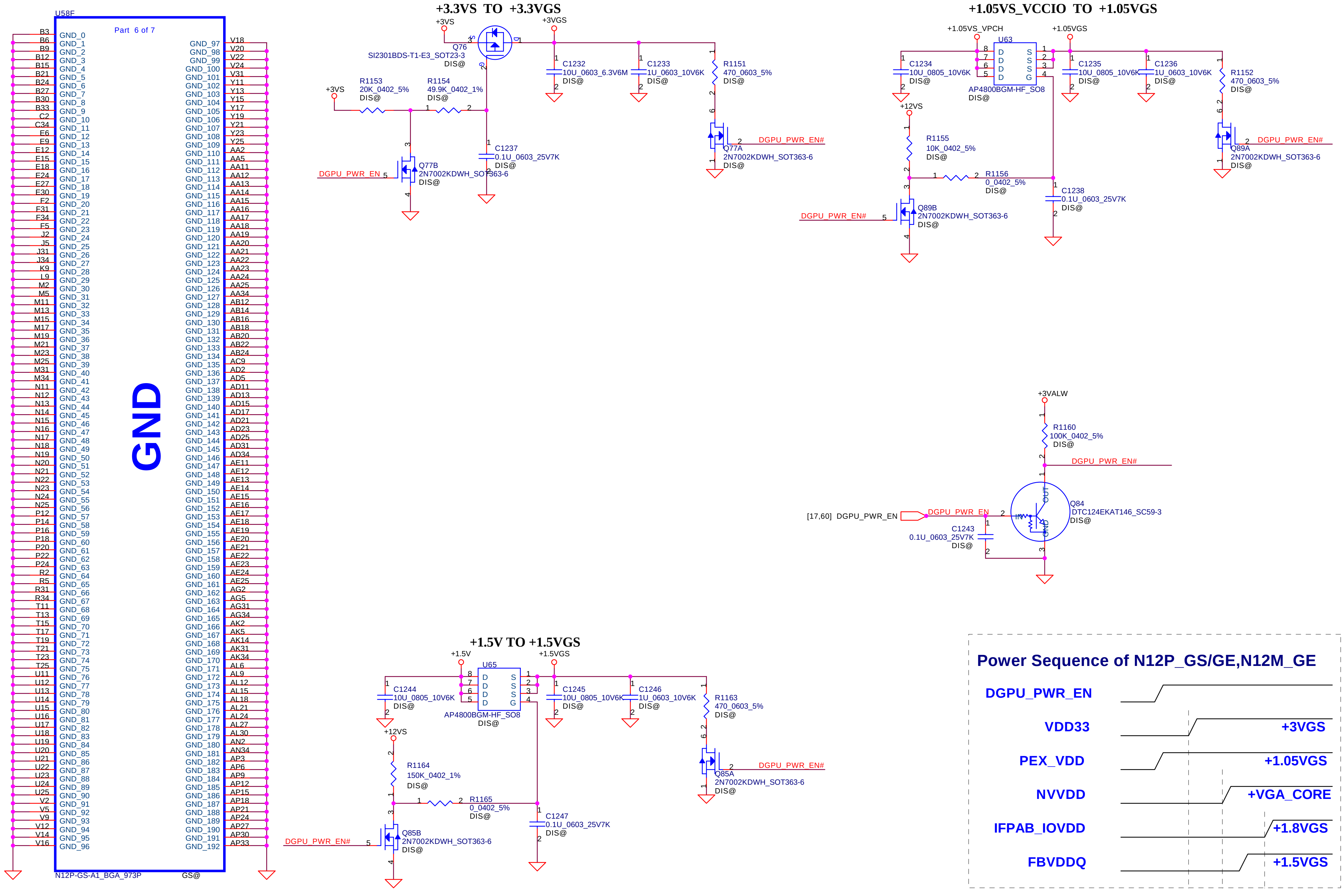
Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

Compal Electronics, Inc.

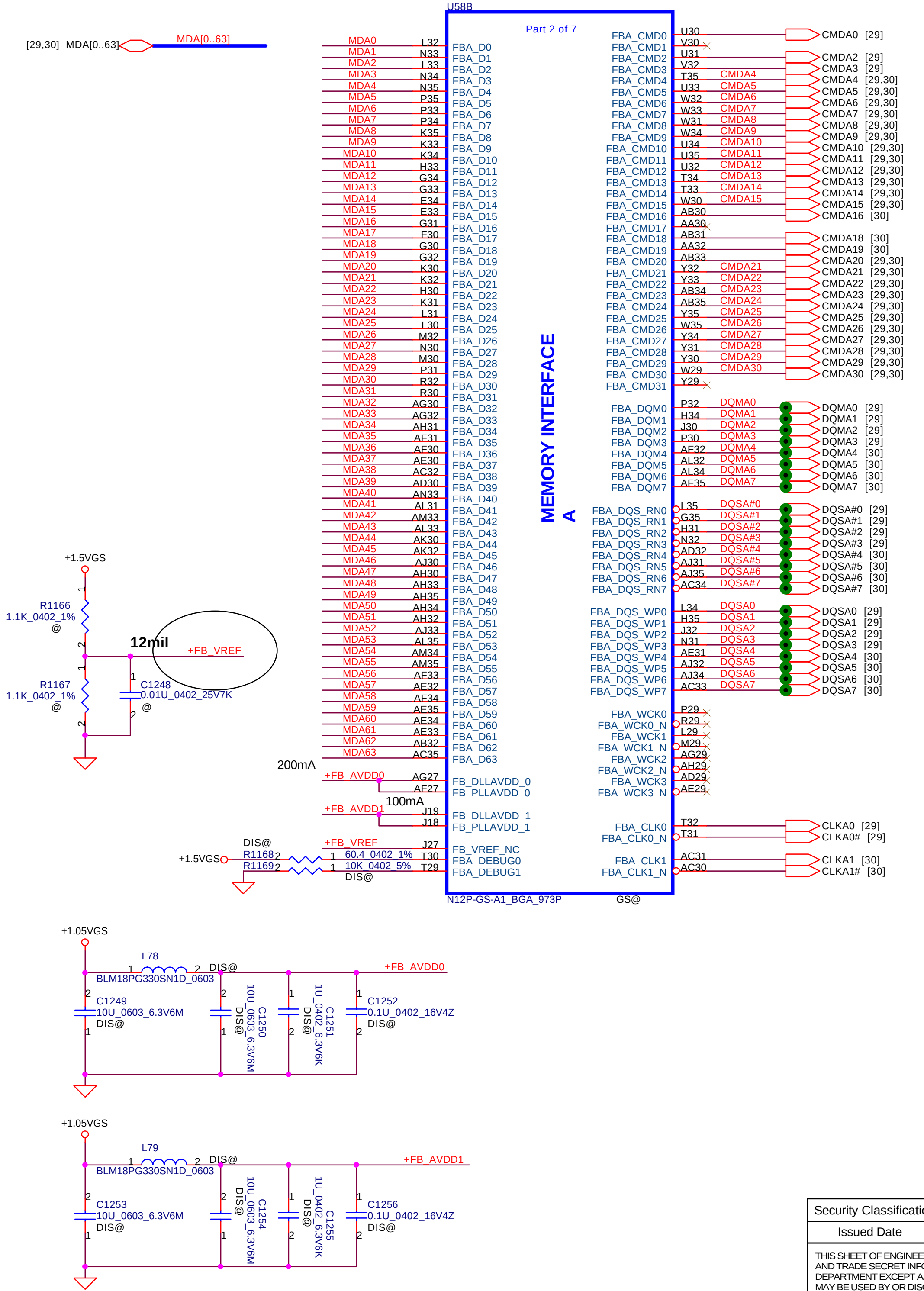
Title: VGA_POWER

Size | Document Number: PCA70 LA-7521P M/B | Rev 0.1

Date: Tuesday, April 12, 2011



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2009/01/01	Deciphered Date	2010/01/01	Title: VGA_GND/POWER
				Size / Document Number: PCA70 LA-7521P M/B / Rev 0.1
				Date: Tuesday, April 12, 2011 / Sheet 26 of 64



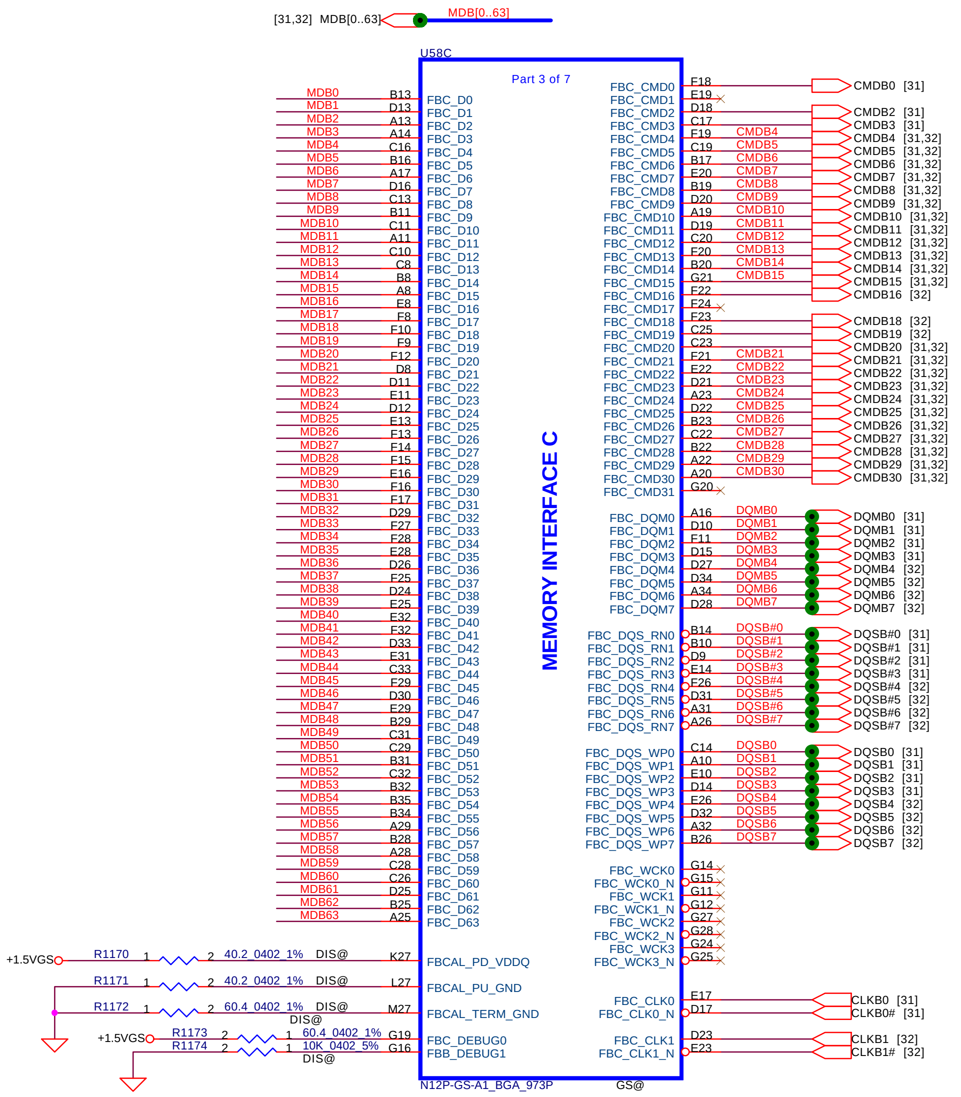
Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

Compal Electronics, Inc.

Title: VGA_MEM Interface A

Size | Document Number: PCA70 LA-7521P M/B | Rev 0.1

Date: Tuesday, April 12, 2011 |



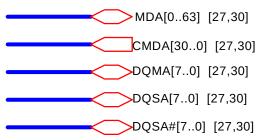
Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

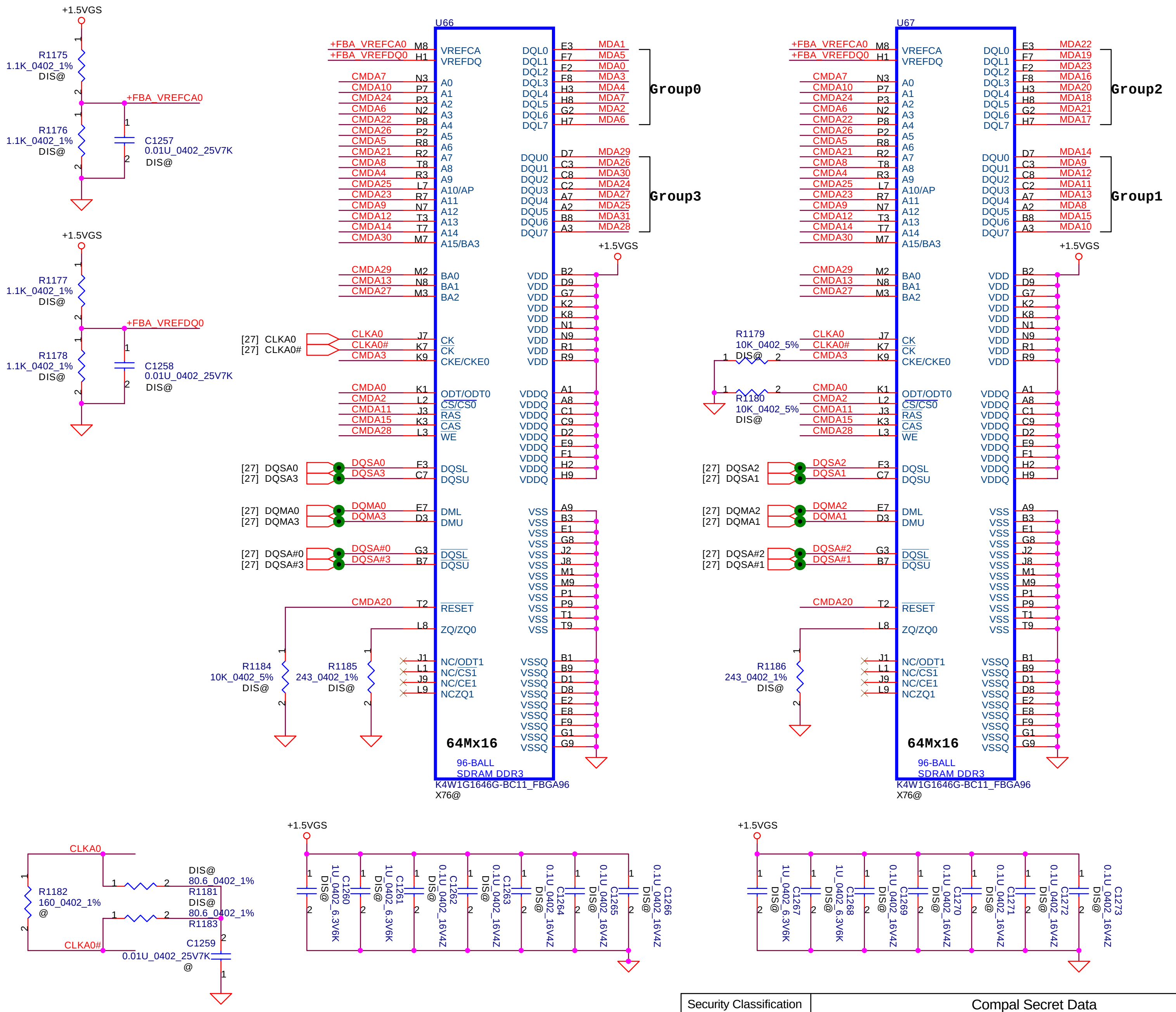
Compal Electronics, Inc.

Title: *VGA_MEM Interface C*

Size | Document Number: **PCA70 LA-7521P M/B** | Rev 0.1

Memory Partition A - Lower 32 bits





GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

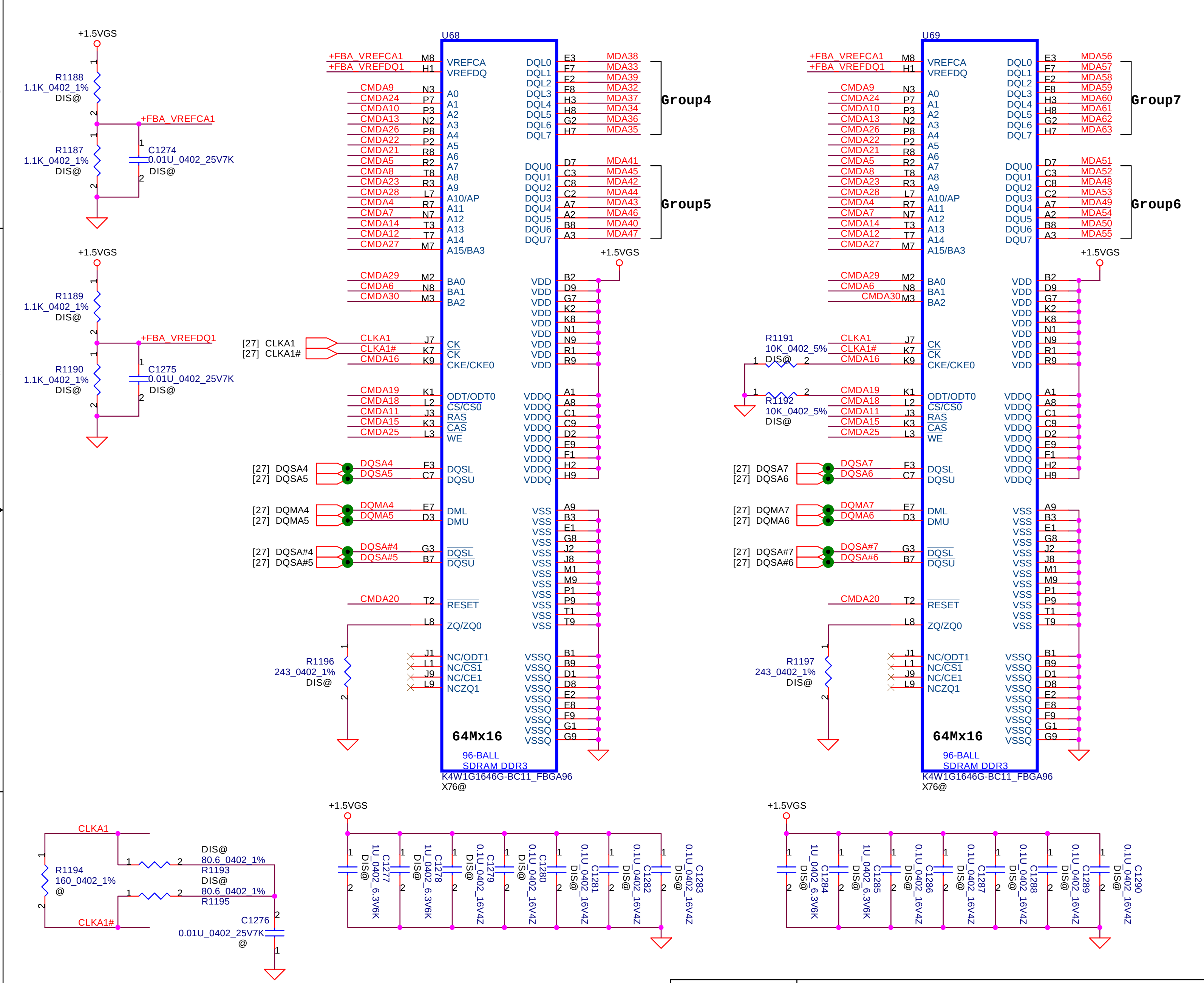
Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

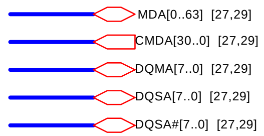
Compal Electronics, Inc.

Title: *VGA_VRAM_A Lower*

Size | Document Number: PCA70 LA-7521P M/B | Rev 0.1

Memory Partition A - Upper 32 bits





GB2-128
Mode E - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

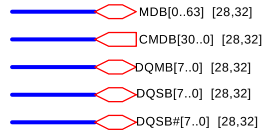
Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

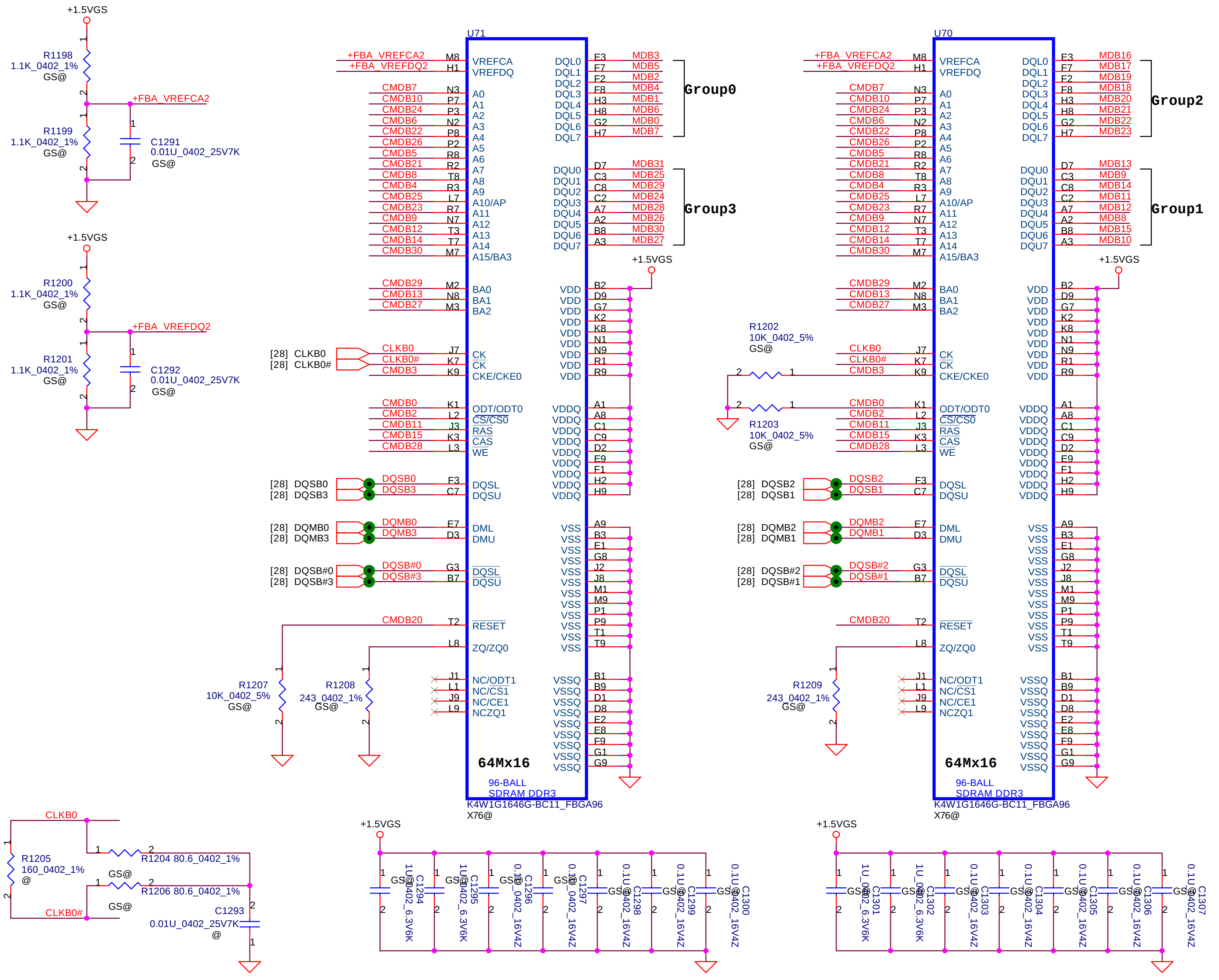
Compal Electronics, Inc.

Title: *VGA_VRAM_A Upper*

Size | Document Number: **PCA70 LA-7521P M/B** | Rev 0.1

Memory Partition C - Lower 32 bits





GB2-128
Mode E - Mirror Mode Mapping

Address	DATA Bus 0..31	DATA Bus 32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

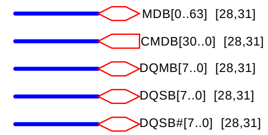
Compal Electronics, Inc.

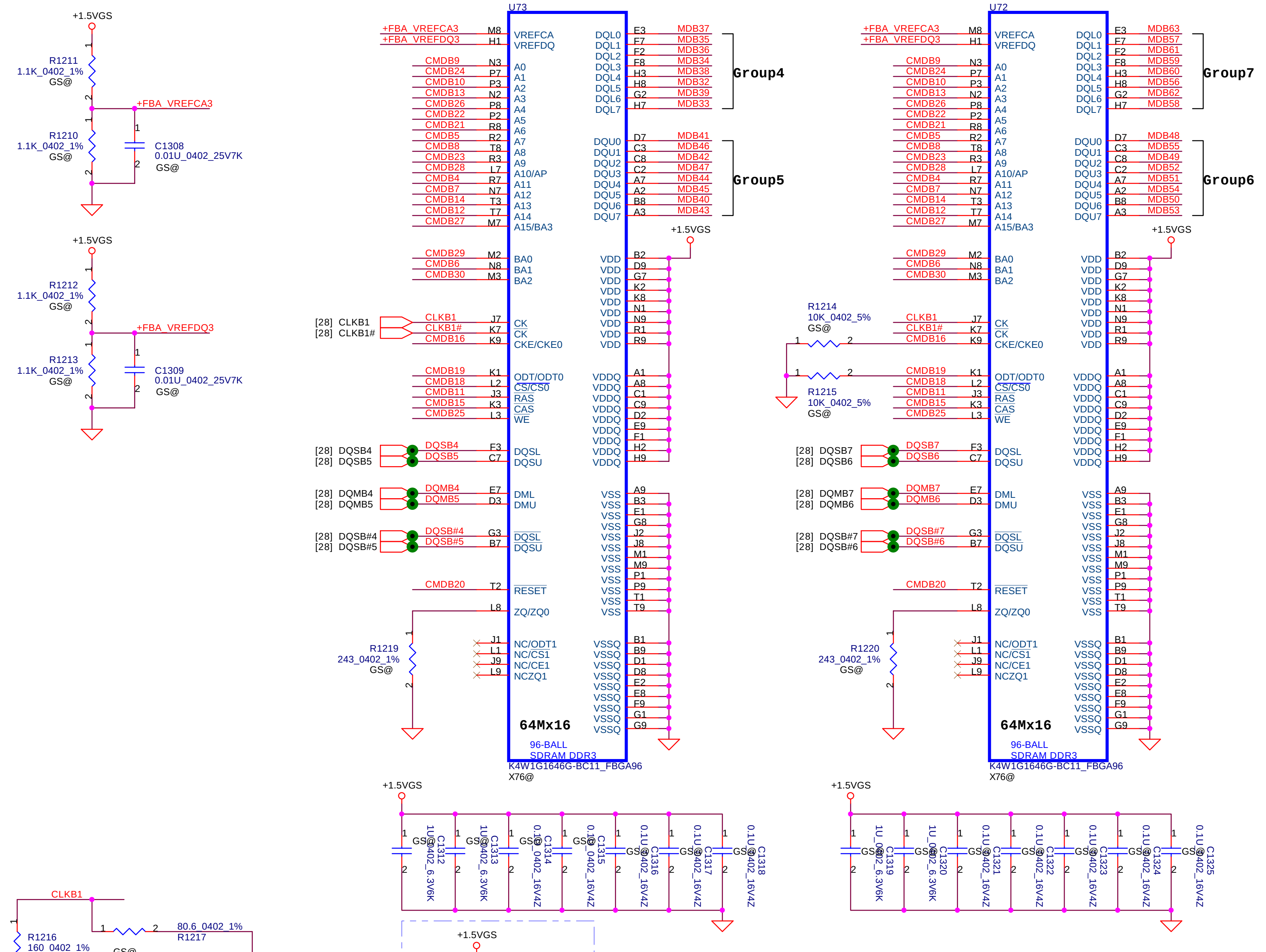
Title: VGA_VRAM_C Lower

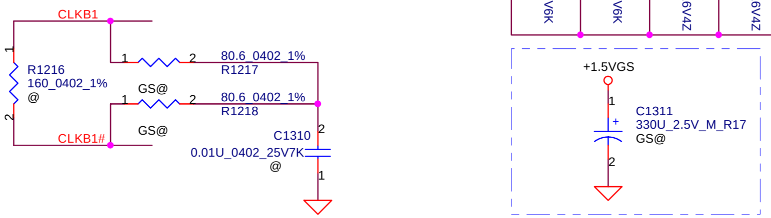
Size: Custom | Document Number: PCA70 LA-7521P M/B | Rev: 0.1

Date: Tuesday, April 12, 2011 |

Memory Partition C - Upper 32 bits







GB2-128
Mode E - Mirror Mode Mapping

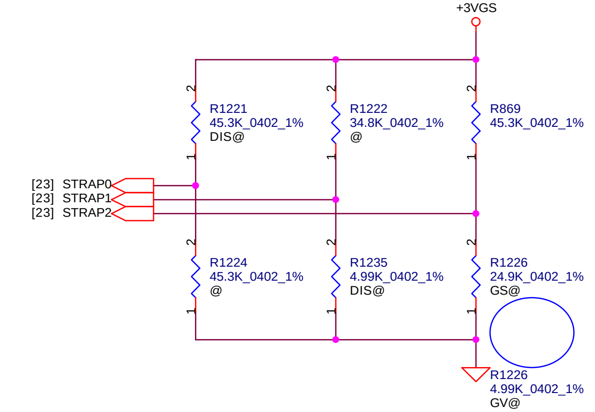
	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

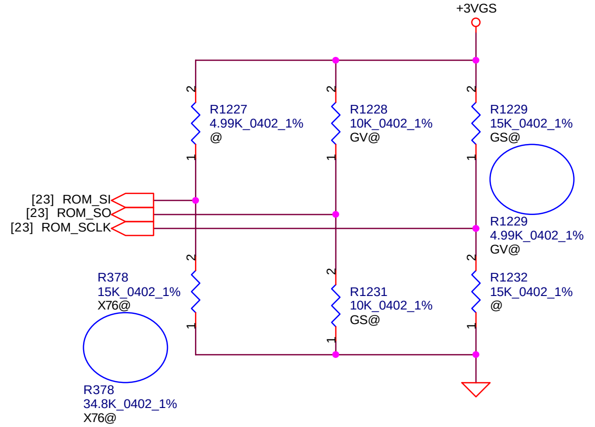
Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

Compal Electronics, Inc.

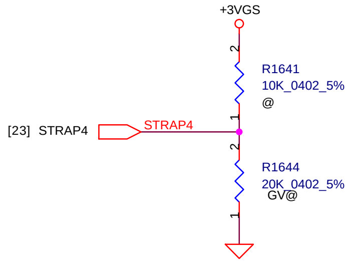
Title: VGA_VRAM_C Upper

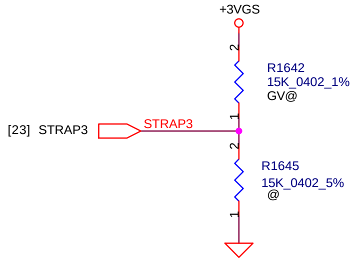
Size: Custom | Document Number: PCA70 LA-7521P M/B | Rev: 0.1





Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111





Physical Strapping pin		Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	GS	+3VGS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
	GV		FB[1]	FB[0]		
ROM_SCLK	GS	+3VGS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
	GV				PCI_DEVID[5]	
ROM_SI		+3VGS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP0		+3VGS	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1		+3VGS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2		+3VGS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3		+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4		+3VGS	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

User [3:0]	
1111	EDID is used 1920x1080
1000-1100	Customer defined

3GIO_PADCFG[3:0]	
0000	RESERVED
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLOCK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

PCIE_MAX_SPEED	
1	Default

DP_PLL_VDD33V	
0	Default

GPU	Package	DeviceID	PCI_DEVID[5..0]
N12P-GS	GB2-128	0x0DF4	(..1111 0100)
N12P-GV-B	GB2b-128	0x1050	(..0101 0000)

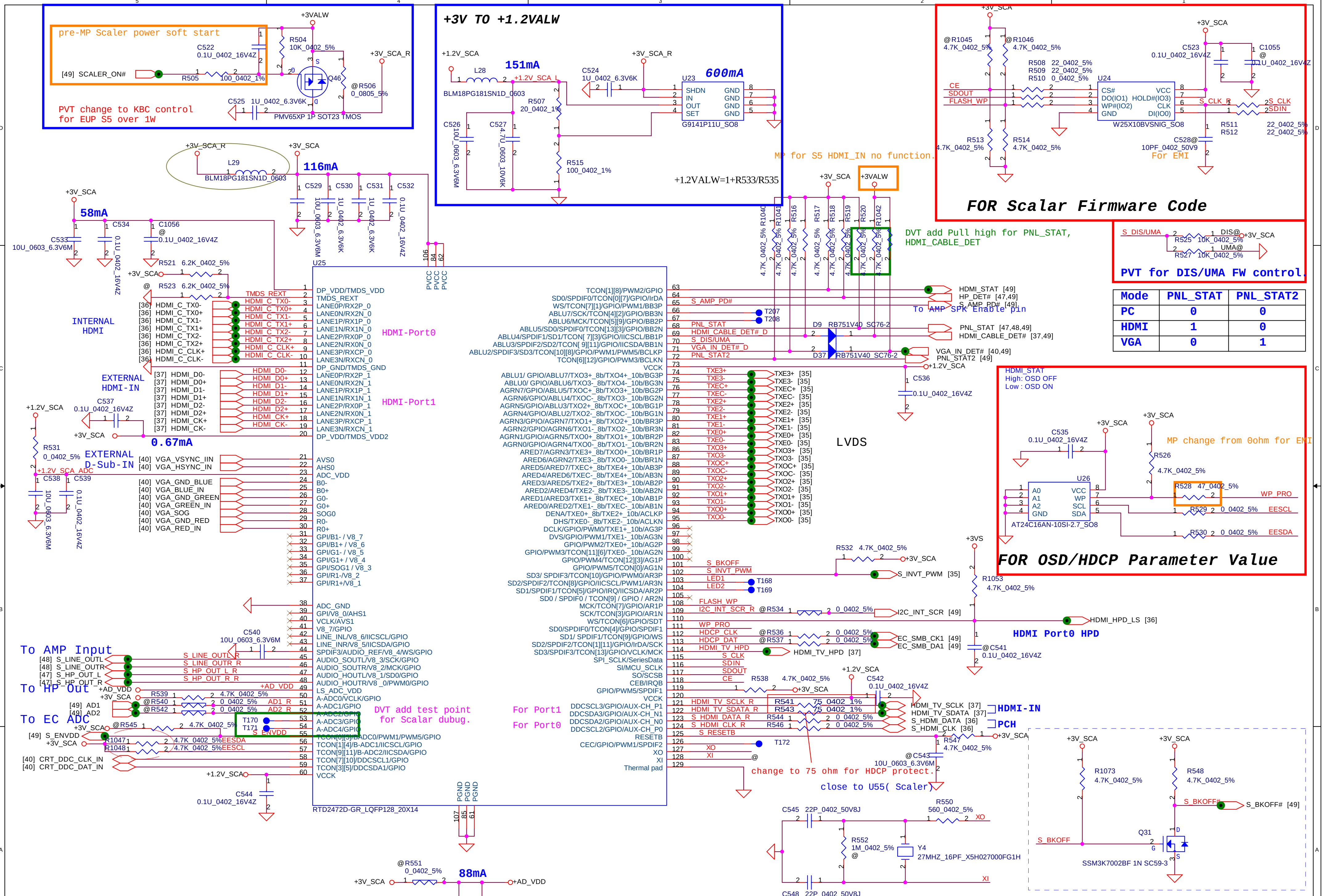
GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N12P-GS	900 MHz	64M* 16* 8 1GB	Hynix (0x2) H5TQ1G63DFR-11C SA000041S60	1111 R1221 PU 45K	0000 R1235 PD 5K	0100 R1226 PD 25K	NC	NC	0010 R453 PD 15K	0001 R1231 PD 10K	1010 R1229 PU 15K
N12P-GS	900 MHz	64M* 16* 8 1GB	Samsung (0x3) K4W1G1646G-BC11 SA00004GS30	1111 R1221 PU 45K	0000 R1235 PD 5K	0100 R1226 PD 25K	NC	NC	0011 R378 PD 20K	0001 R1231 PD 10K	1010 R1229 PU 15K
N12P-GV	900 MHz	64M* 16* 4 512MB	Hynix (0x2) H5TQ1G63DFR-11C SA000041S60	1111 R1221 PU 45K	0000 R1235 PD 5K	0000 R1226 PD 5K	1010 R1642 PU 15K	0011 R1644 PD 20K	0010 R378 PD 15K	1001 R1228 PU 10K	1000 R1229 PU 5K
N12P-GV	900 MHz	64M* 16* 4 512MB	Samsung (0x3) K4W1G1646G-BC11 SA00004GS30	1111 R1221 PU 45K	0000 R1235 PD 5K	0000 R1226 PD 5K	1010 R1642 PU 15K	0011 R1644 PD 20K	0011 R378 PD 20K	1001 R1228 PU 10K	1000 R1229 PU 5K
N12P-GV	800 MHz	128M* 16* 4 1GB	Hynix (0x6) H5TQ2G63BFR-12C SA00003VS30	1111 R1221 PU 45K	0000 R1235 PD 5K	0000 R1226 PD 5K	1010 R1642 PU 15K	0011 R1644 PD 20K	0110 R378 PD 35K	1001 R1228 PU 10K	1000 R1229 PU 5K

Security Classification	Compal Secret Data		
Issued Date	2009/01/01	Deciphered Date	2010/01/01

Compal Electronics, Inc.

Title: VGA_MSIC

Size: Custom | Document Number: PCA70 LA-7521P M/B | Rev 0.1

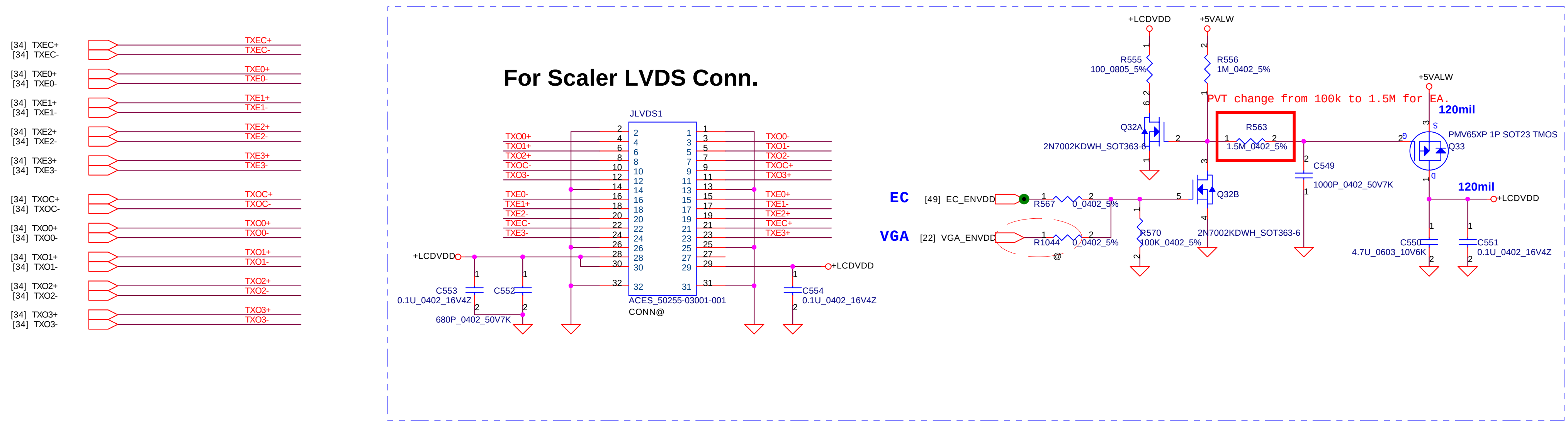


Mode	PNL_STAT	PNL_STAT2
PC	0	0
HDMI	1	0
VGA	0	1

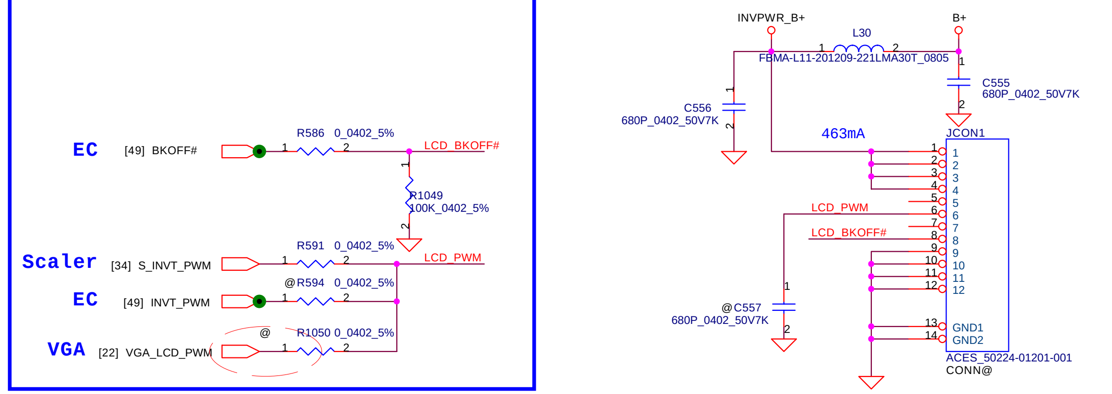
Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/10/1	Deciphered Date	2011/11/01	Title: Scaler RTD2472/82D

Size | Document Number: PCA70 LA-7521P M/B | Rev 0.1

Date: Tuesday, April 12, 2011 |



Converter



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/10/1	Deciphered Date	2011/11/01	Title: LVDS
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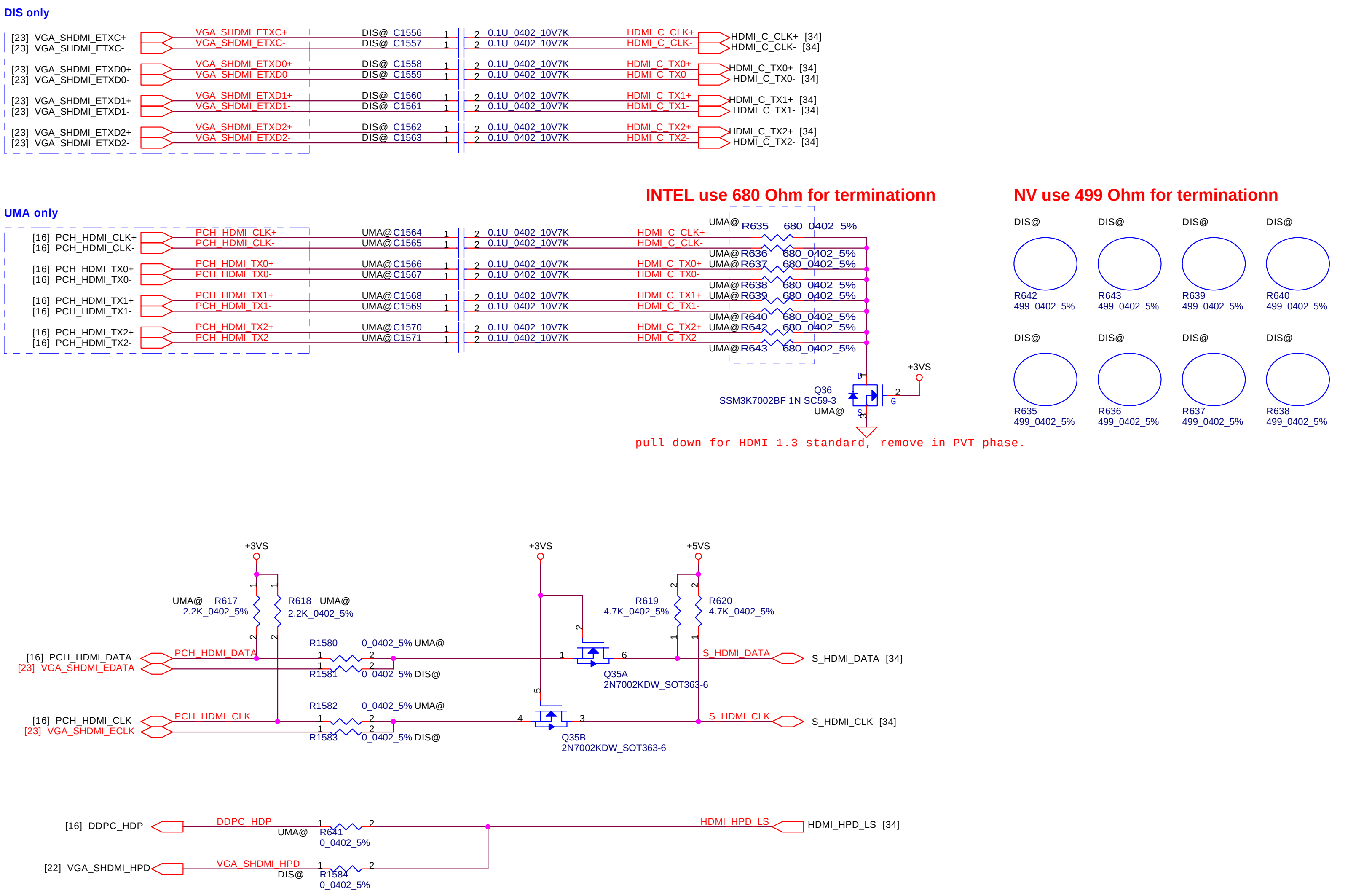
				Date: Tuesday, April 12, 2011; Sheet 35 of 64



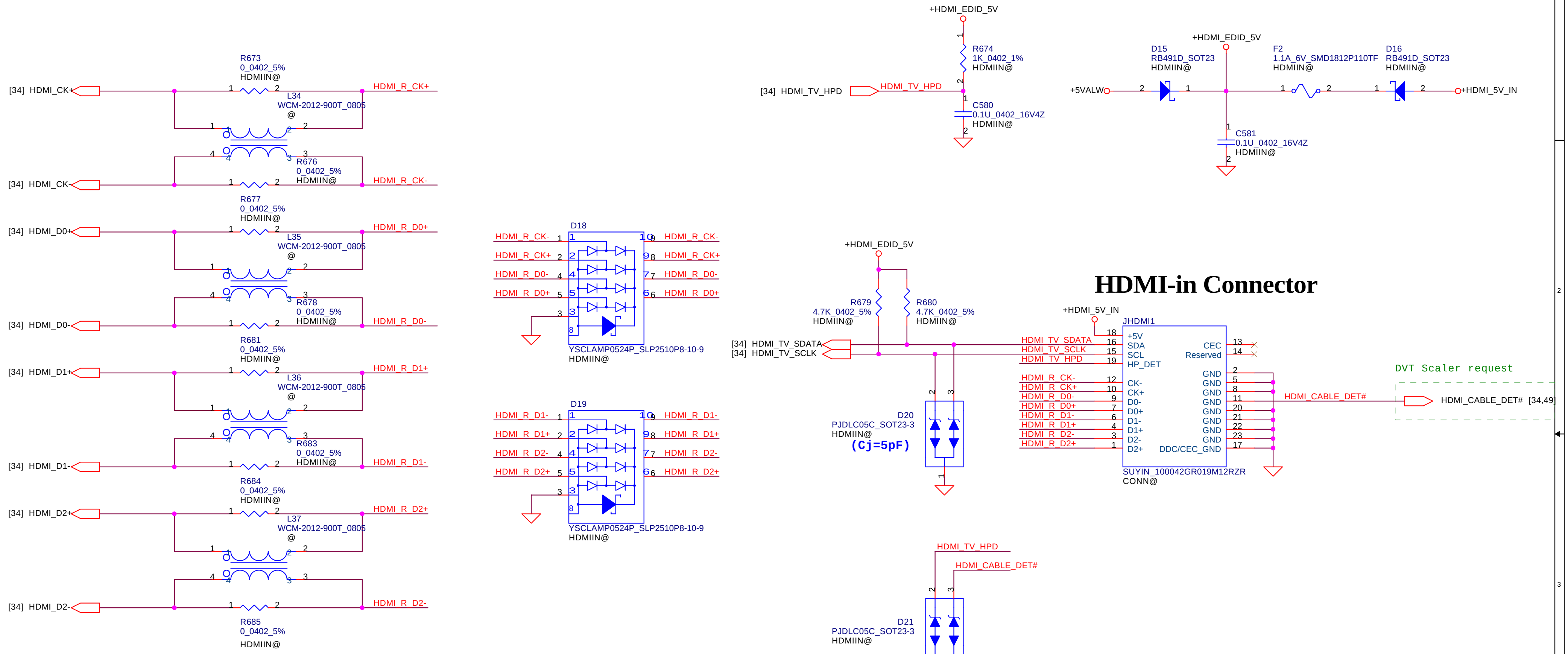
Security Classification	Compal Secret Data		
Issued Date	2010/10/1	Deciphered Date	2011/11/01

Compal Electronics, Inc.

Title: ***HDMI Level Shift Scaler***

Size: Custom | Document Number: **PCA70 LA-7521P M/B** | Rev 0.1

Date: Tuesday, April 12, 2011 |



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2010/10/1	Deciphered Date	2011/11/01	Title: HDMI-IN	
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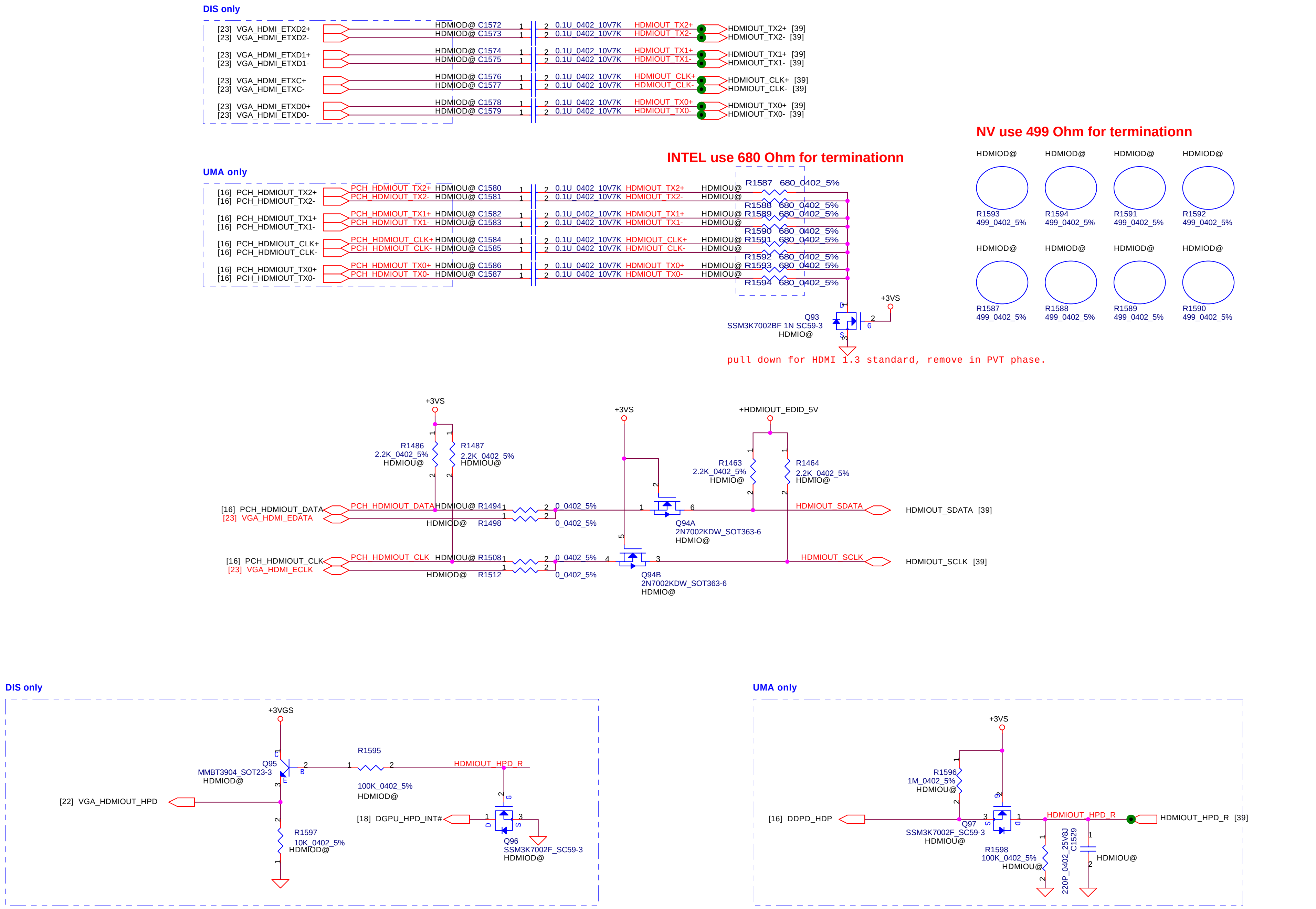
				Date: Tuesday, April 12, 2011	Sheet 37 of 64



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/10/1	Deciphered Date	2011/11/01	Title: HDMI-OUT Level Shift
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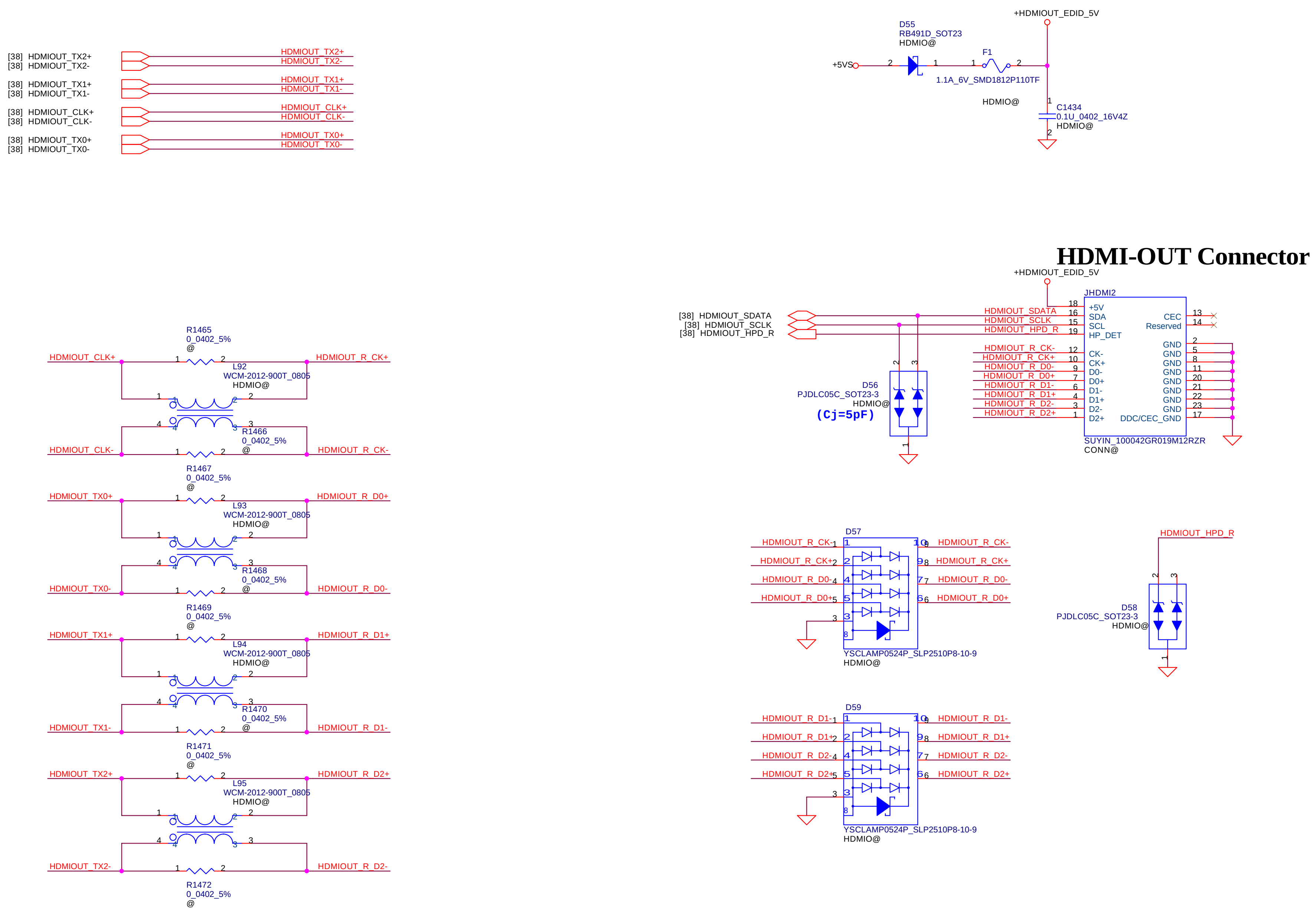
				Date: Tuesday, April 12, 2011; Sheet 38 of 64



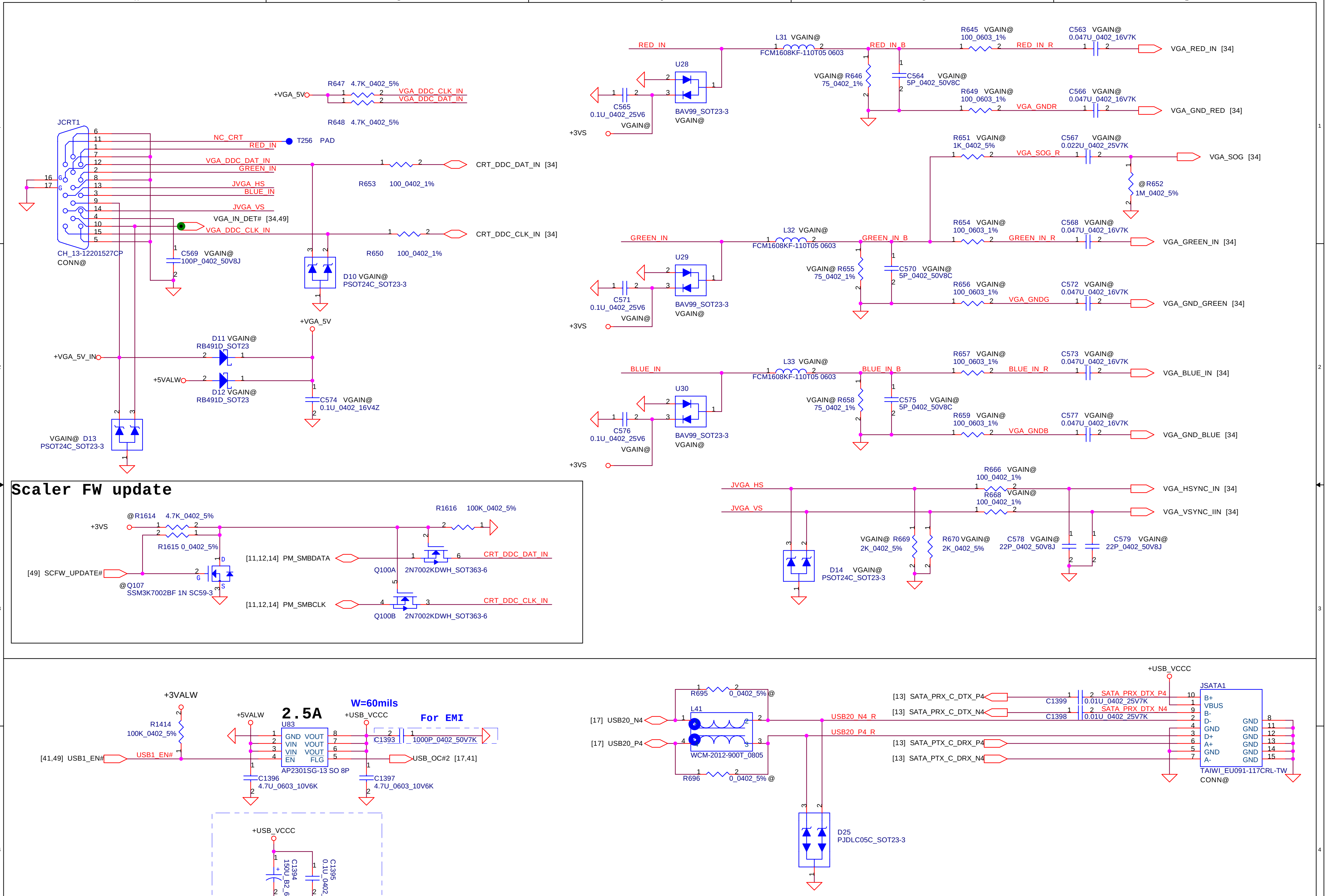
Security Classification	Compal Secret Data		
Issued Date	2010/10/1	Deciphered Date	2011/11/01

Compal Electronics, Inc.

Title: **HDMI-OUT**

Size: Custom | Document Number: **PCA70 LA-7521P M/B** | Rev: 0.1

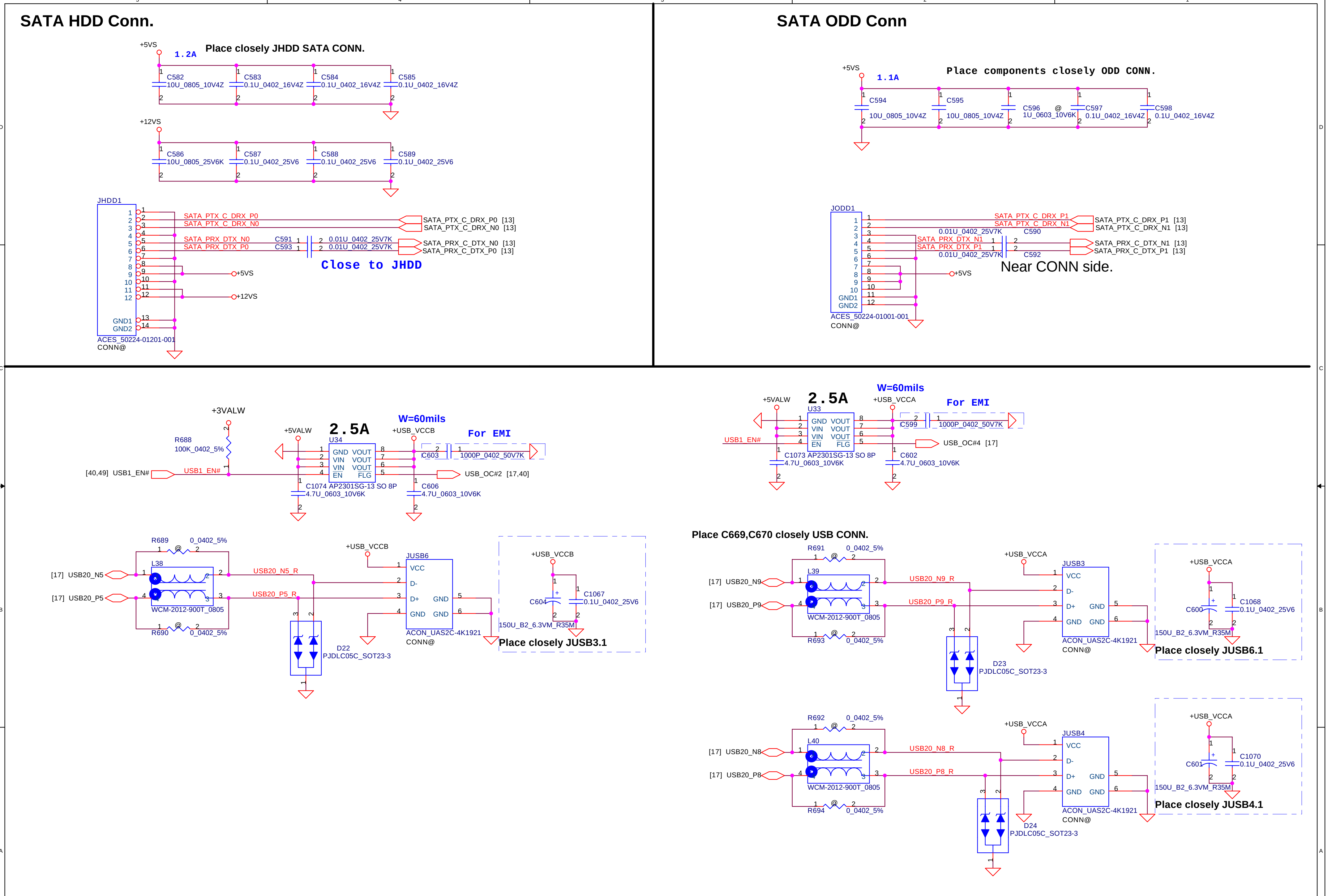
Date: Tuesday, April 12, 2011 |



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/10/1	Deciphered Date	2011/11/01	Title: CRT-IN Connector

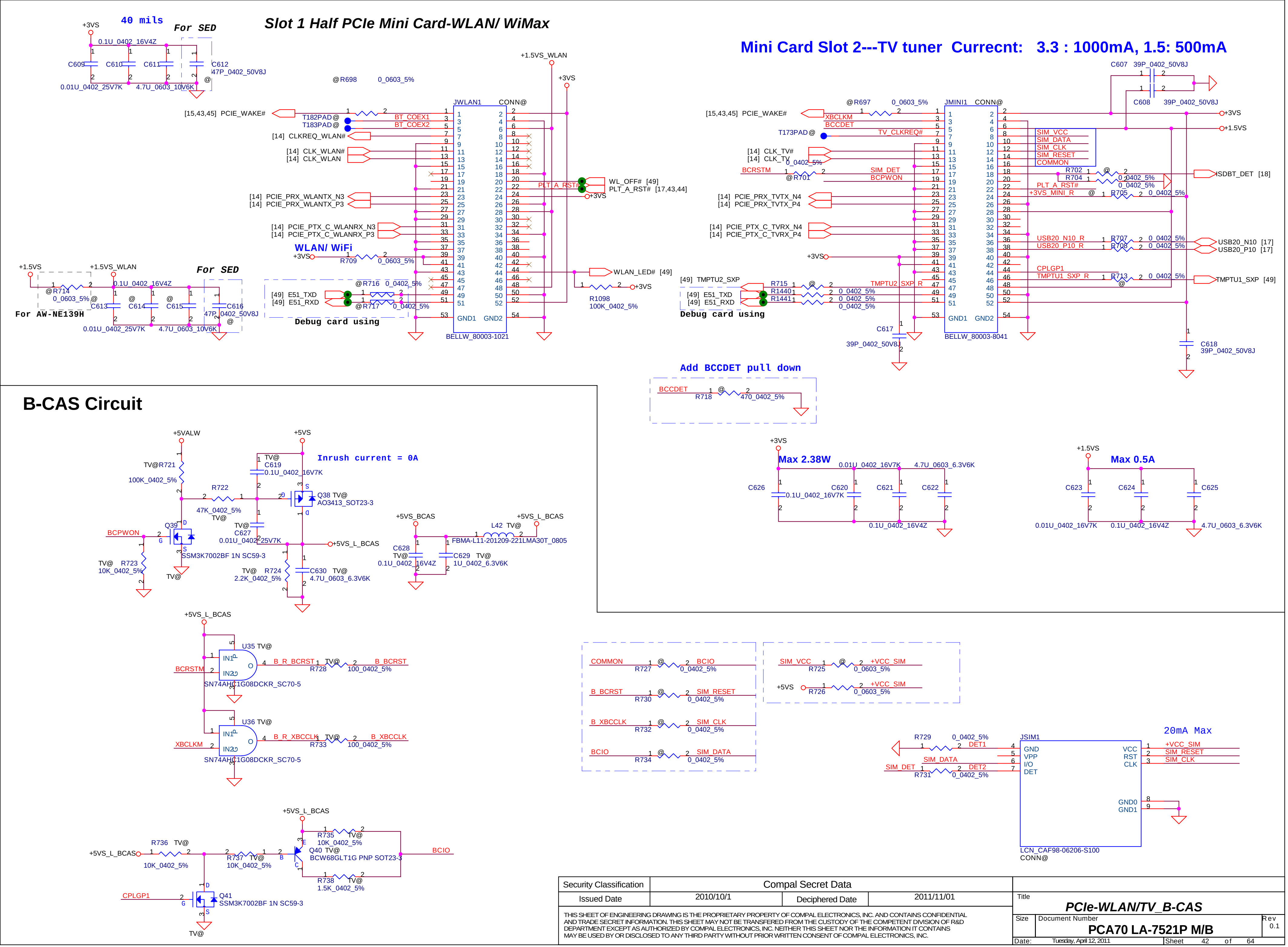
Size	Document Number	Rev
Custom	PCA70 LA-7521P M/B	0.1

Date: Tuesday, April 12, 2011 Sheet 40 of 64



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/10/1	Deciphered Date	2011/11/01	Title: SATA-HDD/ODD/USB

Size | Document Number: PCA70 LA-7521P M/B | Rev 0.1

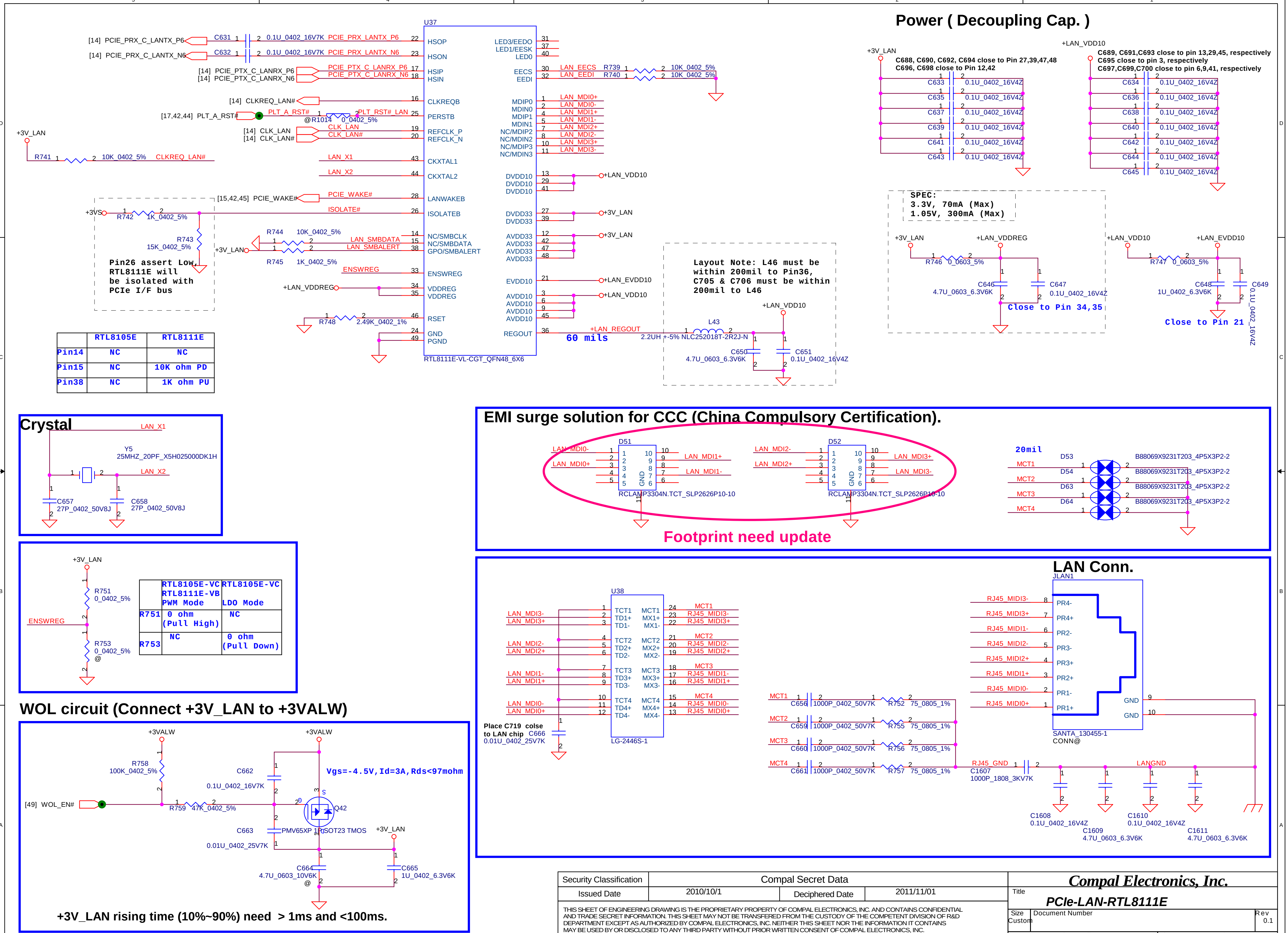


Security Classification	Compal Secret Data		
Issued Date	2010/10/1	Deciphered Date	2011/11/01

Title: PCIe-WLAN/TV_B-CAS

Size | Document Number: PCA70 LA-7521P M/B | Rev 0.1

Date: Tuesday, April 12, 2011



	RTL8105E	RTL8111E
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	NC	1K ohm PU

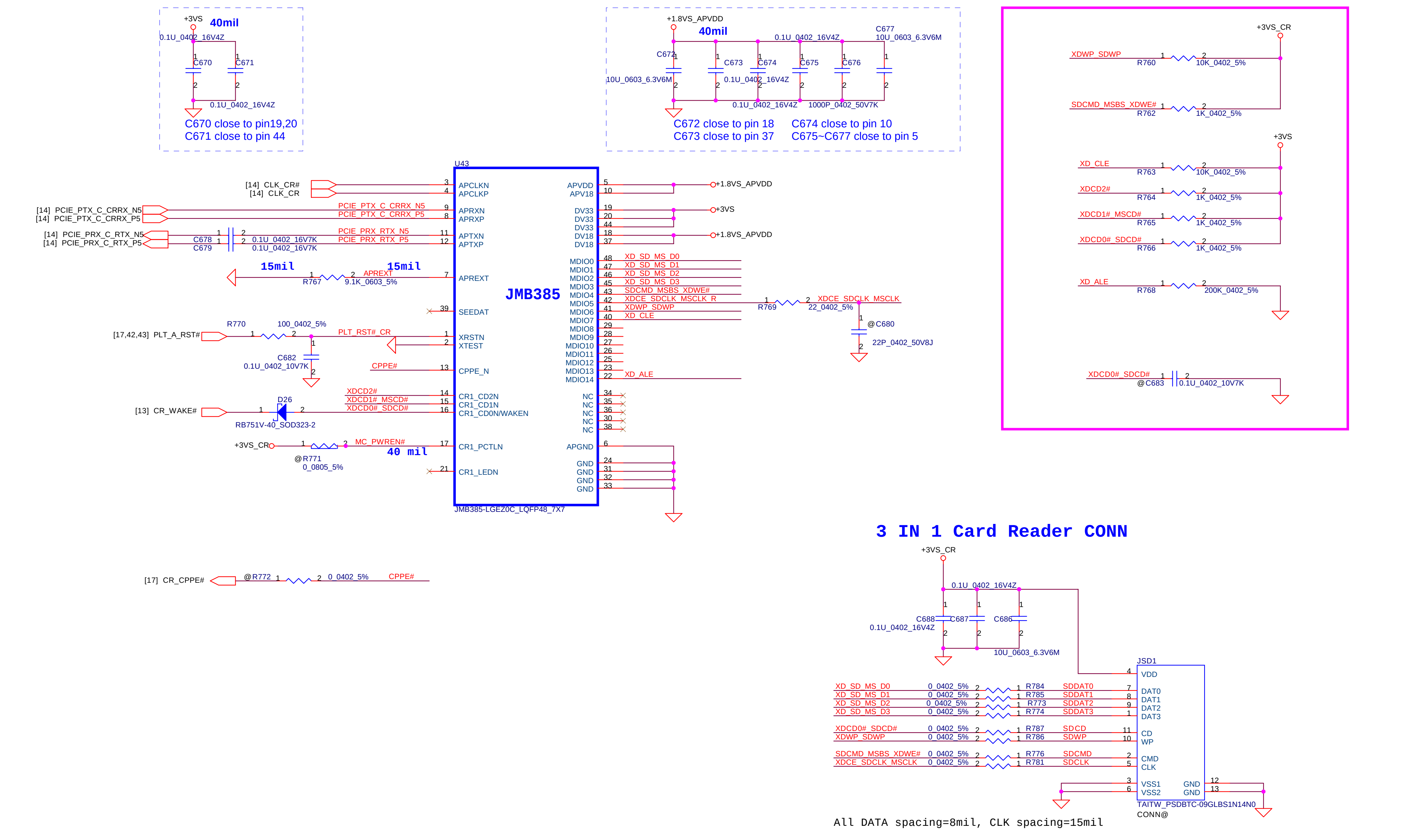
	RTL8105E-VC RTL8111E-VB PWM Mode	RTL8105E-VC LDO Mode
R751	0 ohm (Pull High)	NC
R753	NC	0 ohm (Pull Down)

Security Classification	Compal Secret Data		
Issued Date	2010/10/1	Deciphered Date	2011/11/01

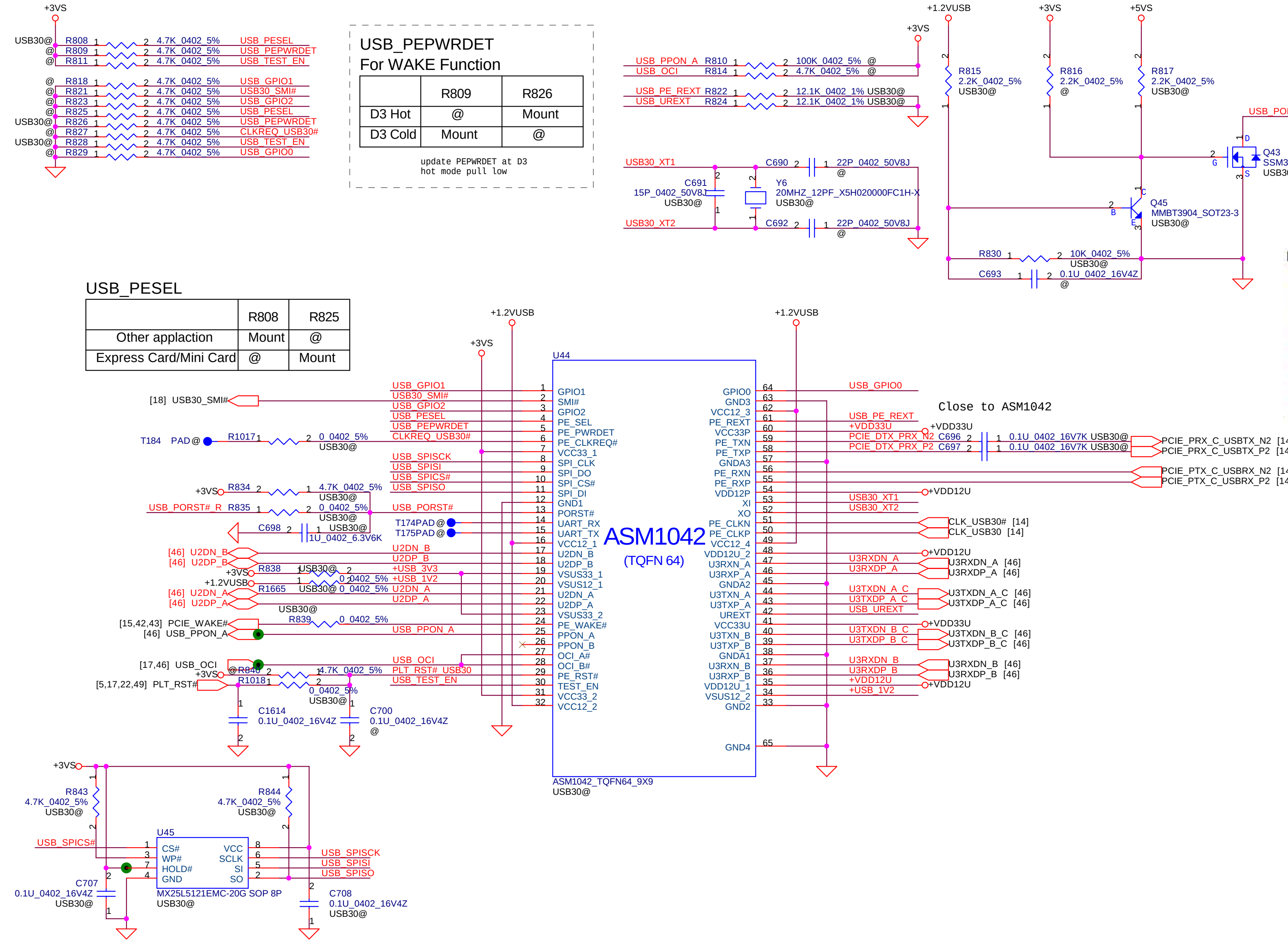
Compal Electronics, Inc.

Title: PCIe-LAN-RTL8111E

Size: Custom | Document Number | Rev 0.1



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/10/1	Deciphered Date	2011/11/01	Title: JMB385 Media Card Controller
				Size: Custom; Document Number: PCA70 LA-7521P M/B; Rev 0.1
				Date: Tuesday, April 12, 2011; Sheet 44 of 64



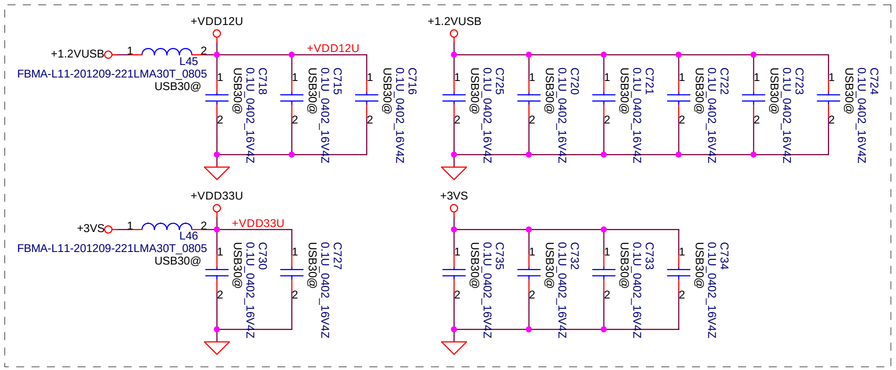
USB_PEPWRDET
For WAKE Function

	R809	R826
D3 Hot	@	Mount
D3 Cold	Mount	@

update PEPWRDET at D3
hot mode pull low

USB_PESEL

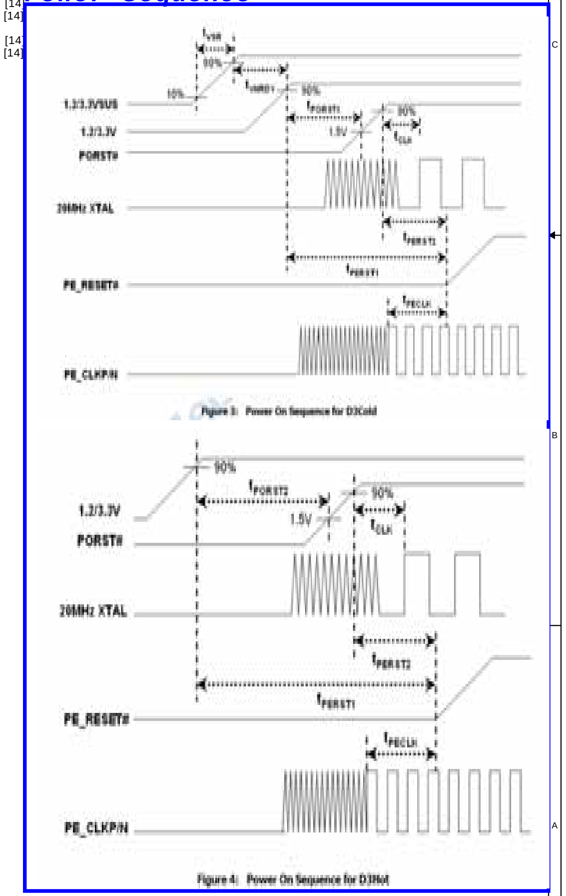
	R808	R825
Other applaction	Mount	@
Express Card/Mini Card	@	Mount



Power On Sequence Timing Specification

Symbols	Parameter	Min	Max	Unit
t_{VSB}	Rising time for Suspend Power Ready		10	ms
t_{NMRDY}	Timing for Normal Power Ready	50		ms
t_{PORST1}	Timing for 1.2V/3.3V Normal Power Ready to Power On Reset (D3Cold)	3	80	ms
t_{PORST2}	Timing for 1.2V/3.3V Normal Power Ready to Power On Reset (D3Hot)	50	80	ms
t_{PECLK}	Timing for PE_CLK Ready to PE_RST#	100		μs
t_{CLK}	Timing for 20MHz Crystal Clock Ready to Power On Reset		20	ms
t_{PERST1}	Timing for PE_RST# delay after Normal Power Ready	100		ms
t_{PERST2}	Timing for PE_RST# delay after PORST# comes up	20		ms

Power Sequence

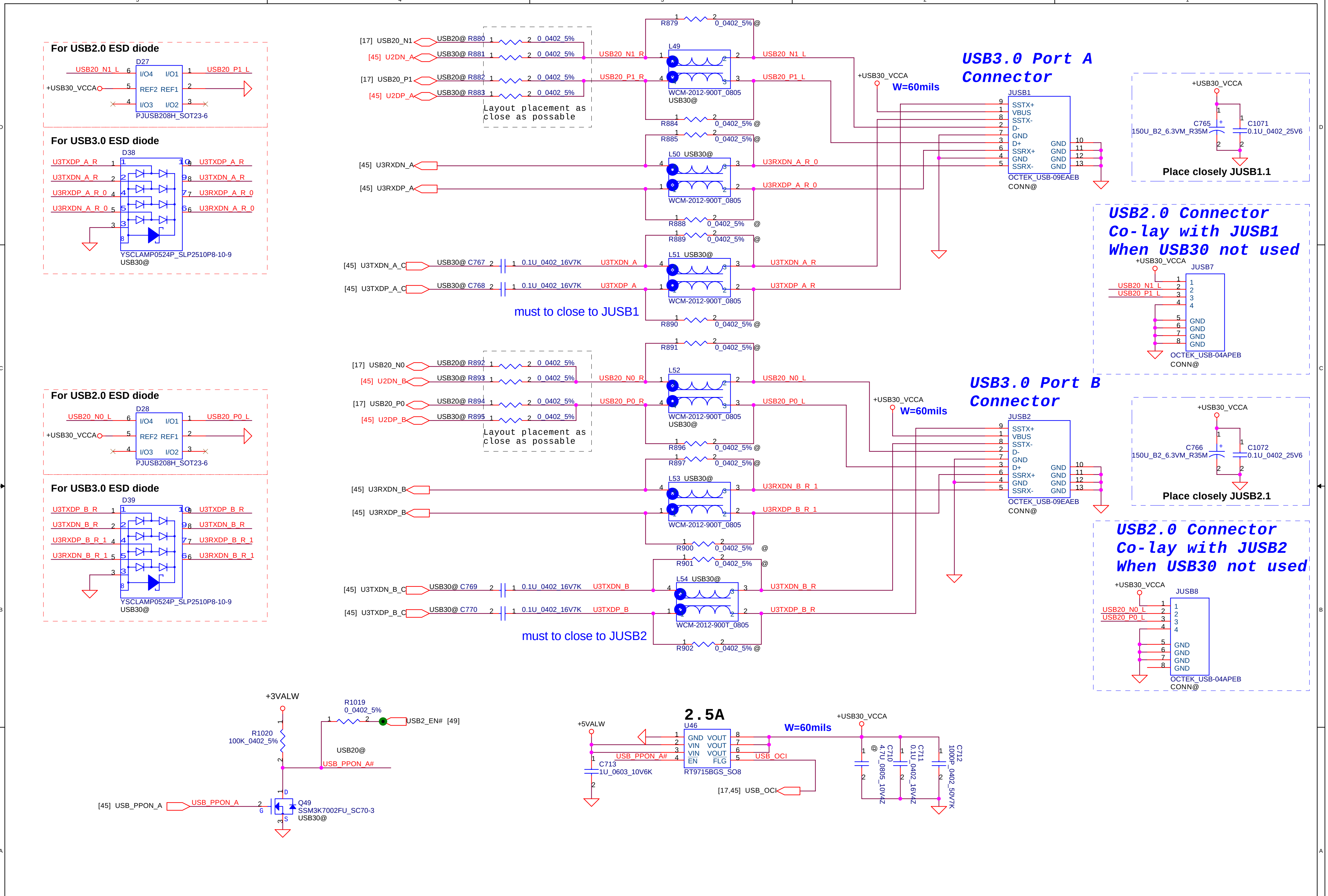


Security Classification	Compal Secret Data		
Issued Date	2010/10/1	Deciphered Date	2011/11/01

Compal Electronics, Inc.

Title: USB3.0

Size: Custom | Document Number: PCA70 LA-7521P M/B | Rev: 0.2

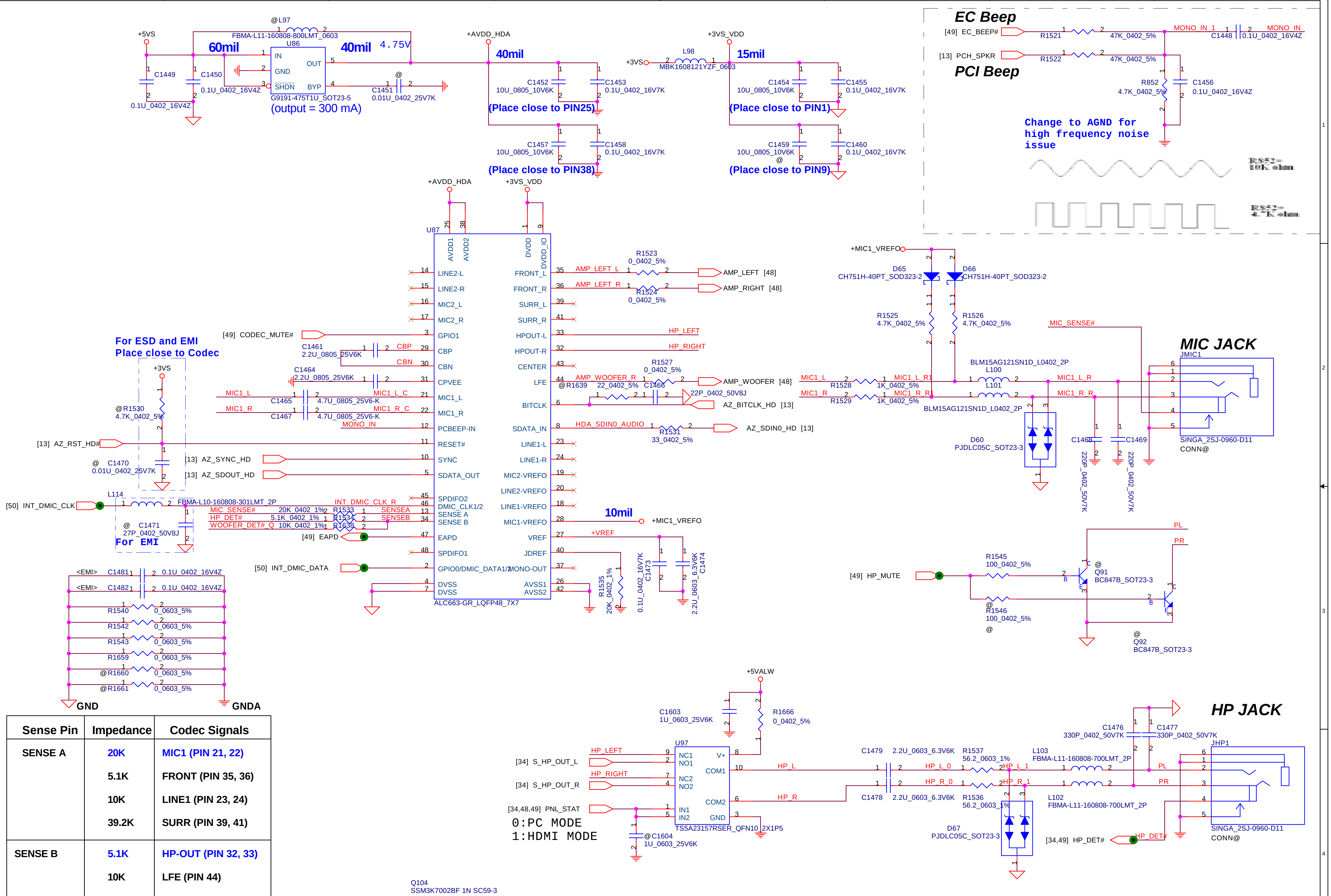


Security Classification	Compal Secret Data		
Issued Date	2010/10/1	Deciphered Date	2011/11/01

Title: USB3.0 CONN

Size | Document Number: PCA70 LA-7521P M/B | Rev 0.1

Date: Tuesday, April 12, 2011 |

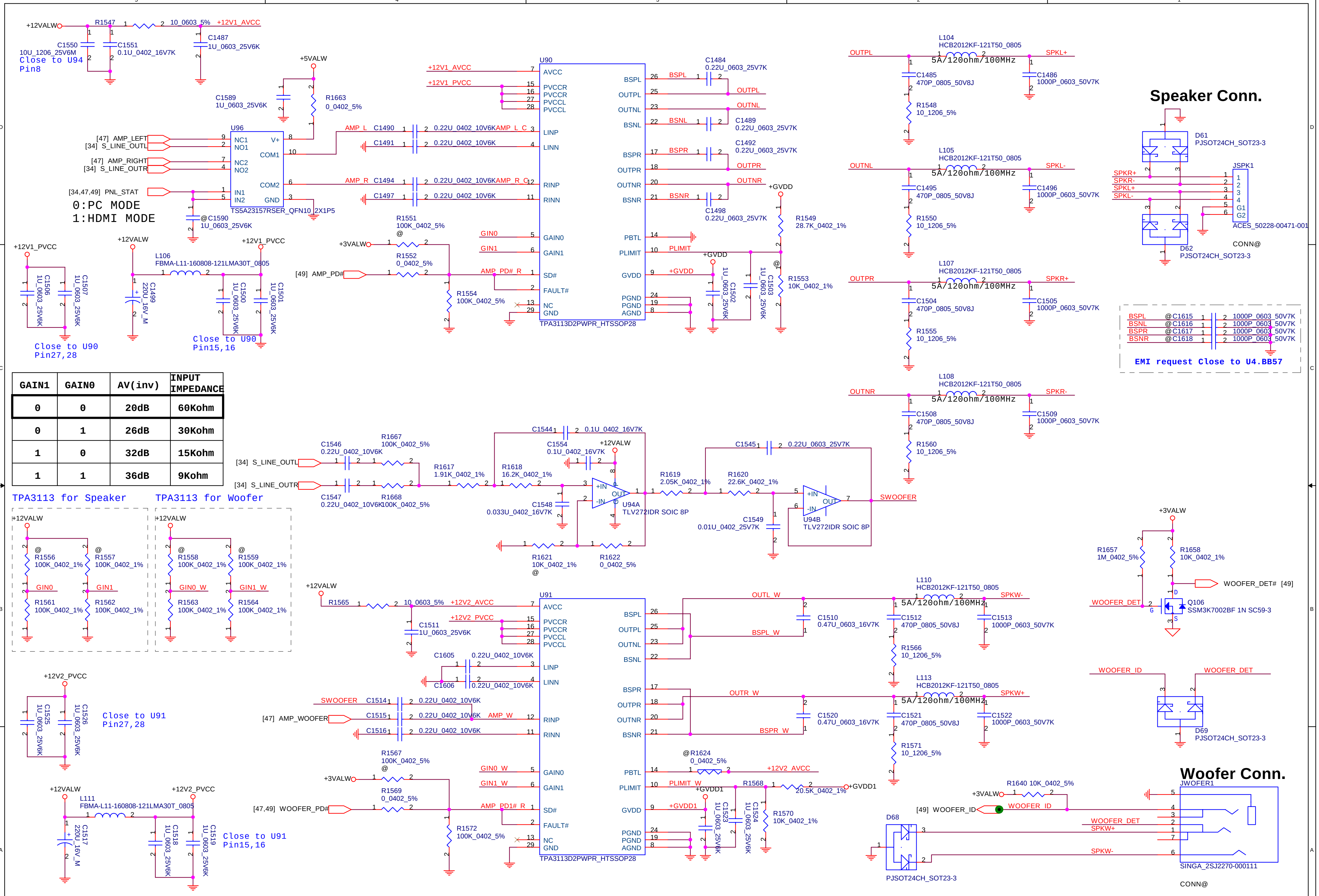


Sense Pin	Impedance	Codec Signals
SENSE A	20K	MIC1 (PIN 21, 22)
	5.1K	FRONT (PIN 35, 36)
	10K	LINE1 (PIN 23, 24)
	39.2K	SURR (PIN 39, 41)
SENSE B	5.1K	HP-OUT (PIN 32, 33)
	10K	LFE (PIN 44)
	10K//5.1K	LFE+HP-OUT
	20K	MIC2 (PIN 16, 17)
	39.2K	LINE2 (PIN 14, 15)

Security Classification	Compal Secret Data		
Issued Date	2010/10/1	Deciphered Date	2011/11/01

Title
HDA-ALC272/HP/MIC

Size | Document Number | Rev
PCA70 LA-7521P M/B | 0.1



GAIN1	GAIN0	AV(inv)	INPUT IMPEDANCE
0	0	20dB	60Kohm
0	1	26dB	30Kohm
1	0	32dB	15Kohm
1	1	36dB	9Kohm

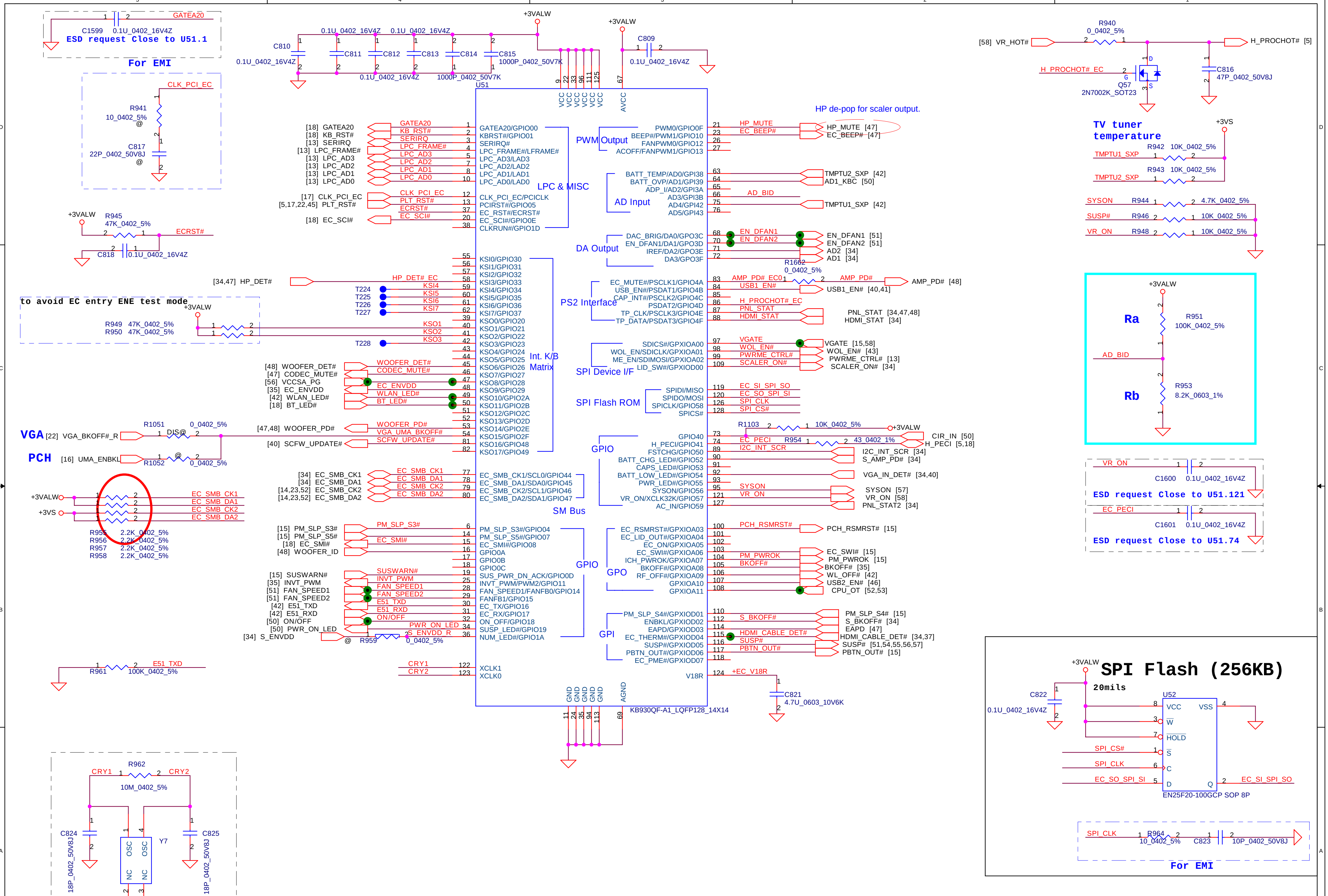
Security Classification	Compal Secret Data	
Issued Date	2010/04/14	Deciphered Date 2011/04/14

Compal Electronics, Inc.

Title: **AMP & Audio Jack**

Size: Custom | Document Number: PCA70 LA-7521P M/B | Rev 1.0

Date: Tuesday, April 12, 2011 | Sheet 48 of 64



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/10/1	Deciphered Date	2011/11/01	Title: LPC-EC-KB930

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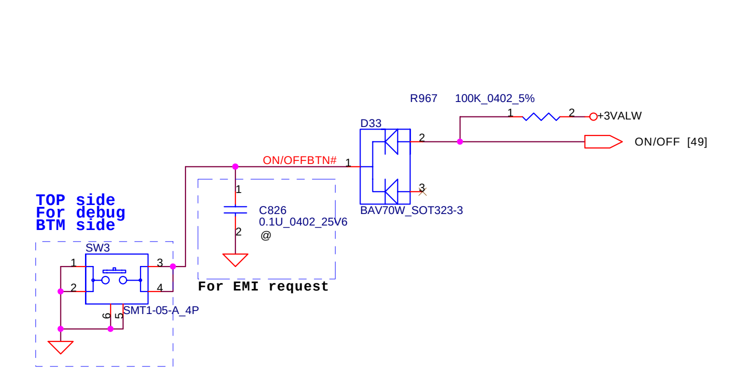
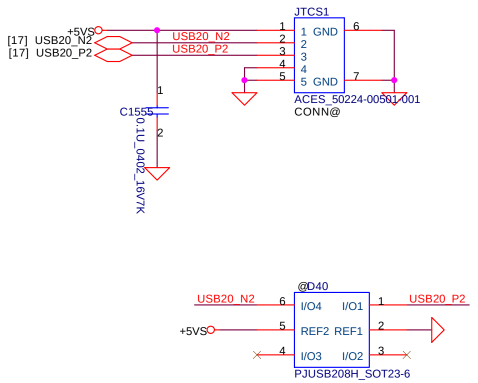
Size | Document Number: PCA70 LA-7521P M/B | Rev 0.1

Date: Tuesday, April 12, 2011 | Sheet 49 of 64

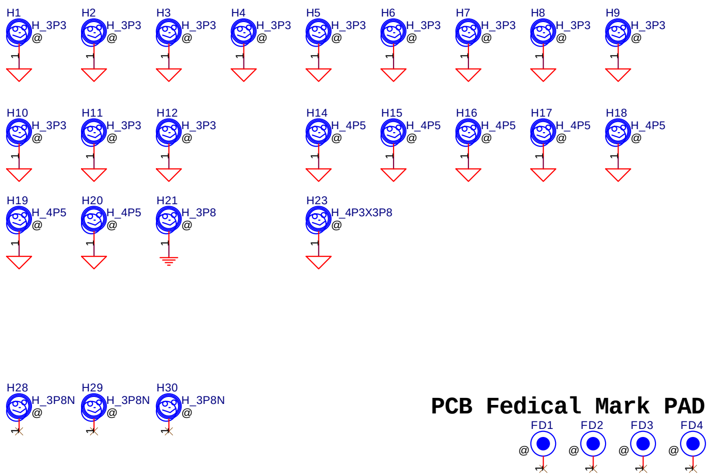
Power Button



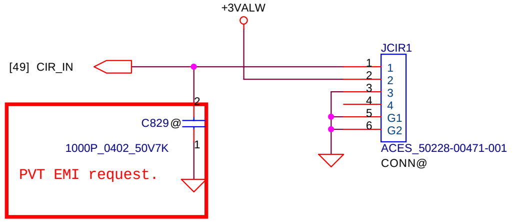
Touchscreen



Screw Hole

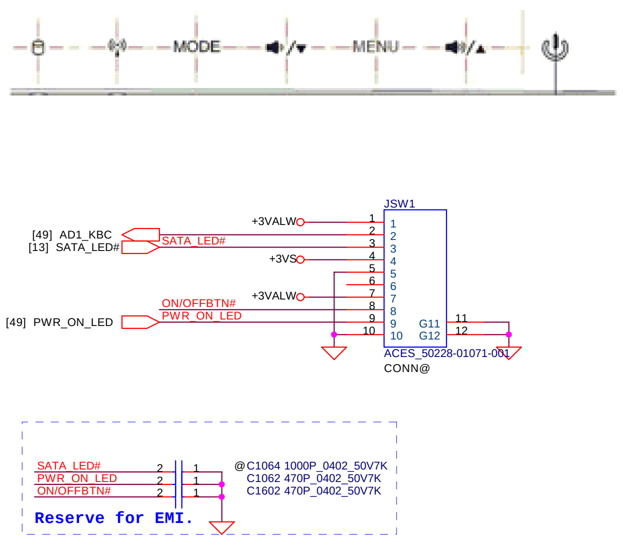


CIR

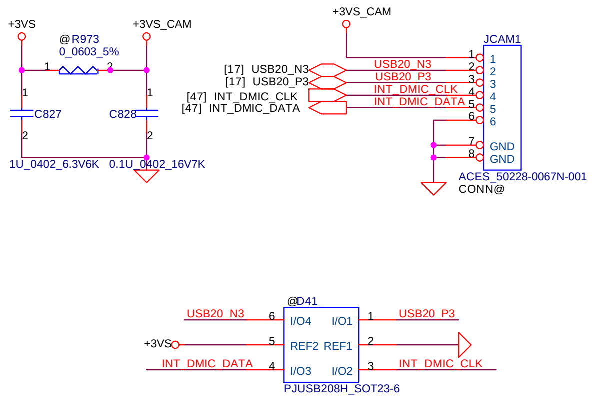


ISPD

CAP Button/B Connector



CAM



Security Classification	Compal Secret Data			Title: PWR/Cap./TP/LED/LP/LS/Screw
Issued Date	2010/10/1	Deciphered Date	2011/11/01	Size / Document Number: PCA70 LA-7521P M/B / Rev 0.1
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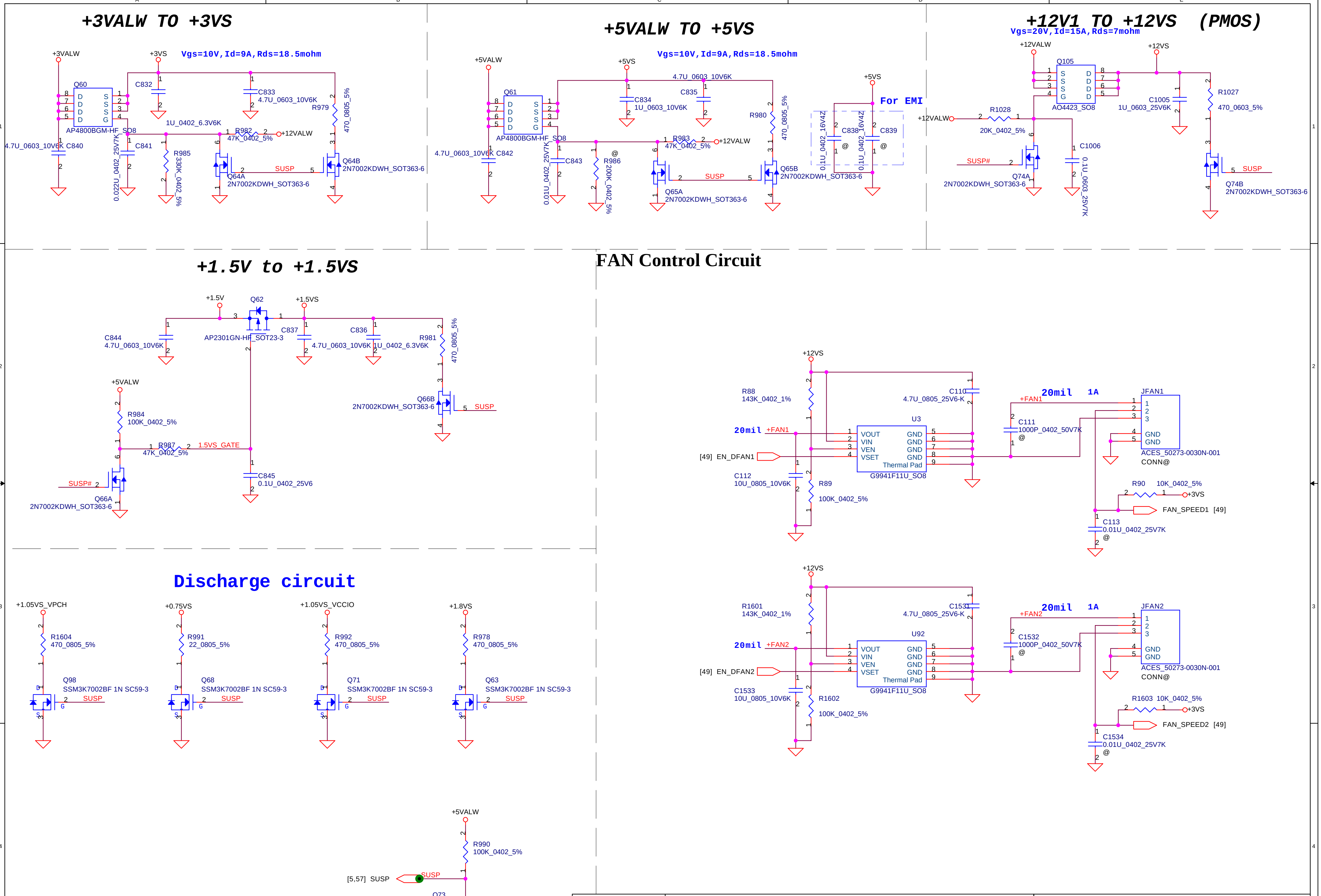


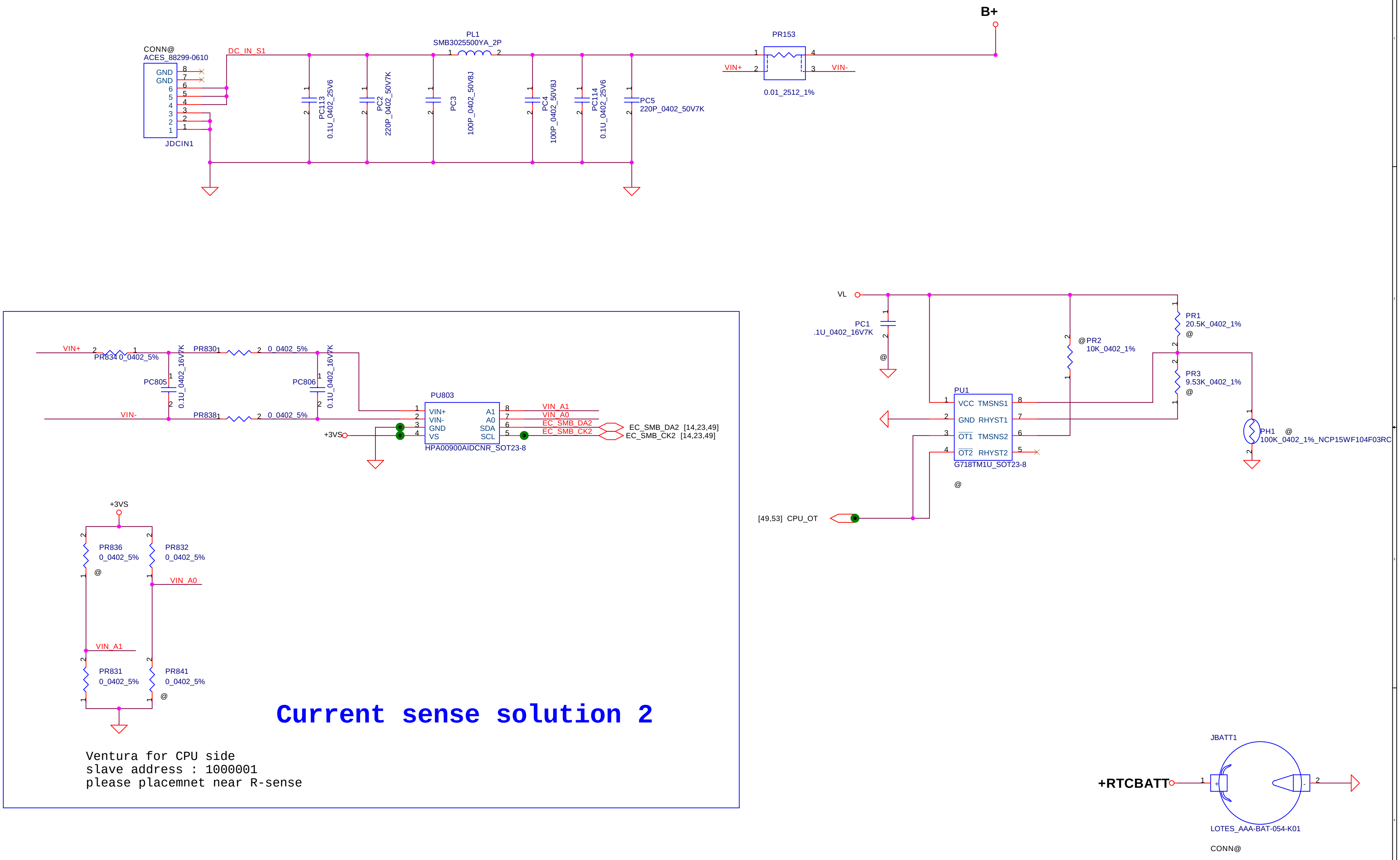
Security Classification	Compal Secret Data		
Issued Date	2010/10/1	Deciphered Date	2011/11/01

Compal Electronics, Inc.

Title: DC-DC INTERFACE

Size | Document Number: PCA70 LA-7521P M/B | Rev 0.1

Date: Tuesday, April 12, 2011



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2010/10/1	Deciphered Date	2011/11/01	Title: P51_PWR_DC-IN	
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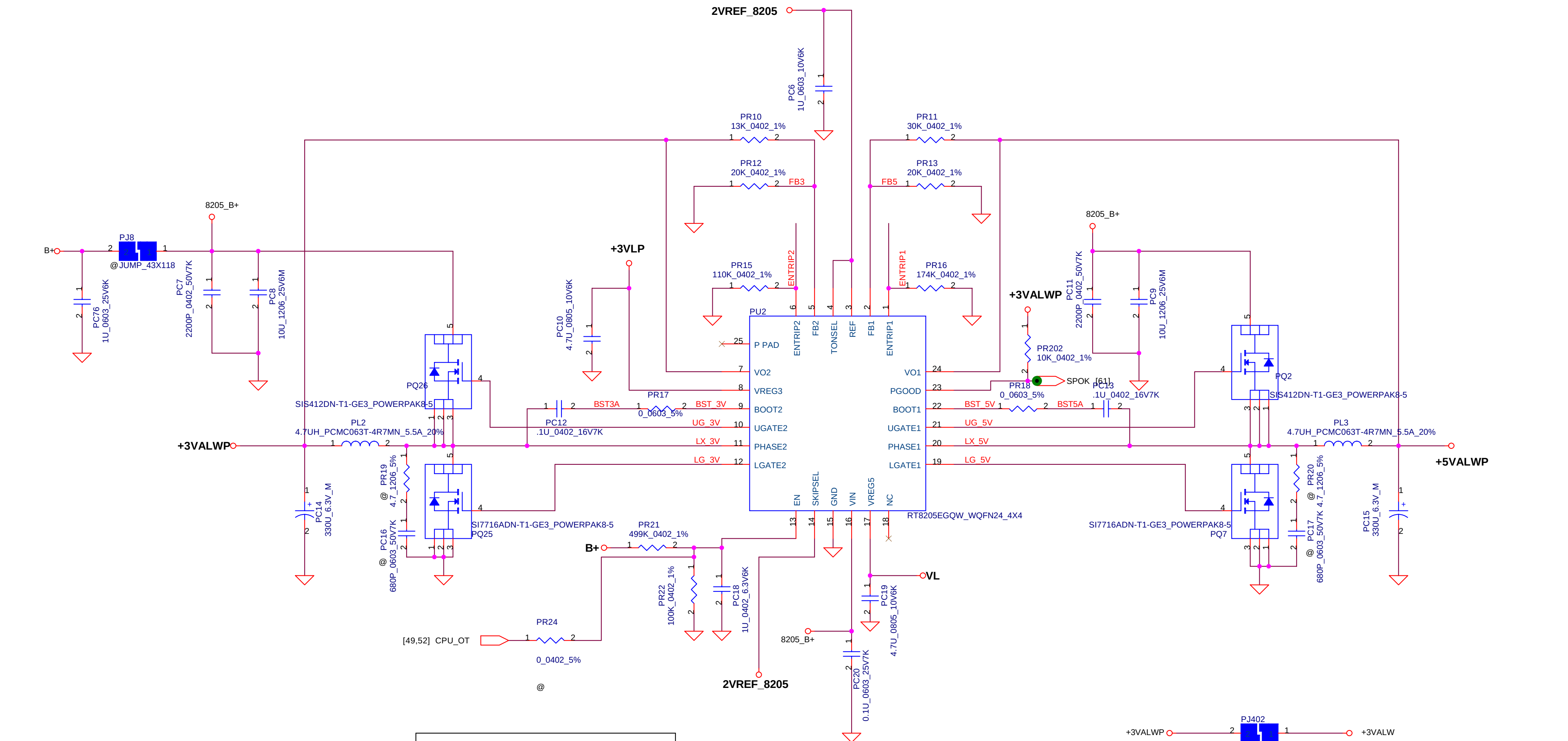
				Date: Tuesday, April 12, 2011	Sheet 52 of 64

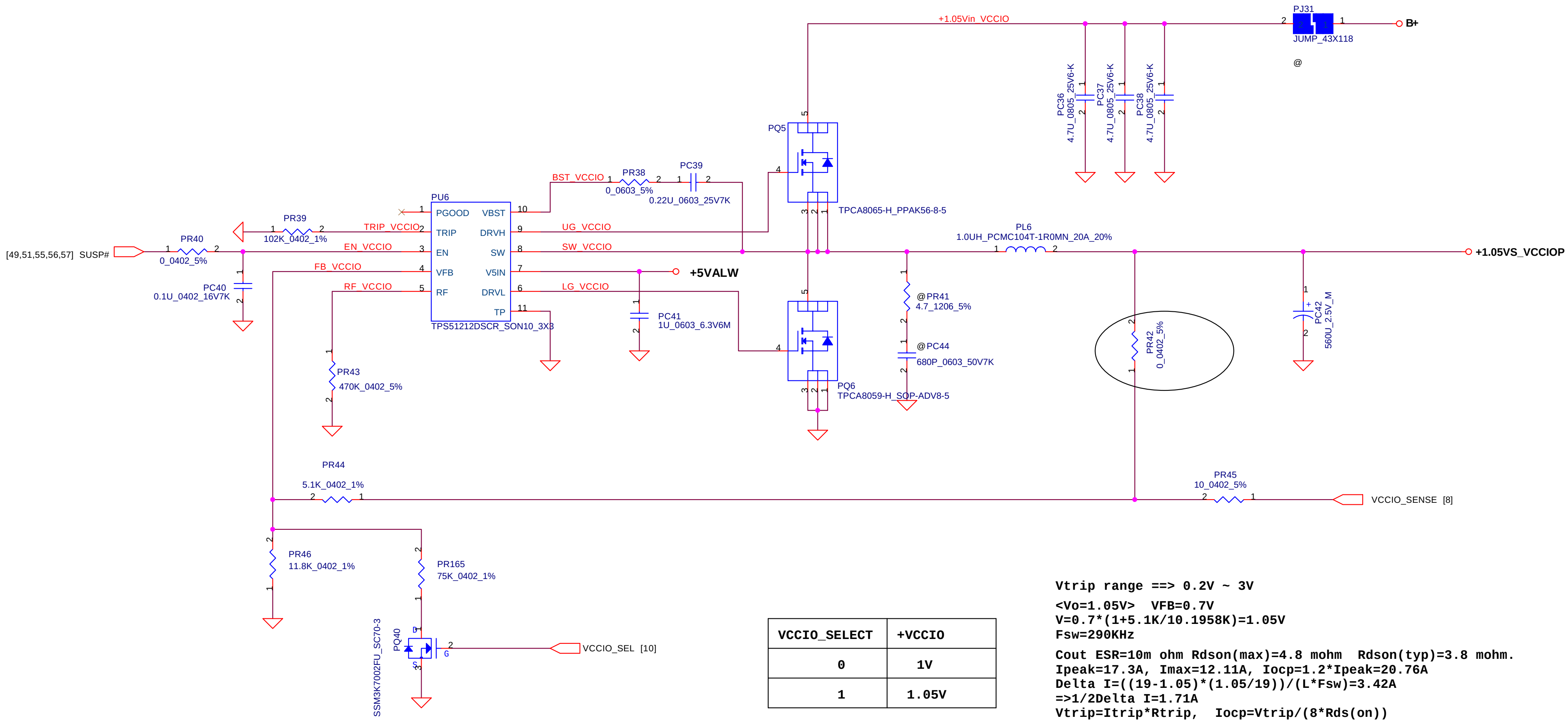



```
TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)
            (2)SMPS2=375KHZ(+3VALWP)
```

+3.3VALWP
Ipeak=5.71A ; 1.2Ipeak=6.852A; Imax=3.997A
f=375KHz, L=4.7UH
Rdson=15~18m ohm
1/2Delta I = 1/2 *(19-3.3)*(3.3/19)/(375KHz*4.7UH)=0.773A
Vlimit=10*10^-6*110Kohm/10=0.11V
Ilimit=0.11/(18m*1.2)~0.11/(15m)=6.34A~9.13A
Iocp=7.113A~10.073A (7.113A>6.852A -> ok) -DVT-

+5VALWP
Ipeak=7.376A ; 1.2Ipeak=8.85A; Imax=5.16A
f=300KHz, L=4.7UH,Rentrip=174k ohm
Rdson=15~18m ohm
1/2Delta I = 1/2 *(19-5)*(5/19)/(300KHz*4.7UH)=1.306A
Vlimit=10*(10^-6)*174Kohm/10=0.174V
Ilimit=0.174/(18m*1.2)~0.174/(15m)=8.055~11.6A
Iocp=9.361~12.906A (9.361>8.85 -> OK)

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/10/1	Deciphered Date	2011/11/01	Title: P52-PWR-+3VALW/+5VALW
Size	Document Number: PCA70 LA-7521P M/B			Rev 0.1
Date: Tuesday, April 12, 2011		Sheet 53 of 64		



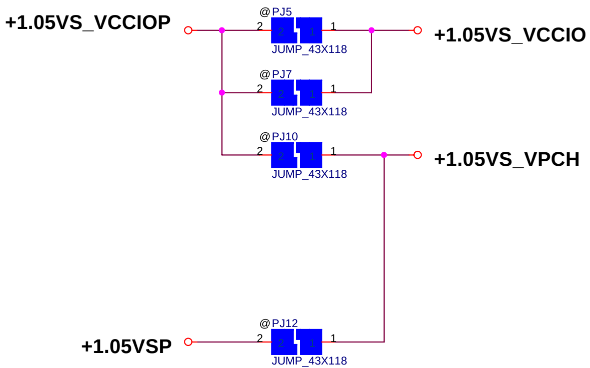
VCCIO_SELECT	+VCCIO
0	1V
1	1.05V

Vtrip range ==> 0.2V ~ 3V

<Vo=1.05V> VFB=0.7V
V=0.7*(1+5.1K/10.1958K)=1.05V
Fsw=290KHz

Cout ESR=10m ohm Rdson(max)=4.8 mohm Rdson(typ)=3.8 mohm.
Ipeak=17.3A, Imax=12.11A, Iocp=1.2*Ipeak=20.76A
Delta I=((19-1.05)*(1.05/19))/(L*Fsw)=3.42A
=>1/2Delta I=1.71A
Vtrip=Itrip*Rtrip, Iocp=Vtrip/(8*Rds(on))
Iocpmax=((102K*11uA)/(8*0.0038))+1.71A=38.617A
Iocpmin=((102K*9uA)/(8*0.0048))+1.71A=25.616A
Iocp=25.616A~38.617A

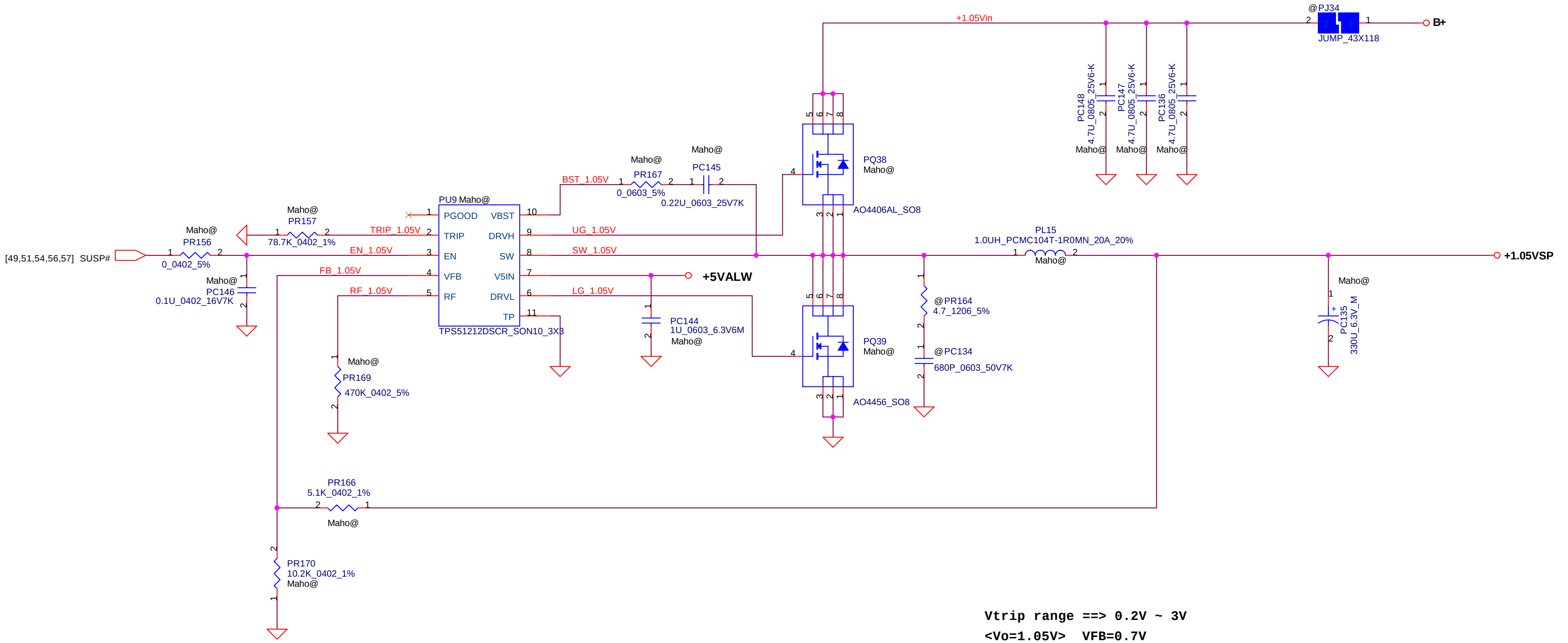
(17A,680mils ,Via NO.=34)



<Vo=1.0V> VFB=0.7V
V=0.7*(1+5.1K/11.8K)=1.0V
Fsw=290KHz

Cout ESR=10m ohm Rdson(max)=4.8 mohm Rdson(typ)=3.8 mohm.
Ipeak=17.3A, Imax=12.11A, Iocp=1.2*Ipeak=20.76A
Delta I=((19-1.0)*(1.0/19))/(L*Fsw)=3.266A
=>1/2Delta I=1.633A
Vtrip=Itrip*Rtrip, Iocp=Vtrip/(8*Rds(on))
Iocpmax=((102K*11uA)/(8*0.0038))+1.633A=38.54A
Iocpmin=((102K*9uA)/(8*0.0048))+1.633A=25.539A
Iocp=25.539A~38.54A

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2009/11/13	Deciphered Date	2009/04/28	Title: +1.05VSP
				Size / Document Number: PCA60/70 LA-7001P M/B / Rev 0.1
				Date: Tuesday, April 12, 2011 / Sheet 54 of 64



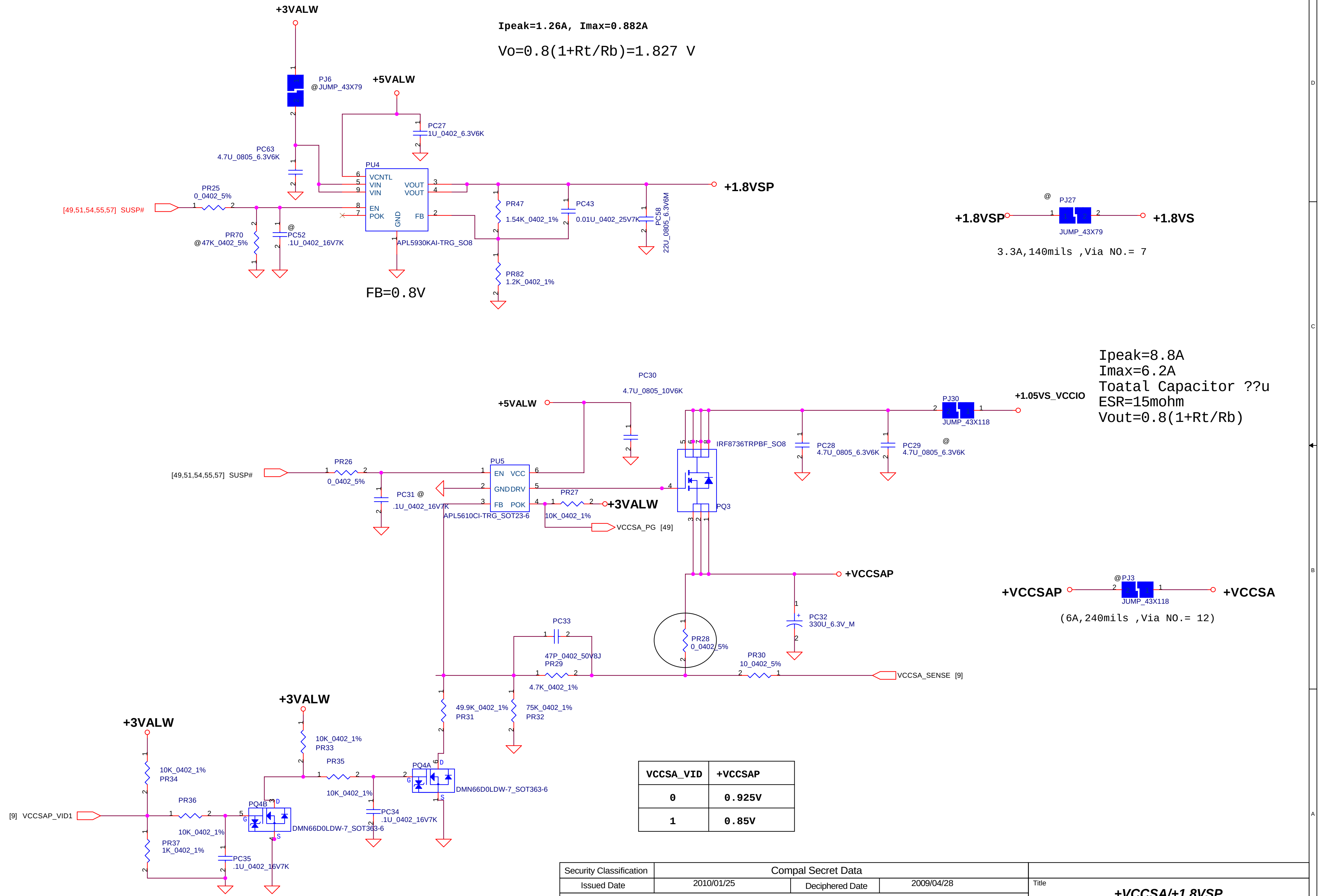

```
Vtrip range ==> 0.2V ~ 3V
<Vo=1.05V>  VFB=0.7V
V=0.7*(1+5.1K/10.2K)=1.05V
Fsw=290KHz
Cout ESR=10m ohm Rdson(max)=5.6 mohm  Rdson(typ)=4.5 mohm.
Ipeak=7.3A, Imax=5.11A, Iocp=1.2*Ipeak=8.76A
Delta I=((19-1.05)*(1.05/19))/(L*Fsw)=3.42A
=>1/2Delta I=1.71A
Vtrip=Itrip*Rtrip,  Iocp=Vtrip/(8*Rds(on))
Iocpmax=((78.7K*11uA)/(8*0.0045))+1.71A=25.75A
 Iocpmin=((78.7K*9uA)/(8*0.0056*1.3))+1.71A=13.871A
Iocp=13.871A~25.75A
```

Security Classification	Compal Secret Data		
Issued Date	2010/10/1	Deciphered Date	2011/11/01

Compal Electronics, Inc.

Title: *P54_PWR-+1.05VSP*

Size | Document Number: **PCA70 LA-7521P M/B** | Rev 0.1

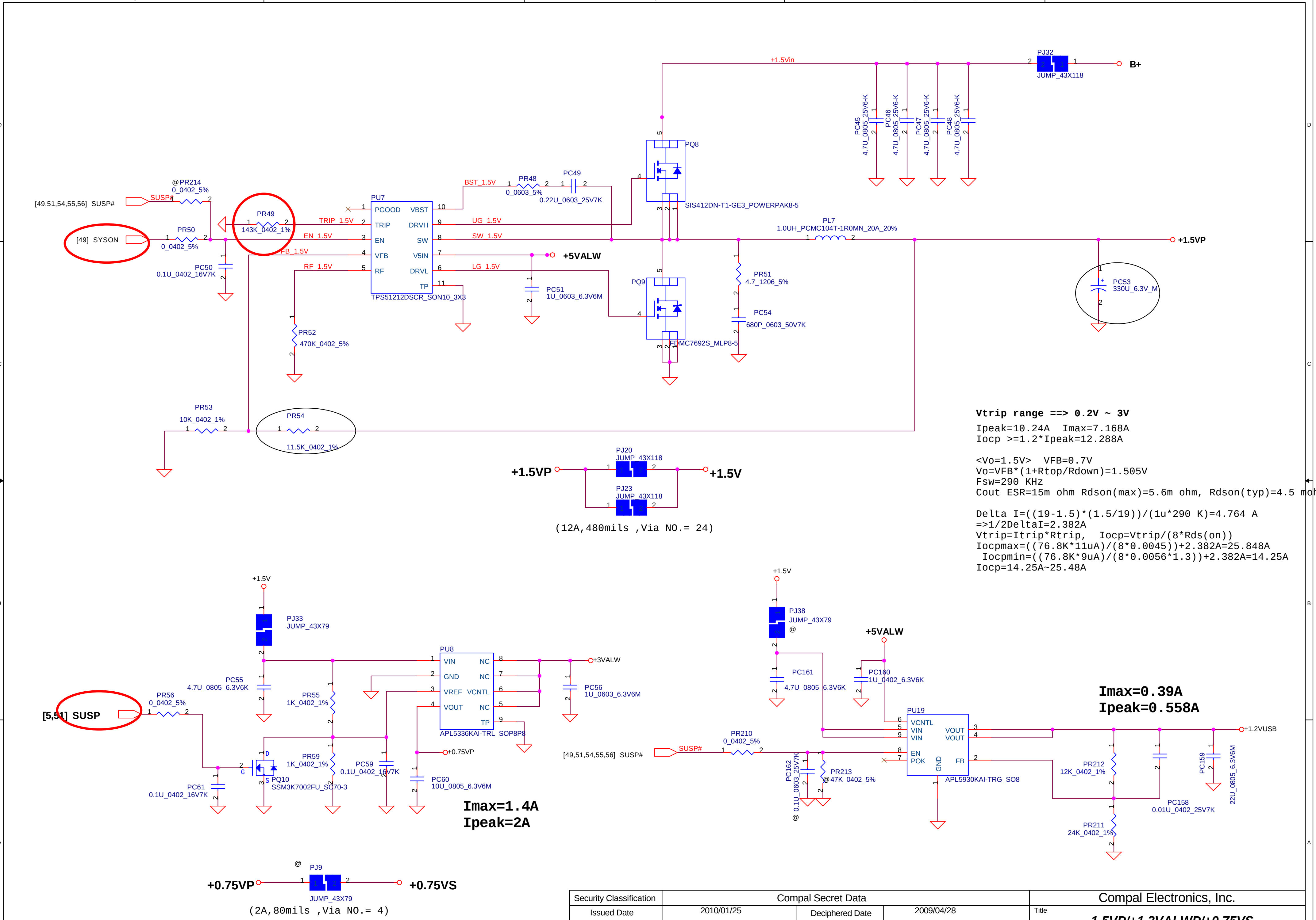


VCCSA_VID	+VCCSAP
0	0.925V
1	0.85V

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2009/04/28

Title: **+VCCSA/+1.8VSP**

Size: Custom | Document Number: **PCA60/70 LA-7001P M/B** | Rev 0.1



Vtrip range ==> 0.2V ~ 3V

Ipeak=10.24A Imax=7.168A
Iocp >=1.2*Ipeak=12.288A

<Vo=1.5V> VFB=0.7V
Vo=VFB*(1+Rtop/Rdown)=1.505V
Fsw=290 KHz
Cout ESR=15m ohm Rdson(max)=5.6m ohm, Rdson(typ)=4.5 mohm

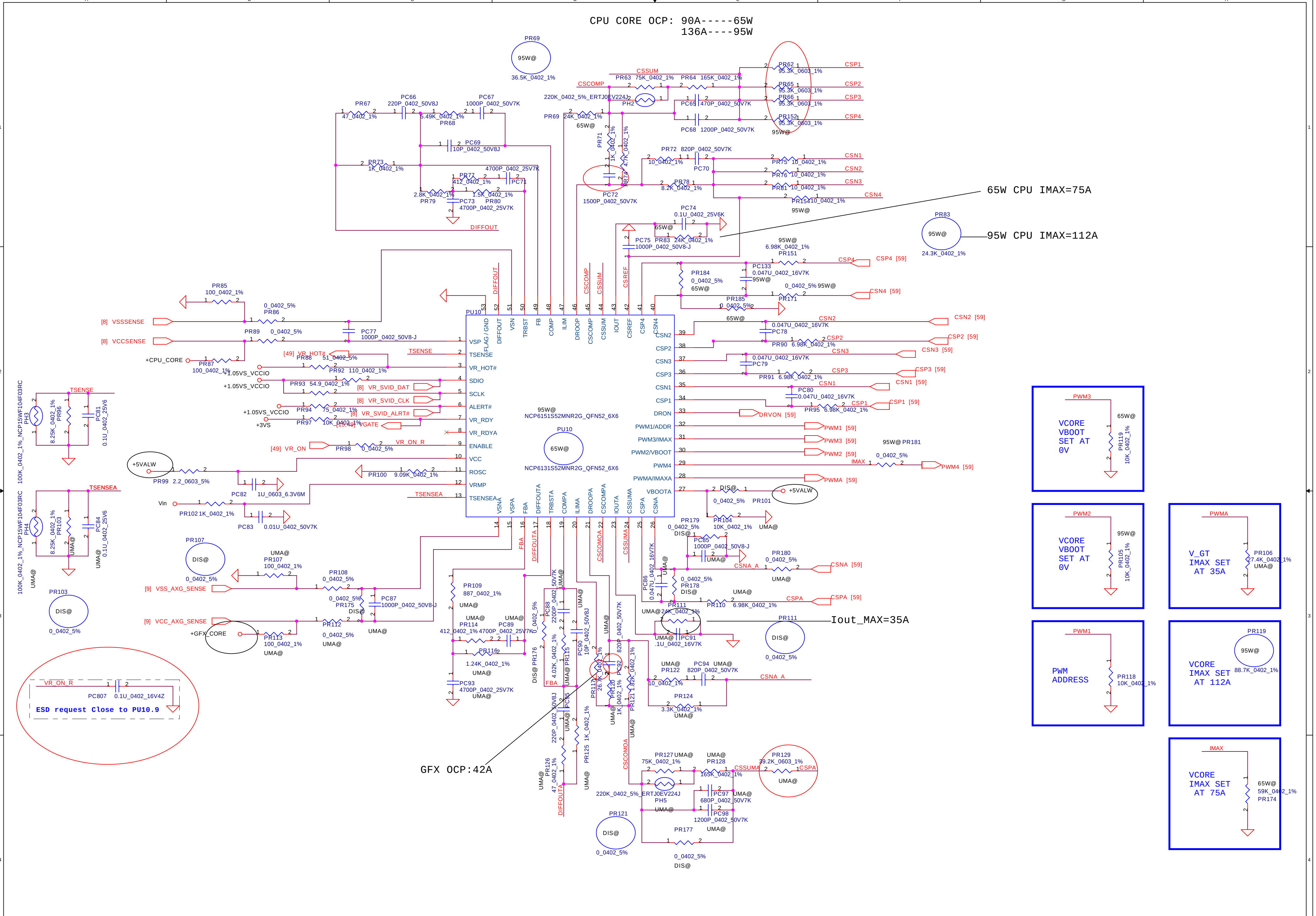
Delta I=((19-1.5)*(1.5/19))/(1u*290 K)=4.764 A
=>1/2DeltaI=2.382A
Vtrip=Itrip*Rtrip, Iocp=Vtrip/(8*Rds(on))
Iocpmax=((76.8K*11uA)/(8*0.0045))+2.382A=25.848A
Iocpmin=((76.8K*9uA)/(8*0.0056*1.3))+2.382A=14.25A
Iocp=14.25A~25.48A

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2009/04/28

Compal Electronics, Inc.

Title: **1.5VP/+1.2VALWP/+0.75VS**

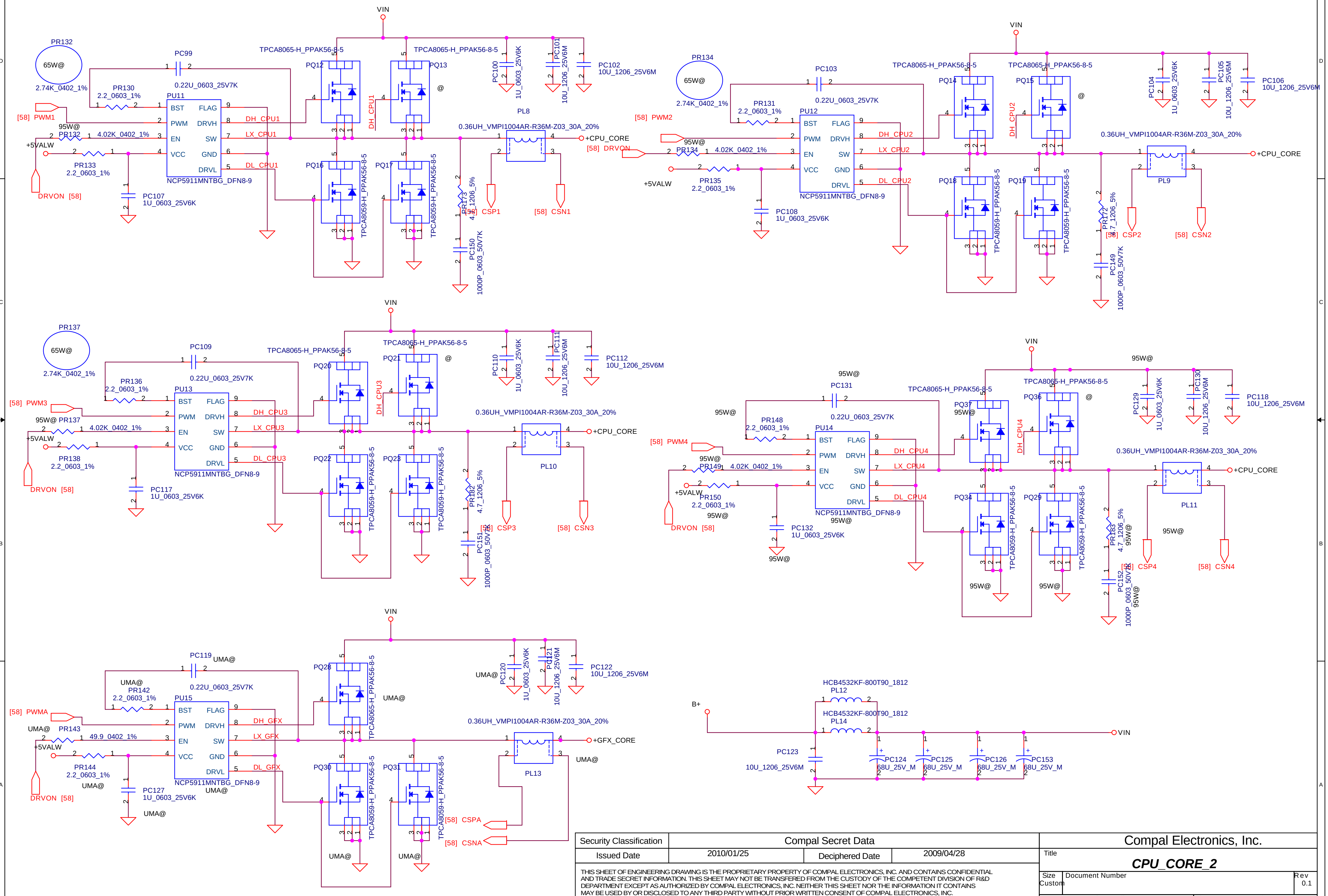
Size: Custom | Document Number: **PCA60/70 LA-7001P M/B** | Rev: 0.1



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/01/25	Deciphered Date	2009/04/28	Title: CPU_CORE_1

Size: C Document Number: PCA60/70 LA-7001P M/B Rev: 0.1

Date: Tuesday, April 12, 2011 Sheet 58 of 64



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2009/04/28

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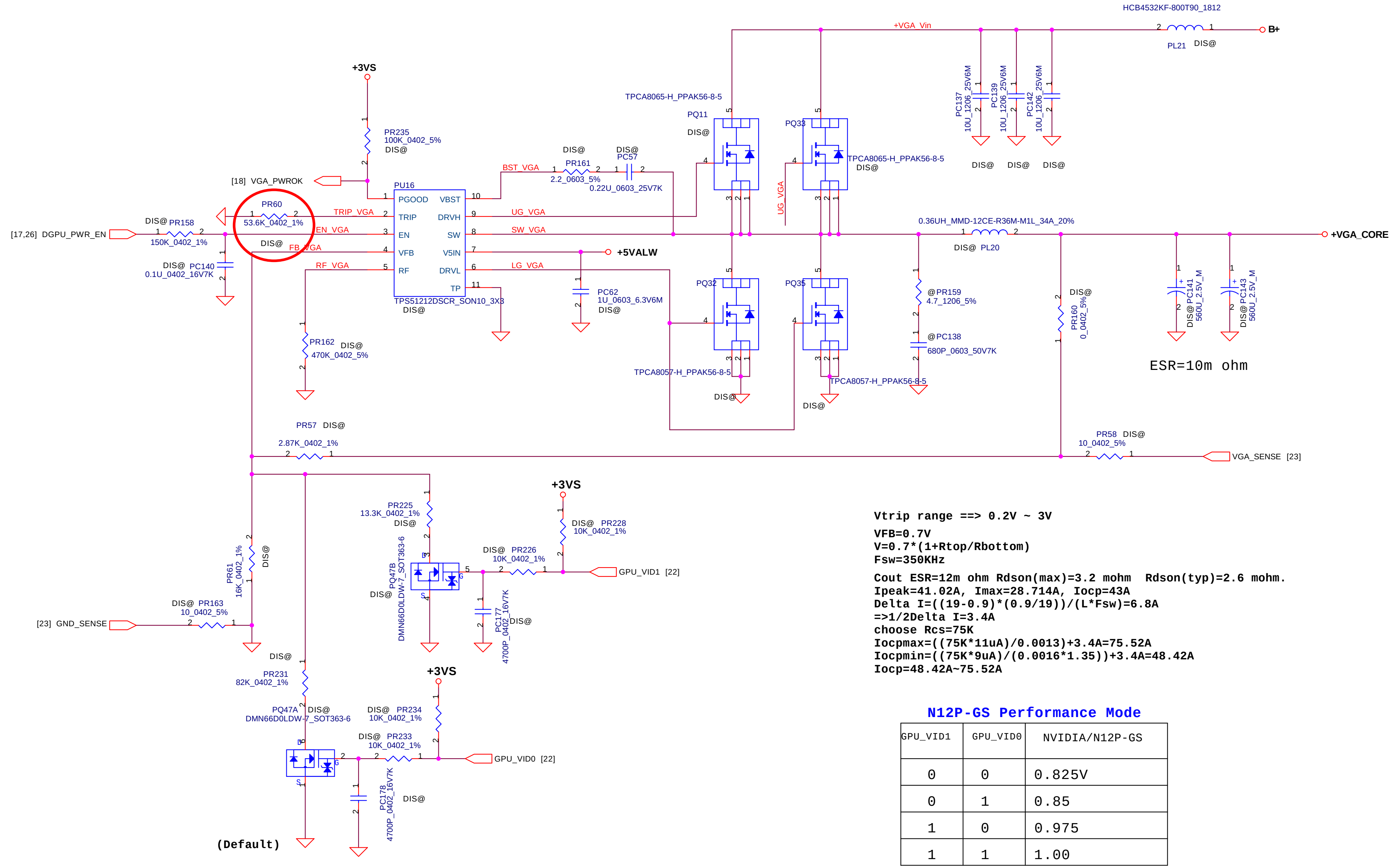
Compal Electronics, Inc.

Title: CPU_CORE_2

Size: Custom | Document Number | Rev 0.1

Date: Tuesday, April 12, 2011 | Sheet 59 of 64

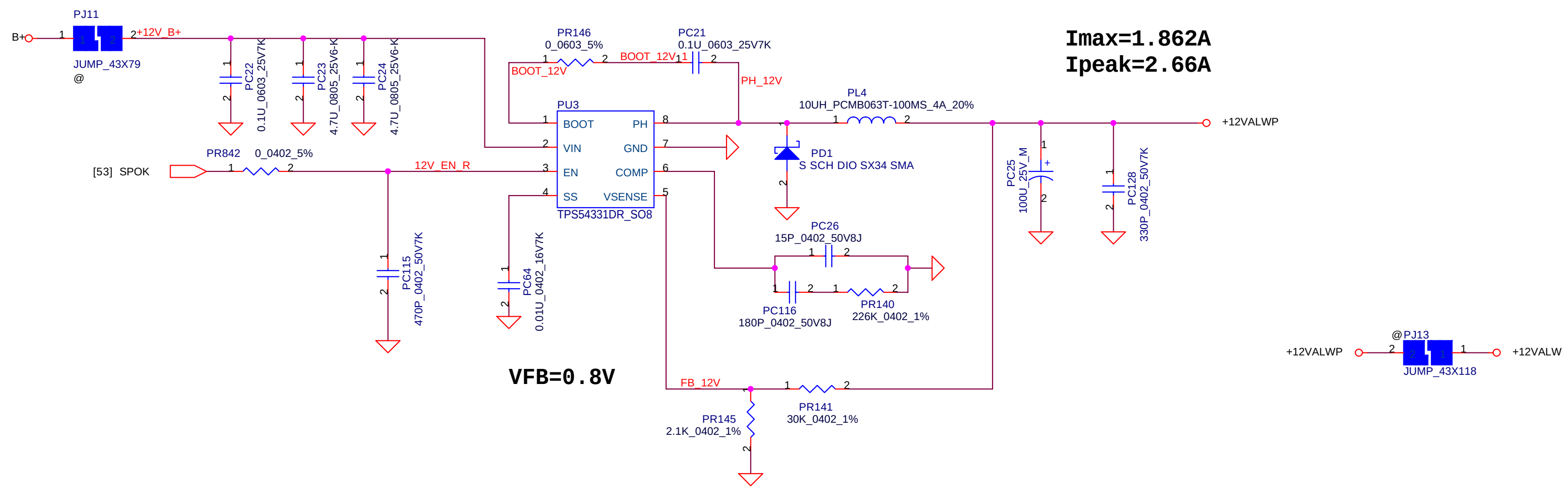



```
Vtrip range ==> 0.2V ~ 3V
VFB=0.7V
V=0.7*(1+Rtop/Rbottom)
Fsw=350KHz
Cout ESR=12m ohm Rdson(max)=3.2 mohm  Rdson(typ)=2.6 mohm.
Ipeak=41.02A, Imax=28.714A, Iocp=43A
Delta I=((19-0.9)*(0.9/19))/(L*Fsw)=6.8A
=>1/2Delta I=3.4A
choose Rcs=75K
Iocpmax=((75K*11uA)/0.0013)+3.4A=75.52A
Iocpmin=((75K*9uA)/(0.0016*1.35))+3.4A=48.42A
Iocp=48.42A~75.52A
```

N12P-GS Performance Mode

GPU_VID1	GPU_VID0	NVIDIA/N12P-GS
0	0	0.825V
0	1	0.85
1	0	0.975
1	1	1.00

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/01/25	Deciphered Date	2009/04/28	Title: VGA_CORE
				Size: Custom; Document Number: PCA60/70 LA-7001P M/B; Rev: 0.1
				Date: Tuesday, April 12, 2011; Sheet 60 of 64



Security Classification	Compal Secret Data		
Issued Date	2010/10/1	Deciphered Date	2011/11/01

Compal Electronics, Inc.

Title: **P60_PWR-+12V**

Size | Document Number: **PCA70 LA-7521P M/B** | Rev 0.1

Date: Tuesday, April 12, 2011 | Sheet 61 of 64

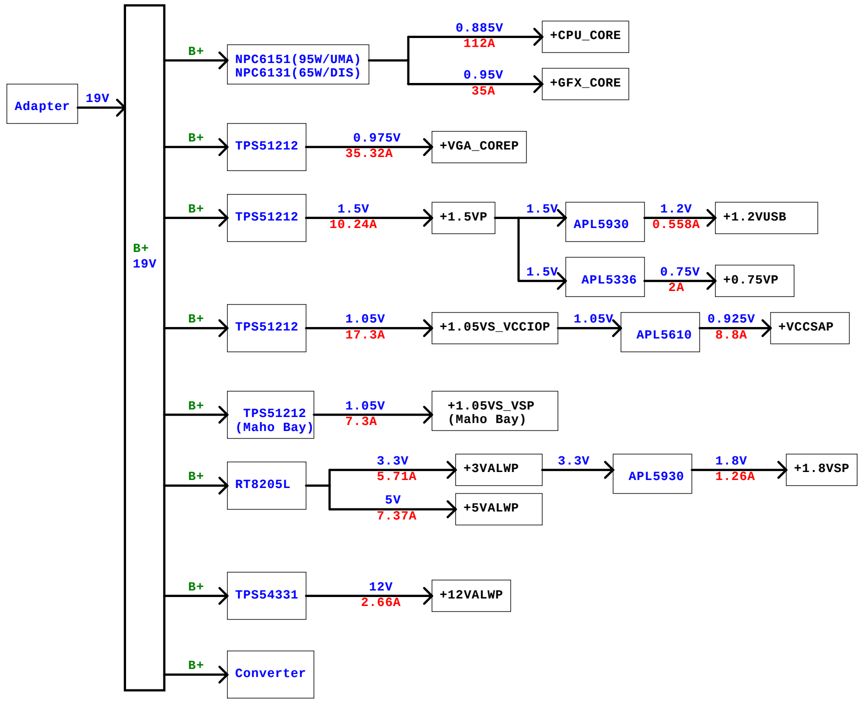
NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	2010/09/30	P48~49	Change PR39 to 118k ohm Change PR49 to 95.3k ohm	Modify OCP setting value
2	2010/10/01	P48	Remove reserved 1.05VP power rail	Because VCCIO will not be changeable voltage on Sandy Bridge platform. We don't need another 1.05V for PCH
3	2010/10/28	P50	PC124,PC125 change to 220u_25V Remove PC126	Modify for input cap
4	2010/10/28	P49	Remove PR70, PR82, PR84, PR171, PR172, PR173, PR174, PC76	Remove forth phase related components
5	2010/10/28	P49	PR62, PR65, PR66 change to 90.9K_0603_1% PC72 change to 1500P_0402_50V	Change for correct droop setting
6	2010/10/28	P49	PR129 change to 39.2K_0603_1% PR117 change to 25.5k_0402_1% PC92 change to 220P_0402_50V	Change for correct GT droop setting
7	2011/01/27	P58	update Net name "IMAX "	update after vender review layout
8	2011/01/27	P61	change PC25 part number to SF000004S00	material shoretage
9	2011/01/27	P59	change PC124/125/126/153 part number from SF000004L00 to SF000004M00	material shoretage
10	2011/02/09	P52	add "@" at BOM structure of PR836 and PR841	change for EC
11	2011/02/16	P53	change PU2 part number to SA00004NY00	change for part EOL
12	2011/03/07	P60	change PR60 from 75Kohm to 53.6Kohm	change for OCP setting point
	2011/03/07	P57	change PR49 from 76.8Kohm to 143Kohm	change for OCP setting point
13	2011/03/25	P60	change BOM structure PQ11 from @ to DIS@	for Thermal team concern
14	2011/03/30	P60	Remove VGA_core Jump for impedence concern	
15	2011/03/30	P52	change PR153 from 15m ohm to 10m ohm for Inrush concern	
16	2011/03/30	P59	change PC124/125/126/153 part number from SF000004M00 to SF000004T00	
17	2011/03/30		change PC101/102/105/106/111/112/118/121/122/123/130/137/139/142 part number from SE142106K80 to SE142106M80	
18	2011/04/06	P52	Remove JDCIN1 pin.7 and pin.8 from GND	Layout modification
19	2011/04/08	P58	add PC807 at PU10.9 for ESD request change PR68=5.49Kohm, PC67=1nF, PR62=PR65=PR66=PR152=95.3Kohm, PC65=470pF, PC69=10pF, PC66=220pF, PR80=1.5kohm, PR79=2.8kohm, PR129=39.2Kohm, PC88=2.2nF, PC97=680pF, PC90=10pF, PC95=220pF, PR116=1.24kohm, PR109=887ohm, PC92=820pF	
20	2011/04/08	P60	change PC141/PC143 part number to SF000002P00	

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/10/1	Deciphered Date	2011/11/01	Title: Power PIR
				Size / Document Number: PCA70 LA-7521P M/B / Rev 0.1
				Date: Tuesday, April 12, 2011 / Sheet 62 of 64

HW PIR (Product Improve Record)

NWQAA LA-6062P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2
GERBER-OUT DATE: 2009/12/30
NO DATE PAGE MODIFICATION LIST PURPOSE

Security Classification	Compal Secret Data		
Issued Date	2010/10/1	Deciphered Date	2011/11/01



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/10/28	Deciphered Date	2011/11/01	Title: ***Power Rail***

Size | Document Number | Rev 0.1

Date: Tuesday, April 12, 2011 |