Compal Confidential
Model Name : SJV53-DN
Compal Project Name : P5WS3
File Name : LA-6972P

Compal Confidential

SJV53_DN/ P5WS3 Schematics Document

AMD Danube

Champlain Processor with RS880M/SB820M/Whistler(Seymour) VGA

2010-10-21

LA6972P REV: 0.2

ZZZ
PCB
PCB 0I5 LA-6972P REV0 M/B
DA80000LP00
LA6972 MB Rev0

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/10/06	Deciphered Date	2010/03/12
Title: Cover Page			
Size: B	Document Number: P5WS3 LA-6972P		Rev: 0.2
Date: Thursday, October 21, 2010	Sheet 1 of 53		

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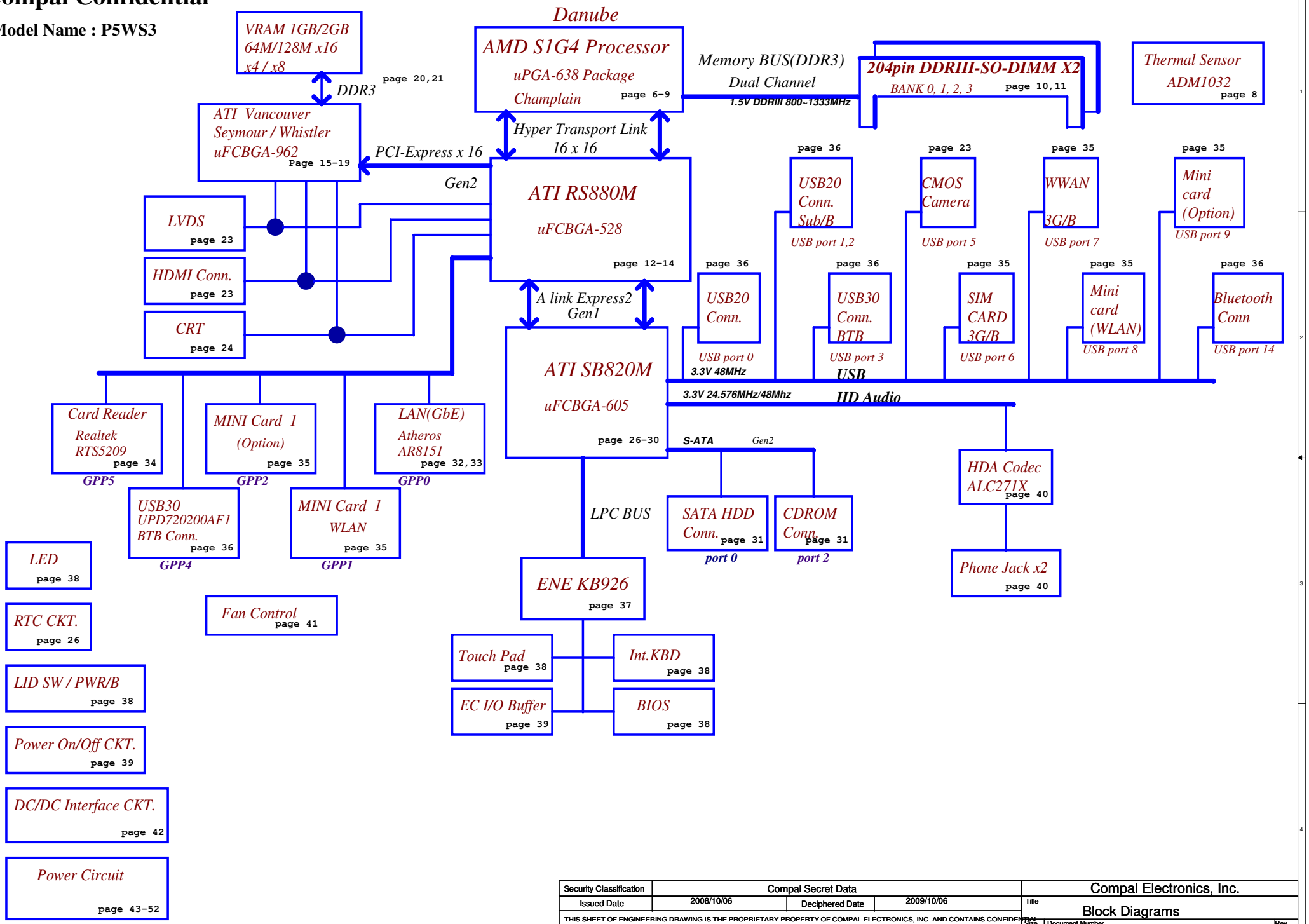
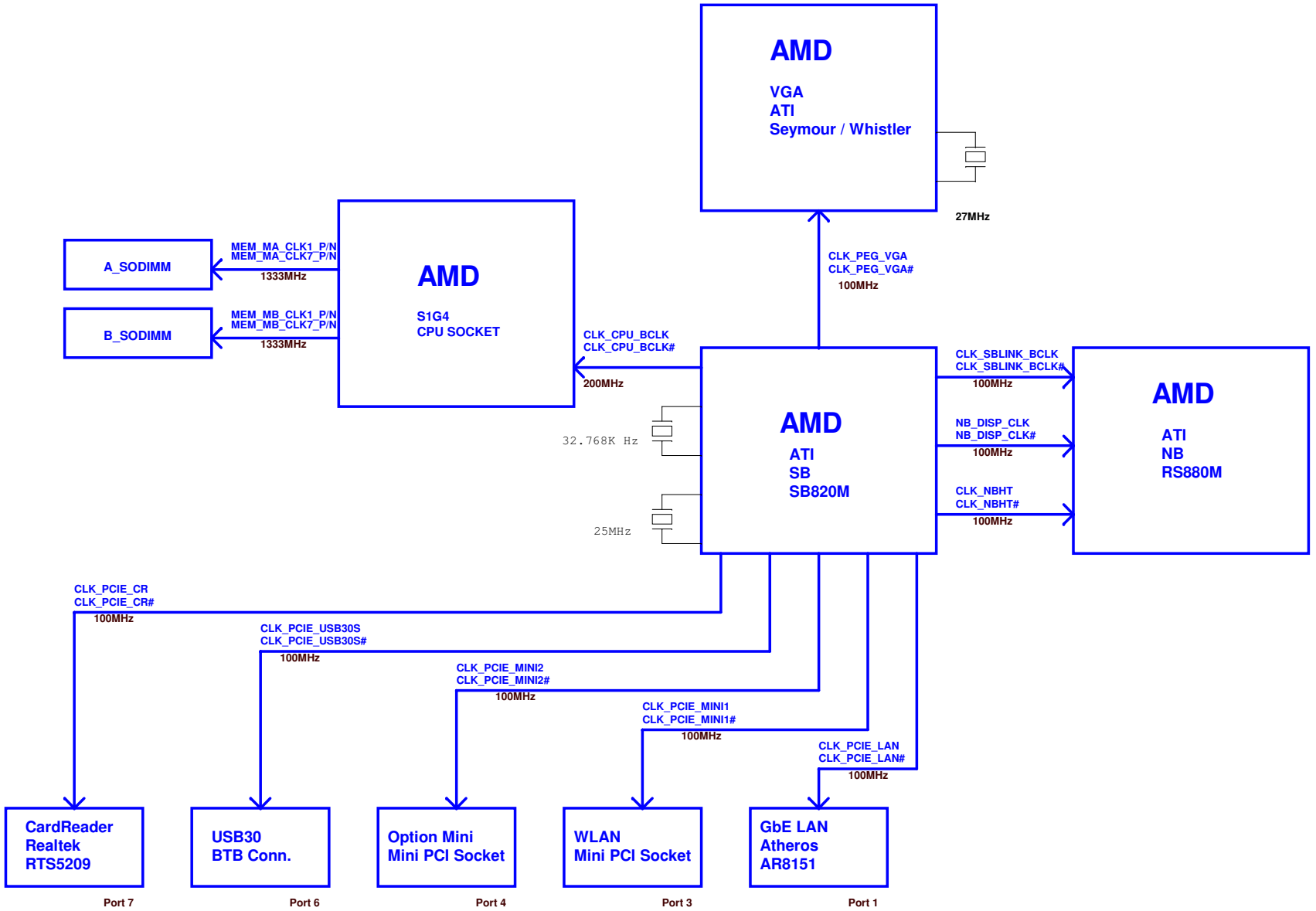
Model Name : P5WS3



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/10/06	Deciphered Date 2009/10/06	Title: Block Diagrams

Size: B	Document Number: P5WS3 LA-6972P		Rev: 0.1
Date: Tuesday, September 28, 2010	Sheet 2 of 53		



Security Classification	Compal Secret Data		
Issued Date	2005/10/10	Deciphered Date	2010/03/12

Title: CLOCK DISTRIBUTION

Size	Document Number	Rev
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU (0.7-1.3V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.2V)	ON	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.8V	1.8V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032 (CPU)	1001 100X b	98H
GMT G781-1 (GPU)	1001 101X b	9AH
SB-Temp Sensor		98H

SB820 SM Bus 0 address

Device	Address	HEX
Clock Generator (SILEGO SLG8SP626)	1101 001Xb	D2
DDR DIMM1	1001 000Xb	90
DDR DIMM2	1001 010Xb	94
Mini card		

SB820 SM Bus 1 address

Device	Address

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	0.1
2	0.2*
3	0.3
4	1.0
5	
6	
7	

Project ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure

BOM Config
DIS: 8151@/BT@/3G@/VGA@/DISO@/HDT@/WOBACO@
UMA : 8151@/BT@/3G@/HDT@/UMALVDS@/UMAHDMI@/UMACRT@/VB@/SBXTAL@
PowerXpress(Muxless):8151@/BT@/3G@/HDT@/UMALVDS@/UMAHDMI@/UMACRT@/VB@/VGA@/BACO@/PX@/SBXTAL@

Note:
For 4 VRAMs,DIS/Muxless with SEYM@
For 8 VRAMs,DIS/Muxless with WHI@
EC use external Crystal, with ECXTAL@
EC use internal CLK(SB820M),with SBXTAL@

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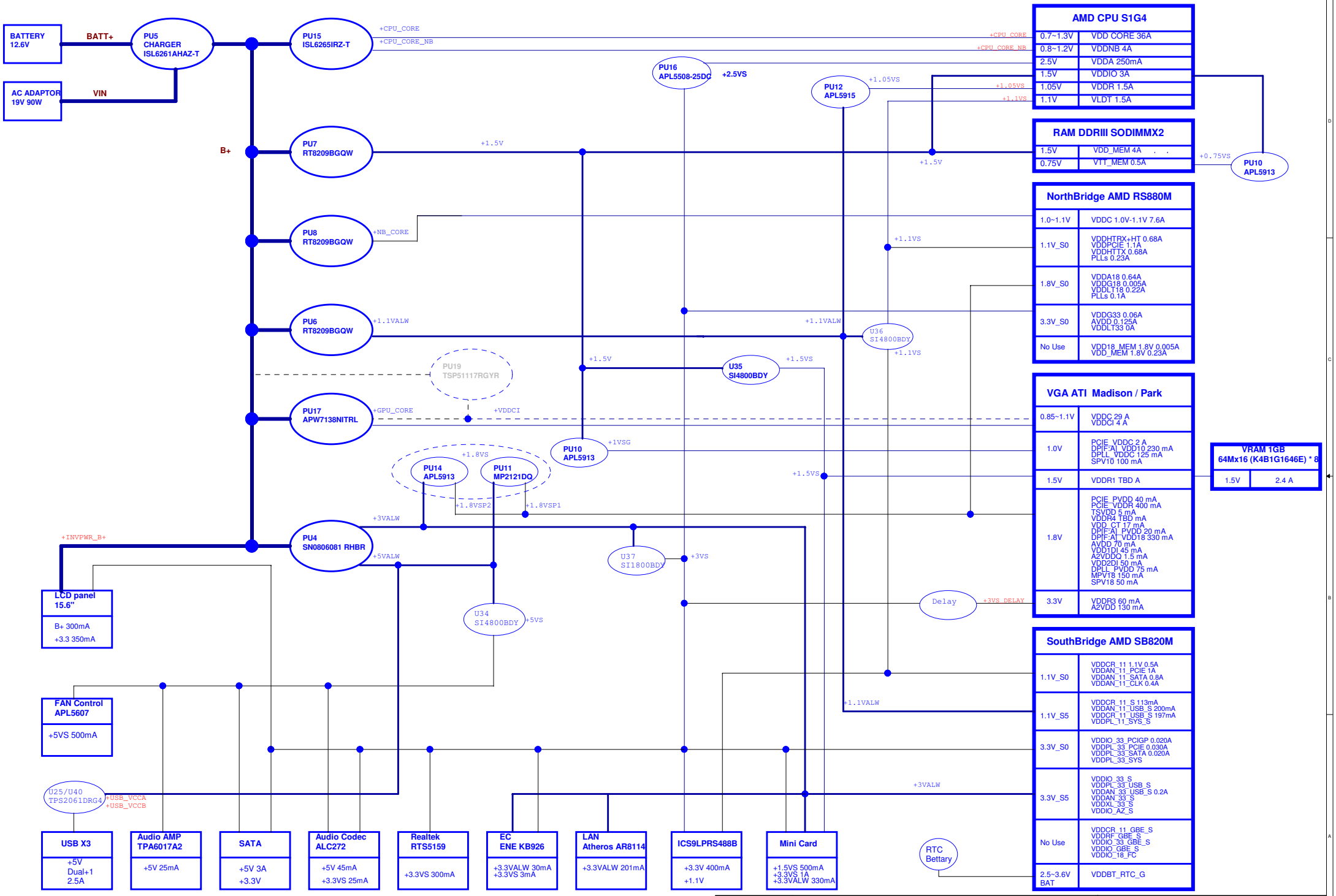
Title	Notes List		
Size B	Document Number P5WS3 LA-6972P		Rev 0.1
Date: Tuesday, October 19, 2010	Sheet 4 of 53		

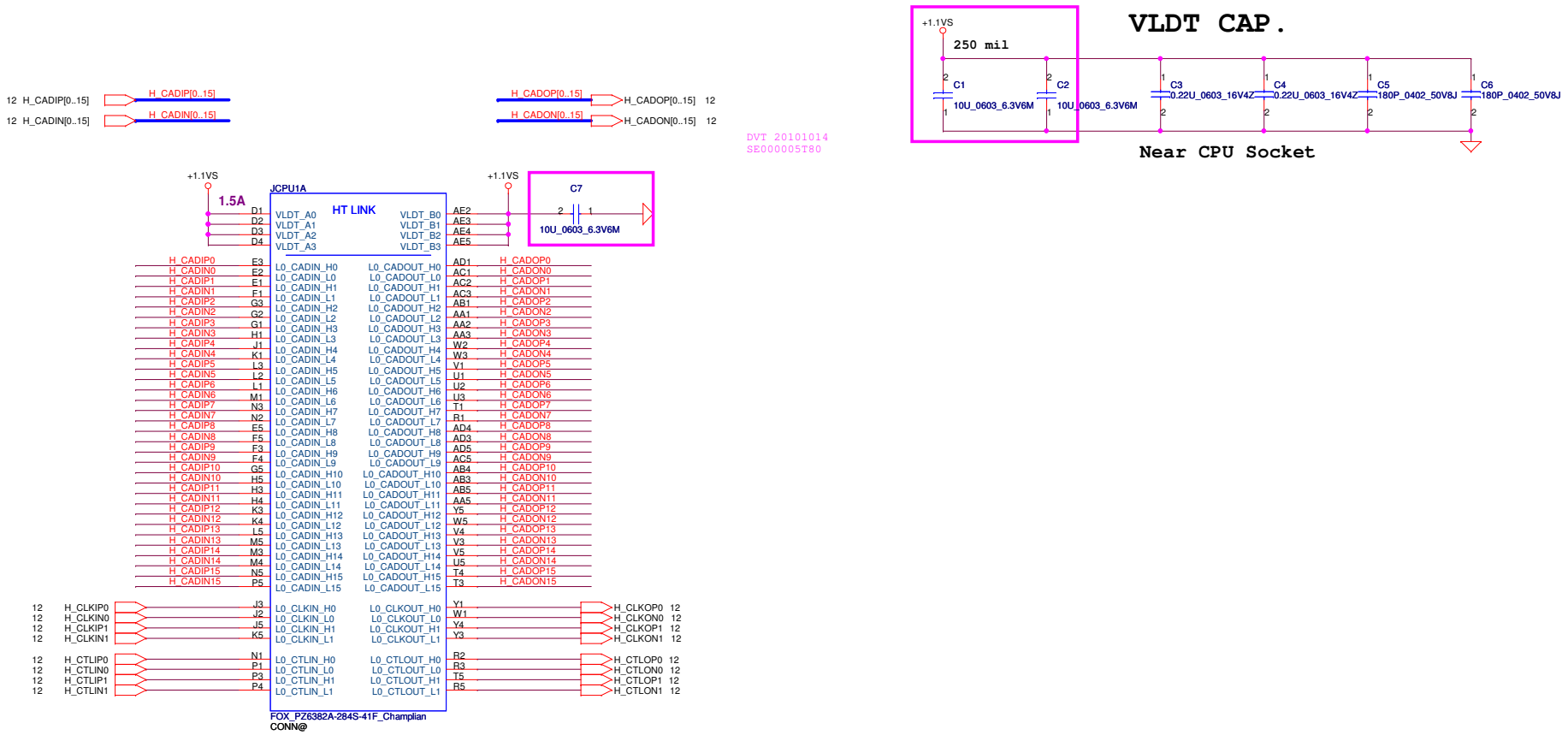


Security Classification	Compal Secret Data		
Issued Date	2009/3/8	Deciphered Date	2010/03/12

Title: POWER DELIVERY CHART

Size	Document Number	Rev
Custom	P5WS3 LA-6972P	0.1

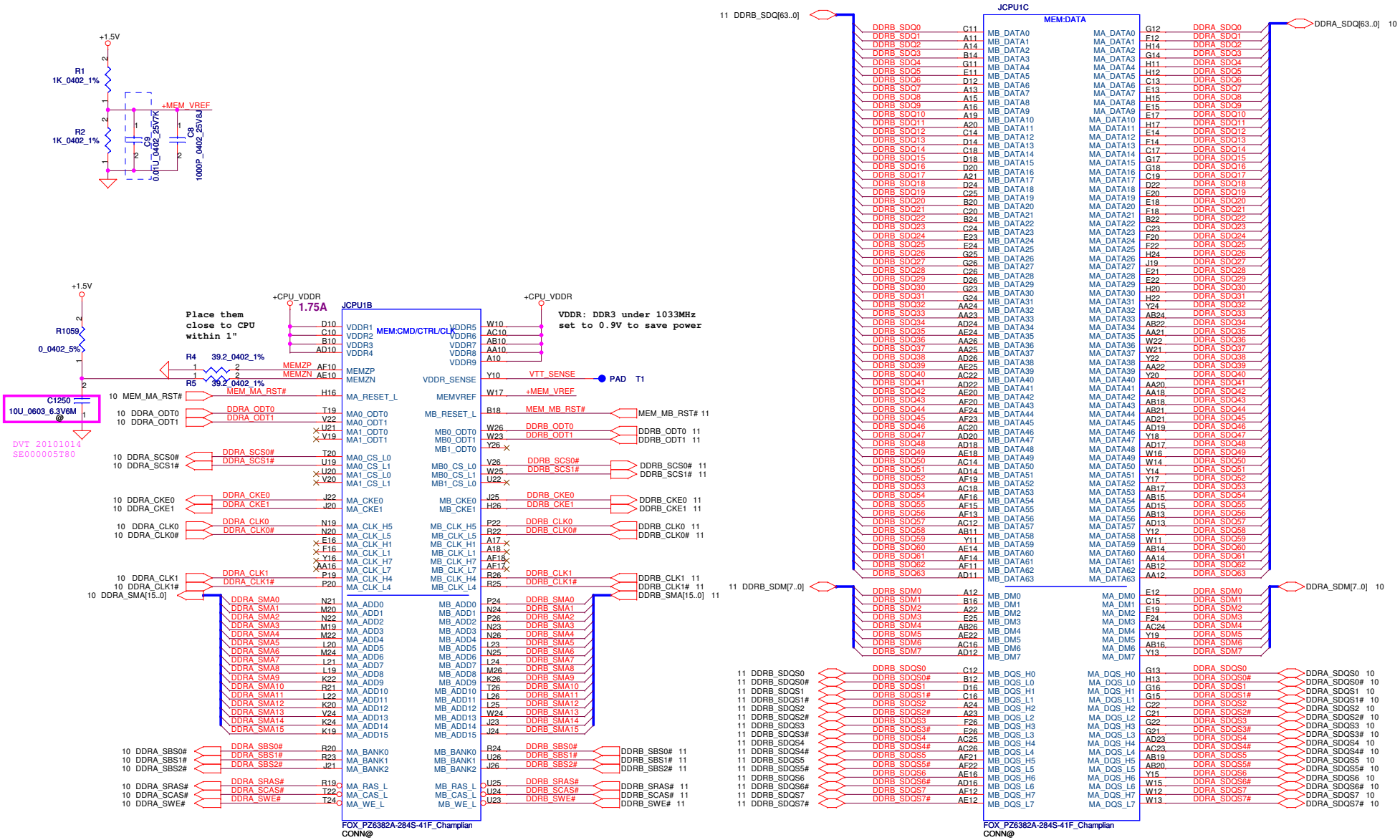
Date: Tuesday, September 28, 2010 Sheet 5 of 53



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/10/06	Deciphered Date 2010/03/12	Title: AMD CPU S1G4 HT I/F

Size: C Custom	Document Number: P5WS3 LA-6972P		Rev: 0.1
Date: Thursday, October 21, 2010	Sheet 6 of 53		

Processor DDR3 Memory Interface



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Issued Date	2008/10/06	Deciphered Date 2010/03/12	Title: AMD CPU S1G4 DDRII I/F
Size: Custom	Document Number: P5WS3 LA-6972P		Rev: 0.1
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Champlain: C1E
C1E: LDT_REQ# no connect
CLMC: LDT_REQ# connect to NB

LDT_RES# / MEMHOT#
no support in S1g4

VDDA=0.25A

JCPU1D

FOX_PZ6382A-284S-41F_Champlian
CONN@

PROCHOT:
Input: For HTC Function
Output: Over Temperature Condition

For SCAN connect use

ADM1032ARMZ_MSOP8

Address 1001 100X b

CPU internal thermal sensor

BSH111, the Vgs is:
min = 0.4V
Max = 1.3V

2.09V for Gate

CONN@ SAMTEC_ASP-68200-07

NC7SZ08P5X_NL_SC70-5

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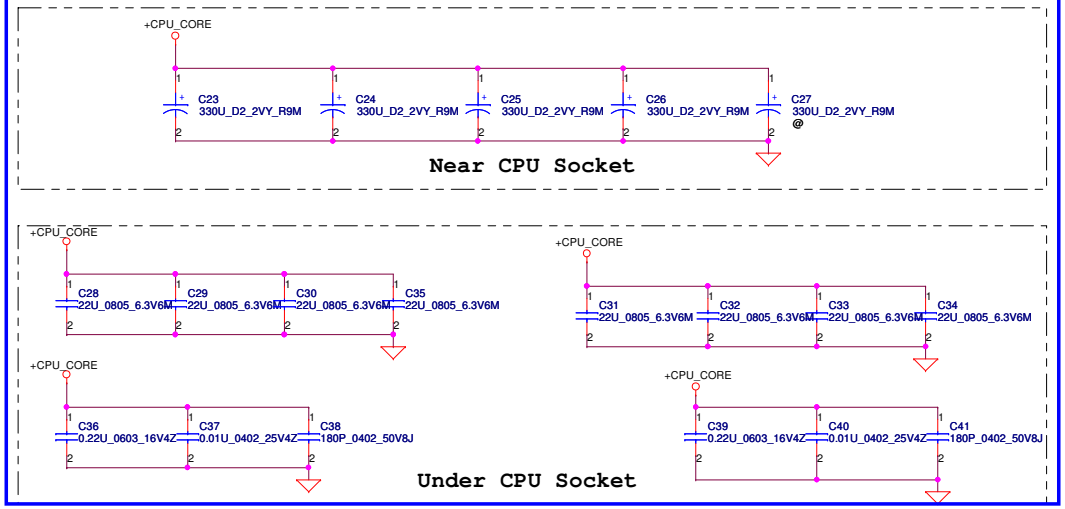
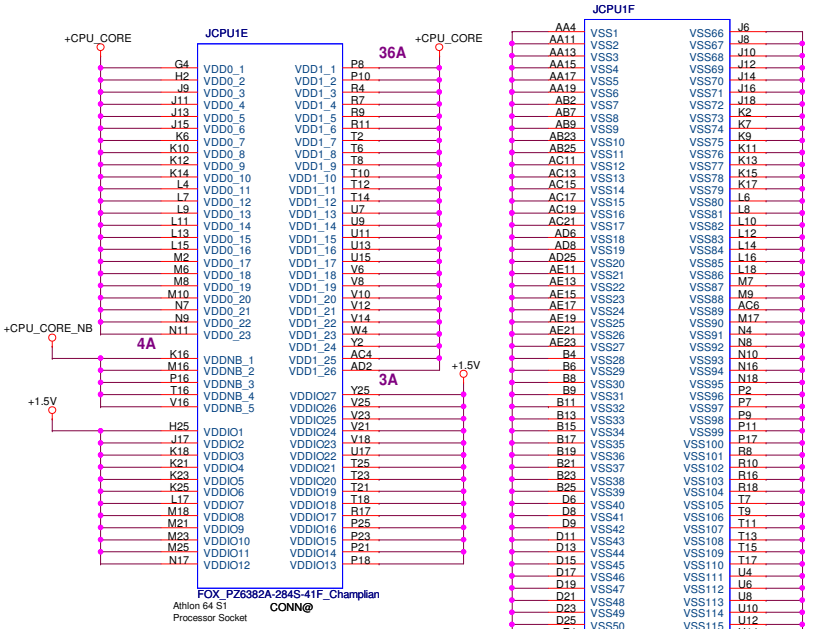
Title: AMD CPU S1G4 CTRL

Size: B25 Custom | Document Number: P5WS3 LA-6972P | Rev: 0.1

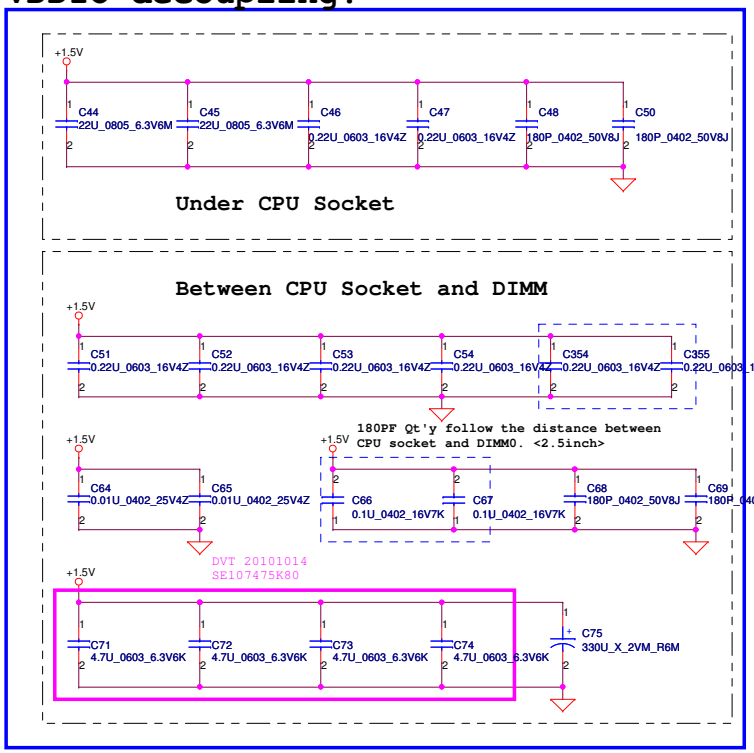
Date: Thursday, October 21, 2010 | Sheet 8 of 53

VDD(+CPU_CORE) decoupling.

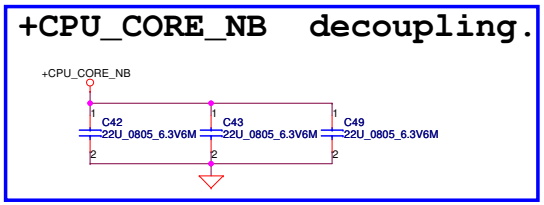




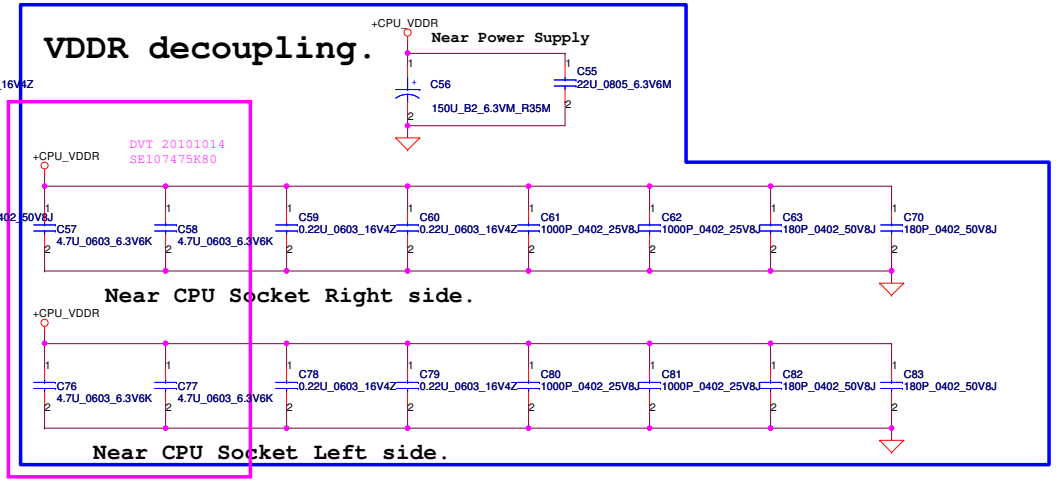
VDDIO decoupling.



+CPU_CORE_NB decoupling.



VDDR decoupling.



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Compal Electronics, Inc.

Title: AMD CPU S1G4 PWR & GND

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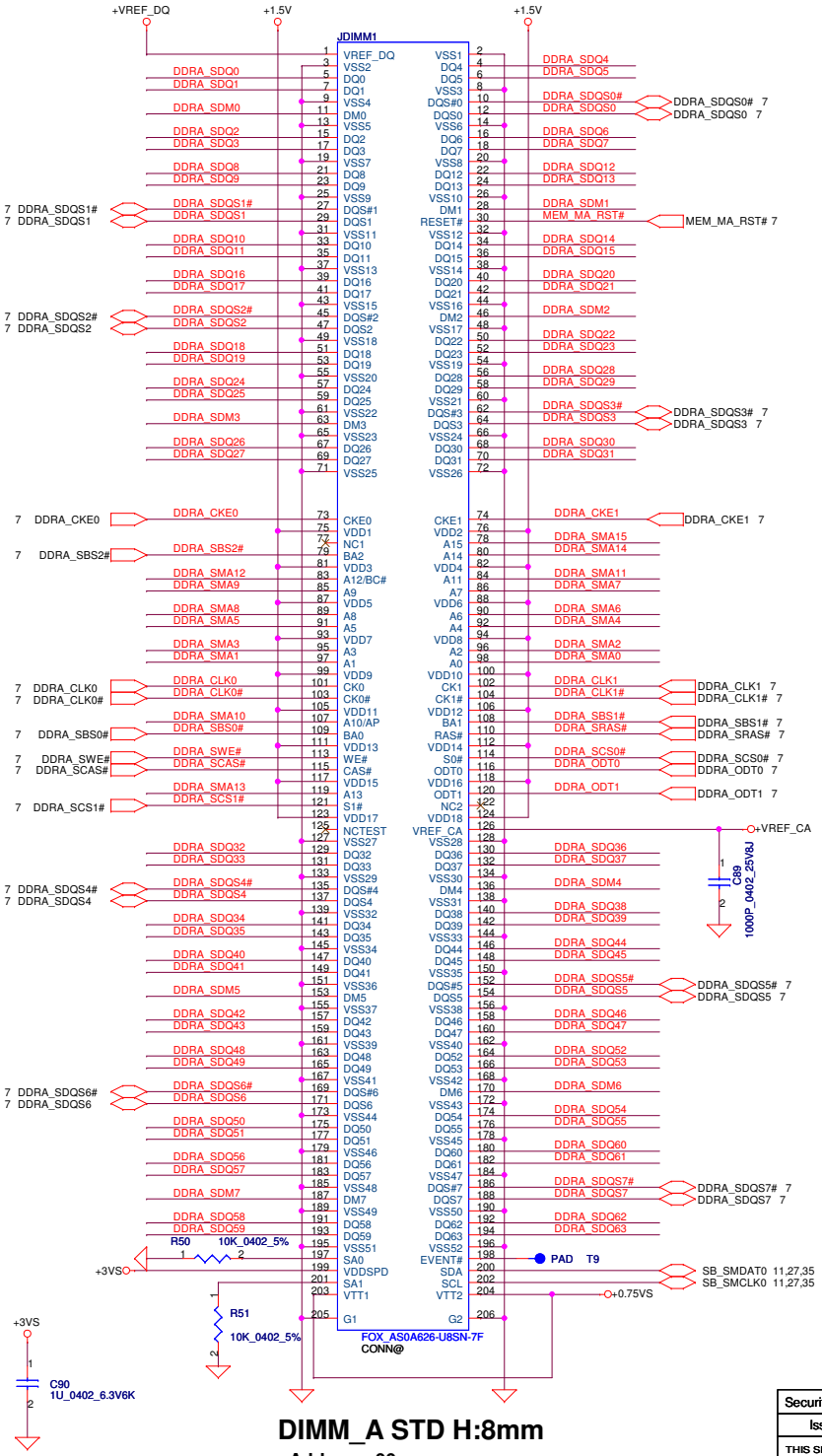
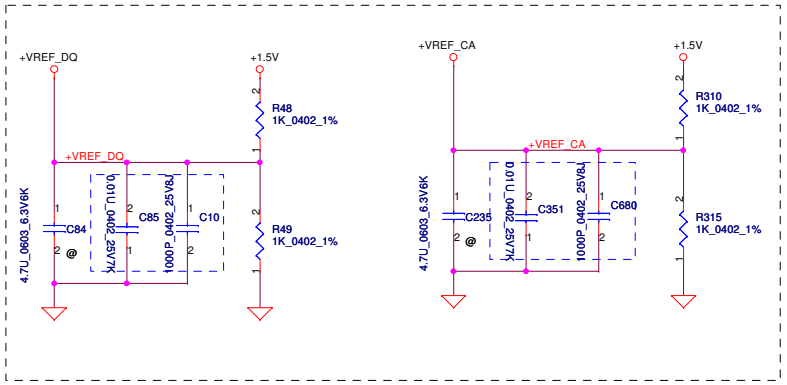
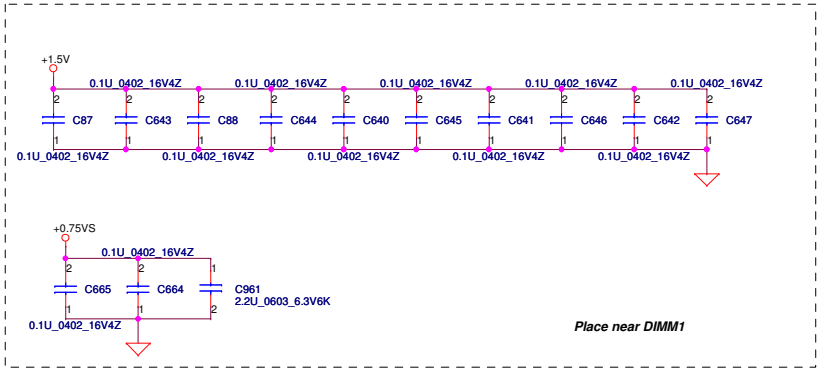
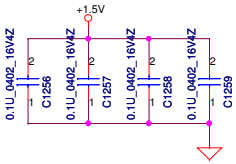
Date: Thursday, October 14, 2010 | Sheet 9 of 53



DDRA_SDQ[0..63] DDRA_SDQ[0..63] 7
DDRA_SDM[0..7] DDRA_SDM[0..7] 7
DDRA_SMA[0..15] DDRA_SMA[0..15] 7







DIMM_A STD H:8mm

<Address: 00>

Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

Compal Electronics, Inc.

Title: DDRII SO-DIMM 1

Size: Custom | Document Number: P5WS3 LA-6972P | Rev: 0.1

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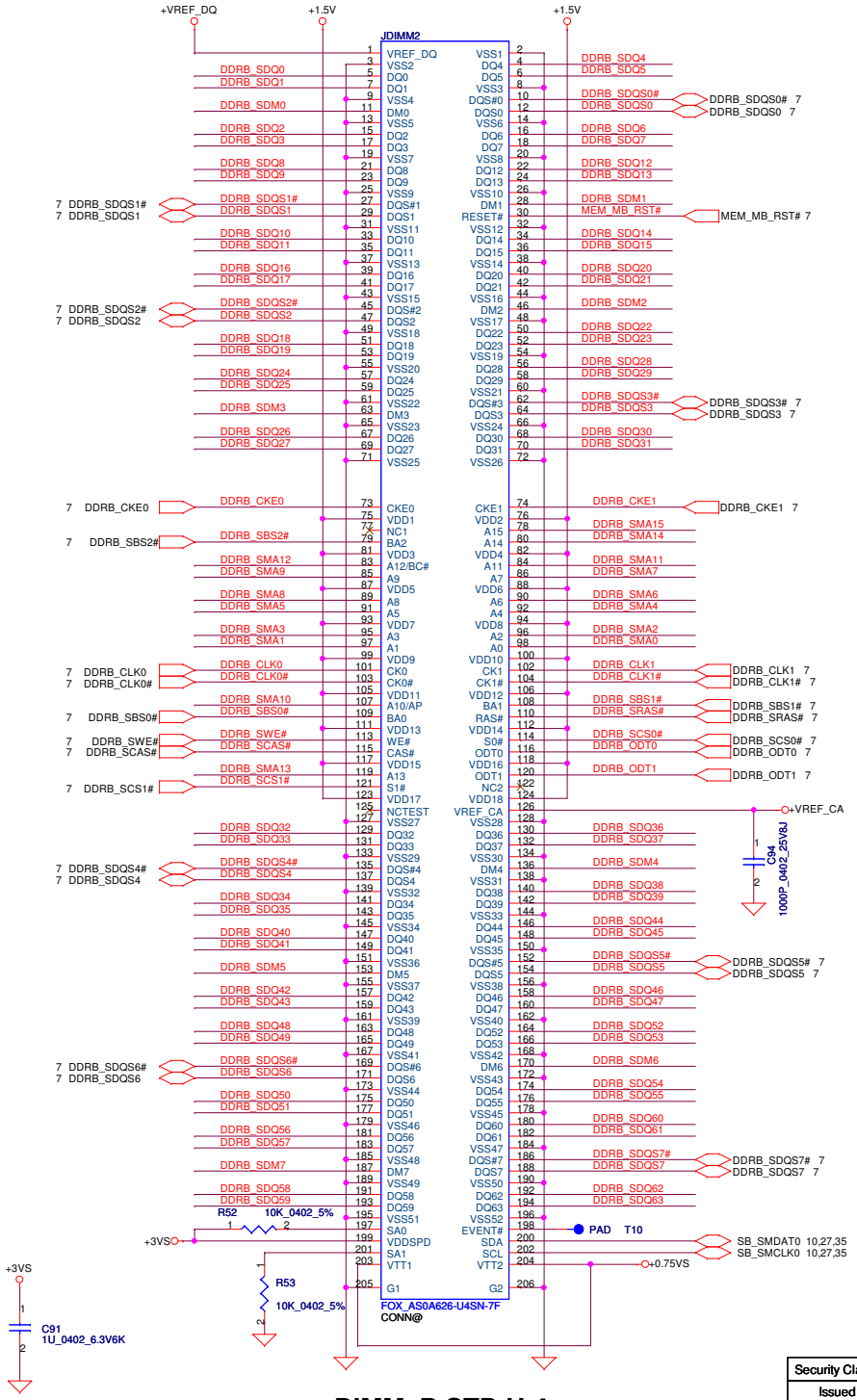

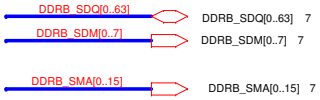

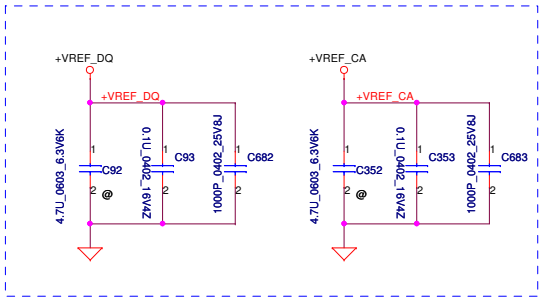

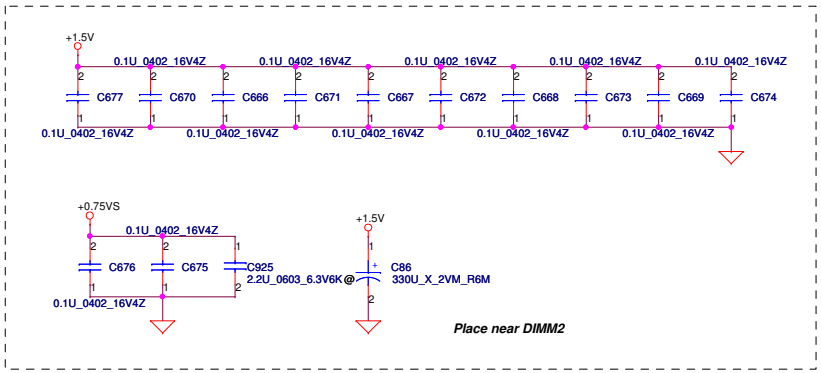

DIMM_B STD H:4mm

<Address: 01>

Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

Compal Electronics, Inc.

Title: DDRII SO-DIMM 2

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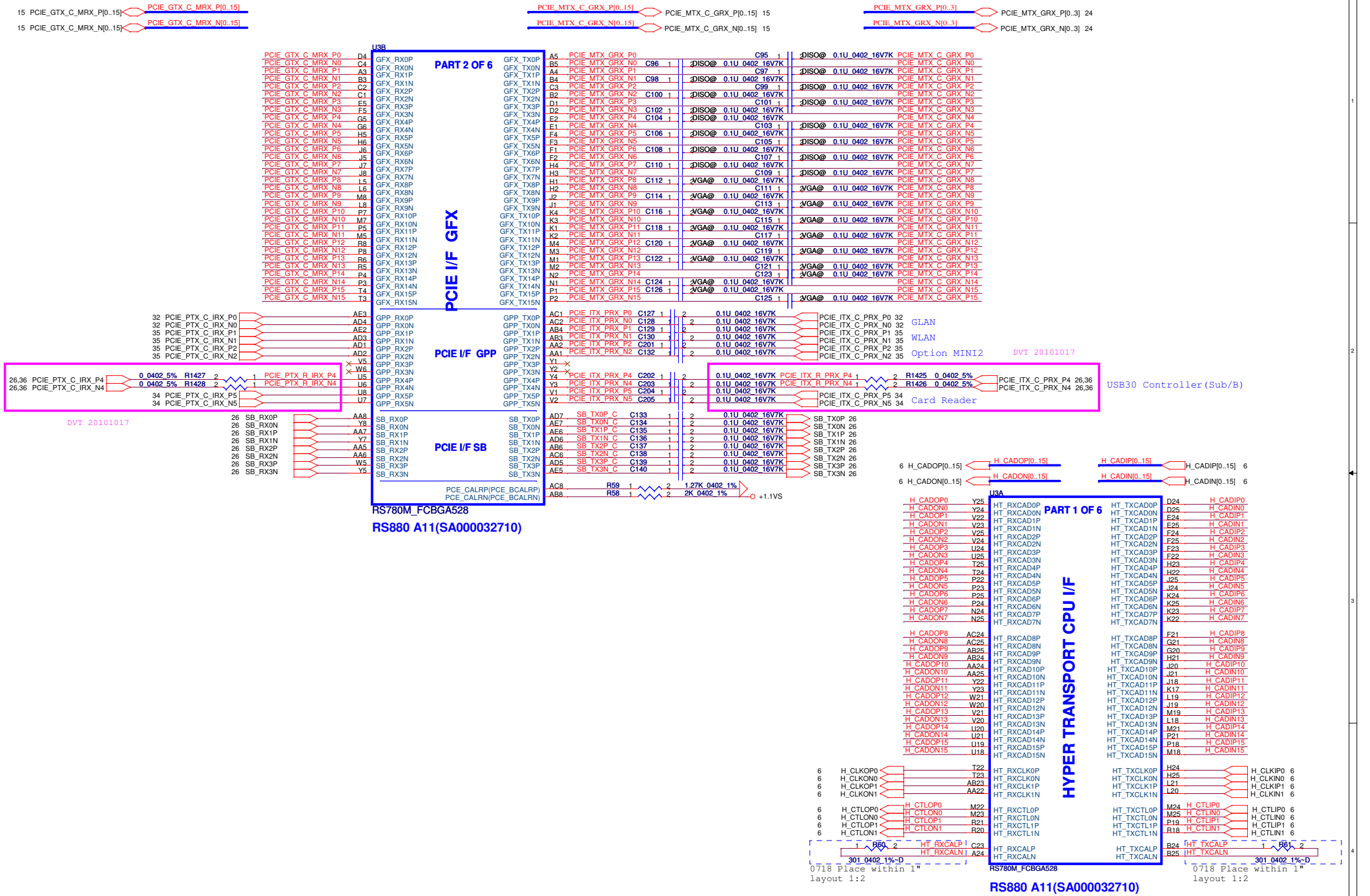
Date: Thursday, October 21, 2010 | Sheet 11 of 53



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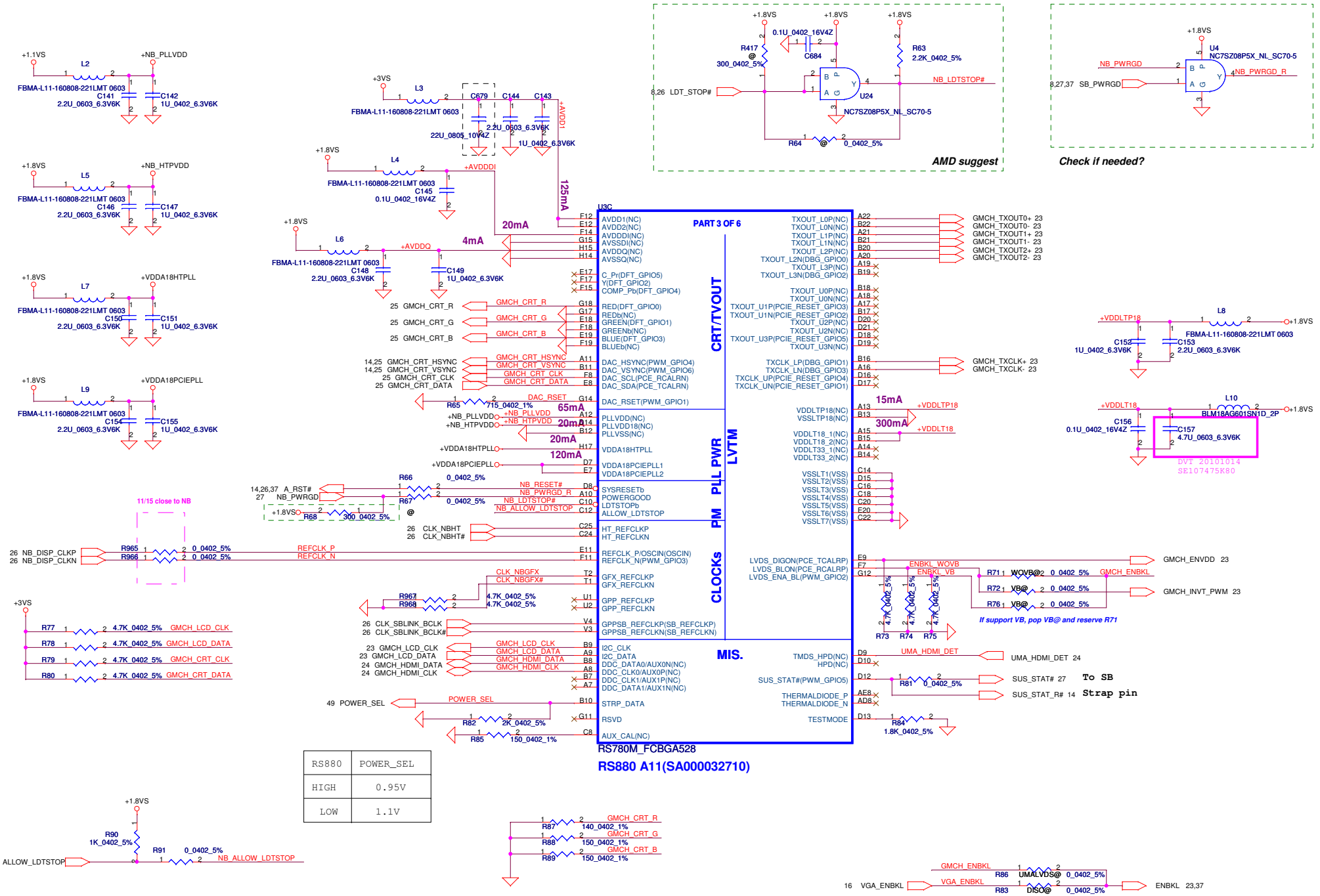
Compal Electronics, Inc.

Title: RS880-HT/PCIE

Size: B25 Custom | Document Number: P5WS3 LA-6972P | Rev: 0.1

Date: Thursday, October 21, 2010 | Sheet 12 of 53



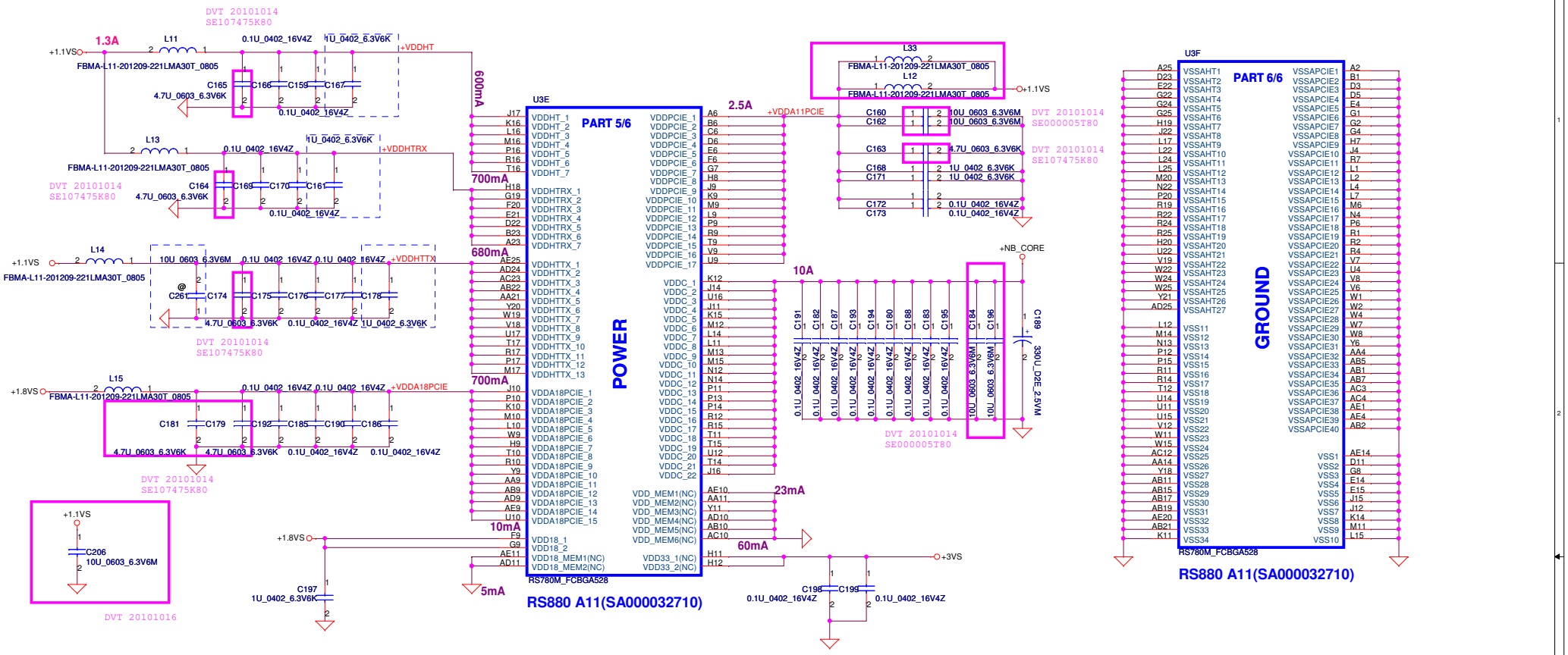
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

Compal Electronics, Inc.

Title: RS880 VEDIO/CLK GEN

Size: Custom | Document Number: P5WS3 LA-6972P | Rev: 0.1

Date: Thursday, October 21, 2010 | Sheet 13 of 53



Side port and Strap setting

Debug Mode

13,25 GMCH_CRT_VSYNC — R92 3K_0402_5% — +3VS
R93 @ 3K_0402_5%

Load EEPROM Strap

13 SUS_STAT_R# — D1 @ RB751V-40_SC76 — A_RST# 13,26,37
R264 @ 3K_0402_5%

Enable Side Port Memory

13,25 GMCH_CRT_HSYNC — R94 3K_0402_5% — +3VS
R95 @ 3K_0402_5%

DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

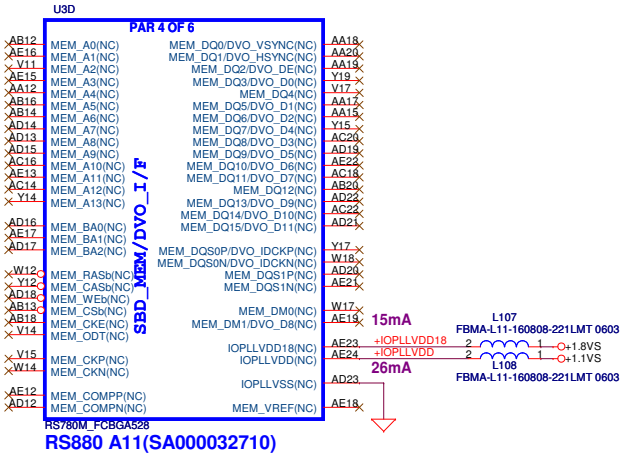
```
Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable
0 : Enable
```

DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
```

Enable Side Port Memory

```
RS880: HSYNC#
0:   Enable      Register Readback of strap:
1 :  Disable     NB_CLKCFG:CLK_TOP_SPARE_D[1]
```



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

Compal Electronics, Inc.

Title: RS880 PWR/GND

Size: B25 Custom | Document Number: P5WS3 LA-6972P | Rev: 0.1

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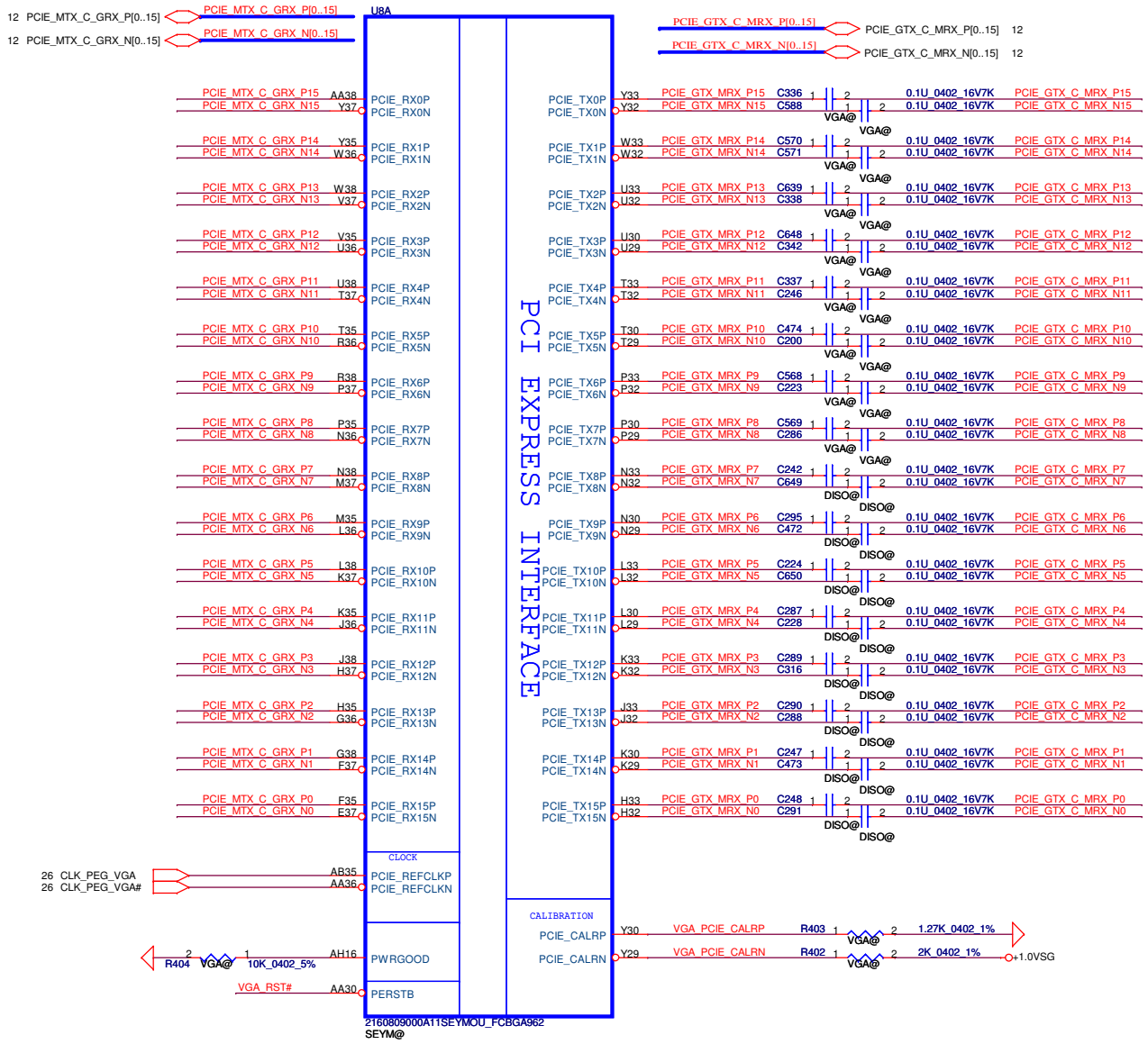
GFX PCIE LANE REVERSAL



Seymour XT P/N: SA000047H10 (S IC 216-0809000 A11 SEYMOUR XT M2 ABO!)

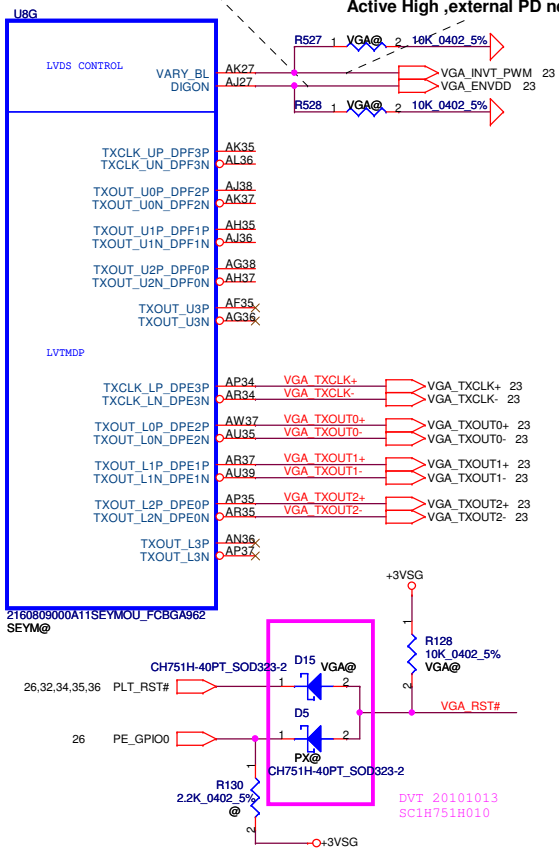
U8 WHI@

216-0810005 A11

WHISTLER PRO M2 A11:
SA00004C720(S IC 216-0810005 A11 WHISTLER PRO FCBGA 962P ABO !)

Controls panel digital power on/off. Active High ,external PD need

LCD PWM (pulse width modulated) output to adjust LCD brightness Active High ,external PD need



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: Vancouver_ PCIE / LVDS

Size: Custom | Document Number: P5WS3 LA-6972P | Rev: 0.1

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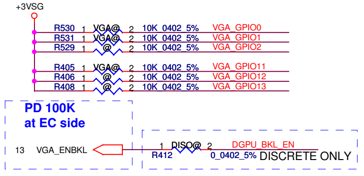
Strap Name	Pin	Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNC (GENLK_VSYNC)	VIP Device Strap Enable indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines (Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis diabled 1: Tx de-emphasis enabled	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : (Internal PD) a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. memory apertures CONFIG[3:0] 128 MB 000 256 MB 001 * 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device (Internal PD) 0: Diable, 1: Enable	0
AUD[1] AUD(0)	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

Don't have this strap on Whistler and Seymour



DVT 20101019

SEYMOUR-XT

ID3-0	Vendor	Size	Freq	P/N	Description
0100	SAM	E-die 64*16	800MHz	SA000035720	K4W1G1646E-HC12
1110	HYN	Vega-die 64*16	900MHz	SA000041S40	H5TQ1G63DFR-11C
1011	HYN	Vega-die 64*16	800MHz	SA000041S40	H5TQ1G63DFR-11C

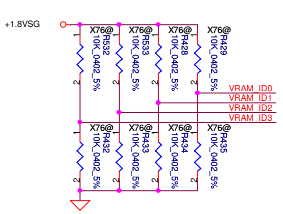
WHISTLER-PRO

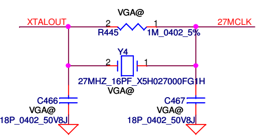
ID3-0	Vendor	Size	Freq	P/N	Description
0000	SAM	E-die 64*16	800MHz	SA000035720	K4W1G1646E-HC12
0001	SAM	C-die 128*16	800MHz	SA00003MQ60	K4W2G1646C-HC12
1001	HYN	Vega-die 128*16	800MHz	SA00003VS10	H5TQ2G63BFR-12C
1010	HYN	Vega-die 64*16	900MHz	SA000041S40	H5TQ1G63DFR-11C
1011	HYN	Vega-die 64*16	800MHz	SA000041S40	H5TQ1G63DFR-11C

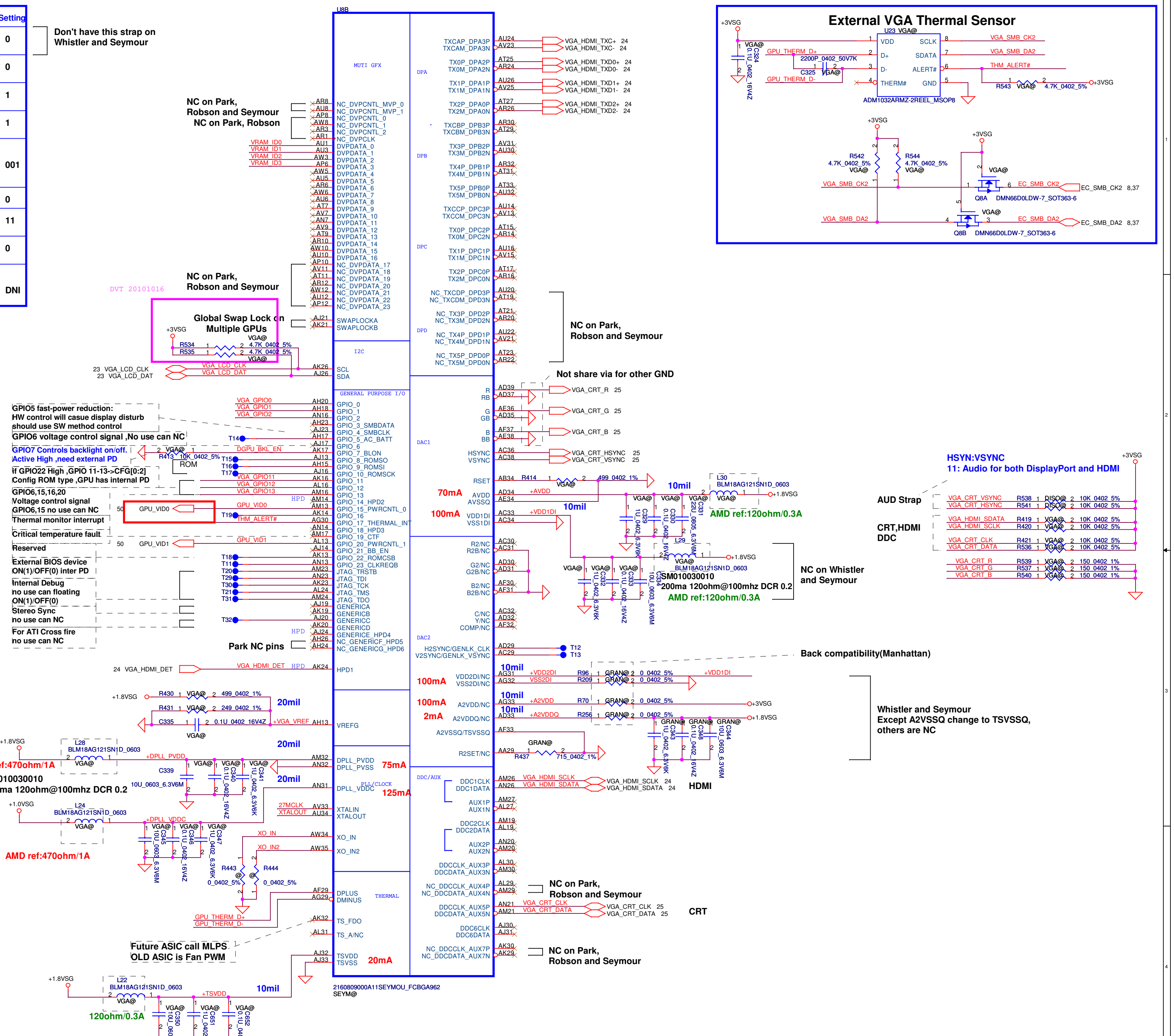
ID3/ID1: VRAM Vender
00:Samsung
10:Hynix
11:Hynix new Die

ID2 : VRAM Pcs
1(4PCS),
0(8PCS)

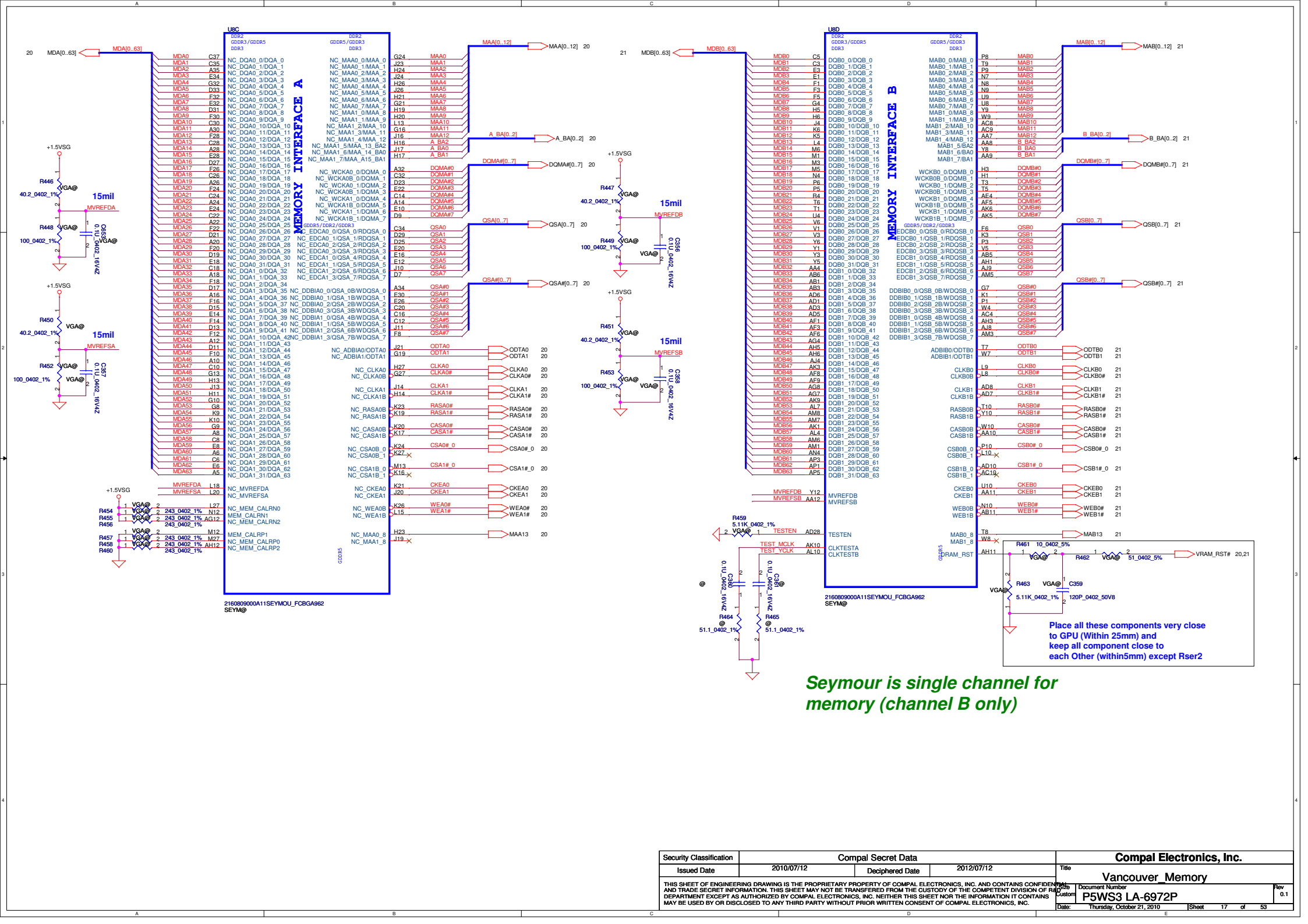
ID0 : VRAM Size
0(64x16)
1(128*16)







Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/07/12	Deciphered Date	2012/07/12	Title: Vancouver_Strape/DP/HDMI//CRT
				Size: Custom; Document Number: P5WS3 LA-6972P; Rev: 0.1
				Date: Thursday, October 21, 2010; Sheet 16 of 53



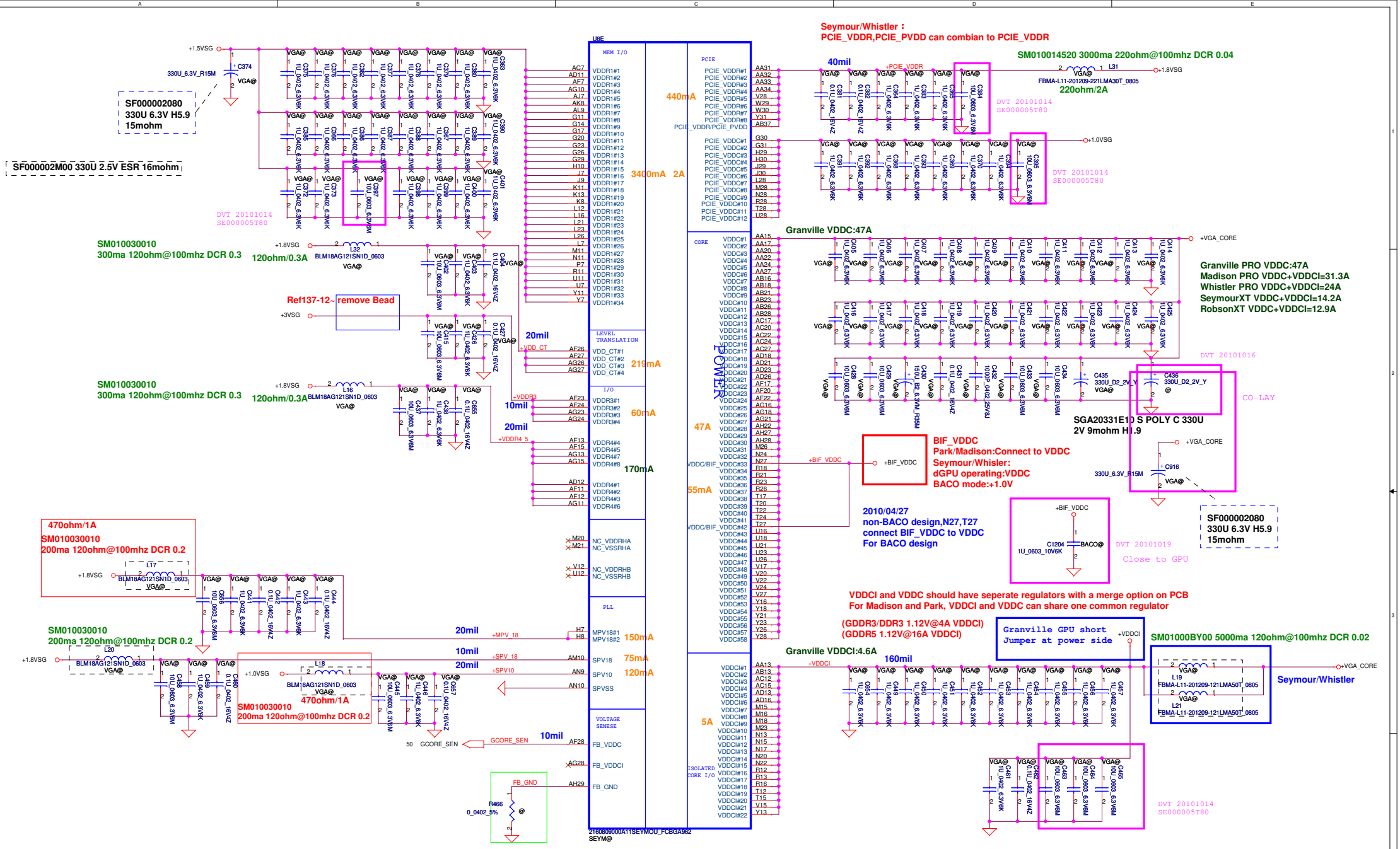
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: Vancouver_Memory

Size: Custom | Document Number: P5WS3 LA-6972P | Rev: 0.1

Date: Thursday, October 21, 2010 | Sheet 17 of 53



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: Vancouver_Power/GND

Size	Document Number	Rev
Custom	P5WS3 LA-6972P	0.1

Date: Thursday, October 21, 2010 | Sheet 18 of 53

DPA_VDD18,DPA_PVDD,DPB_VDD18,DPB_PVDD
can combian to DPAB_VDD18
DPC_VDD18,DPC_PVDD,DPD_VDD18,DPD_PVDD
can combian to DPCD_VDD18
(DPD_VDD18,DPD_PVDD not applicable on Robson/Park)
DPE_VDD18,DPE_PVDD,DPF_VDD18,DPF_PVDD
can combian to DPEF_VDD18

DPx-VSSR,DPx_PVSS can combian to DP_VSSR
(Manhatann should have individual GND)
where x is A,B,C,D,E,F

Seymour/Whistler：
DPA_VDD10,DPB_VDD10
can combian to DPAB_VDD10
DPC_VDD10,DPD_VDD10
can combian to DPCD_VDD10
DPE_VDD10,DPD_VDD10
can combian to DPEF_VDD10

U8F

GND

216080900OA11SEYMOU_FCBGA962
SEYM@

U8H

DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER

216080900OA11SEYMOU_FCBGA962
SEYM@

Manhatann:300mA
Seymour:150mA

Manhatann:220mA
Seymour:110mA

SM01000BL00
1000ma 470ohm@100mhz DCR 0.2
L23 MBK1608221YZF_2P
L25 MBK1608221YZF_2P
L26 MBK1608221YZF_2P
L27 MBK1608221YZF_2P
FootPrint

DP mode:300mA
LVDS mode:440mA

DP mode:220mA
LVDS mode:240mA

DVT 20101019

PX_EN
R469 5.11K_0402_1%
PX_EN 22

PX_EN:
SBIOS will control VGA power on/off.
High :BACO mode enable
LOWLBACO disable

Park/Madison :AL21left NC

Seymour/Whistler:
AL21:PX_EN
use to control discreate GPU regulators
for power express BACO mode
Support BACO:
output High3.3V:turn off regulators (BACO mode on)
output Low0V:turn on regulators (BACO mode off)
need PD resistor
No support BACO:
left NC

NCGND R1420 0_0402_5%

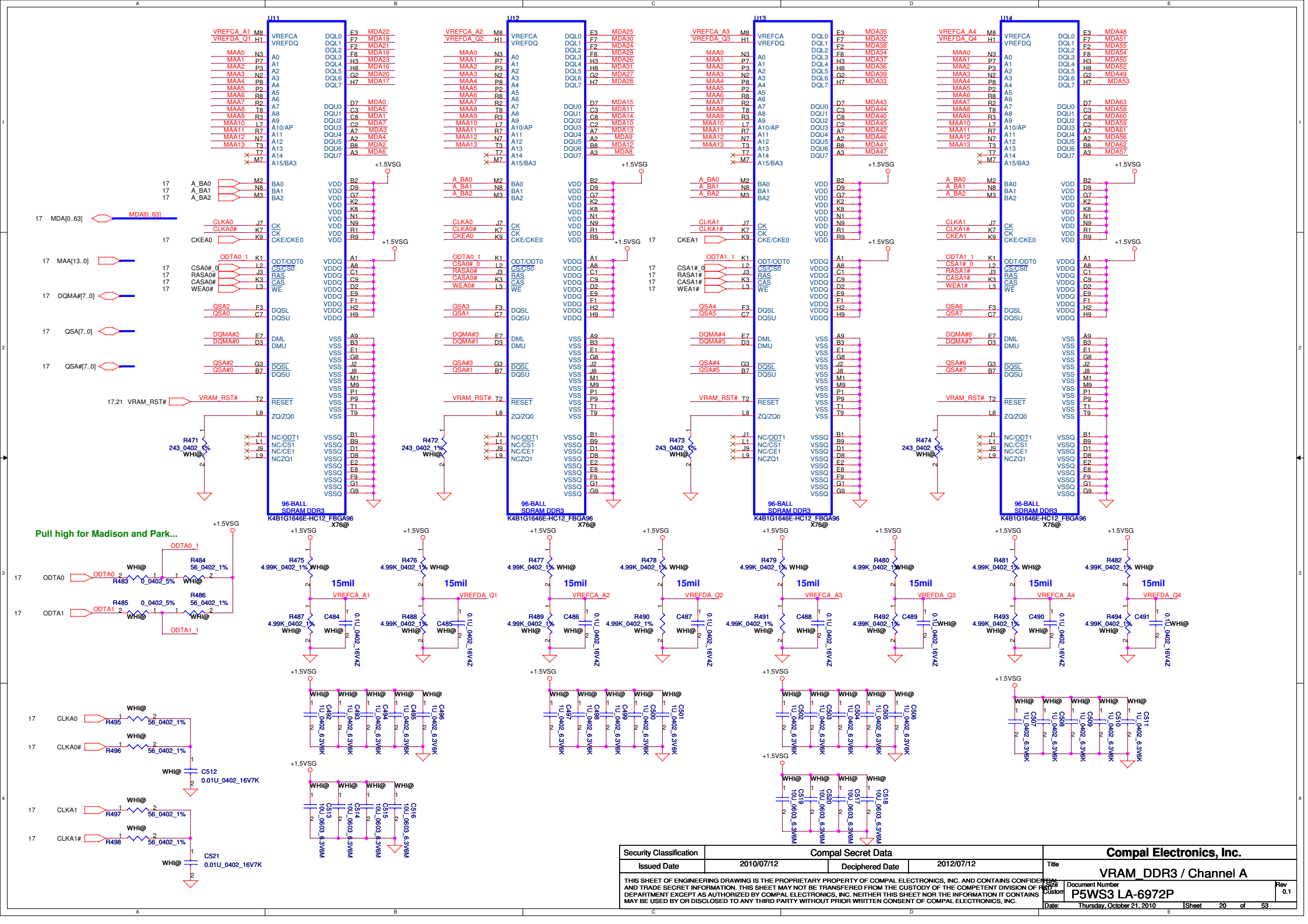
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: Vancouver_Power/GND

Size: Custom | Document Number: P5WS3 LA-6972P | Rev: 0.1

Date: Thursday, October 21, 2010 | Sheet 19 of 53



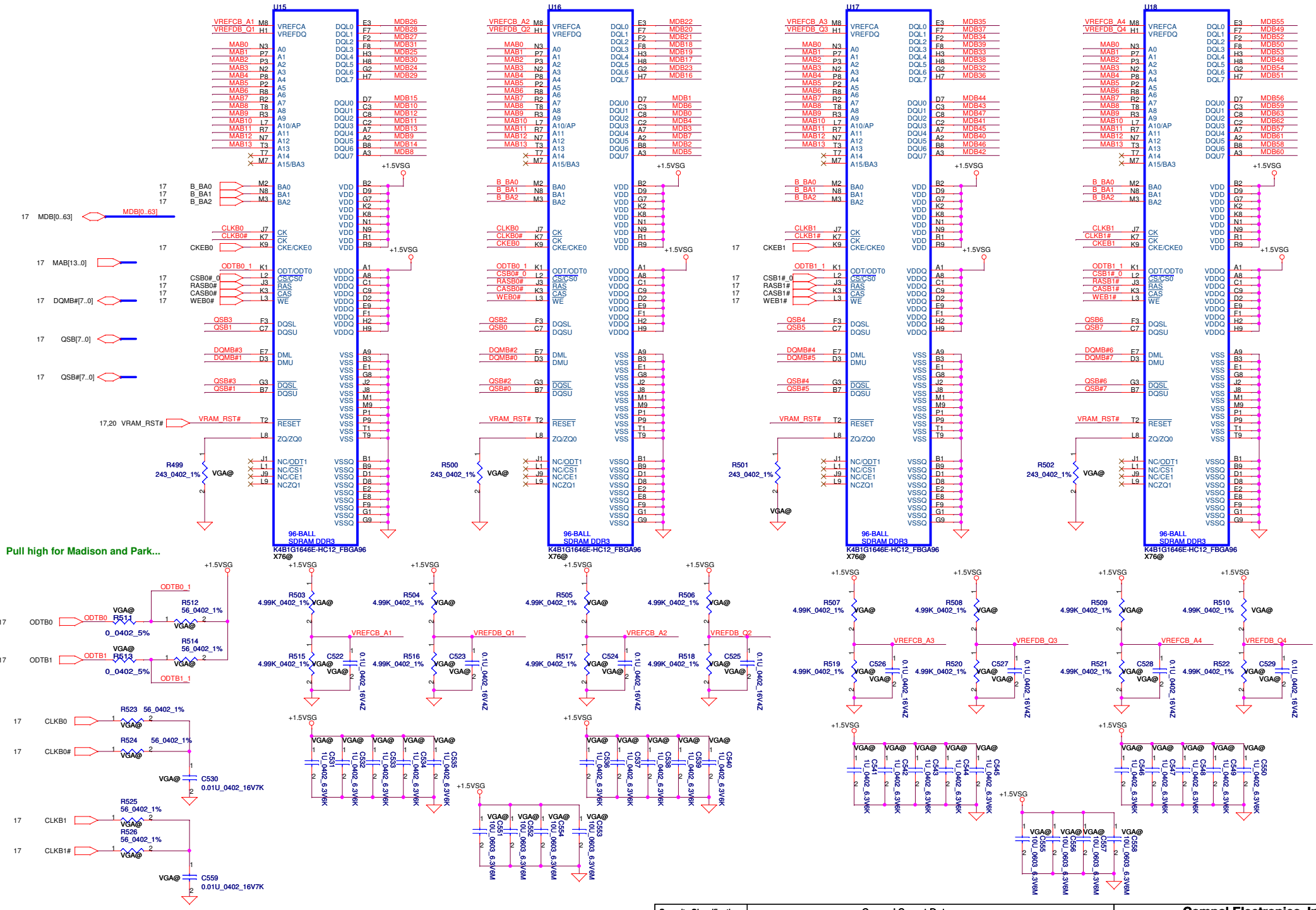
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: VRAM_DDR3 / Channel A

Size: Custom | Document Number: P5WS3 LA-6972P | Rev: 0.1

Date: Thursday, October 21, 2010 | Sheet 20 of 53



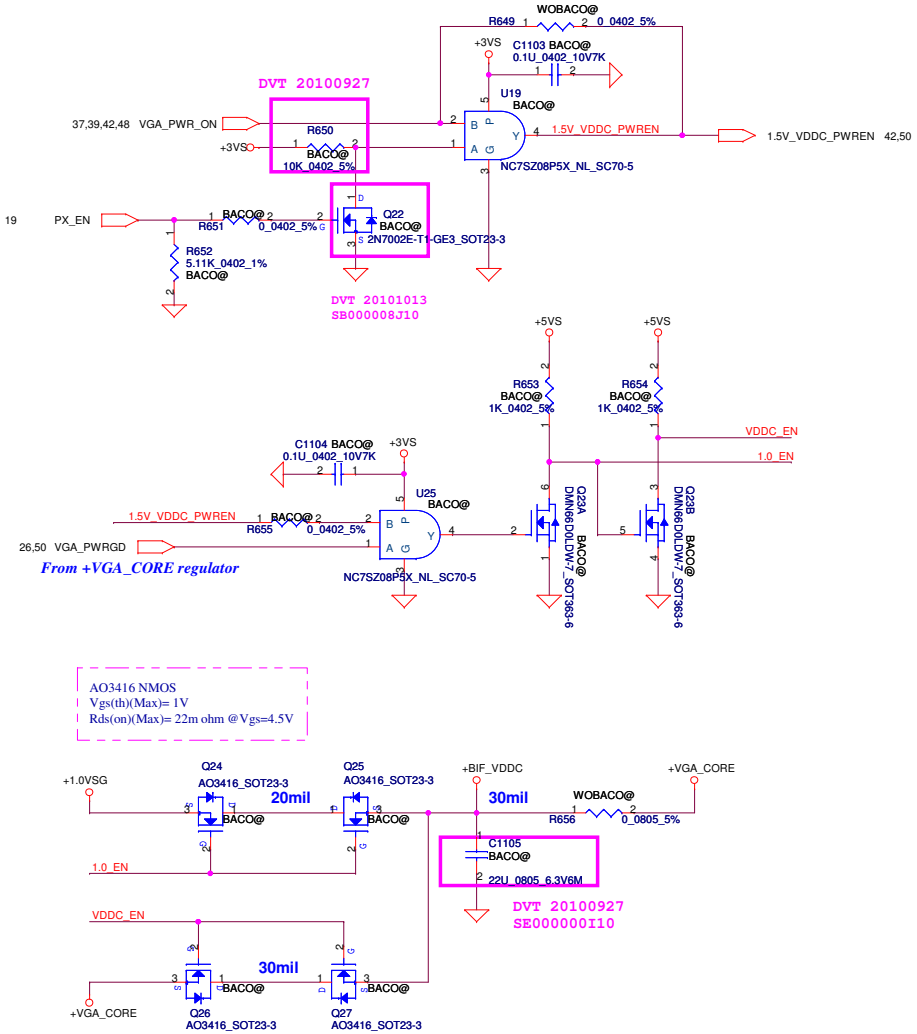
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: VRAM_DDR3 / Channel B

Size: Custom | Document Number: P5WS3 LA-6972P | Rev: 0.1

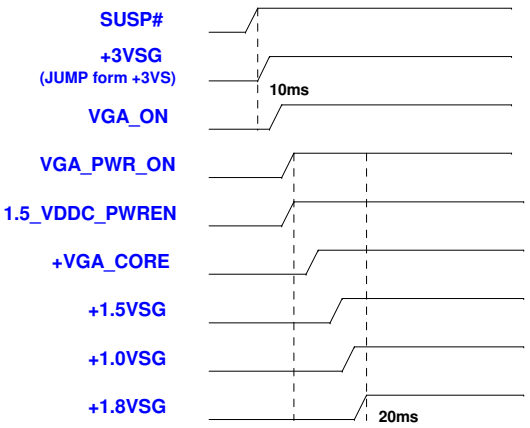
Date: Thursday, October 21, 2010 | Sheet 21 of 53



VGA Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

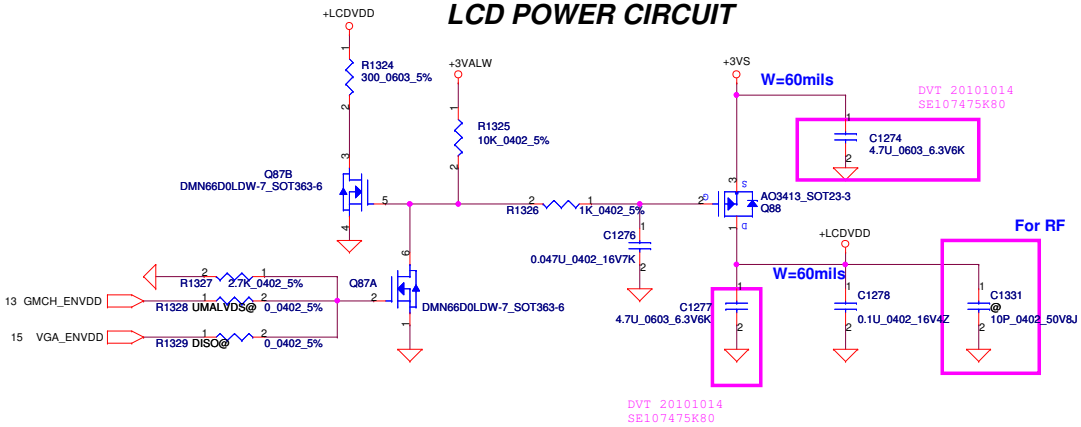
VGA Power Enable Signal Mapping table		
	Graville	Whistler and Seymour
+3.3VSG	VGA_PWR_ON	SUSP#
+1.8VSG	VGA_PWR_ON	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON	VGA_PWR_ON
+VDDCI	VGA_PWR_ON	Combine with +VGA_CORE
+VGA_CORE	VGA_PWR_ON	1.5_VDDC_PWREN
+1.5VSG	VGA_PWR_ON	1.5_VDDC_PWREN

Power Sequence of Whistler and Seymour

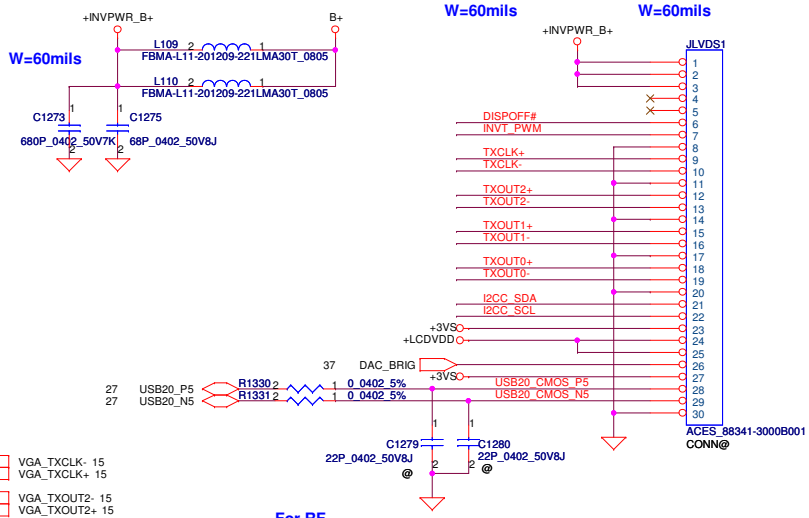


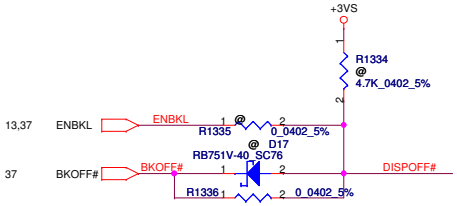
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/08/04	Deciphered Date 2010/08/04	Title: Vancouver_BACO
			Size: Custom; Document Number: P5WS3 LA-6972P; Rev: 0.1
			Date: Thursday, October 21, 2010; Sheet 22 of 53

LCD POWER CIRCUIT

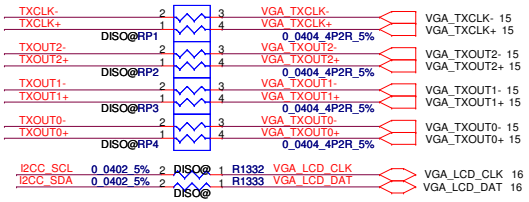


LCD/LED/eDP PANEL Conn.

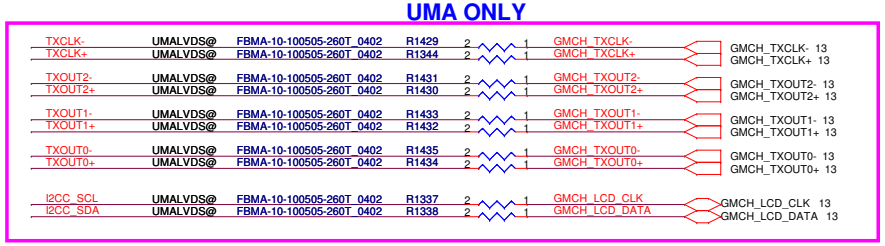




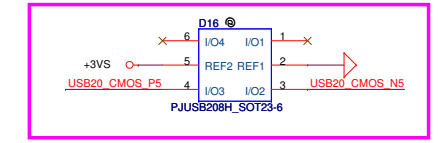
VGA ONLY



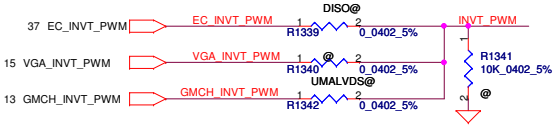
UMA ONLY



DVT 20101018
For RF
DVT 20101019
SM01000GC00 S SUPPRE_ KC FBMA-10-100505-260T 0402

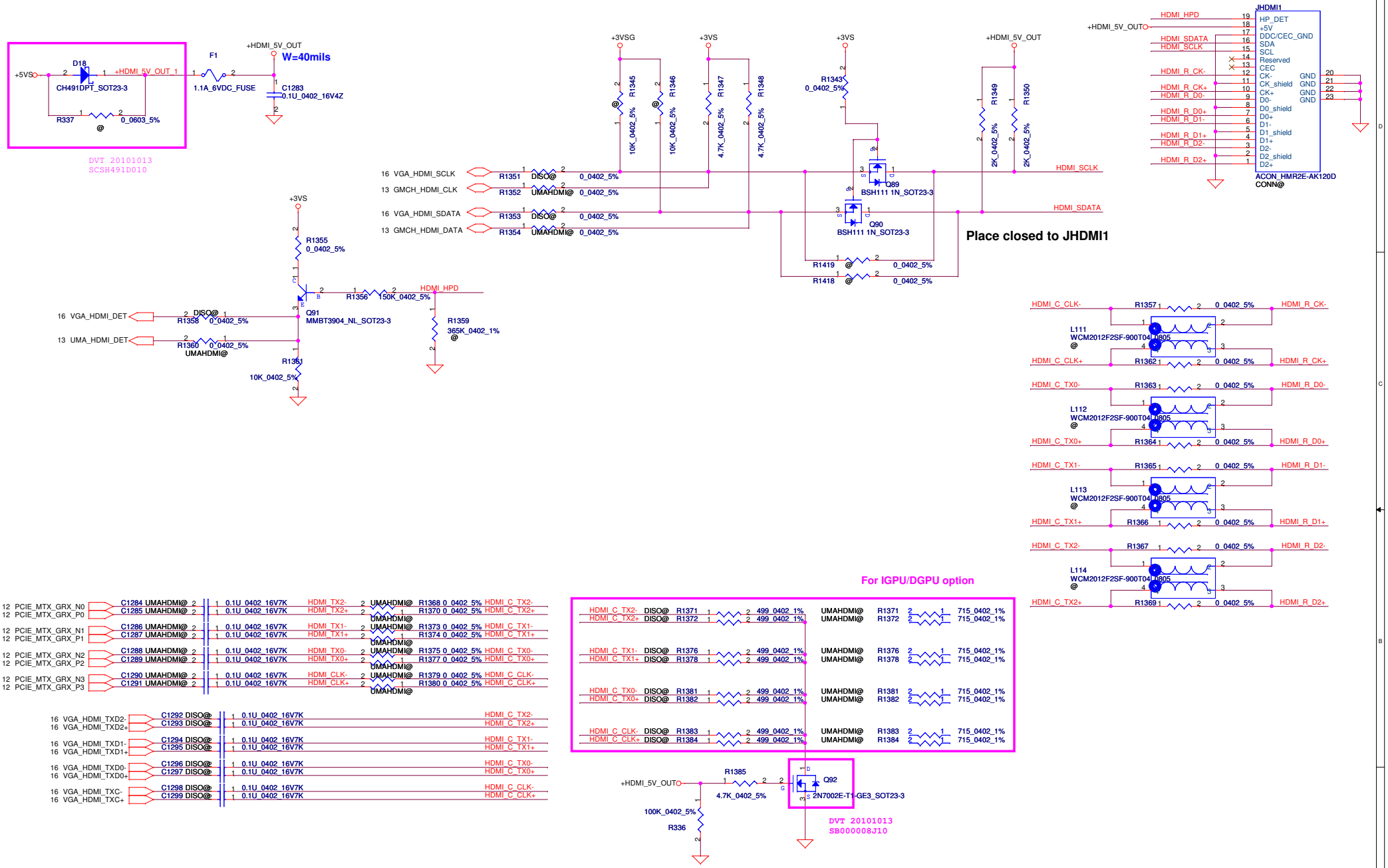


DVT 20101004
SC300000B10



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/10/06	Deciphered Date 2010/03/12	Title: LVDS Connector

Size B	Document Number P5WS3 LA-6972P		Rev 0.1
Date: Thursday, October 21, 2010	Sheet 23 of 53		



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

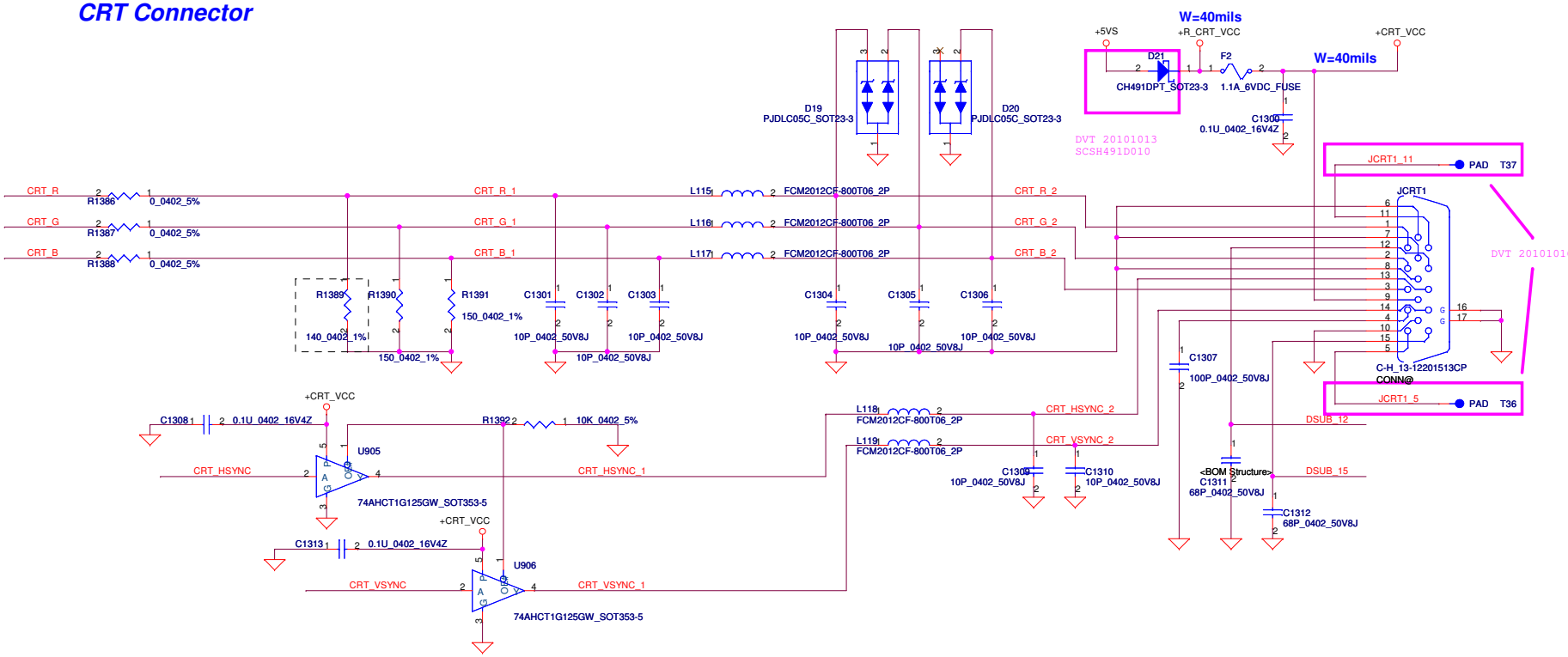
Compal Electronics, Inc.

Title: HDMI Connector

Size	Document Number	Rev
Custom	P5WS3 LA-6972P	0.1

Date: Thursday, October 21, 2010 Sheet 24 of 53

CRT Connector



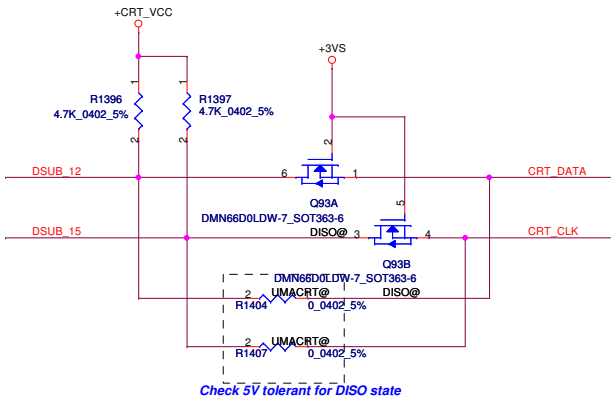
For UMA Only

13 GMCH_CRT_R	GMCH_CRT_R	R1393	UMACRT@	0_0402_5%	CRT_R
13 GMCH_CRT_G	GMCH_CRT_G	R1394	UMACRT@	0_0402_5%	CRT_G
13 GMCH_CRT_B	GMCH_CRT_B	R1395	UMACRT@	0_0402_5%	CRT_B
13,14 GMCH_CRT_HSYNC	GMCH_CRT_HSYNC	R1398	UMACRT@	0_0402_5%	CRT_HSYNC
13,14 GMCH_CRT_VSYNC	GMCH_CRT_VSYNC	R1399	UMACRT@	0_0402_5%	CRT_VSYNC
13 GMCH_CRT_DATA	GMCH_CRT_DATA	R1400	UMACRT@	0_0402_5%	CRT_DATA
13 GMCH_CRT_CLK	GMCH_CRT_CLK	R1401	UMACRT@	0_0402_5%	CRT_CLK

For VGA Only

16 VGA_CRT_R	VGA_CRT_R	R1402	DISO@	0_0402_5%	CRT_R
16 VGA_CRT_G	VGA_CRT_G	R1403	DISO@	0_0402_5%	CRT_G
16 VGA_CRT_B	VGA_CRT_B	R1405	DISO@	0_0402_5%	CRT_B
16 VGA_CRT_HSYNC	VGA_CRT_HSYNC	R1406	DISO@	0_0402_5%	CRT_HSYNC
16 VGA_CRT_VSYNC	VGA_CRT_VSYNC	R1408	DISO@	0_0402_5%	CRT_VSYNC
16 VGA_CRT_DATA	VGA_CRT_DATA	R1409	DISO@	0_0402_5%	CRT_DATA
16 VGA_CRT_CLK	VGA_CRT_CLK	R1410	DISO@	0_0402_5%	CRT_CLK

Close to Conn side



Check 5V tolerant for DISO state

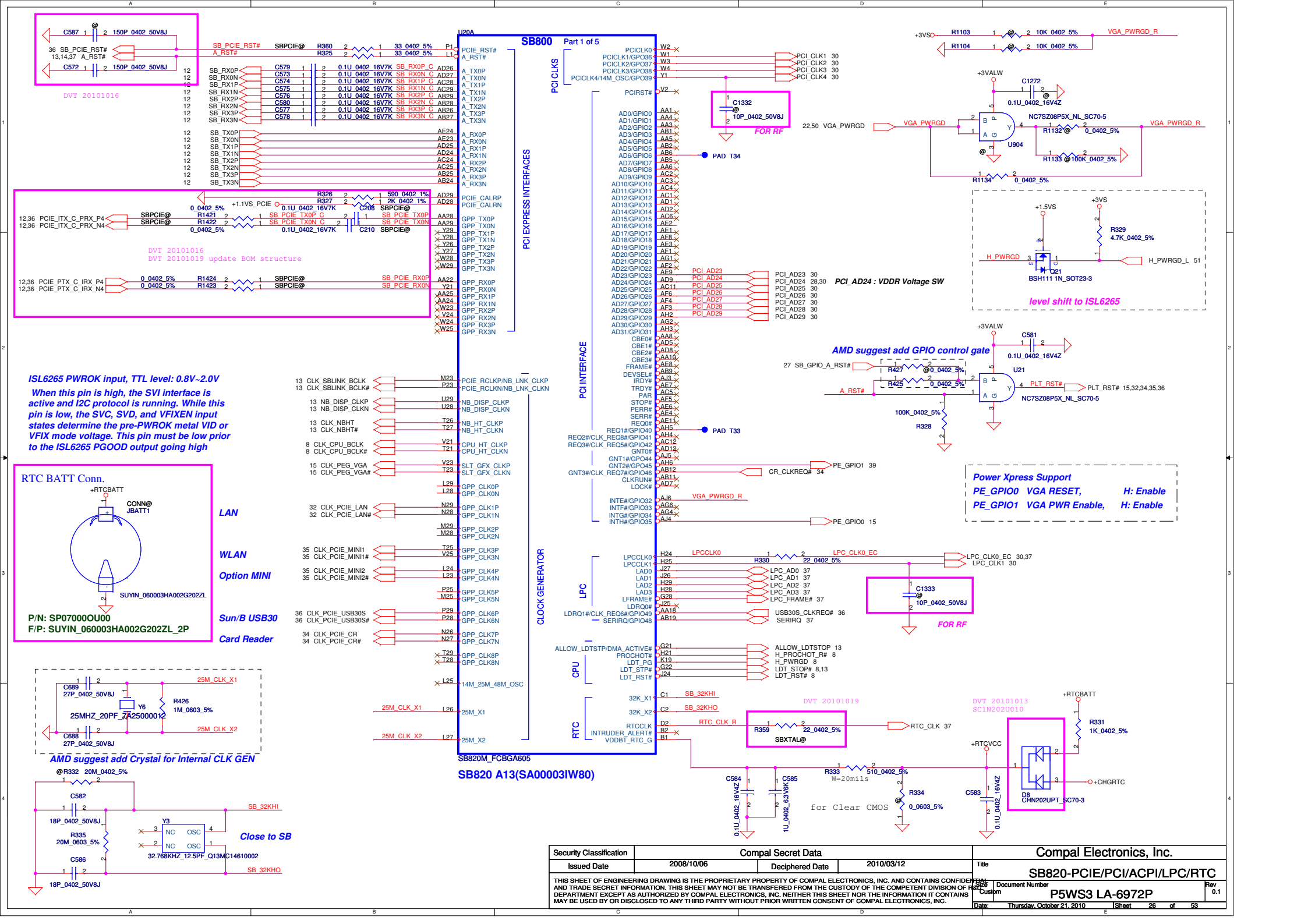
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

Compal Electronics, Inc.

Title: CRT Connector

Size: B | Document Number: P5WS3 LA-6972P | Rev: 0.1

Date: Thursday, October 21, 2010 | Sheet 25 of 53



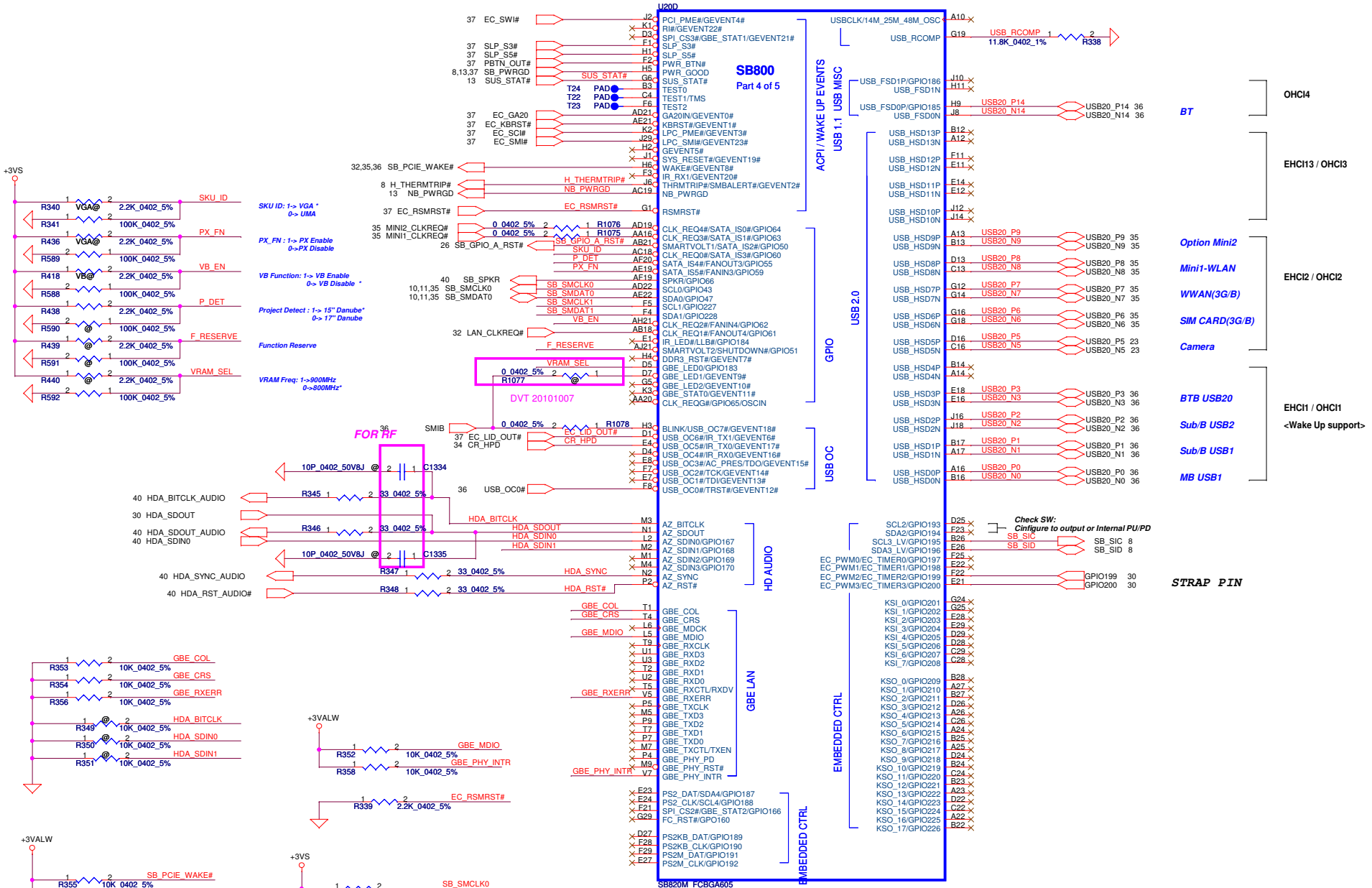
Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

Compal Electronics, Inc.

Title: SB820-PCIE/PCI/ACPI/LPC/RTC

Size: Custom | Document Number: P5WS3 LA-6972P | Rev: 0.1

Date: Thursday, October 21, 2010 | Sheet 26 of 53



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

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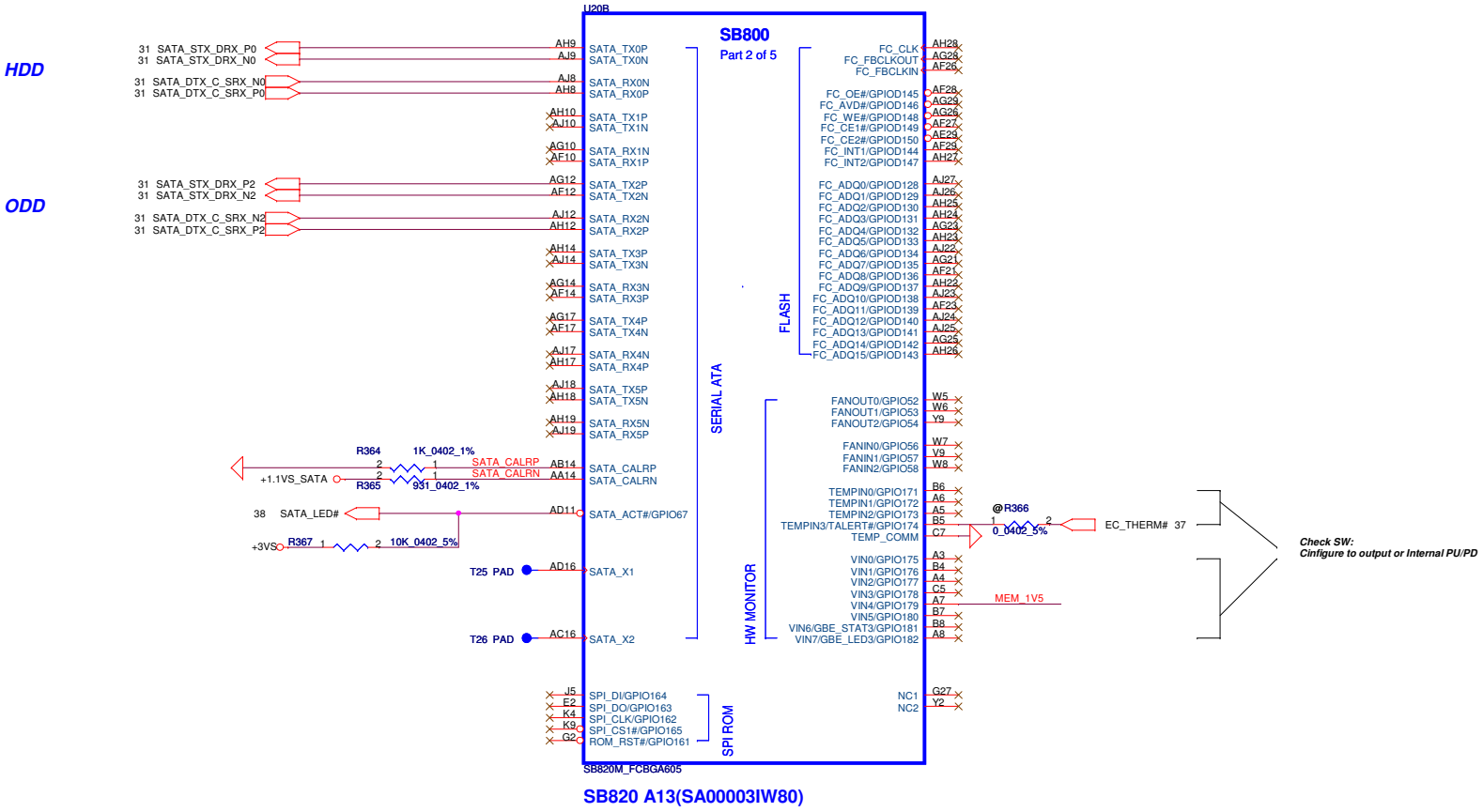
Compal Electronics, Inc.

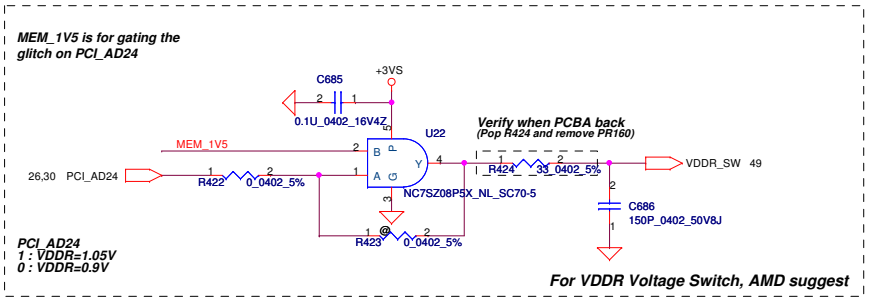
Title: SB820 USB/HD Audio

Size: Custom | Document Number: P5WS3 LA-6972P | Rev: 0.1

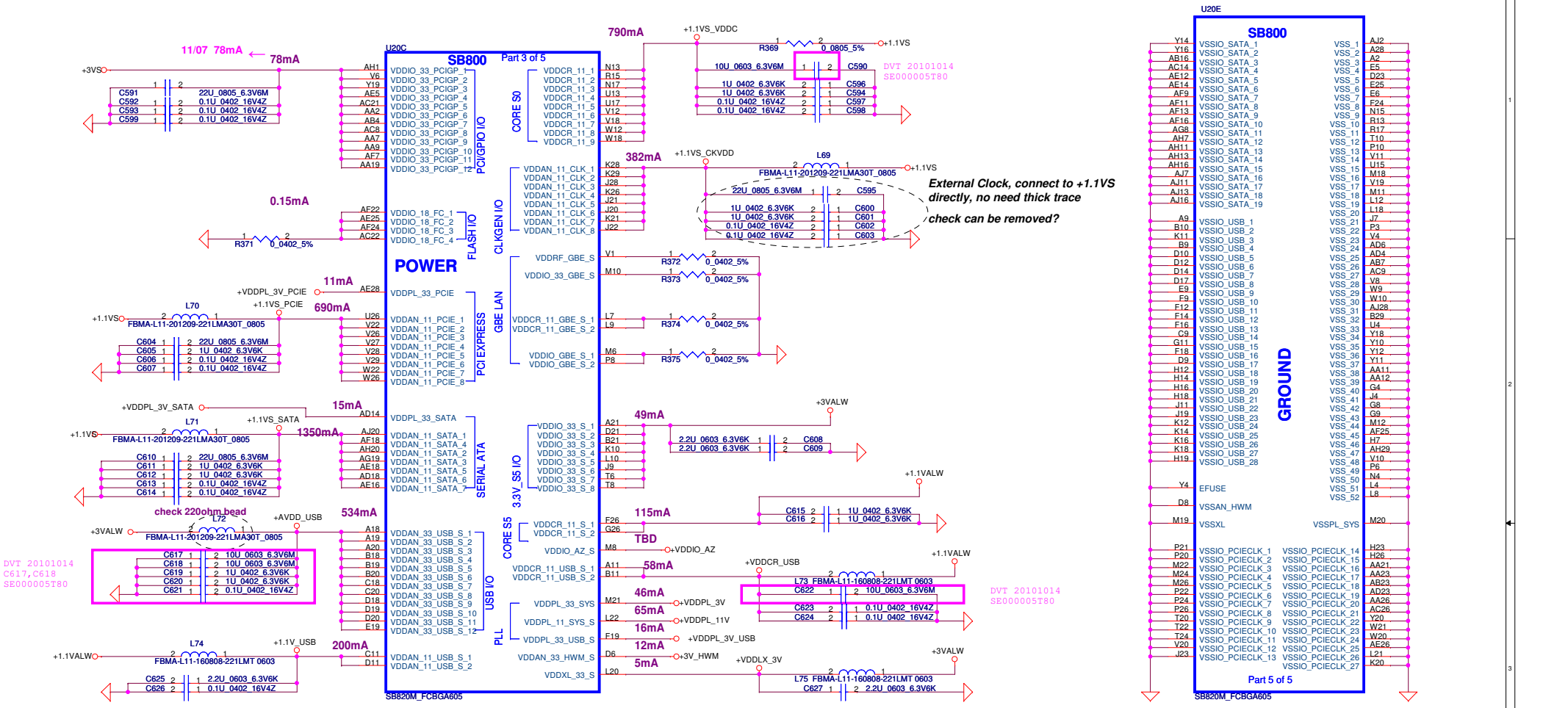
Date: Thursday, October 21, 2010 | Sheet 27 of 53

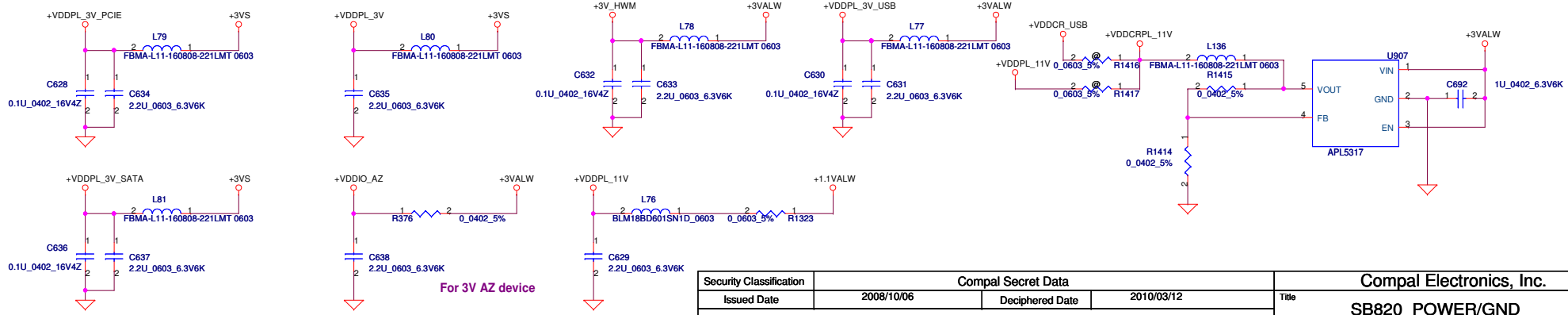


SB820 A13(SA00003IW80)



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/10/06	Deciphered Date 2010/03/12	Title: SB820 SATA/IDE/SPI
Size: Custom	Document Number: P5WS3 LA-6972P		Rev: 0.1
Date: Thursday, October 21, 2010	Sheet 28 of 53		





Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

Compal Electronics, Inc.

Title: SB820 POWER/GND

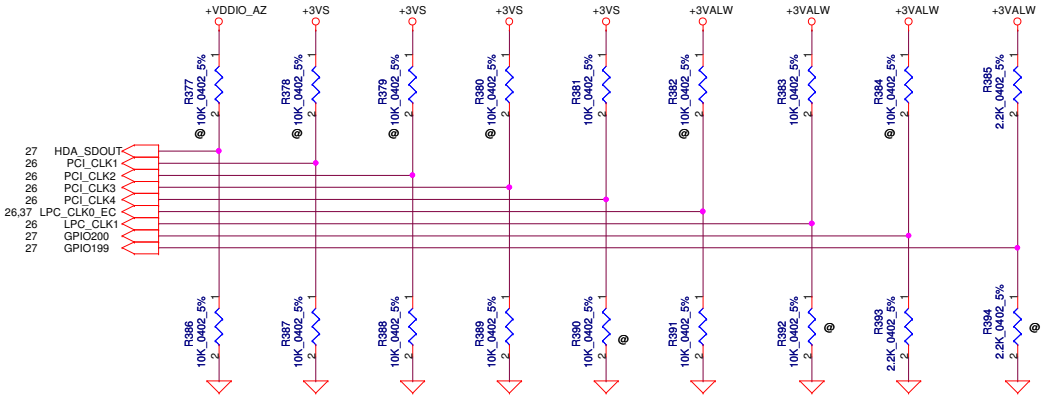
Size: Custom | Document Number: P5WS3 LA-6972P | Rev: 0.1

Date: Thursday, October 14, 2010 | Sheet 29 of 53

REQUIRED STRAPS

Check Internal PU/PD

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LCP_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	Inter CLK Gen Mode Enable DEFAULT	EC ENABLE	CLOCKGEN ENABLE DEFAULT	H,H = Reserved H,L = SPI ROM L,H = LPC ROM (Default L,NC) L,L = FWH ROM
PULL LOW	Performance MODE DEFAULT	FORCE PCIE GEN1 DEFAULT	WATCHDOG TIMER DISABLE DEFAULT	IGNORE DEBUG STRAP DEFAULT	Inter CLK Gen Mode Disable	EC DISABLE DEFAULT	CLOCKGEN DISABLE	



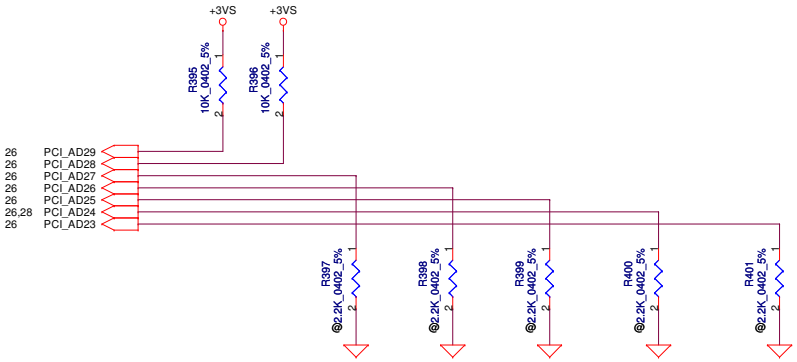
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

		PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH		USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW		BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

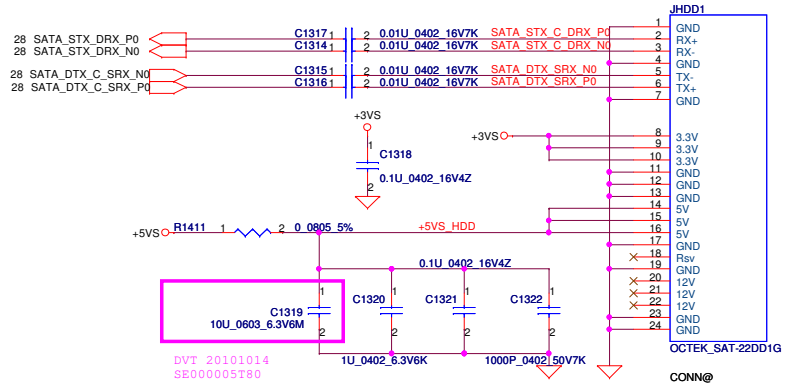
Check AD29,AD28 strap function

check default

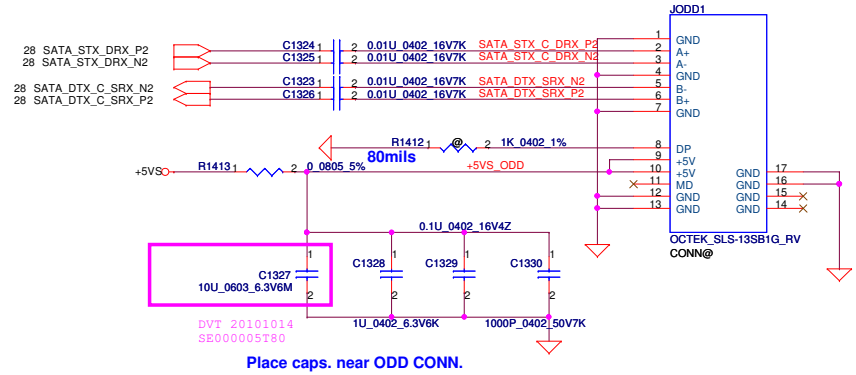


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/10/06	Deciphered Date 2010/03/12	Title: SB820 STRAPS
Size: Custom	Document Number: P5WS3 LA-6972P		Rev: 0.1
Date: Thursday, October 21, 2010	Sheet 30 of 53		

SATA HDD Conn.



SATA ODD Conn.



Place caps. near ODD CONN.

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2008/10/06	Deciphered Date	2010/03/12	Title	HDD & ODD Connector
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				Date: Thursday, October 21, 2010	Sheet 31 of 53

8151@	Populate when AR8151-BL1A
8152@	Populate when AR8152-AL1E

AR8151-BL1A PN:SA00003LE30
AR8152-AL1E PN:SA00003JW10

no overclocking
PD 5.1K

Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable ★	H
	H:SWR Switch mode regulator Select★ AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	--

Pin23 Function:
1.CLKREQ
2.AR8152L revA PH:

R1647 keep away other singal (25mil)

EPAD should be connected to GND by Vias, the number of vias at least 9 pcs

S IC AR8151-BL1A-RL QFN 40P E-LAN CTRL

close to pin13 close to pin31 close to pin6
close to pin19 close to pin34

close to Lan pin37 close to Lan pin24

close to Lan pin40

close to Pin 1

close to Lan pin9 close to Lan pin22 close to Lan pin16

DVT 20101019

Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2009/04/16

Compal Electronics, Inc.

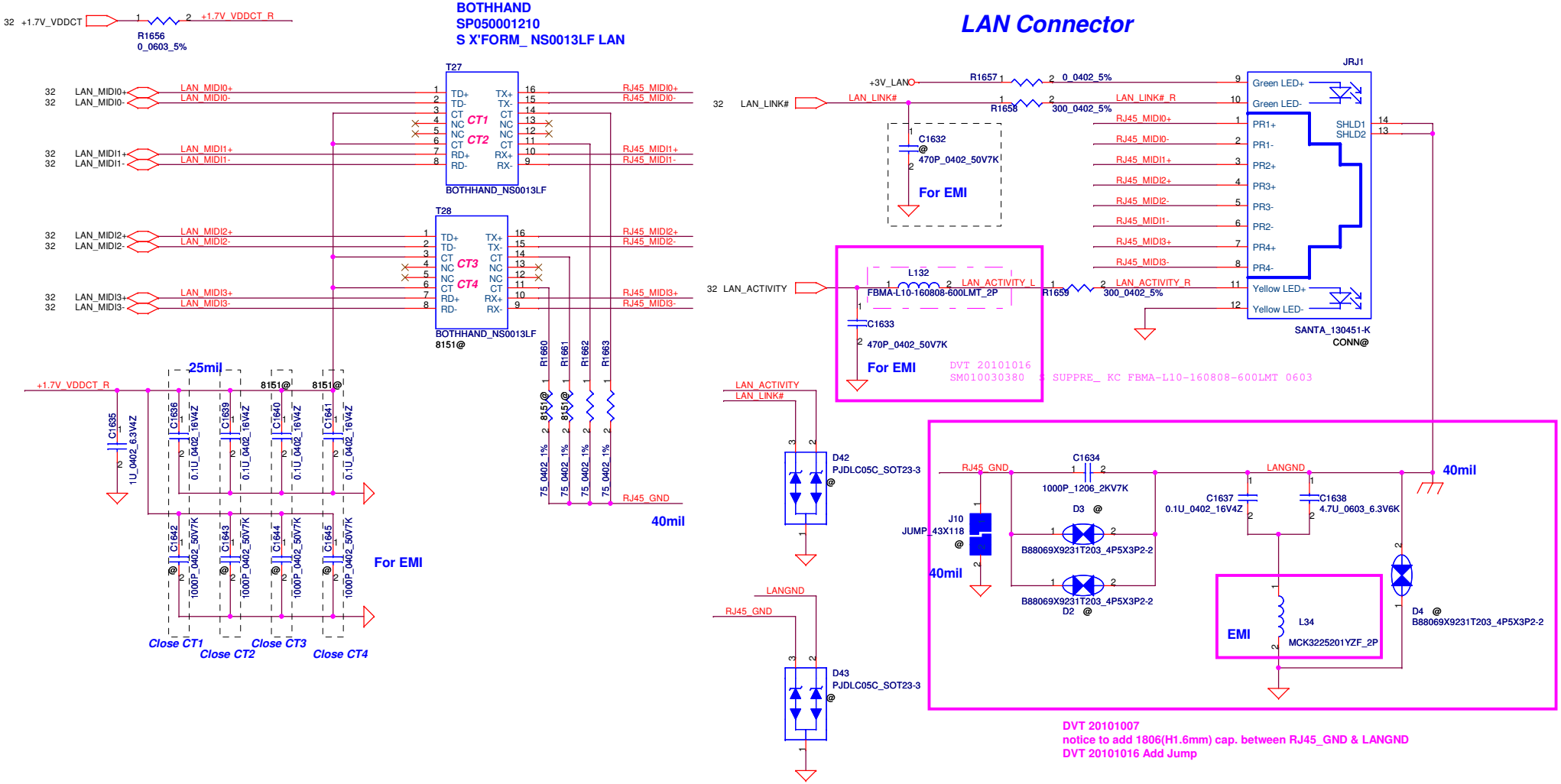
Title: LAN/B AR8151

Size: Custom | Document Number: P5WS3 LA-6972P | Rev: 0.1

Date: Thursday, October 21, 2010 | Sheet 32 of 53

LAN Connector

BOTHHAND
SP050001210
S X'FORM_ NS0013LF LAN



Security Classification	Compal Secret Data		
Issued Date	2010/08/06	Deciphered Date	2011/08/06

Compal Electronics, Inc.

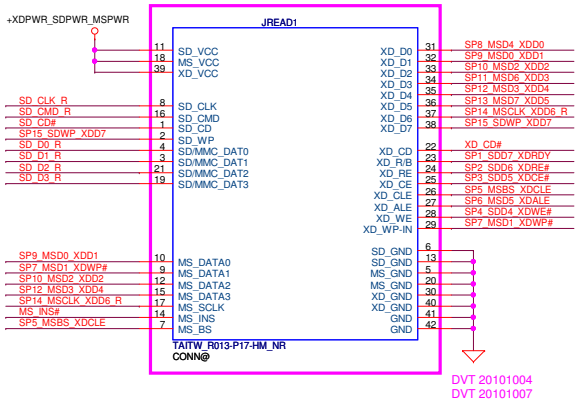
Title: LAN Magnetic & RJ45

Size	Document Number	Rev
Custom	P5WS3 LA-6972P	0.1

Date: Thursday, October 21, 2010 Sheet 33 of 53

Card Reader Connector

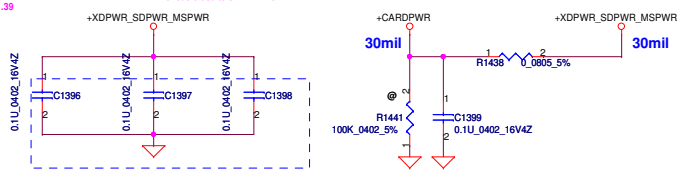
Card Reader Connector



DVT 20101004
DVT 20101007

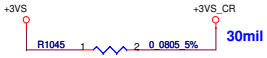
12/14 C1397 close to JREAD1.11
C1398 close to JREAD1.18

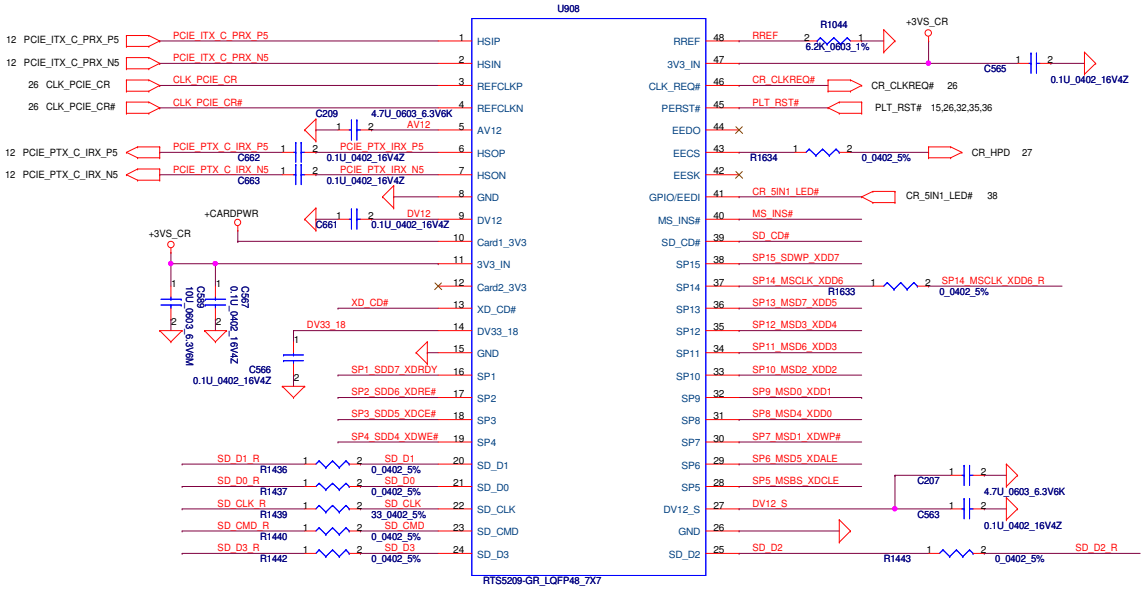
close to JREAD1.39



EMI(Close to Conn.)

RTS5209-GR





Security Classification	Compal Secret Data		
Issued Date	2007/08/28	Deciphered Date	2006/10/06

Compal Electronics, Inc.

Title: **PCIE CardReader&CONN**

Size	Document Number	Rev
Custom	P5WS3 LA-6972P	0.1

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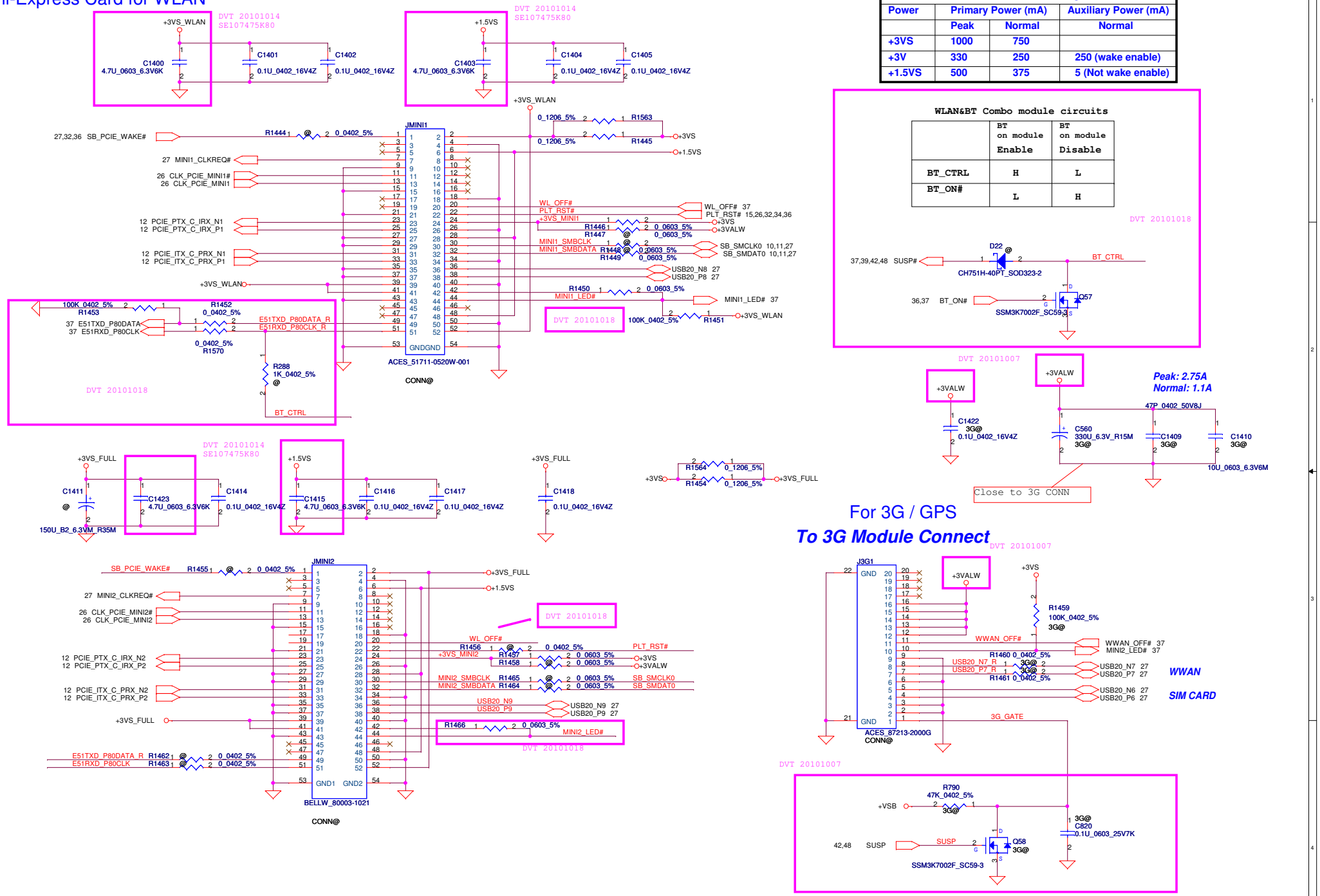
Mini-Express Card for WLAN

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

Compal Electronics, Inc.

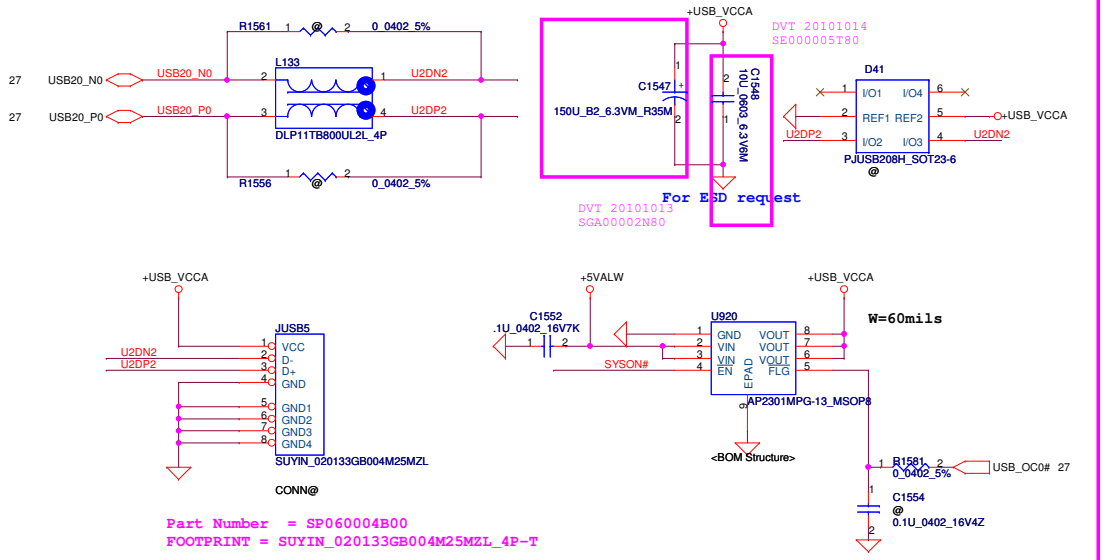
Title: MINI CARD (WLAN) / 3G BOARD

Size: B | Document Number: P5WS3 LA-6972P | Rev: 0.1

Date: Thursday, October 21, 2010 | Sheet 35 of 53

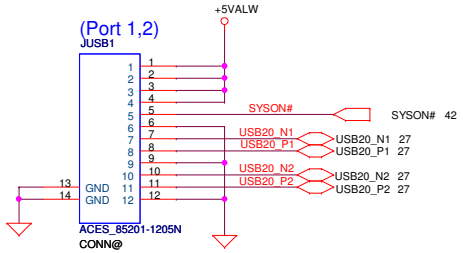
MB USB 2.0 and Conn.

For EMI request

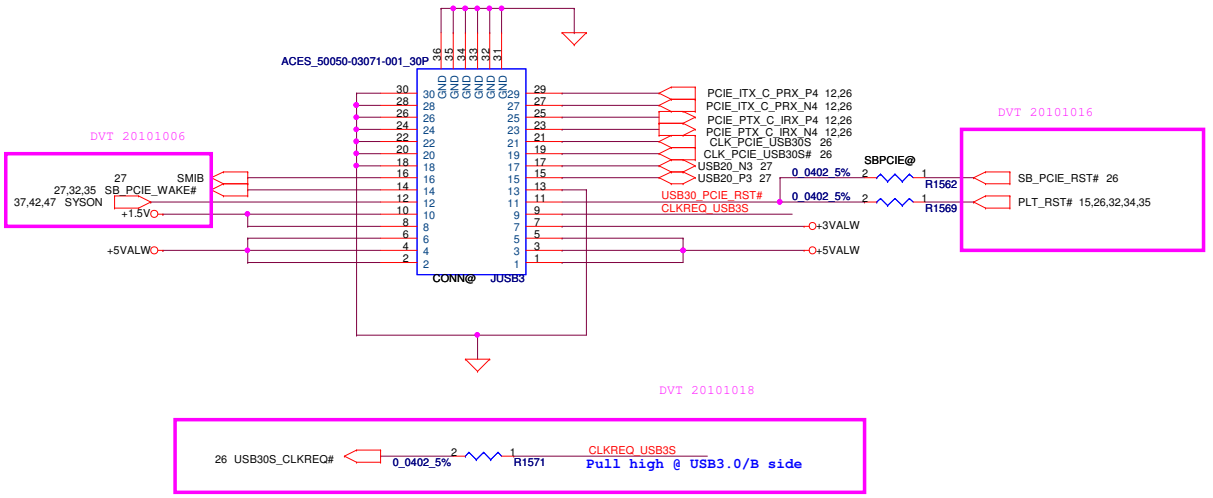


USB 2.0 and Conn

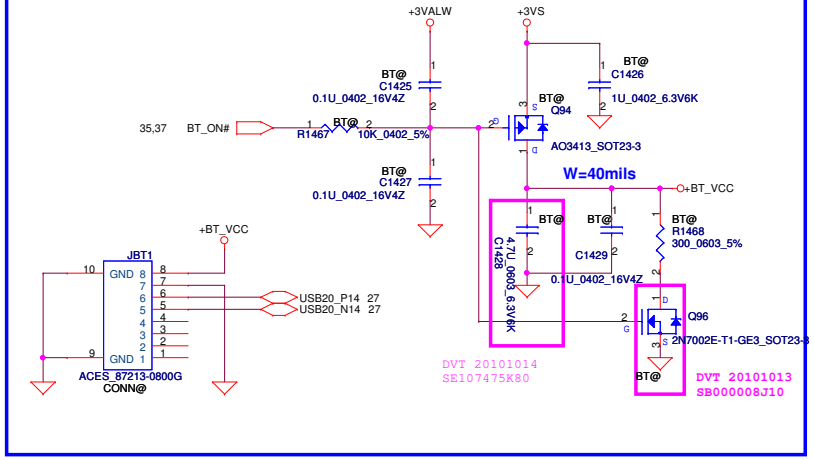
To USB/B Connector



USB3.0 Conn.

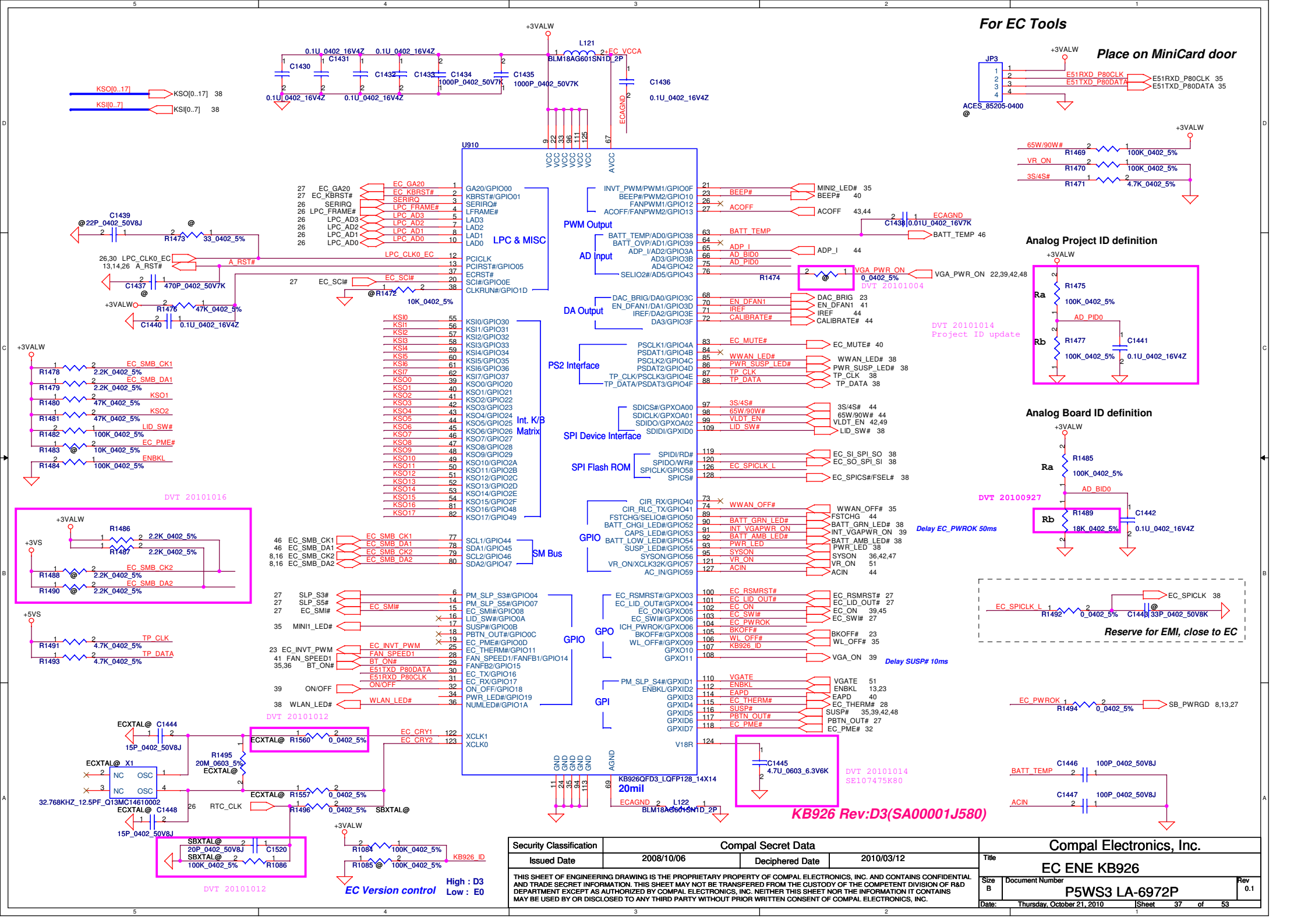


Bluetooth Conn.



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

Compal Electronics, Inc.	
Title	BlueTooth / USB BOARD
Size B	Document Number P5WS3 LA-6972P
Rev	0.1
Date: Thursday, October 21, 2010	Sheet 36 of 53


For EC Tools
Place on MiniCard door
U910
KB926QFD3_LQFP128_14X14
20mil
Int. K/B Matrix
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
SPI Device Interface
SPI Flash ROM
GPIO
GPO
GPI
SM Bus
Analog Project ID definition
Analog Board ID definition
DVT 20101004
DVT 20101014
Project ID update
DVT 20100927
Delay EC_PWROK 50ms
Delay SUSP# 10ms
Reserve for EMI, close to EC
DVT 20101016
DVT 20101012
DVT 20101014
SE107475K80
KB926 Rev:D3(SA00001J580)
EC Version control
High : D3
Low : E0
Security Classification
Compal Secret Data
Issued Date
2008/10/06
Deciphered Date
2010/03/12
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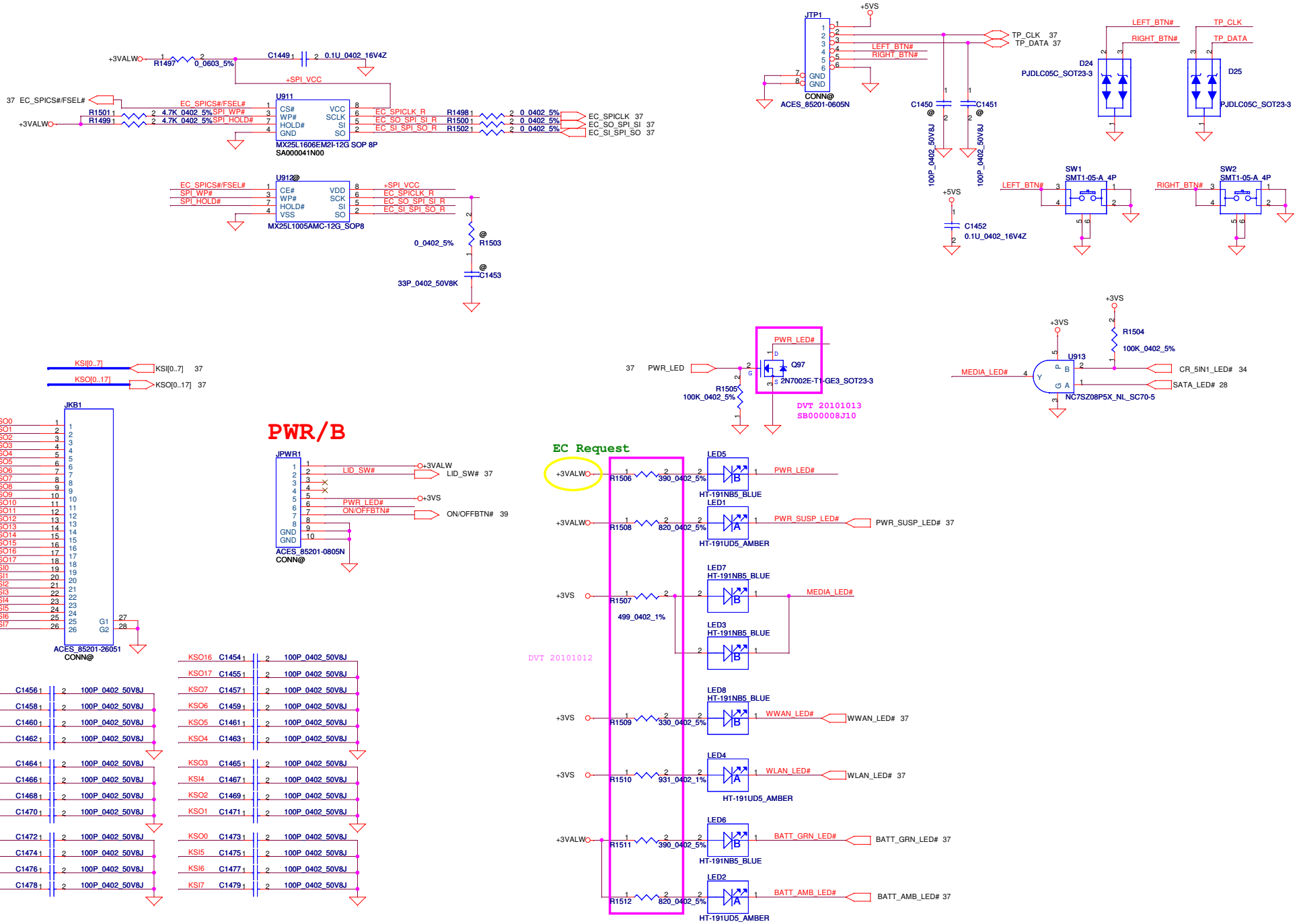
Compal Electronics, Inc.
Title
EC ENE KB926
Size
B
Document Number
P5WS3 LA-6972P
Rev
0.1
Date:
Thursday, October 21, 2010
Sheet
37
of
53



Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

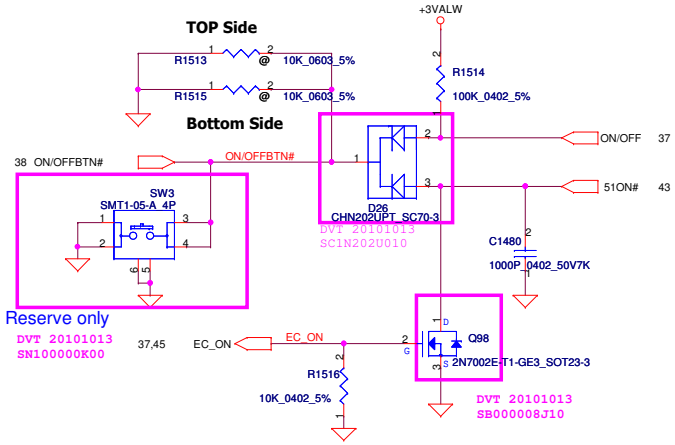
Compal Electronics, Inc.

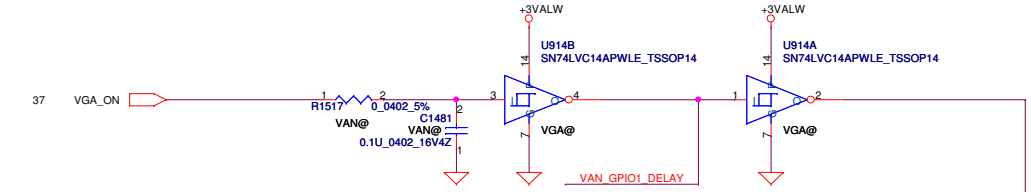
Title: BIOS,LED,I/O Port & K/B Connector

Size: B | Document Number: P5WS3 LA-6972P | Rev: 0.1

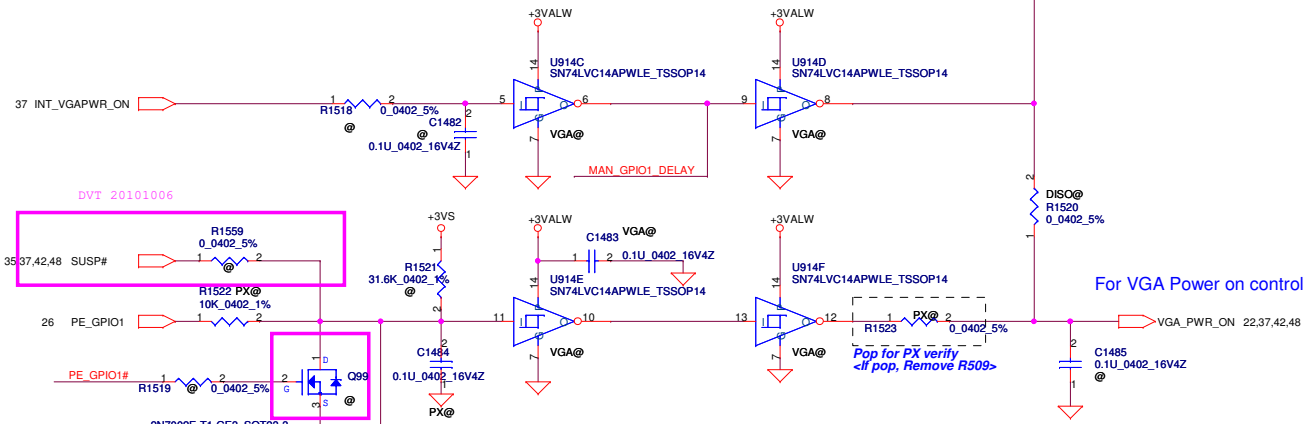
Date: Thursday, October 21, 2010 | Sheet 38 of 53

ON/OFF switch **Power Button**

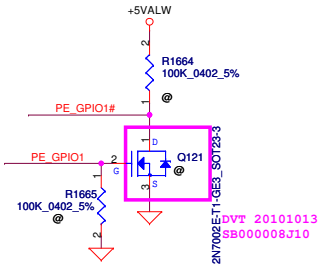




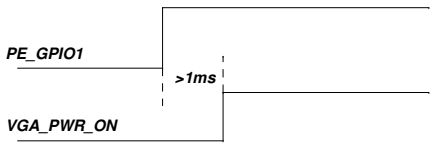
VGA Power ON Circuit



For VGA Power on control



For PX sequence, >1mS delay is required between PE_GPIO1 and VGA_PWR_ON



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2008/10/06	Deciphered Date	2010/03/12	Title: PBTN / VGA SEQUENCE
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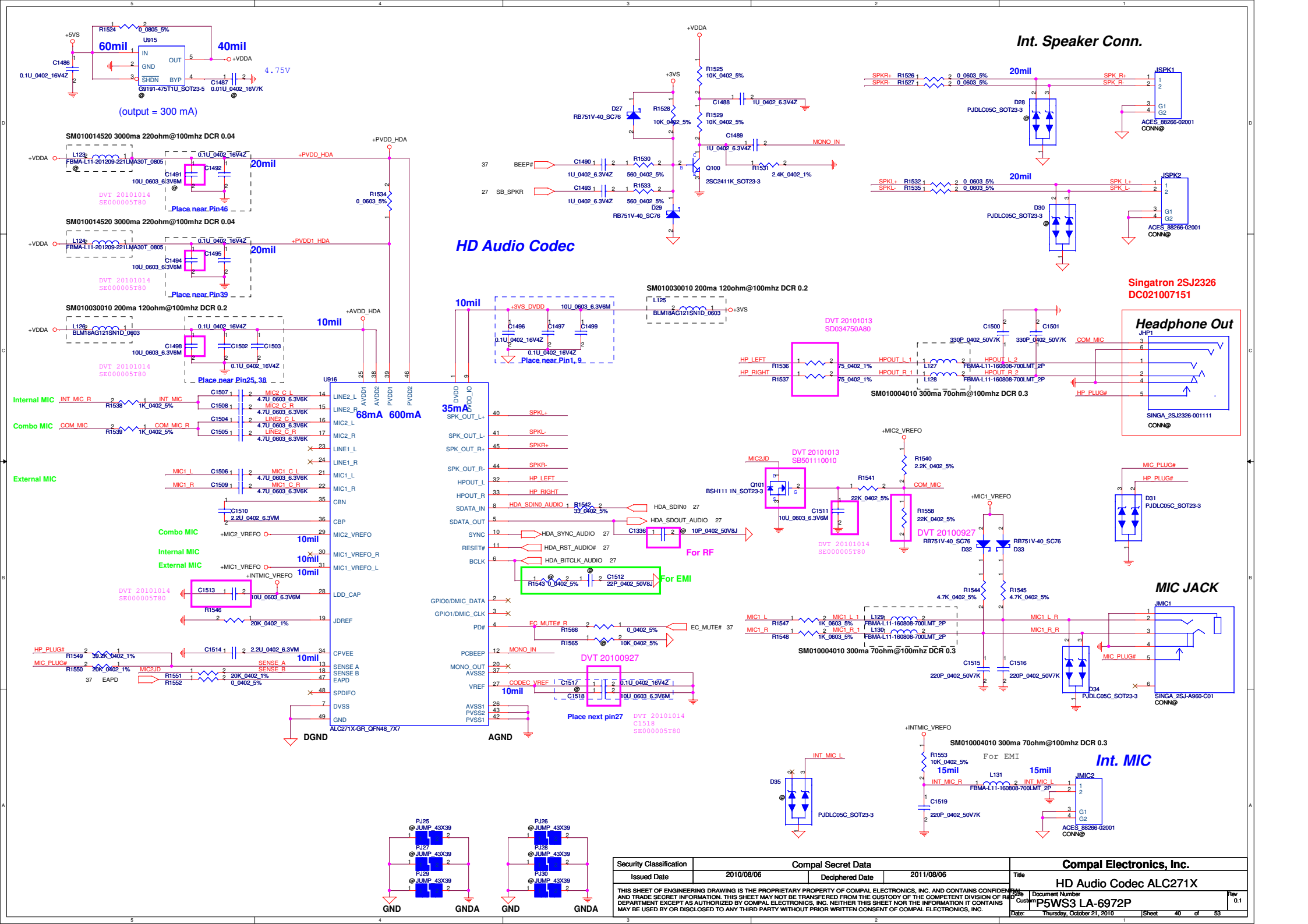
				Date: Thursday, October 21, 2010; Sheet 39 of 53



Security Classification	Compal Secret Data		
Issued Date	2010/08/06	Deciphered Date	2011/08/06

Compal Electronics, Inc.

Title: HD Audio Codec ALC271X

Size: Custom | Document Number: P5WS3 LA-6972P | Rev: 0.1

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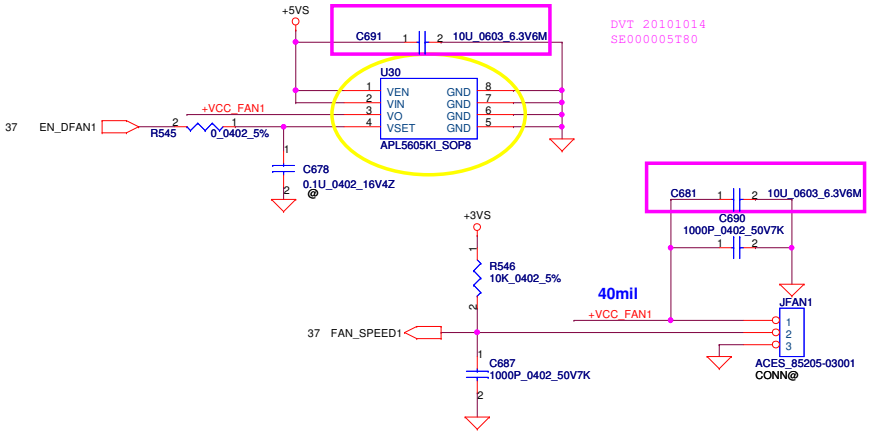
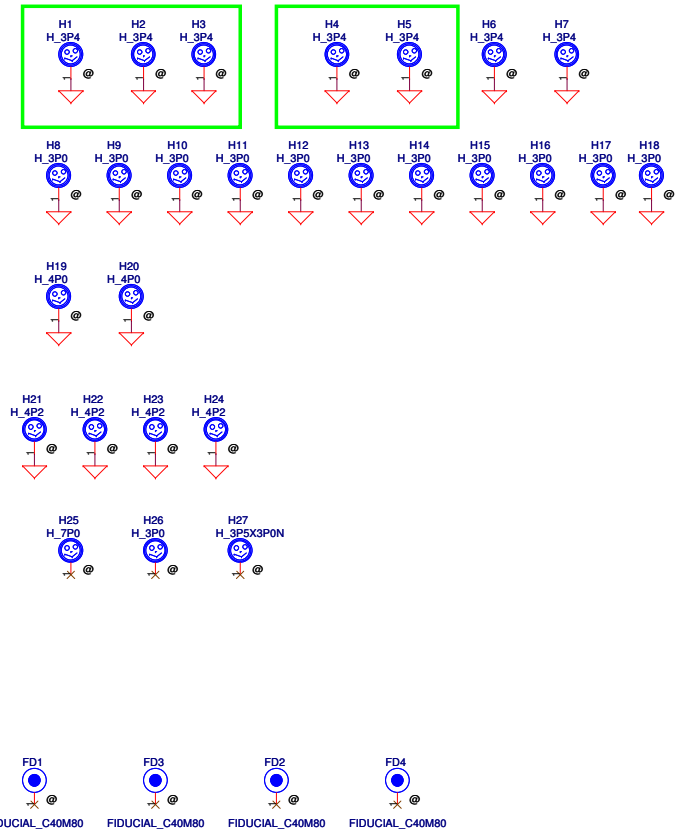
FAN1 Conn



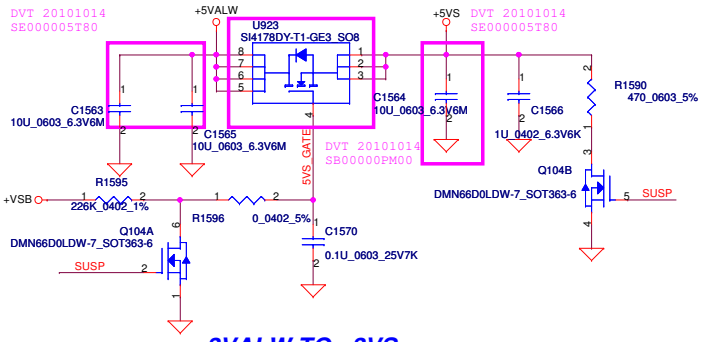
FAN Stand-Off

JUSB3 Stand-Off

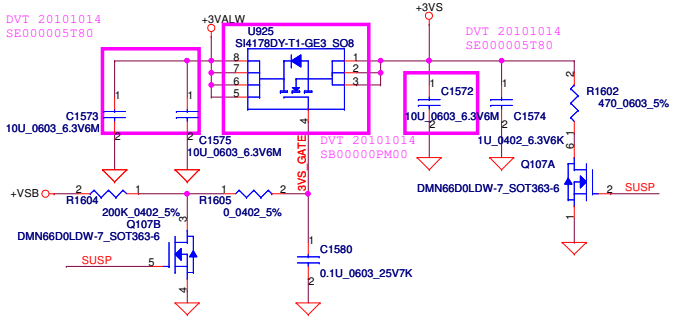


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/10/06	Deciphered Date	2010/03/12
Title	FAN & Screw Hole		
Size B	Document Number P5WS3 LA-6972P		Rev 0.1
Date: Thursday, October 21, 2010	Sheet 41 of 53		

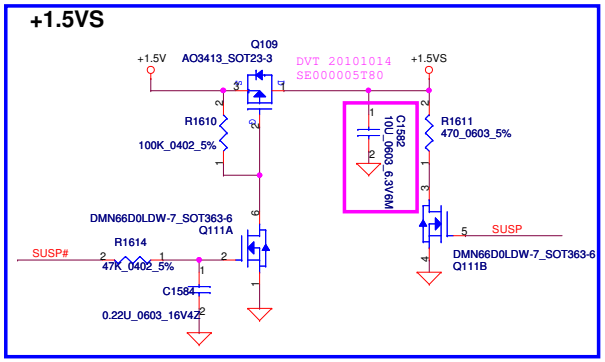
+5VALW TO +5VS



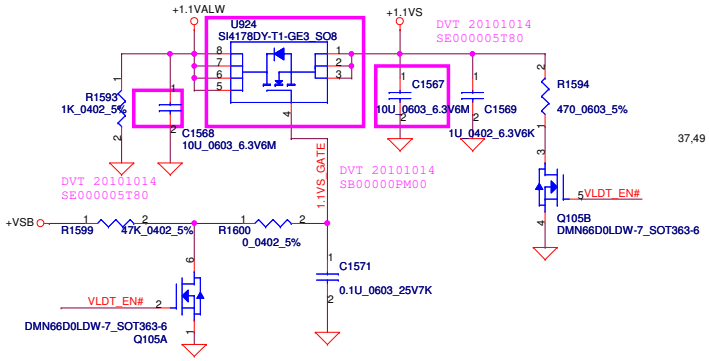
+3VALW TO +3VS



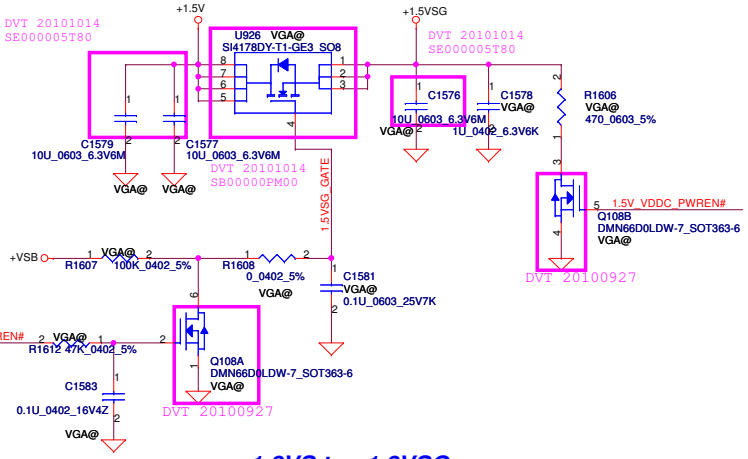
+1.5VS



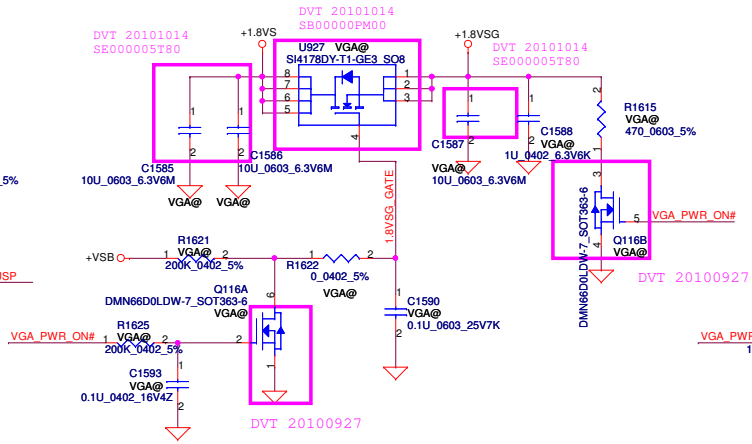
+1.1VALW TO +1.1VS



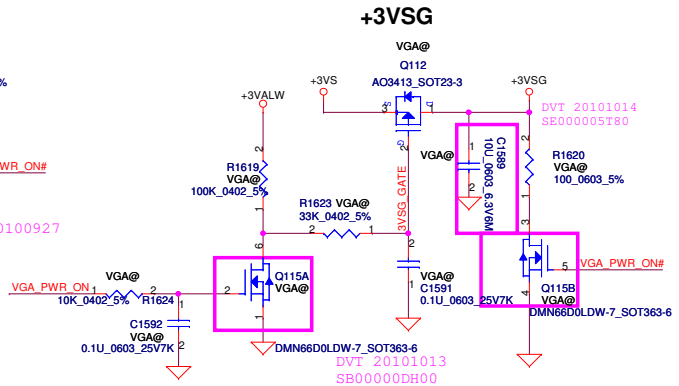
+1.5V to +1.5VSG

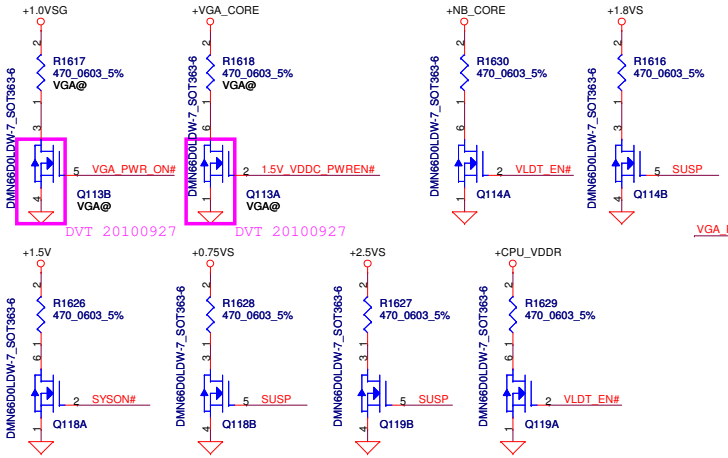


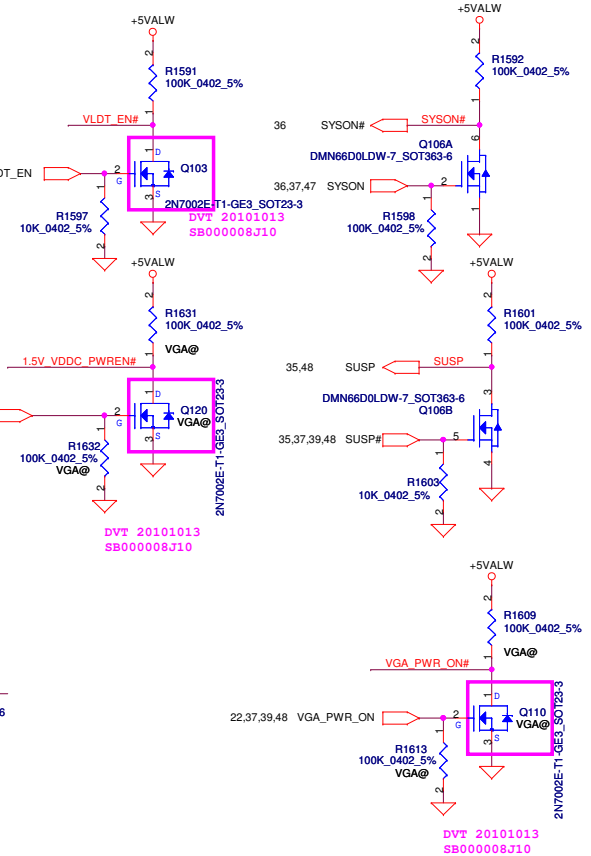
+1.8VS to +1.8VSG



+3VSG







Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

Compal Electronics, Inc.

Title: DC Interface

Size: B | Document Number: P5WS3 LA-6972P | Rev: 0.1

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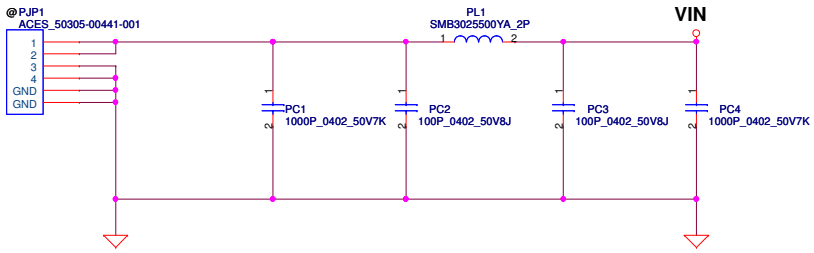
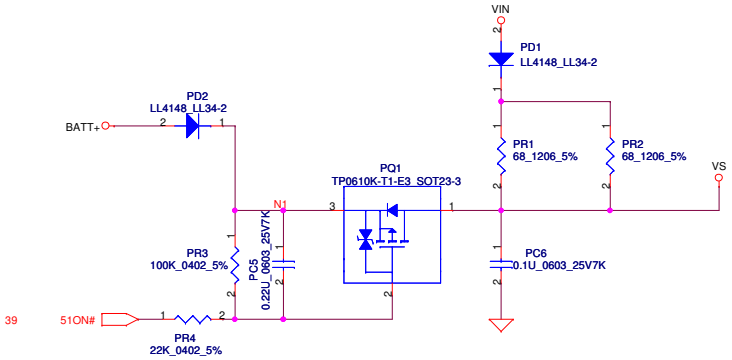
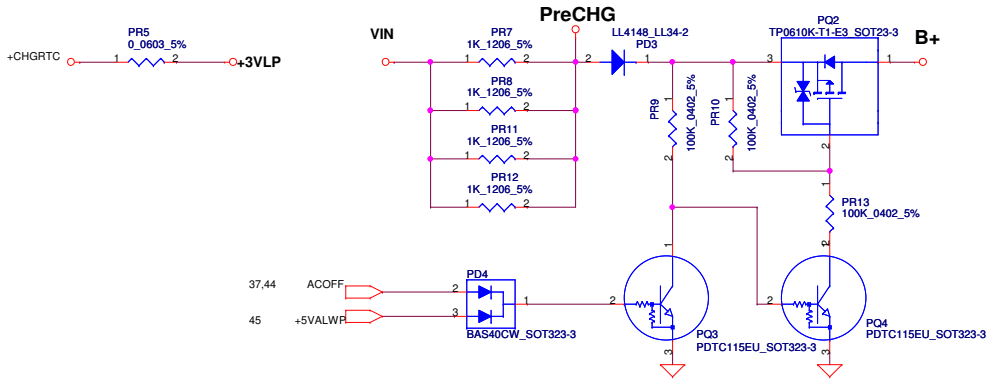
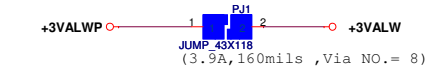
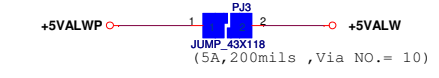
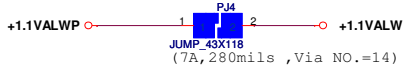


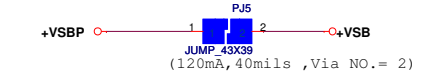


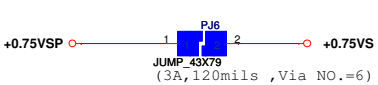


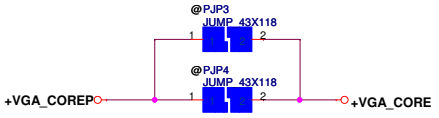


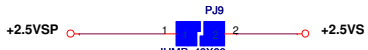


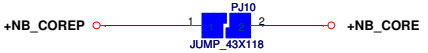


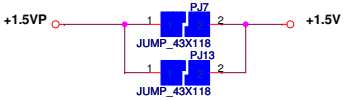


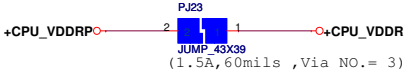












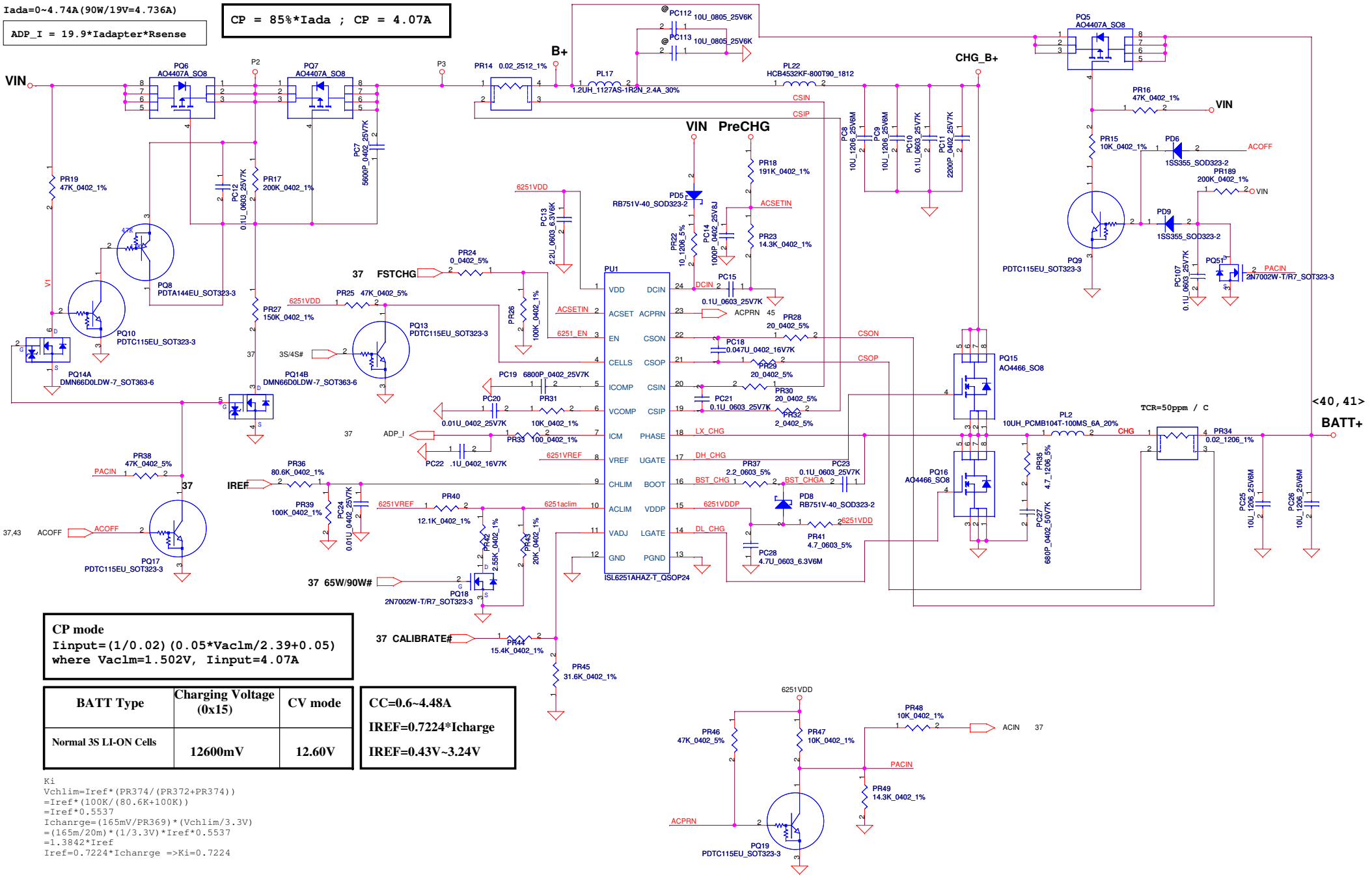
Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Thursday, October 21, 2010 | Sheet 43 of 53



Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: PWR-CHARGER

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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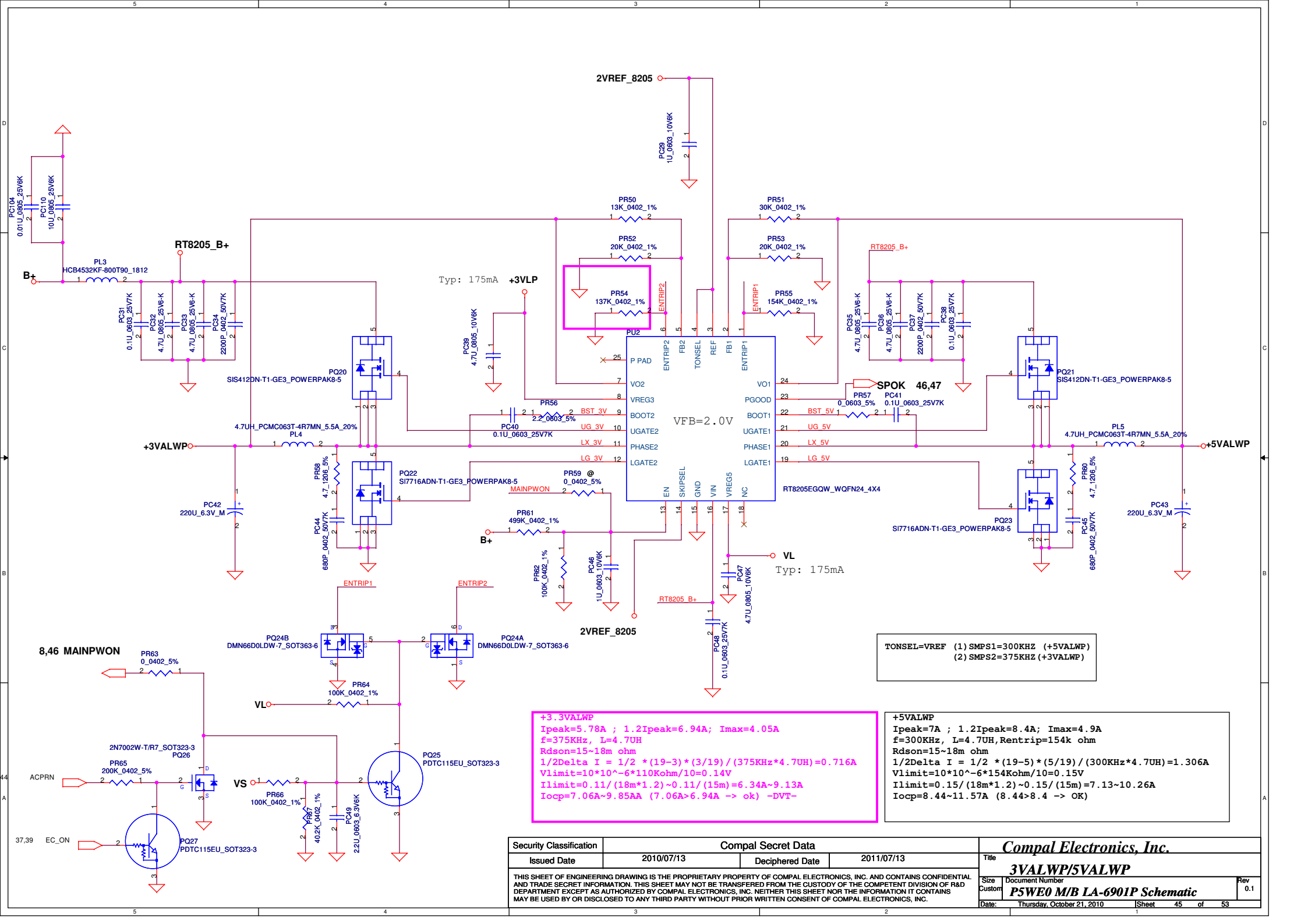
2VREF_8205
PC29 1U_0603_10V6K
PR50 13K_0402_1%
PR51 30K_0402_1%
PR52 20K_0402_1%
PR53 20K_0402_1%
PR54 137K_0402_1%
PR55 154K_0402_1%
PC104 0.01U_0805_25V6K
PC110 10U_0805_25V6K
PL3 HCB4532KF-800T90_1812
B+
RT8205_B+
Typ: 175mA +3VLP
PC39 4.7U_0805_10V6K
PU2
P PAD
VO2
VREG3
BOOT2
UGATE2
PHASE2
LGATE2
ENTRIP2
FB2
TONSEL
REF
FB1
ENTRIP1
VO1
PGOOD
BOOT1
UGATE1
PHASE1
LGATE1
EN
SKIPSEL
GND
VIN
VREG5
NC
VFB=2.0V
RT8205EGQW_WQFN24_4X4
PC31 0.1U_0603_25V7K
PC32 4.7U_0805_25V6-K
PC33 4.7U_0805_25V6-K
PC34 220P_0402_50V7K
PC35 4.7U_0805_25V6-K
PC36 4.7U_0805_25V6-K
PC37 220P_0402_50V7K
PC38 0.1U_0603_25V7K
PQ20 SIS412DN-T1-GE3_POWERPAK8-5
PQ21 SIS412DN-T1-GE3_POWERPAK8-5
PQ22 SI7716ADN-T1-GE3_POWERPAK8-5
PQ23 SI7716ADN-T1-GE3_POWERPAK8-5
SPOK 46,47
PR57 0_0603_5%
PC41 0.1U_0603_25V7K
PR56 2.2_0603_5%
PC40 0.1U_0603_25V7K
BST_3V
UG_3V
LX_3V
LG_3V
BST_5V
UG_5V
LX_5V
LG_5V
4.7UH_PCMC063T-4R7MN_5.5A_20%
PL4
PL5
+3VALWP
+5VALWP
PR58 4.7_1206_5%
PR60 4.7_1206_5%
PC42 220U_6.3V_M
PC43 220U_6.3V_M
PC44 680P_0402_50V7K
PC45 680P_0402_50V7K
PR59 @ 0_0402_5%
MAINPWON
PR61 499K_0402_1%
PR62 100K_0402_1%
PC46 1U_0603_10V6K
VL
Typ: 175mA
PC47 4.7U_0805_10V6K
PC48 0.1U_0603_25V7K
ENTRIP1
ENTRIP2
PQ24B DMN66D0LDW-7_SOT363-6
PQ24A DMN66D0LDW-7_SOT363-6
8,46 MAINPWON
PR63 0_0402_5%
PR64 100K_0402_1%
2N7002W-T/R7_SOT323-3
PQ26
PR65 200K_0402_5%
ACPRN
VS
PR66 100K_0402_1%
PR67 40.2K_0402_1%
PC49 2.2U_0603_6.3V6K
PQ25 PDTC115EU_SOT323-3
37,39 EC_ON
PQ27 PDTC115EU_SOT323-3
TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)
(2)SMPS2=375KHZ(+3VALWP)
+3.3VALWP
Ipeak=5.78A ; 1.2Ipeak=6.94A; Imax=4.05A
f=375KHz, L=4.7UH
Rdson=15~18m ohm
1/2Delta I = 1/2 *(19-3)*(3/19)/(375KHz*4.7UH)=0.716A
Vlimit=10*10^-6*110Kohm/10=0.14V
Ilimit=0.11/(18m*1.2)~0.11/(15m)=6.34A~9.13A
Iocp=7.06A~9.85AA (7.06A>6.94A -> ok) -DVT-
+5VALWP
Ipeak=7A ; 1.2Ipeak=8.4A; Imax=4.9A
f=300KHz, L=4.7UH,Rentrip=154k ohm
Rdson=15~18m ohm
1/2Delta I = 1/2 *(19-5)*(5/19)/(300KHz*4.7UH)=1.306A
Vlimit=10*10^-6*154Kohm/10=0.15V
Ilimit=0.15/(18m*1.2)~0.15/(15m)=7.13~10.26A
Iocp=8.44~11.57A (8.44>8.4 -> OK)
Security Classification
Compal Secret Data
Issued Date
2010/07/13
Deciphered Date
2011/07/13
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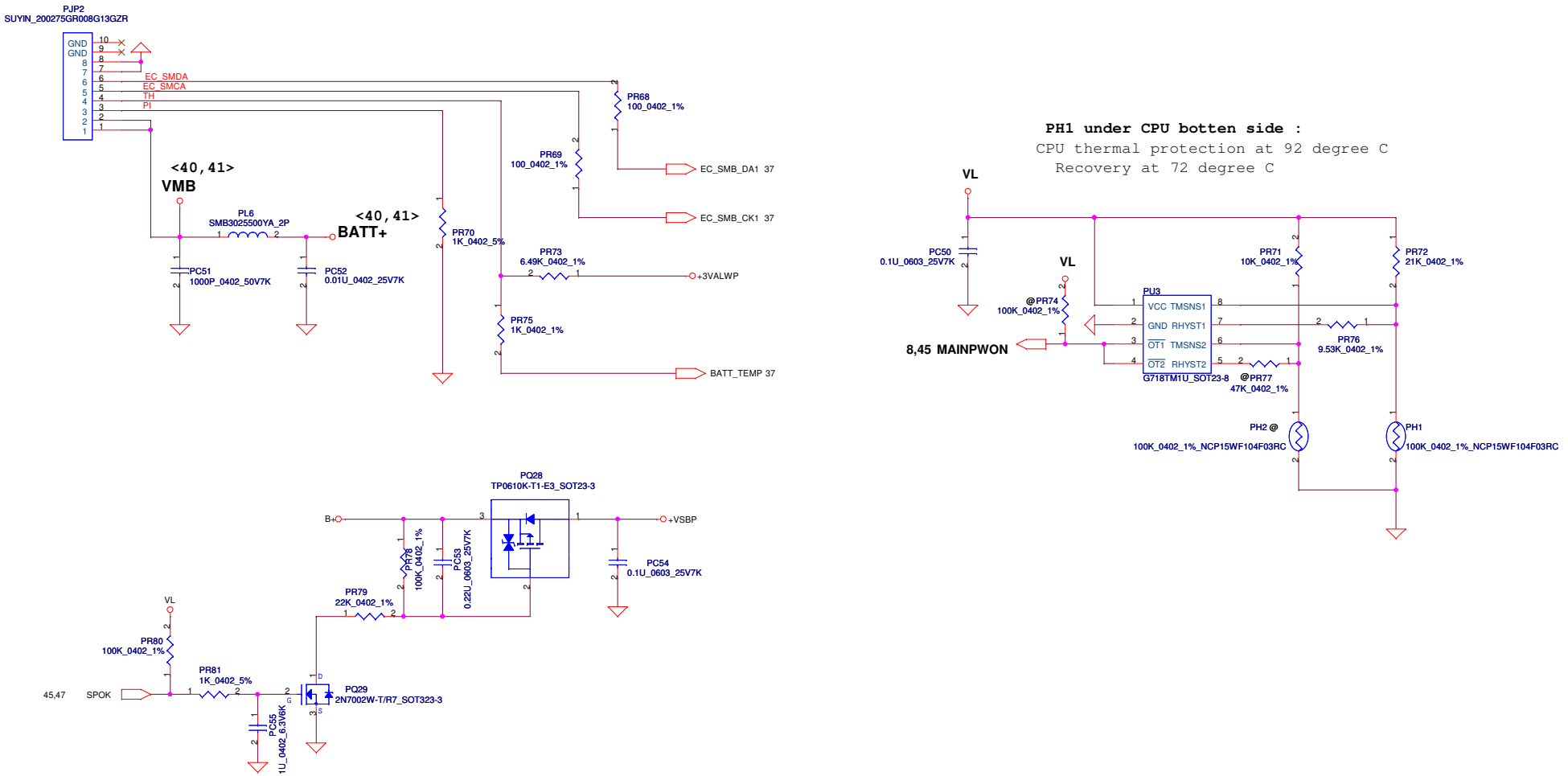
Compal Electronics, Inc.
Title
3VALWP/5VALWP
Size
Custom
Document Number
P5WE0 M/B LA-6901P Schematic
Rev
0.1
Date:
Thursday, October 21, 2010
Sheet
45
of
53



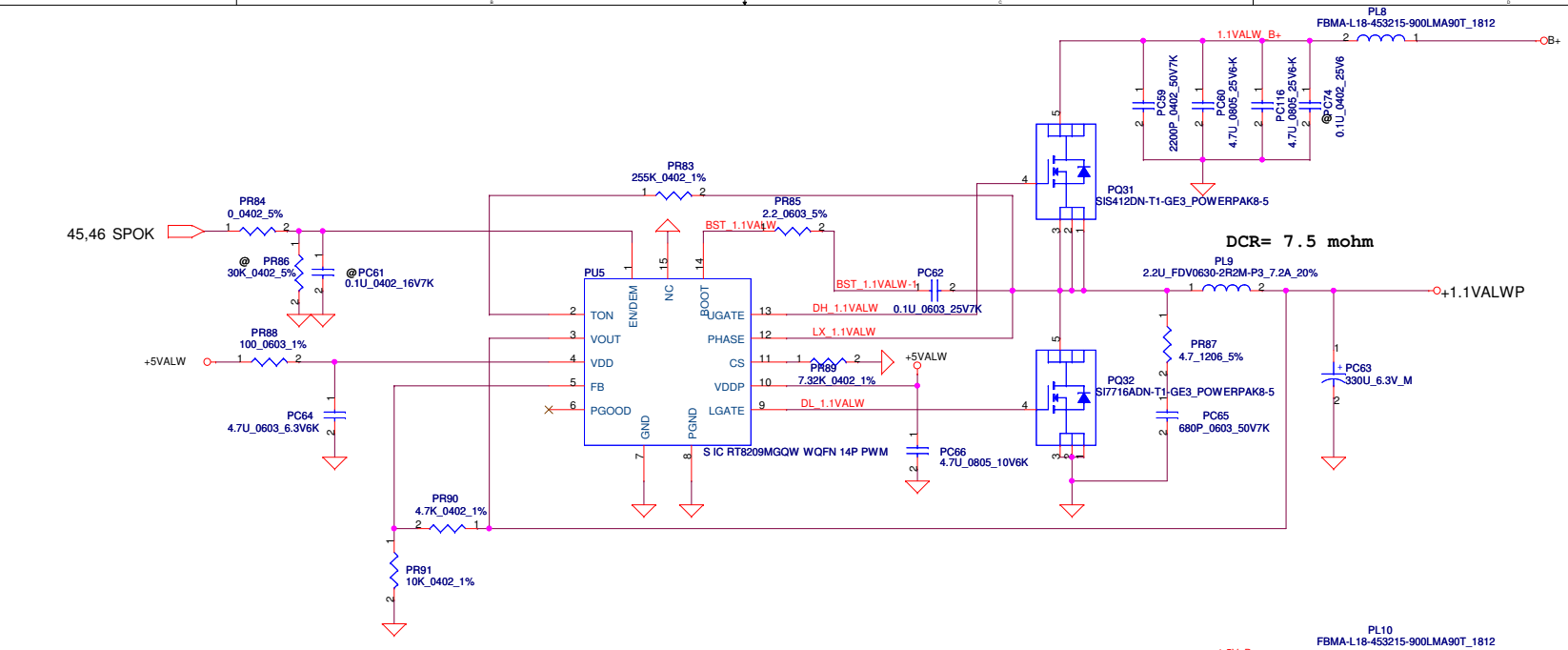
PH1 under CPU botten side :

CPU thermal protection at 92 degree C

Recovery at 72 degree C

Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.			
Title	PWR-BATTERY CONN/OTP		
Size: Custom	Document Number: P5WE0 M/B LA-6901P Schematic		Rev: 0.1
Date: Thursday, October 21, 2010	Sheet 46 of 53		



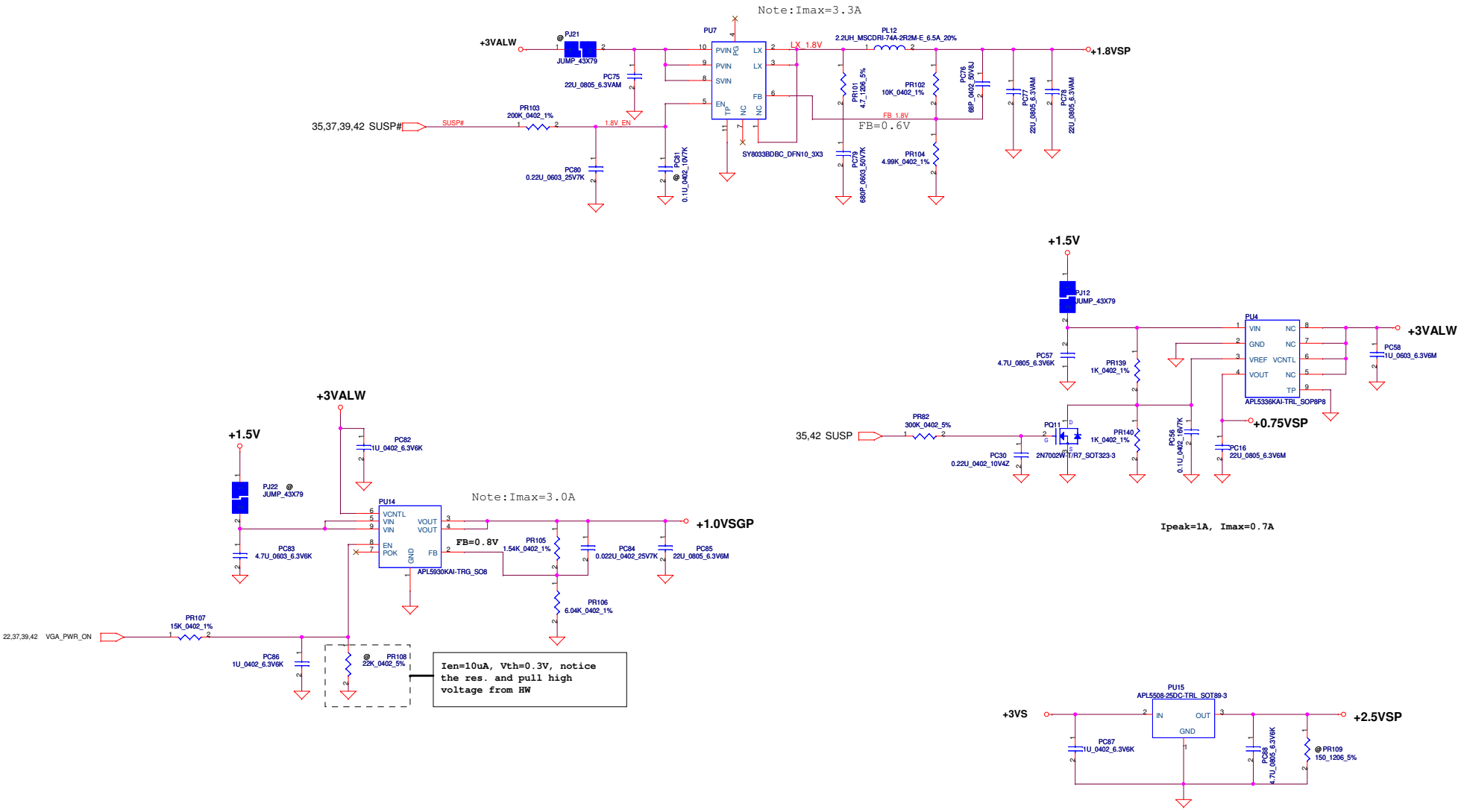
<UMA>Cout ESR=15m ohm Rdson(max)=11.5 mohm Rdson(typ)=9 mohm.
Ipeak=10A, Imax=7A, Iocp=12A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=4.1A
=>1/2Delta I=2.05A
Iocp=10A~14.8A

<DIS>Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=13.8A, Imax=9.7A, Iocp=16.6A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=4.1A
=>1/2Delta I=2.05A
Iocp=10A~17.8A

	G5603	RT8209B	TPS51117	RT8209M
Temperature Compensated	-1180ppm/℃	1600ppm/℃	4500ppm/℃	4800ppm/℃
Vtrip_min (SPEC)	30mV	50mV	30mV	50mV
Vtrip_max (SPEC)	200mV	200mV	200mV	200mV

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/12

Compal Electronics, Inc.	
Title	1.1VALWP/1.5VP
Size: Custom	Document Number: P7WE0 LA-xxxxP
Rev	0.1
Date: Thursday, October 21, 2010	Sheet 47 of 53



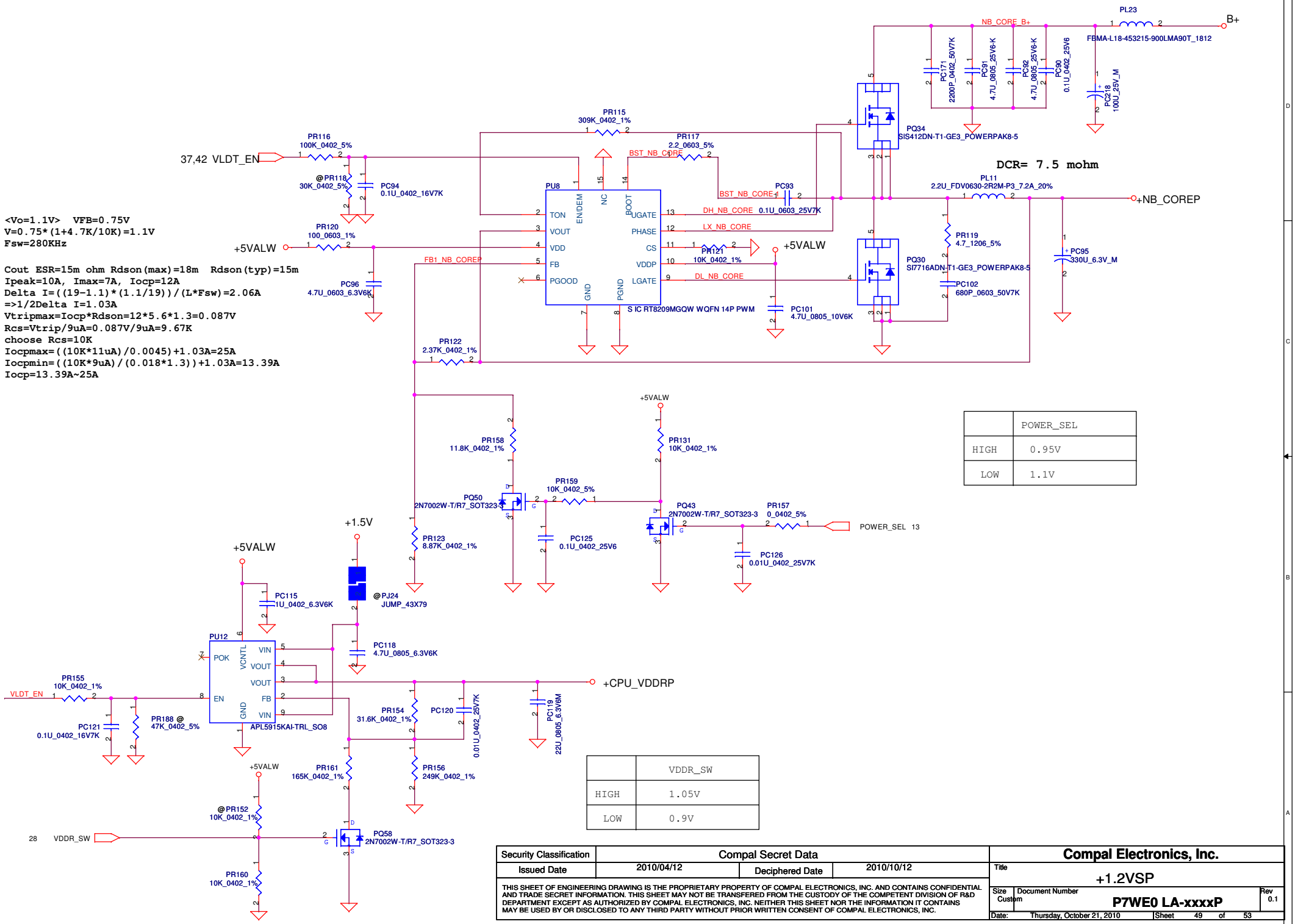
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: +1.8VSGP/+1.0VSGP/+2.5VSP/+0.75V

Size	Document Number	Rev
C		0.1

Date: Thursday, October 21, 2010 | Sheet 48 of 53


<Vo=1.1V> VFB=0.75V
V=0.75*(1+4.7K/10K)=1.1V
Fsw=280KHz
Cout ESR=15m ohm Rdson(max)=18m Rdson(typ)=15m
Ipeak=10A, Imax=7A, Iocp=12A
Delta I=((19-1.1)*(1.1/19))/(L*Fsw)=2.06A
=>1/2Delta I=1.03A
Vtripmax=Iocp*Rdson=12*5.6*1.3=0.087V
Rcs=Vtrip/9uA=0.087V/9uA=9.67K
choose Rcs=10K
Iocpmax=((10K*11uA)/0.0045)+1.03A=25A
Iocpmin=((10K*9uA)/(0.018*1.3))+1.03A=13.39A
Iocp=13.39A~25A
DCR= 7.5 mohm
37,42 VLDT_EN
+5VALW
+1.5V
+CPU_VDDRP
+NB_COREP
B+
NB_CORE_B+
POWER_SEL 13
28 VDDR_SW
PU8
PU12
PQ34 SIS412DN-T1-GE3_POWERPAK8-5
PQ30 SI7716ADN-T1-GE3_POWERPAK8-5
PQ50 2N7002W-T/R7_SOT323-3
PQ43 2N7002W-T/R7_SOT323-3
PQ58 2N7002W-T/R7_SOT323-3
S IC RT8209MGQW WQFN 14P PWM
APL5915KAI-TRL_SO8
PL23 FBMA-L18-453215-900LMA90T_1812
PL11 2.2U_FDV0630-2R2M-P3_7.2A_20%
PR115 309K_0402_1%
PR116 100K_0402_5%
PR117 2.2_0603_5%
PR118 @ 30K_0402_5%
PR119 4.7_1206_5%
PR120 100_0603_1%
PR121 10K_0402_1%
PR122 2.37K_0402_1%
PR123 8.87K_0402_1%
PR131 10K_0402_1%
PR154 31.6K_0402_1%
PR155 10K_0402_1%
PR156 249K_0402_1%
PR157 0_0402_5%
PR158 11.8K_0402_1%
PR159 10K_0402_5%
PR160 10K_0402_1%
PR161 165K_0402_1%
PR188 @ 47K_0402_5%
PC90 0.1U_0402_25V6
PC91 4.7U_0805_25V6-K
PC92 4.7U_0805_25V6-K
PC93 0.1U_0603_25V7K
PC94 0.1U_0402_16V7K
PC95 330U_6.3V_M
PC96 4.7U_0603_6.3V6K
PC101 4.7U_0805_10V6K
PC102 680P_0603_50V7K
PC115 1U_0402_6.3V6K
PC118 4.7U_0805_6.3V6K
PC119 22U_0805_6.3V6M
PC120 0.01U_0402_25V7K
PC121 0.1U_0402_16V7K
PC125 0.1U_0402_25V6
PC126 0.01U_0402_25V7K
PC171 2200P_0402_50V7K
PC218 100U_25V_M
@PJ24 JUMP_43X79
@PR152 10K_0402_1%
DH_NB_CORE
LX_NB_CORE
DL_NB_CORE
BST_NB_CORE
FB1_NB_COREP
TON
VOUT
VDD
FB
PGOOD
EN/DEM
NC
BOOT
UGATE
PHASE
CS
VDDP
LGATE
GND
PGND
POK
VCNTL
VIN
EN
FB
VLDT_EN
POWER_SEL
HIGH 0.95V
LOW 1.1V
VDDR_SW
HIGH 1.05V
LOW 0.9V
Security Classification Compal Secret Data
Issued Date 2010/04/12
Deciphered Date 2010/10/12
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Compal Electronics, Inc.
Title +1.2VSP
Size Custom
Document Number P7WE0 LA-xxxxP
Rev 0.1
Date: Thursday, October 21, 2010
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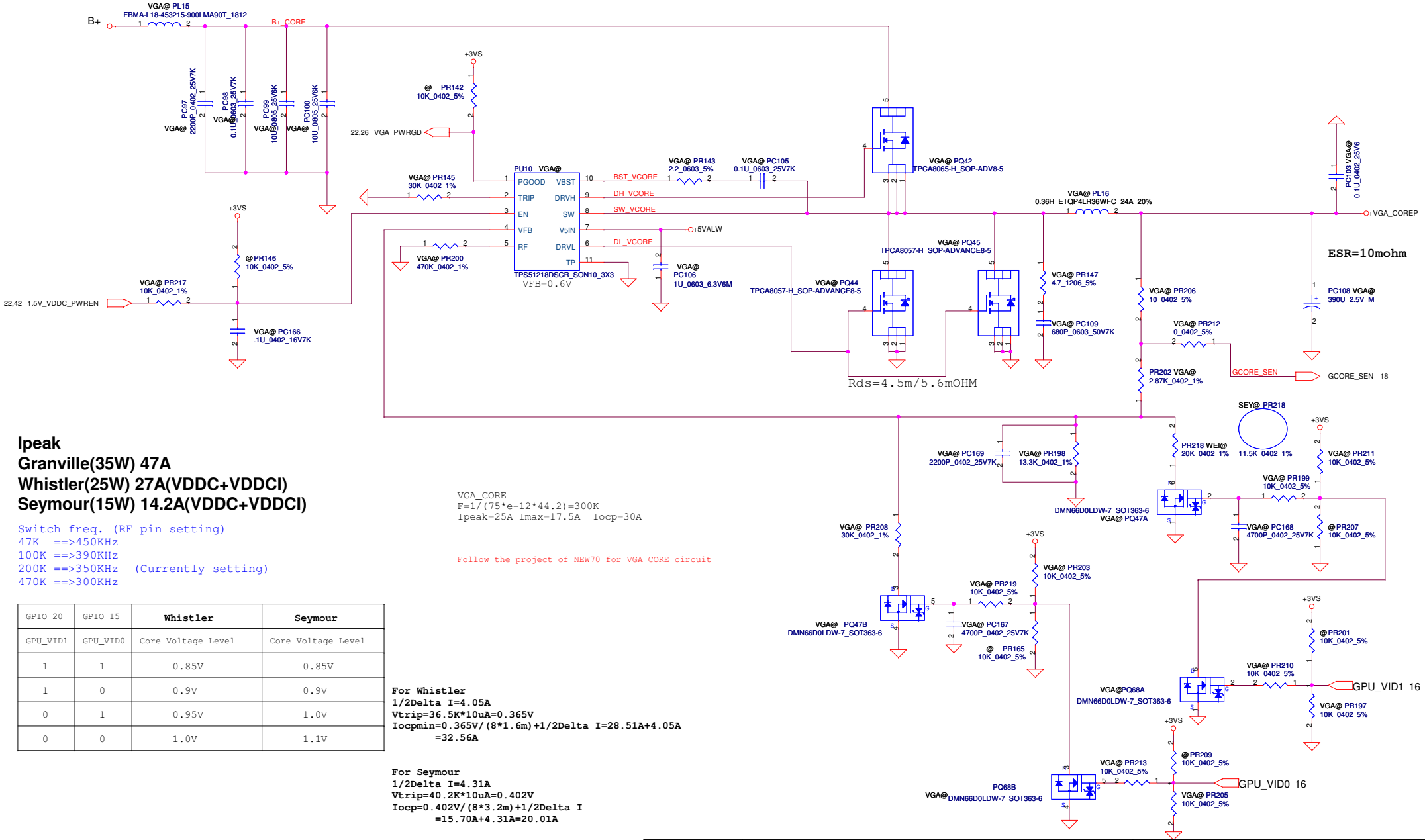


Ipeak
Granville(35W) 47A
Whistler(25W) 27A(VDDC+VDDCI)
Seymour(15W) 14.2A(VDDC+VDDCI)

Switch freq. (RF pin setting)
47K ==>450KHz
100K ==>390KHz
200K ==>350KHz (Currently setting)
470K ==>300KHz

GPIO 20	GPIO 15	Whistler	Seymour
GPU_VID1	GPU_VID0	Core Voltage Level	Core Voltage Level
1	1	0.85V	0.85V
1	0	0.9V	0.9V
0	1	0.95V	1.0V
0	0	1.0V	1.1V

VGA_CORE
F=1/(75*e-12*44.2)=300K
Ipeak=25A Imax=17.5A Iocp=30A

Follow the project of NEW70 for VGA_CORE circuit

For Whistler
1/2Delta I=4.05A
Vtrip=36.5K*10uA=0.365V
Iocpmin=0.365V/(8*1.6m)+1/2Delta I=28.51A+4.05A
=32.56A

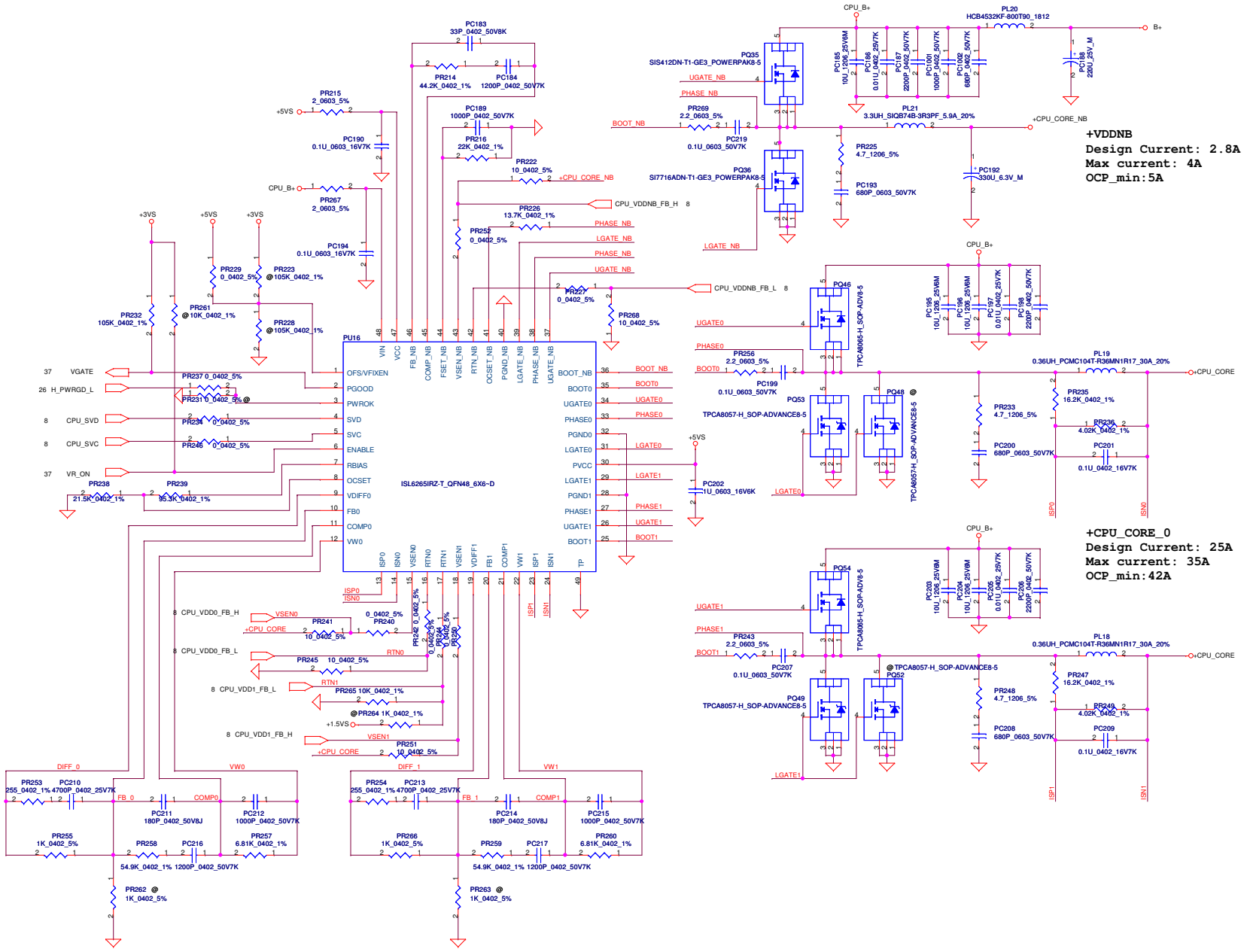
For Seymour
1/2Delta I=4.31A
Vtrip=40.2K*10uA=0.402V
Iocp=0.402V/(8*3.2m)+1/2Delta I
=15.70A+4.31A=20.01A

Security Classification	Compal Secret Data		AP
Issued Date	2010/07/13	Deciphered Date	2011/07/13

Compal Electronics, Inc.

Title: **+VGA_COREP**

Size	Document Number	Rev
Custom	P5WE0	0.1
Date: Thursday, October 21, 2010	Sheet 50 of 53	



Security Classification	Compal Secret Data		
Issued Date	2008/04/16	Deciphered Date	2010/03/12

Compal Electronics, Inc.			
Title: +CPU_CORE			
Size: Custom	Document Number: NELA5		Rev: 1.0
Date: Thursday, October 21, 2010	Sheet 51 of 53		

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: PEW96 LA-6552P | Rev: 0.1

Date: Thursday, October 21, 2010 | Sheet 52 of 53

PHASE	PAGE	MODIFICATION LIST	PURPOSE
DVT	P.22	Change C1105 PN,and set R650 with BACO@	Change C1105 from SE000001120 to SE00000I10
	P.40	Add 22k PD resistor(R1558),unstuff C1518	By Realtek suggestion,R1558 for discahrge and reserve C1518 only
	P.37	Change R1489 to 18k Ohm,unstuff R1474	Update Board ID for DVT phase,R1474 not used
	P.43	Set Q108,Q113,Q116 to VGA@	For GPU only
	P.23	Change D16 PN,change UMA LVDS RP to bead	Change D16 from SC300000B00 to SC300000B10,change RP to bead for RF team
	P.34	Change JREAD1 Footprint and connection	Change JREAD1 from P12 to P17(TAITW)
	P.39	Connect SUSP# with bypass Res to Q99.1	Reserve for VGA only power on sequence
	P.36	Change JUSB3.12 net to SYSON,update circuit	EVT design issue
	P.27	Unstuff R1077	USB30 Controller interrupt signal option(follow inside design)
	P.33	Update RJ45 circuit	Base on EMI demand, update RJ45 circuit
	P.35	Update 3G/MINI PCIE circuit	
	P.37	Update EC crystal circuit,change Project ID	Add bypass Res. to EC_CRY1 and add PD Res./Cap. by EC team suggestion,change project id setting to EC
	P.38	Chagne LED resistor	For LED brightness fine tune resistor
	P.24	Reserve bypass to HDMI power Change main source	Original → Updated SB000008J00,SB570020410 → SB000008J10 SB501380020 → SB501110010 SB548000320 → SB00000PM00 SC1B491D000,SCS00002000 → SCSH491D010 SC1B751V010 → SC1H751H010 SC600000B00 → SC1N202U010 SD013750A80 → SD034750A80 SE053106Z80,SE093106M80 → SE000005T80 SE053475Z80 → SE107475K80 SGA08101180,SGN19151310 → SGA00002N80 SN111002700 → SN100000K00
	P.42	Change Q115,Q117 to Dual channel MOSFET	
	P.18	Unstuff C436,set C1204 with BACO@	
	P.16	Change R534,R536 as VGA@,update VRAM table	
	P.14	Add 10u_0603 cap. to +1.1VS Change CPU thermal sensor option to TSI	Unstuff R1135,R1136,R1488,R1490,stuff R1486,R1487,R1122,R1124
	P.25	Add test point/net to CRT connector Add USB30 GPP (from SB820M)	By Kun Shan DFT team request Add option source
	P.19	Unstuff R469	Had PD on BACO circuit side(Page.22)
	P.32	Change C1622,C1623 to 33pF Set EC CLK source to SB820M(RTCCLK)	Base on Crystal vender suggestion

Security Classification	Compal Secret Data		
Issued Date	2008/10/06	Deciphered Date	2010/03/12

Compal Electronics, Inc.

Title: HW PIR

Size: B | Document Number: P5WS3 LA-6972P | Rev: 0.1

Date: Tuesday, October 19, 2010 | Sheet 53 of 53