

Compal Confidential

PEW71_81_91 UMA <LA-6582P> M/B Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M

2010-07-08

REV: 1.0

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				Custom	PEW71 M/B LA-6582P Schematic	1.0
				Date:	Thursday, July 08, 2010	Sheet 1 of 48

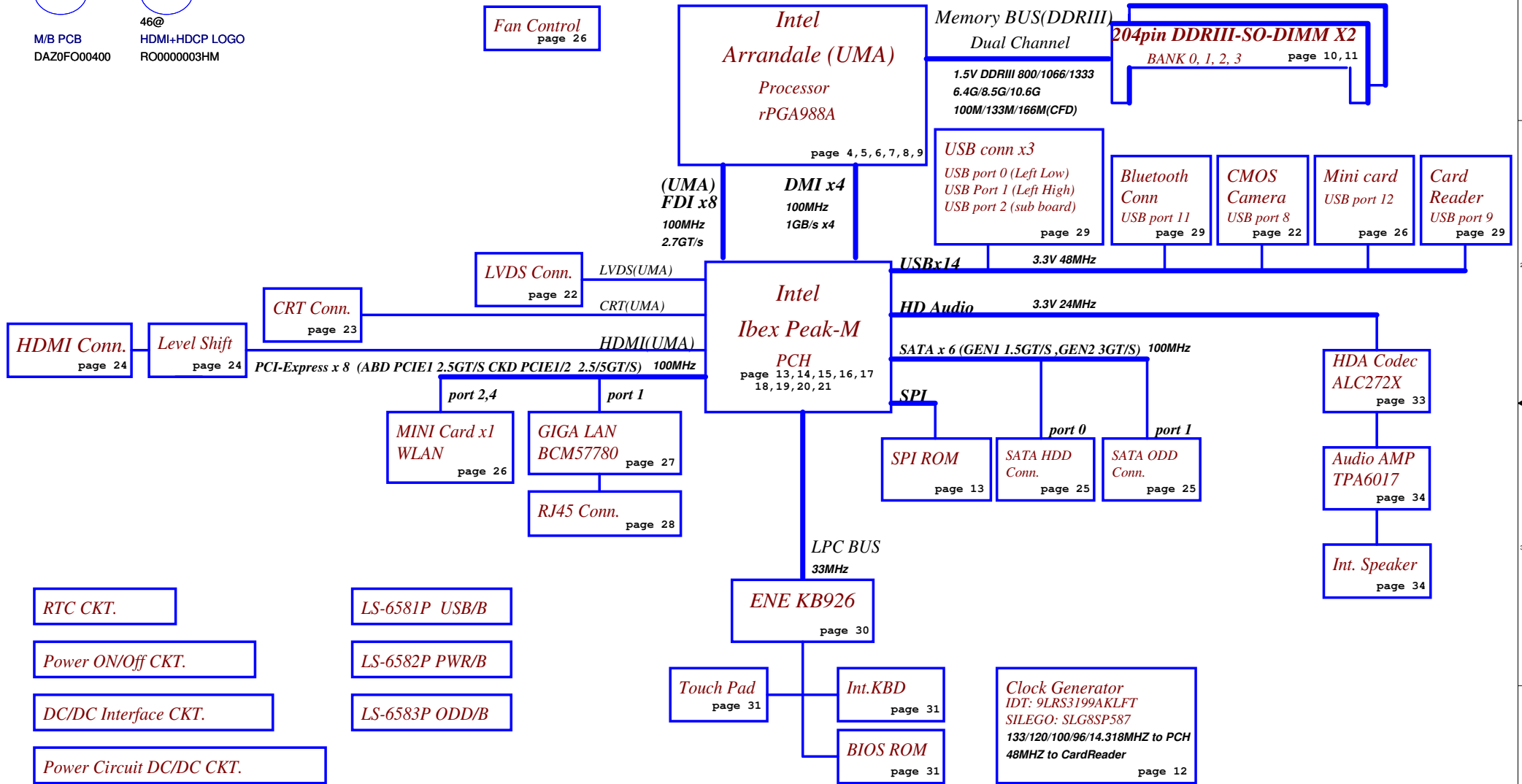
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Model Name PEW71_81_91 UMA

File Name : LA-6582P

ZZZ1
M/B PCB
DAZ0FO00400

ZZZ2
46@
HDMI+HDCP LOGO
RC0000003HM



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				PEW71 M/B LA-6582P Schematic	Rev 1.0
				Date: Thursday, July 08, 2010	Sheet 2 of 48

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.05VS_VTT	1.05V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Project ID / Board ID Table for EC-AD channel

Vcc	3.3V +/- 5%					
Ra/Rc	100K +/- 5%					
	Rb / Rd	VAD_BID min	VAD_BID typ	VAD_BID max	Board ID	Project ID
0	0	0 V	0 V	0 V	0.1	Original NEW70/80/90/50/71/91
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	0.2	PEW71/81/91 Audio Mono/Crystal
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	0.3	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	1.0	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V		
5	100K +/- 5%	1.453 V	1.650 V	1.759 V		
6	200K +/- 5%	1.935 V	2.200 V	2.341 V		PEW71/81/91 Audio Mono/SUSCLK
7	NC	2.500 V	3.300 V	3.300 V		NEW71/91 Optumis

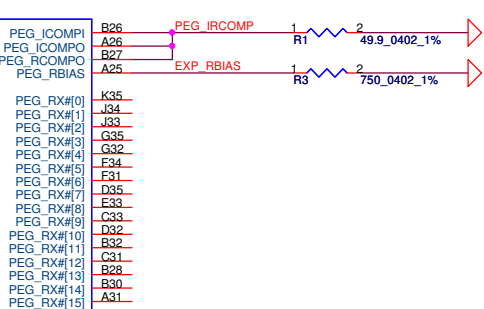
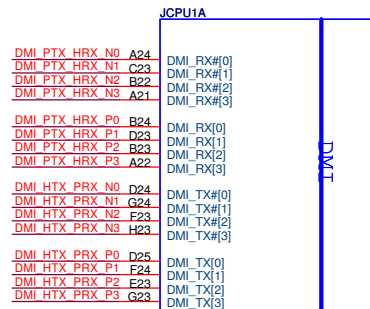
BTO Option Table

BTO Item	BOM Structure
HDMI	HDMI@

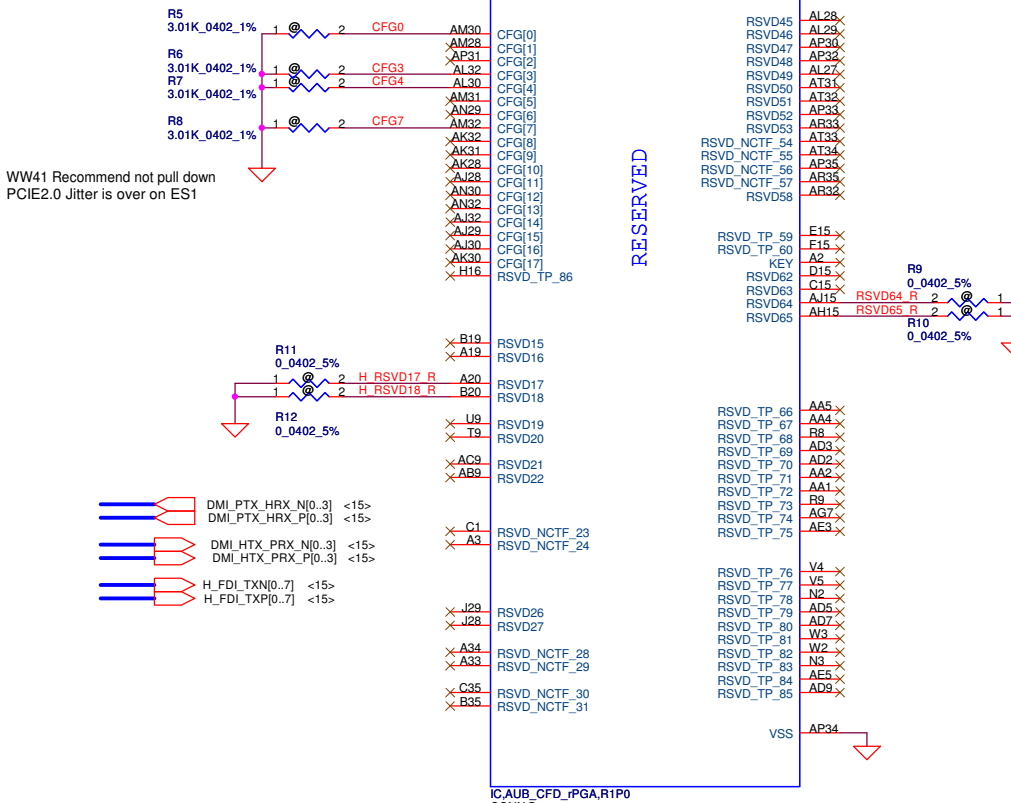
USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port	3 External USB Port
EHC11	UHCI0	0	Ext1 Left Low USB	Ext1 Left Low USB
		1	Ext2 Left High USB	Ext2 Left High USB
		2	Ext3 Right USB	Ext3 Right USB
	UHCI1	3		
		4		
		5		
6				
EHC12	UHCI3	7		
		8	Camera	Camera
	UHCI4	9	Card Reader	Card Reader
		10		
		11	Blue Tooth	Blue Tooth
		12	1st Min-Card	1st Min-Card
		13		

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Size	Document Number		Rev			
B	PEW71 M/B LA-6582P Schematic		1.0			
Date:	Thursday, July 08, 2010		Sheet		3 of 48	



PCI EXPRESS -- GRAPHICS



eDP Signals Mapping

eDP Signal	PEG Singals	Lane Reversal
eDP_TX0	PEG HTX_C_GRX_P15	PEG HTX_C_GRX_P0
eDP_TX#0	PEG HTX_C_GRX_N15	PEG HTX_C_GRX_N0
eDP_TX1	PEG HTX_C_GRX_P14	PEG HTX_C_GRX_P1
eDP_TX#1	PEG HTX_C_GRX_N14	PEG HTX_C_GRX_N1
eDP_TX2	PEG HTX_C_GRX_P13	PEG HTX_C_GRX_P2
eDP_TX#2	PEG HTX_C_GRX_N13	PEG HTX_C_GRX_N2
eDP_TX3	PEG HTX_C_GRX_P12	PEG HTX_C_GRX_P3
eDP_TX#3	PEG HTX_C_GRX_N12	PEG HTX_C_GRX_N3
eDP_AUX	PEG GTX_C_HRX_P13	PEG GTX_C_HRX_P2
eDP_AUX#	PEG GTX_C_HRX_N13	PEG GTX_C_HRX_N2
eDP_HPD#	PEG GTX_C_HRX_P12	PEG GTX_C_HRX_P3

CFG0 - PCI-Express Configuration Select

*1:Single PEG
 0: bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

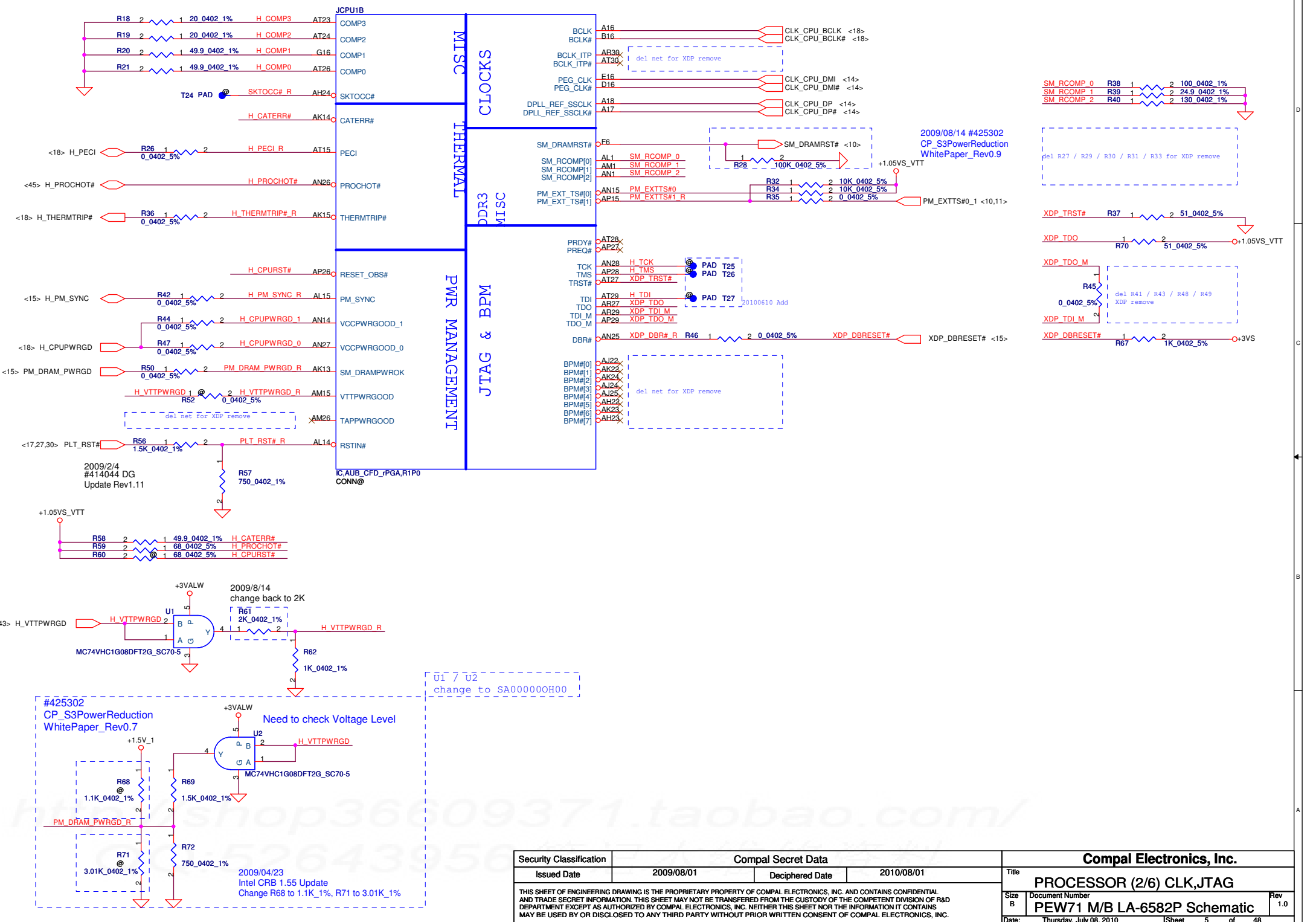
*1 :Normal Operation
 0 :Lane Numbers Reversed
 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
 0:Enabled; An external Display Port device is connected to the Embedded Display Port

**Default

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Date		Sheet		of
Thursday, July 08, 2010		4		48



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				PEW71 M/B LA-6582P Schematic	
				Date:	Thursday, July 08, 2010
				Sheet	5 of 48
				Rev	1.0

<10> DDR_A_D[0..63]
 <10> DDR_A_DM[0..7]
 <10> DDR_A_DQS[0..7]
 <10> DDR_A_MA[0..15]

JCPU1C

DDR A D0 A10
 DDR A D1 C10
 DDR A D2 C7
 DDR A D3 A7
 DDR A D4 B10
 DDR A D5 D10
 DDR A D6 E10
 DDR A D7 A8
 DDR A D8 D8
 DDR A D9 F10
 DDR A D10 E2
 DDR A D11 SA_DQ[10]
 DDR A D12 E9
 DDR A D13 B7
 DDR A D14 E7
 DDR A D15 C6
 DDR A D16 H10
 DDR A D17 G8
 DDR A D18 K7
 DDR A D19 J8
 DDR A D20 G7
 DDR A D21 G10
 DDR A D22 J7
 DDR A D23 J10
 DDR A D24 L7
 DDR A D25 M6
 DDR A D26 M8
 DDR A D27 L9
 DDR A D28 L6
 DDR A D29 K8
 DDR A D30 N8
 DDR A D31 P9
 DDR A D32 AH5
 DDR A D33 AF5
 DDR A D34 AK6
 DDR A D35 AF6
 DDR A D36 AG5
 DDR A D37 AG5
 DDR A D38 AJ7
 DDR A D39 AJ6
 DDR A D40 AJ10
 DDR A D41 AJ9
 DDR A D42 AL10
 DDR A D43 AK12
 DDR A D44 AK8
 DDR A D45 AL7
 DDR A D46 AK11
 DDR A D47 AL8
 DDR A D48 AN8
 DDR A D49 AM10
 DDR A D50 AR11
 DDR A D51 AL11
 DDR A D52 AM9
 DDR A D53 AN9
 DDR A D54 AT11
 DDR A D55 AP12
 DDR A D56 AM12
 DDR A D57 AN12
 DDR A D58 AM13
 DDR A D59 AT14
 DDR A D60 AT12
 DDR A D61 AL13
 DDR A D62 AR14
 DDR A D63 AP14
 SA_DQ[63]

DDR SYSTEM MEMORY A

SA_CK[0] AA6
 SA_CK#0 AA7
 SA_CKE[0] P7
 SA_CK[1] Y6
 SA_CK#1 Y6
 SA_CKE[1] P6
 SA_CS#0 CAE2
 SA_CS#1 CAE8
 SA_ODT[0] AD8
 SA_ODT[1] AF9
 SA_DM[0] B9
 SA_DM[1] D7
 SA_DM[2] LH7
 SA_DM[3] M7
 SA_DM[4] AG6
 SA_DM[5] AM7
 SA_DM[6] AN10
 SA_DM[7] AN13
 SA_DQS#0 C9
 SA_DQS#1 C8
 SA_DQS#2 C9
 SA_DQS#3 CAH7
 SA_DQS#4 CAK9
 SA_DQS#5 CAP11
 SA_DQS#6 CAP11
 SA_DQS#7 CAT13
 SA_DQS[0] C8
 SA_DQS[1] F9
 SA_DQS[2] LH9
 SA_DQS[3] MH9
 SA_DQS[4] AK10
 SA_DQS[5] AN11
 SA_DQS[6] AN11
 SA_DQS[7] AR13
 SA_MA[0] Y3
 SA_MA[1] W1
 SA_MA[2] AA8
 SA_MA[3] AA3
 SA_MA[4] V1
 SA_MA[5] AA9
 SA_MA[6] V8
 SA_MA[7] T1
 SA_MA[8] Y9
 SA_MA[9] U6
 SA_MA[10] AD4
 SA_MA[11] U3
 SA_MA[12] AG8
 SA_MA[13] T3
 SA_MA[14] T3
 SA_MA[15] V9
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 DDR A_CKE0 <10>
 DDR A_CLK1 <10>
 DDR A_CLK1# <10>
 DDR A_CKE1 <10>
 DDR A_CS0# <10>
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 DDR A_ODT0 <10>
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 DDR A_DM5
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 DDR A_DQS#2
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 DDR A_DQS#4
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 DDR A_DQS#6
 DDR A_DQS#7
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 DDR A_DQS2
 DDR A_DQS3
 DDR A_DQS4
 DDR A_DQS5
 DDR A_DQS6
 DDR A_DQS7
 DDR A_MA0
 DDR A_MA1
 DDR A_MA2
 DDR A_MA3
 DDR A_MA4
 DDR A_MA5
 DDR A_MA6
 DDR A_MA7
 DDR A_MA8
 DDR A_MA9
 DDR A_MA10
 DDR A_MA11
 DDR A_MA12
 DDR A_MA13
 DDR A_MA14
 DDR A_MA15

IC_AUB_CFD_rPGA,R1P0
 CONN@

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 <11> DDR_B_DM[0..7]
 <11> DDR_B_DQS[0..7]
 <11> DDR_B_MA[0..15]

JCPU1D

DDR B D0 B5
 DDR B D1 A5
 DDR B D2 C3
 DDR B D3 B3
 DDR B D4 E4
 DDR B D5 A6
 DDR B D6 C4
 DDR B D7 D4
 DDR B D8 D1
 DDR B D9 D2
 DDR B D10 F2
 DDR B D11 F1
 DDR B D12 F2
 DDR B D13 F5
 DDR B D14 F3
 DDR B D15 G4
 DDR B D16 H6
 DDR B D17 G2
 DDR B D18 J6
 DDR B D19 J3
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 DDR B D25 L3
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 DDR B D32 AE1
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 DDR B D63 AT10
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DDR SYSTEM MEMORY - B

IC_AUB_CFD_rPGA,R1P0
 CONN@

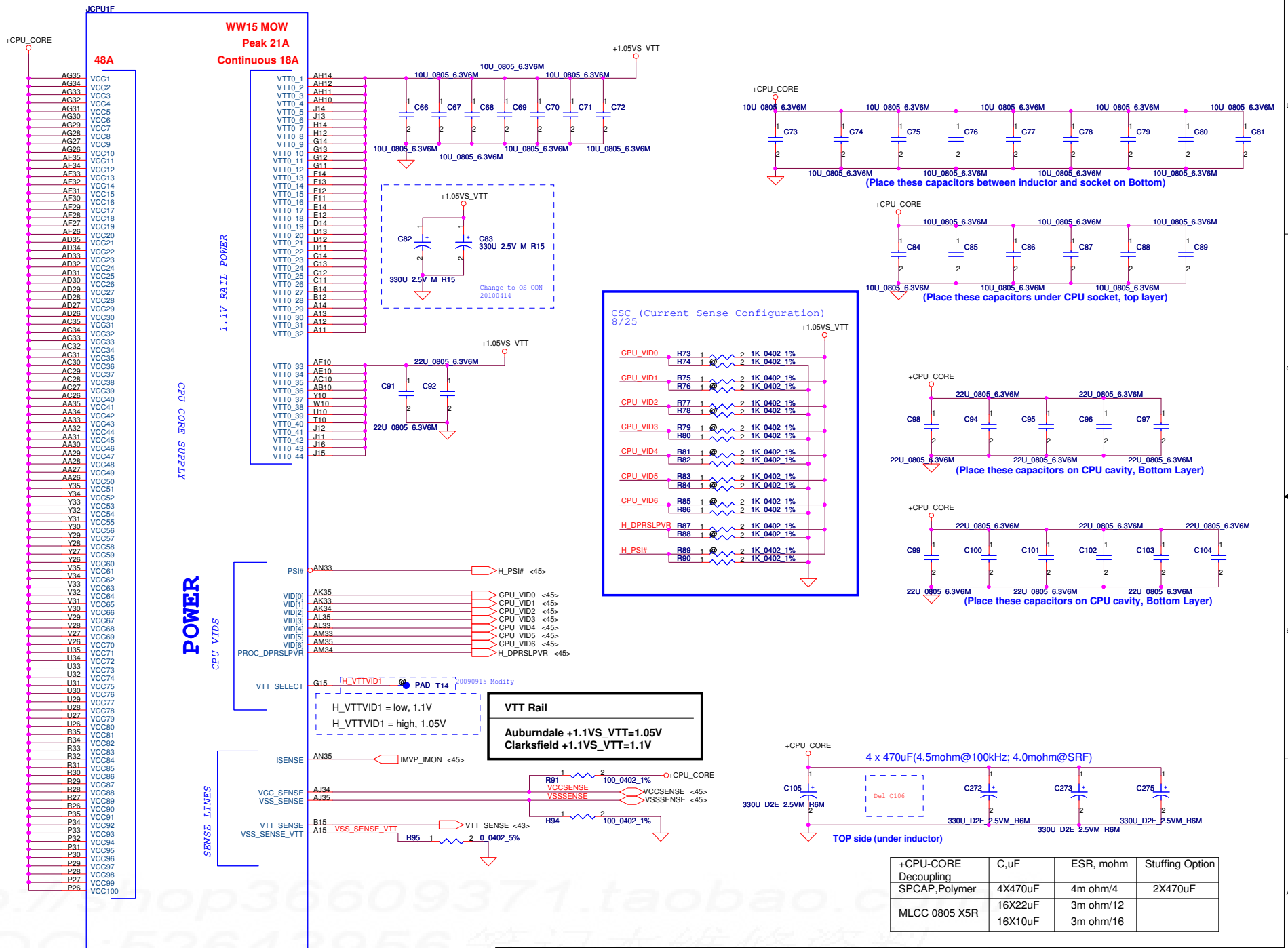
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 SB_CS#1 AD6
 SB_ODT[0] AC7
 SB_ODT[1] AD1
 SB_DM[0] D4
 SB_DM[1] E1
 SB_DM[2] H3
 SB_DM[3] K1
 SB_DM[4] AH1
 SB_DM[5] AL2
 SB_DM[6] AR4
 SB_DM[7] AT8
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 SB_DQS#1 E4
 SB_DQS#2 D4
 SB_DQS#3 L4
 SB_DQS#4 AH2
 SB_DQS#5 AR5
 SB_DQS#6 AR8
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 SB_DQS3
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 SB_MA[5] TR
 SB_MA[6] R2
 SB_MA[7] R6
 SB_MA[8] R4
 SB_MA[9] R5
 SB_MA[10] AB5
 SB_MA[11] P3
 SB_MA[12] R3
 SB_MA[13] AF7
 SB_MA[14] P5
 SB_MA[15] N1
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 DDR B_DM1
 DDR B_DM2
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 DDR B_DM4
 DDR B_DM5
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B	PEW71 M/B LA-6582P Schematic	Thursday, July 08, 2010		1.0	
				Sheet	6 of 48

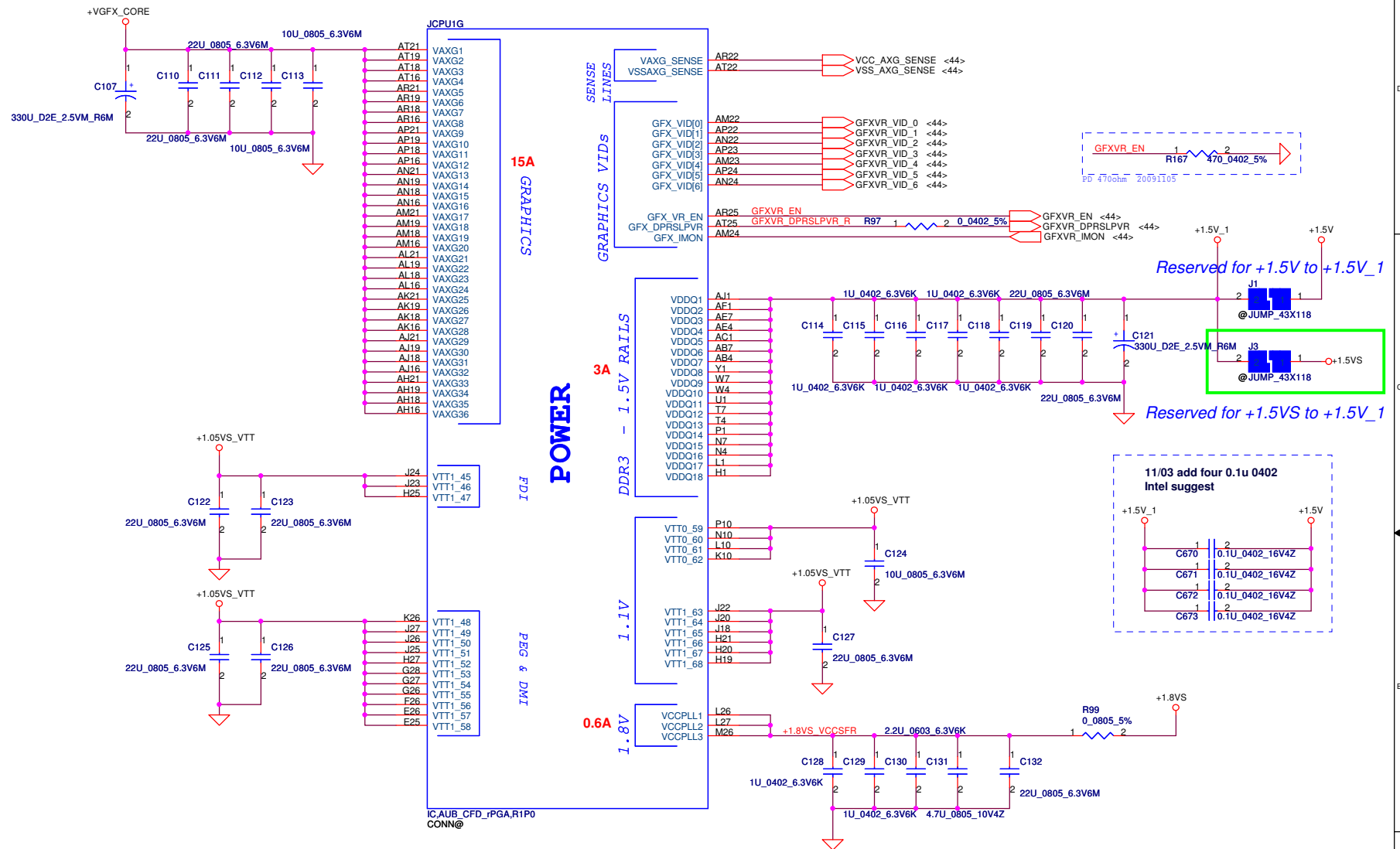


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CONN@

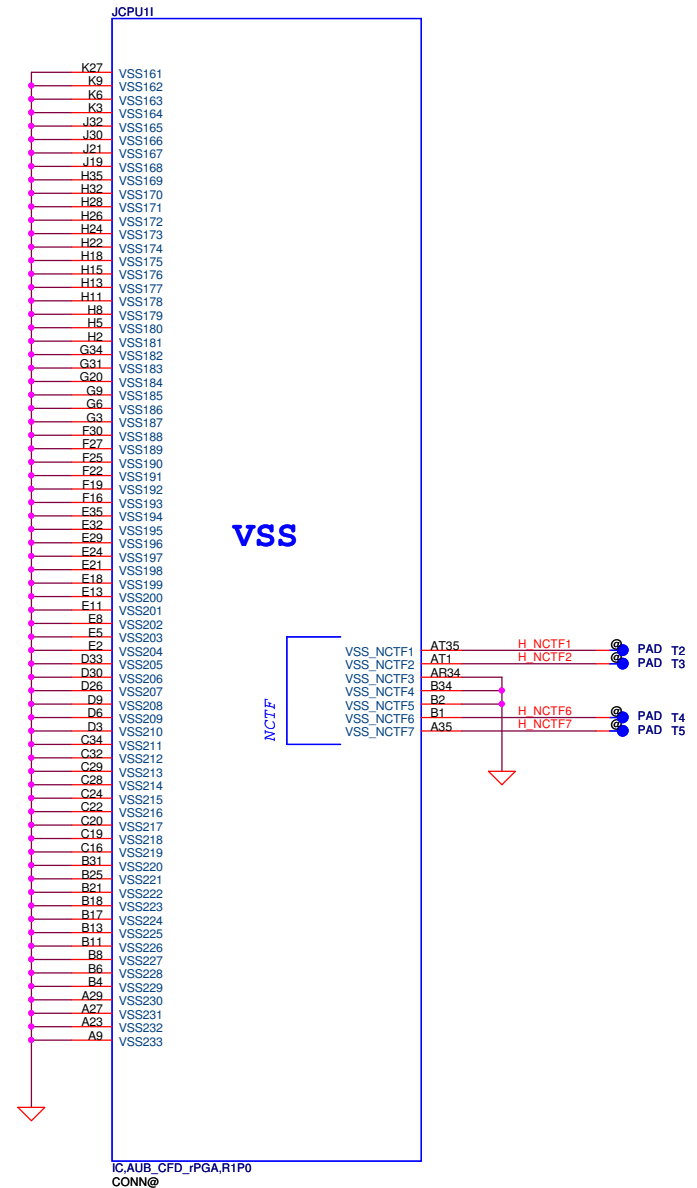
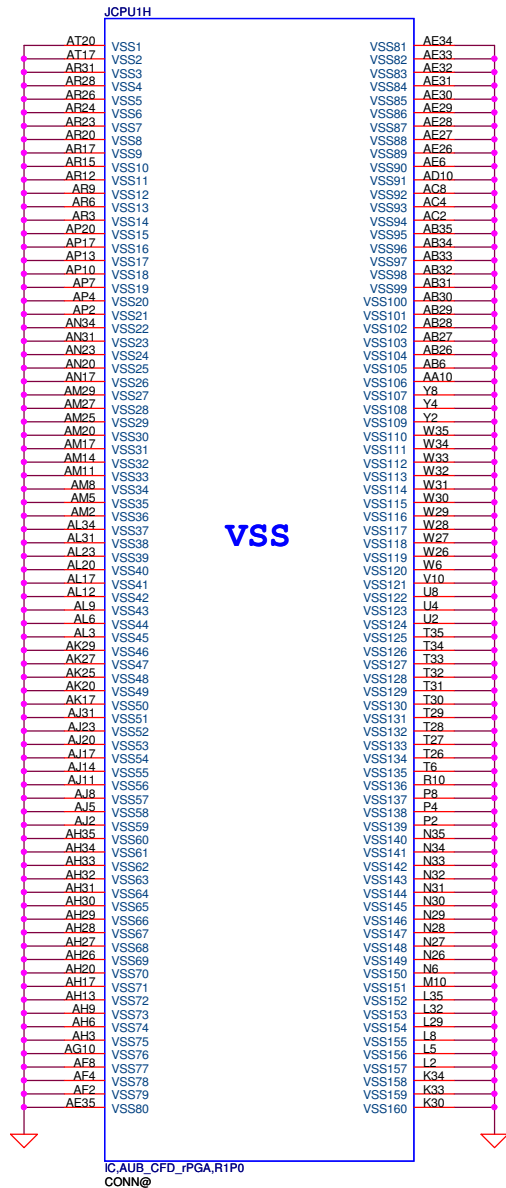
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Compal Electronics, Inc.			
Title			
PROCESSOR (4/6) PWR, Bypass			
Size	Document Number		Rev
Customer	PEW71 M/B LA-6582P Schematic		1.0
Date:	Thursday, July 08, 2010	Sheet	7 of 48

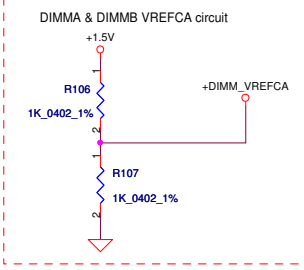
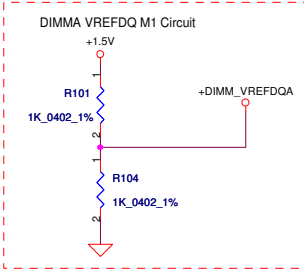


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Size	Document Number	Customer		Rev	
	PEW71 M/B LA-6582P Schematic			1.0	
Date:	Thursday, July 08, 2010	Sheet	8	of 48	

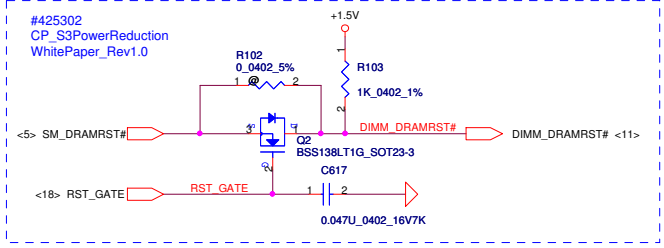


<http://shop3669371.taobao.com/>
QQ:53439

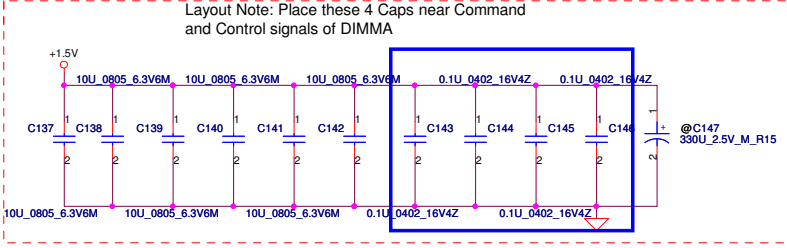
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Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title	
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Size	Document Number	Customer		Rev	
	PEW71 M/B LA-6582P Schematic			1.0	
Date:	Thursday, July 08, 2010	Sheet	9	of 48	



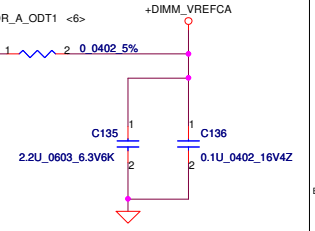
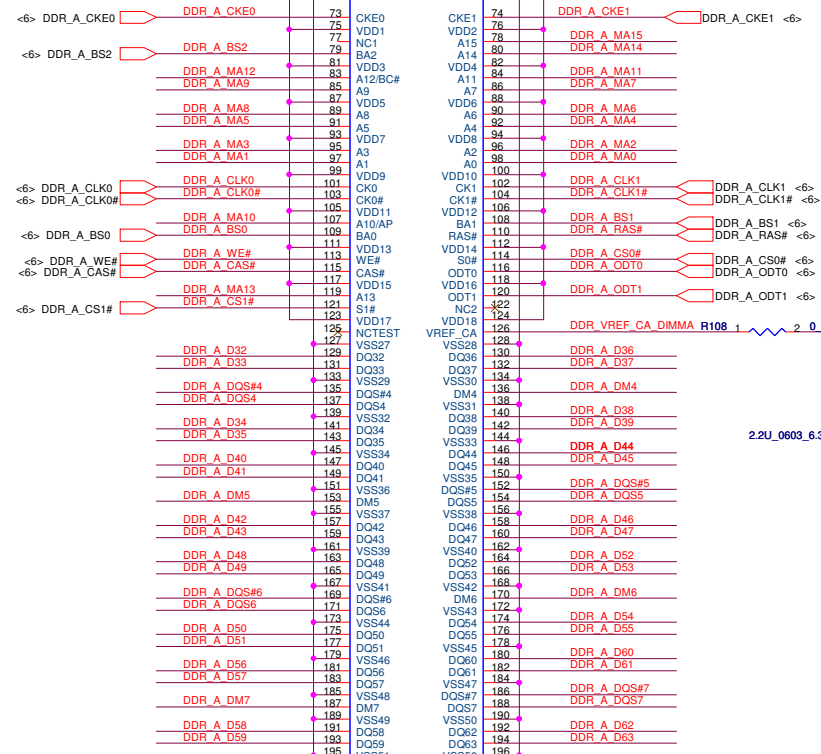
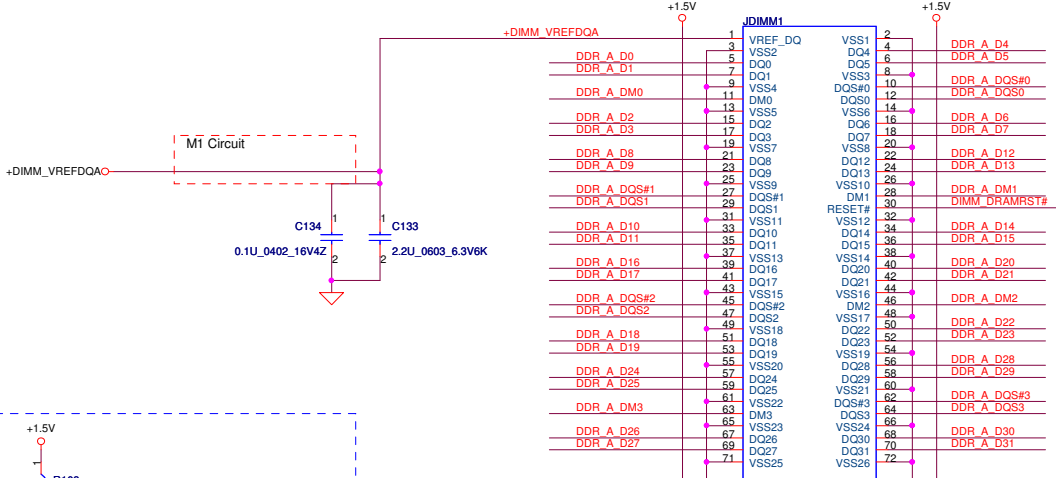
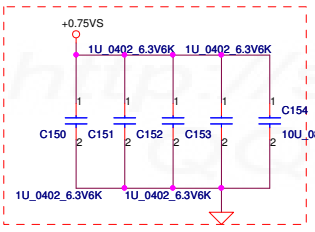
- <6> DDR_A_DQS#[0..7]
- <6> DDR_A_D[0..63]
- <6> DDR_A_DM[0..7]
- <6> DDR_A_DQS[0..7]
- <6> DDR_A_MA[0..15]



Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203 & JDIMM1.204



DDR3 SO-DIMM A Change to Reverse Type 8mm High

Compal Electronics, Inc.
DDRIII-SODIMM SLOT1

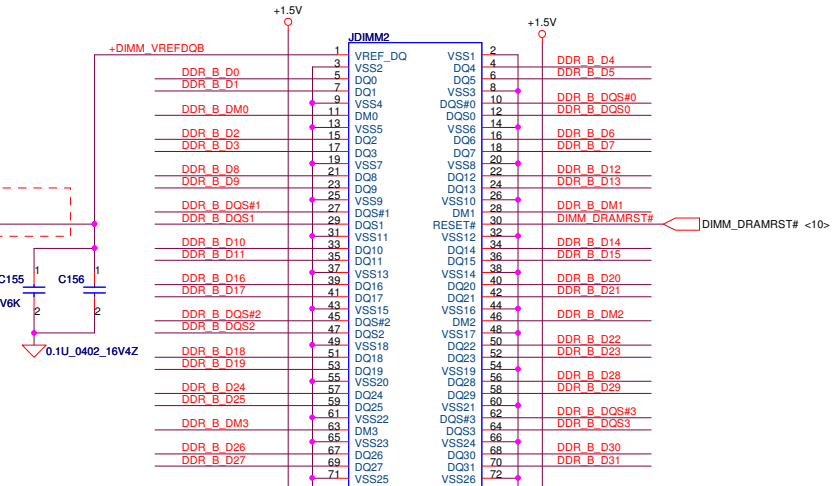
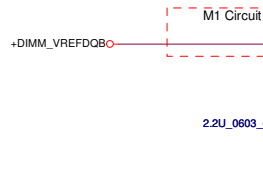
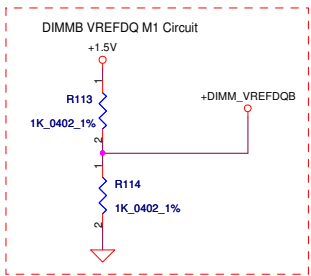
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Issued Date	2009/08/01	Deciphered Date
		2010/08/01

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Title		Date	
Title		Date	Thursday, July 08, 2010
Size	Document Number	Sheet	10 of 48
Custort	PEW71 M/B LA-6582P Schematic	Rev	1.0

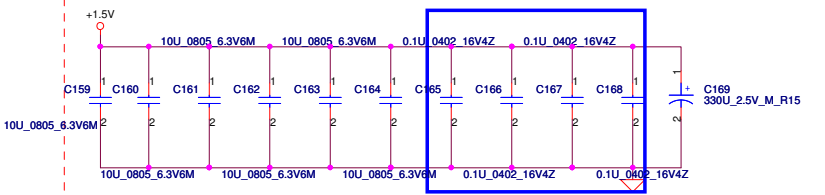
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- <6> DDR_B_D[0..63]
- <6> DDR_B_DM[0..7]
- <6> DDR_B_DQS#[0..7]
- <6> DDR_B_MA[0..15]

2008/9/8 #400755
 Calpella Clarkstead
 DDR3 SO-DIMM
 VREFDQ Platform
 Design Guide Change Details

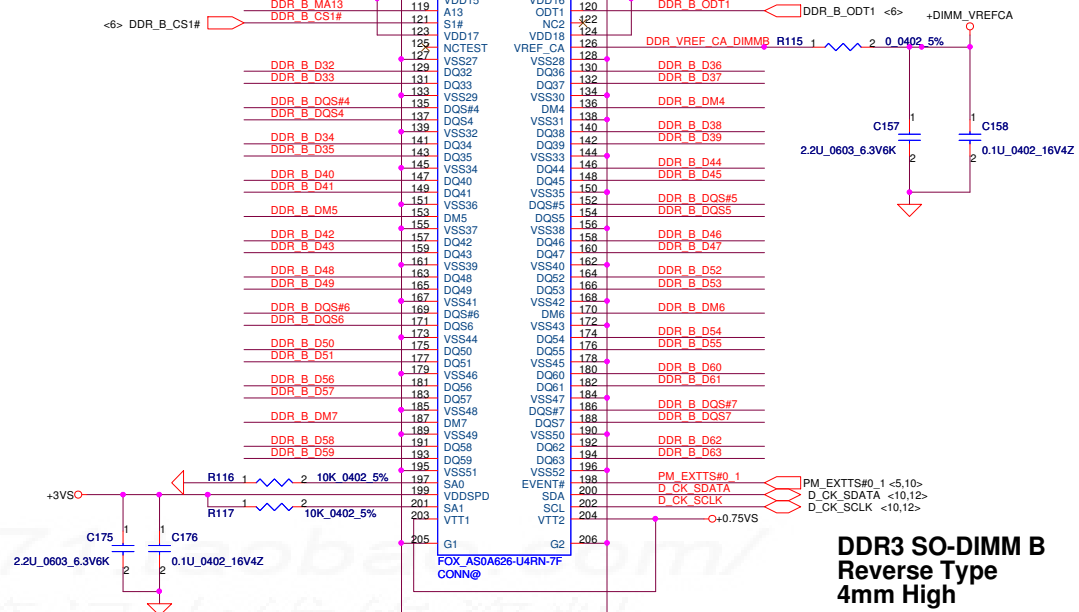
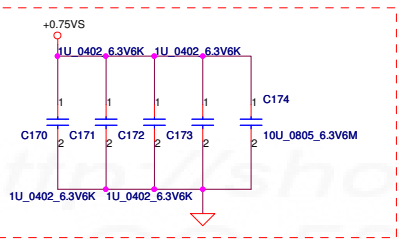


Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB

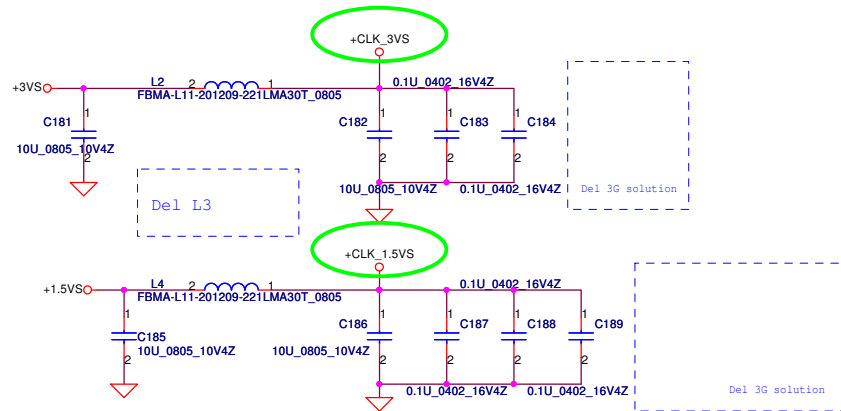
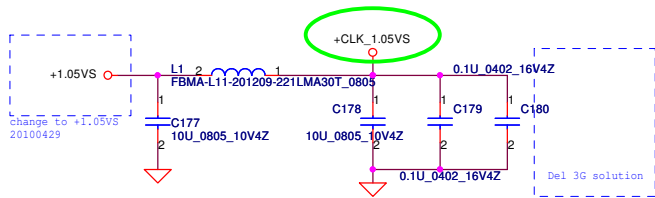


Layout Note:
Place near JDIMM2.203 & JDIMM2.204

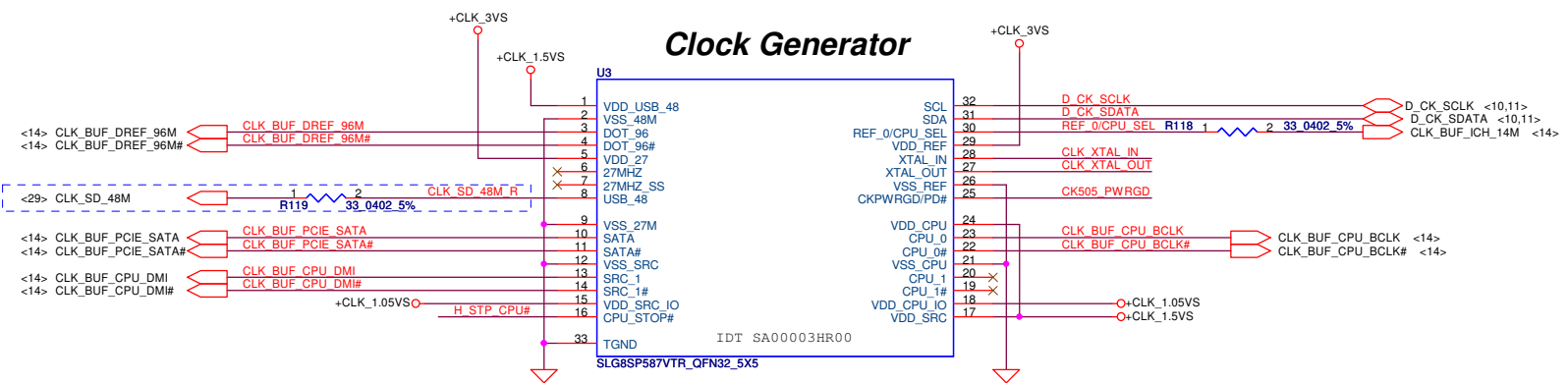


**DDR3 SO-DIMM B
Reverse Type
4mm High**

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<p>Compal Electronics, Inc. DDR3-SODIMM SLOT2</p>			<p>Size Document Number PEW71 M/B LA-6582P Schematic</p>	
Date: Thursday, July 08, 2010			Page: 11 of 48	

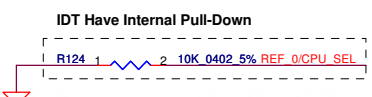
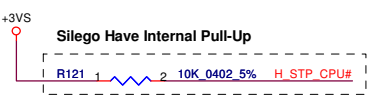


Clock Generator

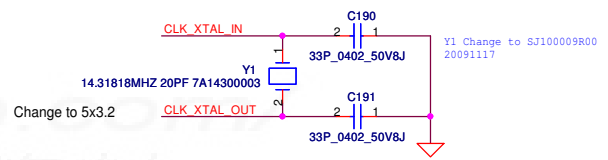
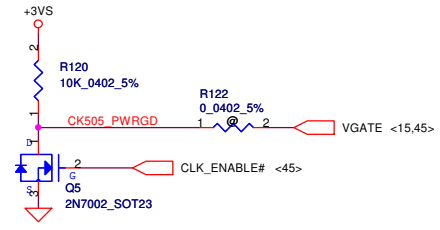
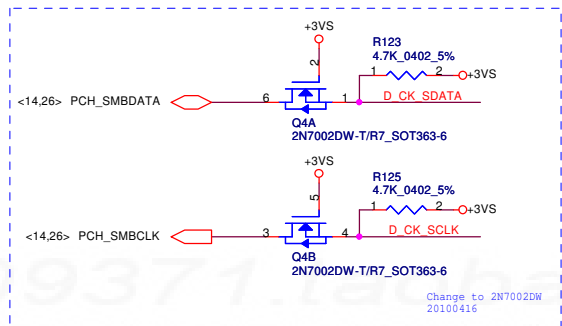


IDT: 9LRS3199AKLFT, SA00003P00
 SILEGO: SLG8SP587V(WF), SA00002XY10
 Low Power:
 IDT: 9LVS3199AKLFT, SA00003HR00
 Realtek: RTM890N-631-GRT, SA00003HQ00

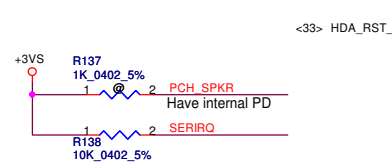
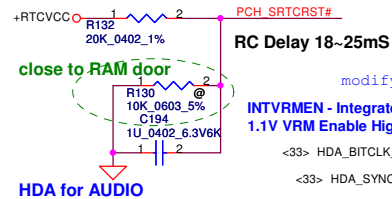
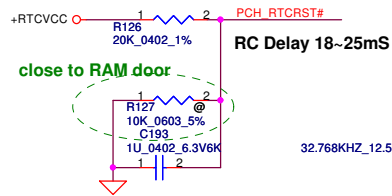
For Cardreader



PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

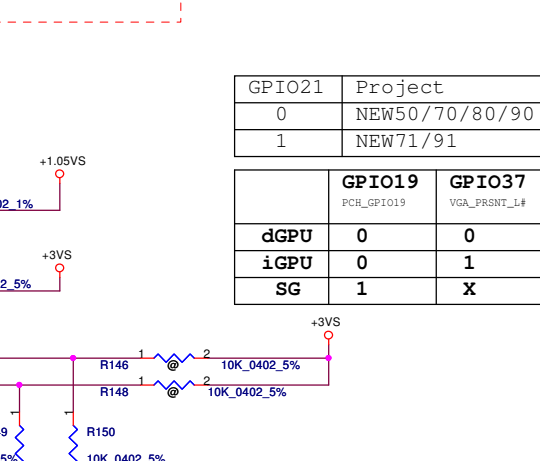
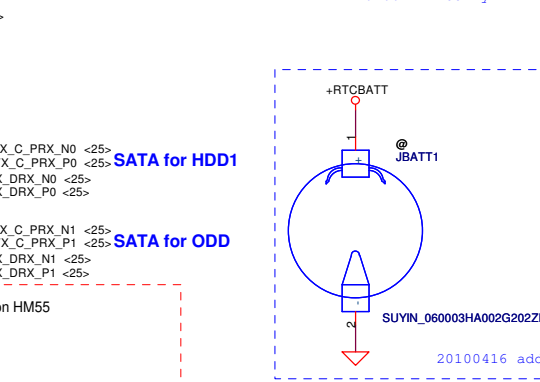
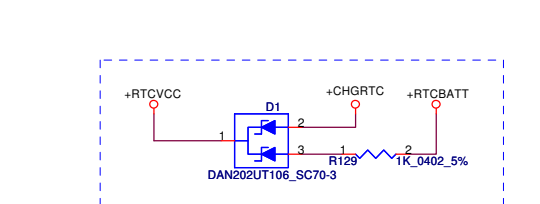
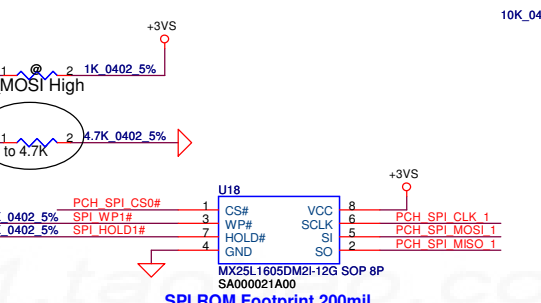
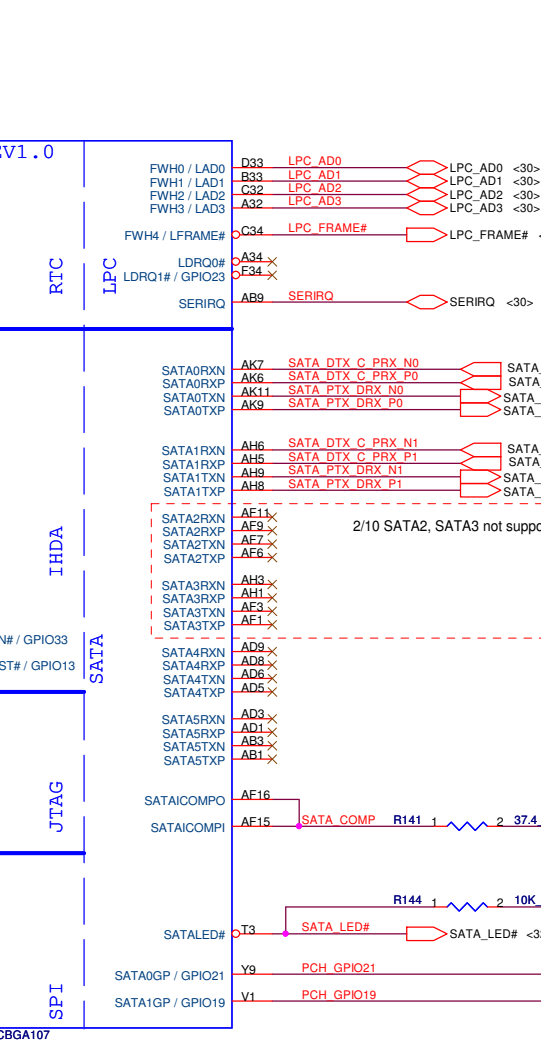
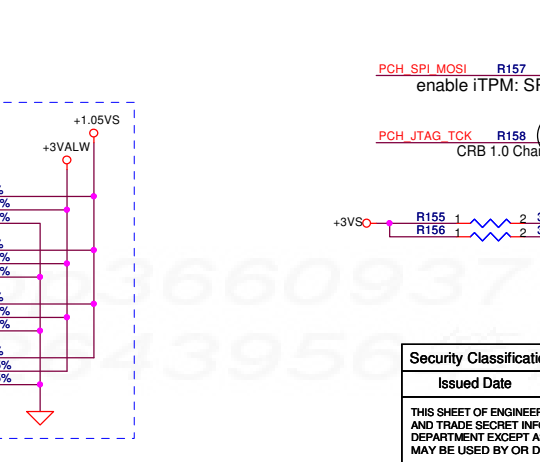
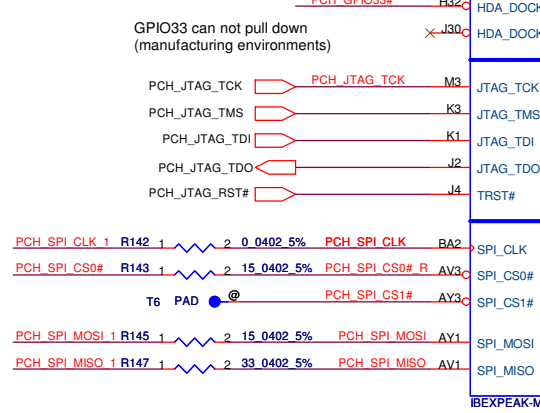
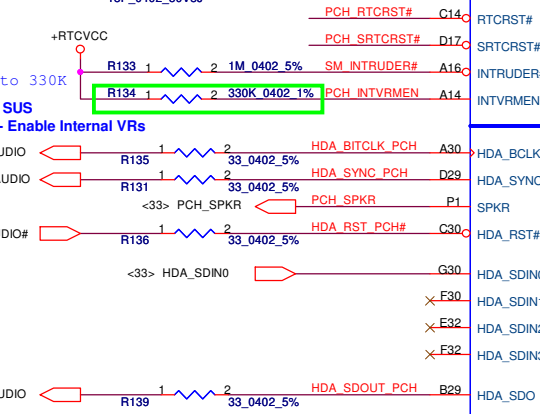
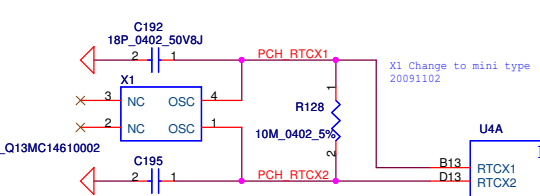


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Size	Document Number	Customer		Rev	
Date	PEW71 M/B LA-6582P Schematic	Thursday, July 08, 2010		1.0	
Sheet 12		of 48			



If GPIO33 pull down, ME will not working. For factory update ME, pull down resistor pull under door.

GPIO33 has a weak internal pull-up
NOTE: Asserting the GPIO33 low on the rising edge of PWROK will also halt Intel Management Engine after chipset bringup and disable runtime Intel Management Engine features. This is a debug mode and must not be asserted after manufacturing/ debug.



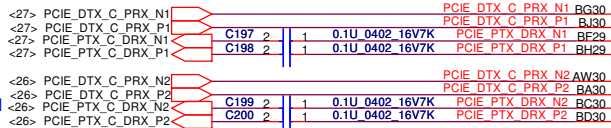
GPIO21	Project
0	NEW50/70/80/90
1	NEW71/91

	GPIO19	GPIO37
	PCH_GPIO19	VGA_PRSNT_L#
dGPU	0	0
iGPU	0	1
SG	1	X

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Size	Document Number	Customer		Rev	
	PEW71	M/B LA-6582P Schematic		1.0	
Date:	Thursday, July 08, 2010	Sheet	13	of 48	

For PCIE LAN

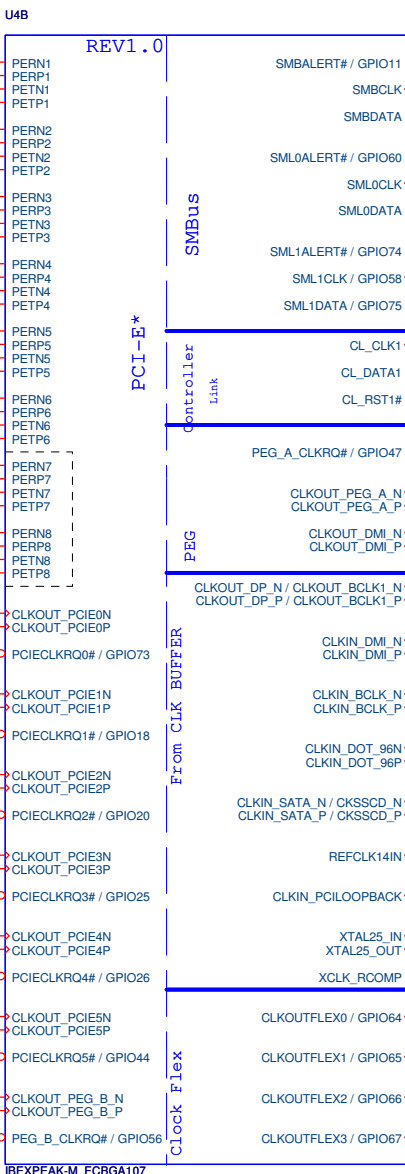
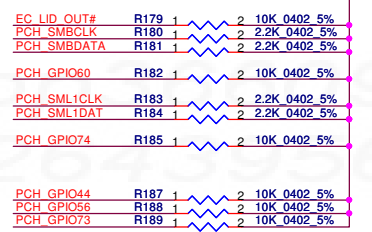
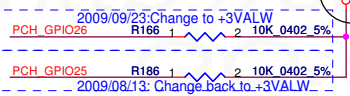
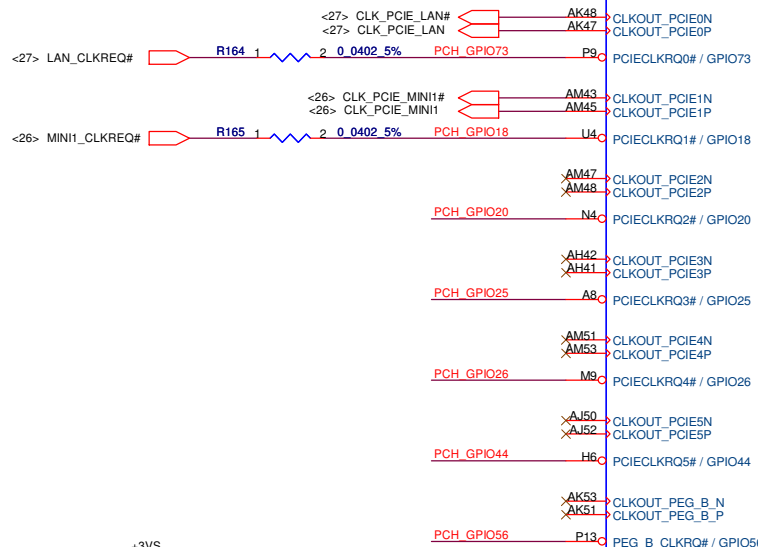
For Wireless LAN



2/10 PCIE7, PCIE8 not support on HM55

For PCIE LAN

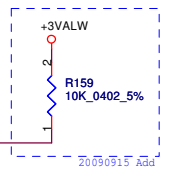
For Wireless LAN



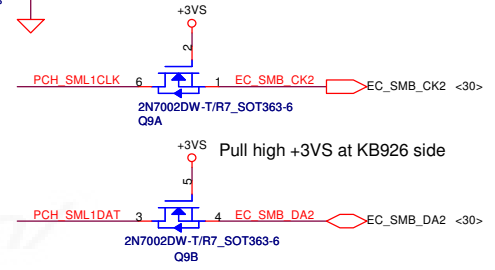
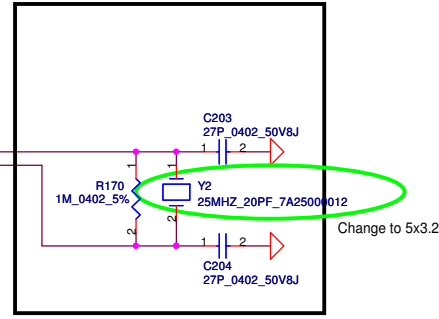
0602 GPIO65 no use
PULL HIGH:PVT
PULL DOWN:DVT

GPIO66 6L/8L	
SATA register spare	
GPIO66	0 6L *
	1 8L

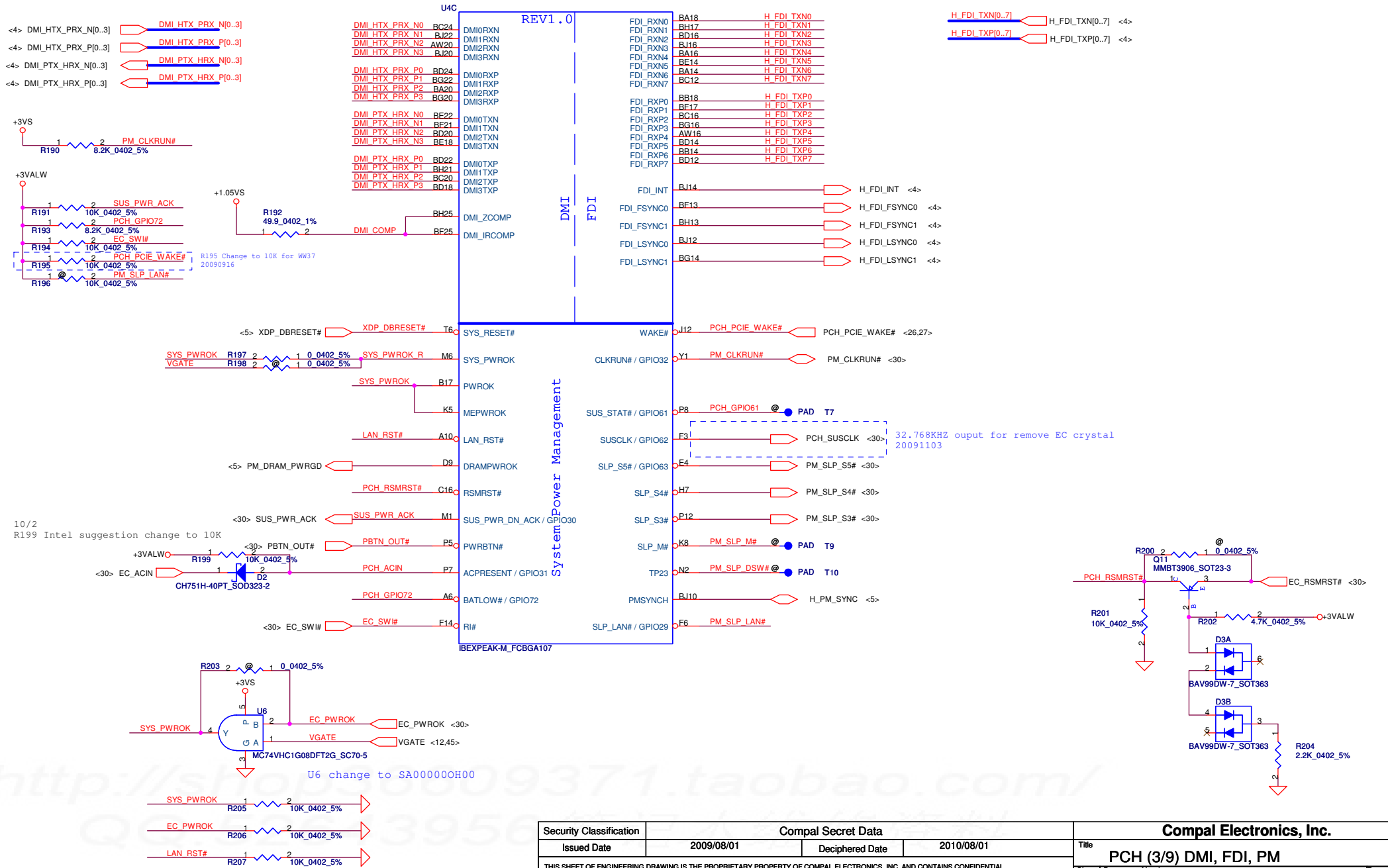
1. Connect Directly EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS LAN
4. Level Shift3, Pull-Up to +3VS CPU & PCH XDP



6/9 MOW23 Request add 25MHz crystal supporting Integrated Graphics

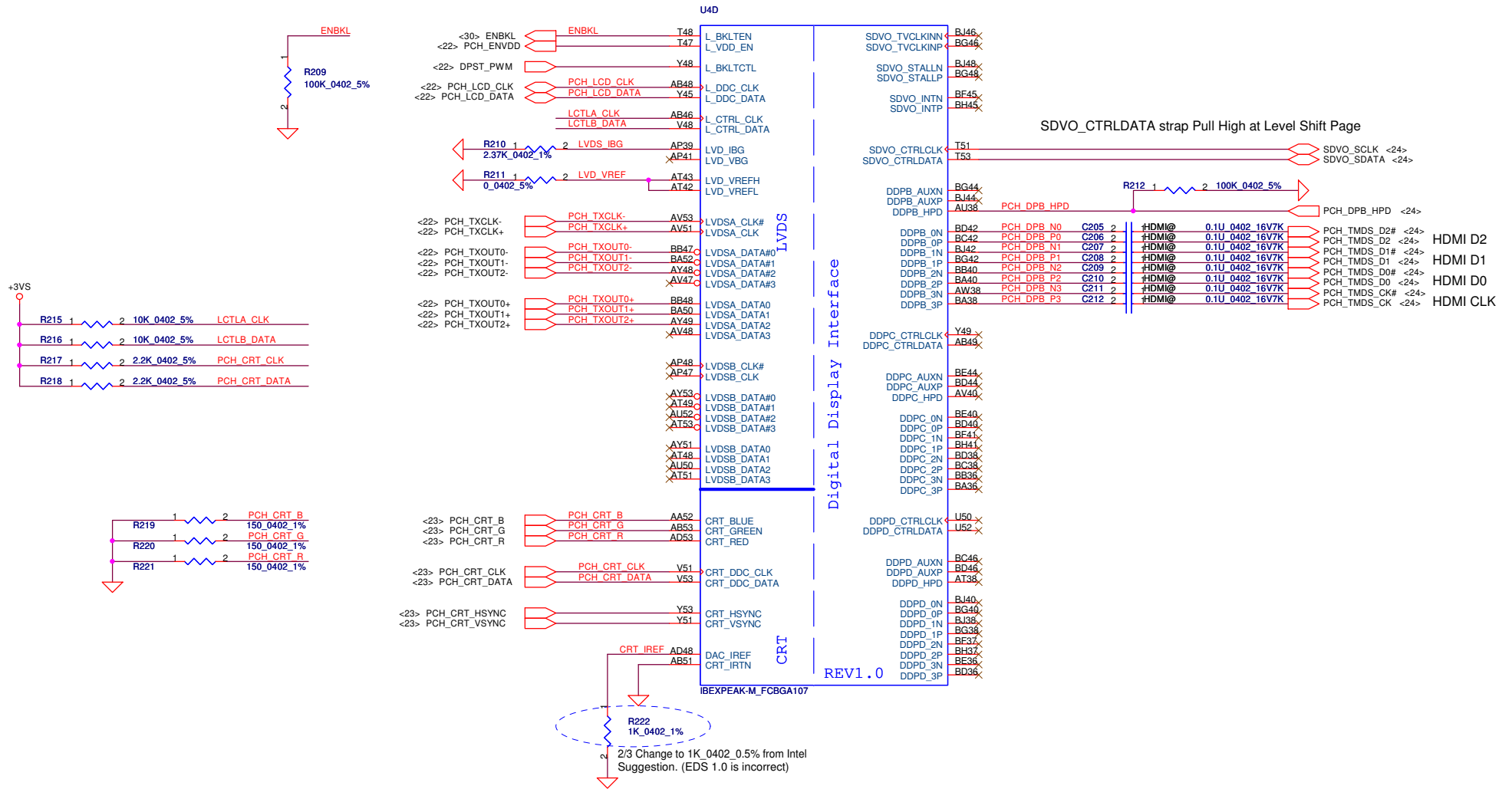


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Size	Document Number	Date	Thursday, July 08, 2010	Sheet	14 of 48
Customer	PEW71 M/B LA-6582P Schematic	Rev	1.0		



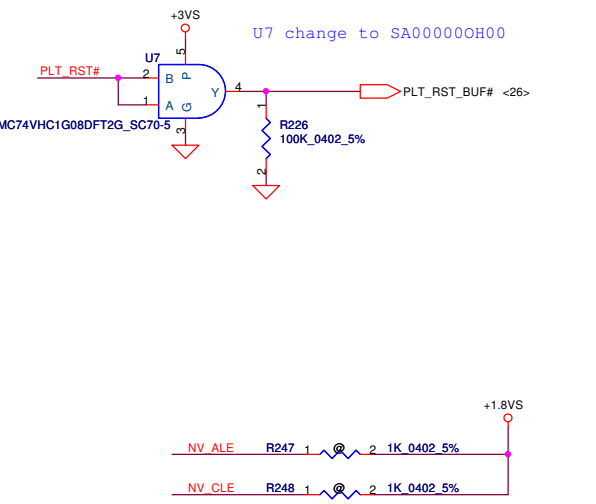
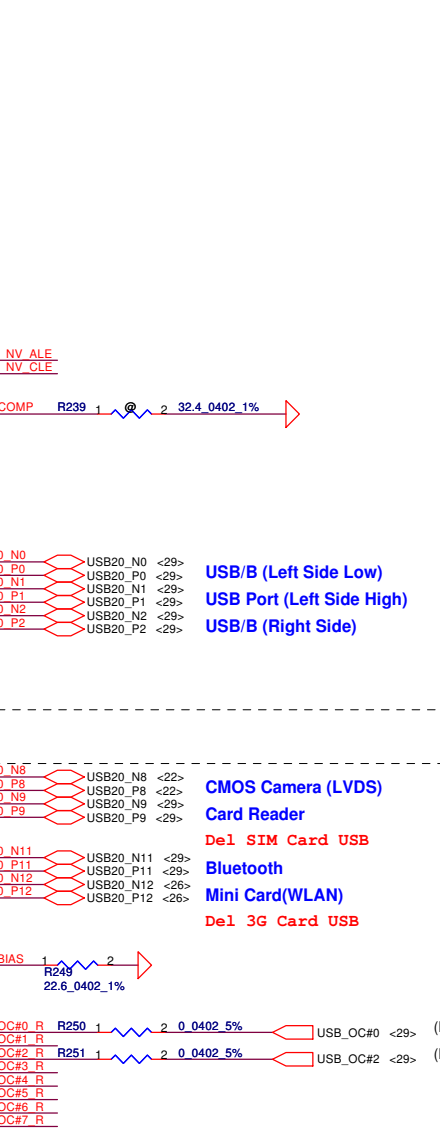
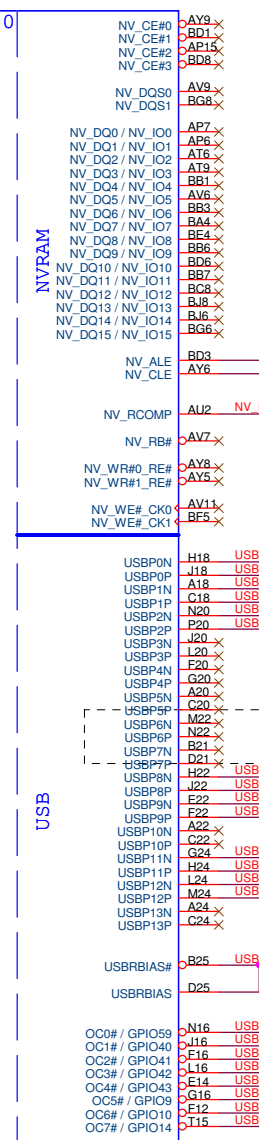
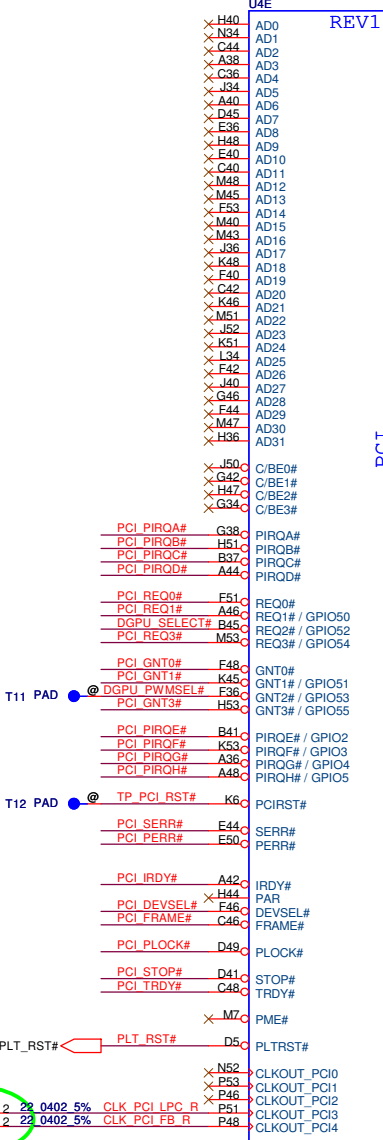
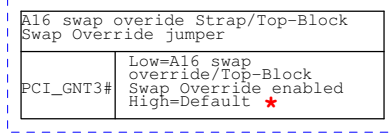
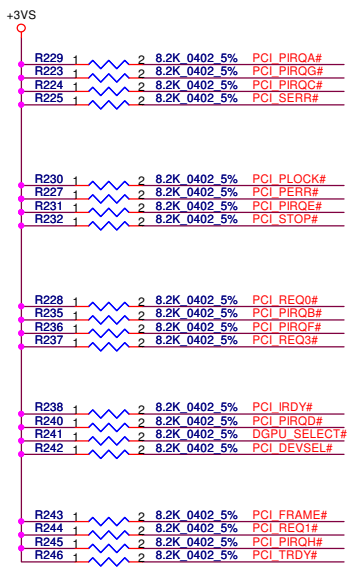
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Size	Document Number	Customer		Rev	
	PEW71	M/B LA-6582P Schematic		1.0	
Date:	Thursday, July 08, 2010	Sheet	15	of 48	

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 QQ:52643956

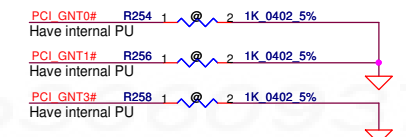
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Size	Document Number	Customer		Rev	1.0
Date:	Thursday, July 08, 2010	Sheet		16	of 48



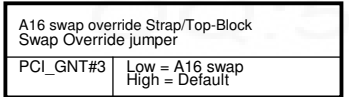
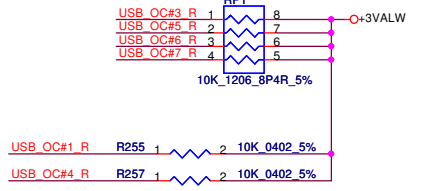
Intel Anti-Theft Technology	
NV_ALE	High=Enabled Low=Disables(floating) *
DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH Set to Vss when LOW

NV_ALE
Enable Intel Anti-Theft Technology : 8.2K PU to +3VS
Disable Intel Anti-Theft Technology : floating(internal PD)
NV_CLE
DMI termination voltage.
weak internal PU, don't PD

PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

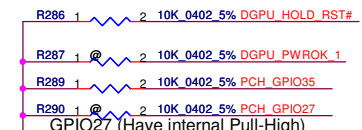
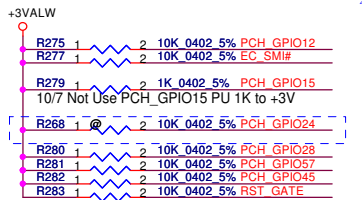
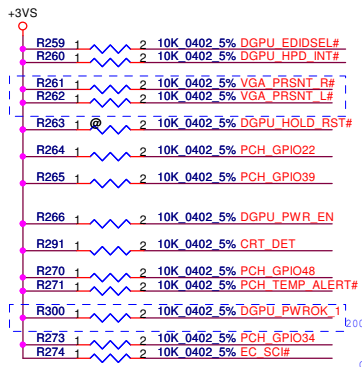


OC[0..3] use for EHCI 1
OC[4..7] use for EHCI 2



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Compal Electronics, Inc.			
Title PCH (5/9) PCI, USB, VRAM			
Size	Document Number	Rev	
Customer	PEW71 M/B LA-6582P Schematic	1.0	
Date:	Thursday, July 08, 2010	Sheet	17 of 48



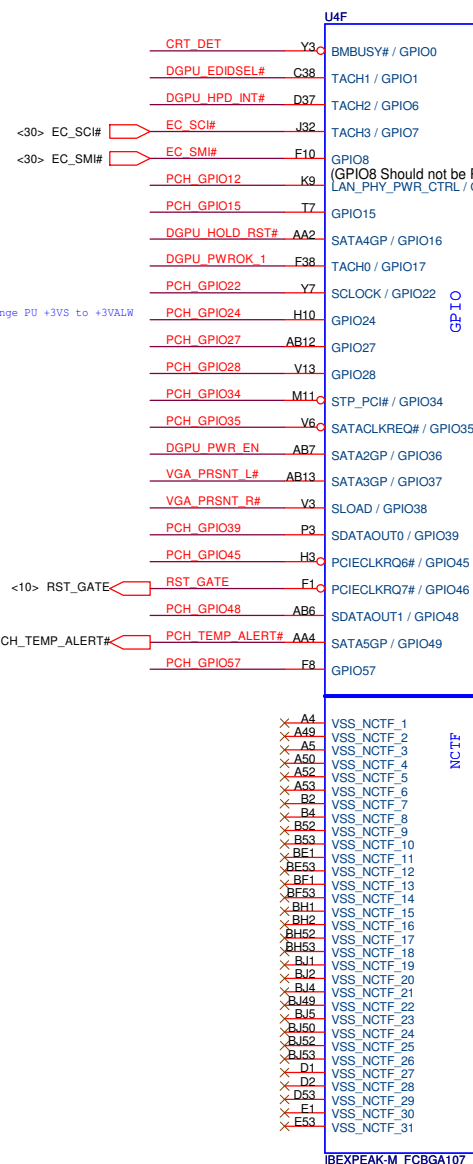
High: VCCVRM VR Enable
Low: VCCVRM VR Disable

	GPIO19	GPIO37
	PCH_GPIO19	VGA_PRSNT_L#
dGPU	0	0
iGPU	0	1
SG	1	0

GPIO27
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

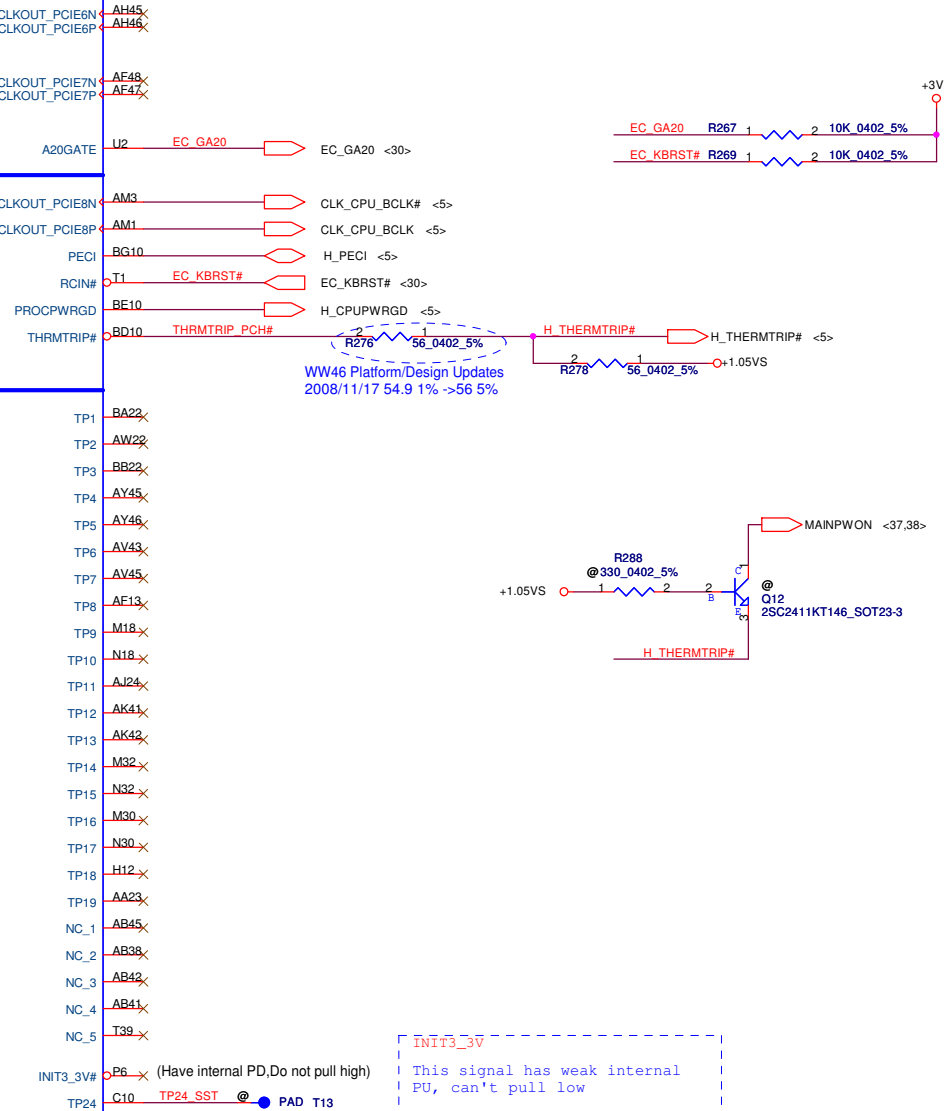
GPIO8
This signal has a weak internal pull up
can't Pull low

GPIO15
Intel ME Crypto Transport Layer Security (TLS) chiper suite with no confidentiality
* H : Intel ME Crypto Transport Layer Security (TLS) chiper suite with confidentiality
L : have weak internal PU 20K



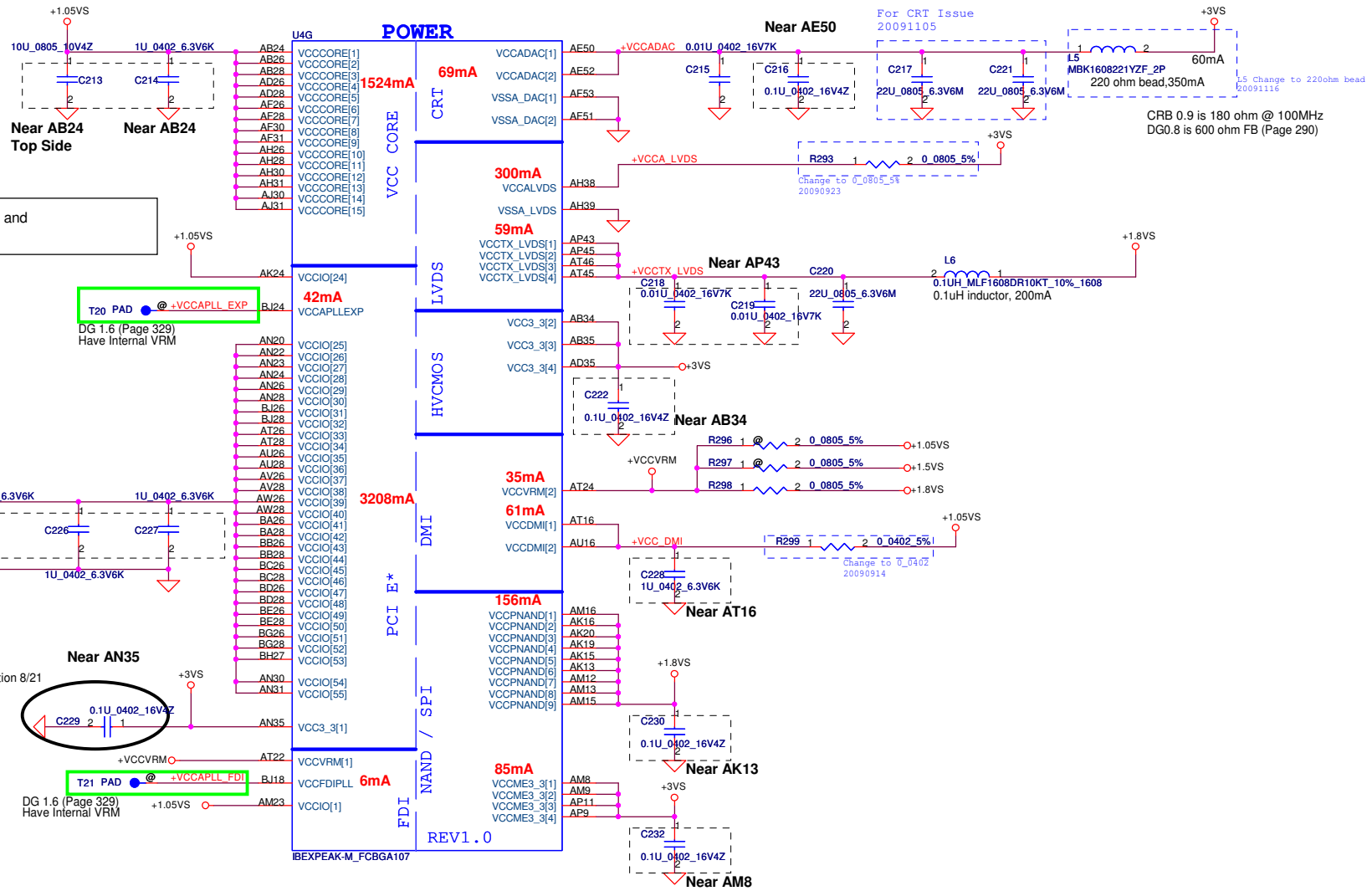
REV1.0

IBEXPEAK-M_FCBGA107



INIT3_3V
This signal has weak internal PU, can't pull low

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Date:	Thursday, July 08, 2010	Sheet	18	of	48



All IbeX Peak-M Power rails with netnames +1.1VS and +1.1V rails are actually +1.05VS and +1.05V rails

Intel suggest follow CRB 8/21

T20 PAD @ +VCCAPLL EXP
DG 1.6 (Page 329)
Have Internal VRM

Follow Intel suggestion 8/21

T21 PAD @ +VCCAPLL FDI
DG 1.6 (Page 329)
Have Internal VRM

For CRT Issue 20091105

Change to 220ohm bead 20091116

CRB 0.9 is 180 ohm @ 100MHz
DG0.8 is 600 ohm FB (Page 290)

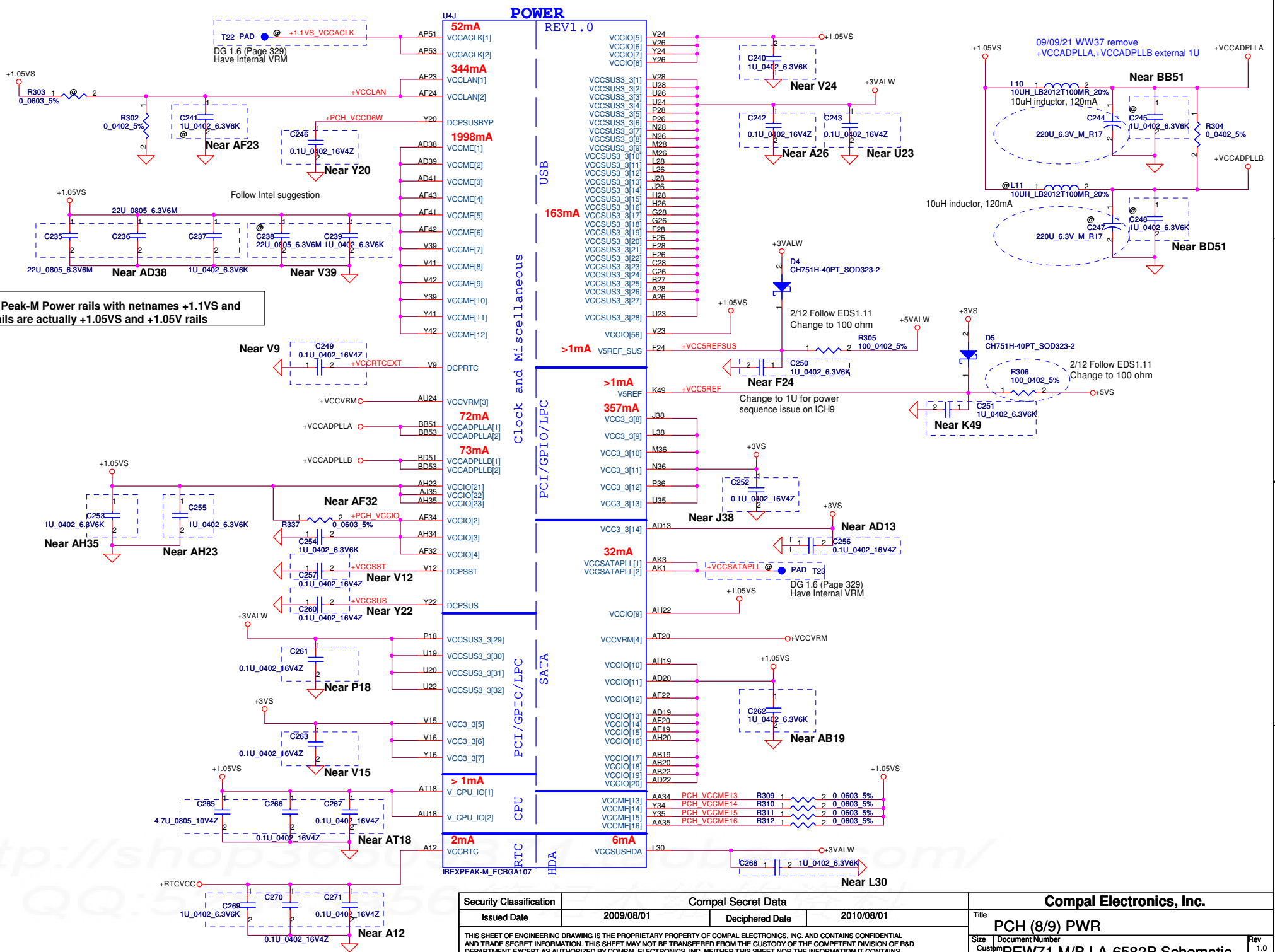
Change to 0.0805_5% 20090923

Change to 0.0402 20090914

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title PCH (7/9) PWR	
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Date:	Thursday, July 08, 2010	Sheet	19	of	48

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QQ:52643956

All Ibox Peak-M Power rails with netnames +1.1VS and +1.1V rails are actually +1.05VS and +1.05V rails



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Compal Electronics, Inc.			
Title: PCH (8/9) PWR			
Size	Document Number	Rev	
Customer	PEW71 M/B LA-6582P Schematic	1.0	
Date:	Thursday, July 08, 2010	Sheet	20 of 48

U4I	VSS	H49
AY7	VSS159	H5
B11	VSS160	H5
B15	VSS161	J24
B19	VSS162	K11
B23	VSS163	K43
B31	VSS164	K47
B35	VSS165	K47
B39	VSS165	L14
B43	VSS166	L18
B47	VSS167	L2
B7	VSS168	L2
B7	VSS169	L22
BG12	VSS170	L32
BB12	VSS171	L36
BB16	VSS172	L40
BB20	VSS172	L52
BB24	VSS173	M12
BB30	VSS174	M16
BB34	VSS175	M20
BB34	VSS176	M20
BB38	VSS177	M38
BB42	VSS178	M38
BB49	VSS178	M38
BB5	VSS179	M42
BC10	VSS180	M46
BC14	VSS181	M49
BC18	VSS182	M5
BC2	VSS183	M8
BC22	VSS184	N24
BC32	VSS185	P11
BC36	VSS186	P22
BC40	VSS187	P22
BC44	VSS188	P30
BC52	VSS189	P32
BH9	VSS190	P34
BD48	VSS191	P42
BD49	VSS192	P45
BD5	VSS193	P47
BE12	VSS194	R2
BE16	VSS195	R52
BE20	VSS196	T12
BE24	VSS197	T41
BE30	VSS198	T46
BE34	VSS199	T49
BE38	VSS200	T5
BE42	VSS201	T8
BE46	VSS202	T30
BE46	VSS203	U30
BE48	VSS204	U31
BE50	VSS204	U32
BE6	VSS205	U34
BE8	VSS206	P38
BE3	VSS207	V11
BF49	VSS208	V19
BF51	VSS209	V19
BG18	VSS210	V20
BG24	VSS211	V22
BG4	VSS212	V30
BG50	VSS213	V31
BH11	VSS214	V32
BH15	VSS215	V34
BH19	VSS216	V35
BH23	VSS217	V38
BH31	VSS218	V43
BH35	VSS219	V45
BH39	VSS220	V46
BH43	VSS221	V47
BH47	VSS222	V49
BH7	VSS223	V5
C12	VSS224	V7
C50	VSS225	V8
D51	VSS226	W2
E12	VSS227	W52
E16	VSS228	Y11
E20	VSS229	Y12
E24	VSS230	Y15
E30	VSS231	Y19
E34	VSS232	Y23
E38	VSS233	Y28
E42	VSS234	Y28
E46	VSS235	Y30
E48	VSS236	Y31
E6	VSS237	Y32
E8	VSS238	Y38
F49	VSS239	Y43
F5	VSS240	Y46
G10	VSS241	P49
G14	VSS242	V5
G18	VSS243	V6
G2	VSS244	V8
G22	VSS245	P24
G32	VSS246	T43
G36	VSS247	AD51
G40	VSS248	ATR
G44	VSS249	AD47
G52	VSS250	Y47
H16	VSS251	AT12
H20	VSS252	AM6
H30	VSS253	AT13
H34	VSS254	AM5
H38	VSS255	AK45
H42	VSS256	AK39
	VSS257	AV14
	VSS258	

REV1.0

IBEXPEAK-M_FCBGA107

U4H	VSS	AK30
AB16	VSS0	AK30
AA19	VSS1	AK31
AA20	VSS2	AK32
AA22	VSS3	AK34
AA19	VSS4	AK35
AA24	VSS5	AK38
AA26	VSS6	AK43
AA28	VSS7	AK46
AA30	VSS8	AK49
AA31	VSS9	AK5
AA32	VSS10	AK6
AB11	VSS11	AK8
AB15	VSS12	AL2
AB23	VSS13	AL52
AB30	VSS14	AM11
AB31	VSS15	BB44
AB32	VSS16	AD24
AB38	VSS17	AM20
AB4	VSS18	AM22
AB47	VSS19	AM24
AB5	VSS20	AM26
AB8	VSS21	AM28
AC2	VSS22	BA42
AC52	VSS23	AM30
AD11	VSS24	AM31
AD12	VSS25	AM32
AD16	VSS26	AM34
AD23	VSS27	AM35
AD30	VSS28	AM38
AD31	VSS29	AM39
AD32	VSS30	AM42
AD34	VSS31	U20
AD42	VSS32	AM46
AD44	VSS33	AV22
AD46	VSS34	AM49
AD49	VSS35	AM7
AD7	VSS36	AA50
AE2	VSS37	BB10
AE4	VSS38	AN32
AE12	VSS39	AN50
Y13	VSS40	AN52
AH49	VSS41	AP12
AU4	VSS42	AP42
AF35	VSS43	AP46
AF13	VSS44	AP49
AF45	VSS45	AP5
AF46	VSS46	AP8
AF49	VSS47	AR2
AF5	VSS48	AR52
AF8	VSS49	AT11
AF9	VSS50	BA12
AG2	VSS51	AH48
AG52	VSS52	AT32
AH11	VSS53	AT36
AH15	VSS54	AT41
AH16	VSS55	AT47
AH24	VSS56	AT7
AH32	VSS57	AV12
AV18	VSS58	AV16
AH43	VSS59	AV20
AH47	VSS60	AV24
AH7	VSS61	AV30
AJ19	VSS62	AV34
AJ2	VSS63	AV38
AJ20	VSS64	AV42
AJ22	VSS65	AV46
AJ23	VSS66	AV49
AJ26	VSS67	AV5
AJ28	VSS68	AV8
AJ32	VSS69	AW14
AJ34	VSS70	AW18
AT5	VSS71	AW2
AJ4	VSS72	BF9
AK12	VSS73	AW32
AM41	VSS74	AW36
AN19	VSS75	AW40
AK26	VSS76	AW52
AK22	VSS77	AY11
AK23	VSS78	AY43
AK28	VSS79	AY47
	VSS158	

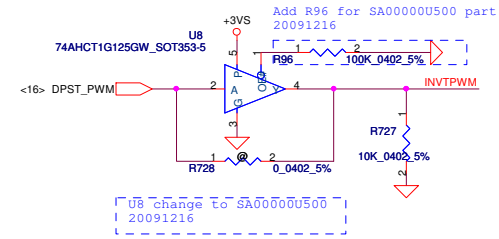
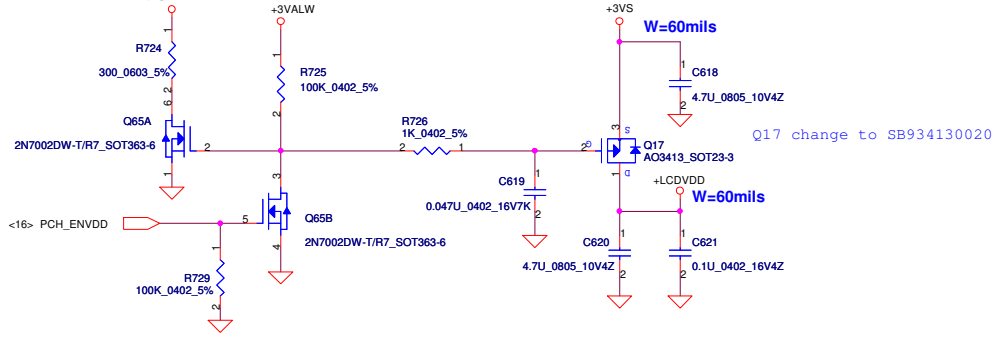
REV1.0

IBEXPEAK-M_FCBGA107

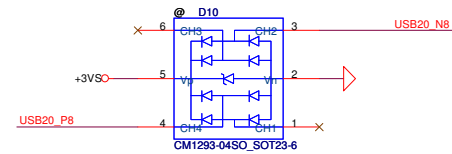
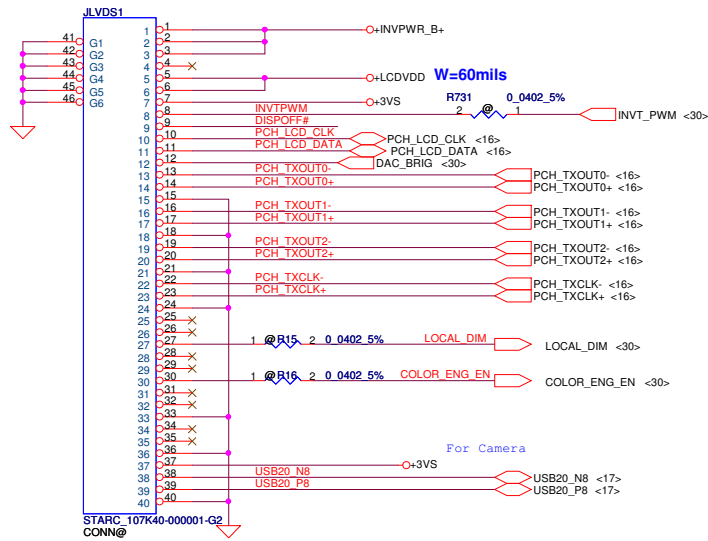
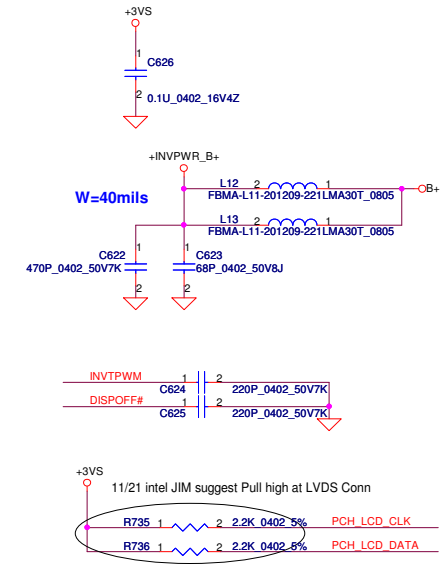
Del PCH XDP

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Size	Document Number	Date		Rev	1.0
Customer	PEW71 M/B LA-6582P Schematic	Thursday, July 08, 2010		Sheet	21 of 48

LCD POWER CIRCUIT



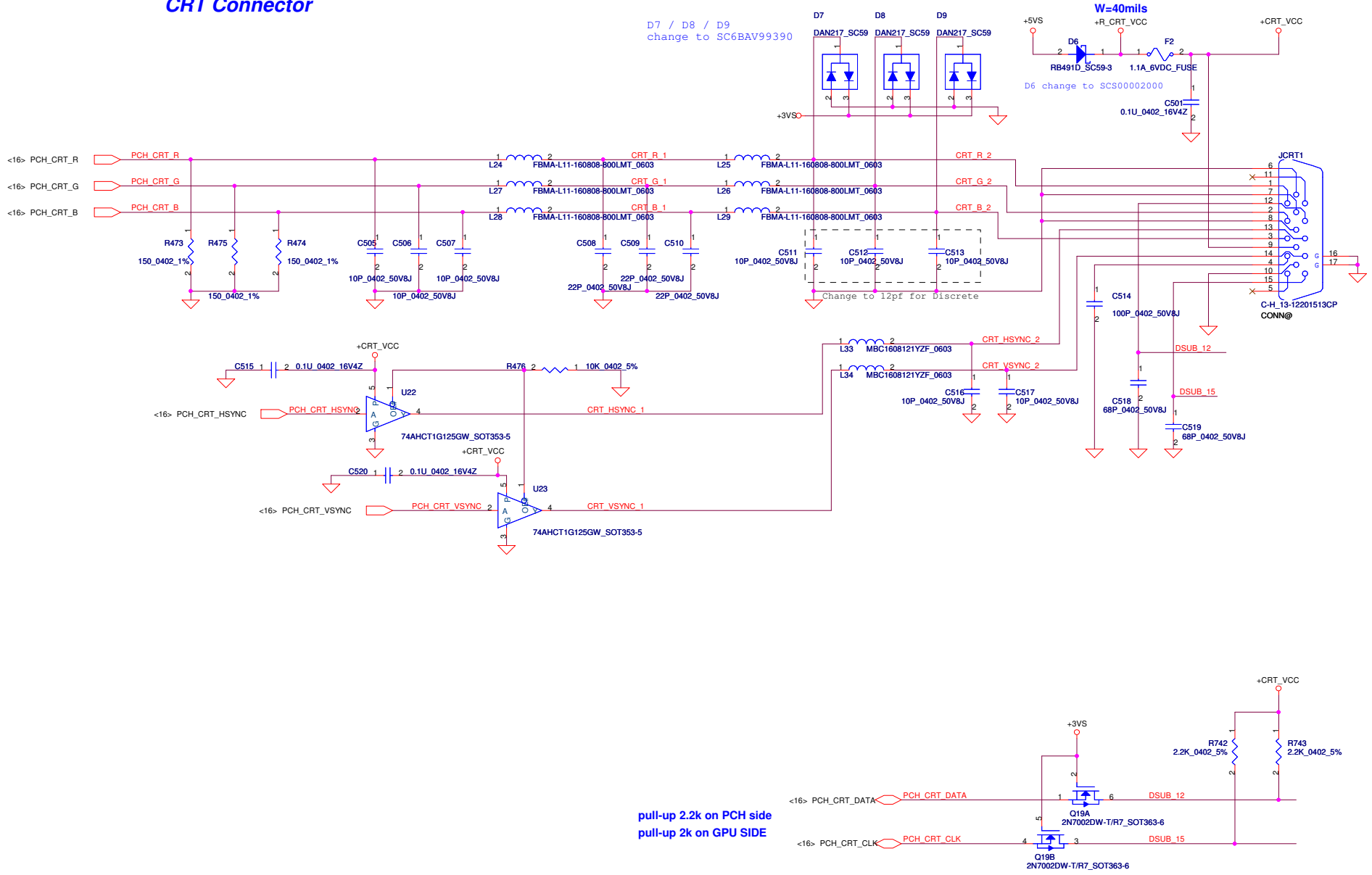
LED PANEL Conn.



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Size	Document Number	Customer	Rev	Date	
	PEW71 M/B LA-6582P Schematic		1.0	Thursday, July 08, 2010	
				Sheet	22 of 48

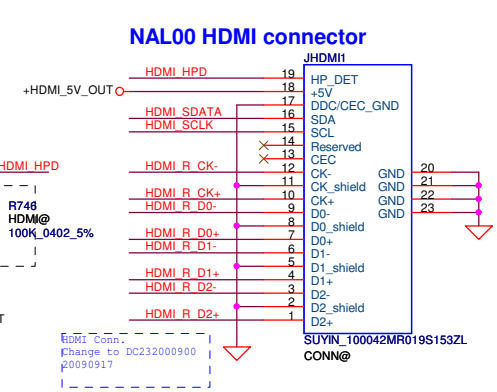
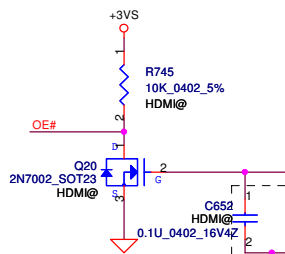
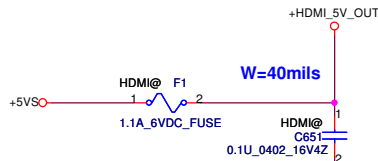
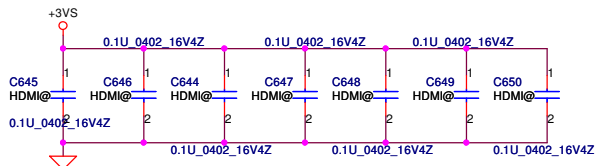
CRT Connector



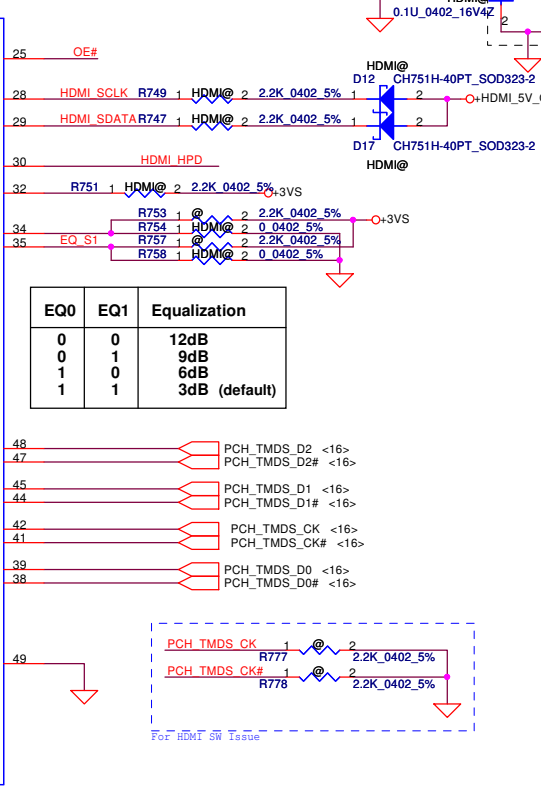
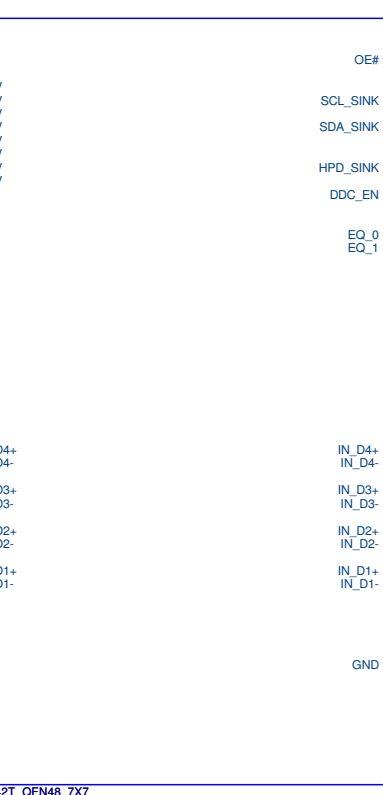
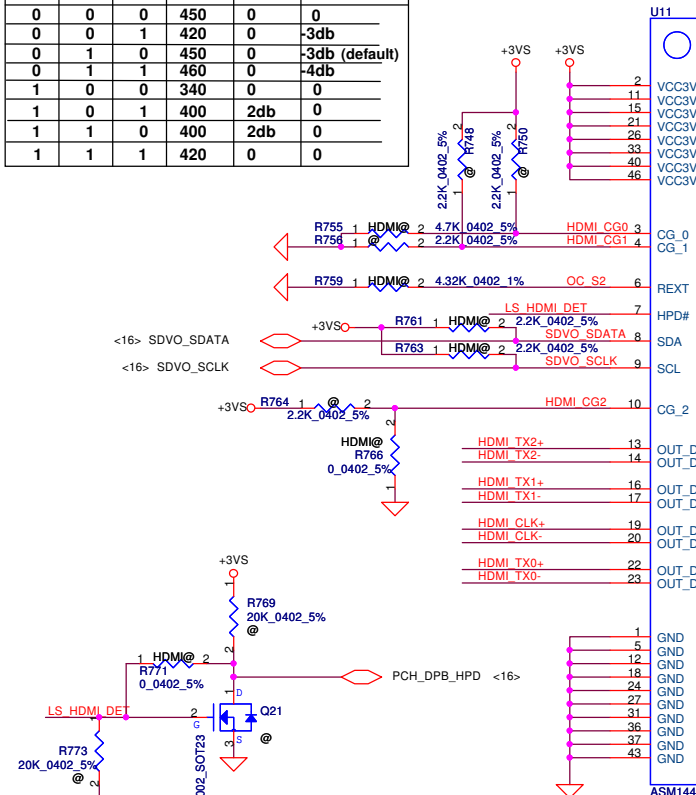
pull-up 2.2k on PCH side
pull-up 2k on GPU SIDE

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QQ:52643956

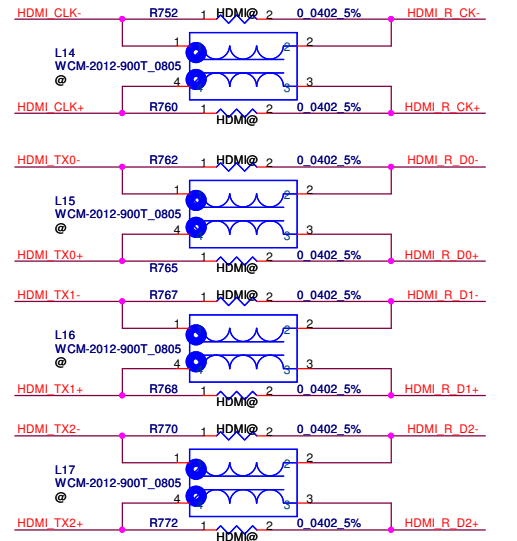
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Issued Date	2009/5/12	Deciphered Date	2010/04/15	Title		
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Size B	Document Number	Date		Thursday, July 08, 2010	Sheet	23 of 48
	PEW71 M/B LA-6582P Schematic	Rev	1.0			



CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0



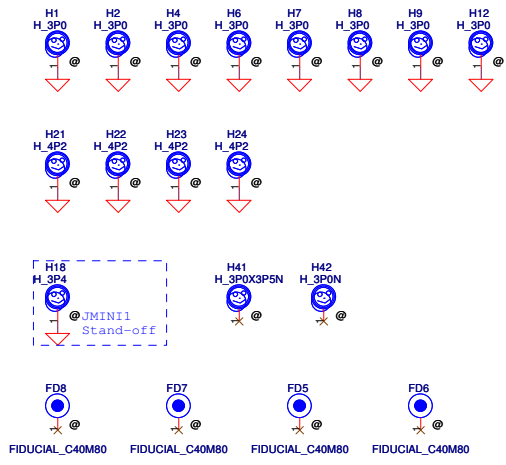
EQ0	EQ1	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB (default)



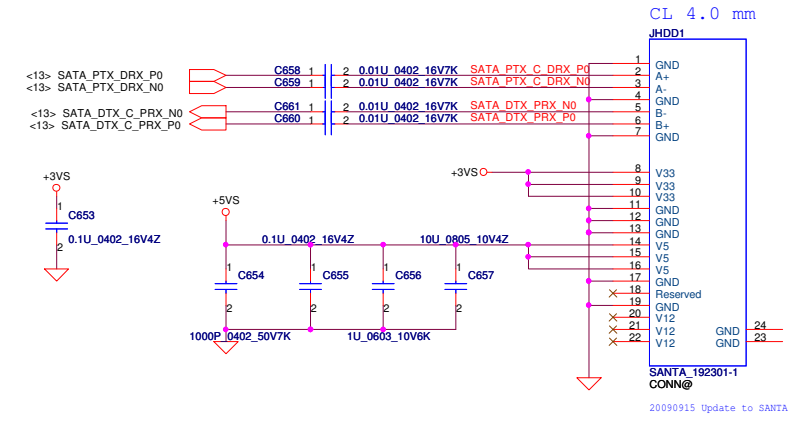
Change to TI P/N: SA00003DS00
20100608

<http://shop36609371.taobao.com/>
QQ:52641956

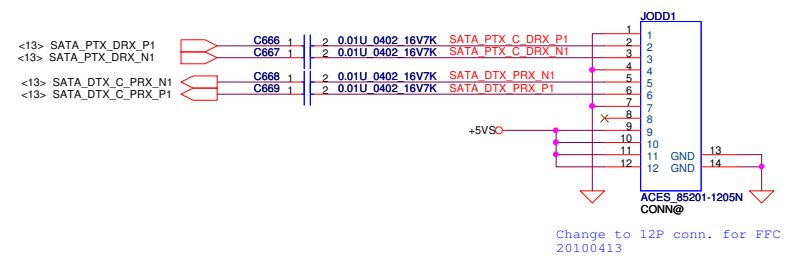
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Issued Date	2009/4/15	Deciphered Date	2010/04/15	Title	
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Size	Document Number	PEW71 M/B LA-6582P Schematic		Rev	1.0
Customer	Date	Thursday, July 08, 2010	Sheet	24	of 48



SATA HDD1 Conn.



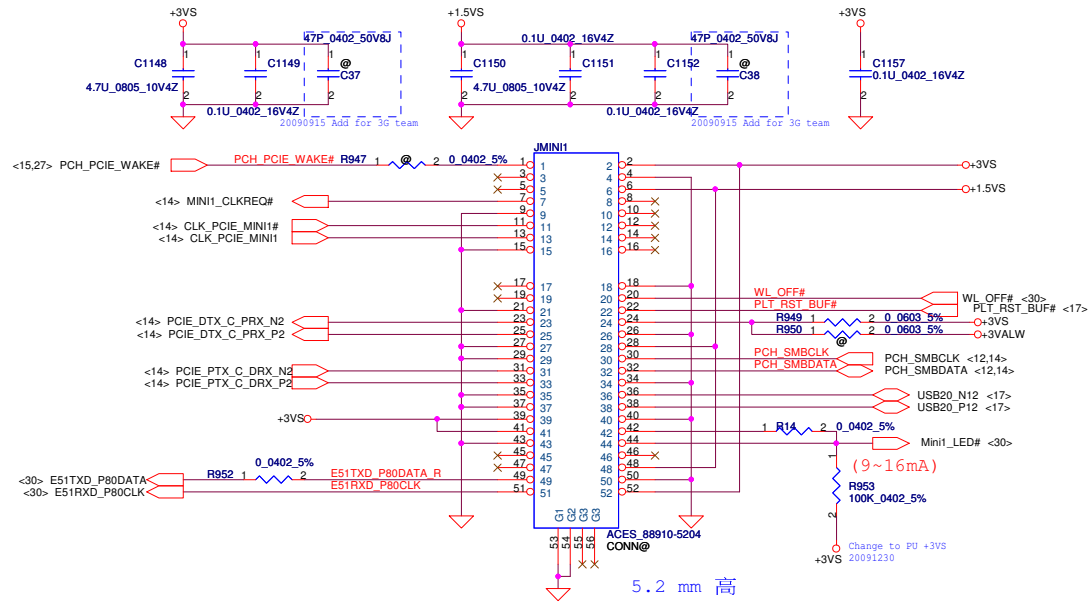
SATA ODD FFC Conn.



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				Date: Thursday, July 08, 2010	Rev 1.0
				Sheet 25	of 48

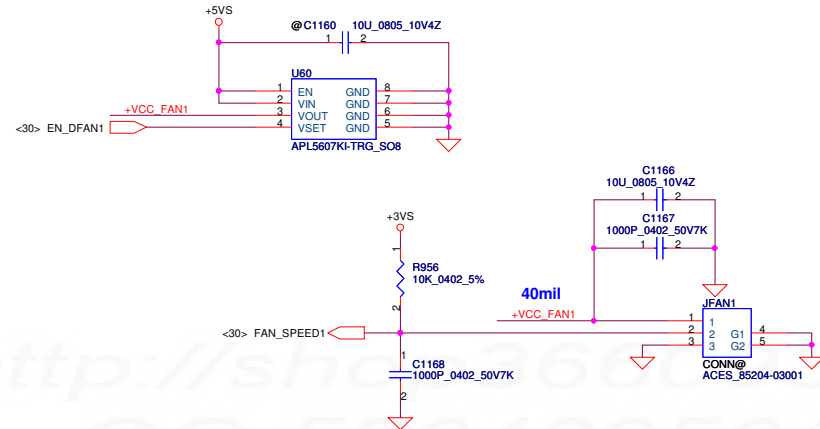
For Wireless LAN



Del 3G / GPS Module Connect

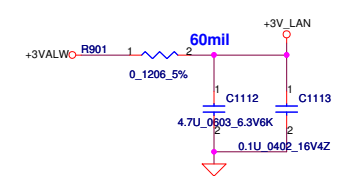
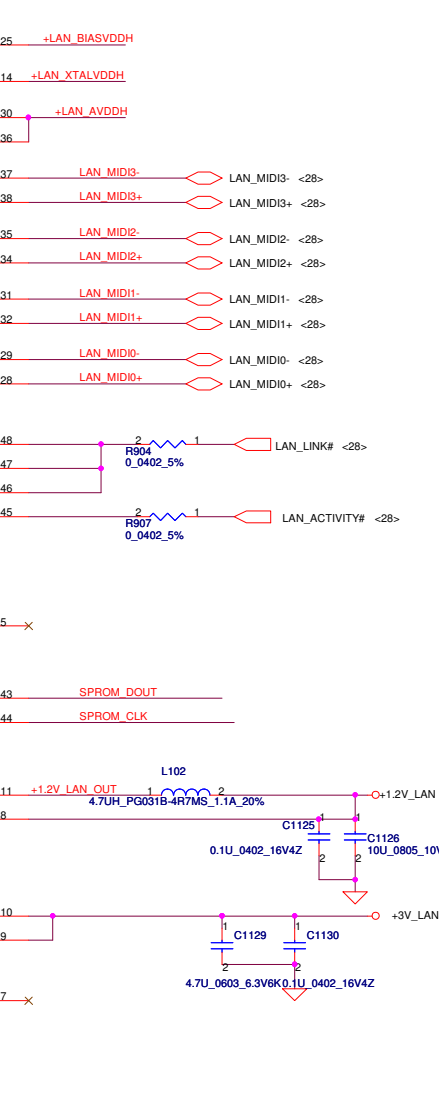
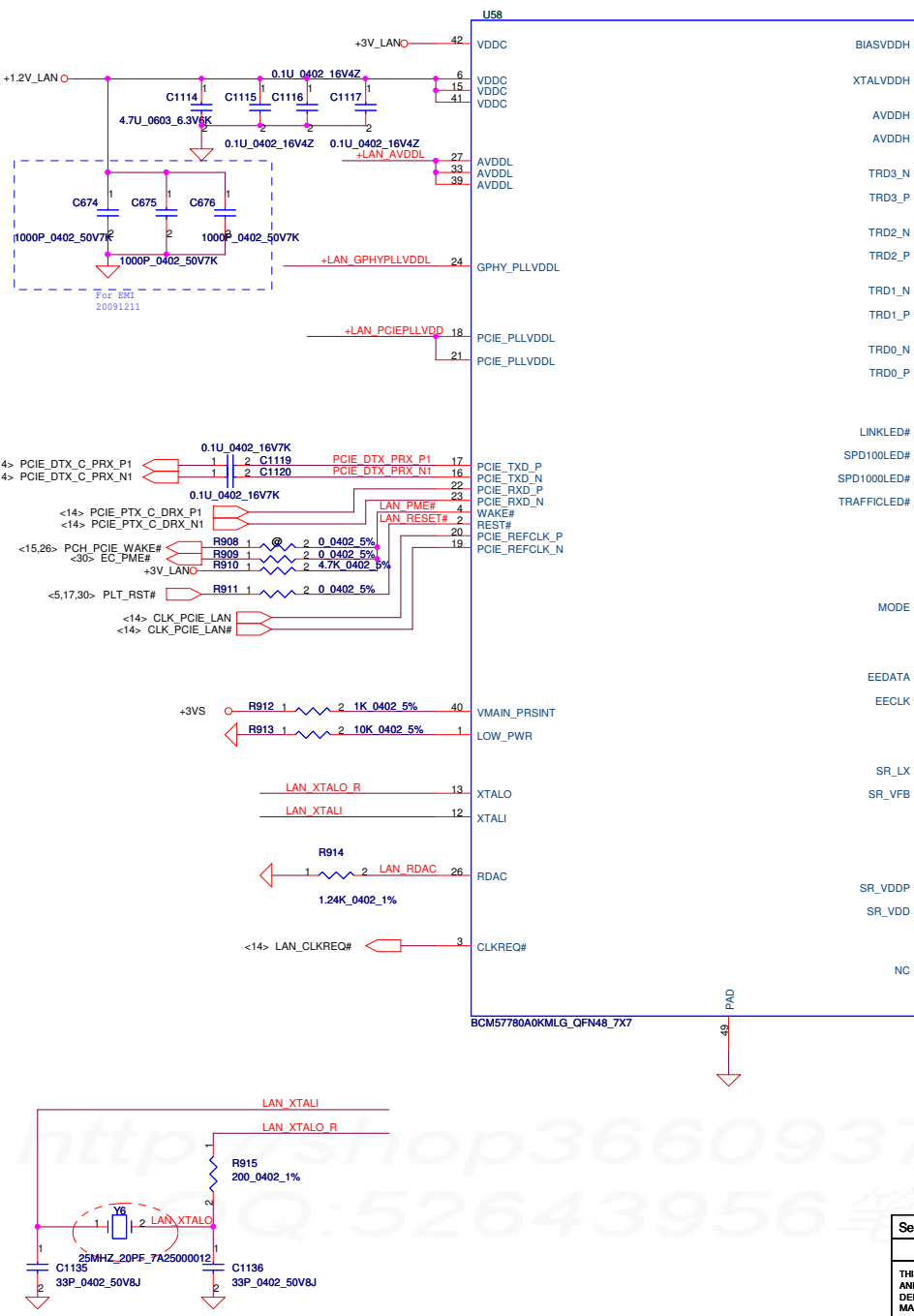
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

FAN1 Conn

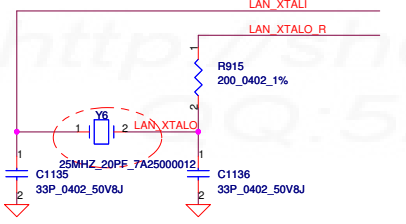
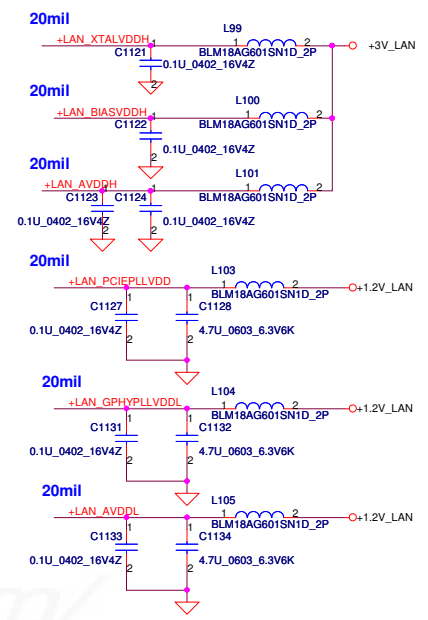
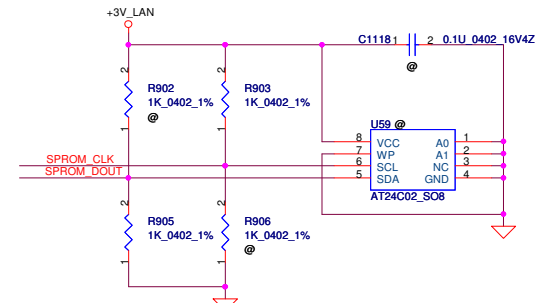


Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2009/5/12	Deciphered Date	2007/12/25	Title		
				MINI CARD (WLAN & 3G)/FAN		
Size	Document Number			Rev		
B	PEW71 M/B LA-6582P Schematic			1.0		
Date:	Thursday, July 08, 2010	Sheet	26	of	48	

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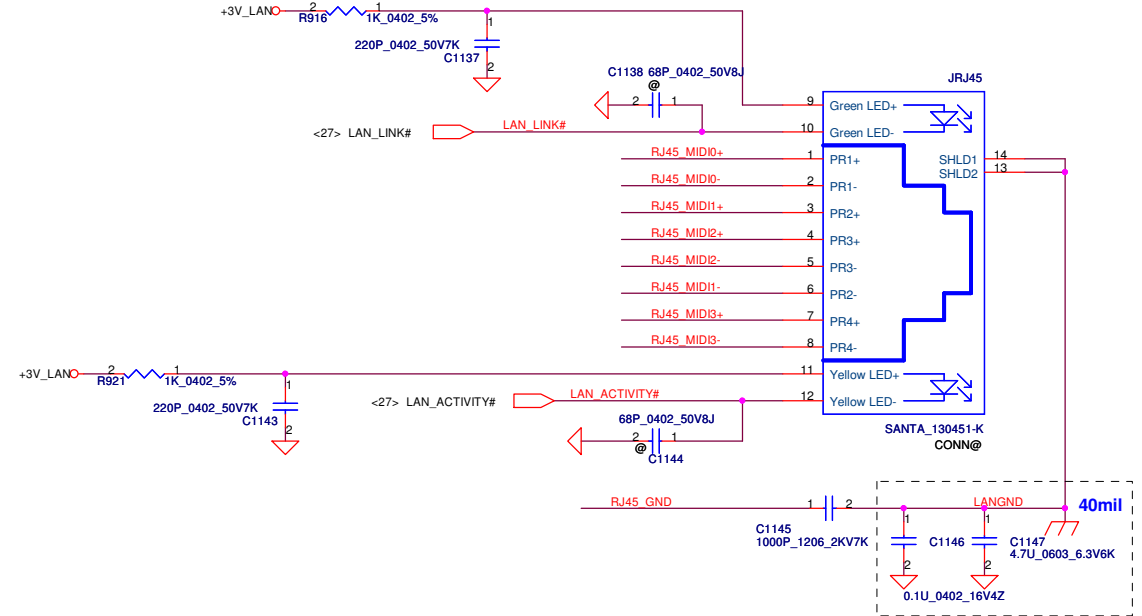
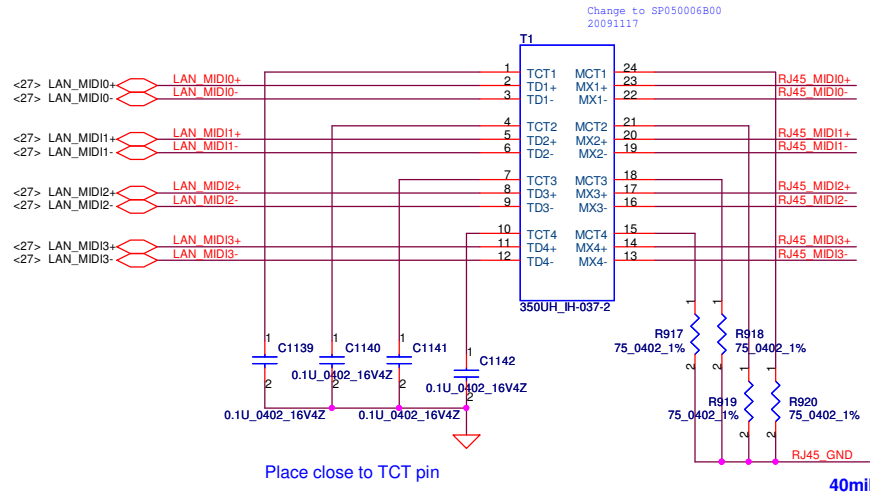


	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1



Security Classification	Compal Secret Data		Title	
Issued Date	2008/08/10	Deciphered Date	2009/08/10	Compal Electronics, Inc.
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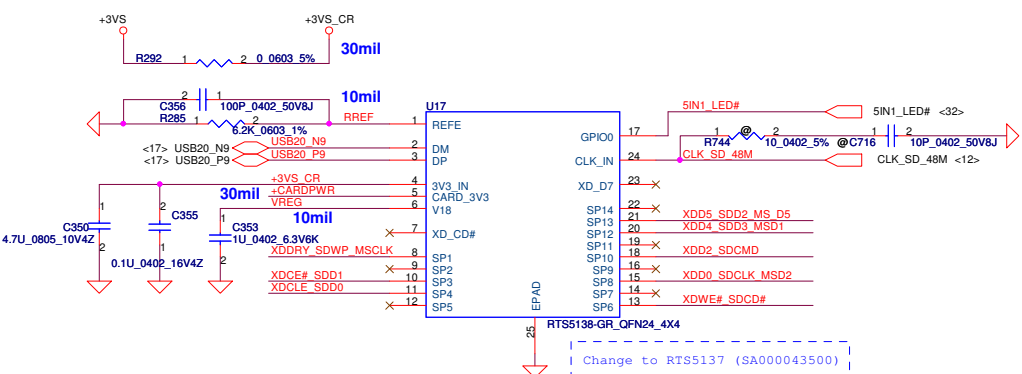
LAN Connector



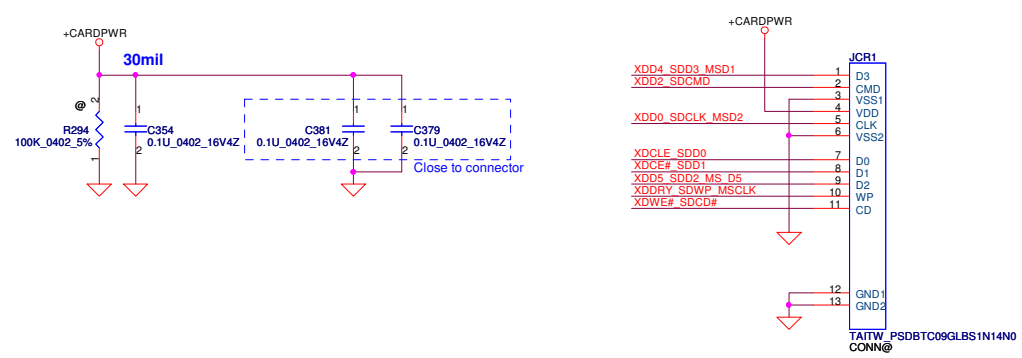
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Size	Document Number	Date		Rev	1.0
Customer	PEW71 M/B LA-6582P Schematic	Thursday, July 08, 2010		Sheet	28 of 48

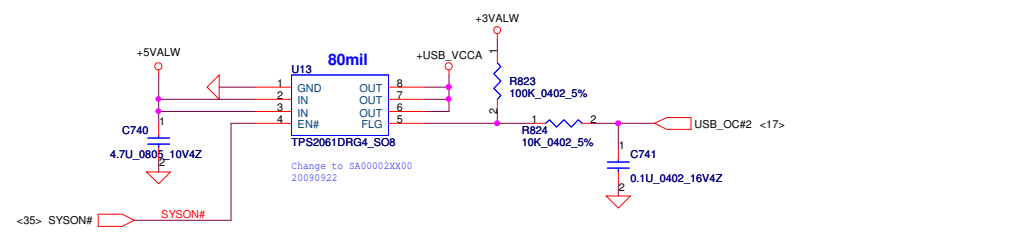
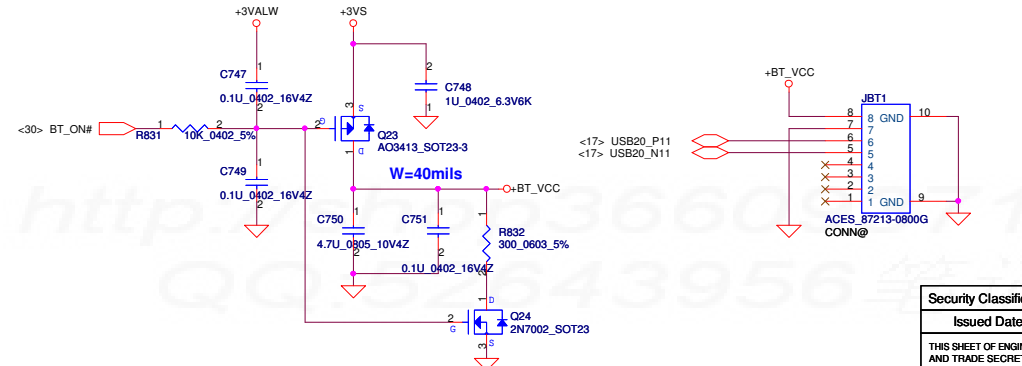
Card Reader RTS5138 / RTS5137 (only SD+MMC function)



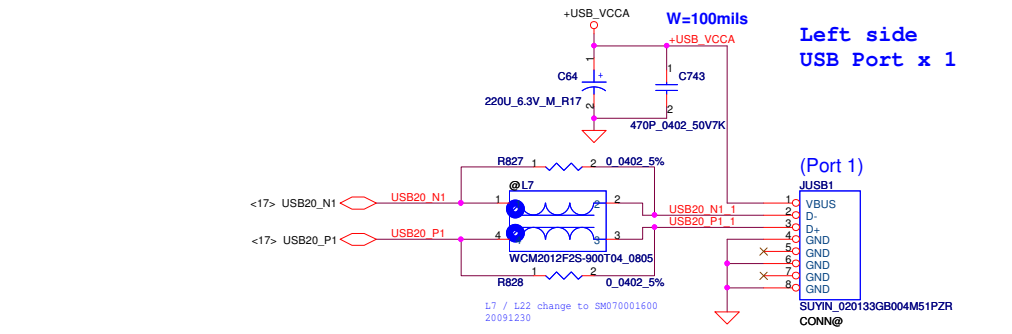
Card Reader Connector



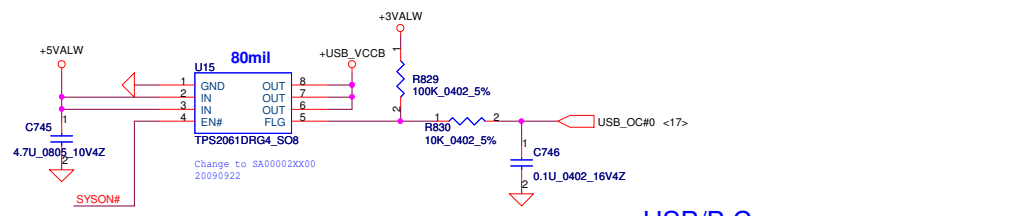
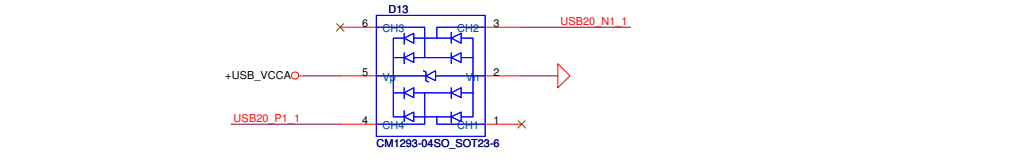
Bluetooth Conn.



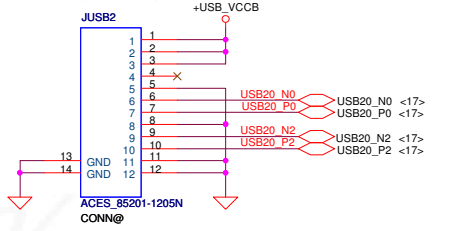
Left side USB Port x 1



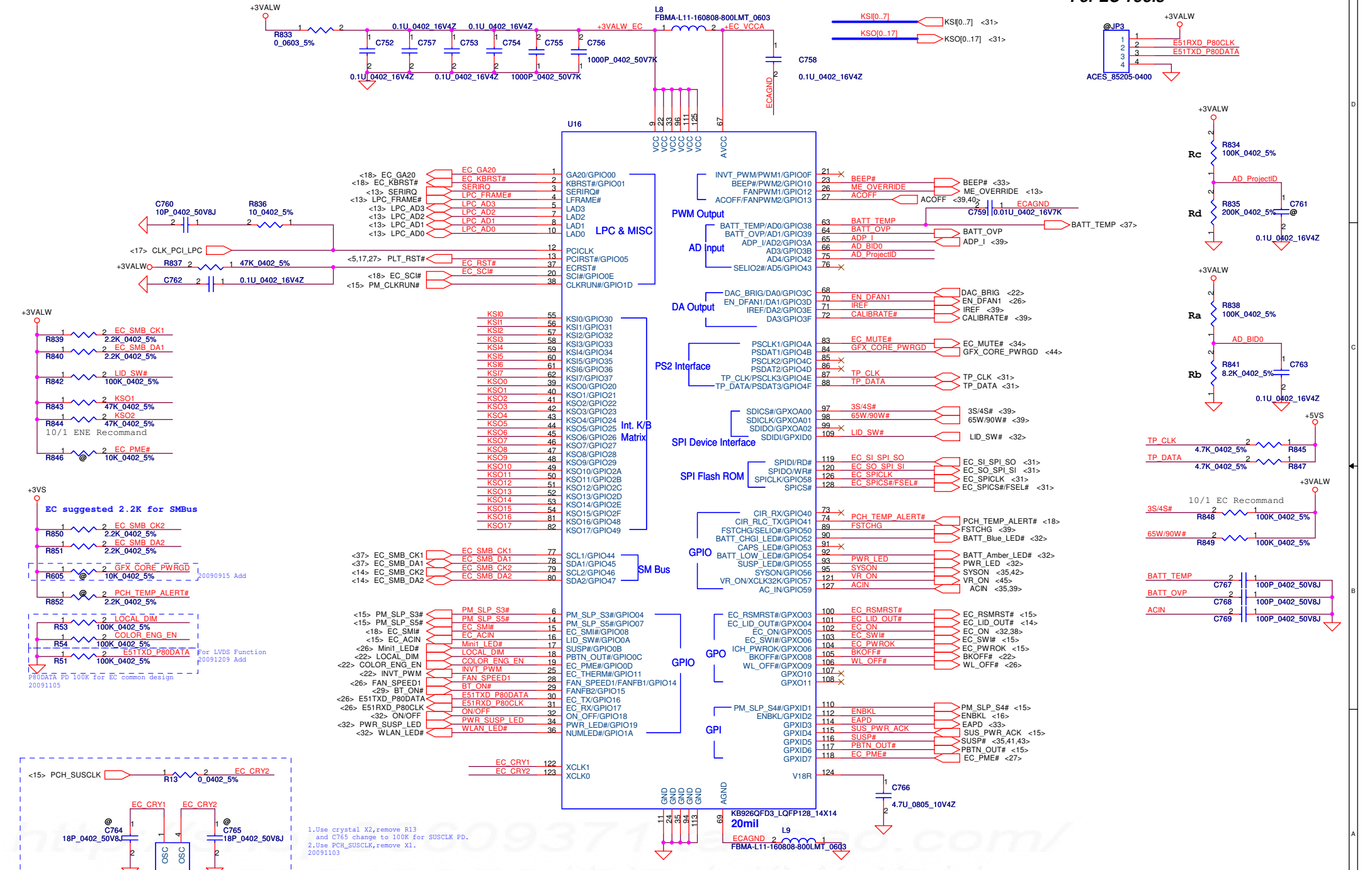
(Port 1)



USB/B Conn. (Port 0,2)



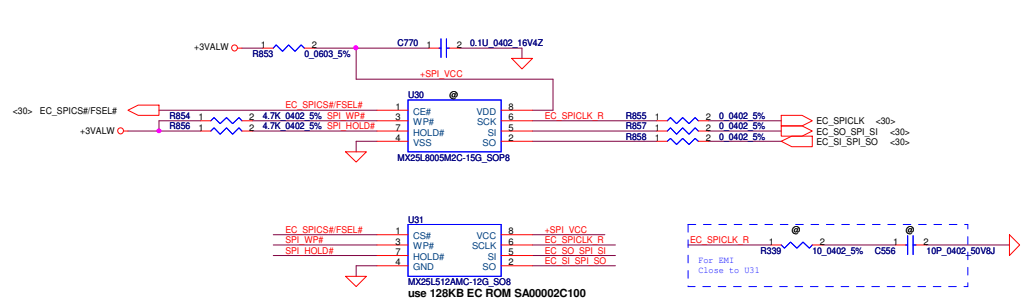
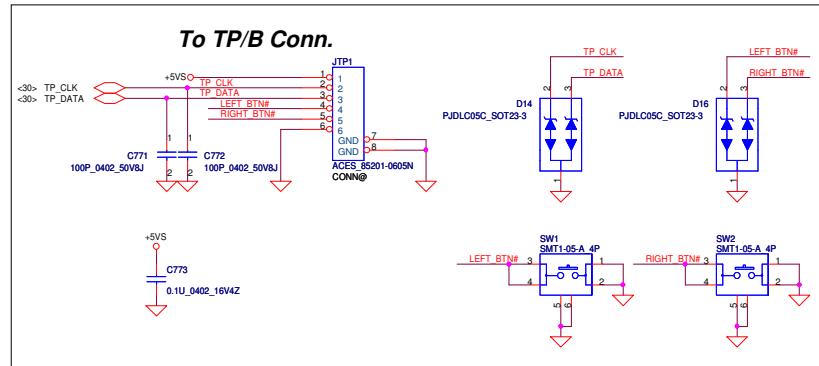
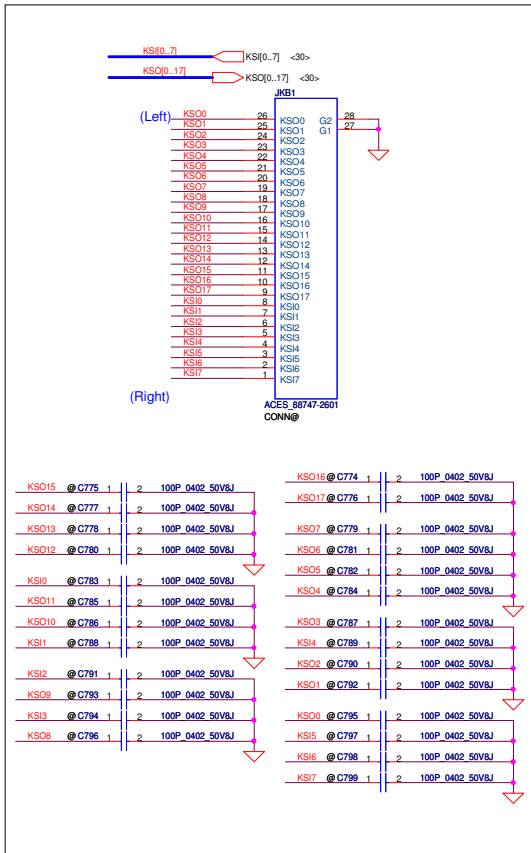
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Size	B	Document Number	PEW71 M/B LA-6582P Schematic	Rev	1.0
Date:	Thursday, July 08, 2010	Sheet	29	of	48



1. Use crystal X2, remove R13 and C765 change to 100K for SUSCLK PD.
 2. Use PCH_SUSCLK, remove X1.
 20091103

For EC SUSCLK PD 100K

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Size B	Document Number	Date		Sheet	Rev
	PEW71 M/B LA-6582P Schematic	Thursday, July 08, 2010		30	1.0



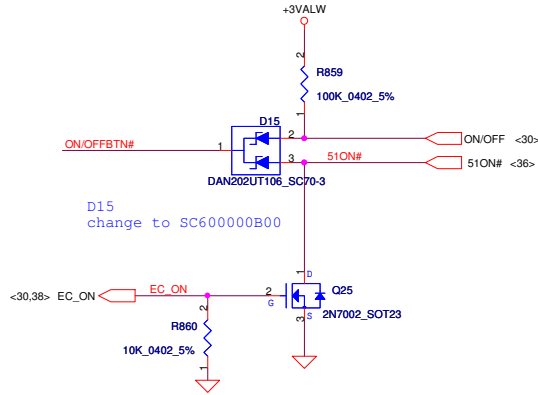
ENE suggestion SPI Frequency over 66MHz
 SST: 50MHz
 MXIC: 70MHz
 ST: 40MHz

To BTN/B Conn.

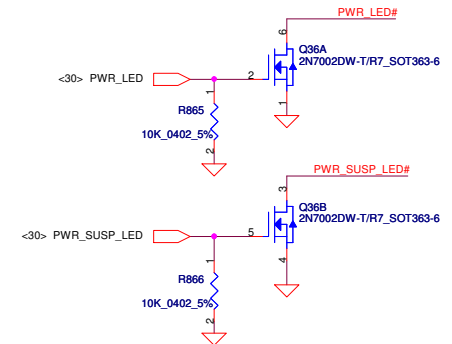
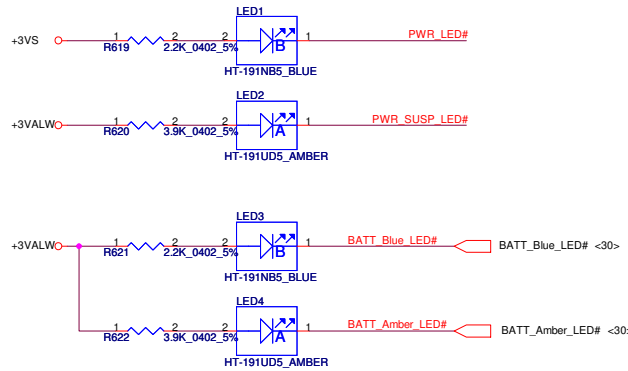
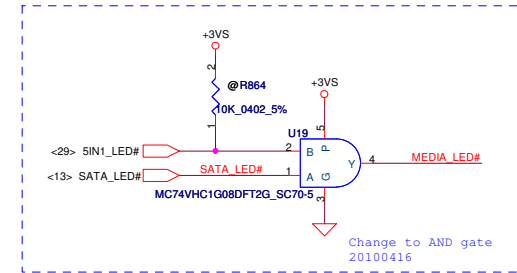
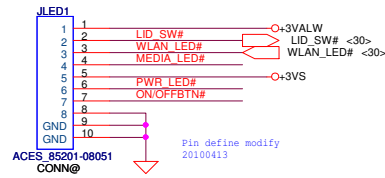
	KSO0	KSO3
KSI1	WL_BTN#	Program_BTN#
KSI2	T/P lock_BTN#	
KSI3	Back up_BTN#	Volum up_BTN#
KSI4	BT_BTN#	Volum down_BTN#
KSI5	Power save_BTN#	

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Power Button

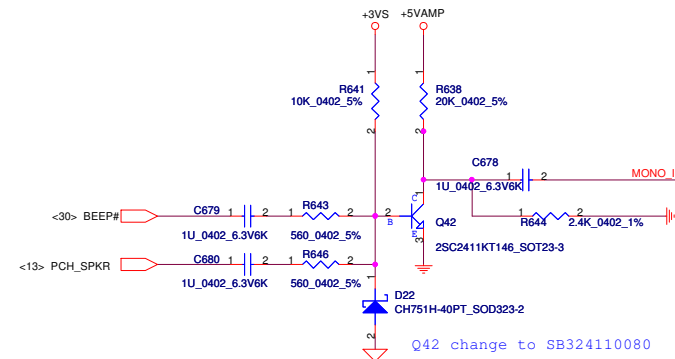
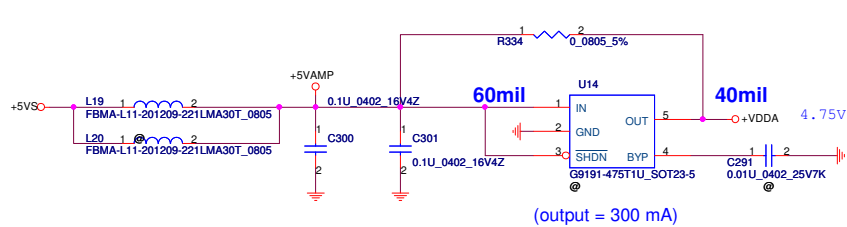


LED/B LEFT

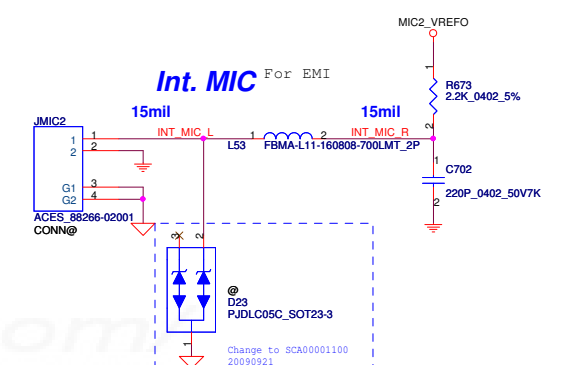
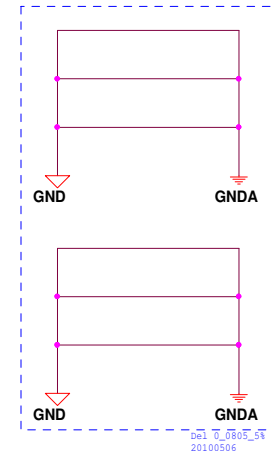
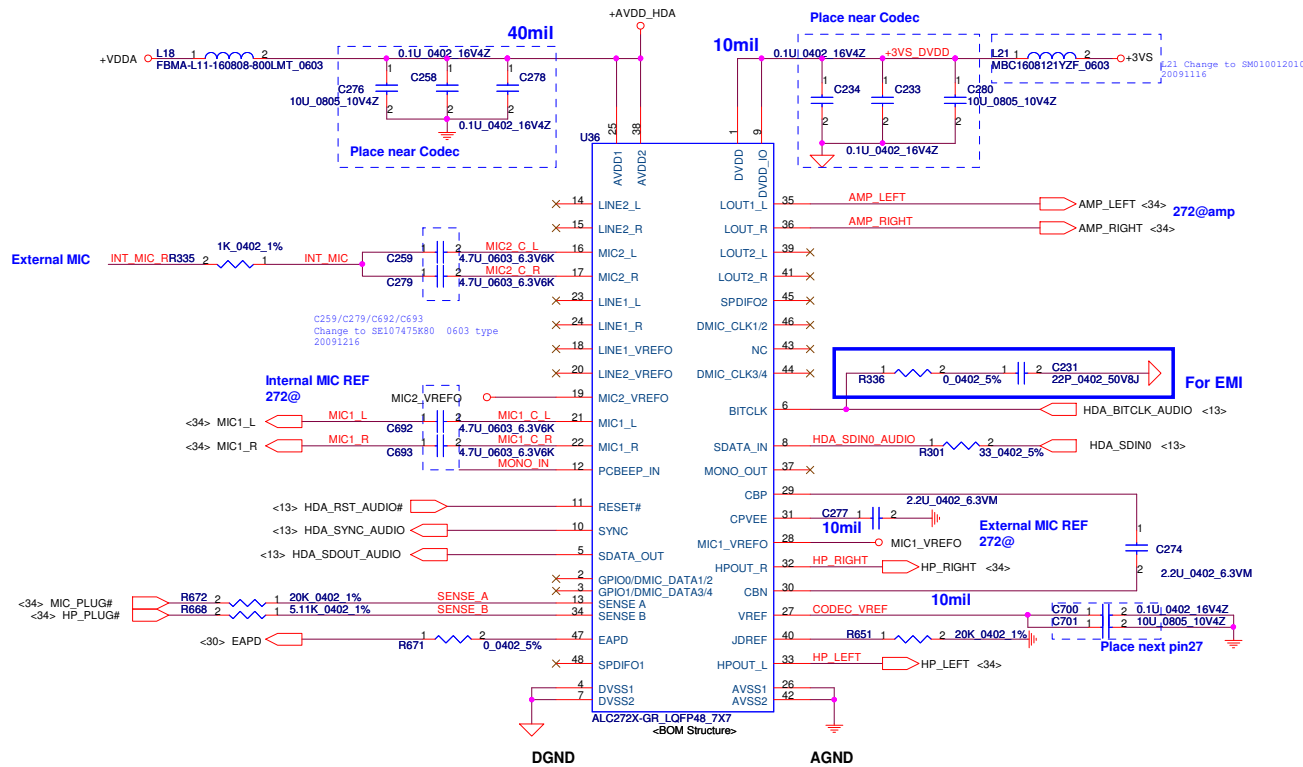


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				PEW71 M/B LA-6582P Schematic	
				Date:	Thursday, July 08, 2010
				Sheet	32 of 48
				Rev	1.0



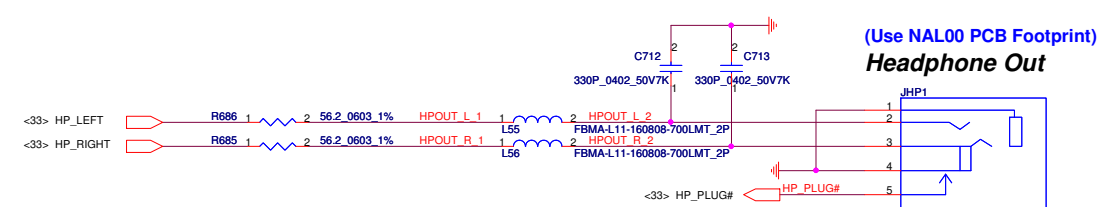
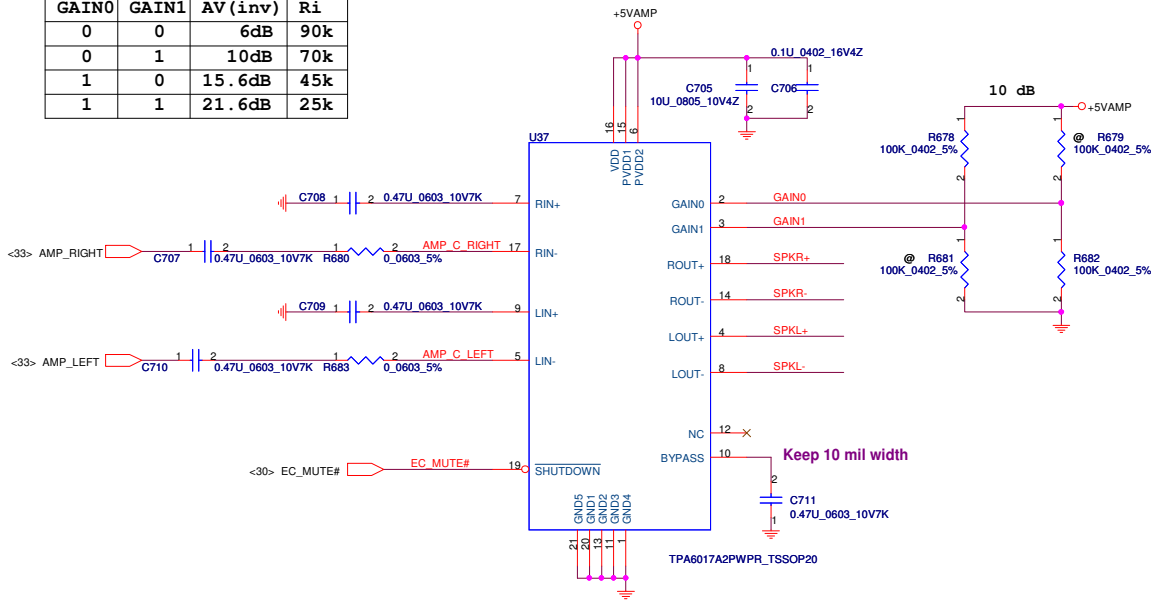
HD Audio Codec



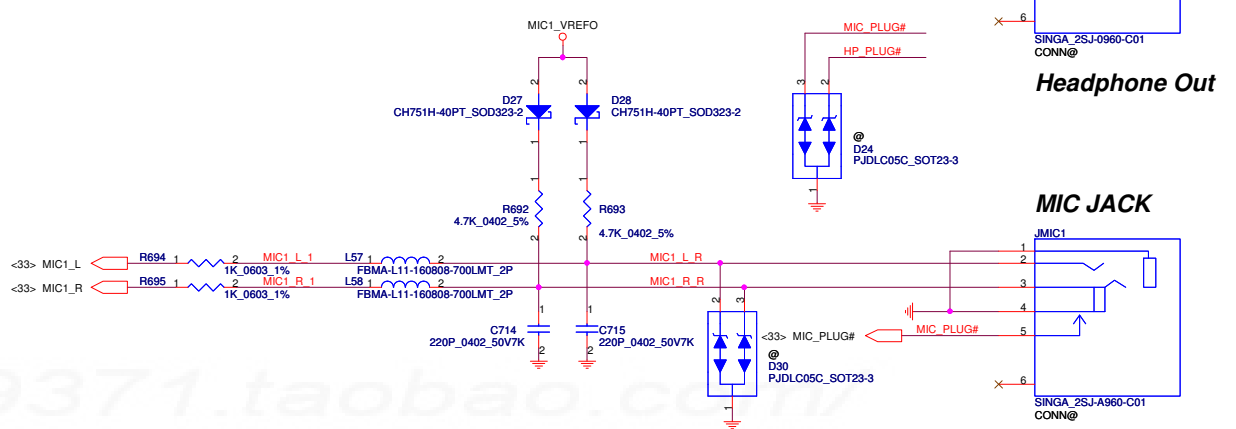
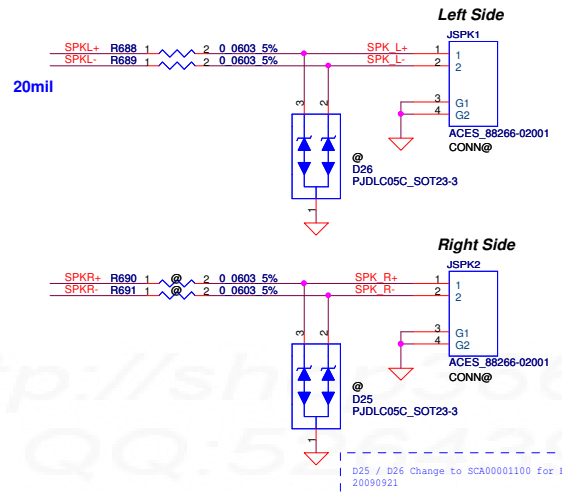
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				Customer	PEW71 M/B LA-6582P Schematic
				Date:	Thursday, July 08, 2010
				Sheet	33 of 48

GAIN0	GAIN1	AV (inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k

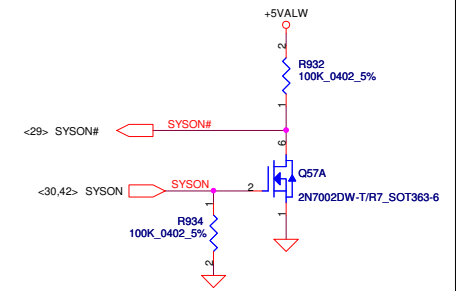
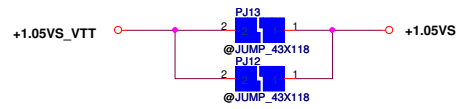
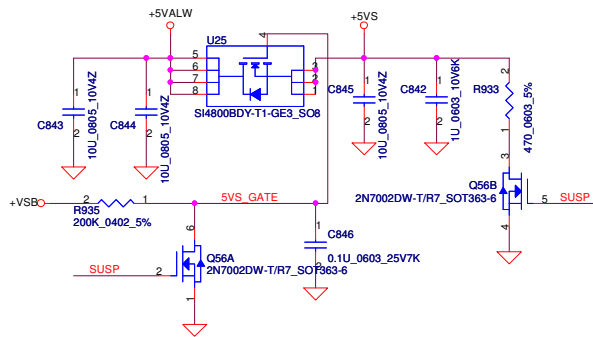


Int. Speaker Conn.

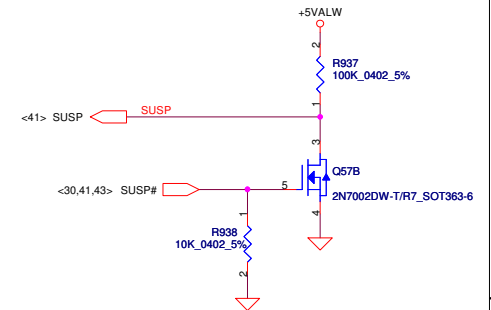
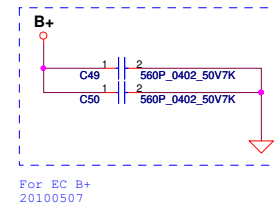
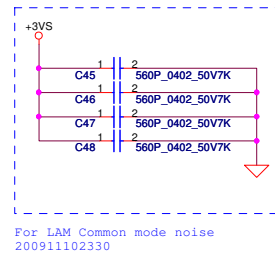
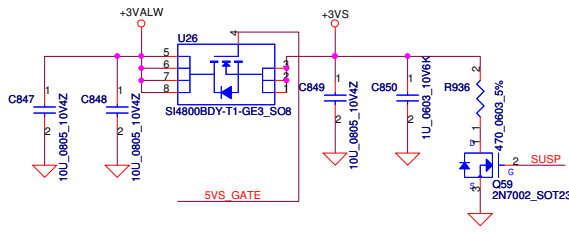


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				Customer	PEW71 M/B LA-6582P Schematic
				Date	Thursday, July 08, 2010
				Sheet	34 of 48
				Rev	1.0

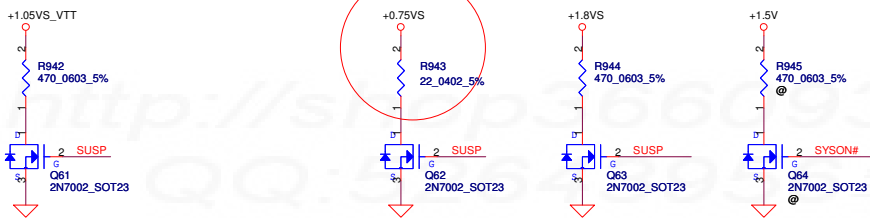
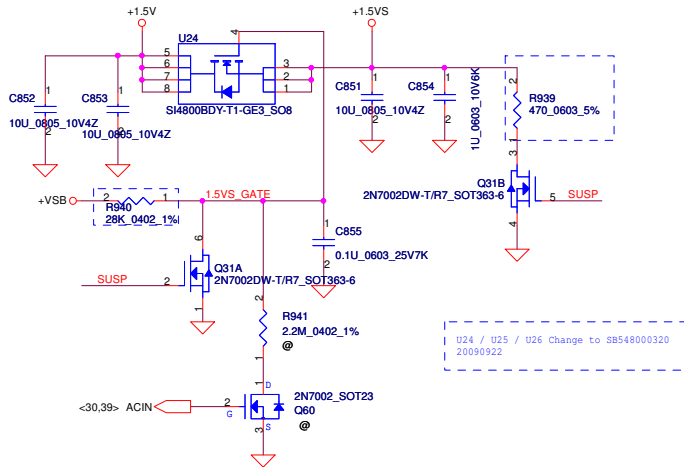
+5VALW TO +5VS



+3VALW TO +3VS

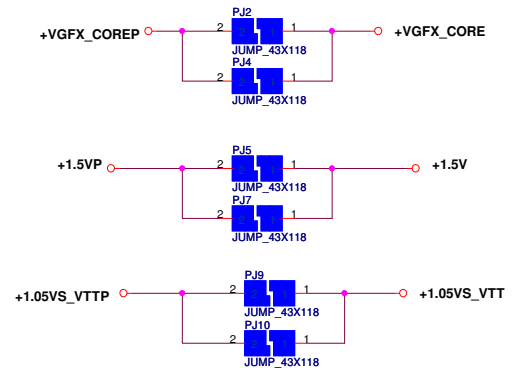
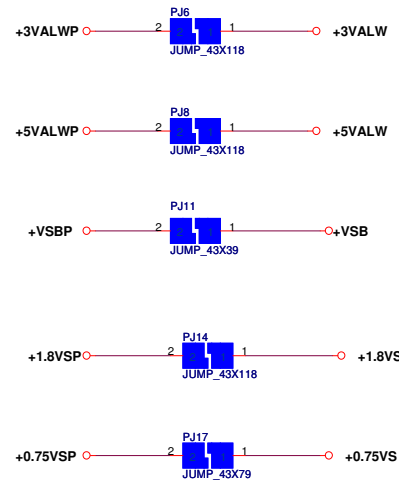
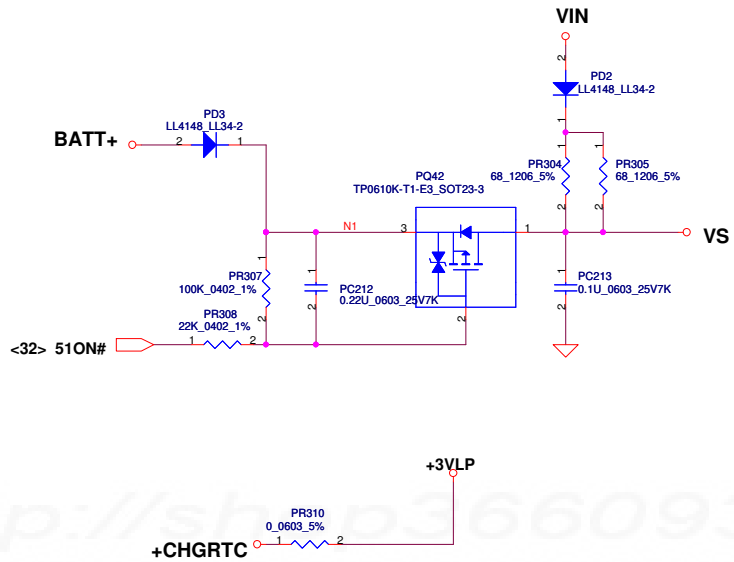
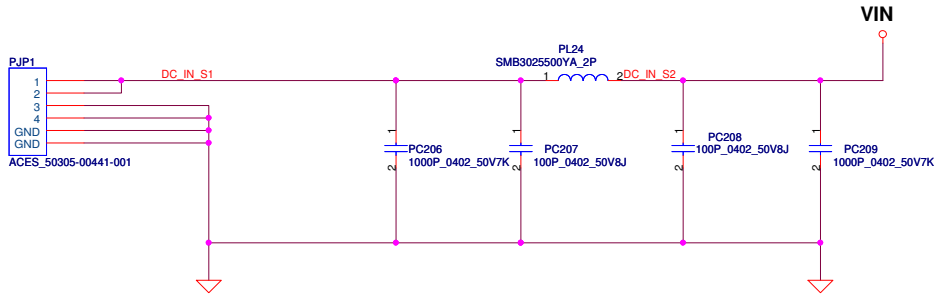


+1.5V to +1.5VS



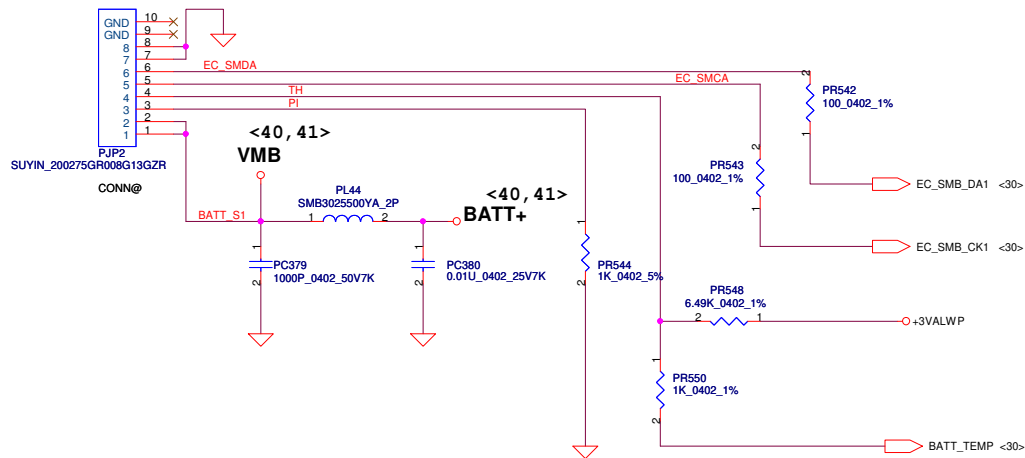
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				DC Interface	
Size B	Document Number	Date: Thursday, July 08, 2010		Rev 1.0	
				PEW71 M/B LA-6582P Schematic	
				Sheet 35 of 48	

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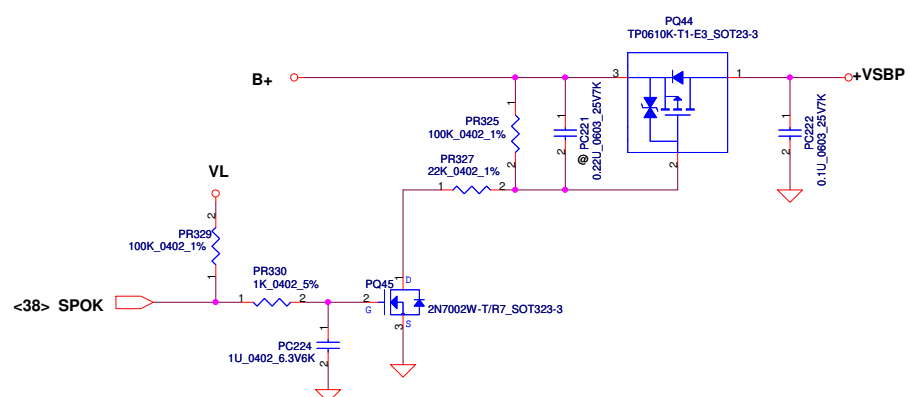
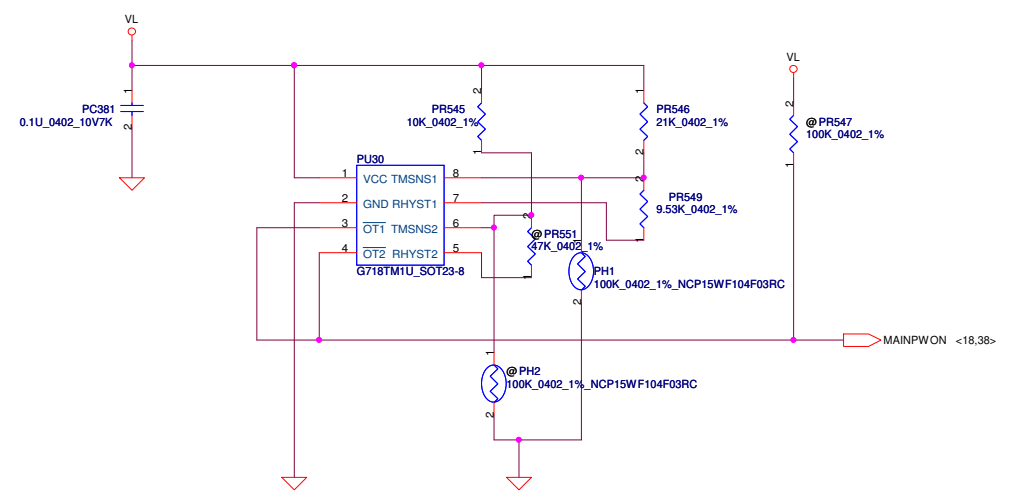


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Size	Document Number	Rev		Date	
Custom	PEW71 M/B LA-6582P Schematic	1.0		Thursday, July 08, 2010	
				Sheet	36 of 48



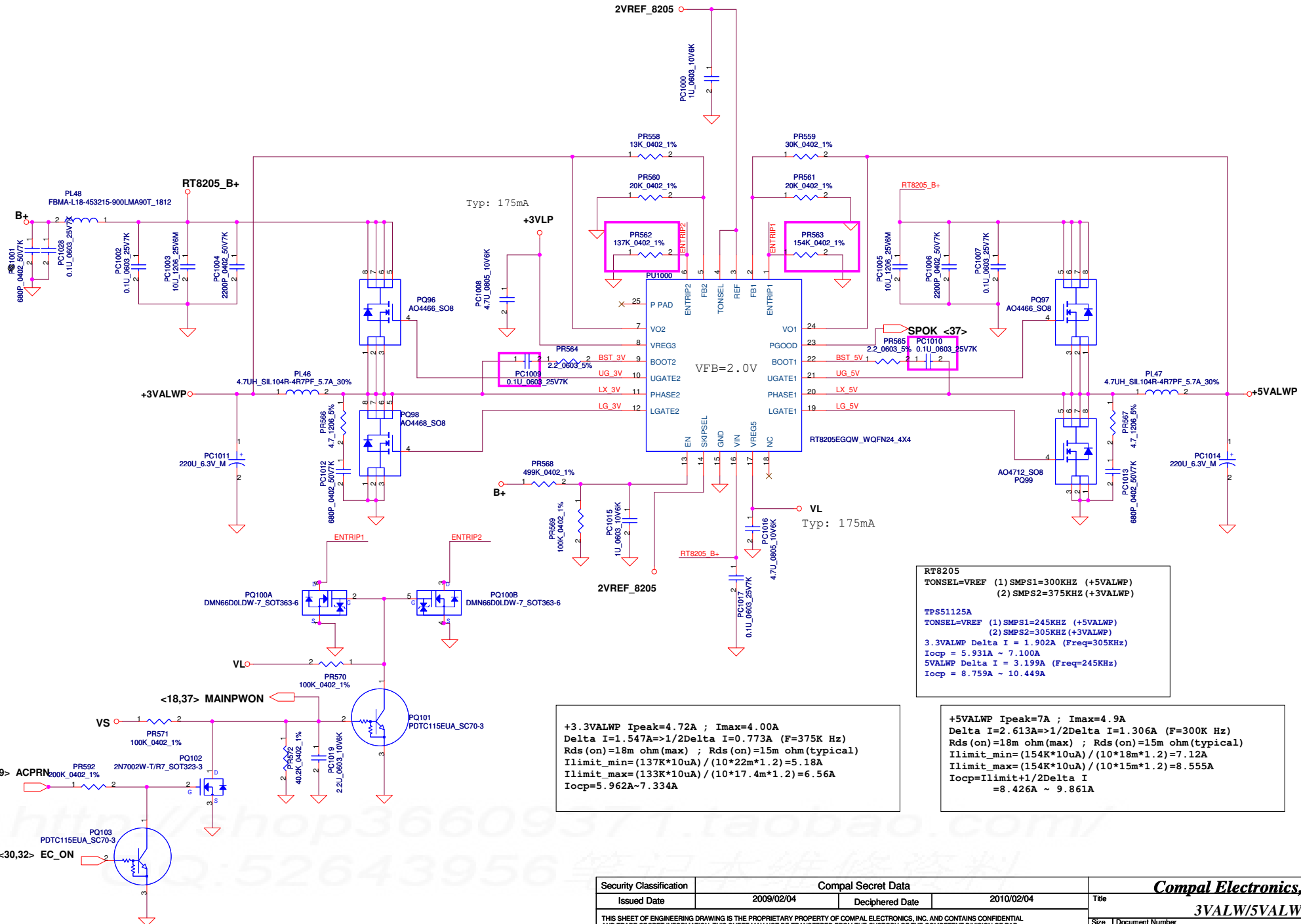
PH1 under CPU botten side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



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Size	Document Number			Rev	
Custom	PEW71 M/B LA-6582P Schematic			1.0	
Date:	Thursday, July 08, 2010	Sheet	37	of	48

Note:
 Use TPS51125 IC can remove RTC refernece LDO
 Use TPS51427 IC must keep RTC refernece LDO



Typ: 175mA

VFB=2.0V

Typ: 175mA

RT8205
 TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)
 (2) SMPS2=375KHZ (+3VALWP)

TPS51125A
 TONSEL=VREF (1) SMPS1=245KHZ (+5VALWP)
 (2) SMPS2=305KHZ (+3VALWP)
 3.3VALWP Delta I = 1.902A (Freq=305KHz)
 Iocp = 5.931A ~ 7.100A
 5VALWP Delta I = 3.199A (Freq=245KHz)
 Iocp = 8.759A ~ 10.449A

+3.3VALWP Ipeak=4.72A ; Imax=4.00A
 Delta I=1.547A=>1/2Delta I=0.773A (F=375K Hz)
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Ilimit_min=(137K*10uA)/(10*22m*1.2)=5.18A
 Ilimit_max=(133K*10uA)/(10*17.4m*1.2)=6.56A
 Iocp=5.962A~7.334A

+5VALWP Ipeak=7A ; Imax=4.9A
 Delta I=2.613A=>1/2Delta I=1.306A (F=300K Hz)
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Ilimit_min=(154K*10uA)/(10*18m*1.2)=7.12A
 Ilimit_max=(154K*10uA)/(10*15m*1.2)=8.555A
 Iocp=Ilimit+1/2Delta I
 =8.426A ~ 9.861A

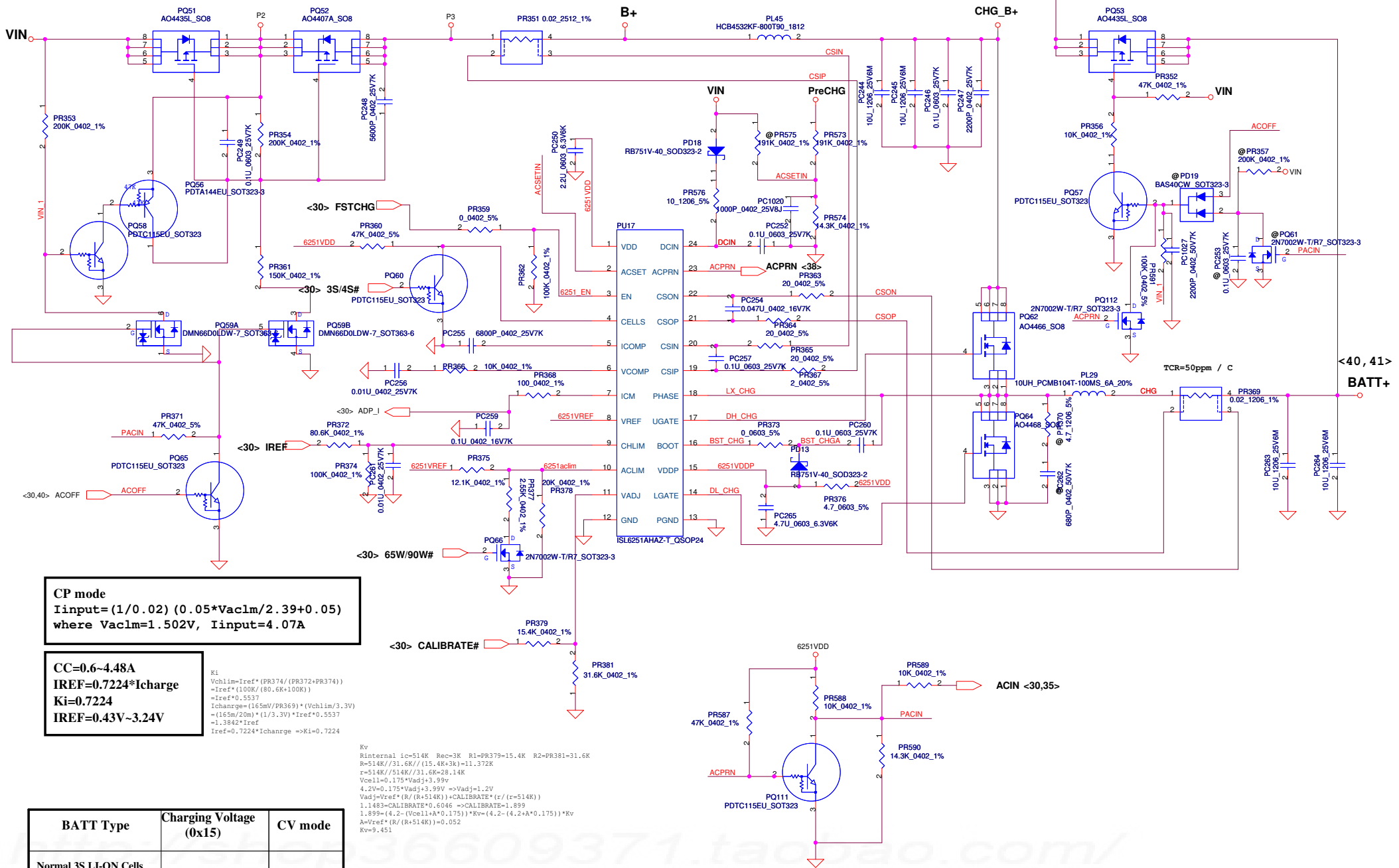
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2009/02/04	Deciphered Date			
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			Custom	PEW71 M/B LA-6582P Schematic	1.0
			Date:	Thursday, July 08, 2010	Sheet 38 of 48

Iada=0~4.74A (90W/19V=4.736A)
 Iada=0~3.42A (90W/19V=3.421A)

$$ADP_I = 19.9 * I_{adapter} * R_{sense}$$

$$CP = 85\% * I_{ada} ; CP = 4.07A$$

$$CP = 85\% * I_{ada} ; CP = 2.91A$$



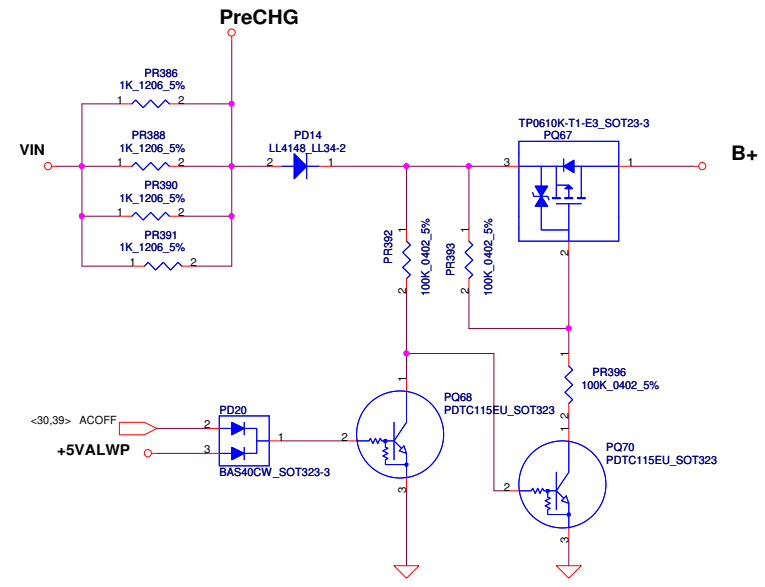
CP mode
 $I_{input} = (1/0.02) (0.05 * V_{ac1m} / 2.39 + 0.05)$
 where $V_{ac1m} = 1.502V$, $I_{input} = 4.07A$

CC=0.6-4.48A
 $I_{REF} = 0.7224 * I_{charge}$
 $K_i = 0.7224$
 $I_{REF} = 0.43V \sim 3.24V$

K_i
 $V_{ch1m} = I_{ref} * (PR374 / (PR372 + PR374))$
 $= I_{ref} * (100K / (80.6K + 100K))$
 $= I_{ref} * 0.5537$
 $I_{charge} = (165mV / PR369) * (V_{ch1m} / 3.3V)$
 $= (165m / 20m) * (1/3.3V) * I_{ref} * 0.5537$
 $= 1.3842 * I_{ref}$
 $I_{ref} = 0.7224 * I_{charge} \Rightarrow K_i = 0.7224$

K_v
 $R_{internal} = 514K$ $R_{ec} = 3K$ $R_1 = PR379 = 15.4K$ $R_2 = PR381 = 31.6K$
 $R = 514K // 31.6K // (15.4K + 3K) = 11.372K$
 $r = 514K // 514K // 31.6K = 28.14K$
 $V_{ce1} = 0.175 * V_{adj} + 3.99V$
 $4.2V = 0.175 * V_{adj} + 3.99V \Rightarrow V_{adj} = 1.2V$
 $V_{adj} = V_{ref} * (R / (R + 514K)) + CALIBRATE * (r / (r + 514K))$
 $1.1483 = CALIBRATE * 0.6046 \Rightarrow CALIBRATE = 1.899$
 $1.899 = (4.2 - (V_{ce1} * 0.175)) * R_v = (4.2 - (4.2 * 0.175)) * R_v$
 $A = V_{ref} * (R / (R + 514K)) = 0.052$
 $R_v = 9.451$

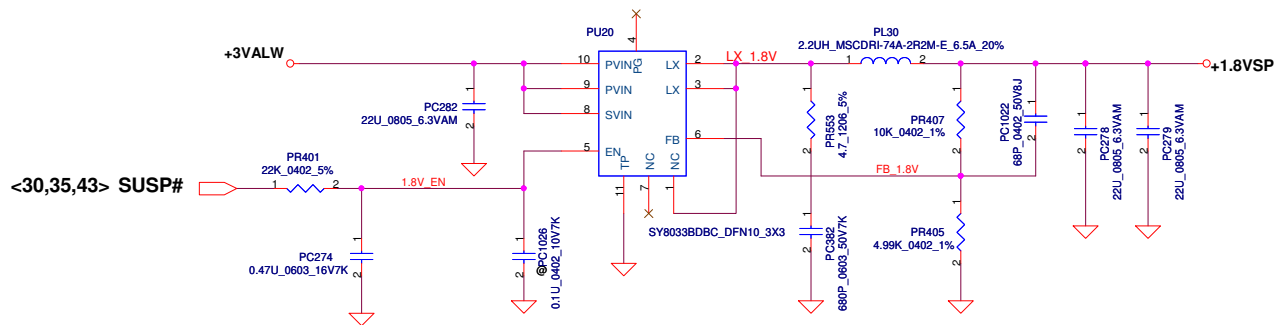
BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V



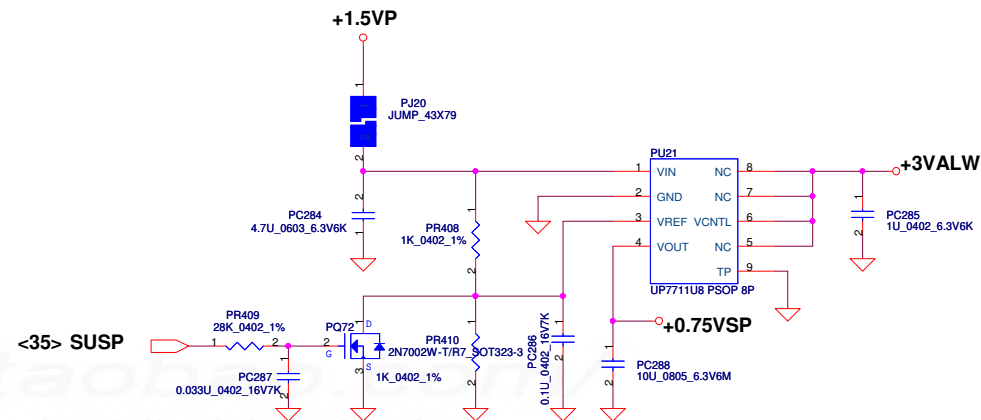
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FB=0.6V
 Note: Iload(max)=3.5A



<30,35,43> SUSP#



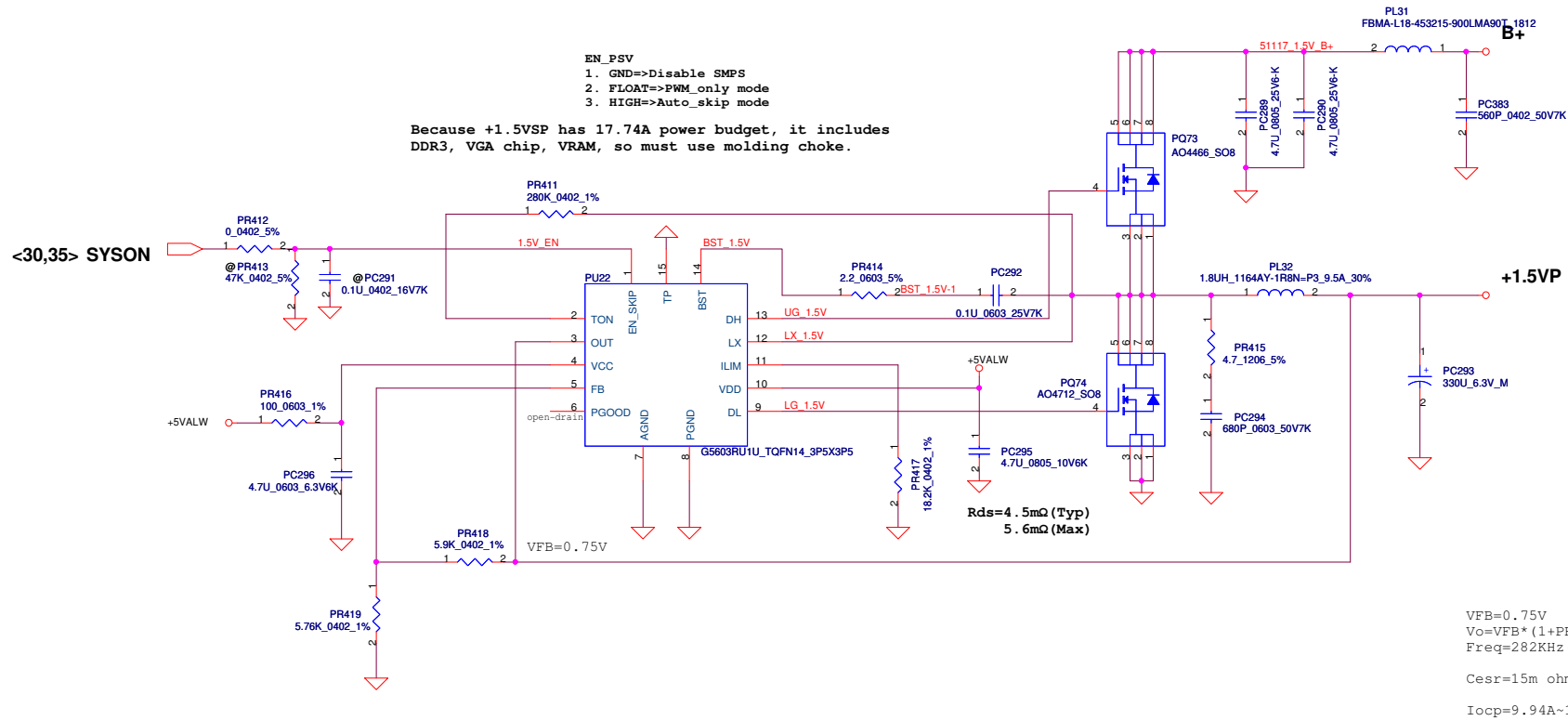
<35> SUSP

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				Document Number PEW71 M/B LA-6582P Schematic	
				Date:	Thursday, July 08, 2010
				Sheet	41 of 48
				Rev	1.0

- EN_PSV
 1. GND=>Disable SMPS
 2. FLOAT=>PWM_only mode
 3. HIGH=>Auto_skip mode

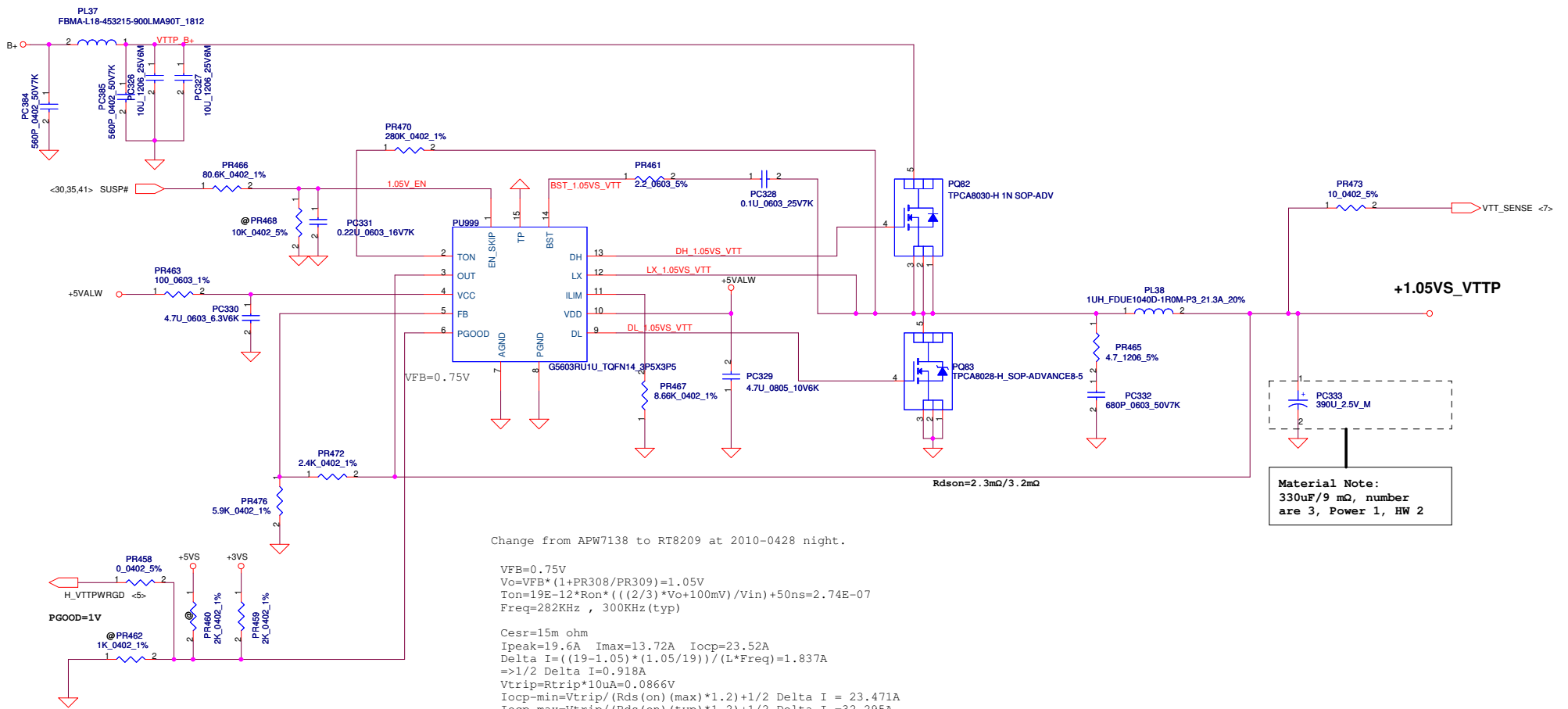
Because +1.5VSP has 17.74A power budget, it includes DDR3, VGA chip, VRAM, so must use molding choke.



$V_{FB}=0.75V$
 $V_o=V_{FB} \cdot (1+PR418/PR419)=1.52V$
 Freq=282KHz (min) , 300KHz (typ)
 C_{esr}=15m ohm
 I_{ocp}=9.94A~13A

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Size	Document Number	Rev		1.0	
Custom	PEW71 M/B LA-6582P Schematic	Date:		Thursday, July 08, 2010	
Sheet		42		of 48	



Change from APW7138 to RT8209 at 2010-0428 night.

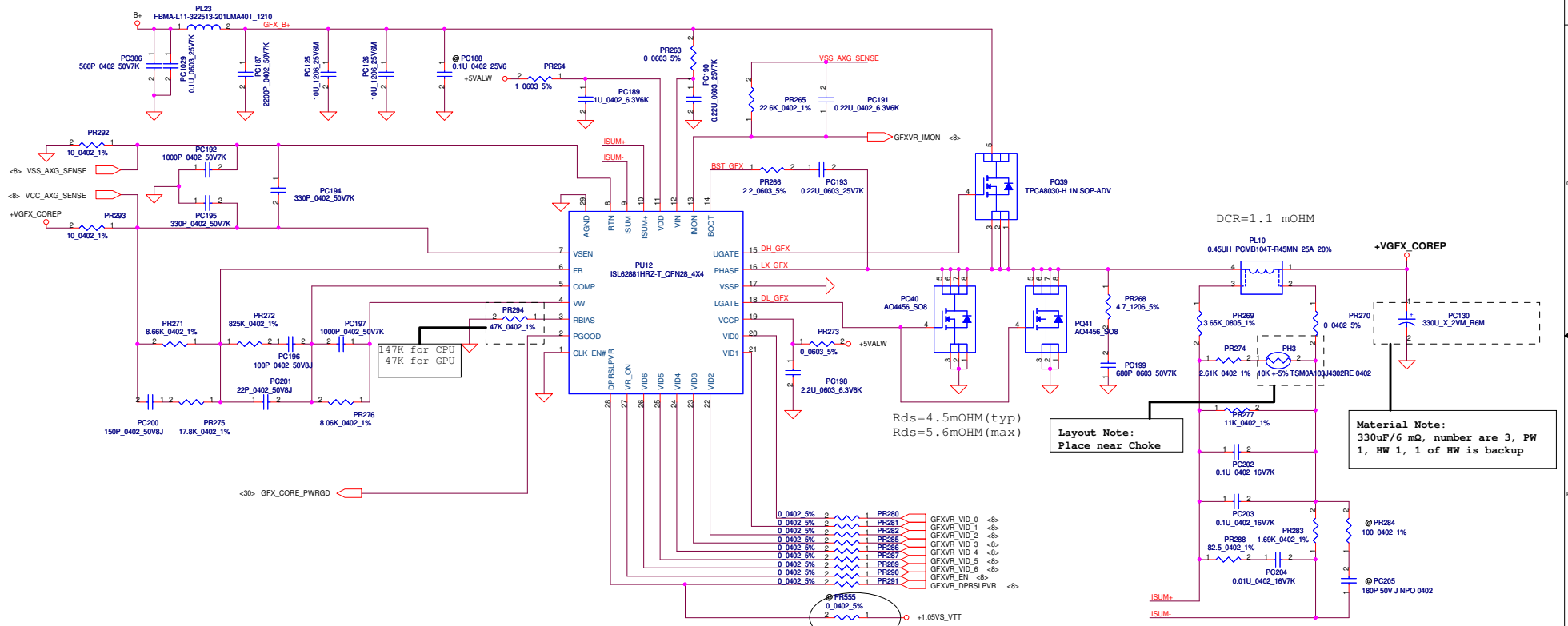
VFB=0.75V
 $V_o = VFB * (1 + PR308 / PR309) = 1.05V$
 $Ton = 19E-12 * Ron * (((2/3) * V_o + 100mV) / Vin) + 50ns = 2.74E-07$
 $Freq = 282KHz, 300KHz (typ)$

Cesr=15m ohm
 $I_{peak} = 19.6A$ $I_{max} = 13.72A$ $I_{ocp} = 23.52A$
 $\Delta I = ((19 - 1.05) * (1.05 / 19)) / (L * Freq) = 1.837A$
 $\Rightarrow 1/2 \Delta I = 0.918A$
 $V_{trip} = R_{trip} * 10uA = 0.0866V$
 $I_{ocp-min} = V_{trip} / (R_{ds(on)}(max) * 1.2) + 1/2 \Delta I = 23.471A$
 $I_{ocp-max} = V_{trip} / (R_{ds(on)}(typ) * 1.2) + 1/2 \Delta I = 32.295A$
 $I_{ocp} = 22.4A \sim 30.8A$

Material Note:
 330uF/9 mQ, number
 are 3, Power 1, HW 2

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				Date: Thursday, July 08, 2010	Sheet 43 of 48
				Rev 1.0	

Intel Aburndale CPU(Integrate Graphics) Ipeak=22A Imax=15A
 OCP calculation : Assume DCR=1.1m ohm
 $G1=Rn/(Rn+Rsum)=0.617$
 where $Rn=PR277 // (PR274+PH3)=5.875k\ ohm$
 $Rsum=PR269=3.65k\ ohm$
 $LL=2*Rdroop*G1*DCR/Ri=6.96m\ V/A$
 where $Rdroop=PR271=8.66k\ ohm$, $Ri=PR283=1.69k\ ohm$
 $Iocp=OCP\ Threshold*Rdroop/LL=24.89A$



Layout Note:
Place near Choke

Material Note:
330uF/6 mΩ, number are 3, PW
1, HW 1, 1 of HW is backup

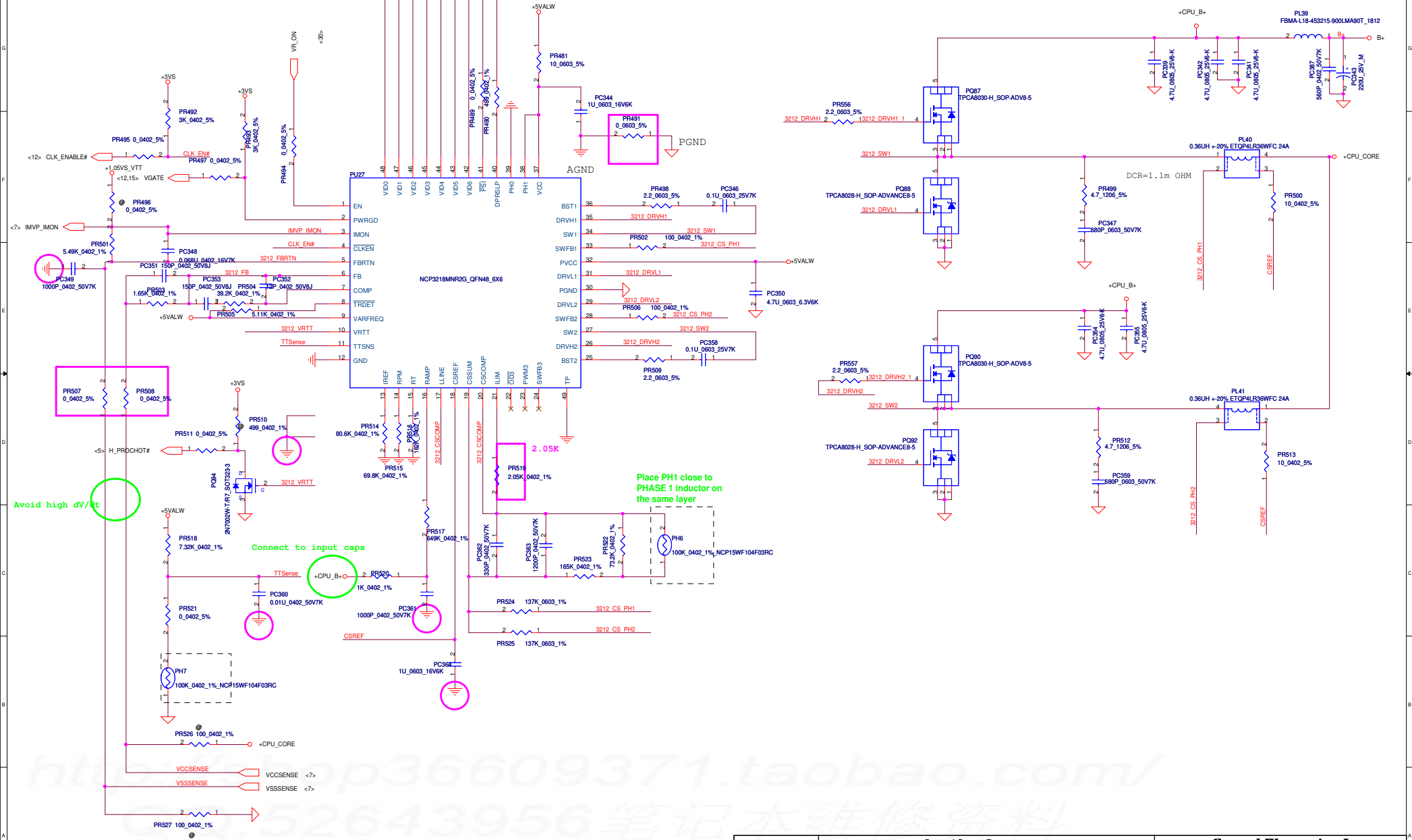
2009-1214 common circuit modify.

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				PEW71 M/B LA-6582P Schematic
				Rev 1.0
				Date: Thursday, July 08, 2010
				Sheet 44 of 48

PH0	PH1	# of PH
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_FDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD



Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1					Change PR353 from SD034470280 to SD034200380.		
2	Pre-Charge circiut update.	Pre-Charge circiut disable in EVT, now modify and enable it.	0.1	39	Change PR371 from SD034220280 to SD034470280. Change PR587 from SD034100380 to SD034470280. Change PR590 from SD034200280 to SD034143280. Change PR591 from SD028470280 to SD028100380.	2010/06/08	to PVT
3					Add PC1027 SE074222K80(S CER CAP 2200P 0402 50V7K) Change PQ111 from SB000006800 to SB301150200		
4	Pre-Charge circiut update.	Pre-Charge circiut disable in EVT, now modify and enable it.	0.1	38	Add PQ102 and PQ103 SB301150200. Add PR592 SD034200380.	2010/06/08	to PVT
5	Pre-Charge circiut update.	Pre-Charge circiut disable in EVT, now modify and enable it.	0.1	40	Change PR386 from SD011000080 to SD011100180. Add PR388, PR390, PR391 SD011100180. Add PD14 SC100001Y80 LL4148_LL34-2	2010/06/08	to PVT
6	EMI fail, add 3/5V snubber and Boost Resister to silve it.	EMI request to solve EMI issue.			Add PR566 and PR567 SD001470B80 S RES 4.7 1206 5%		
7			0.1	38	Add PC1012 and PC1013 SE074681K80 S CER CAP 680P 0402 50V7K	2010/06/08	to PVT
8	EMI fail, add 1.5V snubber.	EMI request to solve EMI issue.	0.1	42	Change PR564 and PR565 from SD013000080 to SD013220B80 Add PR415 SD001470B80 4.7 1206 5%. Add PC294 SE025681K80 S CER CAP 680P 50V K X7R 0603 Add PR465 SD001470B80 4.7 1206 5%.	2010/06/08	to PVT
9	EMI fail, add 1.05V snubber. and Boost Resister.	EMI request to solve EMI issue.	0.1	43	Add PC332 SE025681K80 S CER CAP 680P 50V K X7R 0603	2010/06/08	to PVT
10					Change PR461 from SD013000080 to SD013220B80 Add PR268 SD001470B80 4.7 1206 5%.		
11	EMI fail, add GFX_CORE snubber.	EMI request to solve EMI issue.	0.1	44	Add PC199 SE025681K80 S CER CAP 680P 50V K X7R 0603	2010/06/08	to PVT
12	HW power sequence modify.	HW request.	0.1	43	Change PR466 from SD034576280 S RES 1/16W 57.6K +-1% 0402 to SD034806280 S RES 80.6K 0402 1%) Change PC331 from SE076104K80 S CER CAP .1U 16V K X7R to SE00000R700 S CER CAP 0.22U 16V K X7R 0402	2010/06/08	to PVT
13					chnage PQ101 from SB301150000 to SB301150200.		
14	BOM unique.	BOM unique.	0.1	38		2010/06/08	to PVT
15	EMI request.	EMI request.	0.1	38	Add PC1028 SE042104K80 S CER CAP .1U 25V K X7R 0603	2010/06/08	to PVT
16	EMI request.	EMI request.	0.1	44	Add PC1029 SE042104K80 S CER CAP .1U 25V K X7R 0603	2010/06/08	to PVT
17	Sourcer request to change a common part.	Sourcer request.	0.1	38	Change PC1019 from SE00000GC00 S CER CAP 2.2U 10V K X7R 0603 to SE000003H00 S CER CAP 2.2UF 10V K X5R 0603	2010/06/08	to PVT
18	Per sourcer request.	Sourcer request to change PC331 from SE00000R700 to SE026224K80 for common part.	0.1	43	change PC331 from SE00000R700 to SE026224K80	2010/06/08	to PVT
19	CPU transient issue.	Need modify PC362 to 330P due to transient fail.	0.1	45	Change PC362 from SE074561K80 S CER CAP 560P 50V K X7R 0402 to SE074331K80 S CER CAP 330P 50V K X7R 0402	2010/06/08	to PVT
20	Per sourcer request.	Per sourcer request.	0.1	43 44	Chnage PQ39/PQ82 from SB000008L80 to SB00000HL00.	2010/06/08	to PVT
21	Cost down.	Cost down 3VALWP and Charger Low Side MOS.	0.1	38 39	Change PQ98 from SB00000AJ00 to SB000009580(A04468). Change PQ64 from SB00000CG00 to SB000009580(A04468).	2010/06/08	to PVT
22	Cost down.	Cost down +1.5VP Low side MOS and choke.	0.1	42	Chnage PQ74 from SB000009F80 to SB00000AJ00(A04712). Chnage PL32 from SH000009U00 to SH000009680.	2010/06/08	to PVT
23	Cost down.	re-caculate 1.5VP OCP.	0.1	42	Change PR417 from SD034110280 to SD034182280.	2010/06/08	to PVT

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				Custom	
				Date:	Thursday, July 08, 2010
				Sheet	46 of 48
				Rev	1.0

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24	Cost down.	re-caculate +3VALWP OCP.	0.1	38	Change PR562 from SD034107380 to SD034137380.	2010/06/08	to PVT
25							
26							
27							
28							
29							
30							
31							
32							
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46							

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				Custom	
Date:				Thursday, July 08, 2010	Sheet 47 of 48

Version change list (P.I.R. List)

Item	Phase	PAGE	DATE	Modifycatio list	Purpose
1	EVT		04 / 08 04 / 16 04 / 21 04 / 26 04 / 27 04 / 29 04 / 29 05 / 03 05 / 03 05 / 06 05 / 07 05 / 10 05 / 11 05 / 12 05 / 13 06 / 01 06 / 02 06 / 03 06 / 04 06 / 10 07 / 07 07 / 08	<p>N/A</p> <p>Modify RTC SCH</p> <p>Change LAN to AR8152</p> <p>Update Power SCH</p> <p>Update AND Gate symbol - U1 / U2 / U6 / U7 / U19</p> <p>Update Power MOS symbol - U24 / U25 / U26</p> <p>C196 change to 1U for INTEL disign</p> <p>CLK GEN del C35 / C36 / C30 / C31 / C32 / C33 / C34 / L3 (for 36@ and @ function)</p> <p>Q4+Q6 change to 2N7002DW</p> <p>Update U8 symbol</p> <p>Add DMIC function</p> <p>Modify USB define.</p> <p>Update Power SCH</p> <p>Add R17 for DMIC power</p> <p>Update Power SCH</p> <p>Change LAN to GIGA&10/100 co-lay</p> <p>Del R307 (LVDS conn.)</p> <p>Change +1.05VS VTT to +1.05VS (CLK GEN)</p> <p>Change C842 / C850 / C854 / C656 to SE080105K80 1U_0603_10V6K</p> <p>Change R940 to 28K (S3 Power sequence)</p> <p>SW 1 bin define (LAN)</p> <p>Change R907 (0.0603) to 0.1206 5%</p> <p>Remove C40 / C41 / C42 / C43 / C44</p> <p>Change FAN Conn.</p> <p>Update Power SCH</p> <p>Change LAN to BCM57780 GIGA</p> <p>Del R637 / R639 / R640 / R645 / R647 / R648 (AUDIO)</p> <p>Del DMIC</p> <p>Update Power SCH</p> <p>Update Power SCH</p> <p>Add C49 / C50 (EC B+)</p> <p>Update Power SCH</p> <p>C764 / C765 change to 18P 0402_50V8J (EC)</p> <p>Reserve D13 / D24 / D30 (ESB)</p> <p>U17 change to RTS5137 (SA000043500) Card reader</p> <p>Update Power SCH</p> <p>Unpop L11 / C247 & Pop R304 for cost down</p> <p>Unpop C764 / X2 & Pop R13 & C765 Change to 100K for EC remove Crystal</p> <p>Pop R834 & R835 change to 200K for Project ID</p> <p>Unpop D24 / D30</p> <p>Unpop R690 / R691</p> <p>Pop C49 / C50</p> <p>For HDMI</p> <p>Unpop R753 / R757 , Add R754 / R758 to 0 ohm.</p> <p>Change R759 to 3.9K.</p> <p>Change R755 to 4.7K ohm , Unpop R748.</p> <p>Unpop R778.</p> <p>R833 / R292 0.0805 change to 0.0603.</p> <p>C190 / C191 & C1135 / C1136 change to 33P 0402 50V8J for Vender test report</p> <p>Unpop C774~C799 for EMI cost down.</p> <p>Update Power SCH</p> <p>Add T25 / T26 / T27</p> <p>Update Power SCH</p> <p>Change R759 to 4.32K_1% SB00000J280</p>	

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				Date:	Thursday, July 08, 2010	Sheet 48 of 48