ZZZ1

LA-6001P

DAZ0CG00100

Compal Confidential

NBLB3/5 Schematics Document

Intel Clarksfield Processor with DDRIII + Ibex HM55

2010-04-28

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: SCHEMATIC,MB A6001

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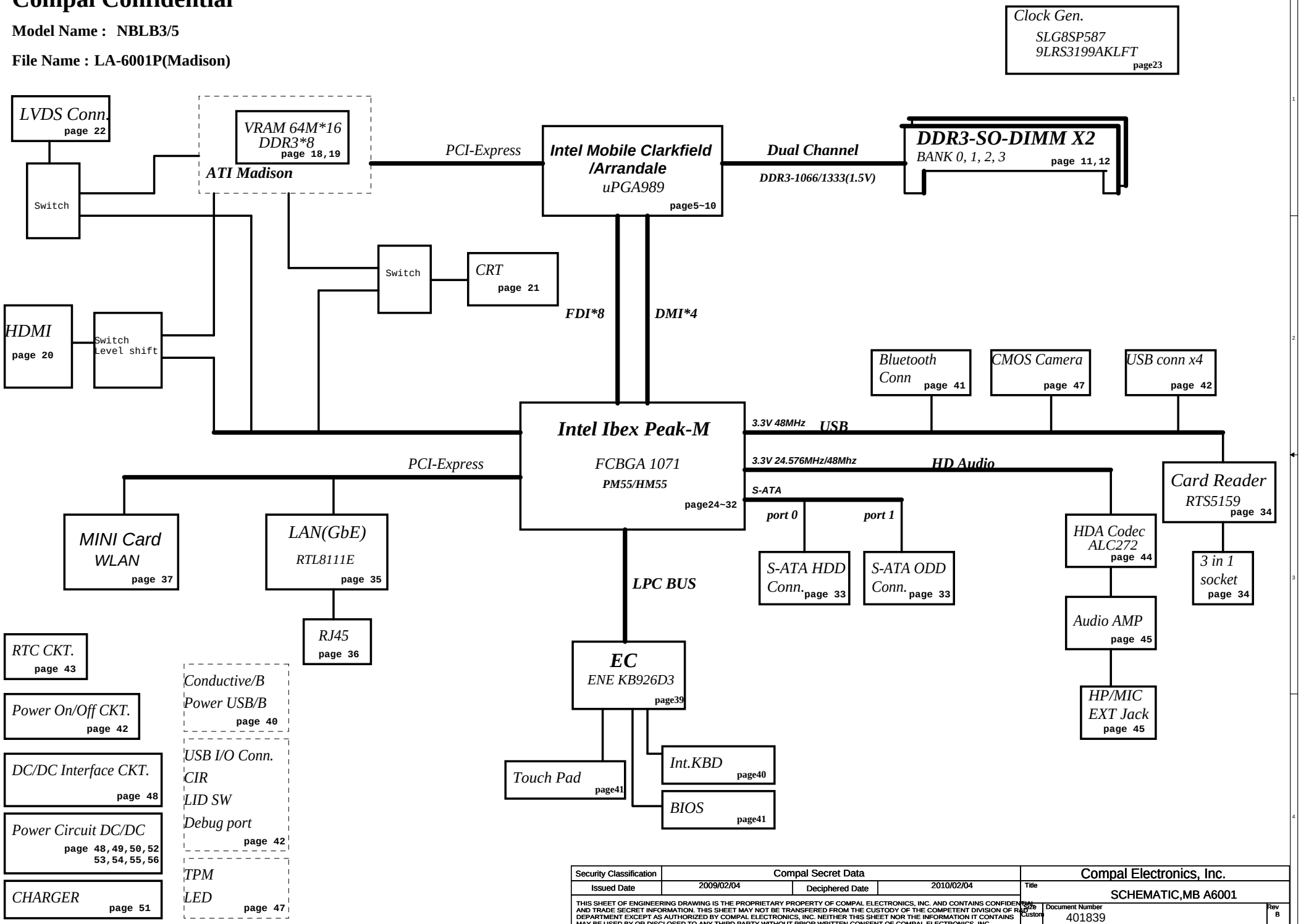
Compal Confidential

Model Name : NBLB3/5

File Name : LA-6001P(Madison)



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DDR3 Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS +1.1VS_VTT +1.5VS_VRAM
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

GPIO PIN Define

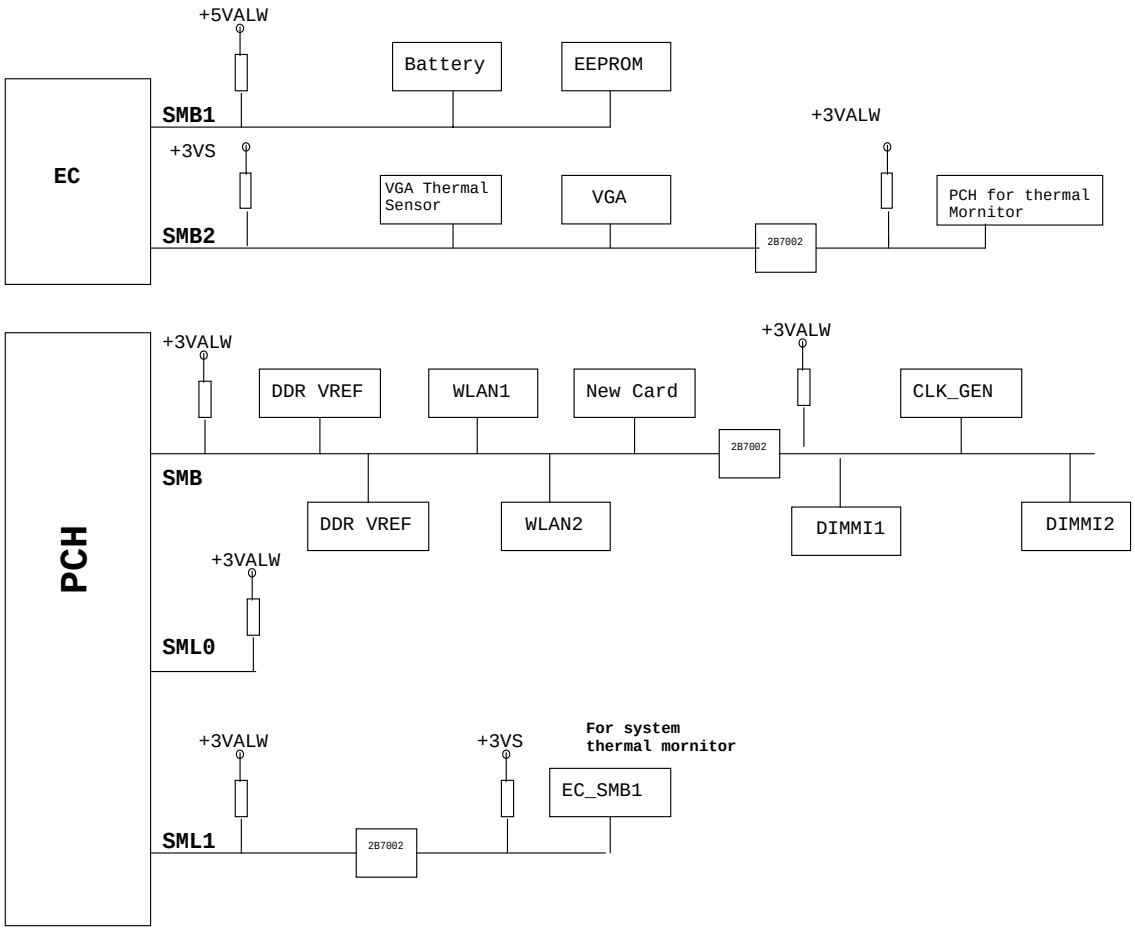
	ID3	ID2	ID1	ID0
NBLB2(1100)	R358	R361	R766	R765
Reserve (1101)	X	X	X	X
Reserve (1110)	X	X	X	X
Reserve (1111)	X	X	X	X
NBLB1 (0000)	R353	R350	R766	R765
Reserve(0001)	X	X	X	X
Reserve(0010)	X	X	X	X
Reserve(0011)	X	X	X	X
Reserve(0100)	X	X	X	X
Reserve(0101)	X	X	X	X
Reserve (0110)	X	X	X	X
Reserve (0111)	X	X	X	X
Reserve (1000)	X	X	X	X
Reserve (1001)	X	X	X	X
Reserve (1010)	X	X	X	X
Reserve (1011)	X	X	X	X

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b

EC SM Bus2 address

Device	Address
EMCI 1402	100_1100X b
NVIDIA N10P-GE1	



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VGA (Madison)

State \ power plane	+1.8VS +1.5VS_VRAM	+3VS_DELAY +VGA_CORE +1.1VS
S0	0	0
S1	0	0
S3	X	X
S5 S4/AC	X	X
S5 S4/ Battery only	X	X
S5 S4/AC & Battery don't exist	X	X

47132_madison_ds_nda_1.04

Madison sequence

POWER UP/DOWN Sequence

Power-Up/Down Sequence
Madison has the following requirements with regards to power supply sequencing to avoid damaging the ASIC.

1, All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

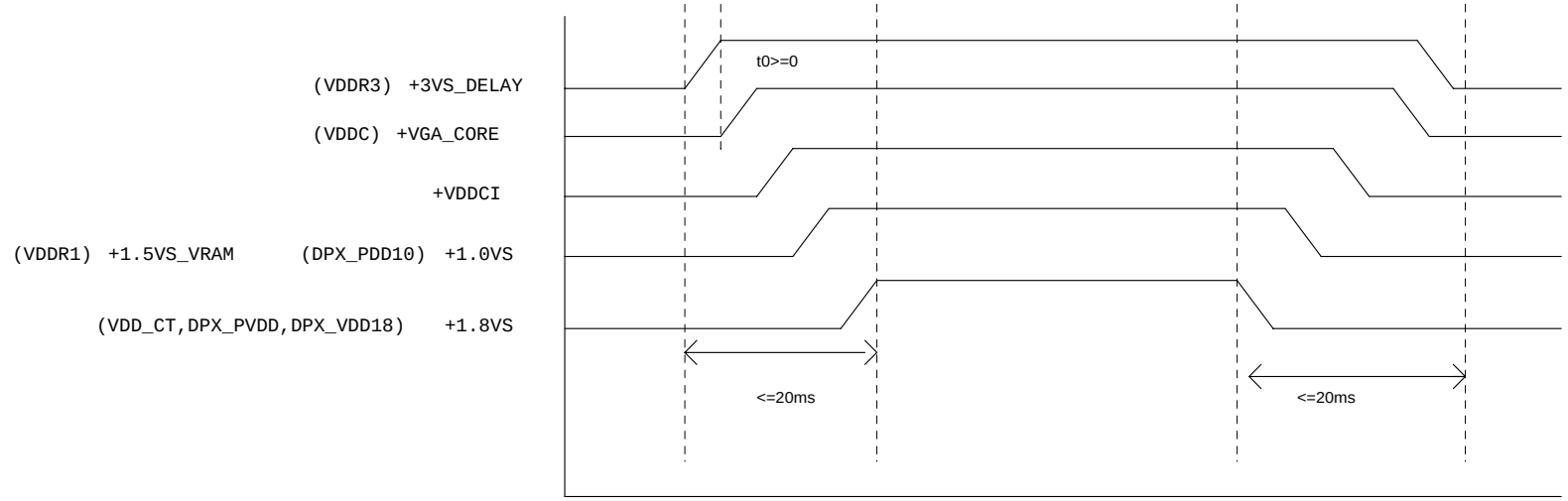
2, VDDR3 should ramp-up before or simultaneously with VDDC.

3, For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

4, The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

5, VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)

6, For power-down, reversing the ramp-up sequence is recommended.



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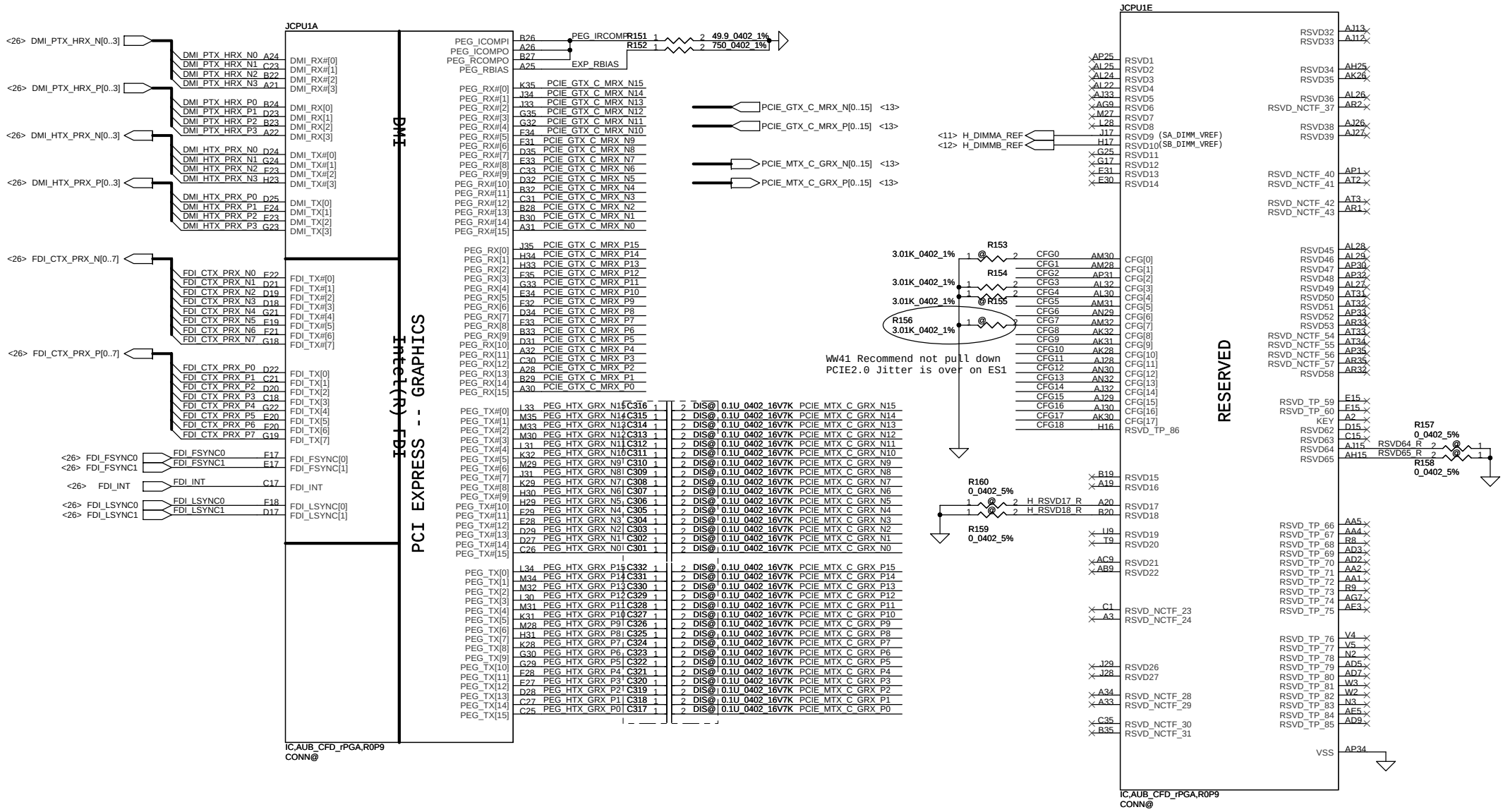

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

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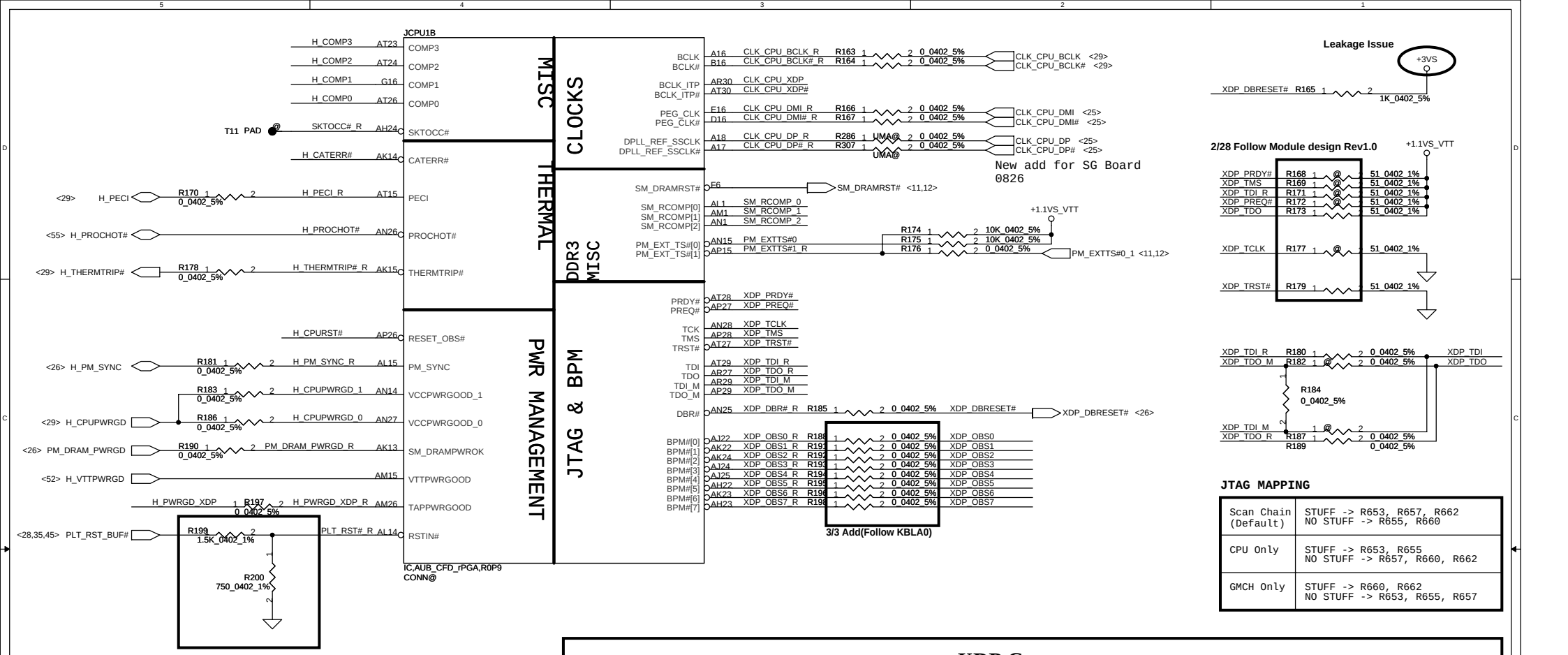
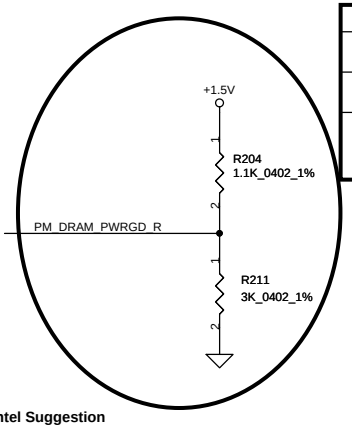
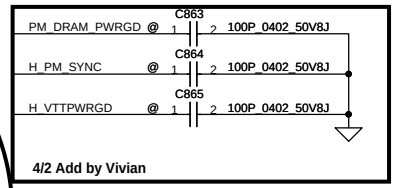
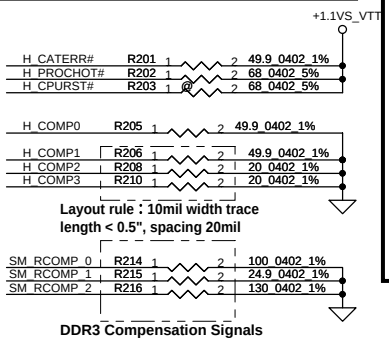


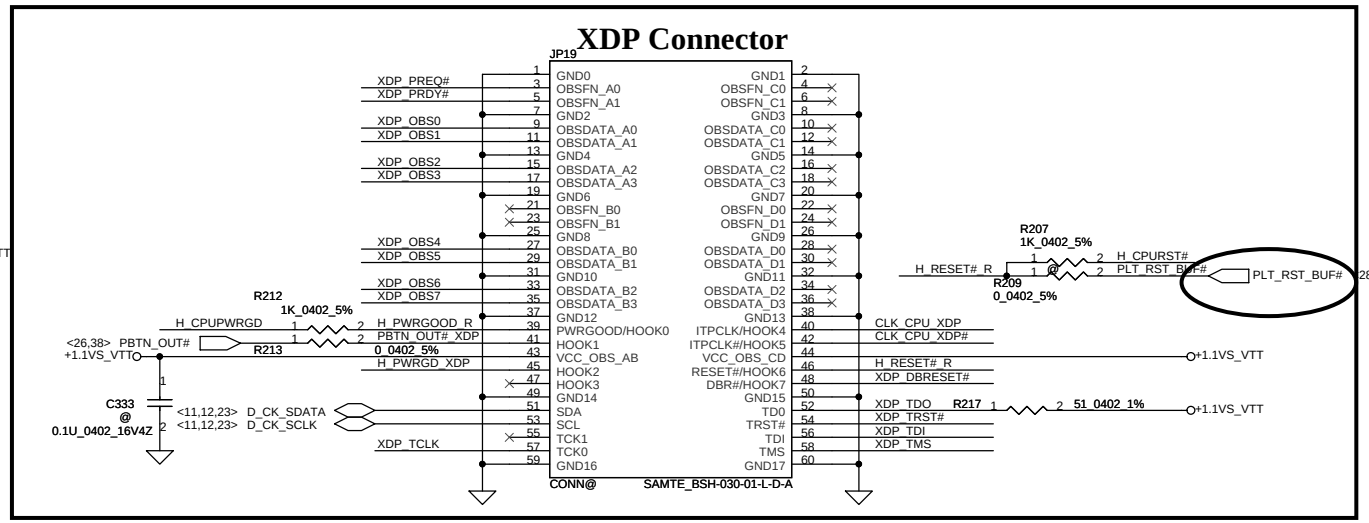
4/17 Modify R199 to 1.5K ohm, R200 to 750 ohm(see DG414044 p.8)



Intel Suggestion
WW14_2009_Calpella_MoW
Notice: V_SM should be available in S3







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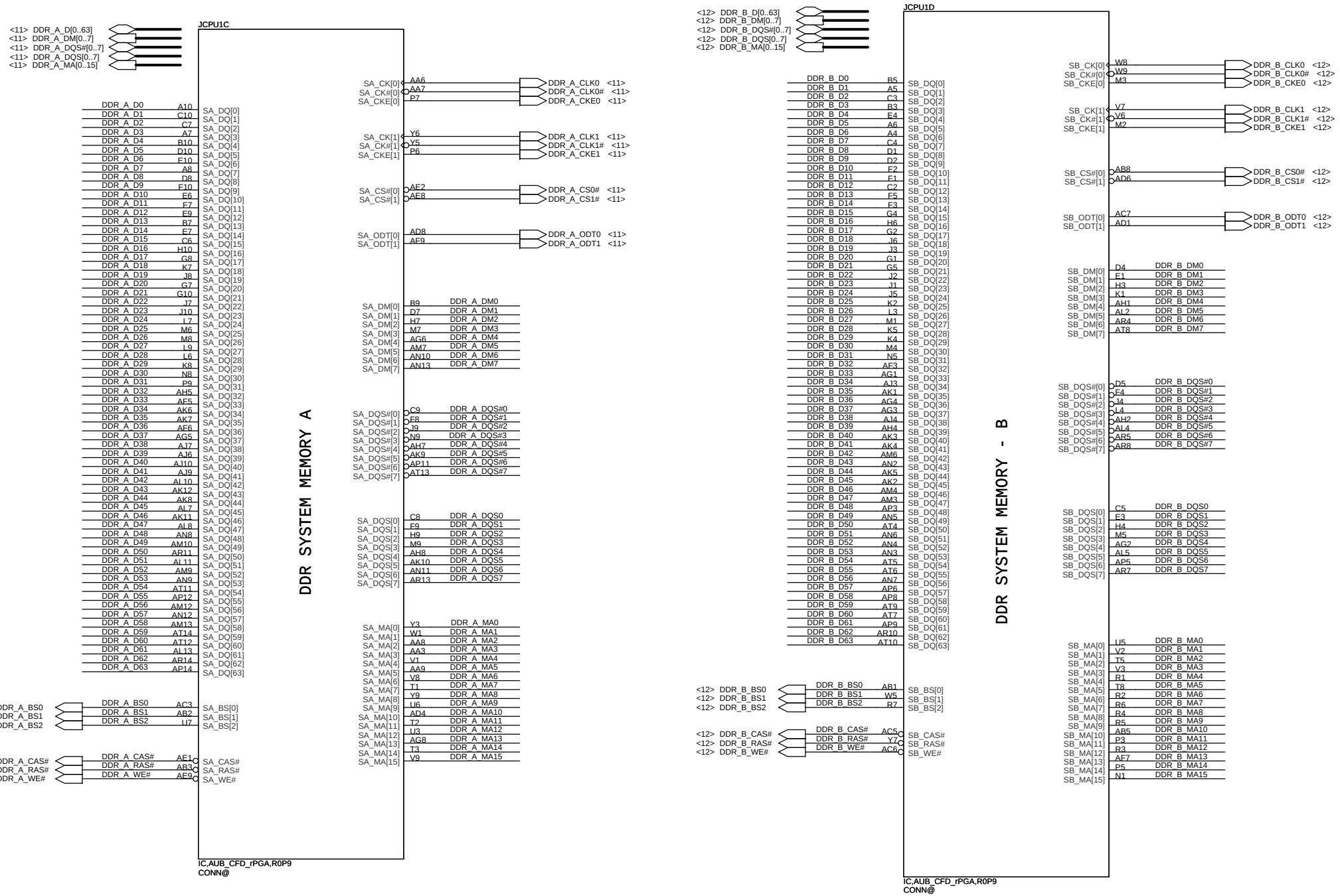

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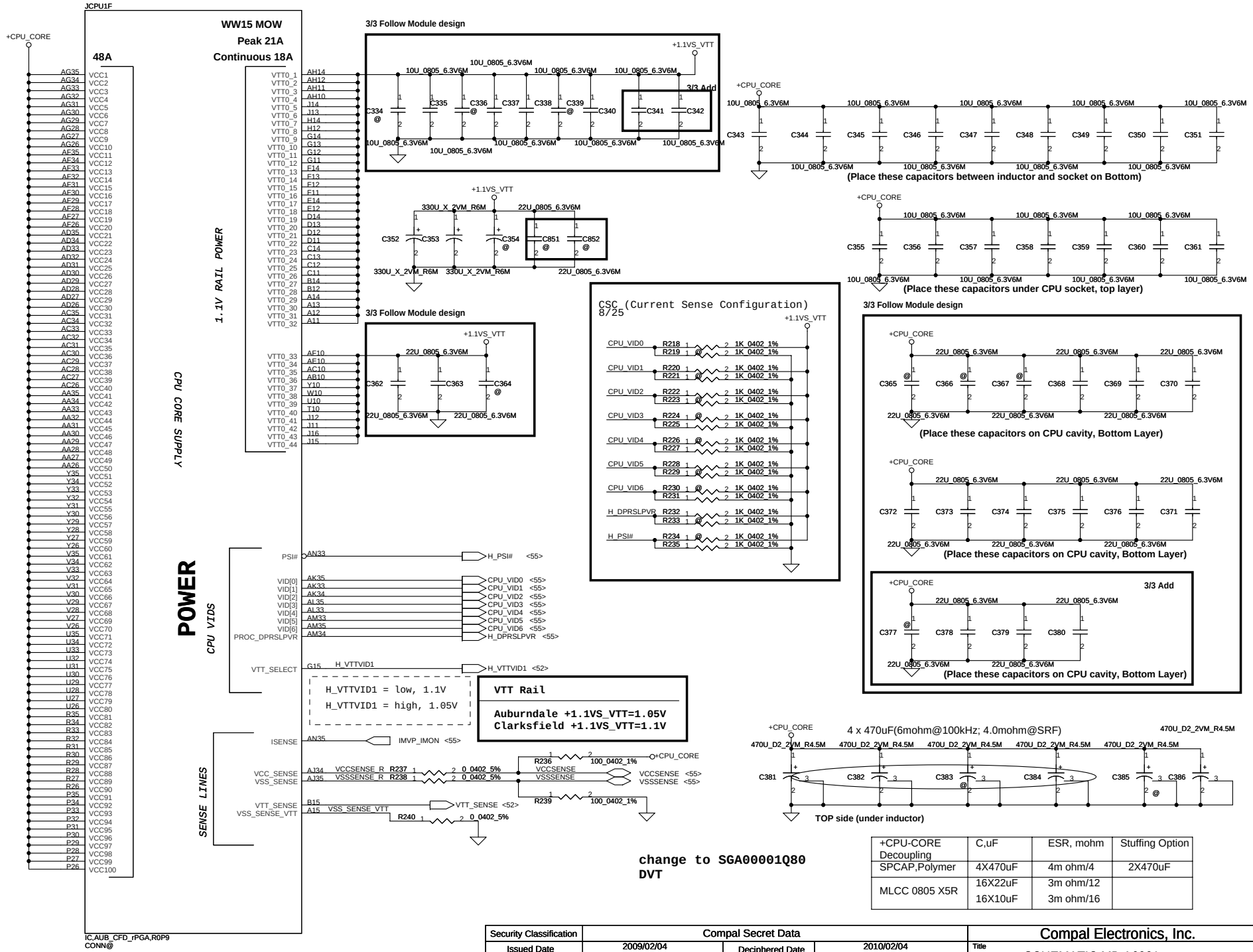

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF 16X10uF	3m ohm/12 3m ohm/16	

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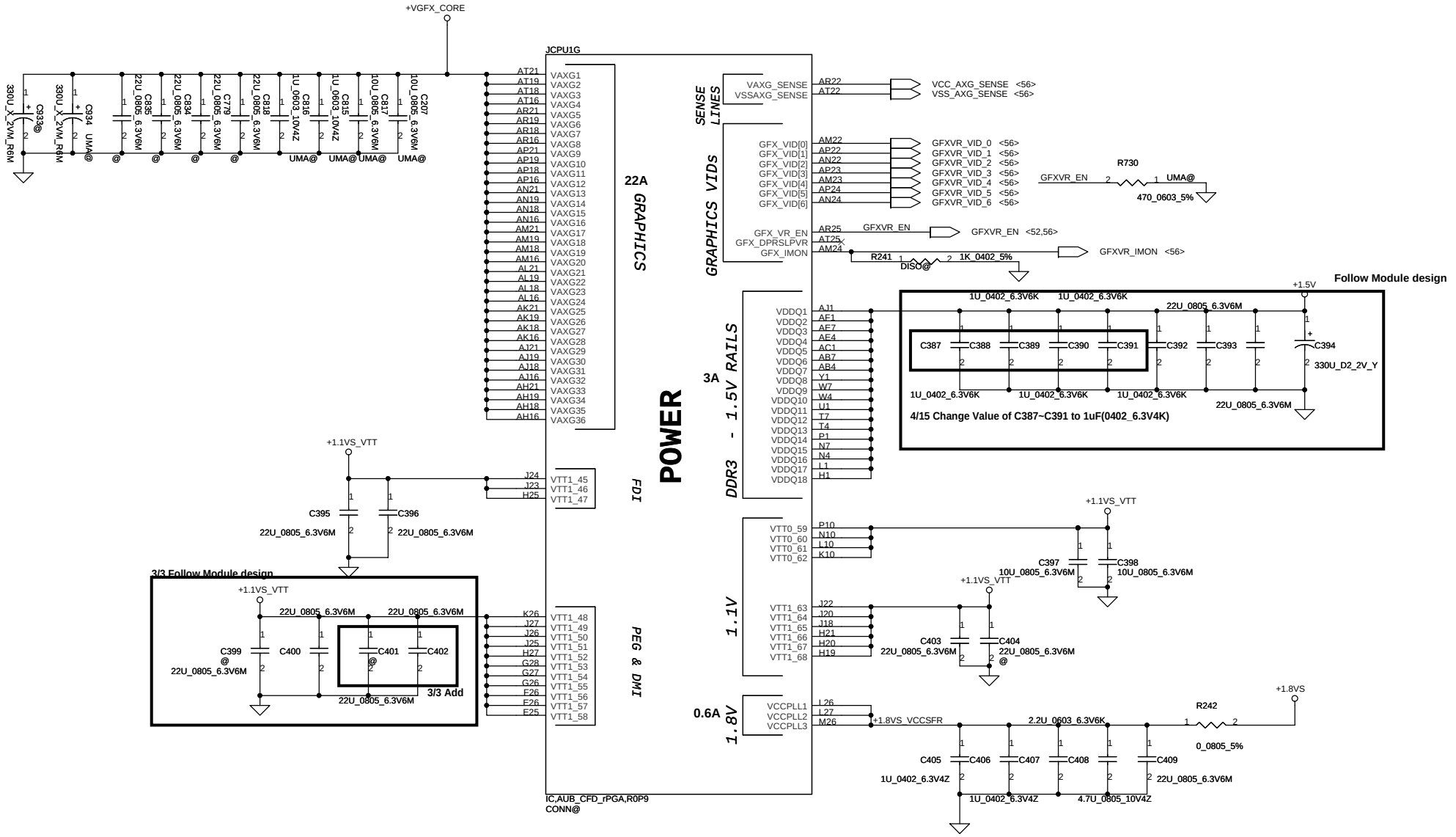

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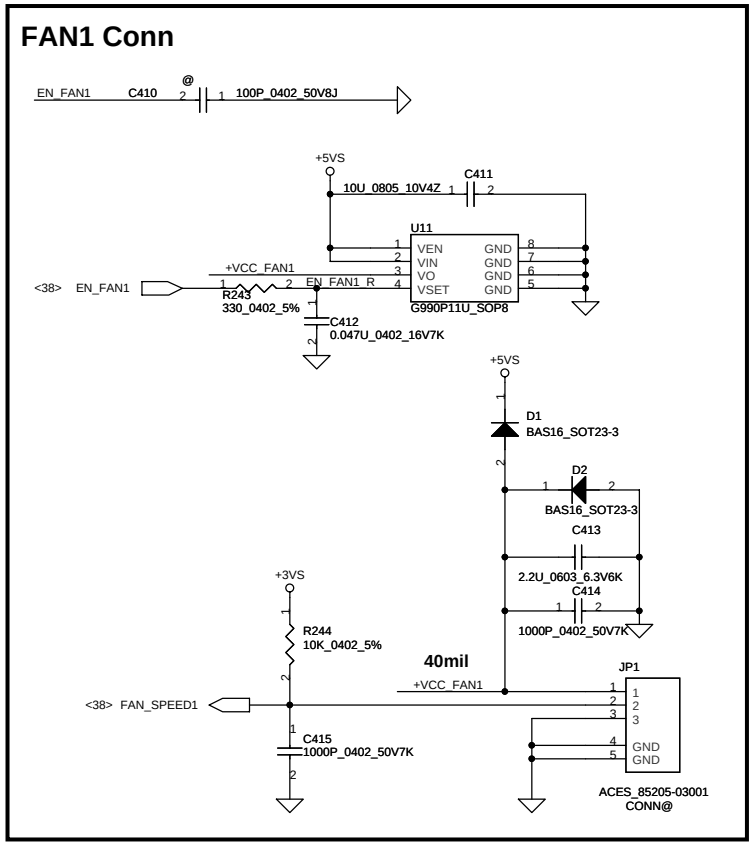

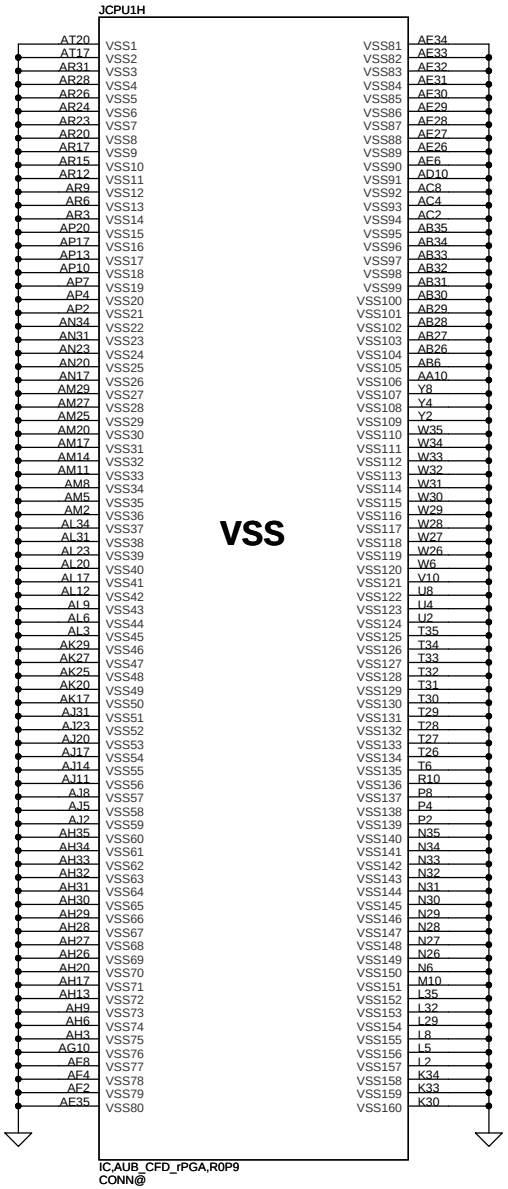

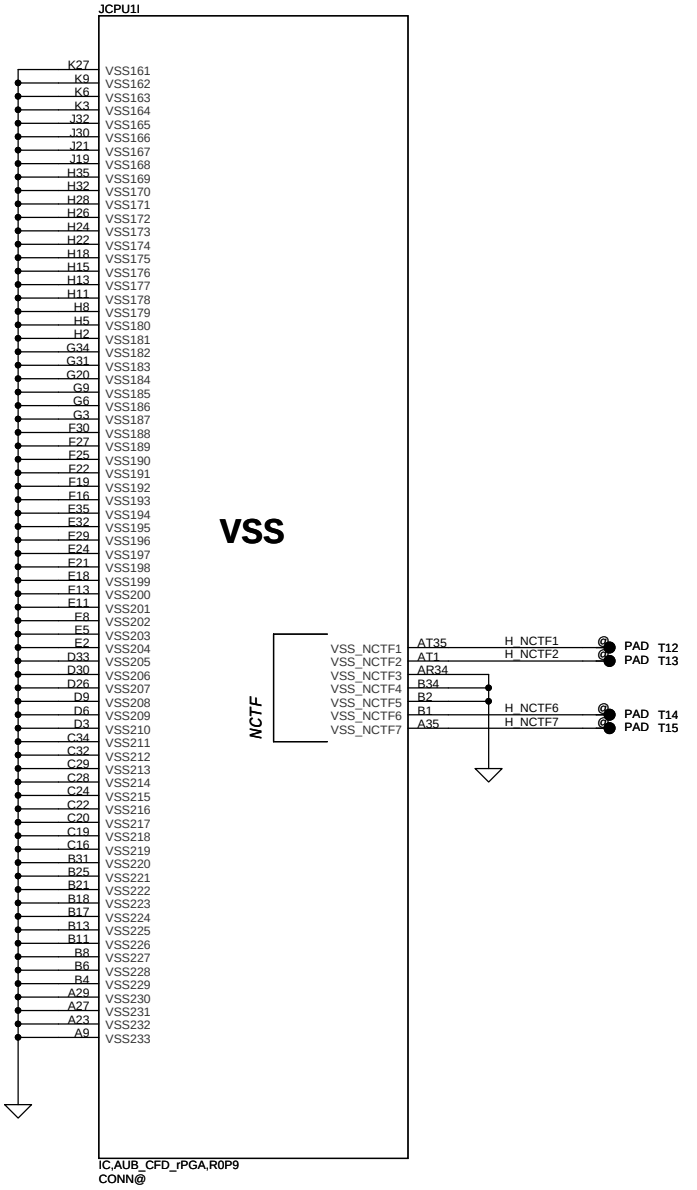

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M1 Circuit

+1.5V

R246 1K_0402_1%

+V_DDR3_DIMM_REF

R249 1K_0402_1%

<7> DDR_A_DQS#[0..7]
<7> DDR_A_D[0..63]
<7> DDR_A_DM[0..7]
<7> DDR_A_DQS[0..7]
<7> DDR_A_MA[0..15]

M3 Circuit DISO@

<5> H_DIMMA_REF — R245 0_0402_5%

+V_DDR3_DIMM_REF — R247 0_0402_5%

C417 0.1U_0402_16V4Z

C416 2.2U_0805_16V4Z

+1.5V

+1.5V

JP2

	VREF_DQA	1	VREF_DQ	VSS1	2	
		3	VSS2	DQ4	4	DDR_A_D4
DDR_A_D0		5	DQ0	DQ5	6	DDR_A_D5
DDR_A_D1		7	DQ1	VSS3	8	
		9	VSS4	DQS#0	10	DDR_A_DQS#0
DDR_A_DM0		11	DM0	DQS0	12	DDR_A_DQS0
		13	VSS5	VSS6	14	
DDR_A_D2		15	DQ2	DQ6	16	DDR_A_D6
DDR_A_D3		17	DQ3	DQ7	18	DDR_A_D7
		19	VSS7	VSS8	20	
DDR_A_D8		21	DQ8	DQ12	22	DDR_A_D12
DDR_A_D9		23	DQ9	DQ13	24	DDR_A_D13
		25	VSS9	VSS10	26	
DDR_A_DQS#1		27	DQS#1	DM1	28	DDR_A_DM1
DDR_A_DQS1		29	DQS1	RESET#	30	SM_DRAMRST# — SM_DRAMRST# <6,12>
		31	VSS11	VSS12	32	
DDR_A_D10		33	DQ10	DQ14	34	DDR_A_D14
DDR_A_D11		35	DQ11	DQ15	36	DDR_A_D15
		37	VSS13	VSS14	38	
DDR_A_D16		39	DQ16	DQ20	40	DDR_A_D20
DDR_A_D17		41	DQ17	DQ21	42	DDR_A_D21
		43	VSS15	VSS16	44	
DDR_A_DQS#2		45	DQS#2	DM2	46	DDR_A_DM2
DDR_A_DQS2		47	DQS2	VSS17	48	
		49	VSS18	DQ22	50	DDR_A_D22
DDR_A_D18		51	DQ18	DQ23	52	DDR_A_D23
DDR_A_D19		53	DQ19	VSS19	54	
		55	VSS20	DQ28	56	DDR_A_D28
DDR_A_D24		57	DQ24	DQ29	58	DDR_A_D29
DDR_A_D25		59	DQ25	VSS21	60	
		61	VSS22	DQS#3	62	DDR_A_DQS#3
DDR_A_DM3		63	DM3	DQS3	64	DDR_A_DQS3
		65	VSS23	VSS24	66	
DDR_A_D26		67	DQ26	DQ30	68	DDR_A_D30
DDR_A_D27		69	DQ27	DQ31	70	DDR_A_D31
		71	VSS25	VSS26	72	
<7> DDR_A_CKE0	DDR_A_CKE0	73	CKE0	CKE1	74	DDR_A_CKE1 — DDR_A_CKE1 <7>
		75	VDD1	VDD2	76	
		77	NC1	A15	78	DDR_A_MA15
<7> DDR_A_BS2	DDR_A_BS2	79	BA2	A14	80	DDR_A_MA14
		81	VDD3	VDD4	82	
DDR_A_MA12		83	A12/BC#	A11	84	DDR_A_MA11
DDR_A_MA9		85	A9	A7	86	DDR_A_MA7
		87	VDD5	VDD6	88	
DDR_A_MA8		89	A8	A6	90	DDR_A_MA6
DDR_A_MA5		91	A5	A4	92	DDR_A_MA4
		93	VDD7	VDD8	94	
DDR_A_MA3		95	A3	A2	96	DDR_A_MA2
DDR_A_MA1		97	A1	A0	98	DDR_A_MA0
		99	VDD9	VDD10	100	
<7> DDR_A_CLK0	DDR_A_CLK0	101	CK0	CK1	102	DDR_A_CLK1 — DDR_A_CLK1 <7>
<7> DDR_A_CLK0#	DDR_A_CLK0#	103	CK0#	CK1#	104	DDR_A_CLK1# — DDR_A_CLK1# <7>
		105	VDD11	VDD12	106	
DDR_A_MA10		107	A10/AP	BA1	108	DDR_A_BS1 — DDR_A_BS1 <7>
<7> DDR_A_BS0	DDR_A_BS0	109	BA0	RAS#	110	DDR_A_RAS# — DDR_A_RAS# <7>
		111	VDD13	VDD14	112	
<7> DDR_A_WE#	DDR_A_WE#	113	WE#	S0#	114	DDR_A_CS0# — DDR_A_CS0# <7>
<7> DDR_A_CAS#	DDR_A_CAS#	115	CAS#	ODT0	116	DDR_A_ODT0 — DDR_A_ODT0 <7>
		117	VDD15	VDD16	118	
DDR_A_MA13		119	A13	ODT1	120	DDR_A_ODT1 — DDR_A_ODT1 <7>
<7> DDR_A_CS1#	DDR_A_CS1#	121	S1#	NC2	122	
		123	VDD17	VDD18	124	
		125	NCTEST	VREF_CA	126	DDR_VREF_CA_DIMMA — R256 0_0402_5%
		127	VSS27	VSS28	128	
DDR_A_D32		129	DQ32	DQ36	130	DDR_A_D36
DDR_A_D33		131	DQ33	DQ37	132	DDR_A_D37
		133	VSS29	VSS30	134	
DDR_A_DQS#4		135	DQS#4	DM4	136	DDR_A_DM4
DDR_A_DQS4		137	DQS4	VSS31	138	
		139	VSS32	DQ38	140	DDR_A_D38
DDR_A_D34		141	DQ34	DQ39	142	DDR_A_D39
DDR_A_D35		143	DQ35	VSS33	144	
		145	VSS34	DQ44	146	**DDR_A_D44**
DDR_A_D40		147	DQ40	DQ45	148	DDR_A_D45
DDR_A_D41		149	DQ41	VSS35	150	
		151	VSS36	DQS#5	152	DDR_A_DQS#5
DDR_A_DM5		153	DM5	DQS5	154	DDR_A_DQS5
		155	VSS37	VSS38	156	
DDR_A_D42		157	DQ42	DQ46	158	DDR_A_D46
DDR_A_D43		159	DQ43	DQ47	160	DDR_A_D47
		161	VSS39	VSS40	162	
DDR_A_D48		163	DQ48	DQ52	164	DDR_A_D52
DDR_A_D49		165	DQ49	DQ53	166	DDR_A_D53
		167	VSS41	VSS42	168	
DDR_A_DQS#6		169	DQS#6	DM6	170	DDR_A_DM6
DDR_A_DQS6		171	DQS6	VSS43	172	
		173	VSS44	DQ54	174	DDR_A_D54
DDR_A_D50		175	DQ50	DQ55	176	DDR_A_D55
DDR_A_D51		177	DQ51	VSS45	178	
		179	VSS46	DQ60	180	DDR_A_D60
DDR_A_D56		181	DQ56	DQ61	182	DDR_A_D61
DDR_A_D57		183	DQ57	VSS47	184	
		185	VSS48	DQS#7	186	DDR_A_DQS#7
DDR_A_DM7		187	DM7	DQS7	188	DDR_A_DQS7
		189	VSS49	VSS50	190	
DDR_A_D58		191	DQ58	DQ62	192	DDR_A_D62
DDR_A_D59		193	DQ59	DQ63	194	DDR_A_D63
		195	VSS51	VSS52	196	
	R257 10K_0402_5%	197	SA0	EVENT#	198	PM_EXTTS#0_1 — PM_EXTTS#0_1 <6,12>
+3VSO		199	VDDSPD	SDA	200	D_CK_SDATA — D_CK_SDATA <6,12,23>
		201	SA1	SCL	202	D_CK_SCLK — D_CK_SCLK <6,12,23>
		203	VTT1	VTT2	204	+0.75VS
		205	G1	G2	206	

C436 2.2U_0603_6.3V6K

C437 0.1U_0402_16V4Z

R258 10K_0402_5%

5.2mm

LCN_DAN06-K4526-0100

CONN@

+V_DDR3_DIMM_REF

C421 2.2U_0603_6.3V6K

C422 0.1U_0402_16V4Z

2/28 Module design don't use pin78(NC),need double check it.

Layout Note:
Place near JP2

Follow Module design

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.5V

10U_0603_6.3V6M: C423, C424, C425, C426, C427, C428

0.1U_0402_16V4Z: C429, C430, C431, C432

330U_D2_2V_Y: C433 @

10U_0603_6.3V6M: C434, C435

3/3 Add(Follow Module design)

10U_0603_6.3V6M 10U_0603_6.3V6M 10U_0603_6.3V6M 0.1U_0402_16V4Z 0.1U_0402_16V4Z 330U_D2_2V_Y 10U_0603_6.3V6M

4/15 Change value of C423~C428 from 10uF(0805_6.3V6M) to 10uF(0603_6.3V6M)

Layout Note:
Place near JP2.203 & JP2.204

+0.75VS

1U_0402_6.3V6K: C438, C439, C440, C441, C442

10U_0805_6.3V6M: C853

4/15 Change value of C438~C442 from 1uF(0603_10V4Z) to 1U(0402_6.3V6K)

Follow Module design

3/16 Add C853= 10uF(0805_6.3V6M)(Intel's comment)

1U_0402_6.3V6K 1U_0402_6.3V6K 10U_0805_6.3V6M

DDR3 SO-DIMM A Standard Type

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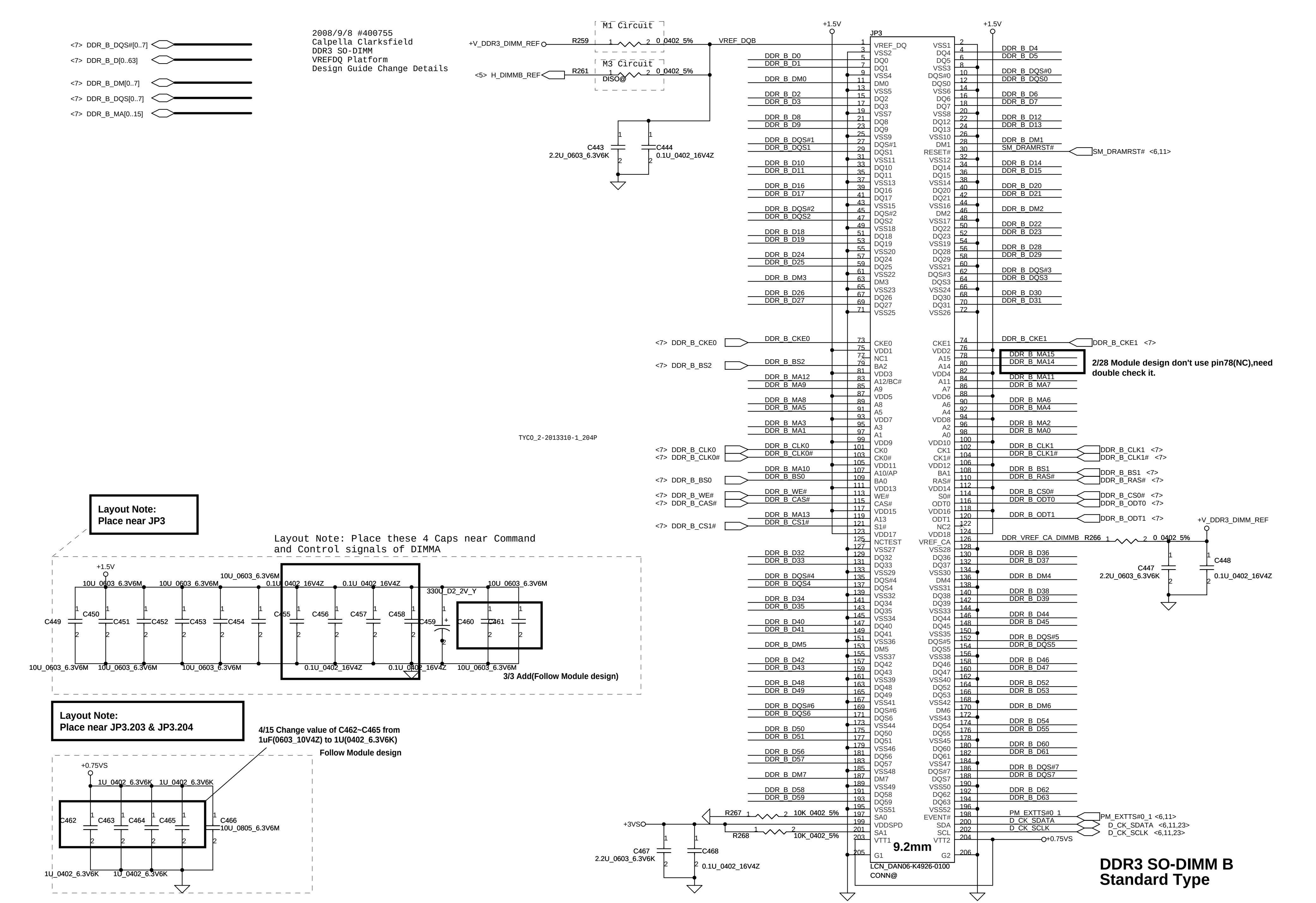

DDR3 SO-DIMM B Standard Type

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U4

SA00002UQ50

216-0729042 A13 M96-M2 FCBGA962 0FA

M96@

U4

SA00003M320

216-0772000 A11 MADISON PRO 030

MADVGA@

U4

SA00003MC20

216-0774007 A11 PARK XT M2 962P 030

PARKVGA@

<5> PCIE_MTX_C_GRX_N[0..15] → PCIE_MTX_C_GRX_N[0..15]

<5> PCIE_MTX_C_GRX_P[0..15] → PCIE_MTX_C_GRX_P[0..15]

<5> PCIE_GTX_C_MRX_N[0..15] ← PCIE_GTX_C_MRX_N[0..15]

<5> PCIE_GTX_C_MRX_P[0..15] ← PCIE_GTX_C_MRX_P[0..15]

U4A

PCI EXPRESS INTERFACE

T2 PAD	PCIE_MTX_C_GRX_P0	AA38	PCIE_RX0P	PCIE_TX0P	Y33	PCIE_GTX_MRX_P0	C58	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_P0
T3 PAD	PCIE_MTX_C_GRX_N0	Y37	PCIE_RX0N	PCIE_TX0N	Y32	PCIE_GTX_MRX_N0	C66	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_N0
	PCIE_MTX_C_GRX_P1	Y35	PCIE_RX1P	PCIE_TX1P	W33	PCIE_GTX_MRX_P1	C68	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_P1
	PCIE_MTX_C_GRX_N1	W36	PCIE_RX1N	PCIE_TX1N	W32	PCIE_GTX_MRX_N1	C79	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_N1
	PCIE_MTX_C_GRX_P2	W38	PCIE_RX2P	PCIE_TX2P	U33	PCIE_GTX_MRX_P2	C83	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_P2
	PCIE_MTX_C_GRX_N2	V37	PCIE_RX2N	PCIE_TX2N	U32	PCIE_GTX_MRX_N2	C86	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_N2
	PCIE_MTX_C_GRX_P3	V35	PCIE_RX3P	PCIE_TX3P	U30	PCIE_GTX_MRX_P3	C87	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_P3
	PCIE_MTX_C_GRX_N3	U36	PCIE_RX3N	PCIE_TX3N	U29	PCIE_GTX_MRX_N3	C94	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_N3
	PCIE_MTX_C_GRX_P4	U38	PCIE_RX4P	PCIE_TX4P	T33	PCIE_GTX_MRX_P4	C95	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_P4
	PCIE_MTX_C_GRX_N4	T37	PCIE_RX4N	PCIE_TX4N	T32	PCIE_GTX_MRX_N4	C104	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_N4
	PCIE_MTX_C_GRX_P5	T35	PCIE_RX5P	PCIE_TX5P	T30	PCIE_GTX_MRX_P5	C105	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_P5
	PCIE_MTX_C_GRX_N5	R36	PCIE_RX5N	PCIE_TX5N	T29	PCIE_GTX_MRX_N5	C108	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_N5
	PCIE_MTX_C_GRX_P6	R38	PCIE_RX6P	PCIE_TX6P	P33	PCIE_GTX_MRX_P6	C109	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_P6
	PCIE_MTX_C_GRX_N6	P37	PCIE_RX6N	PCIE_TX6N	P32	PCIE_GTX_MRX_N6	C116	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_N6
T5 PAD	PCIE_MTX_C_GRX_P7	P35	PCIE_RX7P	PCIE_TX7P	P30	PCIE_GTX_MRX_P7	C117	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_P7
T1 PAD	PCIE_MTX_C_GRX_N7	N36	PCIE_RX7N	PCIE_TX7N	P29	PCIE_GTX_MRX_N7	C122	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_N7
	PCIE_MTX_C_GRX_P8	N38	PCIE_RX8P	PCIE_TX8P	N33	PCIE_GTX_MRX_P8	C124	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_P8
	PCIE_MTX_C_GRX_N8	M37	PCIE_RX8N	PCIE_TX8N	N32	PCIE_GTX_MRX_N8	C128	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_N8
	PCIE_MTX_C_GRX_P9	M35	PCIE_RX9P	PCIE_TX9P	N30	PCIE_GTX_MRX_P9	C130	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_P9
	PCIE_MTX_C_GRX_N9	L36	PCIE_RX9N	PCIE_TX9N	N29	PCIE_GTX_MRX_N9	C135	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_N9
	PCIE_MTX_C_GRX_P10	L38	PCIE_RX10P	PCIE_TX10P	L33	PCIE_GTX_MRX_P10	C139	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_P10
	PCIE_MTX_C_GRX_N10	K37	PCIE_RX10N	PCIE_TX10N	L32	PCIE_GTX_MRX_N10	C144	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_N10
	PCIE_MTX_C_GRX_P11	K35	PCIE_RX11P	PCIE_TX11P	L30	PCIE_GTX_MRX_P11	C146	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_P11
	PCIE_MTX_C_GRX_N11	J36	PCIE_RX11N	PCIE_TX11N	L29	PCIE_GTX_MRX_N11	C149	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_N11
	PCIE_MTX_C_GRX_P12	J38	PCIE_RX12P	PCIE_TX12P	K33	PCIE_GTX_MRX_P12	C150	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_P12
	PCIE_MTX_C_GRX_N12	H37	PCIE_RX12N	PCIE_TX12N	K32	PCIE_GTX_MRX_N12	C157	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_N12
	PCIE_MTX_C_GRX_P13	H35	PCIE_RX13P	PCIE_TX13P	J33	PCIE_GTX_MRX_P13	C158	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_P13
	PCIE_MTX_C_GRX_N13	G36	PCIE_RX13N	PCIE_TX13N	J32	PCIE_GTX_MRX_N13	C162	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_N13
	PCIE_MTX_C_GRX_P14	G38	PCIE_RX14P	PCIE_TX14P	K30	PCIE_GTX_MRX_P14	C163	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_P14
	PCIE_MTX_C_GRX_N14	F37	PCIE_RX14N	PCIE_TX14N	K29	PCIE_GTX_MRX_N14	C165	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_N14
T6 PAD	PCIE_MTX_C_GRX_P15	F35	PCIE_RX15P	PCIE_TX15P	H33	PCIE_GTX_MRX_P15	C166	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_P15
T7 PAD	PCIE_MTX_C_GRX_N15	F37	PCIE_RX15N	PCIE_TX15N	H32	PCIE_GTX_MRX_N15	C168	PM@ 0.1U_0402_16V7K	PCIE_GTX_C_MRX_N15

CLOCK

<25> CLK_PCIE_VGA → CLK_PCIE_VGA AB35 PCIE_REFCLKP

<25> CLK_PCIE_VGA# → CLK_PCIE_VGA# AA36 PCIE_REFCLKN

MAD@ R339 10K_0402_5% PWRGOOD_BUF → AJ21 NC#1, AK21 NC#2, AH16 NC_PWRGOOD

<28> PLTRST_VGA# → PLTRST_VGA# AA30 PERSTB

CALIBRATION

PCIE_CALRP Y30 — R44 1.27K_0402_1% PM@ — 1 2

PCIE_CALRN Y29 — R43 2K_0402_1% PM@ — 1 2 — +1.1VS

216-0729042-00 A13 M96 BGA 962P 030

@

the same with M86

U4G

LVDS CONTROL

VARY_BL AK27 — PM@ R161 10K_0402_5% — VGA_PWM <22>

DIGON AJ27 — R162 PM@10K_0402_5% — VGA_ENVDD <22>

TXCLK_UP_DPF3P	AK35	VGA_LVDS_BCLK <22>
TXCLK_UN_DPF3N	AL36	VGA_LVDS_BCLK# <22>
TXOUT_U0P_DPF2P	AJ38	VGA_LVDS_B0 <22>
TXOUT_U0N_DPF2N	AK37	VGA_LVDS_B0# <22>
TXOUT_U1P_DPF1P	AH35	VGA_LVDS_B1 <22>
TXOUT_U1N_DPF1N	AJ36	VGA_LVDS_B1# <22>
TXOUT_U2P_DPF0P	AG38	VGA_LVDS_B2 <22>
TXOUT_U2N_DPF0N	AH37	VGA_LVDS_B2# <22>
TXOUT_U3P	AF35	
TXOUT_U3N	AG36	

LVTMDP

TXCLK_LP_DPE3P	AP34	VGA_LVDS_ACLK <22>
TXCLK_LN_DPE3N	AR34	VGA_LVDS_ACLK# <22>
TXOUT_L0P_DPE2P	AW37	VGA_LVDS_A0 <22>
TXOUT_L0N_DPE2N	AU35	VGA_LVDS_A0# <22>
TXOUT_L1P_DPE1P	AR37	VGA_LVDS_A1 <22>
TXOUT_L1N_DPE1N	AU39	VGA_LVDS_A1# <22>
TXOUT_L2P_DPE0P	AP35	VGA_LVDS_A2 <22>
TXOUT_L2N_DPE0N	AR35	VGA_LVDS_A2# <22>
TXOUT_L3P	AN36	
TXOUT_L3N	AP37	

216-0729042-00 A13 M96 BGA 962P 030

@

Need check

+1.8VSDGPU — R115 M97@ 2K_0402_1% — PWRGOOD_BUF

+3VS_DELAY — R116 @ 2K_0402_1% — R118 @ 2.37K_0402_1% item 02, Add M97@ 05/06

R117 M97@ 0_0402_5% — EC_VGAPWRGOOD <38>

C251 M97@ 0.22U_0402_10V4Z

Security Classification	Compal Secret Data		
Issued Date	2009/02/24	Deciphered Date	2009/07/15

Compal Electronics, Inc.

Title: SCHEMATIC,MB A6001

Size: Custom | Document Number: 401839 | Rev: B

Date: Thursday, June 10, 2010 | Sheet 13 of 59

Strap Name		Pin Straps description	Default Value
TX_PWRS_ENB	GPIO0	**Transmitter Power Saving Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	0
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
	GPIO23 GPIO21	Reserved	0
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.	001 memory apertures CONFIG[3:0] 128 MB 000 256 MB 001 64 MB 010
BIOS_ROM_EN	GPIO22	**Enable external BIOS ROM device** 0: Diable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	1 1
	GENERICC H2SYNC	Reserved Reserved	0 0
VIP_DEVICE_STRAP_EN	V2SYNC		0

U4B

MUTI GFX

DPA
- AU24 TXCAP_DPA3P — VGA_HDMI_CLK+ — VGA_HDMI_CLK+ <20>
- AV23 TXCAM_DPA3N — VGA_HDMI_CLK- — VGA_HDMI_CLK- <20>
- AT25 TX0P_DPA2P — VGA_HDMI_TX0+ — VGA_HDMI_TX0+ <20>
- AR24 TX0M_DPA2N — VGA_HDMI_TX0- — VGA_HDMI_TX0- <20>
- AU26 TX1P_DPA1P — VGA_HDMI_TX1+ — VGA_HDMI_TX1+ <20>
- AV25 TX1M_DPA1N — VGA_HDMI_TX1- — VGA_HDMI_TX1- <20>
- AT27 TX2P_DPA0P — VGA_HDMI_TX2+ — VGA_HDMI_TX2+ <20>
- AR26 TX2M_DPA0N — VGA_HDMI_TX2- — VGA_HDMI_TX2- <20>

DPB
- AR30 TXCBP_DPB3P
- AT29 TXCBM_DPB3N
- AV31 TX3P_DPB2P
- AU30 TX3M_DPB2N
- AR32 TX4P_DPB1P
- AT31 TX4M_DPB1N
- AT33 TX5P_DPB0P
- AU32 TX5M_DPB0N

DPC
- AU14 TXCCP_DPC3P
- AV13 TXCCM_DPC3N
- AT15 TX0P_DPC2P
- AR14 TX0M_DPC2N
- AU16 TX1P_DPC1P
- AV15 TX1M_DPC1N
- AT17 TX2P_DPC0P
- AR16 TX2M_DPC0N

DPD
- AU20 TXCDP_DPD3P
- AT19 TXCDM_DPD3N
- AT21 TX3P_DPD2P
- AR20 TX3M_DPD2N
- AU22 TX4P_DPD1P
- AV21 TX4M_DPD1N
- AT23 TX5P_DPD0P
- AR22 TX5M_DPD0N

2010-02-09 Updated by Koan

Location / VRAM	MEM_ID0 (R110)	MEM_ID1 (R109)	MEM_ID2 (R108)	MEM_ID3 (R8)
Samsung (1GB)	1	0	0	0
HYNIX (1GB)	0	0	0	0
Samsung (512MB)	1	1	0	0
HYNIX (512MB)	0	1	0	0

MEM_ID0 MEM_ID1 MEM_ID2 MEM_ID3 — MemoryID table

T4PAD T8PAD

DVPCNTL_MVP_0 AR8
DVPCNTL_MVP_1 AU8
DVPCNTL_0 AP8
DVPCNTL_1 AW8
DVPCNTL_2 AR3
DVPCLK AR1
DVPDATA_0 AU1
DVPDATA_1 AU3
DVPDATA_2 AR2
DVPDATA_3 AR4
DVPDATA_4 AW5
DVPDATA_5 AU5
DVPDATA_6 AR6
DVPDATA_7 AW6
DVPDATA_8 AU6
DVPDATA_9 AT7
DVPDATA_10 AV7
DVPDATA_11 AN7
DVPDATA_12 AV9
DVPDATA_13 AT9
DVPDATA_14 AR10
DVPDATA_15 AW10
DVPDATA_16 AU10
DVPDATA_17 AP10
DVPDATA_18 AV11
DVPDATA_19 AT11
DVPDATA_20 AR12
DVPDATA_21 AW12
DVPDATA_22 AU12
DVPDATA_23 AP12

I2C
- SCL AK26 — <22> VGA_LVDS_SCL — VGA_LVDS_SCL
- SDA AJ26 — <22> VGA_LVDS_SDA — VGA_LVDS_SDA

GENERAL PURPOSE I/O

GPIO_0	AH20	VGA_GPIO0	
GPIO_1	AH18	VGA_GPIO1	
GPIO_2	AN16	VGA_GPIO2	
GPIO_3_SMBDATA	AH23	EC_SMB_DA2 R97 0_0402_5%	SMB_DA
GPIO_4_SMBCLK	AJ23	EC_SMB_CK2 R96 0_0402_5%	SMB_CLK
GPIO_5_AC_BATT	AH17	R27 0_0402_5%	VGA_AC_DET_R
GPIO_6	AJ17		
GPIO_7_BLON	AK17	<22> VGA_ENBKL	VGA_ENBKL
GPIO_8_ROMSO	AJ13		SOUT_GPIO8
GPIO_9_ROMSI	AH15		SIN_GPIO9
GPIO_10_ROMSCK	AJ16		
GPIO_11	AK16	VGA_GPIO11	
GPIO_12	AL16	VGA_GPIO12	
GPIO_13	AM16	VGA_GPIO13	
GPIO_14_HPD2	AM14		
GPIO_15_PWRCNTL_0	AM13	GPU_VID0	
GPIO_16_SSIN	AK14		
GPIO_17_THERMAL_INT	AG30	VGA_THERM#	
GPIO_18_HPD3	AN14		
GPIO_19_CTF	AM17		
GPIO_20_PWRCNTL_1	AL13	GPU_VID1	
GPIO_21_BB_EN	AJ14	VGA_GPIO21	
GPIO_22_ROMCSB	AK13	ROMSE_GPIO22	
GPIO_23_CLKREQB	AN13	PEG_CLKREQ#	
JTAG_TRSTB	AM23	GPIO24_TRSTB	
JTAG_TDI	AN23	GPIO25_TDI	
JTAG_TCK	AK23	GPIO26_TCK	
JTAG_TMS	AL24	GPIO27_TMS	
JTAG_TDO	AM24	GPIO28_TDO	
GENERICA	AJ19		
GENERICB	AK19		
GENERICC	AJ20	GENERICC	
GENERICD	AK20		
GENERICE_HPD4	AJ24		
GENERICF	AH26		
GENERICG	AH24		

DAC1
- R AD39 — VGA_CRT_R — VGA_CRT_R <21>
- RB AD37
- G AE36 — VGA_CRT_G — VGA_CRT_G <21>
- GB AD35
- B AF37 — VGA_CRT_B — VGA_CRT_B <21>
- BB AE38
- HSYNC AC36 — VGA_HSYNC — VGA_HSYNC <21>
- VSYNC AC38 — VGA_VSYNC — VGA_VSYNC <21>
- RSET AB34 — R40 PM@ 499_0402_1%
- AVDD AD34 — AVDD — AVDD — 70mA
- AVSSQ AE34
- VDD1DI AC33 — VDD1DI — VDD1DI — 50mA
- VSS1DI AC34

DAC2
- R2 AC30
- R2B AC31
- G2 AD30
- G2B AD31
- B2 AE30
- B2B AF31
- C AC32
- Y AD32
- COMP AE32
- H2SYNC AD29 — H2SYNC
- V2SYNC AC29 — V2SYNC — 40mA
- VDD2DI AG31 — VDD2DI — VDD2DI
- VSS2DI AG32 — 135mA
- A2VDD AG33 — A2VDD — A2VDD
- A2VDDQ AD33 — A2VDDQ — A2VDDQ — 1mA
- A2VSSQ AF33
- R2SET AA29 — R38 715_0402_1% PM@

DDC/AUX
- DDC1CLK AM26 — VGA_DDC_CLK
- DDC1DATA AN26 — VGA_DDC_DATA — CRT
- AUX1P AL27
- AUX1N AL29
- DDC2CLK AL19 — VGA_HDMI_SCL
- DDC2DATA AL19 — VGA_HDMI_SDA — HDMI
- AUX2P AN20
- AUX2N AM20
- DDCCLK_AUX3P AL30
- DDCDATA_AUX3N AM30
- DDCCLK_AUX4P AL29
- DDCDATA_AUX4N AM29
- DDCCLK_AUX5P AN21
- DDCDATA_AUX5N AM21
- DDC6CLK AJ30
- DDC6DATA AJ31
- NC_DDCCLK_AUX7P AK30
- NC_DDCDATA_AUX7N AK29

PLL/CLOCK
- DPLL_PVDD AM32
- DPLL_PVSS AN32
- DPLL_VDDC AN31
- XTALIN AV33
- XTALOUT AU34

THERMAL
- DPLUS AE29
- DMINUS AG29
- TS_FDO AJ32
- TSVDD AJ33
- TSVSS

VREFG
- VGA_VREF AH13

HPD1
- VGA_HDMI_HPD AK24 — <20> VGA_HDMI_HPD

External VGA Thermal Sensor

+3VS_DELAY — R248 330_0402_5% PM@ — C224 0.1U_0402_16V4Z PM@ — 2200P_0402_50V7K — C223 PM@ — THERM# — PM@ ADM1032ARMZ-2REEL_MSOP8

U1: VDD, D+, D-, THERM#, GND, SCLK, SDATA, ALERT#

+3VS_DELAY — R95 4.7K_0402_5% @ — R94 4.7K_0402_5% @

EC_SMB_CK2 <25,38> — EC_SMB_CK2
EC_SMB_DA2 <25,38> — EC_SMB_DA2
VGA_THERM# <38> — VGA_THERM#

+3VS_DELAY — R250 4.7K_0402_5% PM@ — THERM#

+3VS_DELAY

R59 0_0805_5% @ — +3VS_DELAY — Q1 SI2301BDS_SOT23 PM@ — C201 0.1U_0402_16V7K PM@ — +3VS

R103 MAD@ 100K_0402_5%

R343 M96@ 100K_0402_5% — R343 10K_0402_5% MAD@

R111 MAD@ — <42,46,54> VGA_ON — Q2 SSM3K7002FU_SC70-3 PM@ — C241 M96@ 0.1U_0402_16V4Z

R111 M96@ 200K_0402_5%

PWR Sequence

VGA_CORE (VDDC)
+1.8VS
+3VS_DELAY

CRB recommend 4.7Kohm

+3VS_DELAY — R1 4.7K_0402_5% PM@ — R2 4.7K_0402_5% PM@

3/2 ATI benny suggest

10/22 Add by Vivian

Pull Low at LVDS side

+1.8VSDGPU — R110 10K_0402_5% MEM_ID0 — R109 10K_0402_5% MEM_ID1 — R108 10K_0402_5% MEM_ID2 — R8 10K_0402_5% MEM_ID3

for use SBIOS

R119	3K_0402_5%	VGA_GPIO0	
R120	3K_0402_5%	VGA_GPIO1	
R121	3K_0402_5%	VGA_GPIO2	
R122	3K_0402_5%	SOUT_GPIO8	
R123	3K_0402_5%	SIN_GPIO9	
R124 PM@	3K_0402_5%	VGA_GPIO11	
R125	3K_0402_5%	VGA_GPIO12	
R126	3K_0402_5%	VGA_GPIO13	
R127 PM@	3K_0402_5%	VGA_VSYNC	
R128 PM@	3K_0402_5%	VGA_HSYNC	
R129	3K_0402_5%	V2SYNC	
R130	3K_0402_5%	H2SYNC	
R131	3K_0402_5%	ROMSE_GPIO22	
R132	3K_0402_5%	GENERICC	
R133	3K_0402_5%	VGA_AC_DET_R	
R20	10K_0402_5%	VGA_ENBKL	<38> VGA_AC_DET

Check

<54> GPU_VID0 — <54> GPU_VID1 — <16> VGA_GPIO21 — <25> PEG_CLKREQ#

item 24, add test point for VBBP Controller 05/13

M96 can not support

100P_0402_50V8J C227 @ — GPU_VID1

R142 10K_0402_5% @

10/31 Add

03/06 Add by Tock

Change R1211 part number from SD034499080 to SD034249080

XTALIN — R104 1M_0603_5% PM@ — XTALOUT

Y1 27MHz_16PF_6P27000126 — C225 18P_0402_50V8J PM@ — C229 18P_0402_50V8J PM@

R98 @ — 75_0402_1%

+1.8VSDGPU — R32 499_0402_1% PM@ — R19 249_0402_1% PM@ — C54 0.1U_0402_16V4Z PM@ — VGA_VREF

For ATI debug

+3VS_DELAY — R134 10K_0402_5% GPIO24_TRSTB — R135 10K_0402_5% GPIO25_TDI — R136 10K_0402_5% GPIO26_TCK — R137 10K_0402_5% GPIO27_TMS — R138 10K_0402_5% GPIO28_TDO

ATI Option 2 debug

R265 10K_0402_5% GPIO24_TRSTB

R264 10K_0402_5% GPIO26_TCK — CLK_VGA_27M <23>

<15> TESTEN — R262 10K_0402_5% — +3VS_DELAY

120mA

+1.8VSDGPU — BLM18PG121SN1D_0603 L20 PM@ — 0.1U_0402_16V4Z — C110 PM@ — C41 10U_0603_6.3V6M PM@ — C13 1U_0402_6.3V4Z PM@ — DPLL_PVDD

300mA

+1.1VS — BLM18PG121SN1D_0603 L21 PM@ — 0.1U_0402_16V4Z — C9 PM@ — C33 10U_0603_6.3V6M PM@ — C12 1U_0402_6.3V4Z PM@ — DPLL_VDDC

20mA

+1.8VSDGPU — BLM18PG121SN1D_0603 L22 PM@ — 1U_0402_6.3V4Z — C21 PM@ — C47 10U_0603_6.3V6M PM@ — C253 0.1U_0402_16V4Z PM@ — TSVDD

4/2 Add by Vivian

C814 100P_0402_50V8J PM@ — GPU_VID0

40mA

AVDD — 0.1U_0402_16V4Z — L15 BLM18PG121SN1D_0603 PM@ — +1.8VSDGPU
C30 PM@ 1U_0402_6.3V4Z — C35 PM@ — C29 PM@ 10U_0603_6.3V6M

135mA

VDD1DI — 0.1U_0402_16V4Z — L16 BLM18PG121SN1D_0603 PM@ — +1.8VSDGPU
C89 PM@ 1U_0402_6.3V4Z — C245 PM@ — C252 PM@ 10U_0603_6.3V6M

1mA

VDD2DI — L17 0_0603_5% PM@ — +1.8VSDGPU

A2VDD — L18 PM@ 0_0603_5% — +3VS_DELAY

A2VDDQ — L19 BLM18PG121SN1D_0603 PM@ — +1.8VSDGPU
C633 0.1U_0402_16V4Z PM@

+3VS_DELAY — R10 10K_0402_5% PM@ — R9 10K_0402_5% PM@
VGA_DDC_CLK — VGA_DDC_CLK <21>
VGA_DDC_DATA — VGA_DDC_DATA <21>

4/24 ATI suggest

+3VS_DELAY — R101 2.2K_0402_5% PM@ — R100 2.2K_0402_5% PM@
VGA_HDMI_SCL — VGA_HDMI_SCL <20>
VGA_HDMI_SDA — VGA_HDMI_SDA <20>

216-0729042-00 A13 M96 BGA 962P 030
@

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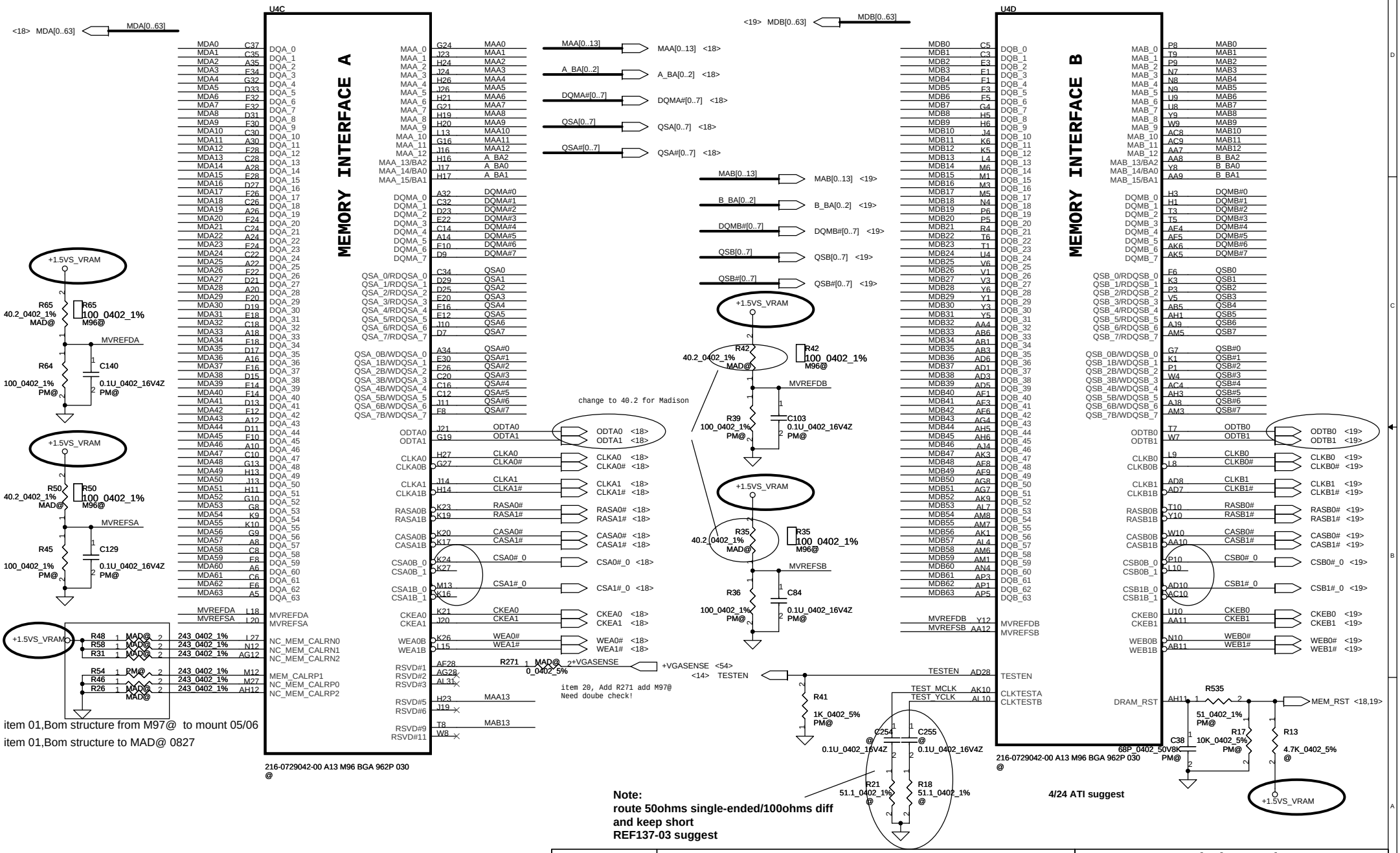

Security Classification	Compal Secret Data		
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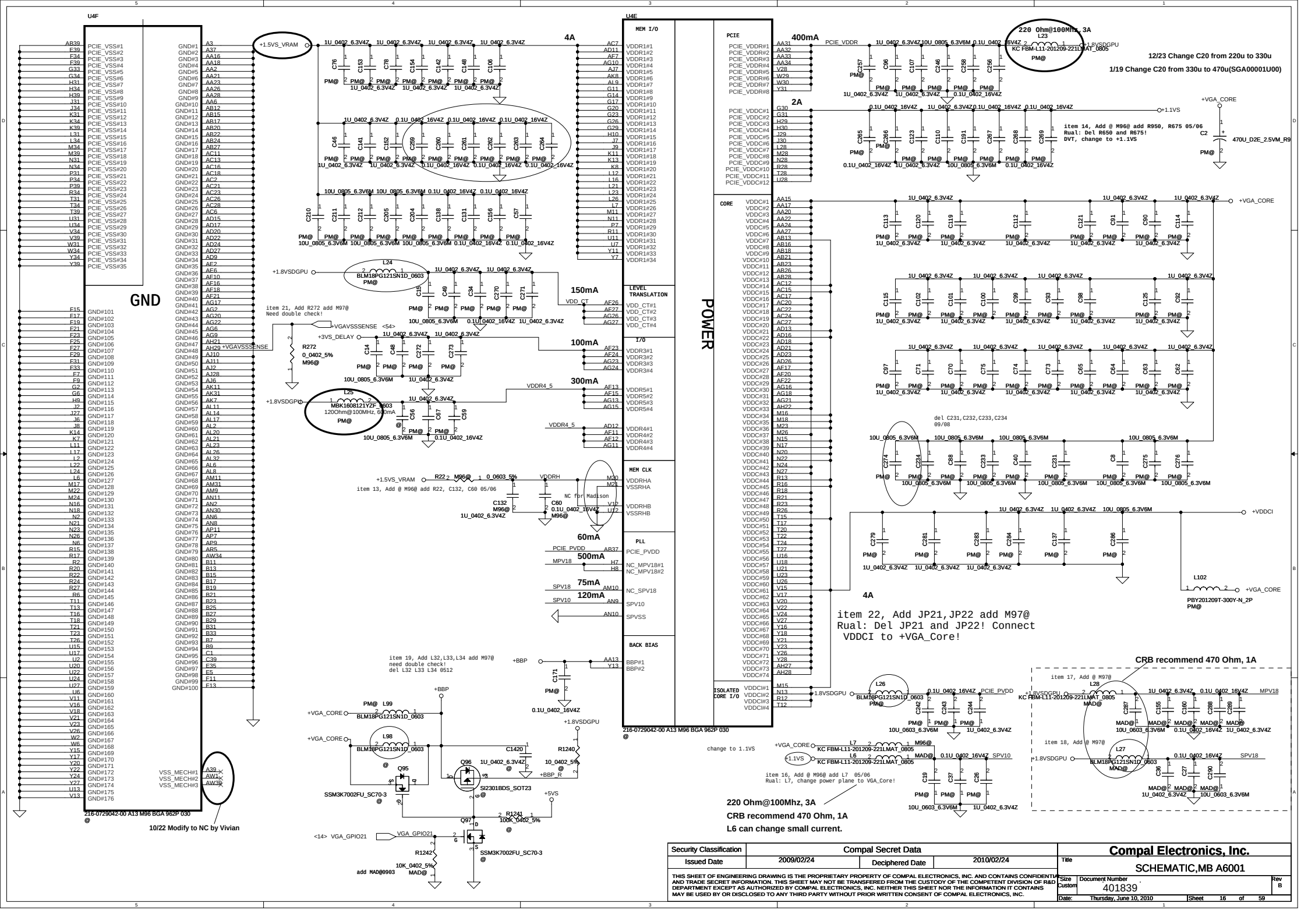

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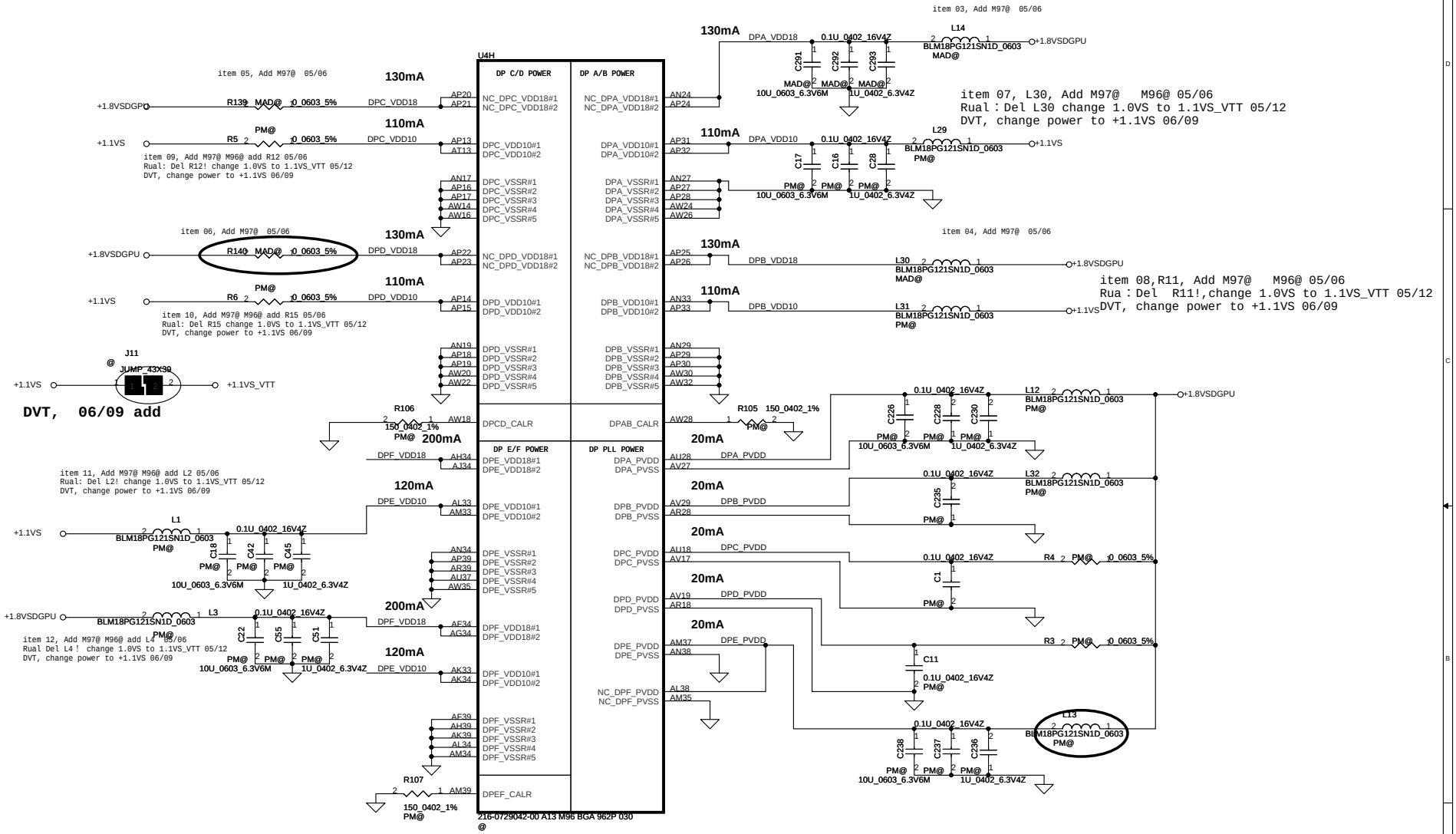

There is no use on DPB/DPC/DPD,DPB_VDD10, DPC_VDD10, DPD_VDD10, DPB_PVDD, DPC_PVDD and DPD_PVDD can be powered without filter

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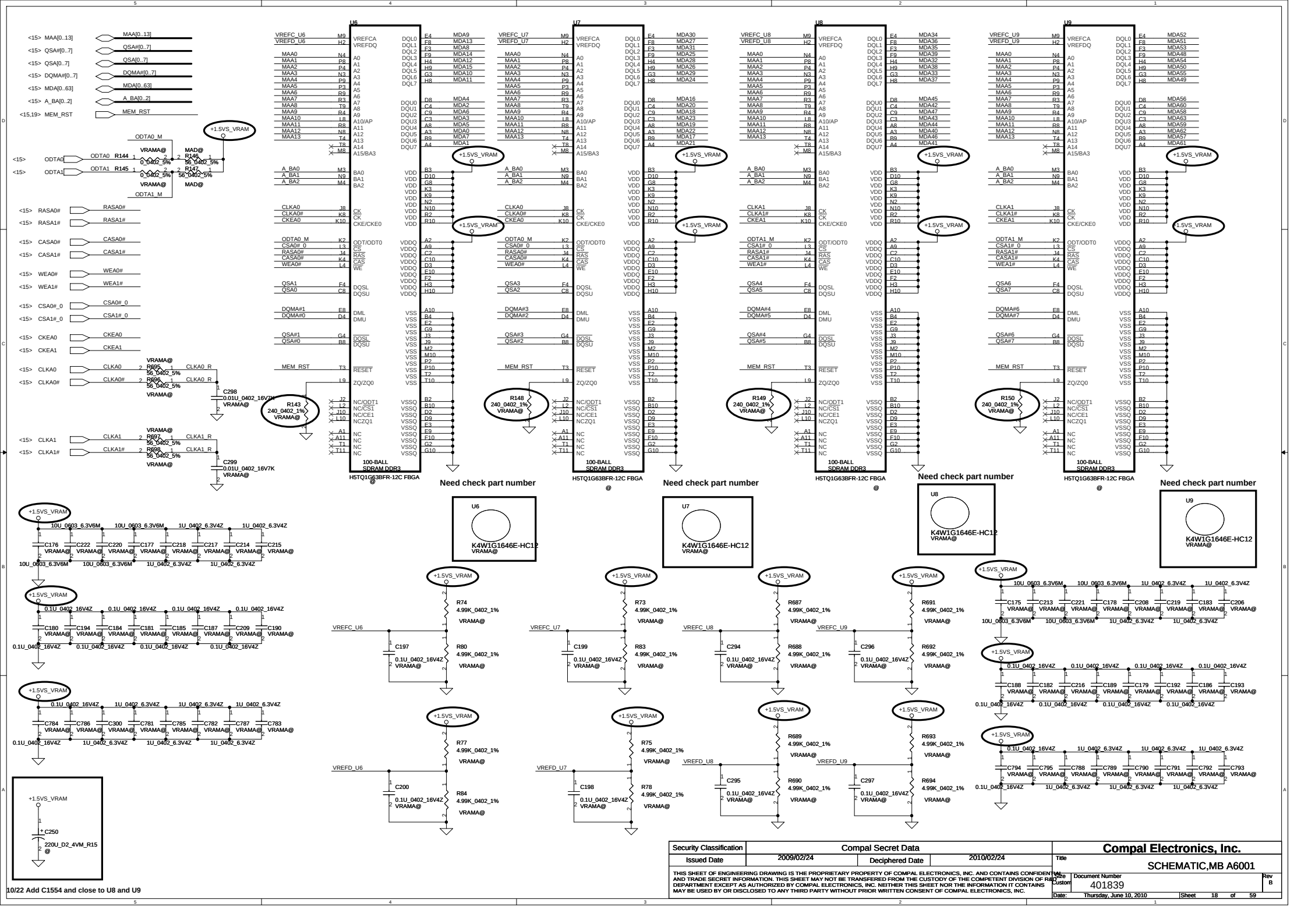

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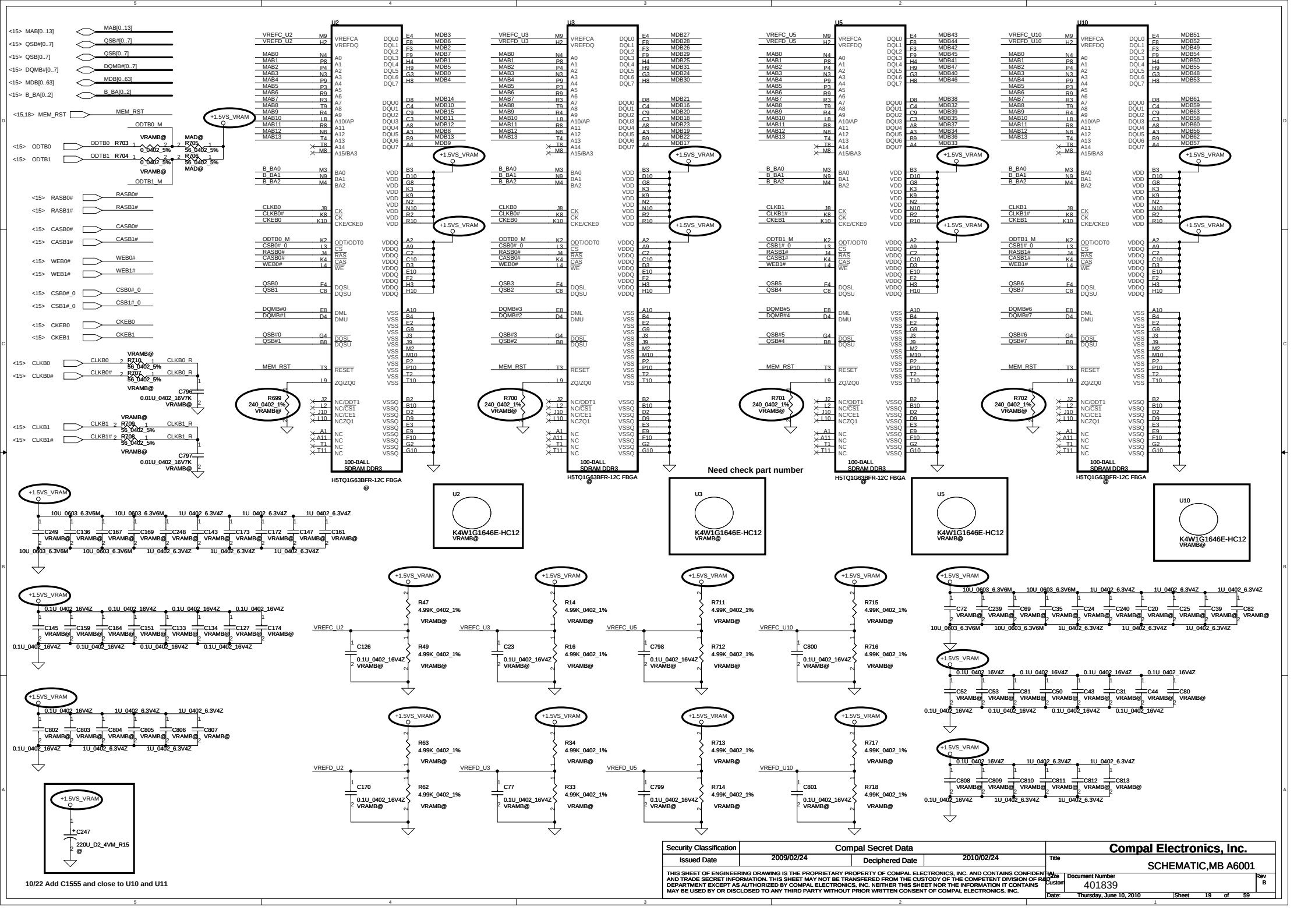

10/22 Add C1555 and close to U10 and U11

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have the pull high on PCH/VGA side

DGPU_SELECT#
L: 0 -> Y(Madison)
H: 1 -> Y(PCH)

DVT, change HDMI detec 06/09

TMDS pull down (500ohm) resistors G9x only

NEAR CONNECT

Same as Nvidia and ATI

L: A=B

OE#--SEL1--SEL2--Result
1----X----X----Hi-Z
0----1----X----A active
0----0----1----B activve
0----0----0----B all port dis

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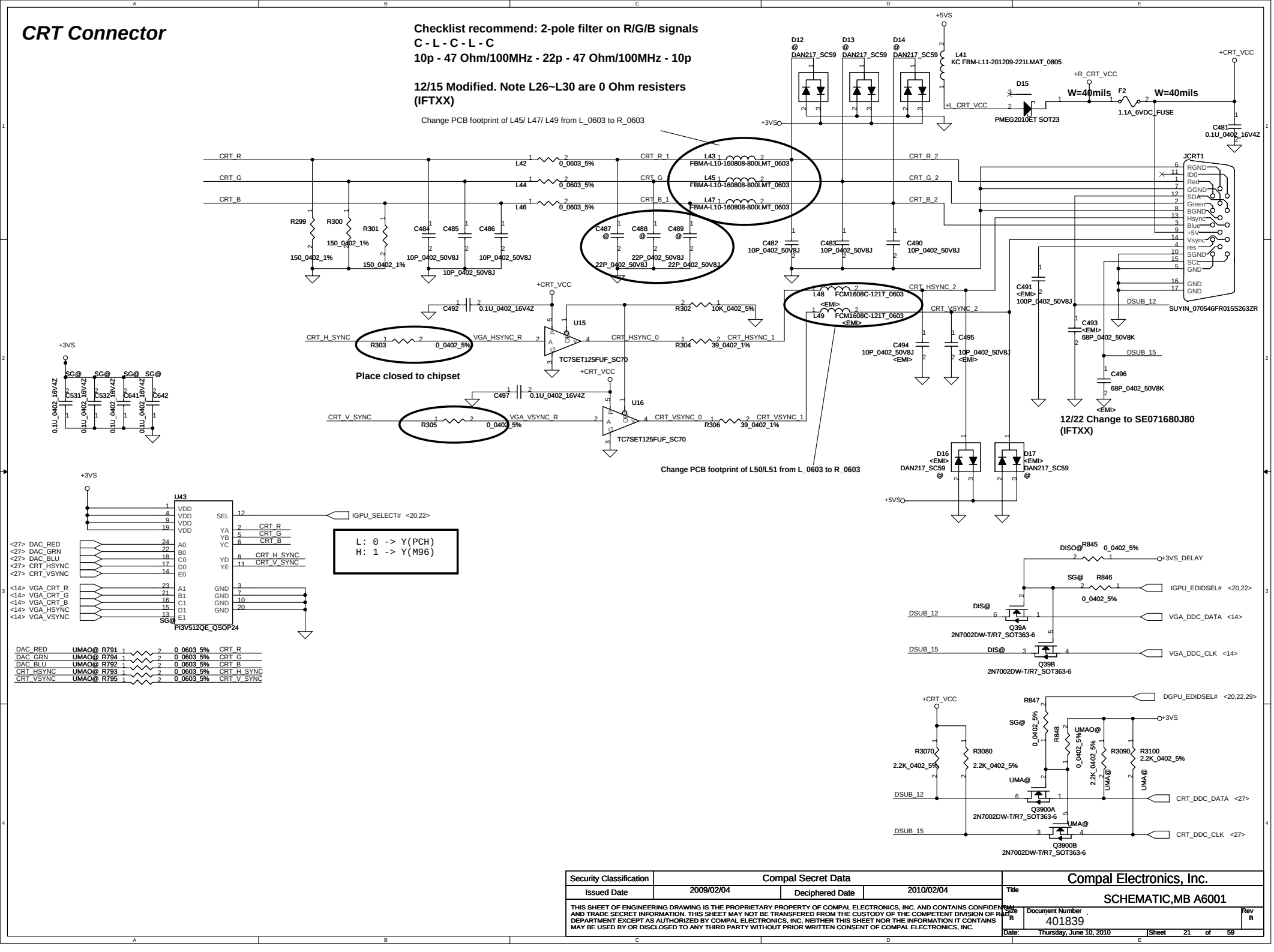
CRT Connector

Checklist recommend: 2-pole filter on R/G/B signals
C - L - C - L - C
10p - 47 Ohm/100MHz - 22p - 47 Ohm/100MHz - 10p

12/15 Modified. Note L26~L30 are 0 Ohm resisters (IFTXX)

Change PCB footprint of L45/ L47/ L49 from L_0603 to R_0603



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Issued Date	2009/02/04	Deciphered Date	2010/02/04

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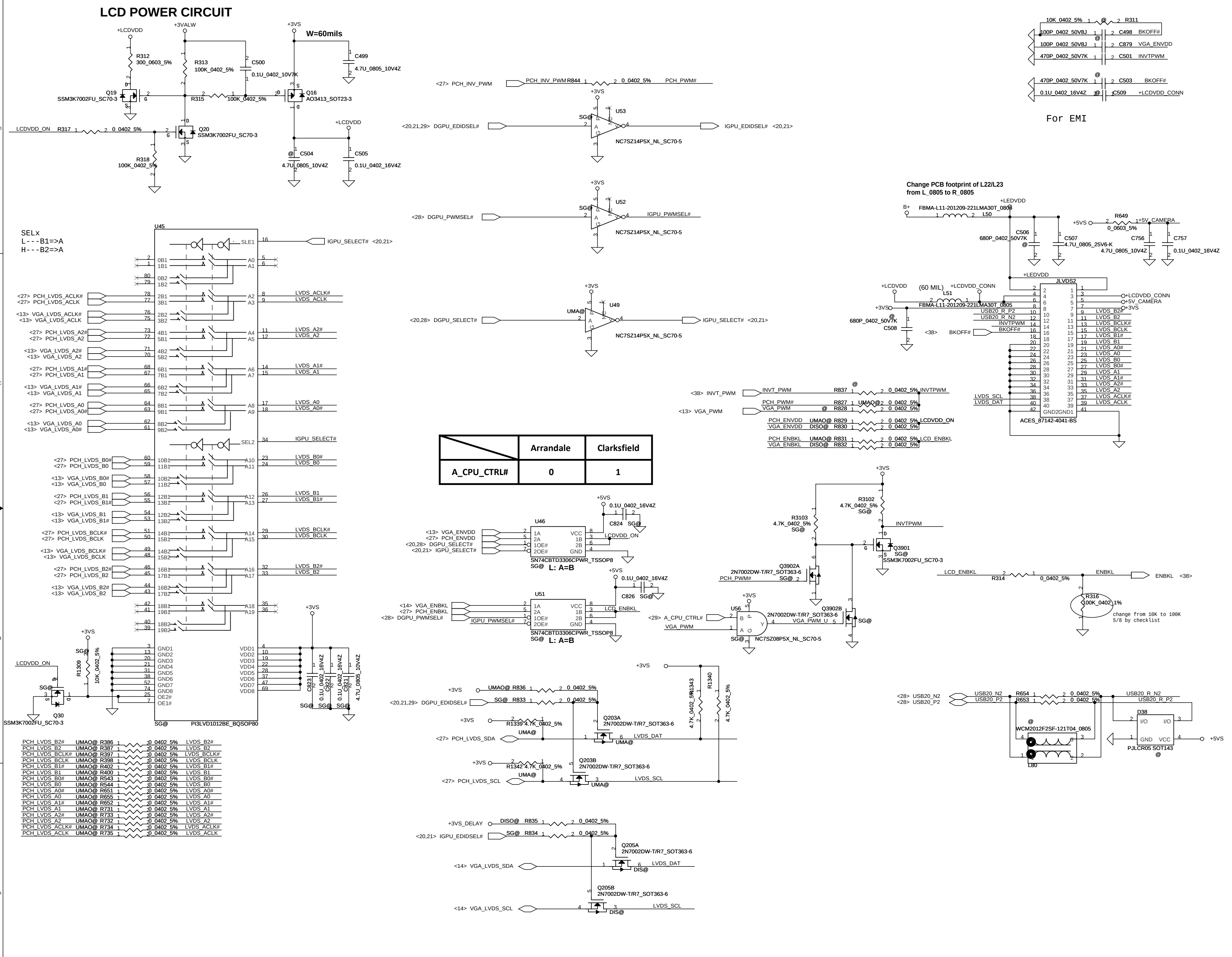

	Arrandale	Clarksfield
A_CPU_CTRL#	0	1

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

Compal Electronics, Inc.

Title: SCHEMATIC,MB A6001

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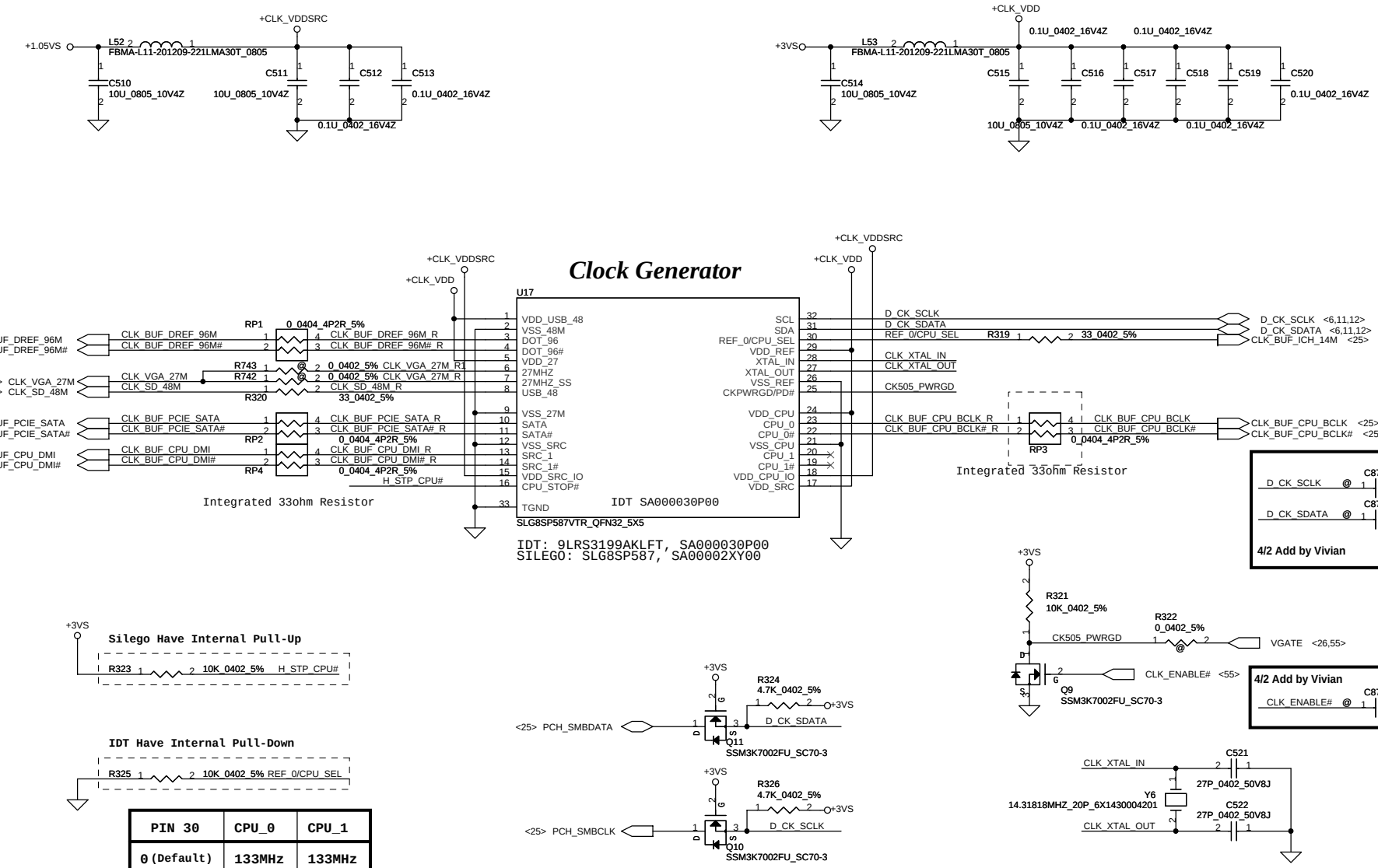

PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/02/04

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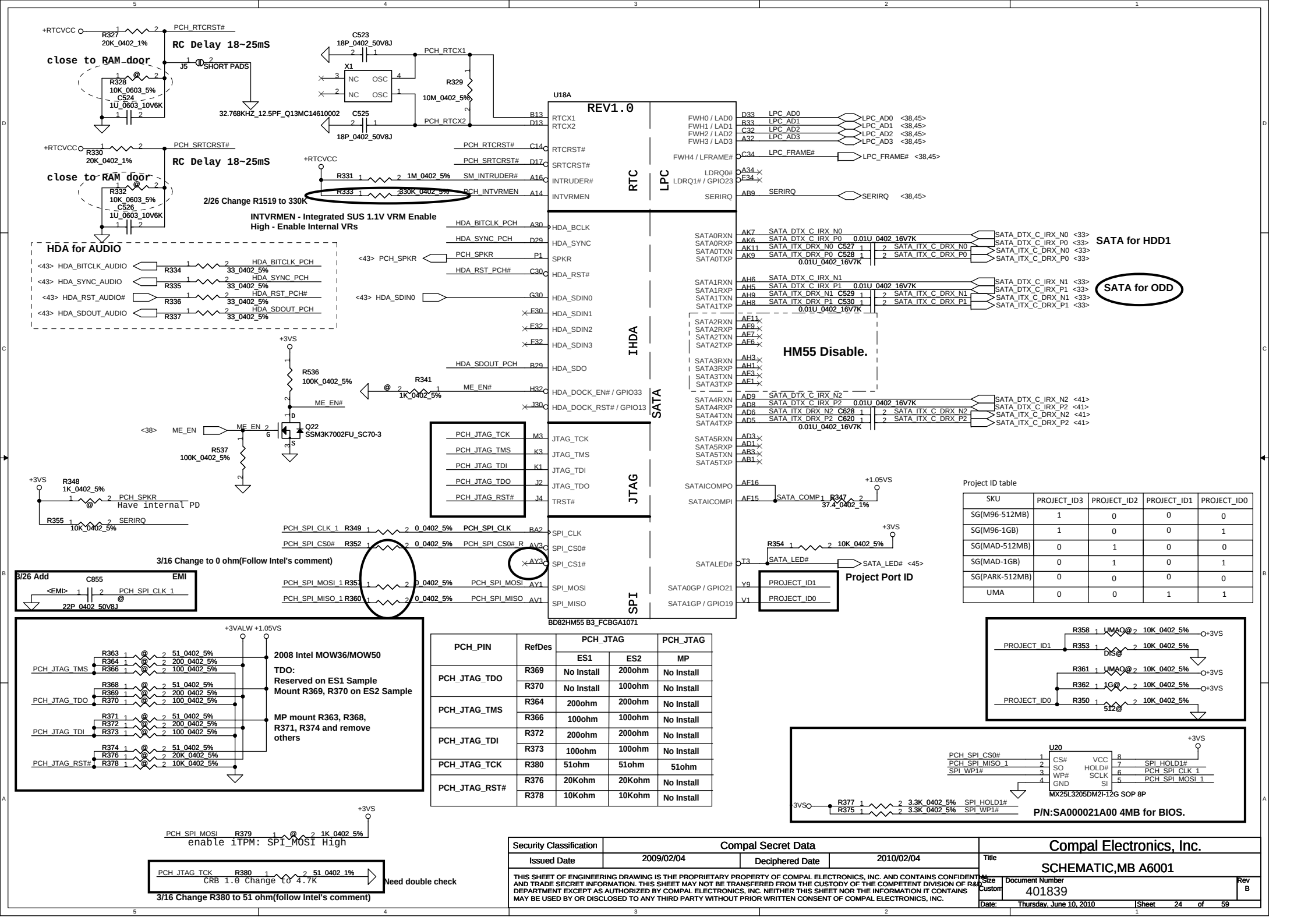

PCH_PIN	RefDes	PCH_JTAG ES1	PCH_JTAG ES2	PCH_JTAG MP
PCH_JTAG_TDO	R369	No Install	200ohm	No Install
	R370	No Install	100ohm	No Install
PCH_JTAG_TMS	R364	200ohm	200ohm	No Install
	R366	100ohm	100ohm	No Install
PCH_JTAG_TDI	R372	200ohm	200ohm	No Install
	R373	100ohm	100ohm	No Install
PCH_JTAG_TCK	R380	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R376	20Kohm	20Kohm	No Install
	R378	10Kohm	10Kohm	No Install

Project ID table

SKU	PROJECT_ID3	PROJECT_ID2	PROJECT_ID1	PROJECT_ID0
SG(M96-512MB)	1	0	0	0
SG(M96-1GB)	1	0	0	1
SG(MAD-512MB)	0	1	0	0
SG(MAD-1GB)	0	1	0	1
SG(PARK-512MB)	0	0	0	0
UMA	0	0	1	1

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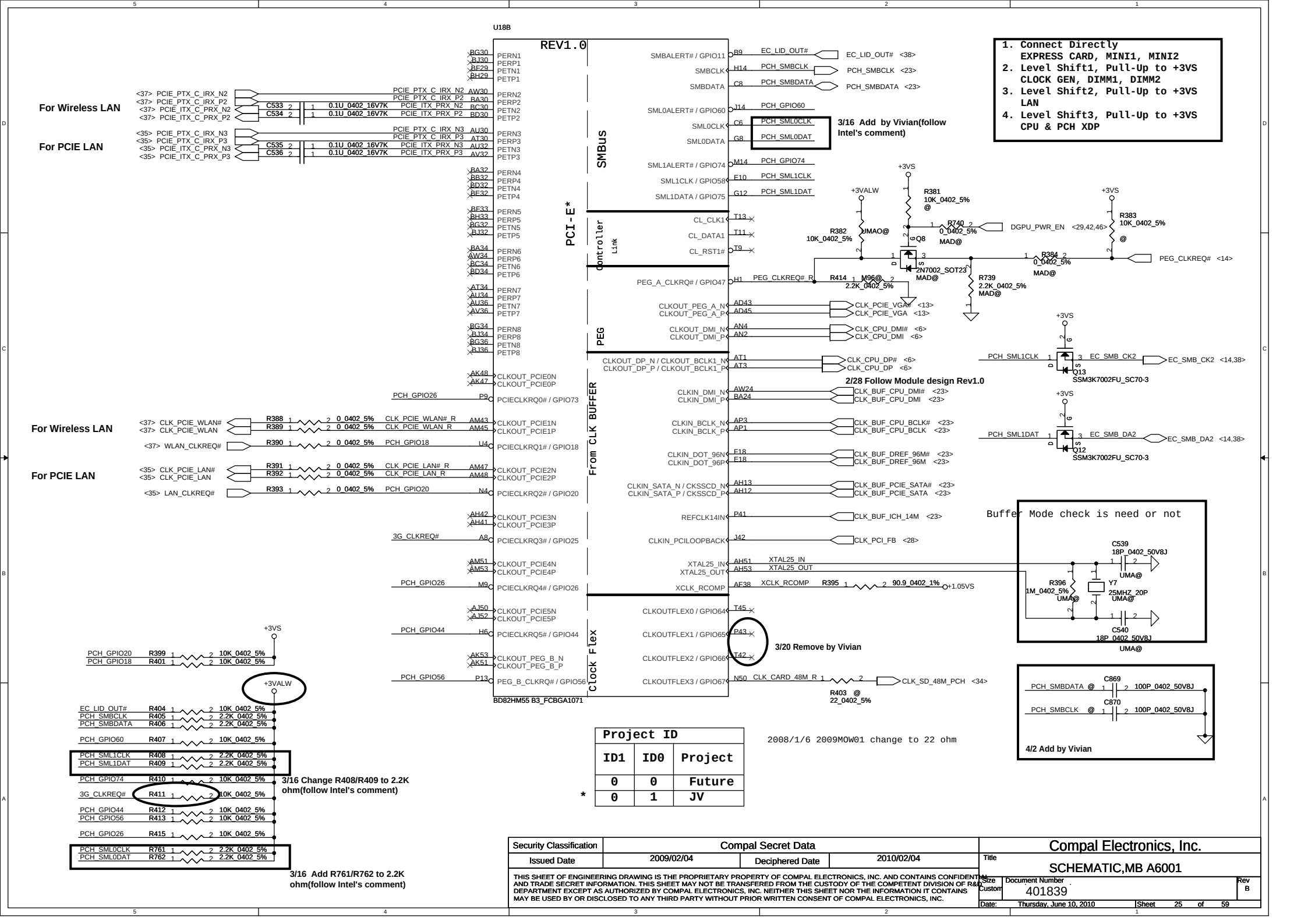
U18B
REV1.0
PCI-E*
SMBus
Controller Link
PEG
From CLK BUFFER
Clock Flex
BD82HM55 B3_FCBGA1071
1. Connect Directly EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS LAN
4. Level Shift3, Pull-Up to +3VS CPU & PCH XDP
For Wireless LAN
For PCIE LAN
3/16 Add by Vivian(follow Intel's comment)
2/28 Follow Module design Rev1.0
3/20 Remove by Vivian
3/16 Change R408/R409 to 2.2K ohm(follow Intel's comment)
3/16 Add R761/R762 to 2.2K ohm(follow Intel's comment)
Buffer Mode check is need or not
4/2 Add by Vivian
2008/1/6 2009MOW01 change to 22 ohm
Project ID
ID1 ID0 Project
0 0 Future
0 1 JV
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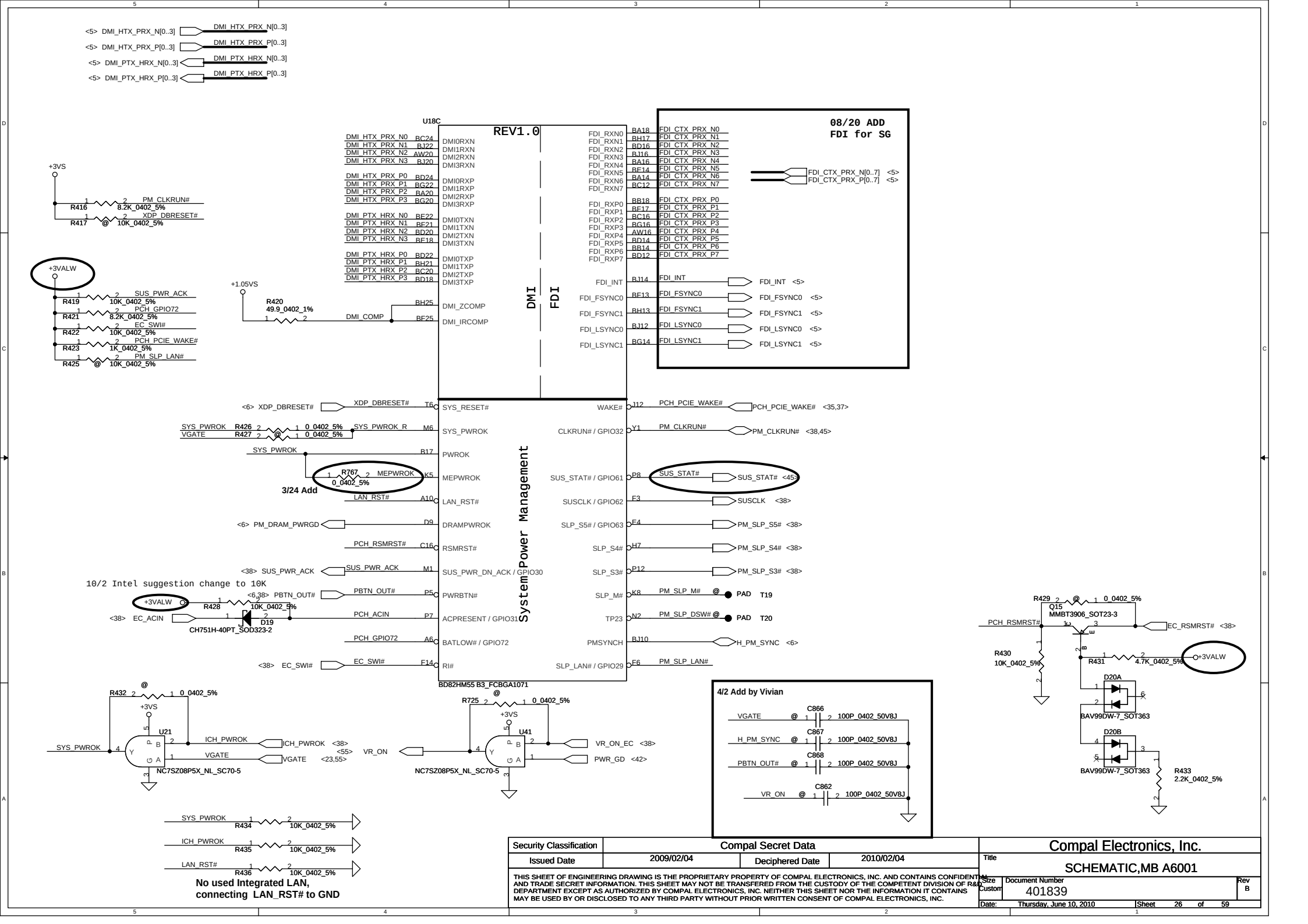

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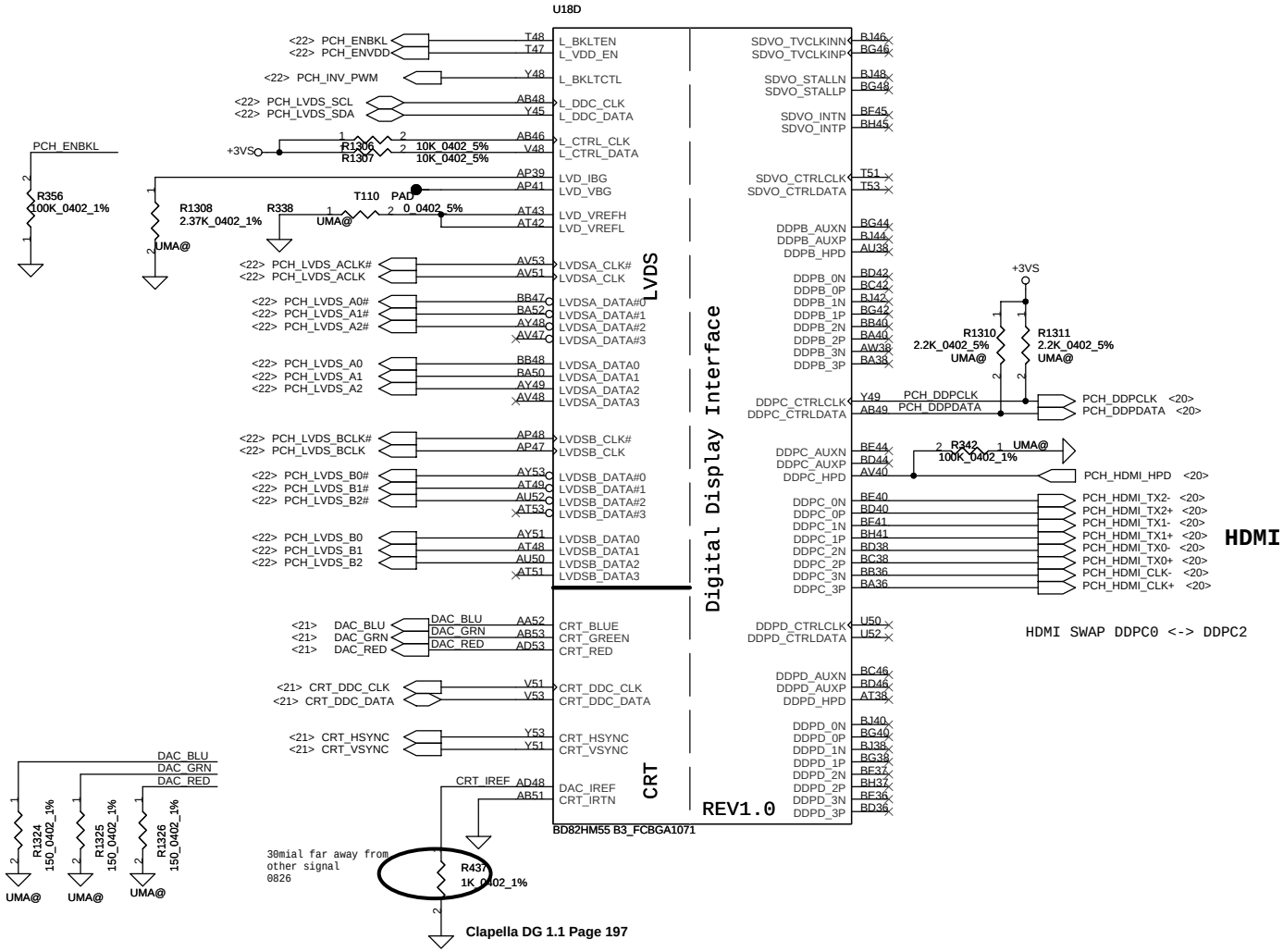

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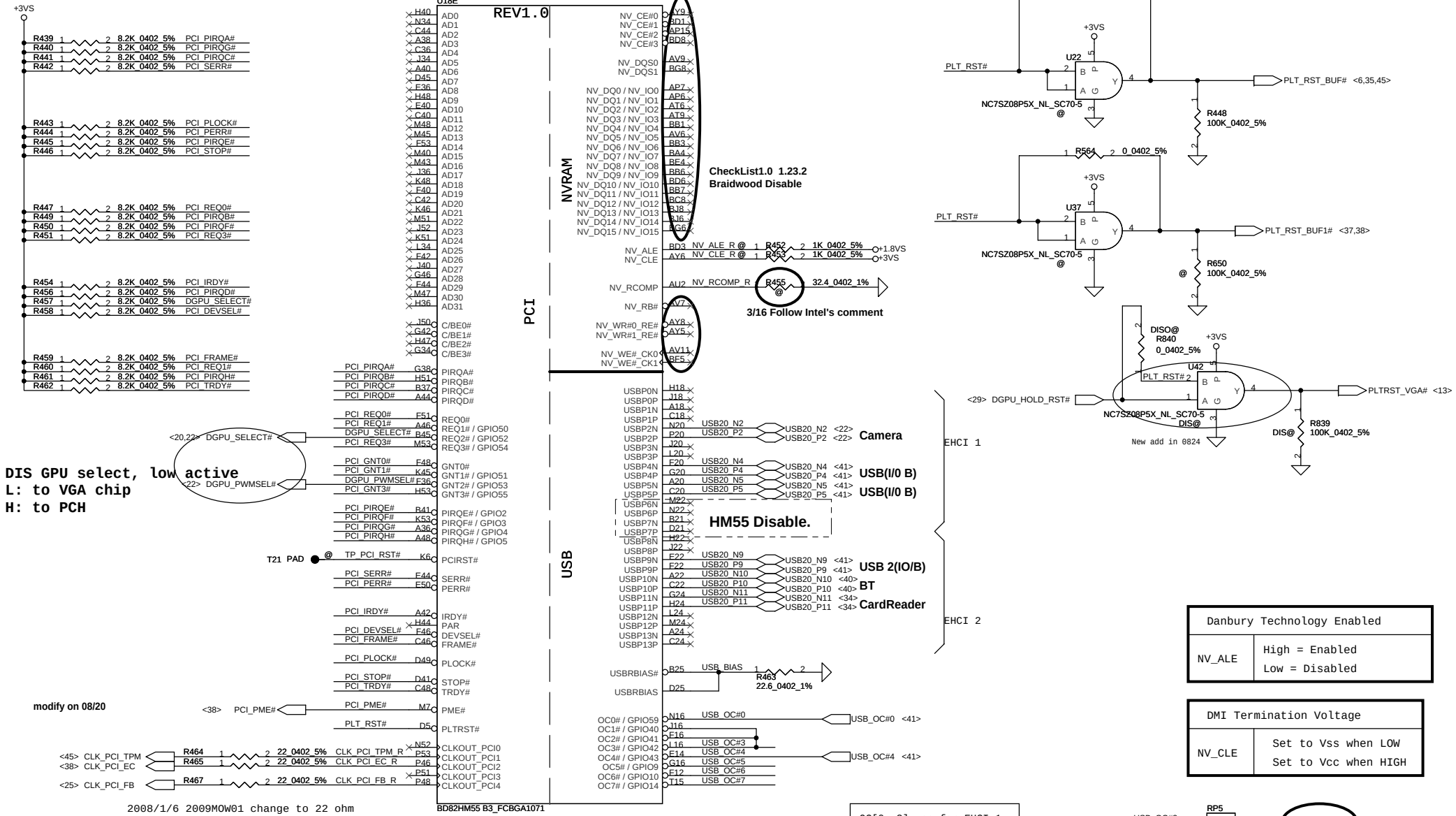

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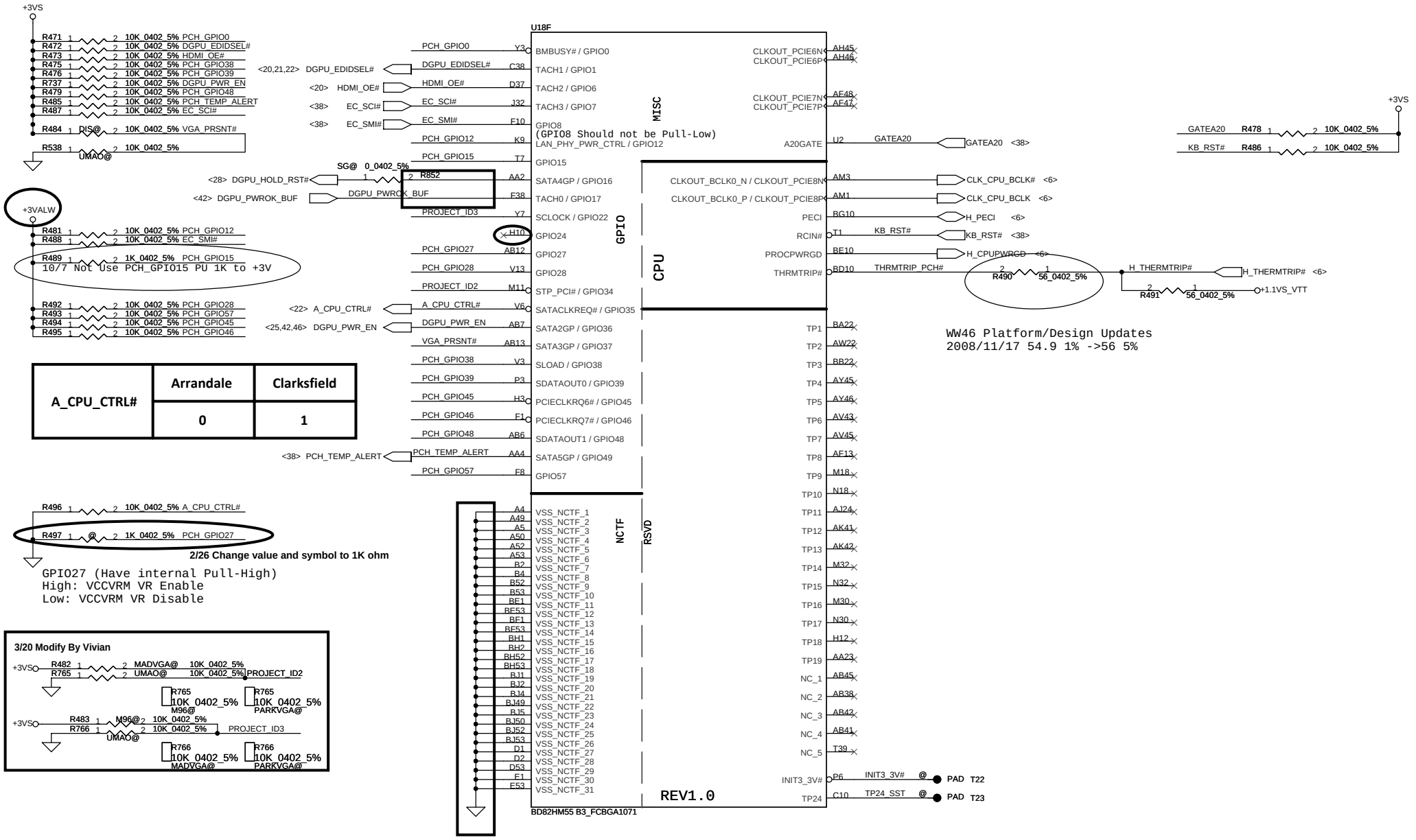

A_CPU_CTRL#	Arrandale	Clarksfield
	0	1

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

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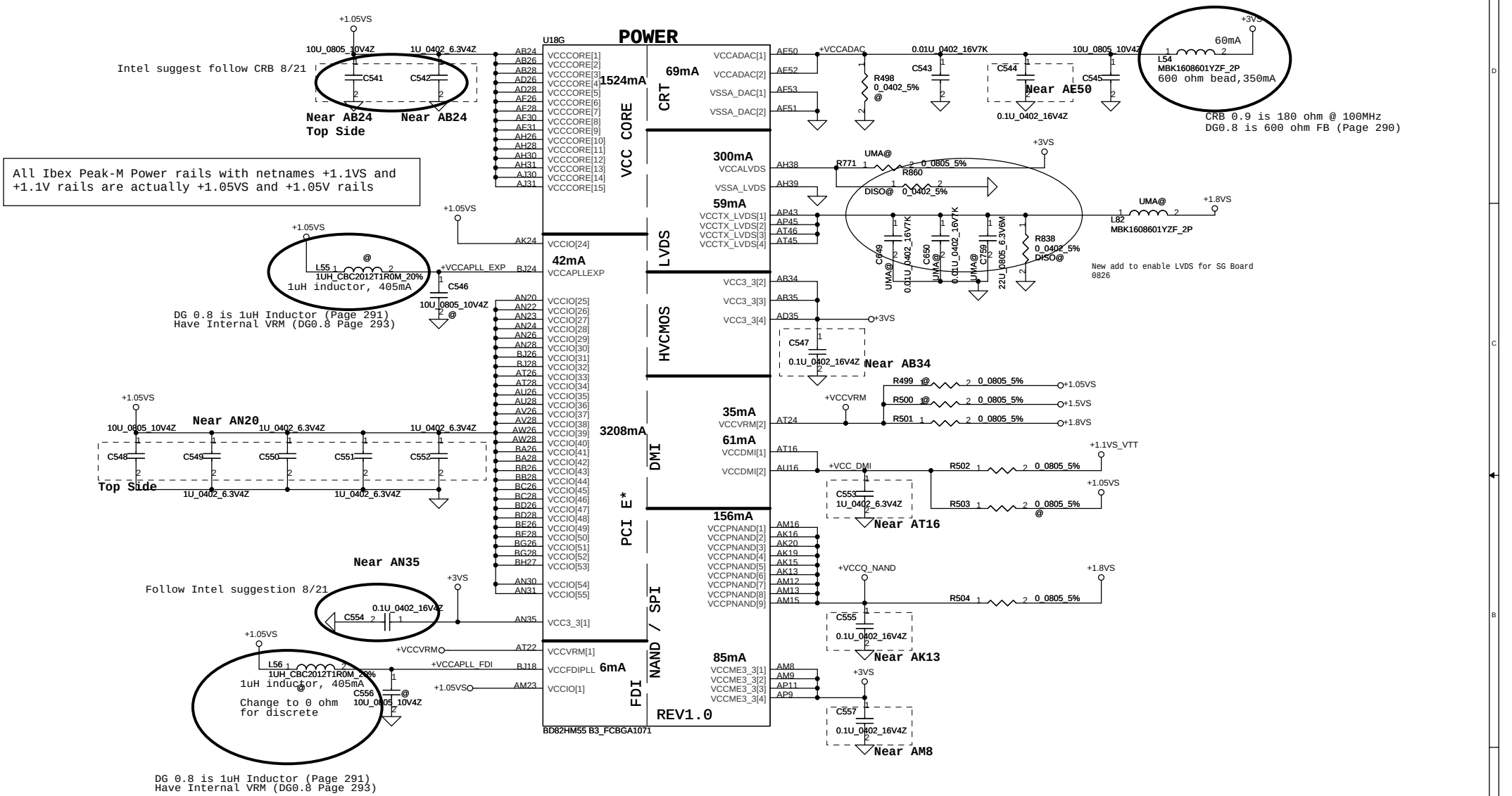

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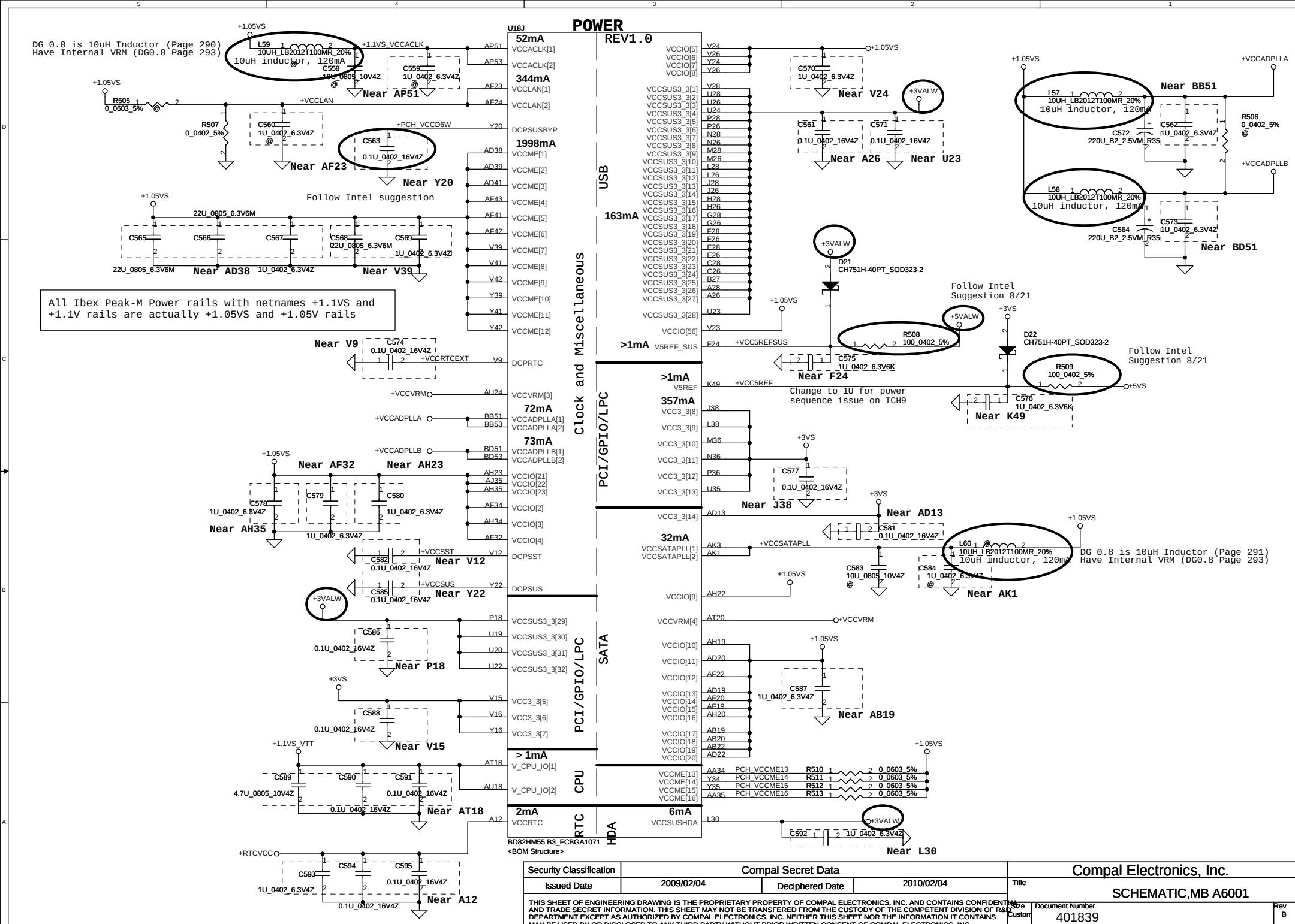
POWER



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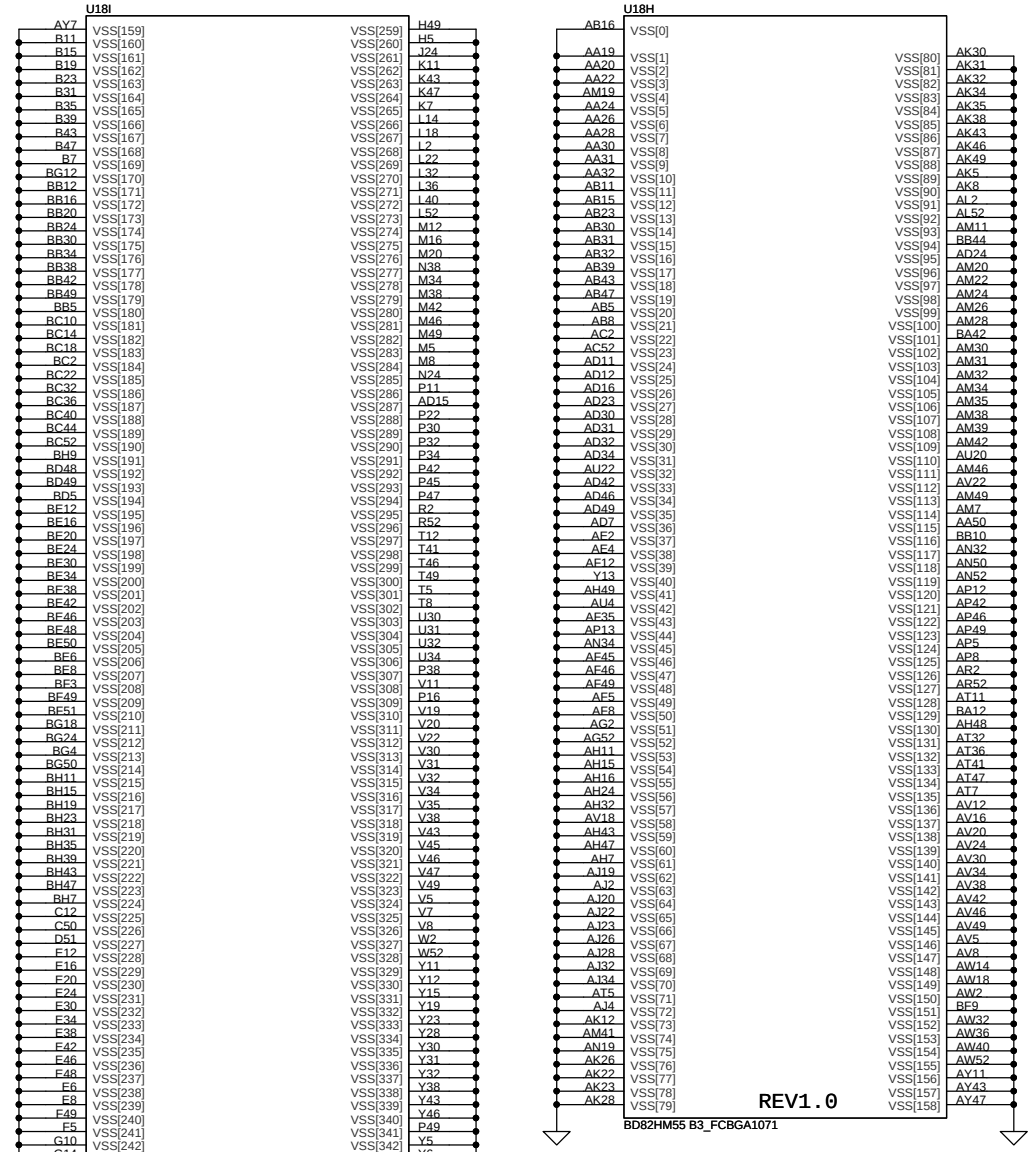

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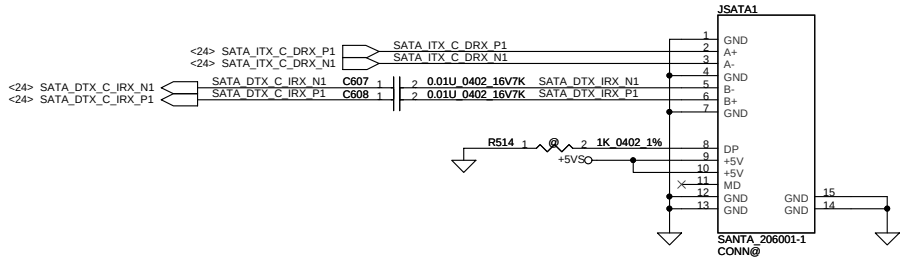
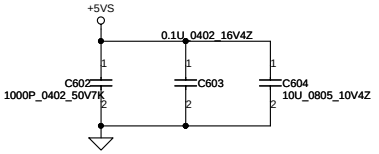
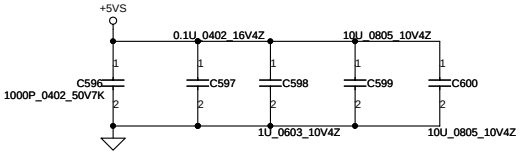
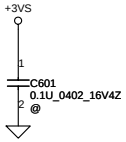
SATA ODD Conn.

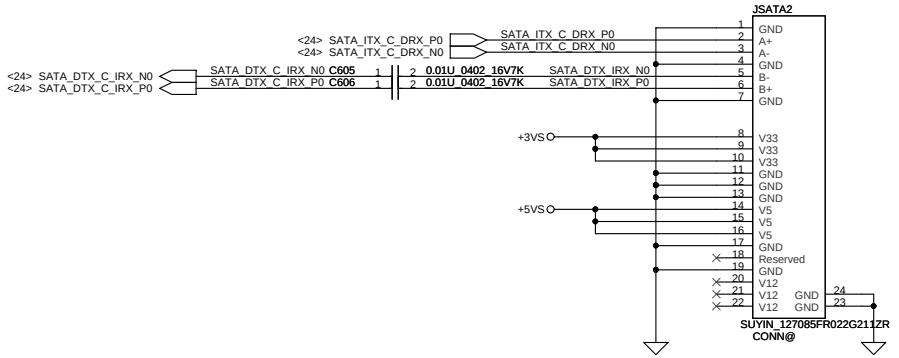




SATA HDD Conn.







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SD,MMC,MS muti-function pin define

MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name
SP1			
SP2	SDWP#		
SP3	SDCD#		
SP4	SDCDAT1		MSWR
SP5			MSBS
SP6			MSCDAT1
SP7	SDCDAT0		MSCDAT0
SP8	SDCDAT7		MSCDAT2
SP9			MS_INS#
SP10	SDCDAT6		MSCDAT3
SP11	SDCCLK		MSCCLK
SP12	SDCDAT5		MSCDAT6
SP13	SDCDAT4		MSCDAT7
SP14			
SP15	SDCDAT3		
SP16	SDCDAT2		
SP17			
SP18			
SP19			

Realtek Recommend

MODE_SEL
C609 @ 47P_0402_50V8J
R516 0_0402_5%

MS_CLK
R515 @ 10_0402_5%
C610 @ 10P_0402_50V8J

SD_CLK
R517 @ 10_0402_5%
C611 @ 10P_0402_50V8J

+3VS_CR_VCC
C612 1U_0603_10V4Z
C613 0.1U_0402_16V4Z
C614 0.1U_0402_16V4Z

0.1U_0402_16V4Z
C615 1U_0603_10V4Z
C616 0.1U_0402_16V4Z
AV_PLL

U23

AV_PLL 20mil (+1.8V internal regulator)

+VCC_OUT
+3VS_CR_VCC
R518 0_0603_5%
+3VALW
R520 @ 0_0603_5%
C617 4.7U_0805_10V4Z
C618 0.1U_0402_16V4Z

+3V3_IN
CARD_RST#
MODE_SEL
CARD_XTLO
CARD_XTLI

<28> USB20_N11
<28> USB20_P11

+3VS_CR_VCC
R521 @ 100K_0402_5%
Internal 200K pull up
R524 0_0603_5% CARD_RST#
C619 1U_0603_10V4Z
R525 499K_0402_1% @

Y_7A25000012_2P

<23> CLK_SD_48M
R528 0_0402_5%
CARD_XTLI
Y8 @
CARD_XTLO
12MHZ_16P_6X12000012
<25> CLK_SD_48M_PCH
R529 @ 0_0402_5%
R531 @ 270K_0402_5%
C621 @ 6P_0402_50V8J
C622 @ 6P_0402_50V8J

R527 6.19K_0402_1%
R530 0_0402_5%
AGND

U23 pin		
1	AV_PLL	
3	NC	
7	NC	
9	CARD_3V3	
11	D3V3	
33	D3V3	
8	3V3_IN	
44	RST#	
45	MODE_SEL	
47	XTLO	
48	XTLI	
4	DM	
5	DP	
14	GPIO0	
2	RREF	
12	DGND	
32	DGND	
6	AGND	
46	AGND	
10	VREG	AV_PLL
22	MS_D4	
30	NC	
43	XD_CLE_SP19	
42	XD_CE#_SP18	
41	XD_ALE_SP17	
40	SD_DAT2/XD_RE#_SP16	SDDAT2
39	SD_DAT3/XD_WE#_SP15	SDDAT3
38	XD_RDY_SP14	
37	SD_DAT4/XD_WP#/MS_D7_SP13	
35	SD_DAT5/XD_D0/MS_D6_SP12	
34	SD_CLK/XD_D1/MS_CLK_SP11	SDCLK_MSCLK
31	SD_DAT6/XD_D7/MS_D3_SP10	SDDAT6_MSD3
29	MS_INS#_SP9	MS_INS#
28	SD_DAT7/XD_D2/MS_D2_SP8	SDDAT7_MSD2
27	SD_DAT0/XD_D6/MS_D0_SP7	SDDAT0_MSD0
26	SD_DAT1/XD_D3/MS_D1_SP6	MSD1
25	XD_D5_SP5	MS_BS
23	XD_D4/SD_DAT1_SP4	SDDAT1
21	SD_CD#_SP3	SD_CD#
20	SD_WP_SP2	SD_WP
19	XD_CD#_SP1	
18	EEDI	
13	XTAL_CTR	
24	MS_D5	
15	EEDO	
16	EECS	
17	EESK	
36	SD_CMD	SD_CMD

R522 0_0402_5% SD_CLK
R523 0_0402_5% MS_CLK
+3VS_CR_VCC
R526 0_0402_5%

S IC RTS5159-GR LQFP 48P CARD READER

2/17 Change Part number of U25 from SA00001NK10 to SA00002YP00

4/2 Add by Vivian
C878 100P_0402_50V8J @ CLK_SD_48M

+VCC_3IN1
40mil
+VCC_OUT
R532 0_0603_5%
C623 4.7U_0805_10V4Z
C624 @ 10U_0805_10V4Z
C625 0.1U_0402_16V4Z

Add C822 4.7u and reserve C808 10u
for cost down Michael 2008/5/30

+VCC_3IN1
JREAD1

SD_WP	1	SD-WP-SW	
SDDAT1	2	SD-DAT1	
SDDAT0_MSD0	3	SD-DAT0	
	4	SD-GND	
	5	MS-GND	
MS_BS	6	MS-BS	
SD_CLK	7	SD-CLK	
MSD1	8	MS-DAT1	
SDDAT0_MSD0	9	MS-DAT0	
	10	SD-VCC	
SDDAT7_MSD2	11	MS-DAT2	
	12	SD-GND	
MS_INS#	13	MS-INS	
SDDAT6_MSD3	14	MS-DAT3	
SD_CMD	15	SD-CMD	
MS_CLK	16	MS-SCLK	
	17	MS-VCC	
SDDAT3	18	SD-DAT3	
	19	MS-GND	
SDDAT2	20	SD-DAT2 GND1	22
SD_CD#	21	SD-CD-SWGND2	23

TAITW_R009-121-LK_RV
CONN@

+3VS
W=40mils
C626 @ 0.1U_0402_16V4Z
C627 @ 1U_0603_10V4Z
R533 0_0805_5%
<38> CR_ON#
R534 @ 100K_0402_5%
Q17 SI2301BDS_SOT23 @
W=40mils
+3VS_CR_VCC

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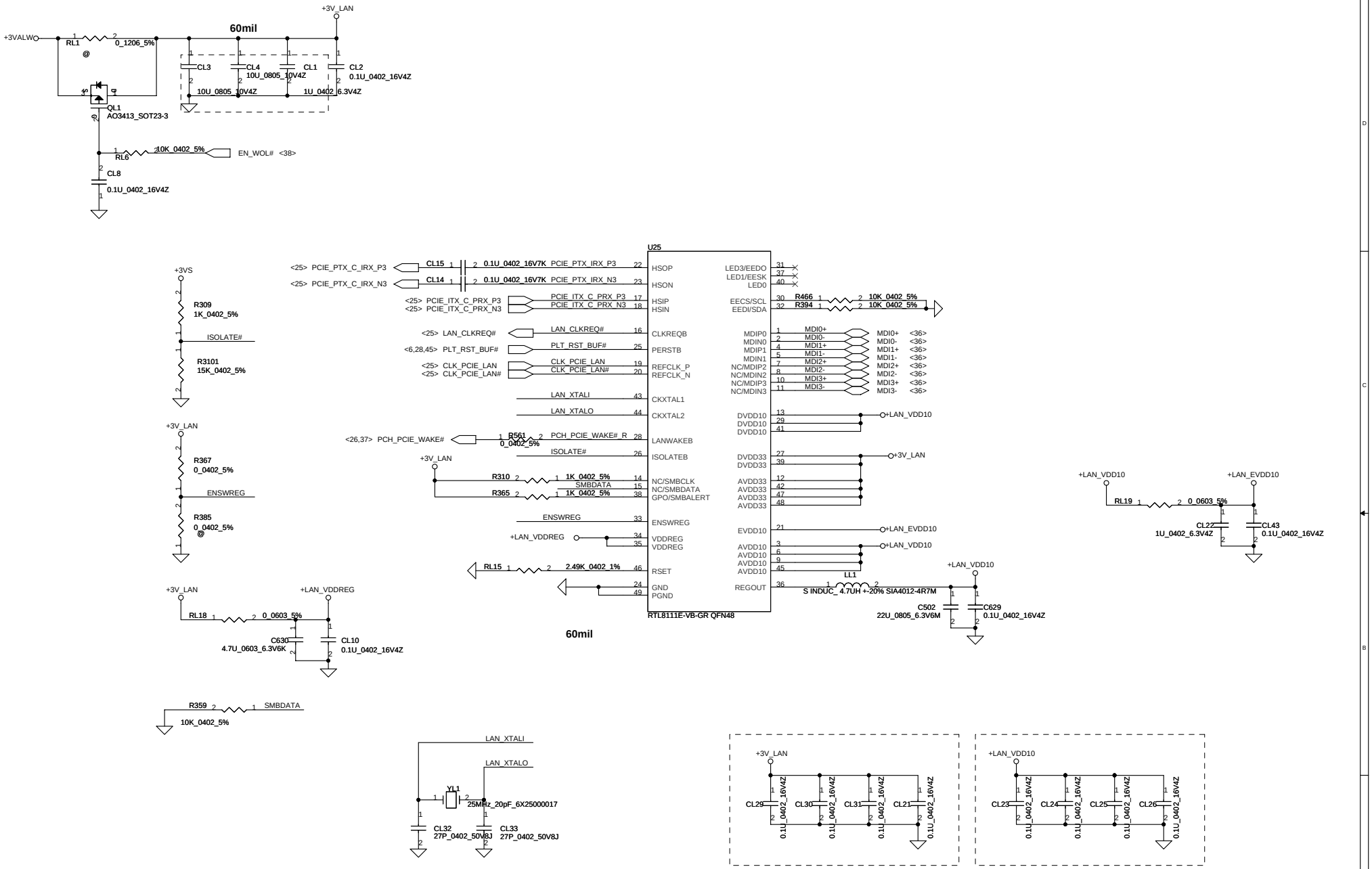

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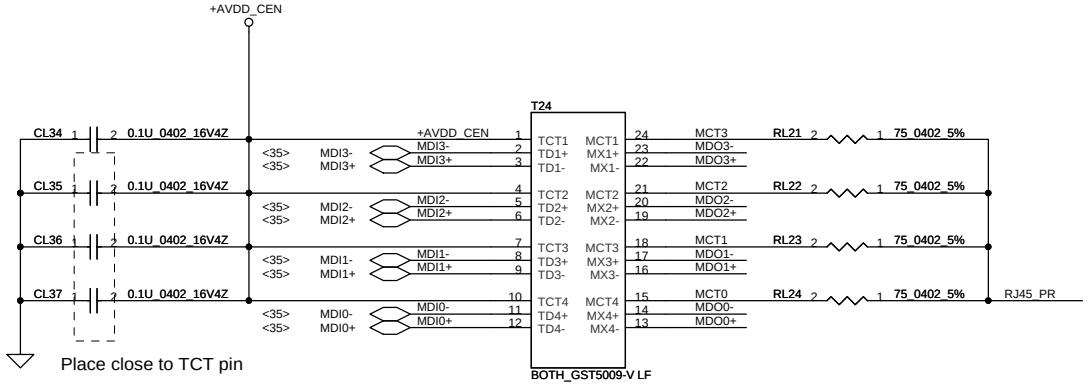
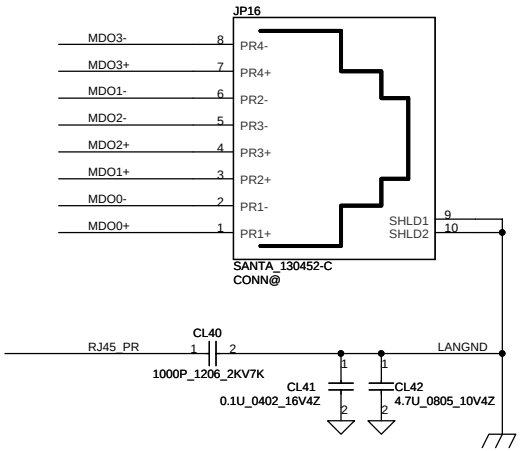


P/N change from SP050003O00 to SP050006300. 11/09

Lan Conn.



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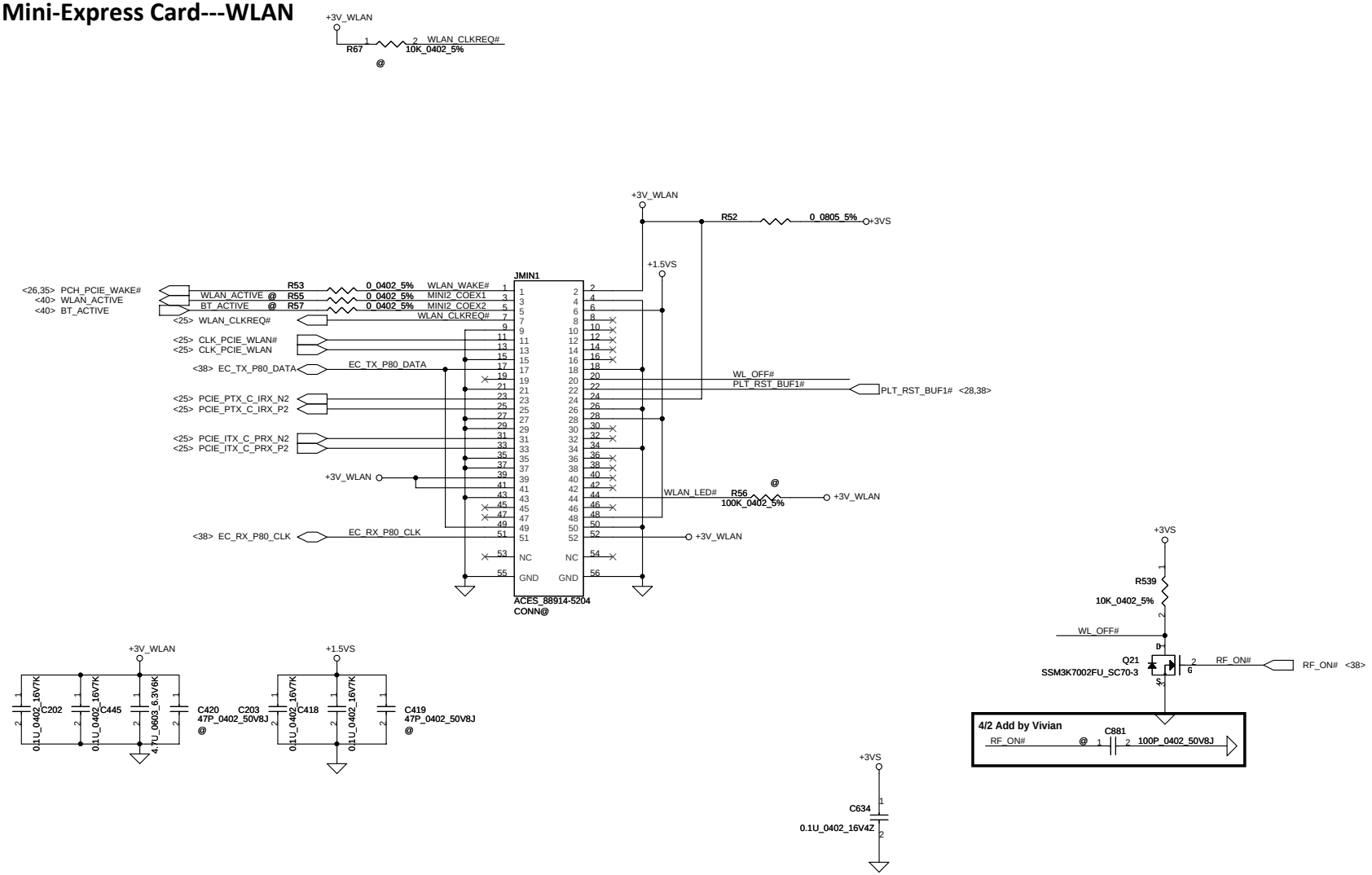
Mini-Express Card---WLAN



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Board ID / SKU ID Table for AD channel

Vcc	3.3V ± 5%			
Ra / Rc	100K ± 5%			
Board ID	**Rb / Rd**	**VAD_BRD min**	**VAD_BRD typ**	**VAD_BRD max**
0	0	0V	0V	0V
1	8.2K ± 5%	0.216V	0.250V	0.289V
2	18K ± 5%	0.436V	0.503V	0.538V
3	33K ± 5%	0.712V	0.819V	0.875V
4	56K ± 5%	1.036V	1.185V	1.264V
5	100K ± 5%	1.453V	1.650V	1.759V
6	200K ± 5%	1.935V	2.200V	2.341V
7	NC	2.500V	3.300V	3.300V

	MB_ID
EVT	0
DVT	1
PVT	2
PreMP	3

	PROJECT_ID
NBLB3	0
NBLB5	7

Signal \ EC_REV	KB926 D3	KB926 E0
EC_REV_SEL	1	0

EC DEBUG PORT

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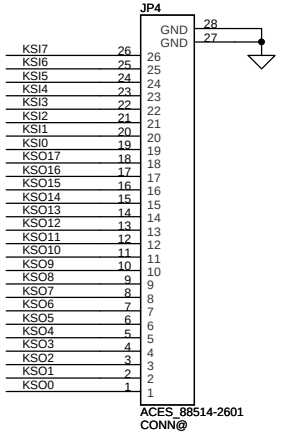
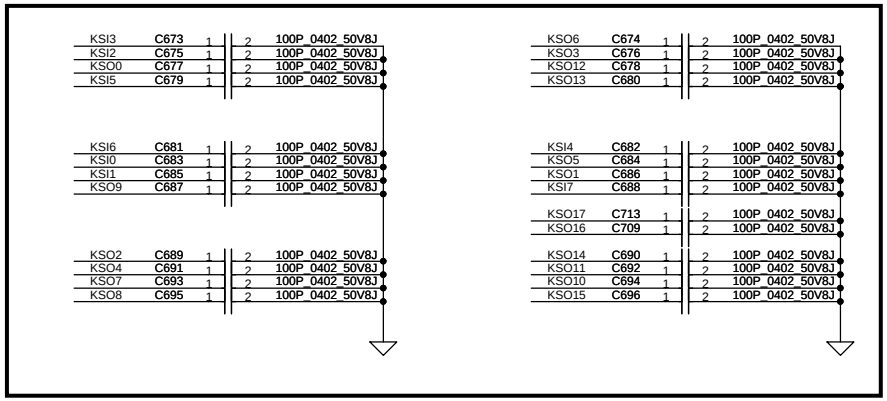
INT_KBD Conn.

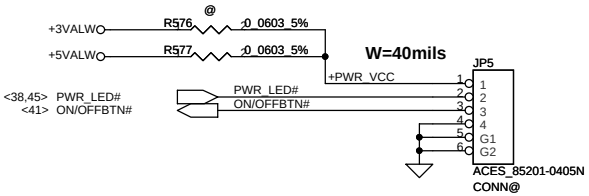


KSI[0..7] KSI[0..7] <38>

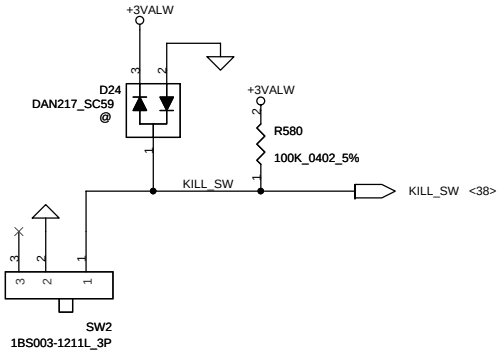
KSO[0..17] KSO[0..17] <38>



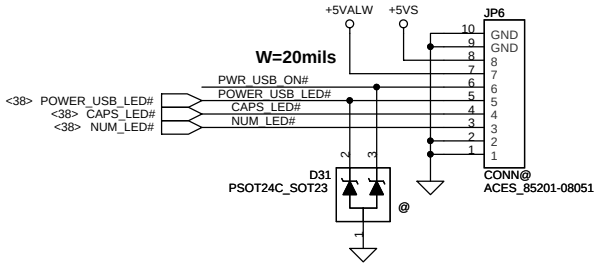
Power BTN Board Conn

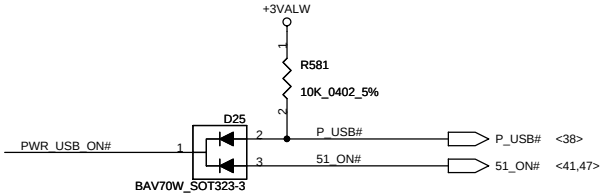


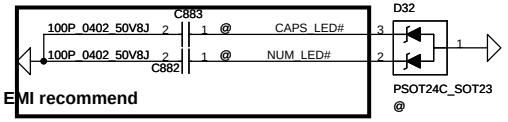
Kill SWITCH



Function board conn







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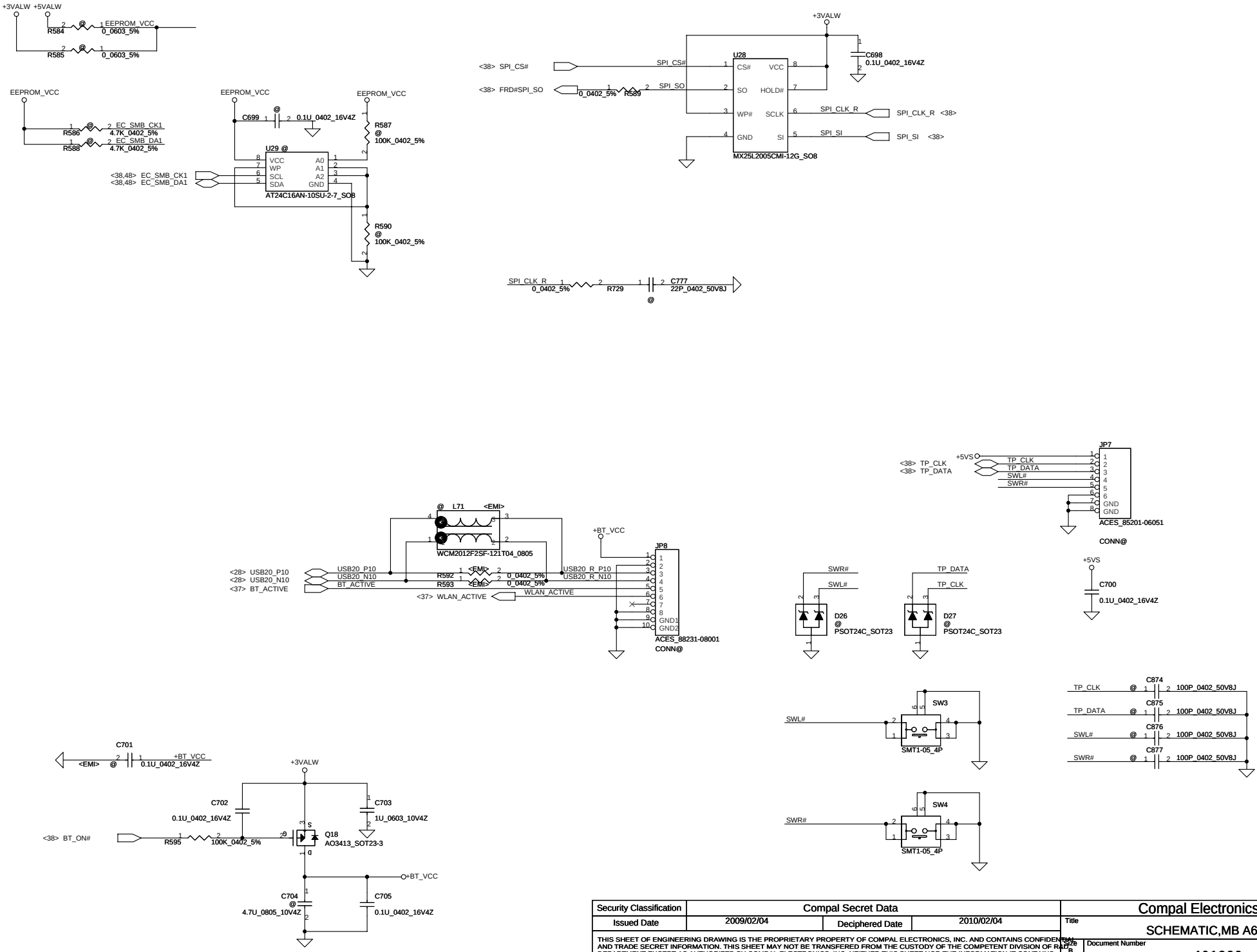

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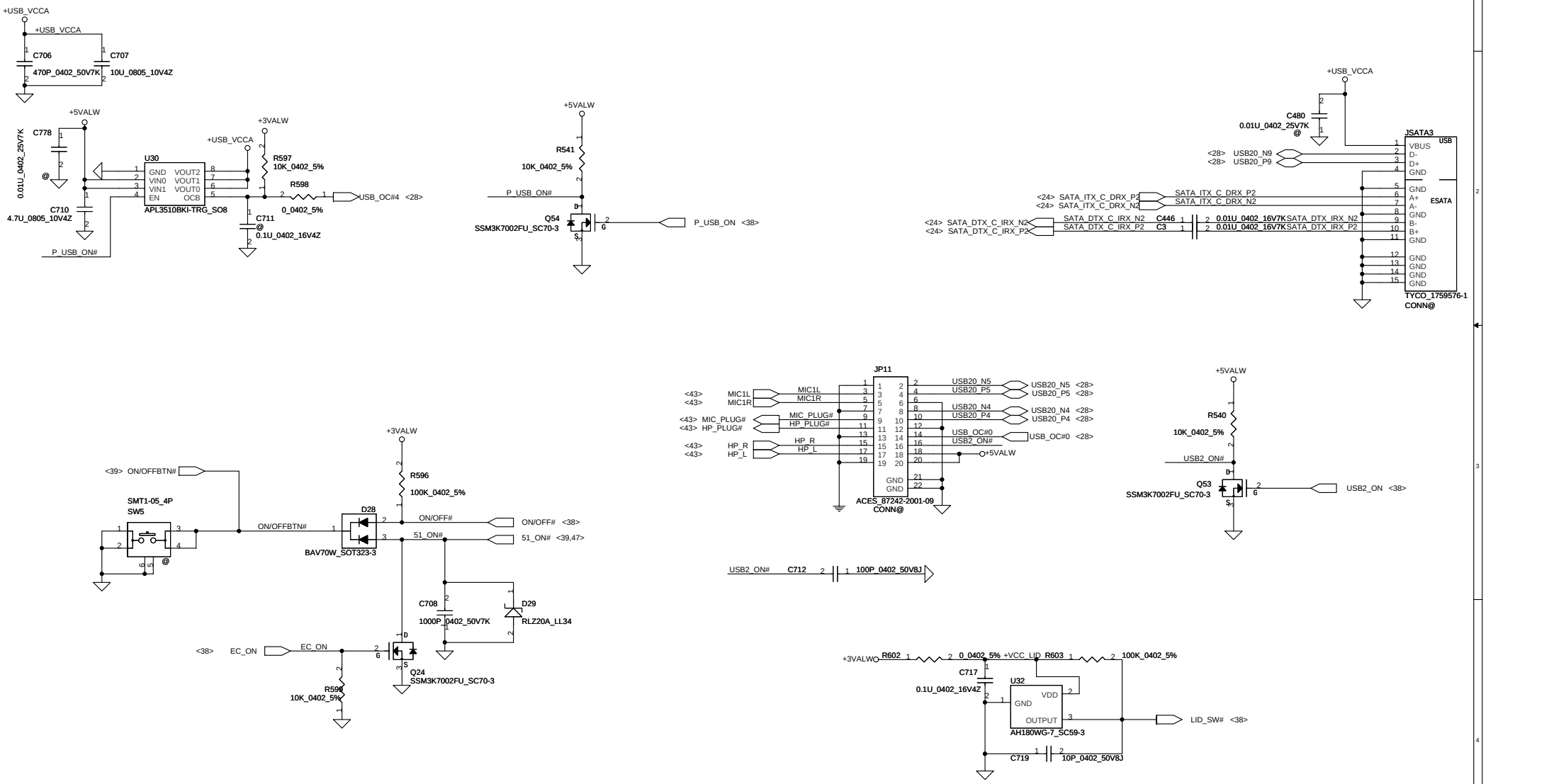
APL3510
APL3511 □□□-□□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code
- Output Current/EN Function

Package Code
K : SOP-8 X : MSOP-8 B : SOT-23-5
Operating Ambient Temperature Range
I : -40 to 85 ºC
Handling Code
TR : Tape & Reel
Output Current/EN Function
A : 2A/Active High B : 2A/Active Low
C : 1A/Active High D : 1A/Active Low
Assembly Material
G : Halogen and Lead Free Device



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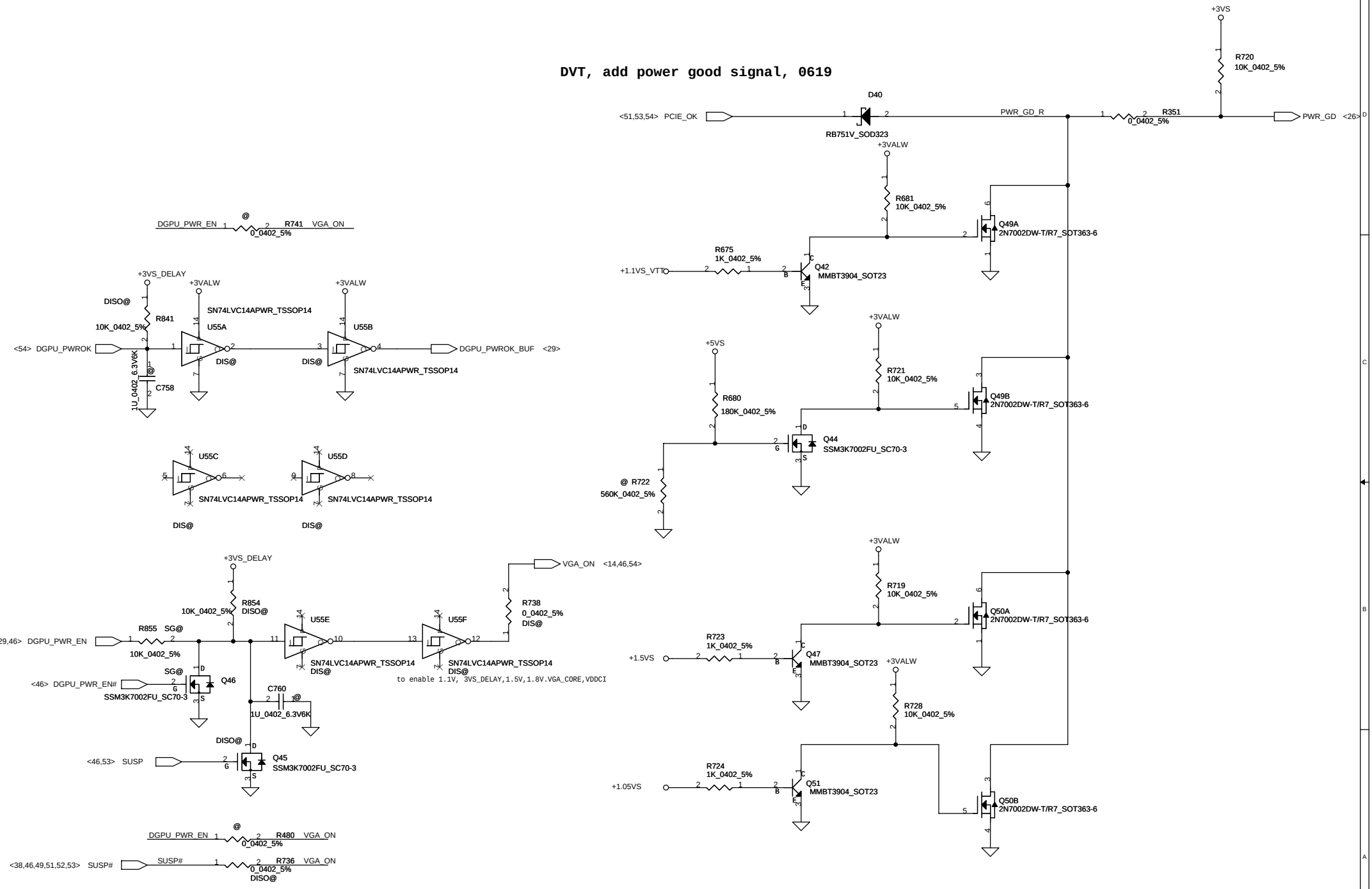
DVT, add power good signal, 0619



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Copy KFTOO

EC Beep

<38> BEEP# — R607 10K_0402_5% — MONO_IN — C726 0.1U_0402_16V4Z — MONO_IN

<24> PCH_SPKR — R608 10K_0402_5%

C722 0.1U_0402_16V4Z

PCI Beep

R609 10K_0402_5%

+5VS — L72 FBMA-L11-201209-221LMA30T_0805 — +5VAMP — 0.1U_0402_16V4Z — 60mil — R606 0_0805_5%

L73 FBMA-L11-201209-221LMA30T_0805

C723 C724 0.1U_0402_16V4Z

U33 G9191-475T1U_SOT23-5 @ — IN OUT GND SHDN BYP — 40mil — +VDDA 4.75V

C725 0.01U_0402_25V7K @

(output = 300 mA)

2/18 Change from GNDA to DGND of vendor suggest

HD Audio Codec

+VDDA — L74 FBMA-L11-160808-800LMT_0603 — 0.1U_0402_16V4Z — 40mil — +AVDD_HDA

C727 10U_0805_10V4Z C728 C729 0.1U_0402_16V4Z

10mil — 0.1U_0402_16V4Z — +3VS_DVDD — L75 MBK1608121YZF_0603 — +3VS

C730 C731 C732 10U_0805_10V4Z 0.1U_0402_16V4Z

U34 — AVDD1 AVDD2 DVDD DVDD_IO

MIC2_VREFO — R610 0_0402_5% @ — D30 RLS4148_LL34-2 — R613 4.7K_0402_5%

<44> MIC2_L — R611 1K_0402_1% — MIC2_R_L C733 4.7U_0805_6.3V6K — MIC2_C_L — MIC2_C_R C734 4.7U_0805_6.3V6K

MIC1_VREFO — R635 4.7K_0402_5% — R633 4.7K_0402_5%

MIC1_L — L100 BLM18BD601SN1D_0603 — MIC1L <41>

MIC1_R — L101 BLM18BD601SN1D_0603 — MIC1R <41>

MIC2_VREFO — C736 MIC1_L 4.7U_0805_6.3V6K — C737 MIC1_R 4.7U_0805_6.3V6K — C738 @ MONO_IN 100P_0402_50V8J

<24> HDA_RST_AUDIO# — <24> HDA_SYNC_AUDIO — <24> HDA_SDOUT_AUDIO

<41> MIC_PLUG# — R618 20K_0402_1% — SENSE_A

<41> HP_PLUG# — R619 5.1K_0402_1% — SENSE_B

<44> MUTE# — R620 0_0402_5%

Pin	Left	Right
14	LINE2_L	LOUT1_L
15	LINE2_R	LOUT_R
16	MIC2_L	LOUT2_L
17	MIC2_R	LOUT2_R
23	LINE1_L	SPDIFO2
24	LINE1_R	DMIC_CLK1/2
18	LINE1_VREFO	NC
20	LINE2_VREFO	DMIC_CLK3/4
19	MIC2_VREFO	
21	MIC1_L	BITCLK
22	MIC1_R	SDATA_IN
12	PCBEEP_IN	MONO_OUT
11	RESET#	CBP
10	SYNC	CPVEE
5	SDATA_OUT	MIC1_VREFO
2	GPIO0/DMIC_DATA1/2	HPOUT_R
3	GPIO1/DMIC_DATA3/4	CBN
13	SENSE A	VREF
34	SENSE B	JDREF
47	EAPD	HPOUT_L
48	SPDIFO1	
4, 7	DVSS1, DVSS2	AVSS1, AVSS2
35		AMP_LEFT → AMP_LEFT <44>
36		AMP_RIGHT → AMP_RIGHT <44>
44		R616 33_0402_5% — C735 33P_0402_50V8J
6		HDA_BITCLK_AUDIO <24>
8		HDA_SDIN0_AUDIO — R617 33_0402_5% — HDA_SDIN0 <24>
37		
29		2.2U_0402_6.3VM
31		C739 — 10mil — MIC1_VREFO
28		C740 2.2U_0402_6.3VM
32		HP_R — HP_R <41>
30		10mil
27		CODEC_VREF — C741 0.1U_0402_16V4Z — C742 10U_0805_10V4Z @
40		R621 20K_0402_1%
33		HP_L — HP_L <41>
26, 42		AVSS1, AVSS2

ALC272-VA2-GR LQFP_48P

DGND GNDA

R622 0_0805_5% — R624 0_0805_5% — R626 0_0805_5% — GND GNDA

R623 0_0805_5% — R625 0_0805_5% — R627 0_0805_5% — GND GNDA

ESD 3/20 Copy KHLBX

+3VS +5VS — R763 4.7K_0402_5% @ — R764 4.7K_0402_5% @ — HDA_RST_AUDIO#

C854 0.01U_0402_16V7K @

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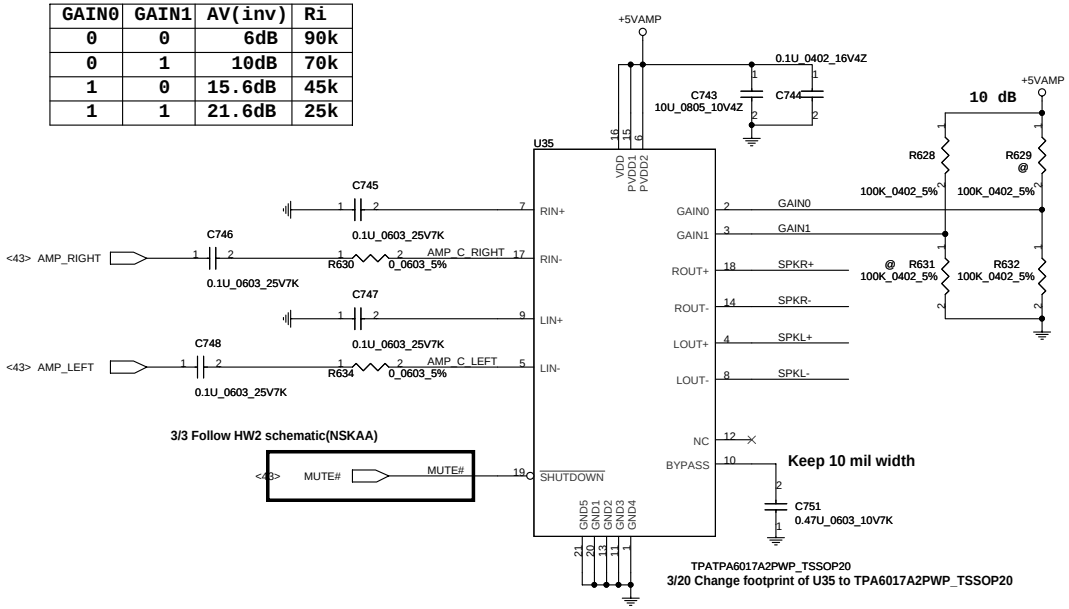
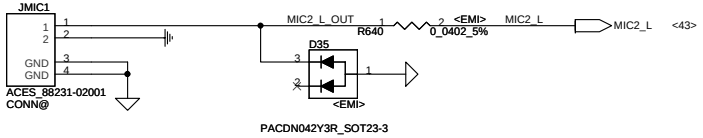
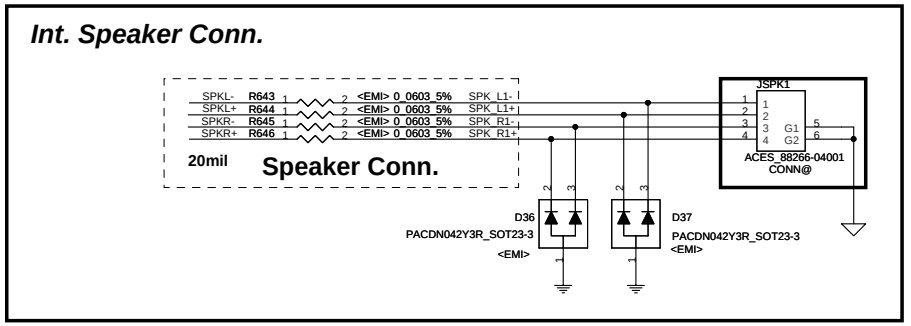
GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k







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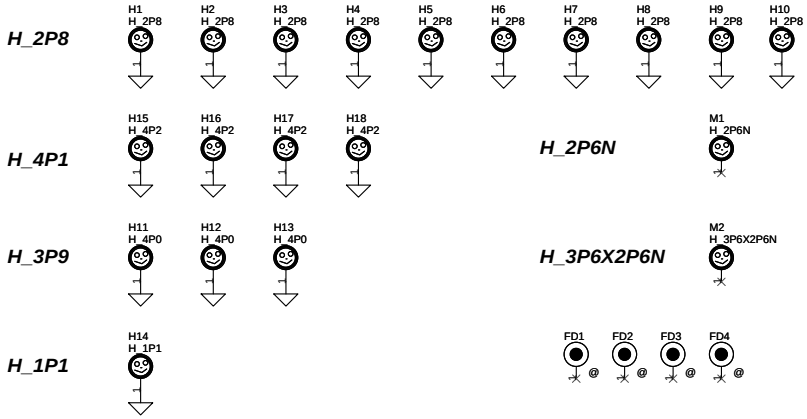
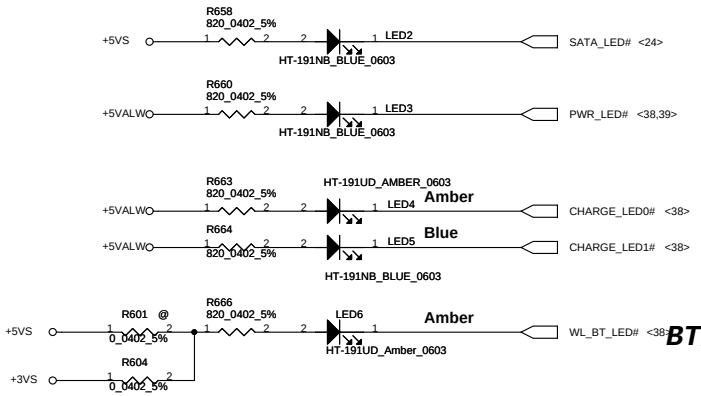


LED



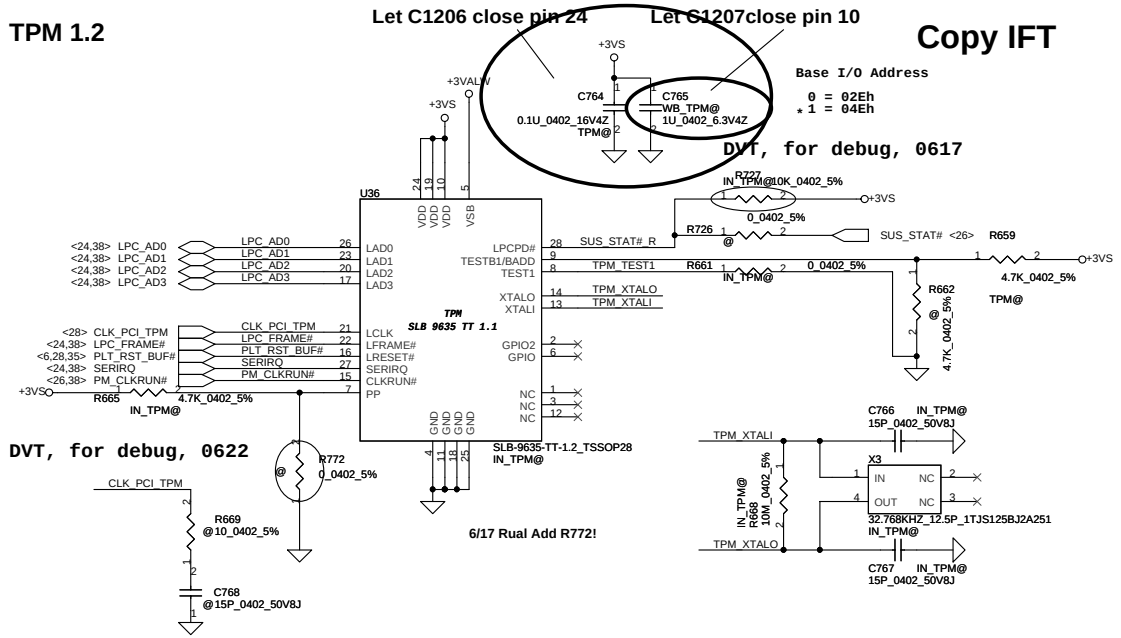
BT/WLAN LED

TPM 1.2

Let C1206 close pin 24

Let C1207close pin 10

Copy IFT



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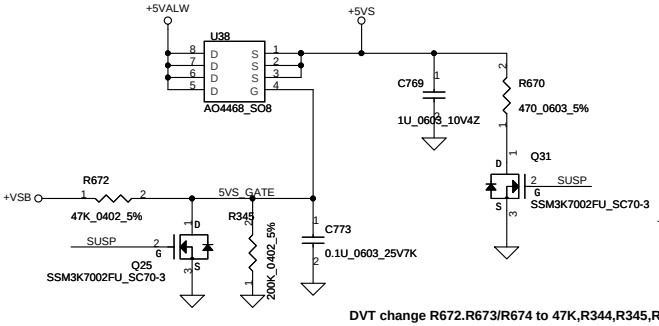
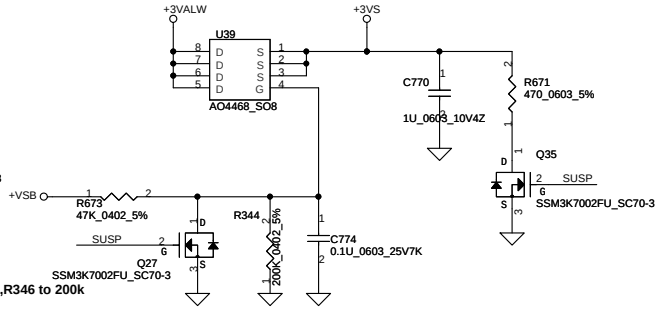
+5VALW TO +5VS



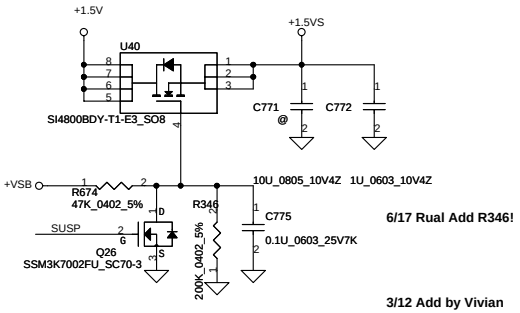
6/17 Rual Add R345!

+3VALW TO +3VS



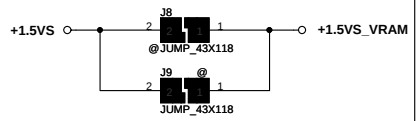
DVT change R672.R673/R674 to 47K,R344,R345,R346 to 200k

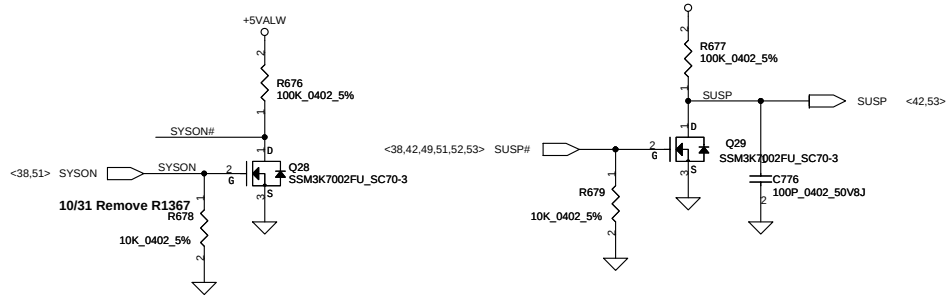
+1.5V TO +1.5VS

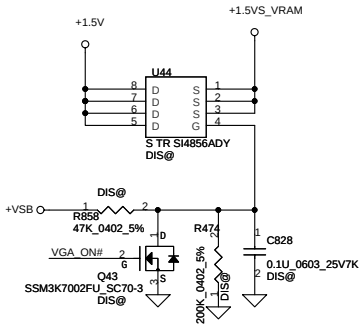


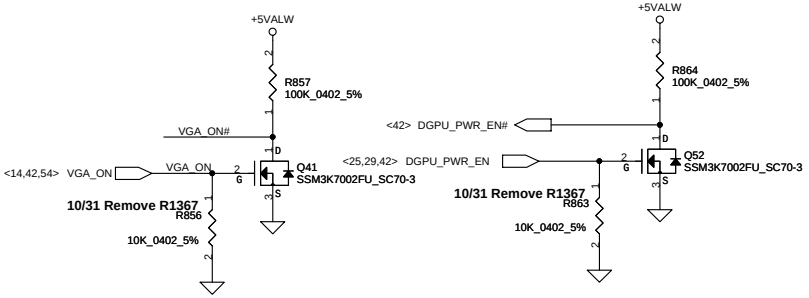
6/17 Rual Add R346!

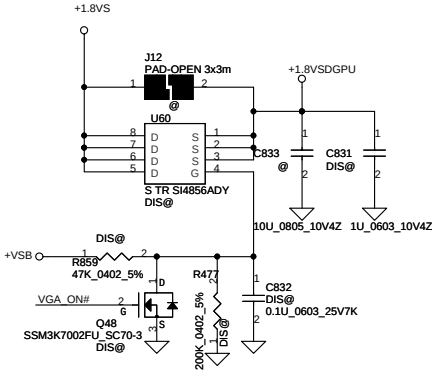
3/12 Add by Vivian



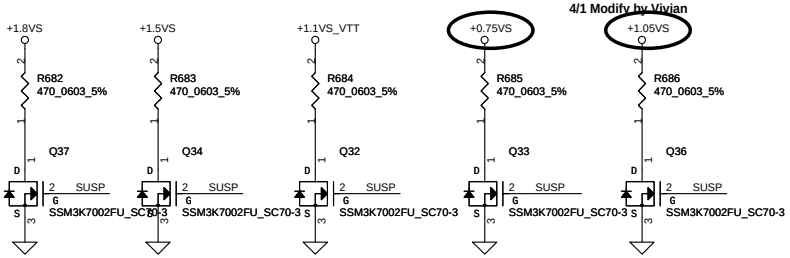


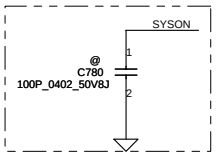






4/1 Modify by Vivian





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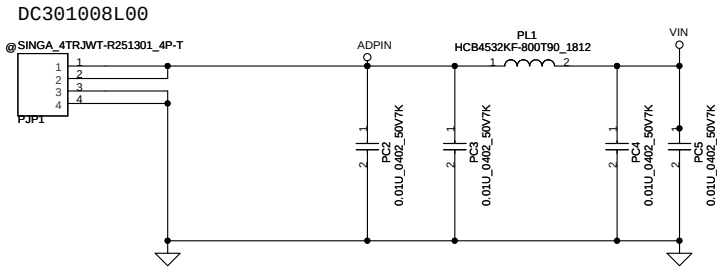
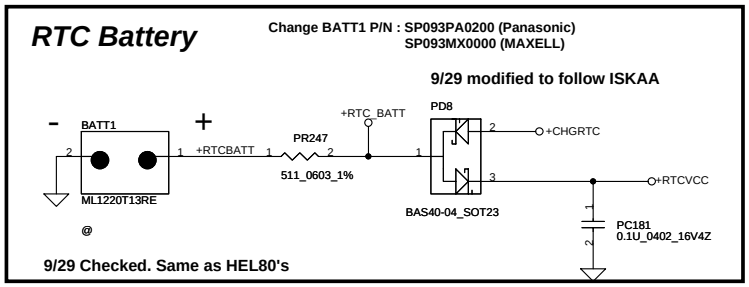




Reserve another location

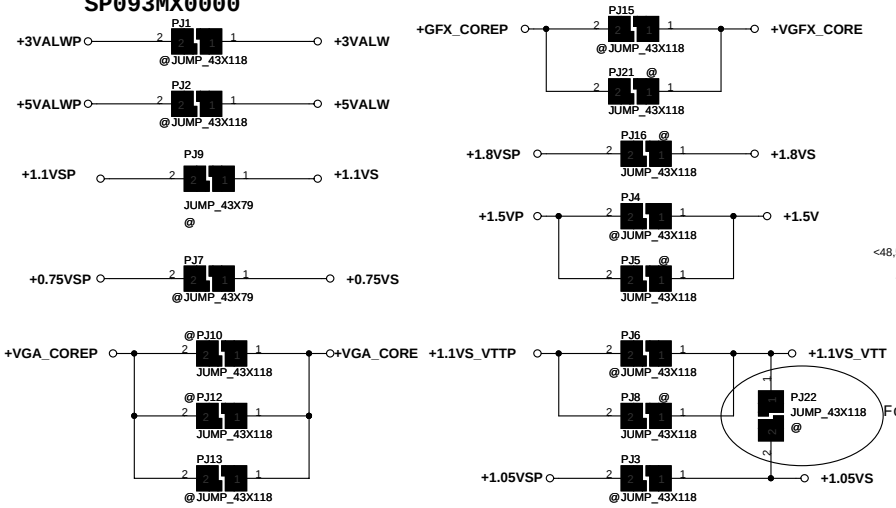
06/24 Rual remove BATT2!

BOM structure comment

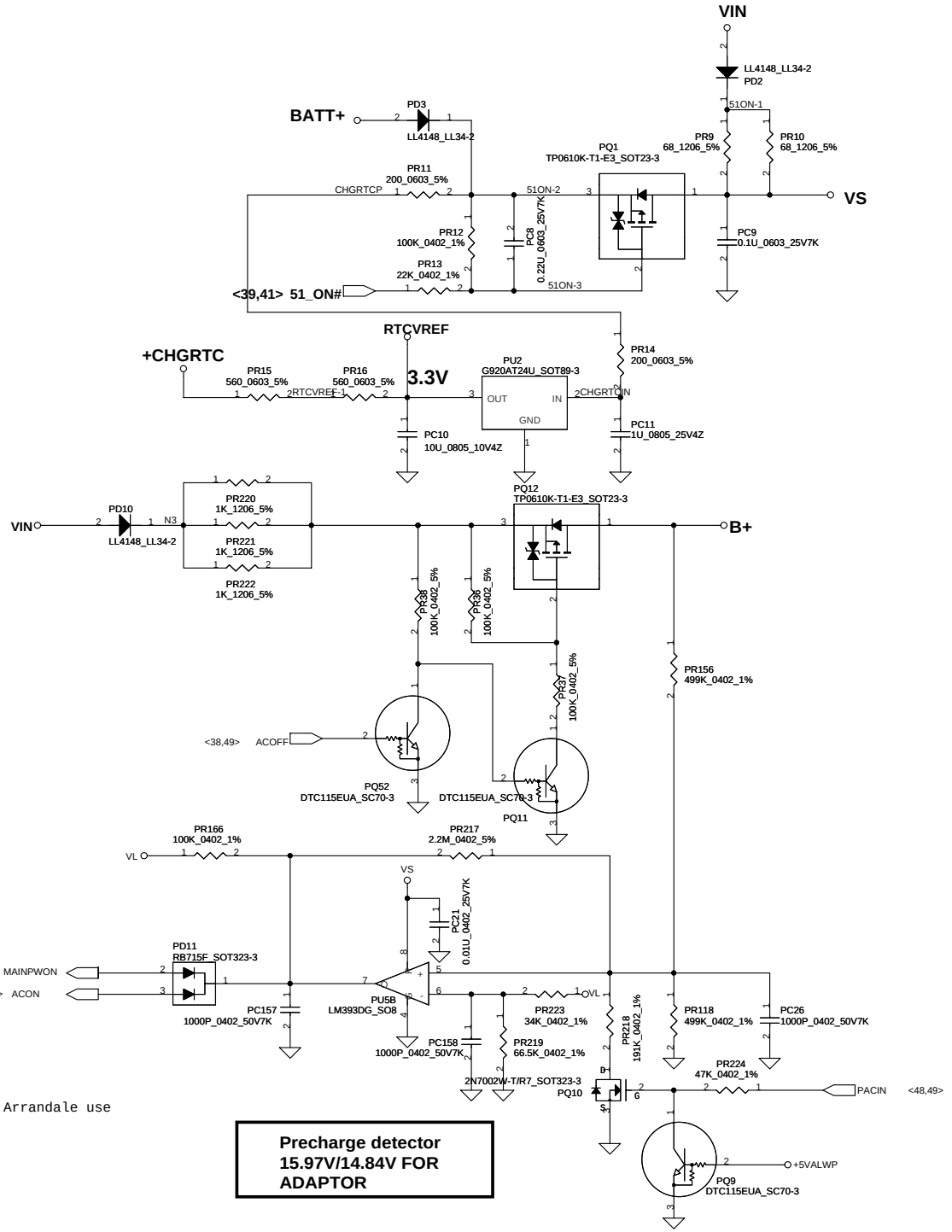
@ ==>unpop

UMA@==>UMA sku only

DIS@==>DIS sku only



For Arrandale use



Precharge detector
15.97V/14.84V FOR ADAPTOR

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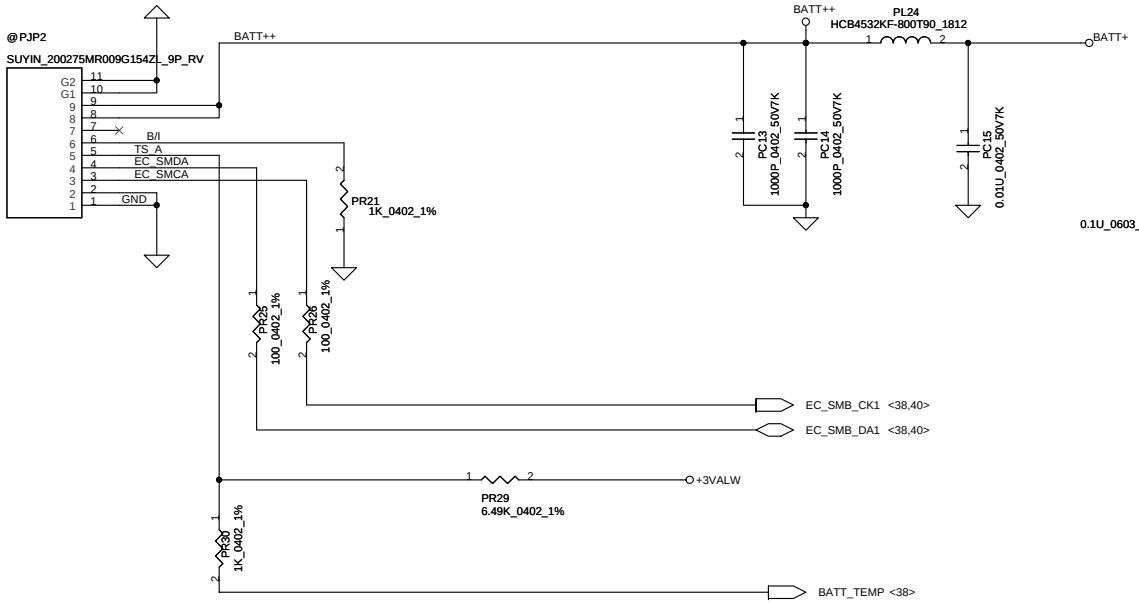
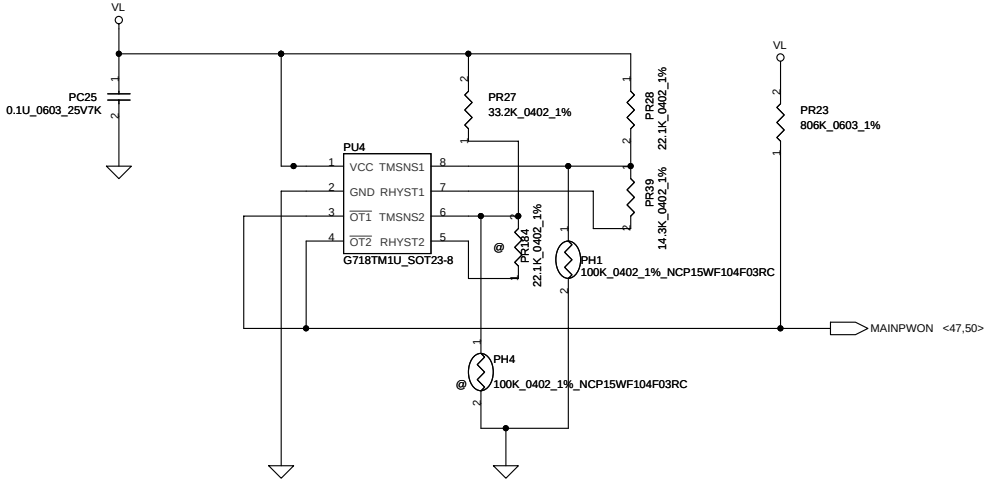
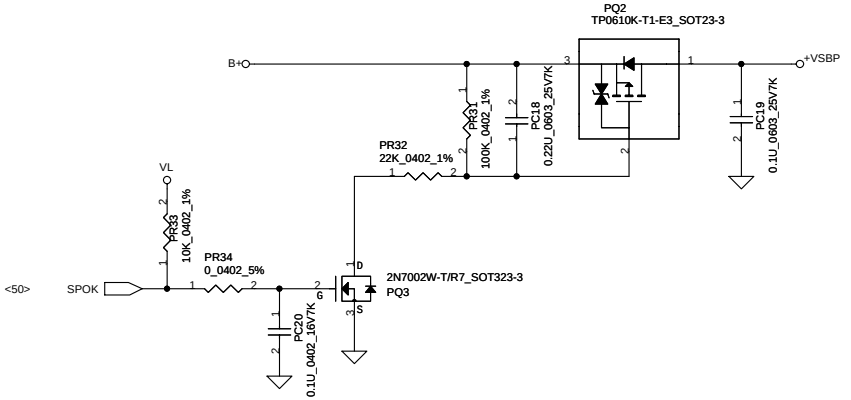


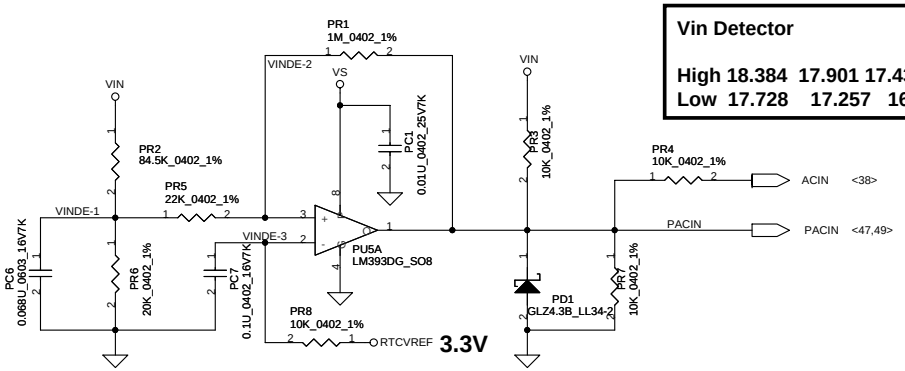
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 70 degree C





Vin Detector

High 18.384 17.901 17.430
Low 17.728 17.257 16.976



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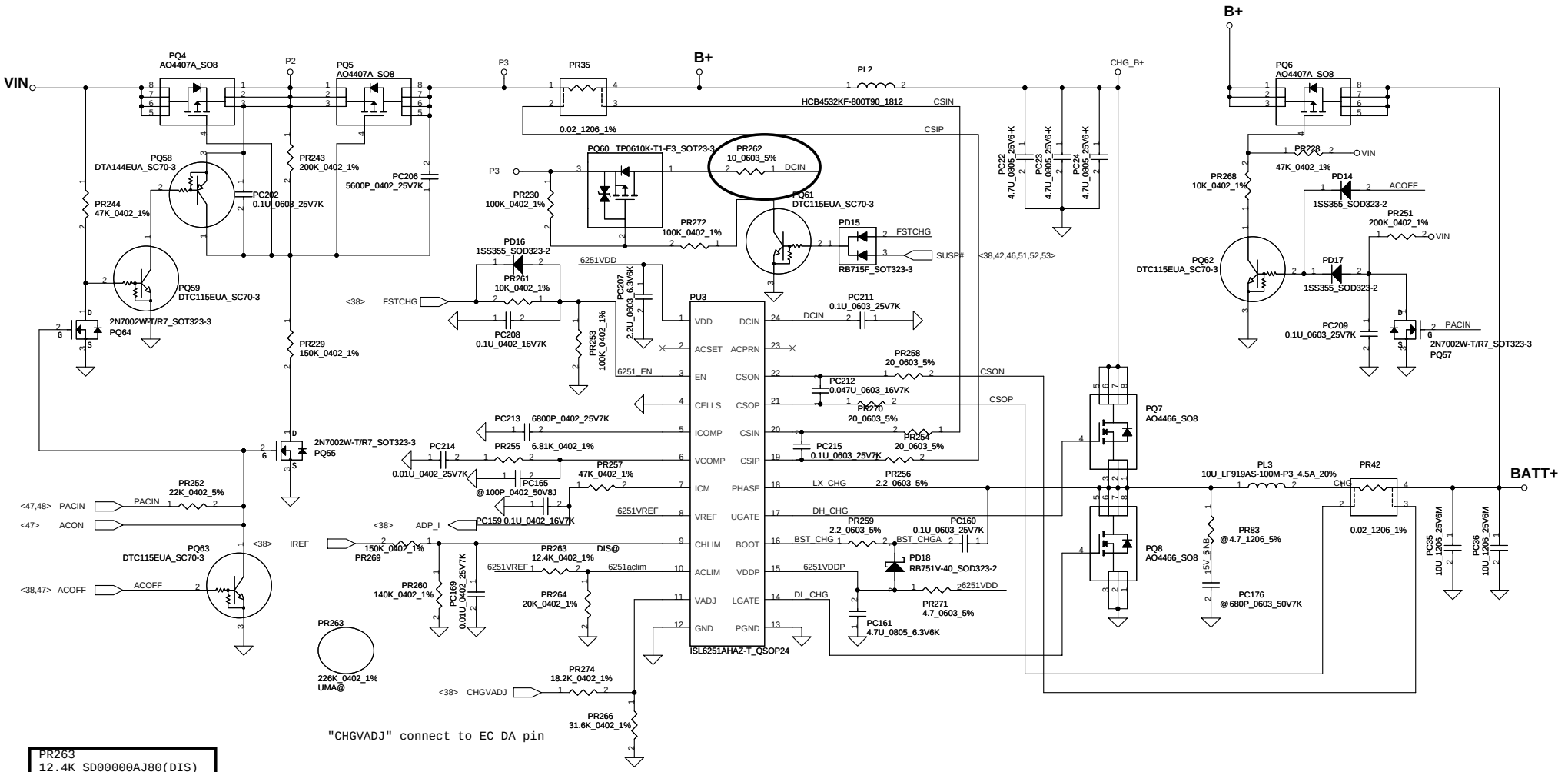

"CHGVADJ" connect to EC DA pin

PR263
12.4K SD00000AJ80(DIS)
226K SD034226380(UMA)

Iada=0~4.74A(90W) CP= 85%*Iada; CP=4.02A

CP mode

Vaclim=2.39*(20K//152K/(20K//152K+12.4K//152K))=1.44966V

Iinput=(1/0.02)((0.05*Vaclm)/2.39+0.05)
where Vaclm=1.44966V, Iinput=4.02A

CC=0.5A~3.64A(0.7C)
IREF=2.42V (4.8AH)
2.62V (5.2AH)

IREF=0.4V~2.62V

CHGVADJ=

Vcell	CHGVADJ
4V	0V
4.2V	1.854V
4.35V	3.12V

CELLS	VDD	GND	Float
CELL number	4	3	2

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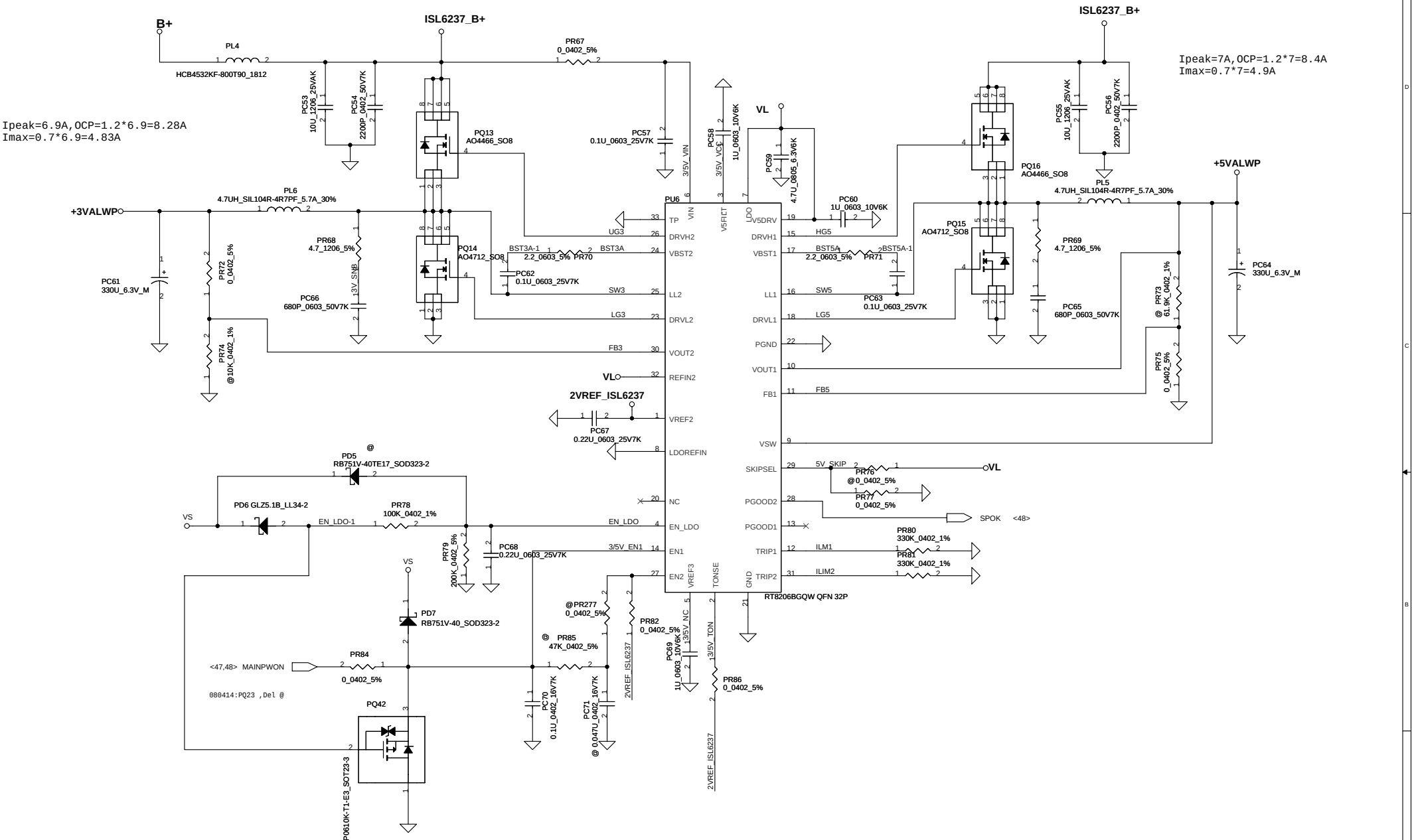

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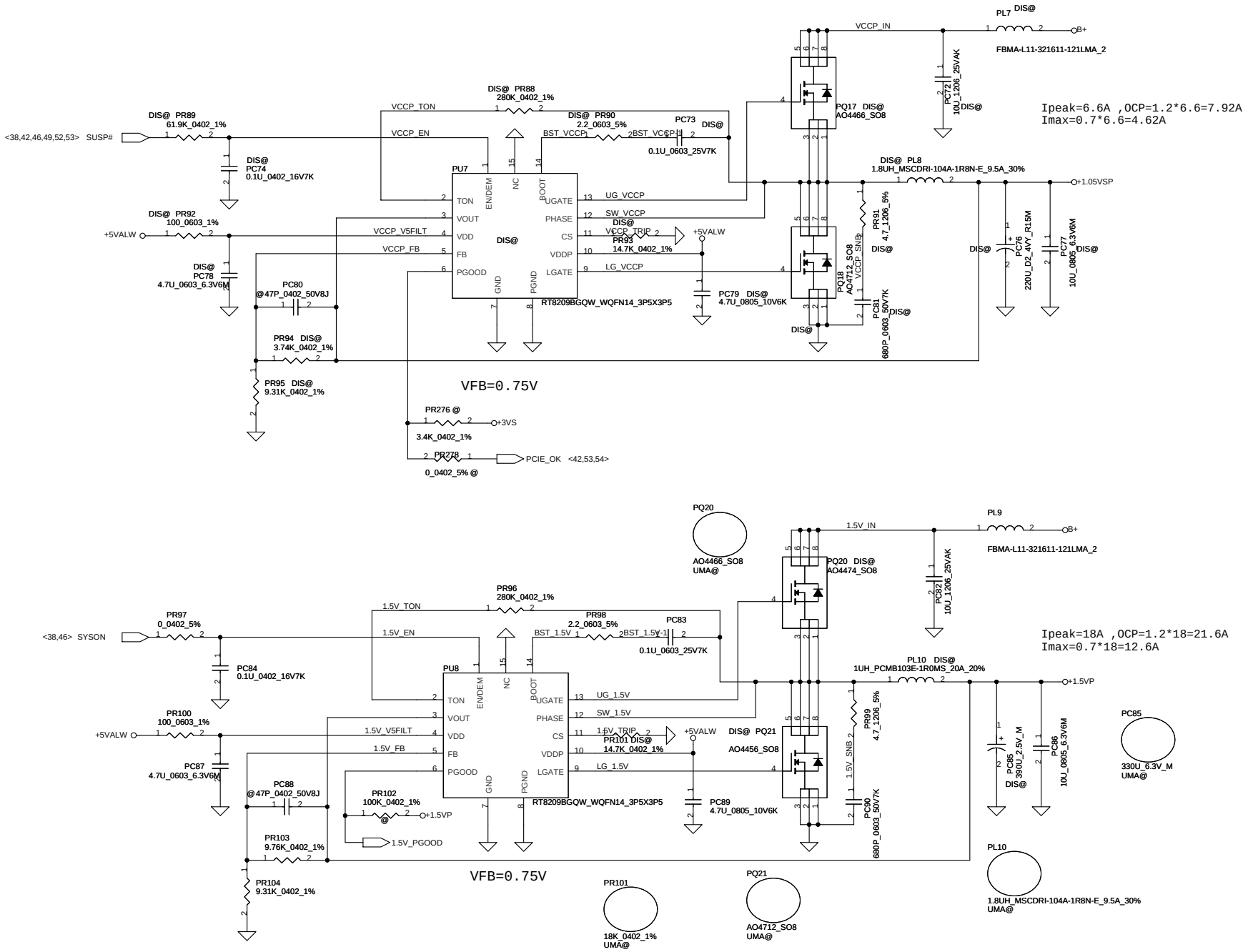

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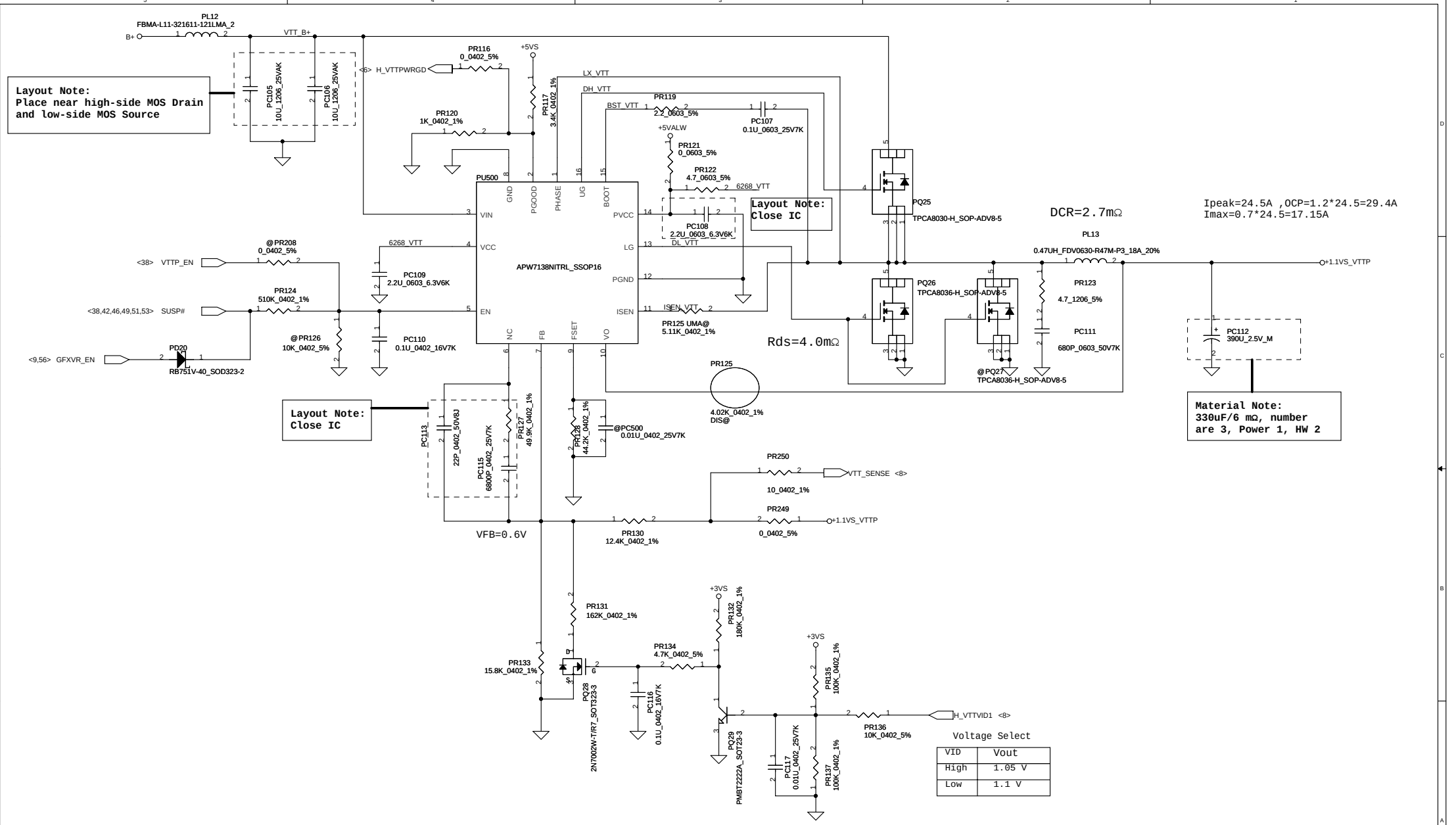

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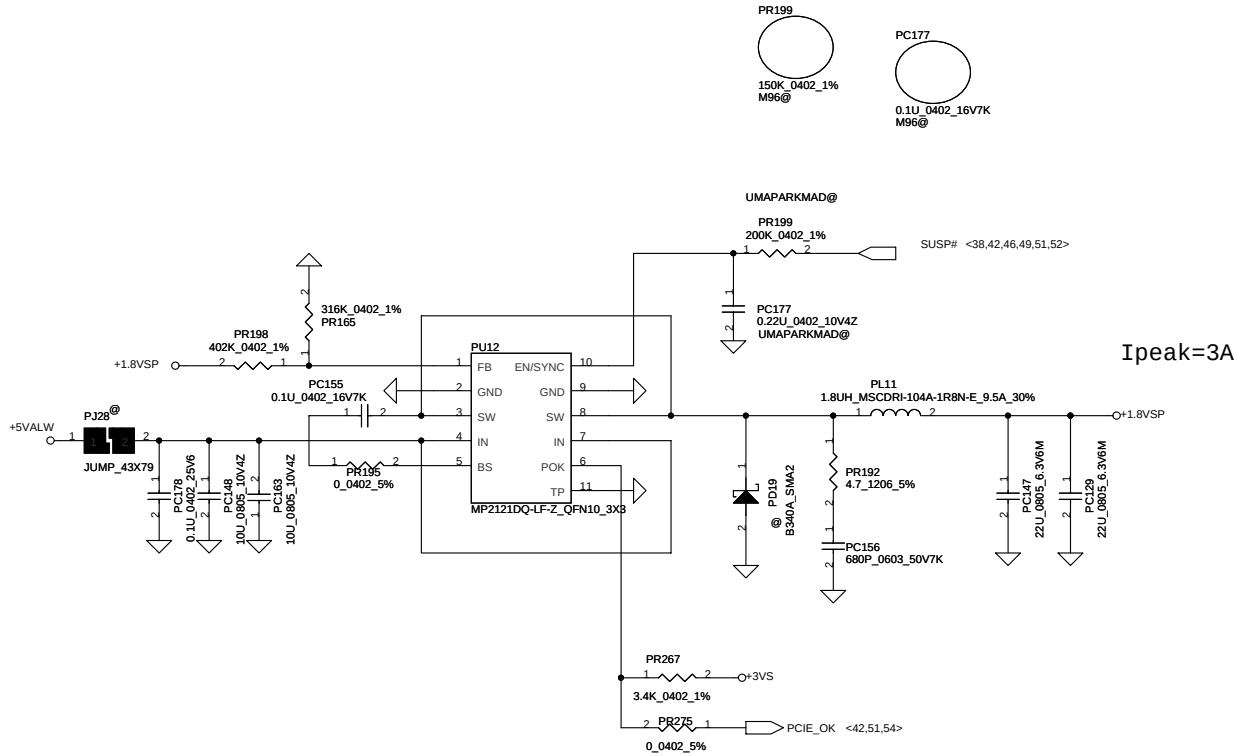
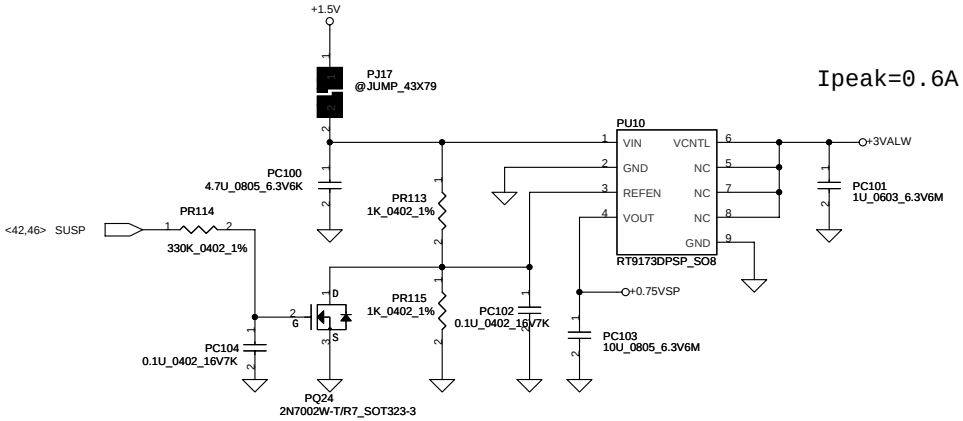
Iocp=RTEIP*ITRIP/RDS(ON)+1/2 I=13k*9u/15m+1/2*2.7=9.15A





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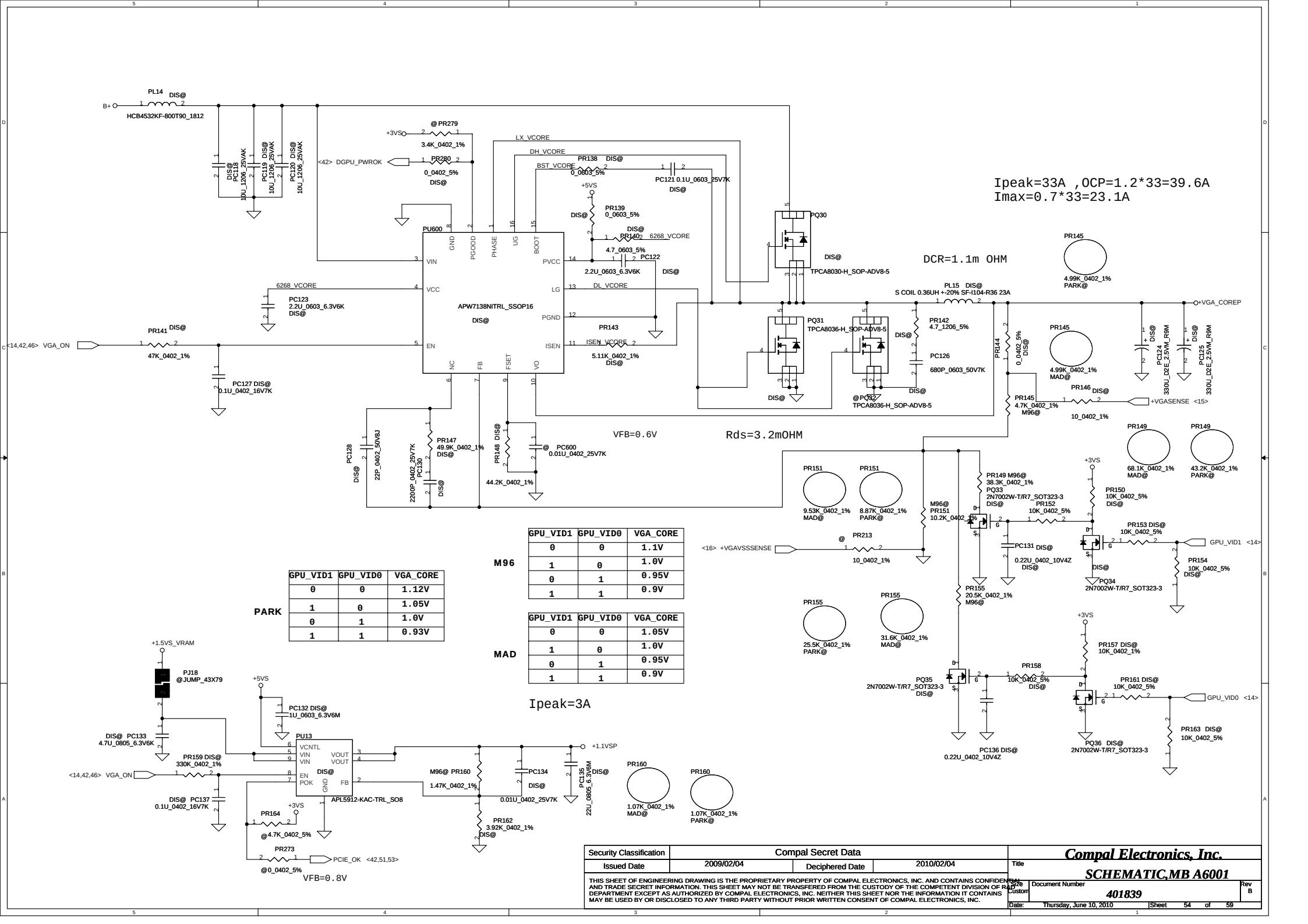

PARK		
GPU_VID1	GPU_VID0	VGA_CORE
0	0	1.12V
1	0	1.05V
0	1	1.0V
1	1	0.93V

M96		
GPU_VID1	GPU_VID0	VGA_CORE
0	0	1.1V
1	0	1.0V
0	1	0.95V
1	1	0.9V

MAD		
GPU_VID1	GPU_VID0	VGA_CORE
0	0	1.05V
1	0	1.0V
0	1	0.95V
1	1	0.9V

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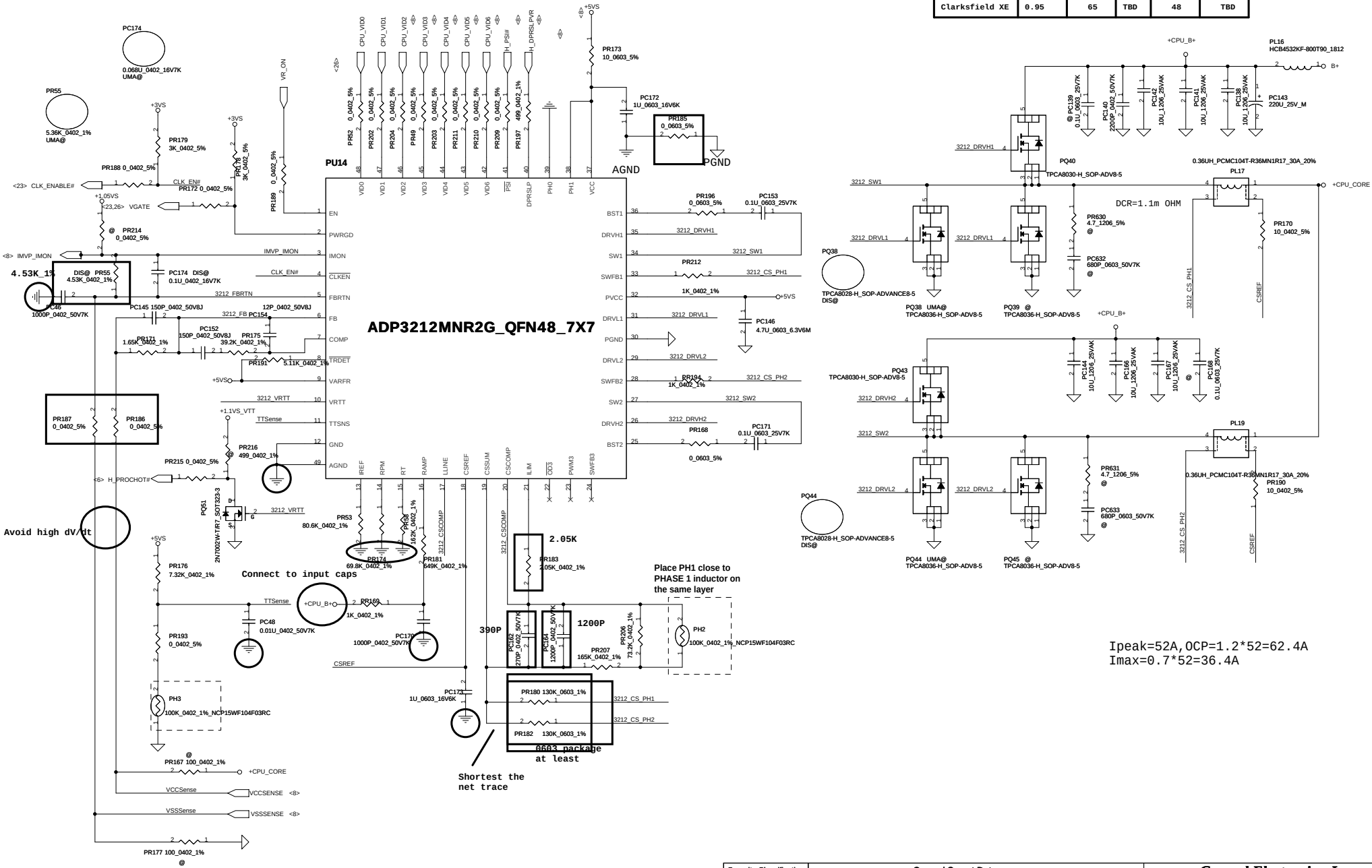
PH0	PH1	# of PH
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD



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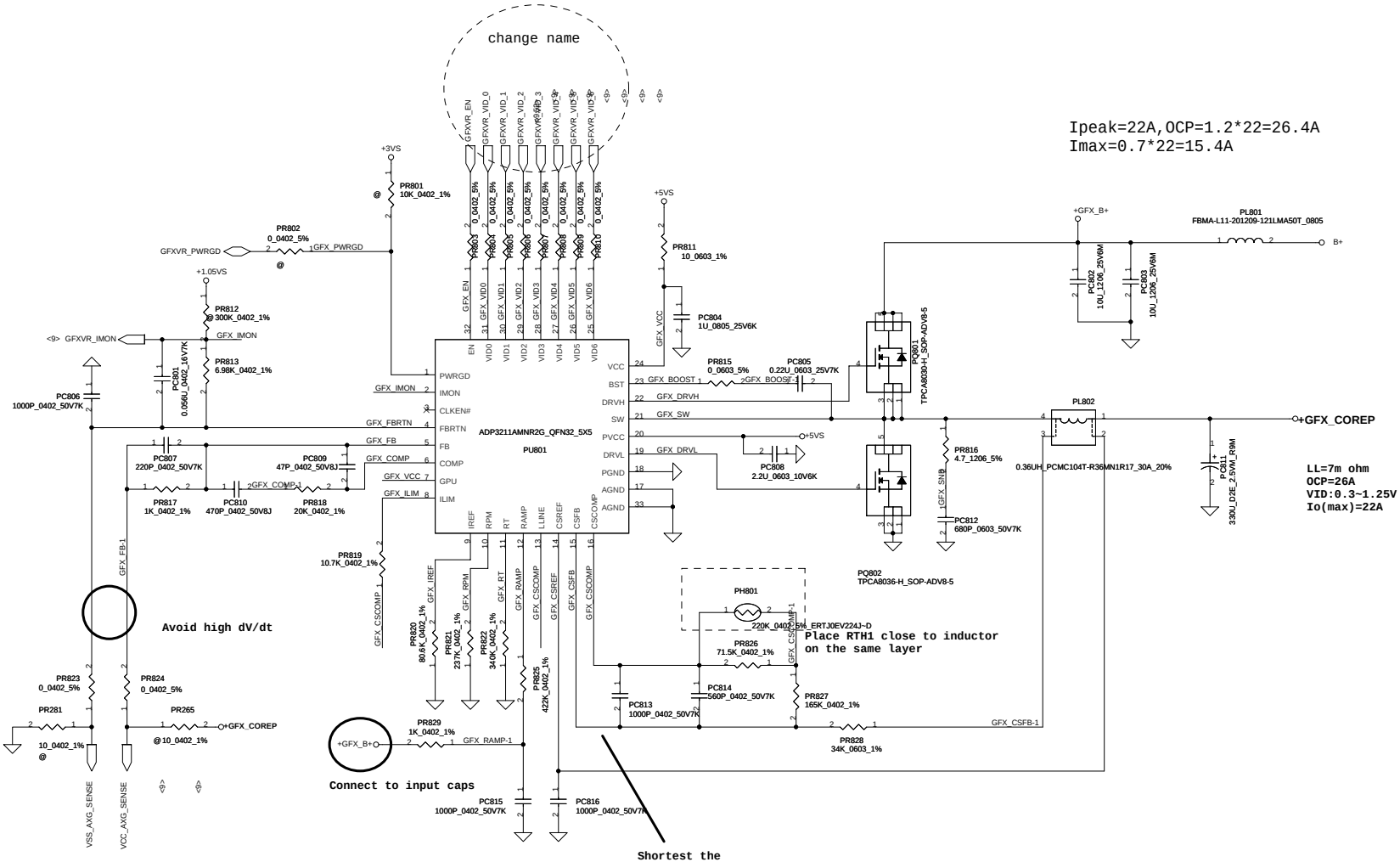

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	can't use PWM to control brightness.	use PCH to control brightness in all SKU.	0.2	22	remove U47, R861,C825; U48; add R844, R827	01/30	DVT
2	Cost down	Cost down	0.2	23	Change Y6 from SJ100002600 to SJ114P3M730	01/30	DVT
3	Cost down	Cost down	0.2	20,21	change D7 and D15 to SCS00003H00	01/30	DVT
4	Cost down	Cost down	0.2	22	delete D18 , change R311 from 4.7K to 10K and pull down to GND.	01/30	DVT
5	Cost down	Cost down	0.2	22,40	change Q16&Q18 from SB923010020 to SB934130000 (AO3413)	01/30	DVT
6	Cost down	Cost down	0.2		delete C433, C404;C852; C851;C401;C399; C364	01/30	DVT
7	Cost down	Cost down	0.2	9,30	Change R242;R501;R502;R504 from SD00000S000 to SD002000080 (0805 0ohm)		
8	Cost down	Cost down	0.2		delete C339;C336;C334		
9	Cost down	Cost down	0.2	38	delete crystal for EC		DVT
10	Cost down	Cost down	0.2	35	change YL1 from SJ100003300 to SJ125P0M200		DVT
11	Cost down	Cost down	0.2	35	change QL1 from SB000005X80 to SB934130000 (AO3413)		DVT
12	Cost down	Cost down	0.2	41	change U30 from SA005280110 to SA000039E00		DVT
13	Cost down	Cost down	0.2	39,41	change D25&D28 from SC2N202U010 to SC600000B00		DVT
14	EMI Reserved.	EMI Reserved.	0.2	20	Add R865 and R866 on HDMI DDC signals for EMI.		DVT
15	EMI&ESD Reserved.	EMI&ESD Reserved.	0.2	39	add D31, D32 and c838.		DVT
16			0.2	22		2/8	DVT
17							DVT
18							
19							
20							
21							
22							
23							

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	ADD PQ64 in BOM	BOM STRUCTURE ERROR	0.1	51	Delete error bom structure	11/12	EVT
2	Battery OTP set	Battery OTP set	0.1	50	Change pr27 from 10k to 33.2k (sd034332280)	11/12	EVT
3	For material EOL issue	For material EOL issue	0.1	51	change pq4,pq5,pq6 from ao4407 to ao4407a (sb00000dl00)	11/12	EVT
4	PH801 part number change	PH801 part number change	0.1	58	change ph801 from sl20000058l to sl200000500	11/18	EVT
5	output voltage unstable	output voltage unstable	0.1	55	change pc129,pc147 from 4.7u to 22u(se000000i10)	11/18	EVT
6	for material shortage issue	for material shortage issue	0.1	51	change pc22,pc23,pc24 from se142475k80 to se000006r80	11/19	EVT
7	For +3valw&5valw enable singal rising time delay	For +3valw&5valw enable singal rising time delay	0.1	52	change pr23 from 100k to 806k(sd014806380)	11/25	EVT
8	cost down	cost down	0.1	52	del pr830(sd034300080)	11/25	EVT
9	Not need	cost down	0.1	50	del pr22(sd034100180)	12/08	DVT
10	cost down	cost down	0.1	53	change pl11 from 2.2u to 1.8u(sh000008u80)	12/18	DVT
11	cost down	cost down	0.1	49	del pr225,pr226,pr265,pc175	12/24	DVT
12	cost down	cost down	0.1	56	change pq801 from si4686 to tpca8030 (sb00000hl00)	12/26	DVT
13	cost down	cost down	0.1	49	change pr35 from 1206 size to 2512 size (sd000001f00)	12/26	DVT
14	pl3 temperature is too hot when charge	pl3 temperature is too hot when charge	0.1	49	change pl3 from sh00000e300 to sh162100m10	12/26	DVT
15	cost down	cost down	0.1	51	change pq20 from ao4474 to ao4466 (sb00000cg00) UMA	12/26	DVT
16	cost down	cost down	0.1	51	change pq21 from ao4456 to ao4712 (sb00000aj00)UMA	12/26	DVT
17	cost down	cost down	0.1	51	change pl10 from 1.0u to 1.8u (sh000008u80)UMA	12/26	DVT
18	cost down	cost down	0.1	51	change pC85 from 390u to 330u (sf000001g00)UMA	12/26	DVT
19	cost down	cost down	0.1	48,49	change pq3 ,pq10,pq55,pq57,pq64 to sb000006800	01/21	DVT
20	for material shortage issue	for material shortage issue	0.1	56	change pq31 ,pq26,pq44,pq38,pq802 to sb00000hr00	01/21	DVT
21	for material shortage issue	for material shortage issue	0.1	47	change pd2 ,pd3,pd10 to sc100001y80	01/21	DVT
22	for material shortage issue	for material shortage issue	0.1	49	change pd7 ,pd18,pd20 to scs00000z00	01/21	DVT
23	for material shortage issue	for material shortage issue	0.1	48	change pd1 to sc400001200	01/21	DVT

Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	for material shortage issue	for material shortage issue	0.1	50	change pd6 to sc400001300	01/21	DVT
2	for material shortage issue	for material shortage issue	0.1	49	change pd11,PD15 to scsh715f080	01/21	DVT
3	for material shortage issue	for material shortage issue	0.1	51	change pl17,pl19,pl15,pl802 to sh000005680	01/21	DVT
4	cost down	cost down	0.1	56	change pl16 to sm010020720	01/21	DVT
5	Change 1.1vsp power level from 1.0v to 1.1v	vga chip change from madison to M96	0.1	54	change pr160 from 1.07k to 1.47k(sd000009480)	1/29	DVT
6	ME interface	ME interface	0.1	49	change pr35 from 2512 size to 1206 size	1/29	DVT
7	OCP SETTING	OCP SETTING	0.1	52	change pr125 from 3.74k to 5.11k in UMA sku, change pr125 from 3.74k to 4.02k in DIS sku	2/2	DVT
8	OCP SETTING	OCP SETTING	0.1	51	change pr101 from 12.7k to 18k in UMA sku, change pr125 from 12.7k to 14.7k in DIS sku	2/2	DVT
9	TPCA8036(PQ38,PQ44) have OTP risk in Clarksfield SKU	TPCA8036(PQ38,PQ44) have OTP risk in Clarksfield SKU	0.1	55	change pq38,pq44from TPCA8036 to TPCA8028 in DIS sku	2/4	DVT
10	For madison voltage level change	For madison voltage level change	0.1	54	change pr151 from 10.2k to 9.53k(sd034953180)	2/5	DVT
11	For madison voltage level change	For madison voltage level change	0.1	54	change pr155 from 20.5k to 31.6k(sd034316280)	2/5	DVT
12	For madison voltage level change	For madison voltage level change	0.1	54	change pr149 from 38.3k to 68.1k(sd034681280)	2/5	DVT
13	For madison voltage level change	For madison voltage level change	0.1	54	change pr145 from 4.7k to 4.99k(sd034499180)	2/5	DVT
14	HW sequency request	HW sequency request	0.1	53	change pr199 from 200k to 150k for M96 VGA chip(sd034150380)	2/23	DVT
15	HW sequency request	HW sequency request	0.1	53	change pc177 from 0.22u to 0.1u for M96 VGA chip(se076104k80)	2/23	DVT
16	H_vttpwrgd glitch issue	H_vttpwrgd glitch issue	0.1	52	change PU500 pin14 pull high voltage from +5vs to +5valw	3/22	PVT
17	fix ki for all 030 project	fix ki for all 030 project	0.1	49	change pr269 from 80.6k to 150k(sd034150380) change pr260 from 100k to 140k(sd034140380)	3/29	PVT
18	fix kv for all 030 project	fix kv for all 030 project	0.1	49	change pr274 from 15.4k to 18.2k(sd034182280)	3/29	PVT
19	for IMON setting	for IMON setting	0.1	55	change pr55 from 4.53k to 5.36k, pc174 from 0.1u to 0.068u in UMA SKU	04/1	PVT
20	for RPM frequency setting	for RPM frequency setting	0.1	55	change pr174 from 47.5k to 69.8k,	04/1	PVT
21			0.1	47		01/21	DVT
22			0.1			01/21	DVT
23			0.1			01/21	DVT

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